

THE DESIGN OF HIGH-VOLTAGE PLANAR TRANSISTORS
WITH SPECIFIC REFERENCE TO THE COLLECTOR REGION

by



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PREFACE

The experimental and theoretical research described in this thesis was carried out by the author in the Semiconductor Technology Laboratory of the Microelectronics Department of the National Electrical Engineering Research Institute (NEERI) of the South African Council for Scientific and Industrial Research during the period January 1979 to April 1984. Work in this laboratory was performed under the supervision of Dr T C Verster, Director, NEERI.

These studies represent original work by the author and have not been submitted in any form to another University for any degree. Where use was made of work carried out by others, it has been duly acknowledged in the text.

Furthermore, as the tasks undertaken involved four major organizations, any comment on or criticism of any of these bodies, either direct or inferred, represents the personal view of the author alone and not an official view of any of these organizations.

Signed

S.A. Smithers

Date

8th June 1984

DEDICATION

For my wife Shirley and our children, Sheryl and Gregory

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I should like to thank Dr K F Poole, Post Office Professor of Micro-electronics at the University of Natal in Durban, for his very able guidance over a period of four years. Professor Poole gave unstintingly of his time and experience, particularly during the vital phase of the preparation of the final text. His approach to the numerous points of discussion was always positive, and this was a great stimulus to the author.

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Mrs G Juran of the Technical Services Department of the CSIR turned sketches and computer plots into the works of art that they are, suitable for publication as parts of this thesis.

Without the willing and able assistance of the persons named in the following list, the development of the high-voltage transistors would not have been brought to a successful conclusion and it would not have been possible to complete the research reported on.

LIST OF PERSONS WHO CONTRIBUTED TO THE TRANSISTOR
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Mr D Meyer	(Quality Assurance)
Mr A Penderis [‡]	(Manager)
Mr N Schoop [‡]	(Process Engineering)
Mr J Stulting	(Manager)
Mrs S Wittstock	(Production Supervision)

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Mrs J Harris [‡]	(Electron Microscopy)
Mr J T Thirlwall	(Electron Microscopy)

CONTINUATION OF LIST OF PERSONS WHO CONTRIBUTED TO THE
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Department of Posts and Telecommunications

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Mr J Breytenbach	(Development and institution of quality assurance auditing procedures)
Mr A Dawson	(Post Office Laboratory : supply of telephometric information)
Mr L S Lochner	(Deputy Director responsible for quality assurance)
Mr M Parsley [§]	(Post Office Laboratory : surge testing of transistors)
Mr J A Raath	(Deputy Director responsible for subscriber equipment)
Mr I C Ramsay [§]	(Senior Director, Engineering)
Mr F Schoombie	(Development and institution of quality assurance auditing procedures)

Messrs Standard Telephones and Cables (SA) Ltd

Mr G Beresford	(Quality Assurance Management)
Mr R Gould	(Director)
Mr M Falk	(Transistor Assembly)
Mr E Paxton	(Components Manager)
Mr V Serrano [§]	(Transistor Assembly)

Messrs Telephone Manufacturers of South Africa (Pty) Ltd

Mr A J Annis	(Technical Manager)
Mr K Hartyani	(Technical Executive)
Mr R Holmes [§]	(Telephone development)

ABSTRACT

THE DESIGN OF HIGH-VOLTAGE PLANAR TRANSISTORS
WITH SPECIFIC REFERENCE TO THE COLLECTOR REGION

The thesis represents a major contribution to the understanding of the design and fabrication of high-voltage planar silicon bipolar transistors, and reports on the original research carried out and the special methods evolved leading to the successful design, development and industrialization of two highly specialized transistors. The development of these transistors, destined for high-reliability applications in subscriber telephone systems, was funded by the South African Department of Posts and Telecommunications.

The first device developed was a discrete transistor meeting the requirements of a singularly difficult specification that included the following.

- An accurately controlled upper limit to quasi-saturation operation, so that above a collector-emitter voltage of 4 V at 60 mA, the device characteristics should be extremely linear.
- An extremely small range of acceptable gains, with lower and upper limits of 80 and 180 respectively.
- Both accurately reproducible and high breakdown-voltages exceeding 200 V.
- The ability to withstand 100 W pulses of 10 μ s duration at a case temperature of 95 °C and a collector-emitter voltage of 130 V.

The second device represents a design and development breakthrough resulting in a unique high-voltage integrated Darlington transistor incorporating the following design features.

- The standard discrete high-voltage transistors used initially in the Darlington application were found to fail frequently due to an external breakdown mechanism under lightning surge conditions, which are common in South Africa. To overcome this weakness, the integrated Darlington incorporates a special clamping circuit to absorb the surge energy non-destructively within the bulk of the device and thereby prevent external breakdown.

- To act as an electrostatic shielding system a new '**inverted metallization structure**' was developed and incorporated in the Darlington transistor design. With this structure it was possible to realize transistors with a combination of extremely high gains, approaching 10^5 , and very low collector-emitter leakage currents, often lower than 1 nA at an applied 240 V, and no device with comparable properties has been reported on elsewhere.

During the development of the integrated Darlington it was recognized that there was a necessity for a simple yet accurate method of predicting quasi-saturation operation. This consideration led to the development of a totally new, user-orientated, graphical model for predicting the gain of a transistor when operating in the quasi-saturation mode : a model involving the use of entirely new yet easily measured parameters. The model was successfully applied to the verification of the Darlington design and the optimization of processing parameters for the device.

Although undertaken in a research environment, the projects were handled under pressures normally associated with industrial conditions. Time schedules were constrained, and this influenced design strategy. As a consequence, however, the need arose to develop fast and efficient design aids since much of the theoretical design was implemented for production without recourse to long-term experimental verification in the laboratory. Whilst the author viewed this approach as less than ideal, the successful production of almost two million of these highly specialized devices, including both types, has lent authority to the design techniques developed.

In spite of the industry-like pressures imposed during the course of the work, many aspects of the development programmes were further investigated and refined by research that would have been omitted had the author accepted the realization of a working device as the only goal. This research has not only contributed to the production of devices of exceptionally high quality, but has also produced a wealth of new information valuable to future designers. These aids include a new and highly accurate correction for the parasitic collector resistance of a transistor; design data for the specification of epitaxial layers for transistors with collector-emitter breakdown voltages ranging between 5 V and 800 V; information on Gate Associated Transistor (GAT) structures; and the entirely new graphical method, mentioned above, for modelling saturation effects in bipolar transistors.

Process development was successfully carried out within the strict confines of compatibility with available equipment, and the pre-requisite that the existing production of low-voltage bipolar integrated circuits should in no way be compromised. Successful transfer of the technology, followed by industrialization, has demonstrated the effectiveness of a method developed by the author for the rapid communication and dissemination of appropriate information in a system without precedents for such procedures.

Listed below are other examples showing that useful information was gathered and new techniques developed.

- Emitter-region defects associated with the metallization process were identified.
- Test data were used to monitor project performance and in the development of data management techniques.
- Interaction with the author resulted in the establishment of the first Quality Assurance and Audit function for micro-electronics activities by the Department of Posts and Telecommunications in the Republic of South Africa. The group formed had the authority to handle the certification of semiconductor capabilities and the qualification for service of semiconductor components.
- An entirely new continuous failure analysis programme was introduced covering both the products manufactured and similar types from other sources : a programme that has brought to light the major failure mechanisms in the high-voltage transistors.

On the basis of the knowledge gained during the research and development programmes it has been possible to make recommendations, substantiated by preliminary investigations for further original research work on a new type of negative-resistance high-voltage device. This would initially be destined for use in subscriber telephones to improve their immunity to surges, and it would form the basis of the development of a totally new type of interface circuit with in-built protection against surges, for application at the subscriber line interface in electronic exchanges.

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LIST OF PRINCIPAL SYMBOLS

A_{dr}	: collector active area of the driver transistor in the integrated Darlington transistor
A_C	: total area of the collector region of a transistor
A_E	: area of the emitter of a transistor
A_{eff}	: corrected area of the active collector region of a transistor
A_{out}	: collector active area of the output transistor in the integrated Darlington transistor
BV_{CBO}	: collector-base breakdown voltage with the emitter open
BV_{CBS}	: collector-base breakdown voltage with the emitter and base shorted
BV_{CEO}	: collector-emitter breakdown voltage with the base open
BV_{EBO}	: emitter-base reverse breakdown voltage with the collector open
C	: constant in the gain droop equation 4.4E (page 131)
D	: constant in the gain droop equation 4.4E (page 131)
E_a	: an empirically determined activation energy
E_g	: the band-gap of silicon
E_p	: peak field at the avalanche voltage in silicon
h_{FE}	: common emitter current gain measured at a given V_{CE} and I_C
h_{FE1}	: h_{FE} of the driver stage in a Darlington pair
h_{FE2}	: h_{FE} of the output stage in a Darlington pair
h_{FEM}	: the peak common emitter current gain, termed the 'Process Gain' for modelling purposes
h_{FED}	: common emitter current gain of the integrated Darlington transistor
I_B	: bipolar transistor (DC) base current
I_C	: bipolar transistor (DC) collector current
I_{CBO}	: collector-base leakage current at a fixed applied voltage; emitter open
I_{CBS}	: collector-base leakage current at a fixed applied voltage; base and emitter shorted
I_{CEO}	: collector-emitter leakage current at a fixed applied voltage; base open

LIST OF PRINCIPAL SYMBOLS (CONTINUED)

I_{CEO1}	: collector-emitter leakage current of driver transistor in a Darlington pair; base open
I_{CEOCL}	: I_{CEO} of the clamp transistor in the integrated Darlington
I_{CO}	: value of collector current at cut-off voltage (V_{CO})
I_{E1}	: emitter current of the driver transistor in a Darlington pair
I_{EBO}	: emitter-base leakage current at a fixed applied voltage; collector open
I_K	: knee current or critical current above which gain droop was included in the modelling calculations : equivalent to the knee current used in 'SPICE' modelling only when measured at $V_K = I_K \times R_C$
I_{QS}	: 'quasi-saturation current', a new concept introduced
J_C	: collector current density
J_K	: knee current density above which the gain droop equation was used
k	: Boltzmann's constant
K	: a constant used in computing V_{BE2}
K_1	: a device temperature constant in Figure 4.15 (page 141)
K_2	: a device temperature constant in Figure 4.15 (page 141)
K_3	: a device temperature constant in Figure 4.15 (page 141)
K'	: Breakdown voltage incremental factor for the Gate Associated Transistor
ℓ	: a device constant used as $kT/\ell q$ in equation 4.6A for calculating V_{BE2}
L	: channel length in the Gate Associated Transistor
L_E	: emitter periphery
N	: an N type region
N'	: the ratio between the area of the integrated Darlington output device and that of the driver
N_+	: a highly doped N type region
N_-	: a lightly doped N type region : normally the epitaxial layer
PC	: the process constant, the ratio R_{QS}/R_C

LIST OF PRINCIPAL SYMBOLS (CONTINUED)

q	: electronic charge
r_{epi}	: resistivity of the epitaxial layer
R_{B2}	: base resistance of the output device, used to calculate V_{BE2}
R_{C}	: passive value of the resistance of the collector epitaxial layer for a given active area
R_{C1}	: R_{C} value of driver transistor in Darlington pair
R_{QS}	: 'quasi-saturation resistance', a new concept introduced
R_{S}	: resistance seen via the collector terminal of a transistor operating in saturation
R_{T}	: resistance of a silicon resistor at temperature T
R_{300}	: resistance of the same silicon resistor at 300°K
S	: gate spacing in the Gate Associated Transistor
T	: temperature in degrees Celcius or, if indicated, absolute temperature in degrees Kelvin as in kT/q
T_{CASE}	: case temperature of transistor
t_{epi}	: thickness of the epitaxial layer
V_{BE}	: base-emitter (DC) voltage
V_{BE2}	: base-emitter voltage of the output transistor in a Darlington pair
V_{CE}	: collector-emitter (DC) voltage
V_{CE1}	: collector-emitter voltage of the driver transistor in a Darlington pair
V_{CEK}	: collector-emitter knee voltage as defined for the PTO14 transistor in the TR2 - Issue 3 specification
$V_{\text{CEO(SUS)}}$: collector-emitter sustaining voltage with base open
V_{CO}	: collector cut-off voltage, a new concept introduced
V_{CT}	: conduction threshold voltage at which transistor operation ceases - approximately kT/q (about 25mV)
V_{E}	: Early voltage
V_{K}	: knee voltage : V_{CE} value at transition from normal to quasi-saturation operation, i.e. $V_{\text{K}} = R_{\text{C}} \times I_{\text{C}}$ (Note : Although quantifying the same effect, V_{K} and V_{CEK} are not equivalent.)
V_{QS}	: 'quasi-saturation voltage', a new concept introduced
V_{TO}	: collector-emitter voltage for a Lambda Bipolar Transistor (LBT) above which the collector current falls
W_{D}	: depletion width of the lightly-doped region of an abrupt junction diode at the ideal breakdown voltage.

LIST OF PRINCIPAL ABBREVIATIONS AND ACRONYMS

BIP	:	'bipolar' transistor
CSIR	:	South African Council for Scientific and Industrial Research, P O Box 395, Pretoria 0001, Republic of South Africa
DID	:	diffused-in defects
DPT	:	Department of Posts and Telecommunications, Private Bag X74, Pretoria 0001, Republic of South Africa
EBIC	:	electron-beam induced contrast
EDXA	:	electron-dispersive X-ray analysis
EDG	:	edge dislocation grids
EED	:	emitter edge dislocations
E.M.F.	:	electromotive force
EQH	:	equipotential ring
FET	:	field-effect transistor
FP	:	field plate
GAT	:	gate associated transistor
I^2L	:	integrated injection logic
IC	:	(silicon) integrated circuit
IM	:	inverted metallization
IPB	:	impulse push-button dial telephone for loop disconnect dialling
NEERI	:	National Electrical Engineering Research Institute of the CSIR, P O Box 395, Pretoria 0001, Republic of South Africa
NI	:	an integrated Darlington transistor with the stages isolated by an N^+ diffusion
O.N.	:	the 'on-normal' transistor that switches the telephone speech circuit 'on' in the off-hook condition and 'off' during dialling
OXIS	:	oxide isolation technology for integration of high-voltage gated diodes

LIST OF PRINCIPAL ABBREVIATIONS AND ACRONYMS (CONTINUED)

- PCM : pulse code modulation used in the digital transmission of data within and between telephone exchanges
- Potelin : Post Office Telectronic Institute, Private Bag X74, Pretoria 0001, Republic of South Africa
- PT014 : discrete high-voltage transistor developed for the Protea telephone (stands for 'Post Office Transistor number 014, where the digits 014 are taken from the NEERI die code */014)
- PT018 : integrated Darlington transistor developed for the buffer stages of the impulse push-button dial telephone manufactured for the S A Department of Posts and Telecommunications (the origin of the type number is the same as for the PT014, above, the NEERI die code was */018)
- Pte/PVT. : abbreviations used for 'Private' in Private Bag
- RI : an integrated Darlington transistor with the stages isolated by spatial separation in the high resistivity collector epitaxial layer
- SA : (Republic of) South Africa or South African
- SAPO : South African Post Office : see DPT above
- SEI : secondary electron image
- SIT : static induction transistor
- SLIC : subscriber line interface circuit
- SPICE : simulation program for integrated circuit engineering (developed at the University of California, Berkeley)
- STC : Standard Telephones and Cables (SA) Ltd, P O Box 286, Boksburg 1460, Republic of South Africa
- TM : Telephone Manufacturers of SA (Pty) Ltd, P O Box 906, Springs 1560, Republic of South Africa
(or TMSA)
- VDR : voltage dependent resistor.

FOREWORD

'Why,' said the Dodo (to Alice), 'the best way to explain it is to do it.'

The truth of these words was indeed borne out many times over while the high-voltage transistors were being developed and manufactured : it was only by doing that it became possible to understand and explain.

The course taken could be likened to travelling an unknown road in a foreign land to a known destination : the map and road signs were inadequate, and the road was found to be rough and precipitous, with unexpected roadblocks; seldom was there time to stop and look for another and better route : it was essential to blunder past the roadblocks, since the course had been chosen and could not be changed for fear of delays or the necessity of having to turn back. In the end the trip would be completed successfully, much about the route having been learned that would be of benefit to others were it to be documented.

It was thus with the work described in this dissertation : the components were successfully developed and put into production, often after feverish efforts to overcome inexplicable phenomena. Understanding steadily grew, sometimes only maturing after long periods, and with the continued research effort came the ability to improve on what were already adequate components, or the possibility of designing new and better devices, should the need arise.

This thesis presents many original 'navigational aids' and it is the hope of the author that they will be of use to others who may have to traverse a similar technological route.

CHAPTER 1

MICRO-ELECTRONICS ACTIVITIES IN THE REPUBLIC OF SOUTH AFRICA

1.1 SUMMARY OF CHAPTER

The main purpose of this chapter is to outline the historical background of micro-electronics in South Africa in order to assist the reader to appreciate the facilities by means of which were developed the transistors described in the succeeding chapters. The lack of pertinent design information in the literature on discrete devices made it necessary to undertake the very thorough and wide range of investigations that formed the core of the research work reported on in this thesis.

1.2 THE HISTORICAL PERSPECTIVE OF MICRO-ELECTRONICS IN SOUTH AFRICA

Today, a successful micro-electronics operation is inseparable in concept from the mass-manufacture of highly complex and sophisticated electronic devices and systems. However, in the historical context this did not apply to the first venture into semiconductor device operations in South Africa. In 1963, at the site of Messrs Standard Telephones and Cables SA Ltd in Boksburg, a facility was established for assembling silicon transistors for use in the telecommunications industry (Paxton, pers. comm.[§]) the capability probably being introduced to enhance the 'local content' of electronic systems for telecommunications. The 'local content' concept was an incentive based on 'import tariff protection' and introduced to stimulate South African industries to undertake operations that would otherwise be financially unattractive; in the telecommunications field this also meant the preferential selection of systems incorporating locally-produced components. It is certain that numerous advanced capabilities now available in the country were established as a result of the scheme.

This move into the assembly arena in 1963 formed the springboard from which the technology for the fabrication of planar silicon devices was introduced into the country in 1968, with the establishment, on the same site, of a facility for diffusing small-signal bipolar transistors. From this time onwards there has been an increasing involvement in silicon technology in the country as the potential benefits have been ever more widely recognized.

§E Paxton (1984) Standard Telephones and Cables SA Ltd, P O Box 286, Boksburg

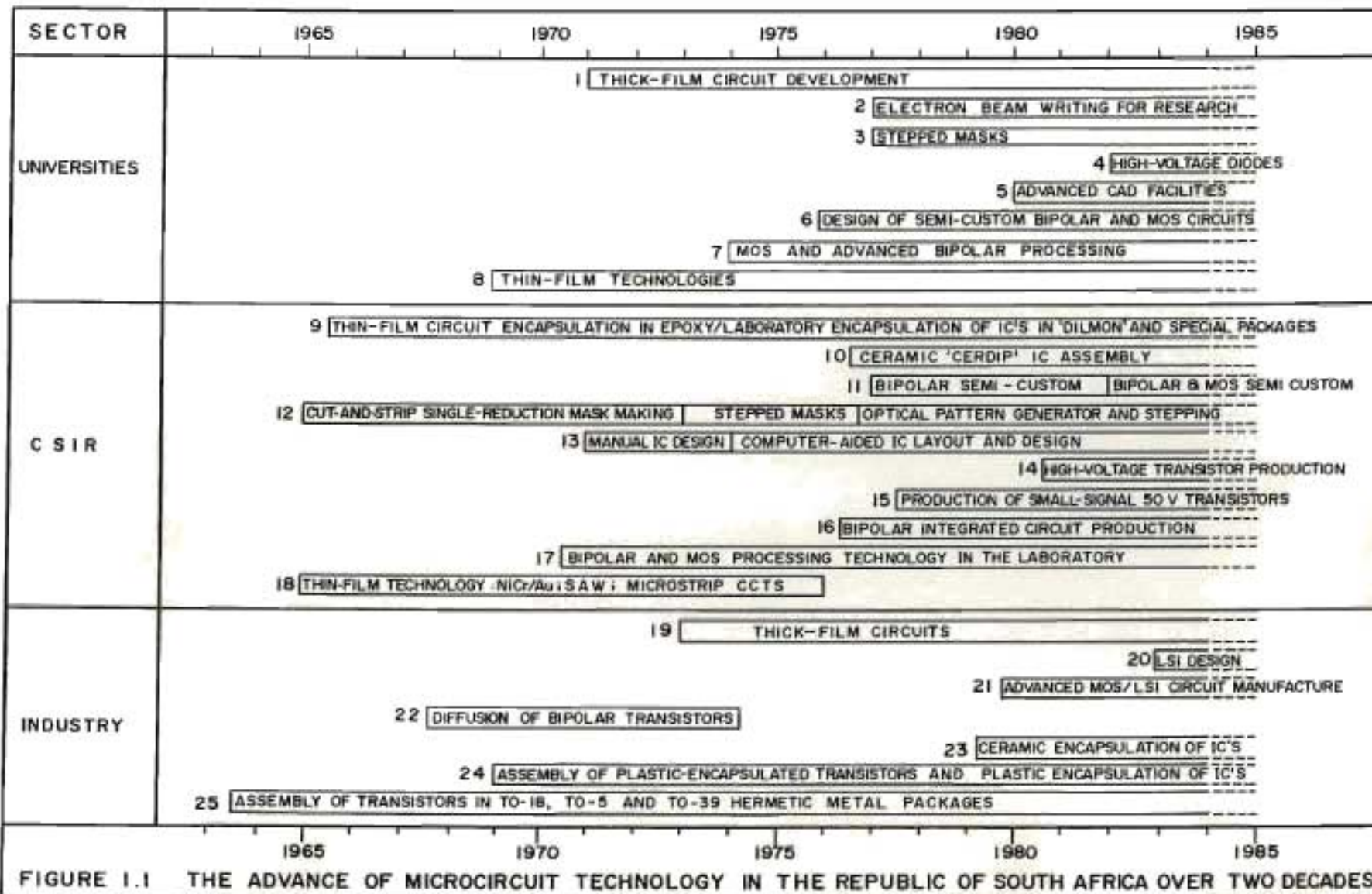
The South African Council for Scientific and Industrial Research (CSIR) was the first research organization in the Republic to devote attention to microcircuits embodying more than a single active device. This began in 1965 with investigations into the technology of thin-film circuits. The various aspects of early microcircuit work in the Republic up to 1975 have been covered by Lutsch¹. Figure 1.1 (page 3) summarizes key activities in the microcircuit arena up to 1984, and subdivides the activities amongst Industry, the CSIR and the Universities. Whilst this chart is neither definitive nor comprehensive, certain key features emerge that are enlarged upon in the succeeding paragraphs.

During 1970 the CSIR began to carry out research and development in the field of bipolar microcircuits. After the author had gained valuable insight into the physical operation of bipolar transistors during the successful development of a computer-aided design technique for the class C transistor amplifier (Smithies²), he was responsible in 1971 for the first wholly local design and diffusion of bipolar transistors. During 1973 Stulting (pers. comm.³) designed and diffused the first South African bipolar integrated circuit.

Diffusion of transistors by industry ceased in 1974, probably for economic reasons. The CSIR in 1976 established a small bipolar microcircuit facility at the National Electrical Engineering Research Institute (NEERI) with the specific objective of satisfying the local requirement for non-standard or so-called 'custom' integrated circuits. The operation was relatively small, and capable of handling a maximum of 100 two-inch wafers per week. Attached to the diffusion unit was a small assembly operation that could handle up to about 10 000 fully screened ceramic 'CERDIP' packages, of all sizes, per annum. No considerable expansion of this facility was planned, as it was envisaged that should large-scale local production of bipolar integrated circuits become necessary, it would be the task of the industrial sector to provide for this.

The infrastructure necessary for the CSIR operation was set up during the early 1970s, and by the end of 1976 designers had available a computer-aided mask layout system feeding an optical pattern generator, used in conjunction with a step-and-repeat camera having a 14 mm field, for chrome photomasks. From 1975, circuit simulation programs such as

³J D Stulting (1984) IC Facility, NEERI, CSIR, P O Box 395, Pretoria 0001,



'SCEPTRE' and later 'SUPER*SCEPTRE', developed at the University of South Florida, were available for integrated circuit design. It was only in 1980, after the introduction of both the dedicated integrated circuit simulation programme 'SPICE 2' developed at the University of California, Berkeley, and also the British Post Office 'GAELIC' layout and logic simulation programs that computer simulation of integrated circuit designs became standard practice at the CSIR. At about the same time the Universities and Industry started to make use of the CSIR facilities.

During 1980 a second microcircuit facility came into operation : South African Micro-electronic Systems (SAMES), dedicated to the mass-production of complex MOS integrated circuits, primarily for the telecommunications industry. This company, set up from public funds, has the ability to handle some 1 000 three-inch wafers a week, and a large assembly capability for both ceramic and plastic packages. SAMES has enabled many local workers in the micro-electronics field to further their horizons in the design of large-scale integrated circuits (LSI) in MOS technology. It has also led to the establishment of a Design Centre for digital integrated circuits, and to the full utilization and planned expansion of the mask-making facility at the CSIR.

It is clear then that with a small but versatile bipolar integrated circuit capability, and a much larger MOS capability available in the Republic, it was now possible to realise a very wide range of integrated circuit designs.

1.3 DISCRETE DEVICE MANUFACTURE

Although the South African commercial assembly operations for discrete devices have flourished from the outset, after having started with small-signal transistors and following these by diodes and later even power semiconductors such as rectifiers and thyristors, commercial diffusion of bipolar transistors ceased in 1974, as was pointed out earlier.

During 1977, soon after the establishment of the NEERI Integrated Circuit Facility (IC Facility) it was found that the volume of custom-designed integrated circuits was small, and that a suitable 'base load' was required for the Facility to help stabilize production processes. The manufacture of small-signal BC107 NPN transistors, with a maximum voltage rating of 50 V, was successfully introduced to form this 'base load'. These transistors were produced using a modified design layout supplied by

another manufacturer, and a number of process steps similar to a 20 V integrated circuit process then in use. The BC107 transistors had a total die area of about $0,25 \text{ mm}^2$ and the production level soon exceeded one million per annum, and yet this comprised only about 300 wafers. These transistors were automatically probe-tested at the CSIR and then shipped to the assembly plant, where the wafers were back-lapped, gold sputter-coated and, after scribe-and-break, assembled into TO-18 hermetic metal packages. This procedure was continued until the beginning of 1984, when the CSIR took over the back-lapping and gold-sputtering operations.

Throughout the whole period of both integrated circuit and transistor manufacture in South Africa all the silicon wafers, both plain and epitaxial, have been imported from various overseas manufacturers, as the local silicon industry was geared only to the production of industrial-grade material (Delaney³). The feasibility of producing solar and semiconductor grade silicon from the local industrial grade was investigated by Stander⁴, but production has never commenced. In the field of process gases the local industry has been well catered for, and all standard semiconductor grade carrier gases are manufactured locally (Beal⁵).

1.4 DEVELOPMENT OF THE HIGH-VOLTAGE DEVICES

From the foregoing it may be seen that in South Africa in 1978 when negotiations with the CSIR to develop a high-voltage transistor commenced, the level of discrete transistor production technology in South Africa was indeed low, but considerable experience had been built up in related fields at NEERI.

As previously stated, the author had designed the first wholly South African bipolar transistor in 1971. Subsequent work on dye-sensitized MOS structures (Smithies et al.⁶) had yielded an excellent insight into surface effects in devices. In 1974 the author⁷ made an important contribution to the technological aspects of the gate-region oxidation process during development of the first P channel MOS integrated circuit in South Africa. A successful investigation of integrated injection logic (I²L) technology carried out by Crooke⁸ in the NEERI Semiconductor Technology Laboratory had yielded considerable insight into both the design of bipolar transistors and the development of the associated process technology.

Owing to the success of these investigations and others not mentioned here, and also in view of the fact that the NEERI Laboratories were adequately equipped, the SA Department of Posts and Telecommunications approached the

Institute with a proposal to develop a highly specialized transistor for use in the 'Protea' electronic telephone. The task set was to produce a suitable high-voltage transistor design and to generate a suitable process technology that could be instituted at the NEERI Integrated Circuit Facility. Two important constraints were imposed on the author, and the first was that any modifications to either processes or equipment in this facility should only be carried out provided no disruption of normal production was caused, and the second was that minimal capital expenditure should be incurred. These difficulties were overcome, and the considerable success of the first high-voltage transistor led to a contract for the development of a second device which was a high-voltage integrated Darlington transistor.

1.5 THE ORDER AND WEIGHTING OF MATERIAL PRESENTED IN THIS THESIS

The major contributions to micro-electronics yielded by the development programmes was that they clarified understanding of the effects of the collector region resistance, and enabled an improved design methodology to be developed for planar high-voltage transistors where internal and external effects are important, either singularly or in combination. This then forms the mainstream of the thesis and the findings are presented in Chapters 2 and 3. Chapter 4 presents a totally new concept of modelling saturation effects, making it possible for the first time to readily compute the contribution of collector region resistance.

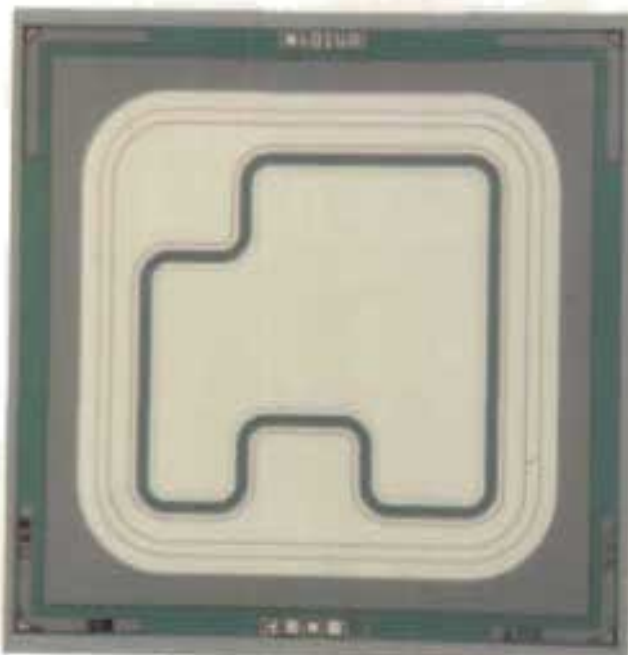
Chapter 5 is intended to demonstrate the broad base on which the projects were undertaken and, after an assessment of the capabilities available compared to those required, the processes developed are discussed. Development of the process technology required both experience of processing techniques and an insight into the nature of the physical and chemical processes involved. Much of the process development work was based on the individual judgement of the author, and here conformance with the electrical specification and the ability to target device parameters adequately were important factors. Chapter 5 also covers the successful management of the project from the stage when the device and the process technology were developed, through the industrialization phase, to a demonstration of the value of production data management.

Chapter 6 clearly identifies the direction which further original research on high-voltage devices for telecommunications could take, the recommendations being supported by the results of preliminary investigations.

PLATE 1 : THE PROTEA TELEPHONE AND PT014 TRANSISTOR DIE



The Protea rotary-dial electronic telephone with transistorized transmission and tone-call circuitry.



The die of the surge-resistant high-voltage PT014 transistor that was specially developed for use in the Protea telephone. (Die size is 1,27 x 1,27 mm)

CHAPTER 2

DEVELOPMENT OF THE HIGH-VOLTAGE TRANSISTOR TYPE PT014
FOR THE PROTEA TELEPHONE

2.1 SUMMARY OF CHAPTER

The successful development is described of a special high-voltage transistor, the PT014, for the Protea telephone of the SA Department of Posts and Telecommunications; also, and what is perhaps more important, details are given of a number of significant findings made during the investigations carried out as part of the development programme.

The role of interdigitated structures in the emitters of transistors was questioned, and it was experimentally verified that the use of a simple emitter structure with no extension of the periphery was better suited to the PT014 application. For calculating the collector region resistance, it was proposed that a simple, new correction for the active area of a transistor be used; the accuracy of this procedure was experimentally verified. A simple relationship between maximum finger spacing in emitter structures and epitaxial layer thickness is also given.

An improved understanding was gained of the critical relationship between the epitaxial layer thickness and resistivity, and breakdown voltages that may be reliably attained in planar double-diffused NPN transistors. Design curves for epitaxial layers, together with instructions for their use, are presented in an entirely new form and have application to devices with collector-emitter breakdowns ranging between 2 V and 800 V.

A new type of planar device structure was investigated, termed the 'Gate Associated Transistor' (GAT), originally developed to increase the available value of BV_{CEO} , and it was found that the published design formulae were inaccurate. Whilst it turned out that the device could provide a worth-while increase in BV_{CEO} , the fact that parameters were to a greater extent dependent on the process of manufacture, and there was a need for a refinement in design technique, precluded the use of the structure for this project.

2.2 BACKGROUND TO THE DEVELOPMENT OF THE TRANSISTOR

2.2.1 Transistor failures in the Protea electronic telephone

A transistorized telephone called the 'Protea' was first brought into service in the Republic by the SA Post Office during the late 1960s. This instrument, compared with earlier non-electronic models, offered a number of advantages including, briefly, improved side-tone rejection coupled with automatic line compensation of the output level, a low-noise, low-distortion speech circuit utilizing a dynamic type microphone transducer, and an electronic tone caller with three selectable output levels.

The Protea was one of the earliest electronic telephones introduced into service anywhere in the world, and it performed admirably, meeting all the performance targets set, with the exception of reliability. Catastrophic failure of one or both of the transistors caused the field failure rate to be more than double that of earlier non-electronic telephones in service. (Bets, Pers. comm. #)

2.2.2 Causes of the transistor failures

At first it was believed that these failures were due to lightning-induced surges, but as failure statistics accumulated it was found by the Post Office that TR2, the transistor which acted as the output transistor in the call-tone oscillator and speech amplifier, was the one that failed most often and that there was no real relationship between this failure rate and lightning frequency.

When the problem was investigated in the Post Office Laboratory by Head⁹ the far-sighted study showed the fault to be related to an incorrect cradle switch sequence. During calling, with an applied 75 V 17 Hz ringing signal from the exchange, the output transistor case temperature could rise to 95 °C, and when the receiver was lifted this could produce a high-power surge of short duration but sufficiently powerful to destroy the transistor.

#B A Bets (1978) Telecommunications Headquarters, Private Bag X74, Pretoria 0001, Republic of South Africa.

To quantify the surge, a scheme similar to that shown in Figure 2.1 (page 11) was used. By applying the ringing signal to sample telephones whilst the cradle switch was being automatically operated, the incorrect switching sequence of the six microswitches was identified. This wrong sequence was the result of ageing of the mechanism. The surge across the collector-emitter terminals of the transistor TR2 reached a value of 130 V at 0,75 A and had a duration of about 10 microseconds. This caused the device either to degrade or fail.

2.2.3 Corrective measures to improve the reliability of the telephone

The manufacturer modified the design so as to ensure maintenance of the correct cradle switch sequence in new telephones, but it was totally out of the question for the Post Office to recall more than one million telephones for modification. The only way to solve the problem with the existing telephones was to specify another transistor, capable of replacing the TR2 and having the ability to withstand the surges that might occur, and to install this substitute transistor in telephones sent in for repair at the country-wide service centres. The new transistor would, of course, also be incorporated in all new telephones.

At this stage negotiations commenced with the CSIR to produce a suitable device locally, and the author, appointed to head the project, was actively involved both with the drawing-up of the final electrical specification for the substitute transistor and the subsequent development programme.

2.3 SPECIFICATION OF DEVICES ABLE TO WITHSTAND THE SURGES

2.3.1 Considerations in specifying a transistor to withstand the surges

As the magnitude of the surges was known, it appeared to be simply a matter of revising the breakdown limits of the transistor and adding a requirement in the specification for surge resistance. Two major problems arose, however :

- (a) there were very few commercially available transistors in TO-5 or TO-39 packages with collector-emitter breakdown voltages between 100 and 250 V; and

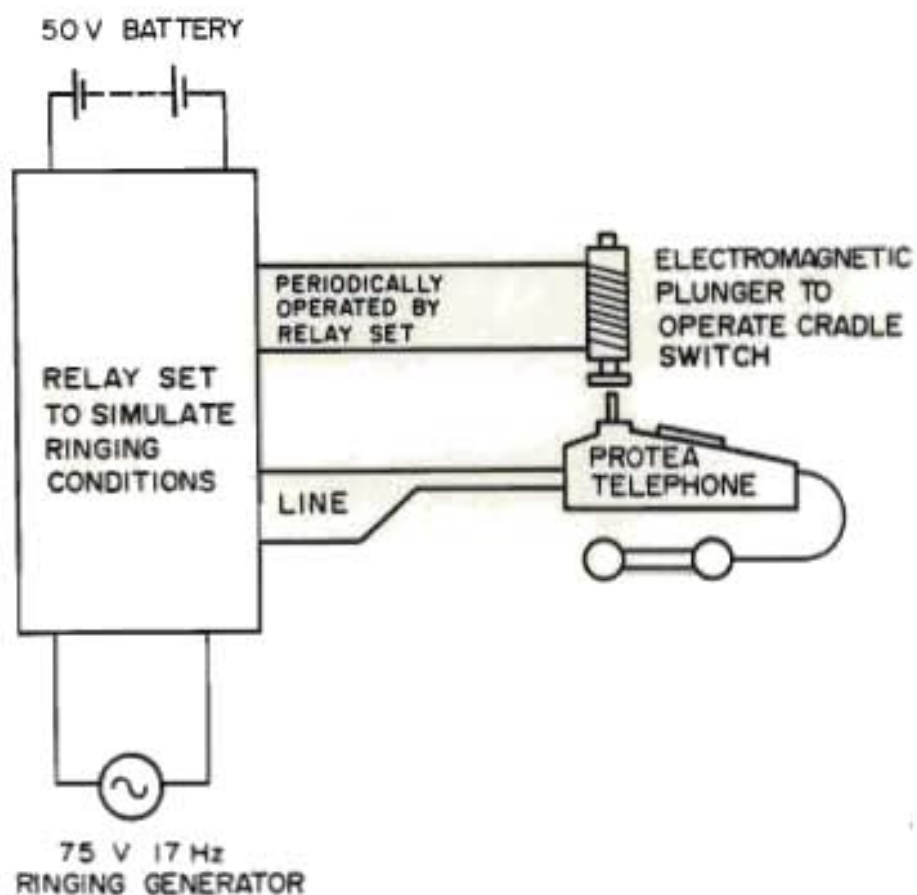


FIGURE 2.1 SIMPLIFIED TEST SCHEME USED IN THE EVALUATION OF THE PROTEA TELEPHONE TO INDUCE LARGE SURGE CURRENTS IN THE OUTPUT TRANSISTOR, TR2. UP TO 20 000 CRADLE SWITCH OPERATIONS WERE CARRIED OUT ON A TELEPHONE. (SOURCE: LABORATORY REPORT 5515 OF THE DEPT OF POSTS AND TELECOMMUNICATIONS, SEPTEMBER 1974)

- (b) transistors of this size with breakdown voltages over 250 V, that were more readily available, generally provided poor linearity at the collector-emitter operating voltage of 4 V and a collector current of 60 mA. This linearity was important, as in the telephone circuit the transistor had a voltage-dependent resistor (VDR) incorporated into the emitter circuit for line compensation purposes. Very frequently, this combination of the VDR and a high-voltage transistor, resulted in an unstable operating point in the off-hook case.

2.3.2 Revised specification for the transistor TR2

The revised specification included two additional tests. These were, first, a surge test, and secondly a test for non-linearity in the low-voltage characteristics; the latter introduced an entirely new parameter, the 'knee voltage', V_{CEK} . Table 2A shows the surge test that was included in the transistor specification.

Table 2A : Surge test for transistor TR2

Parameter	Test Condition	Limit	Unit
$F_2(\text{Pk})$	$V_{CE} = 130 \text{ V}$ $I_C = 0,75 \text{ A}$ dissipation time = 10 μs case temperature = 95 $^{\circ}\text{C}$	100 (min)	W

After a surge under these conditions, the allowable gain drift was only +/- 20 per cent of the originally measured value for the device. A limit of + 100 per cent was set on the change of all leakage currents.

The entirely new concept of a 'knee voltage', V_{CEK} , test was introduced after a further investigation of gain requirements for the transistor had been carried out by the Department of Posts and Telecommunications. In the specification, 'TR2 - Issue 3', reproduced in Appendix 2.1 (page 228), the test values for the knee voltage are given in a form suited to automatic test gear. The nature of this test is shown in Figure 2.2 (page 13).

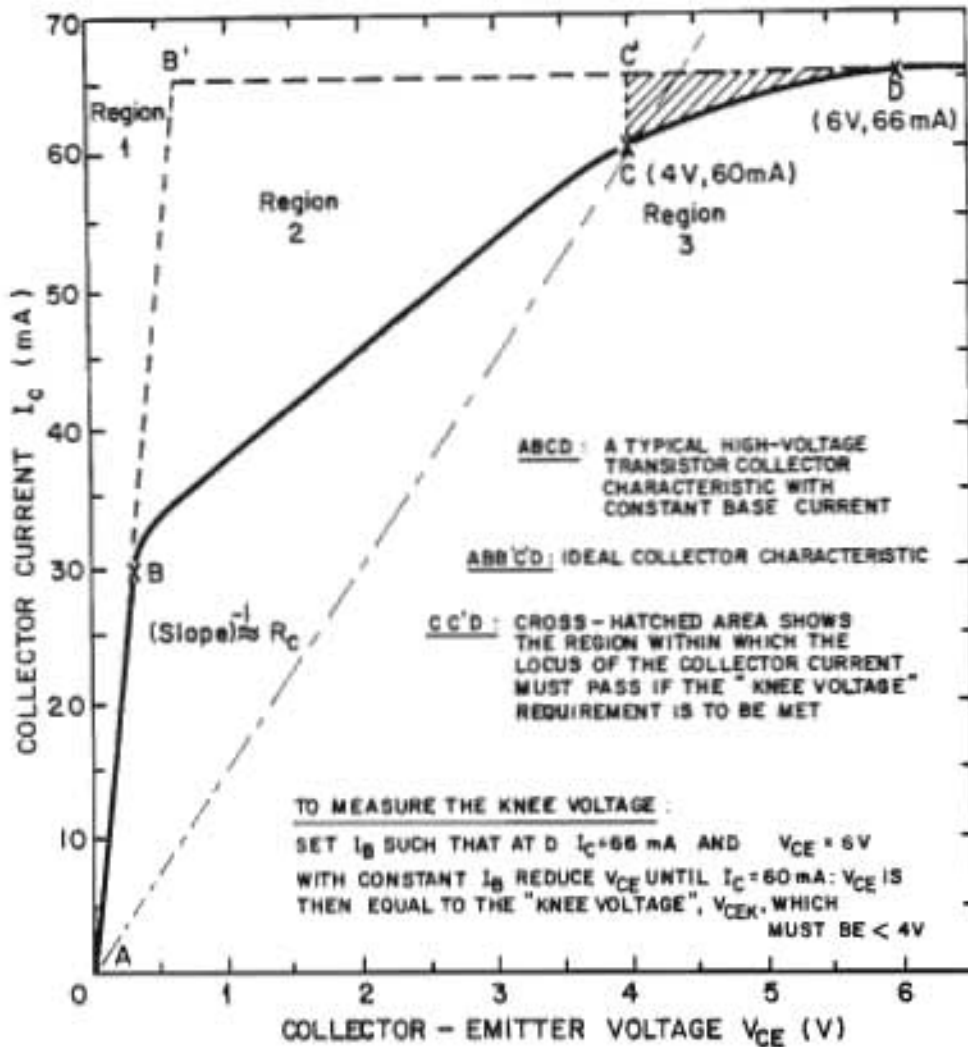


FIGURE 2.2 THE REGIONS OF OPERATION OF A HIGH-VOLTAGE TRANSISTOR AND THE CONCEPT OF THE KNEE VOLTAGE, V_{CEK} , AS DEFINED IN THE TRANSISTOR SPECIFICATION TR2-ISSUE 3.

- REGION 1 : THIS REPRESENTS 'TRUE SATURATION' WHERE THE COLLECTOR IS SATURATED WITH MAJORITY CARRIERS FROM THE EMITTER.
- REGION 2 : 'QUASI-SATURATION' WHERE THE COLLECTOR IS ONLY PARTIALLY SATURATED WITH MAJORITY CARRIERS. BC REPRESENTS THE COLLECTOR CHARACTERISTIC.
- REGION 3 : NORMAL OPERATION WHERE THE OPERATING POINT $V_{CE}/I_C > R_C$ WHERE R_C IS THE RESISTANCE OF THE COLLECTOR REGION AND IS THE INVERSE OF THE SLOPE OF THE LINE AC, TO A ROUGH APPROXIMATION.
- (IN CHAPTER 4 A MORE ACCURATE DEFINITION IS GIVEN FOR R_C)

2.3.3 Transistors invited for evaluation

After the publication of the TR2 - Issue 3 specification, and while the development of the PT014 was still in the embryo stage, the Department of Posts and Telecommunications ordered a thorough evaluation of commercially available transistors that might meet the requirements. In this investigation, carried out by Heesen¹⁰, ten manufacturers submitted a total of one hundred and thirty devices (ten of each transistor type) for evaluation. Subdivided into categories there were nine different die species. The tests carried out were the following.

- (a) Parametric, to meet the basic electrical requirements as given in the TR2 - Issue 3 specification.
- (b) The surge test : 130 V and 0,75 A for 10 μ s at a case temperature of 95 °C.
- (c) A second parametric test to record the parametric changes.

Eight different transistor types containing only four different die species were found to be acceptable. The other devices either failed the initial parametric tests or exhibited unacceptable parametric changes after surging.

2.3.4 Problems with the die available for the local assembly of transistors to meet the specification TR2 - Issue 3

Of the four different die species found to be acceptable, only one, manufactured by Messrs Texas Instruments, was available for local assembly, and a photograph of this die type is shown in Figure 2.3 (page 15). Disadvantages associated with this die were the following.

- (a) High cost (in the region of 20 cents in SA currency).
- (b) Both wafer and die yields low, primarily owing to failure on either the knee voltage or gain test, or both, which failures in turn could be ascribed to the fact that the transistor being tested was not a purpose-made device.

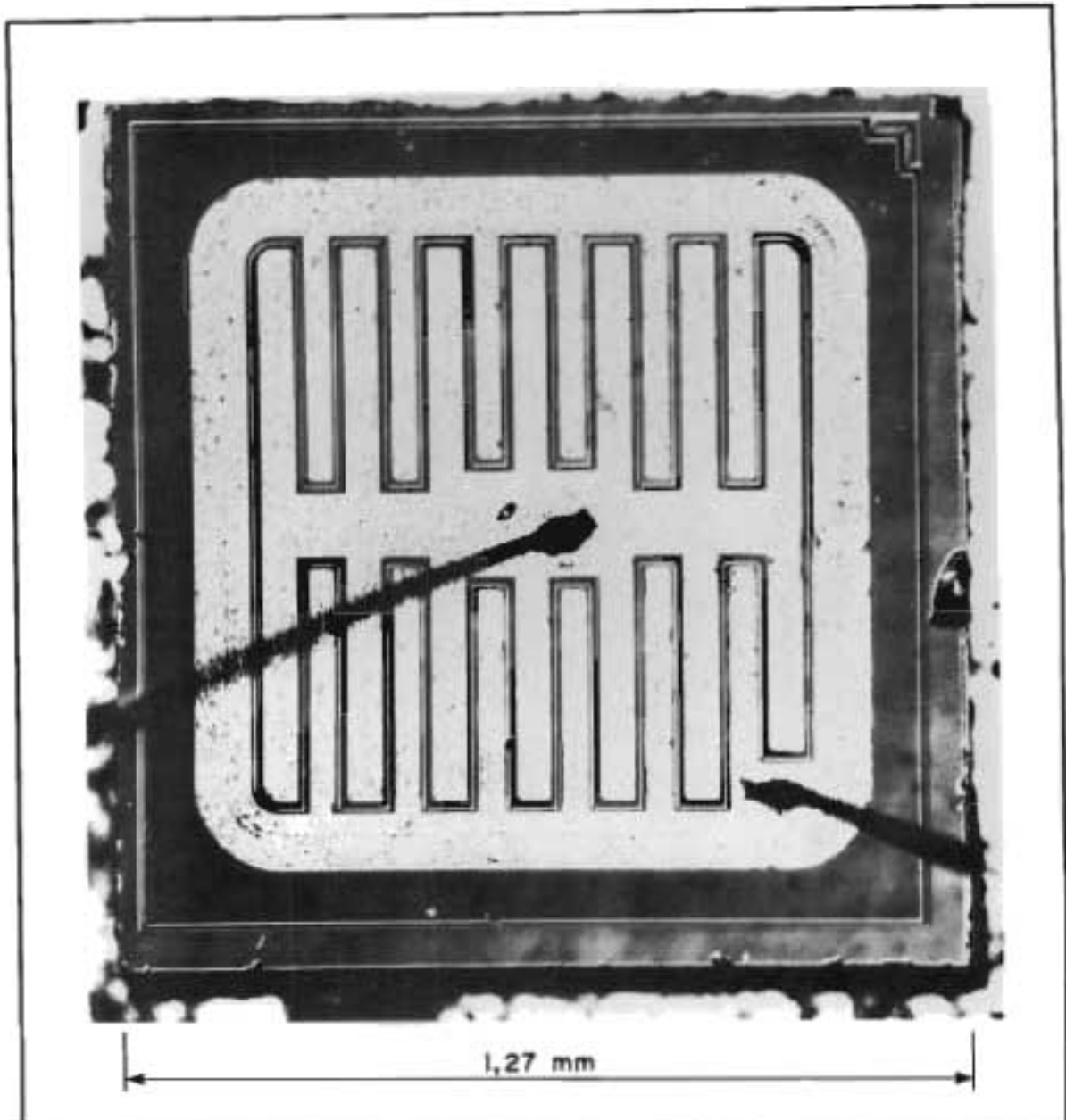


FIGURE 2.3 AN ASSEMBLED TEXAS INSTRUMENTS TRANSISTOR DIE FOR THE TR2 APPLICATION. THE LAYOUT OF THE DEVICE WITH AN INTERDIGITATED EMITTER AND BASE REGION AND THE SMALL CLEARANCE BETWEEN METAL AND SCRIBE CHANNEL IS INDICATIVE OF A DEVICE LAID OUT FOR A LOWER-VOLTAGE APPLICATION WITH HIGHER EMITTER CURRENT DENSITIES THAN REQUIRED FOR THE TR2.

- (c) Bonding pad areas for both the base and emitter too small, as a result of which the surrounding die was frequently damaged during assembly.

The Texas instruments die was used in the telephones during the period the PT014 was being developed.

2.4 THE DEVELOPMENT STRATEGY AND PRODUCTION TECHNOLOGY FOR THE PT014 TRANSISTOR TO MEET THE TR2 - ISSUE 3 SPECIFICATION

2.4.1 Device development proposal

Verster¹¹ proposed that samples of transistors that were known to be satisfactory should be analysed and a 'reverse engineering' exercise be carried out to develop a local equivalent. This approach, which coupled a knowledge of the properties of the die in use to the requirements of the specification, yielded information not only on what should be done but, what was even more important, on what should not be done during the development of the PT014 transistor.

A development period of nine months was proposed by NEERI and this was accepted, together with the estimated cost of the development programme which was underwritten by the Department of Posts and Telecommunications¹². The phases of the development and production programmes for the PT014 are shown in Figure 5.1 (Chapter 5 page 182).

2.4.2 Adoption of a planar device structure

In the investigation by Heeson¹⁰ both planar and non-planar device structures had been shown to be suitable for the device application, and a planar technology was chosen for the PT014 for the following reasons.

- (a) NEERI had no expertise in non-planar, in this case MESA technology.
- (b) The development of a new technology for MESA devices would, in all probability, have taken longer than the adaptation of an existing technology.

- (c) New capital equipment for lapping, polishing and etching for MESA technology would have to be procured for both the development and production phases, which would increase both the lead times and cost.
- (d) Additional staff for production processing and process maintenance would be required.

2.5 DESIGNING THE DEVICE TO MEET THE PRIMARY ELECTRICAL CHARACTERISTICS

The two most important parameters to be met for the TR2 - Issue 3 specification were the collector-emitter breakdown voltage, BV_{CEO} , and the knee voltage, V_{CEK} , as defined in Figure 2.2 (page 13). These critical parameters were coupled with a gain spread requirement of less than 3 : 1, which implied that excellent process control for this single device type was essential for good yields to be realized.

At the stage when this project was undertaken, NEERI had a capability for diffusing small-signal 50 V NPN transistors in a process similar to one that was used for 20 V integrated circuits. This process was not applicable to higher-voltage devices as the junction depths were too shallow and the emitter-base reverse breakdown voltage too low.

Two major areas of the development programme, described in this chapter, are the following.

- (a) The choice of a suitable epitaxial layer to give the breakdown voltages required.
- (b) Layout of the device to provide both a suitable knee voltage, V_{CEK} , and ability to withstand the surge $P_{2(PK)}$.

The process that was developed is described in Chapter 5. In practice it was possible to meet the electrical requirements reliably, with a good yield and a small expected parameter drift during the useful life of the device.

2.5.1 Meeting the breakdown requirements

In a double-diffused transistor, an example of which is shown in the sectional drawing in Figure 2.4 (page 19), the collector epitaxial layer plays a vital role in determining the value of BV_{CBO} and indirectly BV_{CEO} . In devices where BV_{CBO} is less than about 200 V the value does not differ greatly from the ideal value computed for an infinite abrupt junction. At higher voltages, however, the departure from ideal characteristics can be considerable and depends, *inter alia*, on the following.

- (a) The field concentration that occurs at the edge of the diffused area in a finite junction, causing preferential breakdown at lower voltages.
- (b) Surface effects that make the device sensitive to processing and layout. These are particularly important in the areas surrounding a diffusion where lateral depletion takes place.
- (c) A non-homogeneous impurity distribution with localized increased concentrations or precipitations of dopant. This irregular distribution is a greater problem in higher-resistivity silicon substrates and epitaxial layers. (This was one of the prime reasons why neutron transmutation doped silicon was developed for high-voltage devices such as thyristors.)

2.5.1.1 The 'punchthrough diode collector' to control breakdown

A method of providing a stable collector-base breakdown was to generate a preferential breakdown path between the base region and the collector N^+ substrate. By using the principle of the punchthrough diode as described by Ghandi¹³, it was possible to control the collector-base breakdown characteristic by a purely geometrical factor, viz the epitaxial layer thickness. In Figure 2.5 (page 19) the conventional diode is compared with a punchthrough diode structure. The punchthrough structure may be used directly as the collector region of a transistor. Since depletion stretches very much further into the collector region than into the base region, the following discussion will be devoted only to an abrupt-junction model of the collector-base region of the transistor.

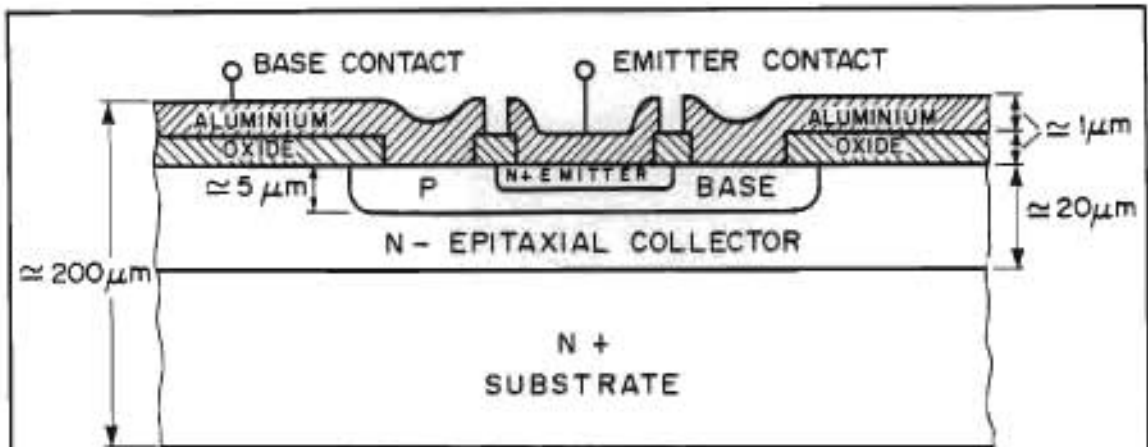


FIGURE 2.4 SECTION OF A TYPICAL LOW-VOLTAGE PLANAR EPITAXIAL TRANSISTOR

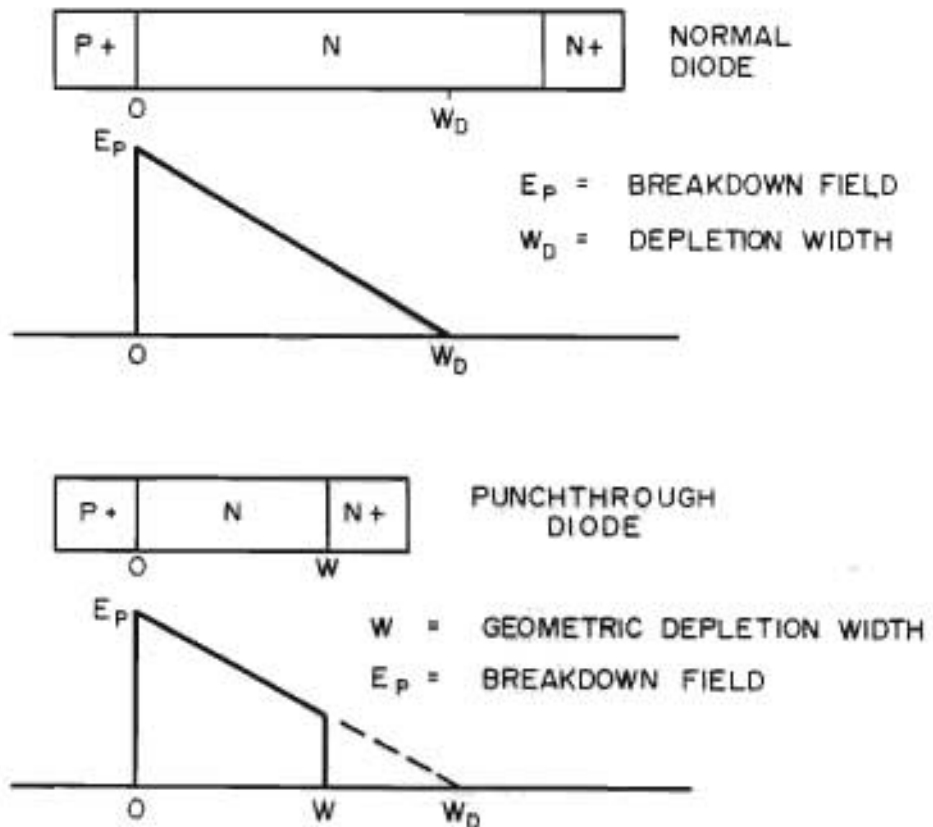


FIGURE 2.5 BREAKDOWN CONDITIONS IN A NORMAL AND A PUNCHTHROUGH DIODE

Other relevant aspects of junction termination are covered in section 2.5.3.

2.5.1.2 Setting the design values for BV_{CEO} and BV_{CBO}

The relationship between collector-base and collector-emitter breakdowns, given by Burger and Donovan¹⁴ as well as Ghandi¹⁵, is as follows :

$$BV_{CEO}/BV_{CBO} = (h_{FE})^{-1/n} \quad \dots\dots\dots 2.5A$$

where

n is a process constant related to the avalanche multiplication factor; Ghandi¹⁶ states that typical values of n range from 3 to 4 for NPN devices;

BV_{CEO} is the collector-emitter breakdown voltage;

BV_{CBO} is the collector-base breakdown voltage;

h_{FE} is the device gain in the linear region.

To obtain a representative value of n for the transistor design to be carried out, the author made a large number of measurements on commercially available high-voltage, medium-power transistors. It was found that values of n ranged from 5 to 7 for the transistors tested, although instabilities in breakdowns frequently precluded reliable results being obtained. During the development programme values of n approximating 5 were obtained.

The TR2 - Issue 3 specification had a lower limit of 130 V for BV_{CEO} , and with 'insets' or safety margins allowed by the transistor assembly plant it was necessary to produce devices with a minimum BV_{CEO} of 160 V. With a gain spread factor of 3 and an assumed value of n = 5, a device with a maximum gain of 210 and minimum BV_{CEO} of 160 V would, if diffused to a gain of 70, and using equation 2.5A, exhibit a BV_{CEO} of 200 V. As it was known that spreads of thickness and resistivity of +/- 20 per cent were common in epitaxial layers, a target figure of 250 V was taken for BV_{CEO} to accommodate such spreads.

To obtain the target value for BV_{CBO} , the value of 250 V for BV_{CEO} was used. As an added safety margin the gain h_{FE} associated with this

value of BV_{CBO} was increased from 70 to 100. Using equation 2.5A again with a value of $n = 5$ the target value for BV_{CBO} was 630 V.

2.5.1.3 Specifying the epitaxial layer thickness and resistivity

For this section reference was made to data from case four of the alternative designs of a 1700 V diode as presented by Ghandi¹⁶. These data were found to be accurate for the purposes of the PT014 design. (For convenience the relevant table is reproduced in Appendix 2.2 on page 229.)

Using the figure of $BV_{CBO} = 630$ V and an optimum avalanche field strength of 165 kV/cm for a punchthrough diode, the thickness of epitaxial silicon required below the base was about 38 μm . Allowing for an 8 μm base junction and about 0,5 μm of silicon to be consumed in oxidation, an epitaxial layer thickness of 46,5 μm was required.

The depletion width W_D at the avalanche field was about four times the geometrical width of the layer in case four, and this criterion was applied to the transistor collector where a geometrical width of 38 μm for the collector implied a depletion width of approximately 152 μm . From the curves of carrier concentration v. resistivity by Irvin¹⁷, as updated by Thurber et al.¹⁸, a resistivity of about 45 ohm.cm was indicated for the N-type epitaxial layer with $W_D = 150$ μm .

2.5.1.4 Experimental verification of the epitaxial layer requirements

The above approach to specifying the epitaxial layer parameters was based on data for a diode with a doping concentration lower by a factor of 3 than that for the transistor it was desired to develop, and it was thus deemed necessary to check these figures experimentally. Two epitaxial layer types with a nominal layer thickness of 45 μm were evaluated. The first layer type had a resistivity in the range 20-33 ohm.cm and the resistivity of the second was in the range 33-50 ohm.cm. With the lower resistivity layer, collector-emitter breakdown voltages of between 120 and 180 V were measured, and on the 33-50 ohm.cm material, values of about 260 V were obtained for the gains in the region of 100. In addition, a BV_{CBO} value of approximately 600 V was obtained on the higher-resistivity material. Agreement with the projected figures was thus excellent.

After negotiations with the silicon manufacturer the final epitaxial silicon specification, which is reproduced in Appendix 2.3 (page 230), was agreed to and the allowed layer thickness spread was from 38 to 52 μm , this being associated with a resistivity spread of from 33 to 50 ohm.cm.

2.5.2 Test transistors : Merit of an interdigitated structure

The device that had been accepted for local assembly was an interdigitated structure 1,27 mm x 1,27 mm in size. The value of this type of structure in the PT014 application was questioned, for the following reasons.

- (a) Interdigitated structures are generally used to assist in providing a more uniform current distribution across the emitter region of a transistor at high injection levels of typically $> 1 \text{ A/mm}^2$, but the specification did not call for such high injection levels.
- (b) Numerical analyses have indicated that for optimum effect the width of the stripes should not be greater than about 10 to 14 times the base width (Ghandi¹⁹). The device to be developed would have a base width of about 2 μm and this would certainly lead to a far denser finger structure than the one used in the Texas Instruments die. Samples of the TI die were lapped and stained and found to have a base width of about 2 micrometres.
- (c) The effect of a highly resistive collector region on the requirements for the design of an interdigitated structure had not been considered in the literature.

2.5.3 Junction termination

Published information located at this stage of the project mainly covered the design of junctions with a view to optimizing the internal field distribution. The problems associated with the junction termination of a 250 V transistor were apparently not considerable, and data from Ghandi²⁰ were used in the design of the test transistors.

The first feature included in the transistors designed was a field Plate (FP) structure. The FP structure is a metallization layout measure commonly used to spread depletion near the edge of a diffused junction. The action of an FP is shown in Figure 2.6 (page 24) and it is apparent that excessive field concentration around the edge of the diffused junction is reduced considerably. The FP structure was used as it provided an easy method of obtaining an almost ideal abrupt junction approximation in transistors with a punchthrough collector design. In the devices that were developed, an overlap of 20 μm of aluminium over the base junction diffusion window was used. For production an overlap of 36 μm was adopted and the test geometries used on the production layout to optimize the overlap are described in Section 2.5.6.

The second feature included in the transistor designs was a diffused N-type equipotential ring (EQR), included in the collector region surrounding the transistor structures, as shown in Figure 2.6 (page 24). The EQR provided a precise boundary to terminate lateral depletion around the base junction, thus ensuring stable and repeatable junction breakdown. As the potential gradient across the oxide between the base metallization and the EQR was established rapidly, stability with regard to the external field was ensured.

The clearance between the FP metallization and EQR was important and, to prevent external discharge, a critical external field strength of 4,3 V/ μm , as measured by Zoroglu and Clark²¹, was used to determine the minimum FP to EQR clearance for a value of BV_{CEO} of 300 V. This gave a figure of 70 μm . In the prototype devices a conservative figure of 80 μm was used. This was increased in the production geometry to ensure a stable BV_{CEO} characteristic as well.

2.5.4 Layout of the prototype devices

The primary limit on the area of the transistor to be developed was the collector resistance, which had to be low enough to meet the knee voltage requirement. For the specified knee voltage of 4 V at 60 mA, the maximum permissible collector region resistance was $4/0.06 = 66$ ohms. With 38 μm of 45 ohm.cm epitaxial silicon below the base region of the transistor, the minimum active area required was

$$A_{\text{min}} = 100 \times (45 \times .0038) / 66 = 0,26 \text{ mm}^2.$$

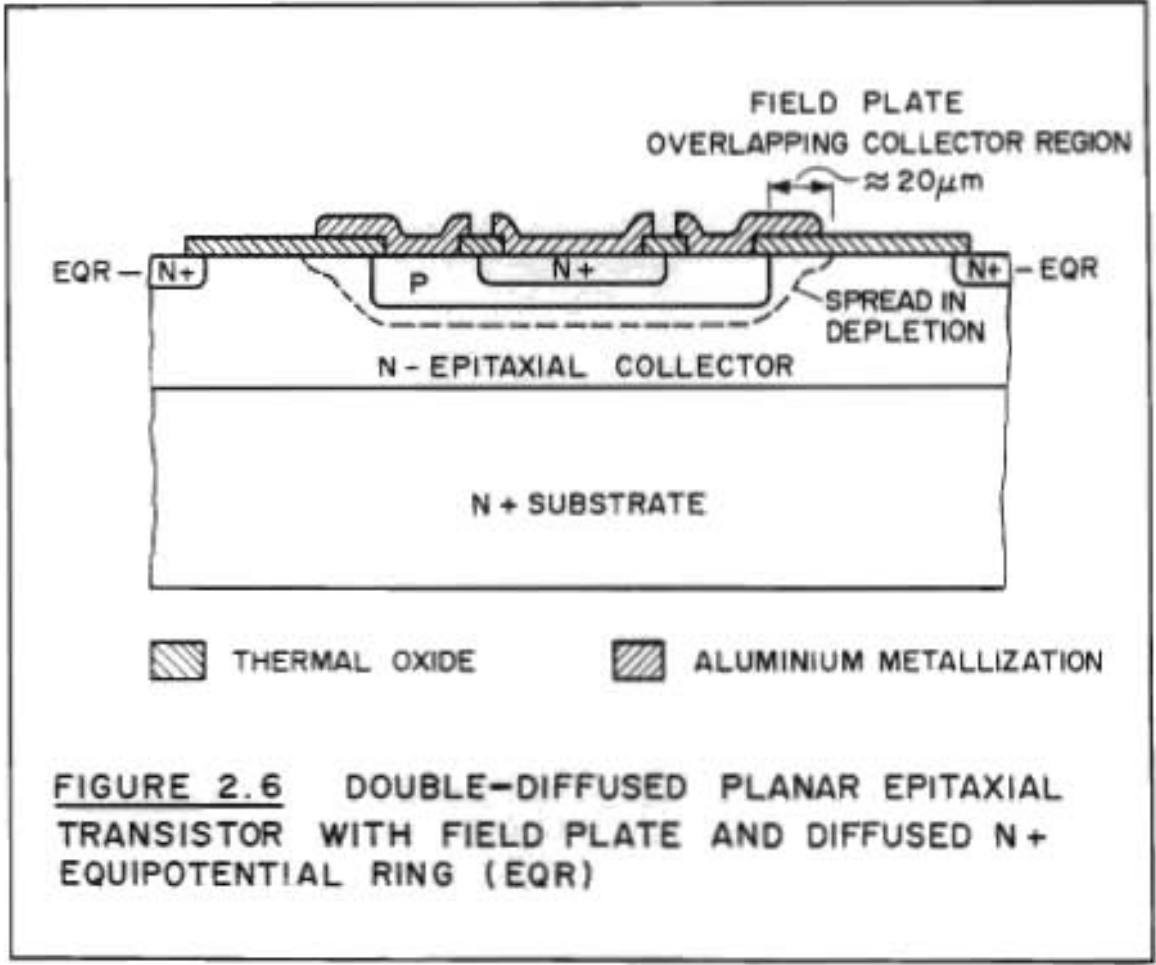


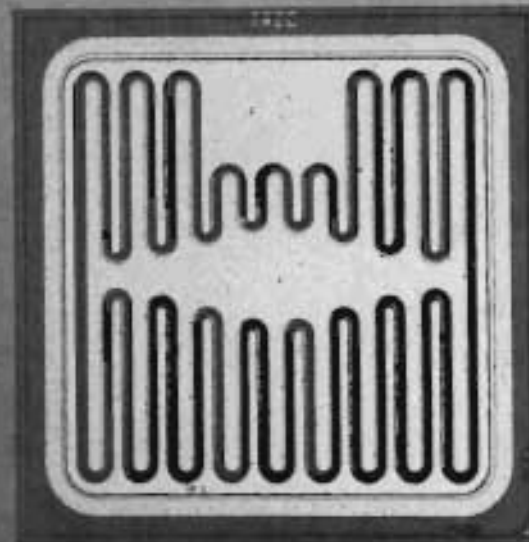
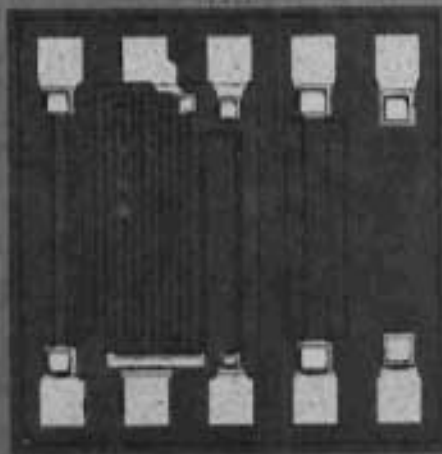
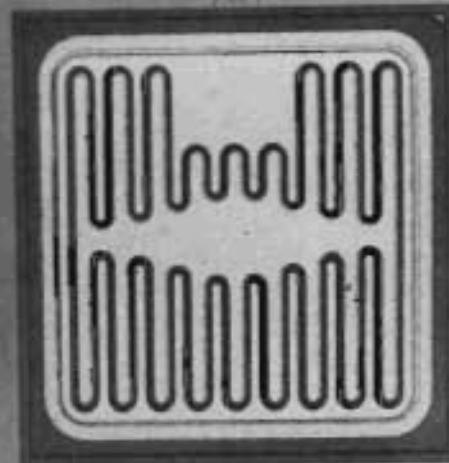
FIGURE 2.6 DOUBLE-DIFFUSED PLANAR EPITAXIAL TRANSISTOR WITH FIELD PLATE AND DIFFUSED N+ EQUIPOTENTIAL RING (EQR)

For good yield on knee voltage, which was a poor feature of the Texas Instruments die that was in use, it was decided to lay out the smallest of the three test transistors with an emitter area of approximately $0,26 \text{ mm}^2$.

As pointed out earlier in this section, the use of an interdigitated emitter structure was questionable, as the peak emitter current density would be $0,25 \text{ A/mm}^2$. To check whether an interdigitated emitter structure was required, the first test transistor, TR2A, was laid out with a simple emitter structure, as shown in Figure 2.7a (page 26). Two base-connecting pads were provided to facilitate die orientation during assembly. The outer dimension of TR2A was $1 \text{ mm} \times 1 \text{ mm}$ and the emitter area was $0,24 \text{ mm}^2$. Whilst this was slightly less than $0,26 \text{ mm}^2$, it will be seen that the effects of parasitic resistance in the collector region do markedly increase the actual active area of the device.

The interdigitated layout of the TR2B, shown in Figure 2.7b (page 26), was suggested by the layout of the Texas Instruments (TI) die that was in use. The new die was almost identical in size to the TI die and had an outer dimension of $1,25 \text{ mm} \times 1,25 \text{ mm}$. This layout incorporated the following features.

- (a) Bonding pads that were substantially larger than on the TI die, an inclusion at the request of the assembly plant.
- (b) A $50 \mu\text{m}$ spacing between the emitter fingers. Although the author had etched an interdigitated metallization pattern with a spacing of only $4 \mu\text{m}$ between fingers on a single layer (Smithies⁶), the registration tolerance of the four consecutive process masks used was $4 \mu\text{m}$. Allowance for adequate overlap to cover poor registration and undercutting led to this seemingly large $50 \mu\text{m}$ spacing between the fingers. Whilst on the one hand this dimension was approximately twice that required for high injection levels, as described in Section 2.5.2, it was also feared that with a larger spacing, valuable emitter area would be lost to the detriment of the knee voltage; however the actual area of the emitter region of TR2B was $0,41 \text{ mm}^2$; larger than that of the TR2A.
- (c) Rounded geometries, adopted as a further precaution to reduce high collector-base field concentrations and to reduce the risk of

FIGURE 2.7a TR2AFIGURE 2.7b TR2BFIGURE 2.7d TR2T
(x 50)FIGURE 2.7c TR2CFIGURE 2.7 THE TR2 EVALUATION TRANSISTORS

THE DEVICES WERE THE FOLOWING SIZES

TR2A	: 1 mm x 1 mm
TR2B	: 1,25 mm x 1,25 mm
TR2C	: 1,5 mm x 1,5 mm

TR2A HAD A SIMPLE EMITTER GEOMETRY. TR2B AND TR2C HAD COMPLEX INTERDIGITATED EMITTER STRUCTURES.

FIGURE 2.7d (TR2T) WAS A TEST CIRCUIT USED FOR PROCESS CONTROL

dislocations in the silicon near corners in a diffusion window.

TR2C was the largest test transistor and is shown in Figure 2.7c (page 26). The device was simply a scaled-up version of TR2B with a die dimension of 1,5 mm x 1,5 mm and an emitter area of 0,61 mm².

TR2T, the test circuit, shown in Figure 2.7d (page 26), enabled rapid process control tests to be carried out on the wafer adjacent to working transistors. This facilitated the setting up of process limits, as all sheet resistivities and junction breakdown voltages could be measured on it.

2.5.5 Electrical evaluation of the prototype devices

The first thing done during evaluation of the prototype devices was a parametric probe test. From the batch of experimental wafers, produced with different emitter process times, one wafer was selected, after sample testing, for subsequent 100 per cent testing to the TR2 - Issue 3 specification.

The results were as follows.

Number of transistors tested	:	612
Number rejected	:	281.

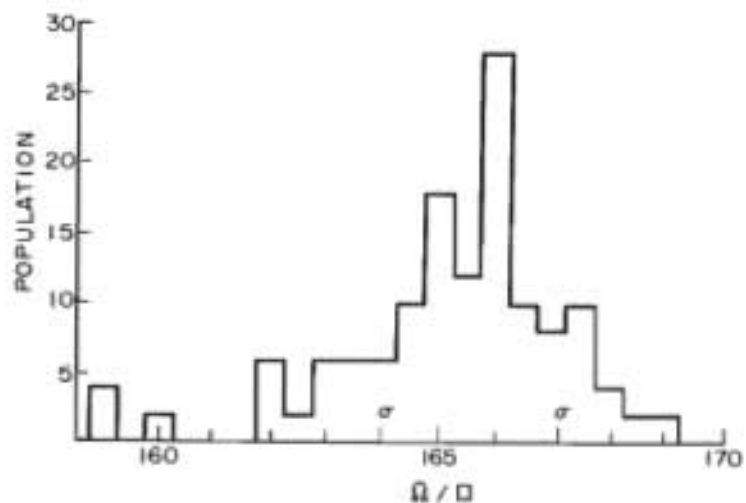
The overall probe yield was thus 54 per cent, which was broken down for the three transistor types as follows :

Yield on TR2A type	:	64,0 per cent
Yield on TR2B type	:	48,5 per cent
Yield on TR2C type	:	50,0 per cent.

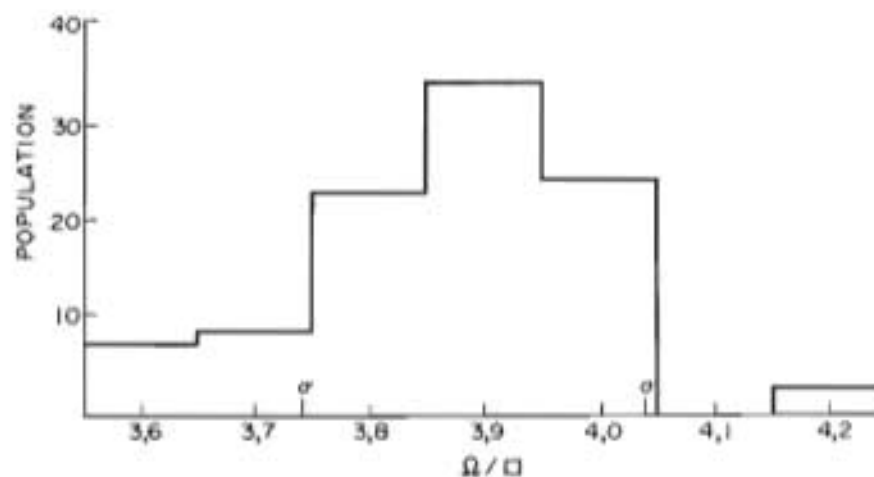
The parameter spreads were measured from the drop-in test structures and are presented in the population distributions in Figure 2.8 (page 28). The most salient feature is the small gain spread measured, with 96 per cent of the values between 105 and 185.

After further analysis the major causes for rejection were broken up into the following three categories.

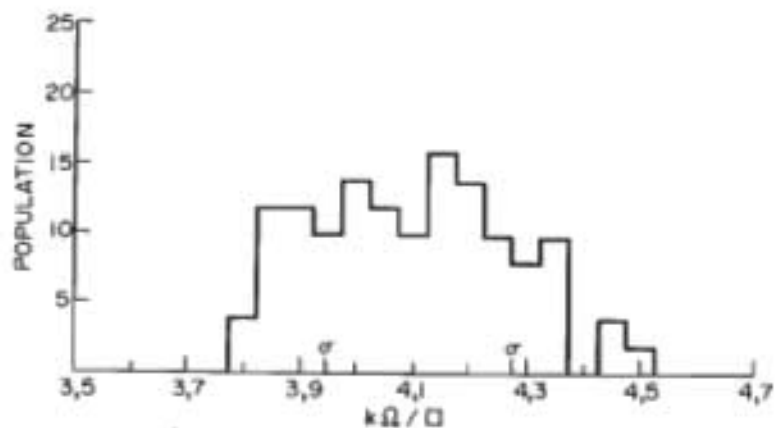
BASE SHEET RESISTIVITY



EMITTER SHEET RESISTIVITY



PINCH RESISTOR SHEET RESISTIVITY



TEST TRANSISTOR GAIN

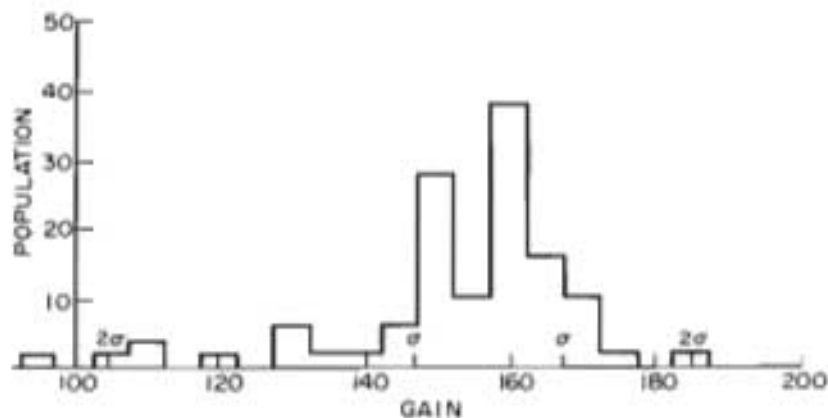


FIGURE 2.8 POPULATION DISTRIBUTIONS OF PARAMETERS MEASURED ON THE TR2T DROP-IN TEST STRUCTURE MEASUREMENTS ON A TWO INCH WAFER EXCLUDING OUTER 3 mm PERIPHERY TO CONFORM WITH THE SILICON SPECIFICATION

- Category 1 Collector-emitter and collector-base characteristics leaky or with breakdowns lower than those specified.
- Category 2 Emitter-base junction characteristics leaky or with breakdowns lower than those specified.
- Category 3 Other failures on gain and knee-voltage tests.

Table 2B : Failure categories in percentages

Geometry	Category (failures in per cent)		
	1	2	3
TR2A	92	6	2
TR2B	78	20	2
TR2C	86	12	2

A number of important observations were based on the data given above and other more specific measurements.

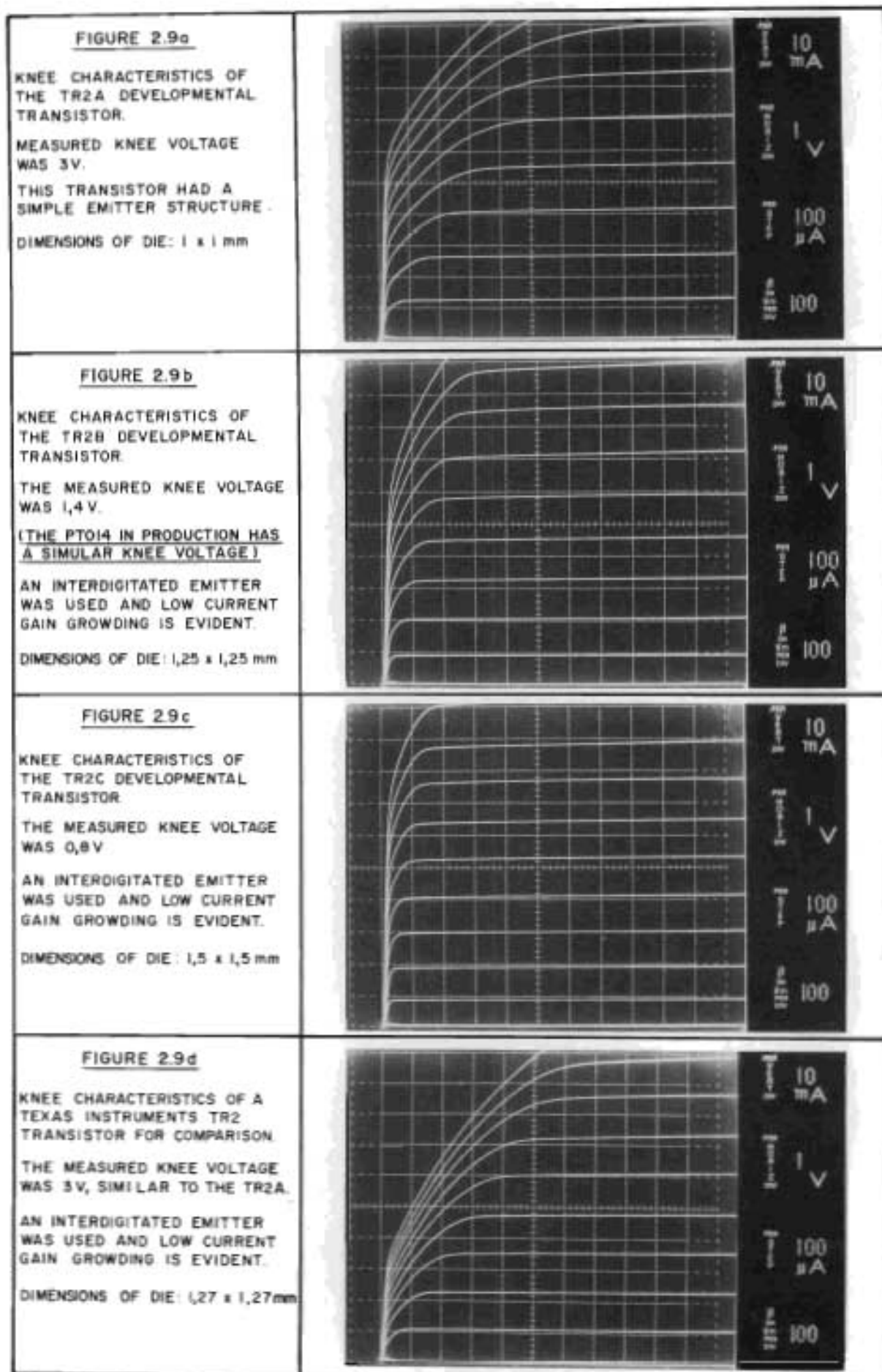
- (a) Failures due to emitter-base leakage on the TR2B and TR2C type geometries were significantly greater than those on the TR2A type. This was attributed to the much longer emitter periphery on the interdigitated structures, providing a much longer path for the formation of process-induced crystallographic faults. That the smaller TR2B type had a higher reject percentage than the TR2C type on this characteristic was believed to be due to the fact that the clearances allowed for oxide and metallization overlap were inadequate, being proportionally smaller on the TR2B type.
- (b) Whereas all three geometries had a yield in excess of 98 per cent on the specified gains, it was noted from the figures recorded that at collector currents between 10 and 100 mA, the gains of adjacent TR2B and TR2C types were generally about 10 per cent lower than those for the adjacent A types.
- (c) All three adjacent geometries were found to have similar collector-

base breakdown voltages (approximately 600 V). It was noted, however, that the TR2B and TR2C types both had collector-emitter breakdown voltages some 10 to 20 V lower than the adjacent A types. Application of equation 2.5A (page 20), which relates gains and breakdowns, provides an immediate conflict with the observation in (b) above. It is clear, then, that both the actual transistor geometry and the process have an important bearing on gains and breakdowns.

- (d) At collector currents below 1 mA, significant gain crowding was noted on only the TR2B and TR2C types. At 500 μ A the gains of the TR2B and TR2C types had dropped to half their peak values, whilst only at 10 μ A was the gain of the TR2A type halved.
- (e) The knee characteristics were similar for all three structures, as shown in Figures 2.9a, b and c (page 31), with the knee voltage simply scaled in proportion to the values of the collector resistance, R_C . The fact that an interdigitated structure was used did not affect the scaled knee characteristic other than, perhaps, to sharpen it.
- (f) Figure 2.9d (page 31) shows, for comparison, the knee characteristics of a TR2 interdigitated device of Texas Instruments manufacture that met the TR2 - Issue 3 specification. This device had a dimension of 1,27 mm x 1,27 mm and had a knee voltage approximately equal to that of the TR2A, which was only 1 mm x 1 mm in size.

The surge test, as in the TR2 - Issue 3 specification, was a key test for the acceptance of the device, and the results were outstandingly good. Three samples each of the TR2A, TR2B and TR2C geometry devices, assembled in TO-39 packages, were subjected to the 100 W 10 μ s surge test at a case temperature of 95 °C. All parameters measured before and after the surge test showed virtually no change when compared (Serrano - Appendix 2.4 commencing on page 231). The important parameter of gain changed by only -0,72 per cent on average.

These results were in contrast to those of tests on the acceptable commercial types evaluated by Heeson¹⁰, where changes recorded were considerably greater. Gain changes of between 2,4 and 9,8 per cent were recorded, for example. Clearly the 8 μ m depth base junction process that



was developed was highly suited to the application.

2.5.6 The production geometry

The success of the prototype devices was such that the authorization to proceed with production was received without delay.

Two key features from the developmental transistors were incorporated into the production geometry, which was termed the #/014 layout. These features were the following.

- (a) Use of a simple geometry similar to that of the TR2A type with a view to both an improved yield and also large bonding areas, as these were favoured.
- (b) Adoption of a die dimension of 1,27 mm x 1,27 mm to give a collector region resistance of about 30-40 ohms and a knee voltage of less than 2 V. (The 1 mm square TR2A types had knee voltages of about 3 V.)

The #/014A layout is shown in Figure 2.10a (page 33), whilst two metal variants, used to confirm that the 36 μ m field plate overlap used was optimal, are shown in Figures 2.10b and 2.10c (page 33).

2.6 A NOVEL LIGHT EMISSION PHENOMENON AND NEW DATA FROM THE DEVELOPMENT AND PRODUCTION PROGRAMMES

This section reports on a novel light emission phenomenon, two new aspects of transistor design that have emerged from the analysis of data from the development and production of PT014 transistors and an evaluation of a new transistor structure, the Gate Associated Transistor (GAT), for the PT014 application.

2.6.1 The first production layout - an unusual phenomenon observed

The first #/014 production layout incorporated features in the lateral depletion region of the collector, and a most unusual effect was observed which had not been reported before. Figure 2.11a (page 34) shows

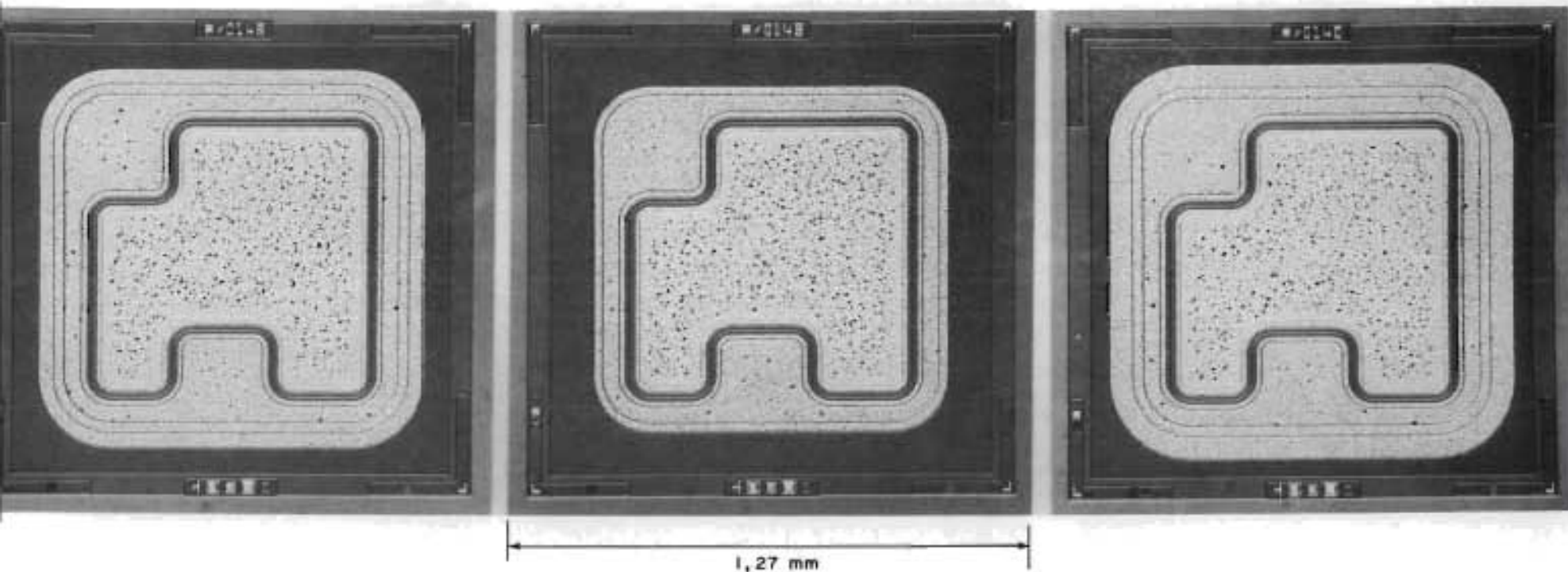


FIGURE 2.10a
 THE PRODUCTION GEOMETRY OF THE O14 TRANSISTOR. THE A-METAL VARIANT HAD A FIELD PLATE OVERLAP OF $36\ \mu\text{m}$ AND PROVIDED STABLE COLLECTOR-BASE AND COLLECTOR-EMITTER BREAKDOWN CHARACTERISTICS.

FIGURE 2.10b
 THE B-METAL VARIANT HAD NO OVERLAP OVER THE COLLECTOR REGION AND SOME 'WALKOUT' INSTABILITY IN THE COLLECTOR-BASE BREAKDOWN CHARACTERISTIC WAS NOTED.

FIGURE 2.10c
 THE C-METAL HAD A $58\ \mu\text{m}$ OVERLAP OVER THE COLLECTOR REGION AND THE DEVICE HAD A VERY STABLE COLLECTOR-EMITTER BREAKDOWN CHARACTERISTIC. ON TESTING THE COLLECTOR-BASE BREAKDOWN CHARACTERISTIC INSTABILITY DUE TO EXTERNAL BREAKDOWN OCCURRED

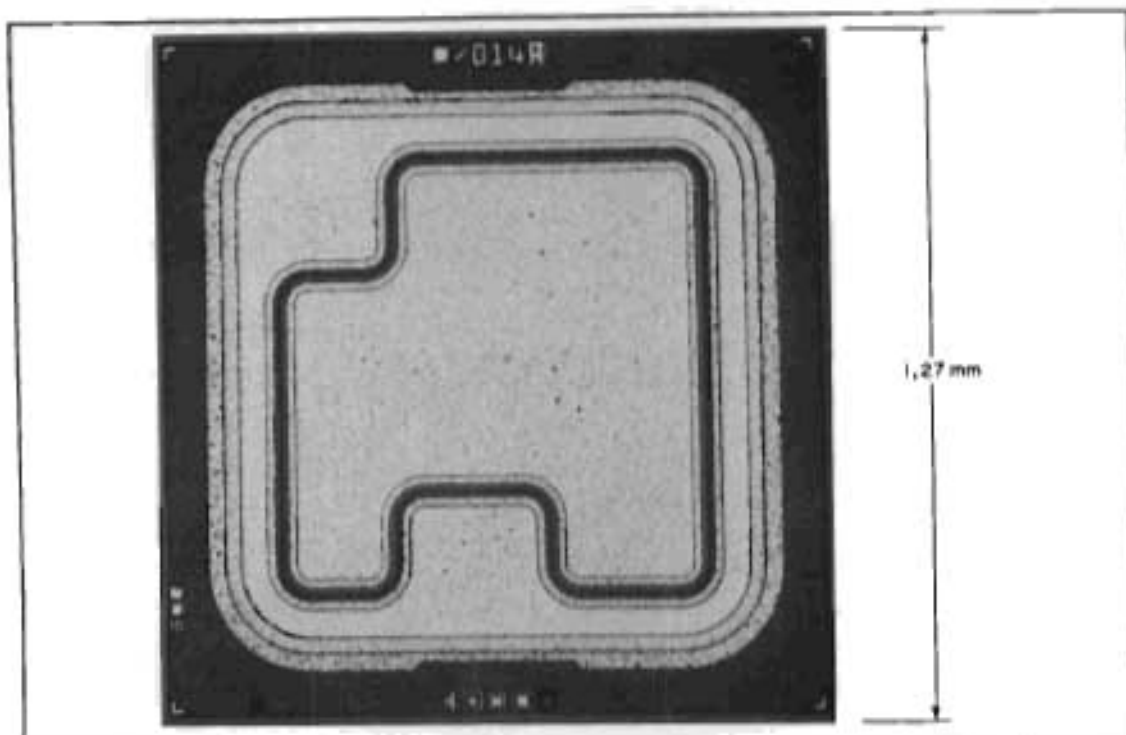


FIGURE 2.11a

THE FIRST LAYOUT OF THE M/014 DIE FOR THE PTO14 TRANSISTOR.

P-TYPE BASE DIFFUSIONS WERE INCLUDED UNDER THE DIE TYPE NUMBER AND THE ALIGNMENT TARGET (BOTTOM CENTRE) ALUMINIUM WAS CONNECTED TO THESE FEATURES

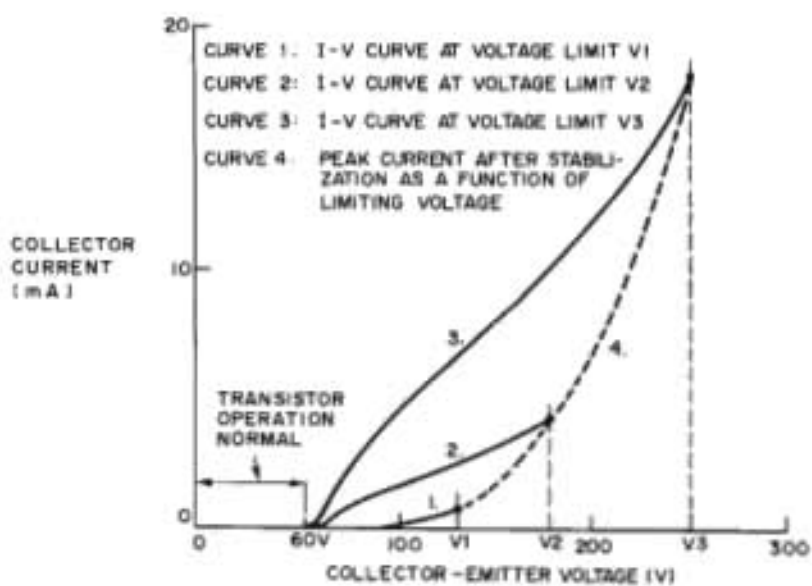


FIGURE 2.11b

REVERSIBLE INCREASE IN COLLECTOR - EMITTER LEAKAGE CURRENT AS A FUNCTION OF APPLIED VOLTAGE.

NOTE: REPETITIVE TRACES AFTER STABILIZATION ARE PRESENTED AND BASE CURRENT WAS ZERO

this first layout where, due to an oversight in checking, the registration marks and resolution targets were left in the N- collector region adjacent to the N+ equipotential ring.

Measurements on breakdowns after the contact photo-engage gave stable results, and gain characteristics were good. After metallization the devices exhibited a highly unstable but fully reversible increase in collector-emitter leakage above a threshold of 60 V. The leakage current increased roughly as the square of the applied voltage, and took approximately 0,5 s to settle. On removal of the voltage stress, the device recovered in a similar time. Figure 2.11b (page 34) shows the I_{CEO} vs V_{CE} characteristic observed after metallization, and indicates the voltage dependence. After observation of the electrical characteristic, Salama (Pers. comm.[†]) ascribed the effect to surface contamination. Subsequent observation of a stressed die in the dark showed the effect to be thermal in nature, with the formation of localized mesoplasmas between the P-diffusion in the collector region and the N+ equipotential ring. Figure 2.11c (page 36) shows this effect as observed.

A probable explanation of the phenomenon was that the inclusion of the P-type diffusions near the equipotential ring formed a P-N-P-N-N+ layered diode which was triggered by external field effects only after metallization. The lighted areas were simply mesoplasmas of localized heating, and the long time constant associated with the effect was doubtless thermal in origin. That the trigger was due to external effects was confirmed by Rusu et al.²² who used a gate electrode in the position of the field plate over a PN junction to induce a reversible breakdown voltage collapse.

In a later publication, Gupta et al.²³ induced visible luminescence in a double-diffused PN junction under reverse bias, and a similar light-emission phenomenon has been observed in the channel region of a silicon MOSFET by Tam et al.²⁴

Removal of the P-diffusions from the lateral collector depletion region in the final layout of the #/014 die resulted in devices with highly stable breakdown characteristics.

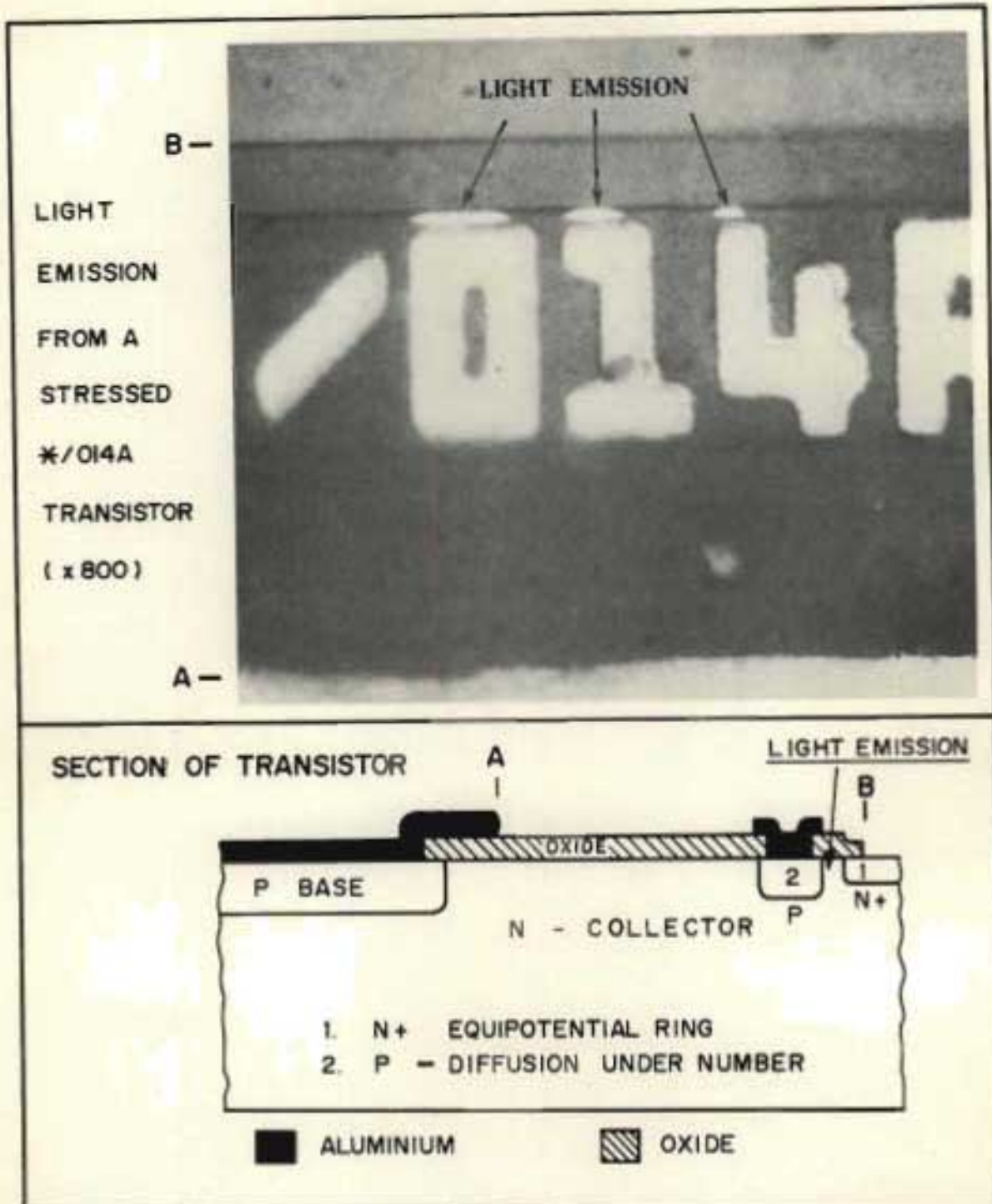


FIGURE 2.11c LIGHT EMISSION FROM A * / 014A TRANSISTOR AT AN APPLIED COLLECTOR-EMITTER VOLTAGE OF 250 V IS CLEARLY VISIBLE ABOVE THE P-DIFFUSED AND METALLIZED '014'; (A double exposure was made to show both transistor features and light emission).

NO DIFFUSION IS UNDER THE 'A' AND NO LIGHT EMISSION IS VISIBLE. THE SECTIONAL DRAWING SHOWS THE LOCATION OF THE DIFFUSIONS AND METALLIZATION IN THE TRANSISTOR. A AND B COINCIDE ON THE PHOTOGRAPH AND DRAWING. THE MEAN FIELD BETWEEN A AND B WAS 30 kV/cm FOR THE PHOTOGRAPH.

2.6.2 A new correction factor for collector resistance and a new rule for minimum interdigitated finger spacing

Sound reasons for not using an interdigitated structure for the PT014 have been given. Nevertheless, for applications where the emitter current density is sufficiently high to merit use of this structure, the following considerations on minimum finger spacing in high-voltage devices are important.

Although in general acceptable, the rule given by Ghandi¹⁹ for the maximum spacing between emitter fingers, viz that this spacing should be about 14 times the base width, was found to be impractical in the technology used for the PT014, which had a base width of about 2 micrometres. In addition, it was quite clear that in these high-voltage devices the collector resistance, R_C , played a cardinal role in performance at high currents, and that this figure should be minimized in an interdigitated structure. A new correction factor for R_C was therefore developed and then applied to interdigitated structures.

In Figures 2.12a and 2.12b (page 38), reproduced from Ghandi²⁵, the limiting conditions are shown when compensating for collector parasitic resistance due to current spreading. For thin epitaxial layers the active device area is simply taken as the area of the emitter, and for a non-epitaxial device with a collector width of some 200 μm , the active area used in calculating collector resistance is given as

$$A_{\text{eff}} = (A_E + A_C)/2 \quad \dots\dots\dots 2.6A$$

where

A_{eff} is the effective collector area used to calculate R_C ;

A_E is the area of the emitter; and

A_C is the total area of the collector region.

With the TR2A, TR2B and TR2C geometries it was clear that neither set of conditions was accurate in attempting to calculate the collector resistance, R_C , and an intermediate approach was required.

GHANDI'S APPROACH TO COLLECTOR AREA CORRECTION TO CALCULATE COLLECTOR RESISTANCE, R_c

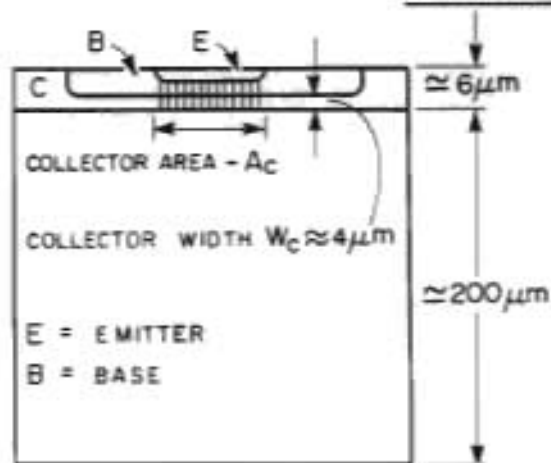


FIGURE 2.12a THIN EPITAXIAL COLLECTOR

$A_{\text{eff}} = \text{EFFECTIVE AREA}$
 $= A_E \text{ (EMITTER AREA)}$
 $= A_C \text{ (COLLECTOR AREA)}$

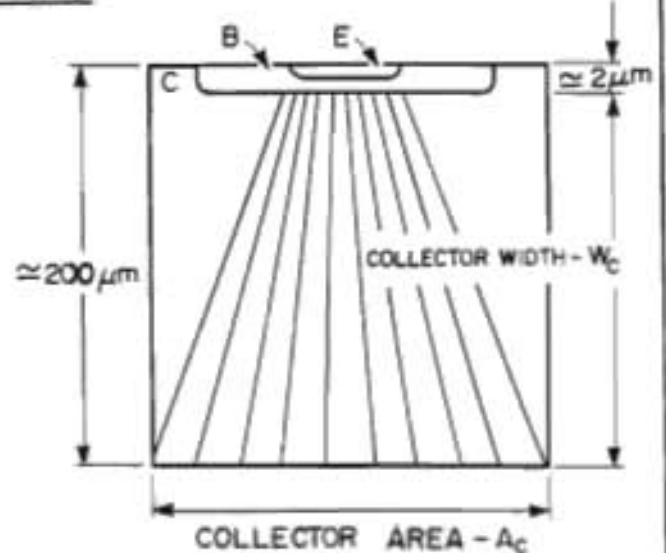
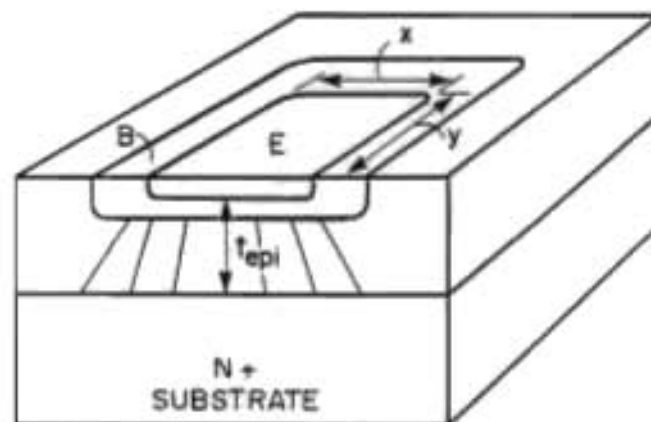


FIGURE 2.12b WIDE COLLECTOR

$A_{\text{eff}} = \text{EFFECTIVE AREA}$
 $= (A_C + A_E) / 2$

PROPOSED GENERAL APPROACH TO CALCULATE EFFECTIVE COLLECTOR AREA



$t_{\text{epi}} = \text{EPITAXIAL LAYER THICKNESS BELOW EMITTER-BASE JUNCTION}$
 $L_E = \text{EMITTER PERIPHERY} = 2(x + y)$
 $A_E = \text{EMITTER AREA} = x \cdot y$
 $A_{\text{eff}} = \text{EFFECTIVE COLLECTOR AREA} = A_E + (L_E \times t_{\text{epi}} / 2)$

FIGURE 2.12c PROPOSED AREA CORRECTION TO CALCULATE R_c

A new approximation was proposed, shown in Figure 2.12c (page 38), and a good correlation obtained between emitter geometries and measured collector resistance. In this proposal, an emitter periphery correction related to the epitaxial layer thickness is used, as follows :

$$A_{\text{eff}} = A_E + L_E \times t_{\text{epi}}/2 \quad \dots\dots\dots 2.6B$$

where

L_E is the length of the emitter periphery;

t_{epi} is the epitaxial layer thickness.

Comparison of measured and predicted results on one sample each of TR2A, TR2B and TR2C devices from the same wafer, with the specified epitaxial layer, gave the results presented in Table 2C. (For the purposes of Ghandi's correction for a thick collector region, the whole collector area of the test transistors was taken, as bounded by the equipotential ring.)

Table 2C : Comparison of measured and predicted values of R_C

Device	Measured R_C	Predicted R_C (no correction)		Ghandi's R_C correction		Author's R_C correction	
	R_C (ohms)	R_C (ohms)	A_E (mm ²)	R_C (ohms)	A_E (mm ²)	R_C (ohms)	A_E (mm ²)
TR2A	55,6	62,9	0,244	28,3	0,542	54,1	0,284
TR2B	28,4	37,1	0,414	20,6	0,747	23,3	0,658
TR2C	16,5	25,1	0,611	15,9	0,965	16,9	0,904

Quite clearly the new correction using equation 2.6B (page 39) was the most accurate. With Ghandi's correction for a wide collector, the result for the TR2A was about half the measured value and for the TR2B and TR2C the values were still low. A most important feature of the correction in equation 2.6B was that predicted results were accurate when vastly differing emitter layouts were used.

The following deductions were made.

- (a) Equation 2.6B indicates that if the emitter stripe separation of an interdigitated transistor is less than the epitaxial layer thickness, the collector resistance is not affected. Larger separations will give increased values of R_C .
- (b) For lower-voltage epitaxial devices, reduced emitter stripe clearances should also, if possible, be related to the base width of the process used, as recommended by Ghandi¹⁹. In more than fifty different commercial medium-power devices of both epitaxial and non-epitaxial structure that were inspected, neither this rule nor one similar to that in (a) had been applied. It would appear to be true to say that finger spacing has not been a vital consideration in the design of commercial medium-power devices. Using modern photolithographic equipment with automatic alignment features and careful wet etching, minimum finger spacing could be reduced to about 20 μm without prejudicing yields significantly. In terms of the correction in (a), this would cover devices with collector-emitter breakdowns down to about 50 V.
- (c) When designing a transistor for optimum device performance, the collector current range should be chosen with care. For analogue devices requiring operation over a wide range of injection levels, the all-too-common use of an interdigitated structure is questionable. For a switching device requiring optimum gain at high injection levels, the emitter stripe spacing must be considered critically on the basis of a knowledge of both the epitaxial layer thickness and the base width.

2.6.3 Generalized data for the specification of epitaxial layers

The derivation of the PT014 epitaxial layer specification was guided by the limited data available and subsequent experimental verification. In view of the lack of generalized curves from which an epitaxial layer could be readily and reliably specified, data from the work in this chapter, including the GAT experiments, were combined with existing data on breakdowns generated in the parallel low-voltage IC and transistor processes. The results which

follow may be used for specifying an epitaxial layer for double-diffused transistors, or planar bipolar integrated circuits over a range of collector-emitter breakdowns from 2 to 800 V. The curves in this section corroborate data that were derived from experimentally determined ionization rates as presented by Roulston and Depey²⁶. Poorer agreement was found with their curves drawn from a theoretical investigation of ionization rates.

Figure 2.13 (page 42) shows BV_{CEO} and the depletion width, W_D , at the avalanche breakdown field as a function of epitaxial layer resistivity. In order to specify an epitaxial layer the following procedure is used.

- (a) Normalize the gain.

Note the target values of h_{FE} and BV_{CEO} , with insets on either parameter to ensure good yield; then, using equation 2.5A (page 20), normalize BV_{CEO} to a gain of 100, using a value of $n = 5$ for devices with breakdowns in excess of 50 V. For breakdowns below 50 V use $n = 4.5$.

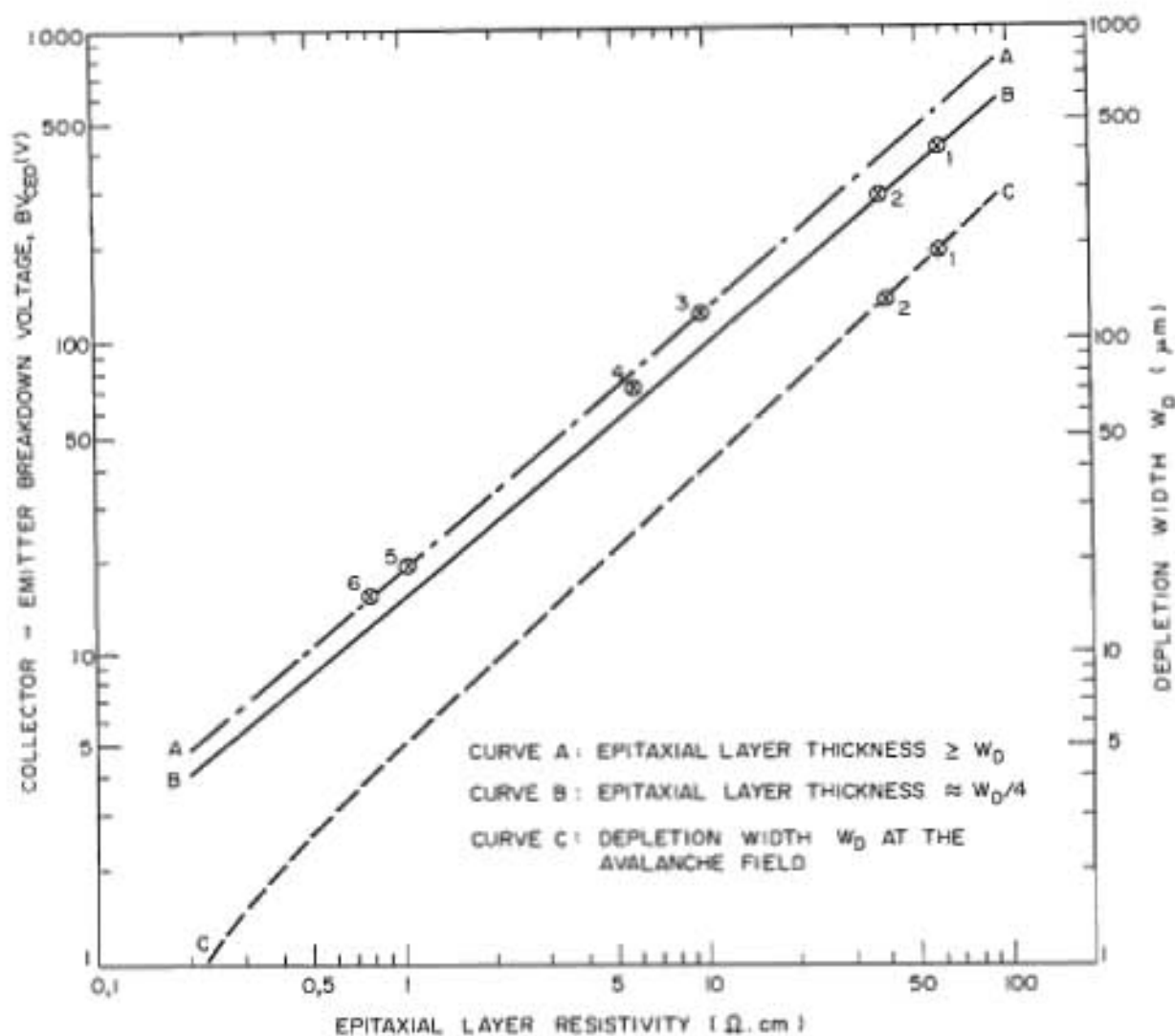
- (b) Choose the collector structure.

Figure 2.14 (page 43) shows the ratio between the collector resistance of a transistor designed with a full depletion width (W_D) collector and one designed with a one-quarter depletion width ($W_D/4$) punch-through collector, as a function of BV_{CEO} . If collector resistance is to be minimized, or if BV_{CEO} values of greater than 100 V are desired, a punchthrough collector is advisable. (Another reason why a punchthrough collector is useful in such cases is that it controls BV_{CEO} accurately.)

- (c) Take epitaxial layer description from Figure 2.13 (page 42).

For the non-punchthrough collector read the epitaxial layer resistivity from line A. The epitaxial layer thickness W_D for that resistivity is given by line C.

For the punchthrough case the resistivity is obtained from line B and the layer thickness is one quarter of the value of W_D . (The



- DATA POINTS :
- 1 - MEASUREMENTS ON PTO18 TRANSISTORS
 - 2 - MEASUREMENTS ON PTO14 TRANSISTORS
 - 3 - MEASUREMENTS ON STANDARD μ /O14 TRANSISTORS IN GAT EXPERIMENTS USING $10 \Omega \cdot \text{cm}$ SUBSTRATES
 - 4 - MEASUREMENTS ON BC107 TRANSISTORS FROM NEERI IC FACILITY
 - 5 - MEASUREMENTS ON $1 \Omega \cdot \text{cm}$ SILICON IN GAT EXPERIMENTS (STANDARD μ /O14)
 - 6 - MEASUREMENTS ON $0.8 \Omega \cdot \text{cm}$ EPITAXIAL LAYERS PRODUCED FOR THE NEERI STANDARD IC PROCESS

OTHER DATA SOURCE : ROULSTON D.J. AND DEPEY M. (1980) ELECTRONICS LETTERS VOLUME 16 NUMBER 21 p.804 - FIGURE 2 (EXPERIMENTAL DATA)

FIGURE 2.13 CURVE OF COLLECTOR - EMITTER BREAKDOWN VOLTAGE AND DEPLETION WIDTH vs EPITAXIAL LAYER RESISTIVITY FOR NPN TRANSISTORS WITH $h_{FE} \approx 100$

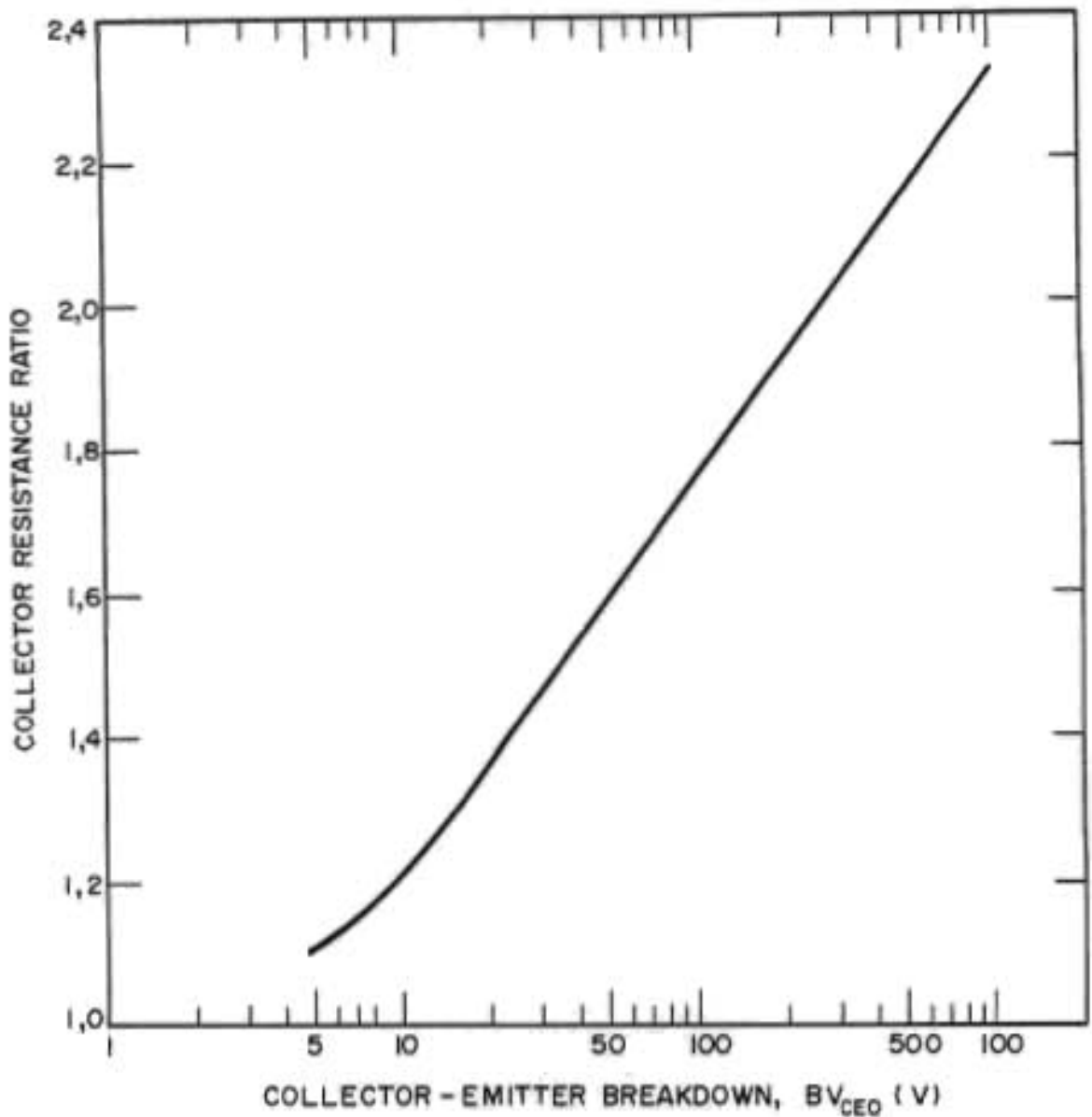


FIGURE 2.14 INCREASE IN COLLECTOR RESISTANCE OF A TRANSISTOR WITH A FULL DEPLETION WIDTH COLLECTOR, W_D , RELATIVE TO A TRANSISTOR WITH A QUARTER DEPLETION WIDTH, $W_D/4$, PUNCHTHROUGH COLLECTOR AS A FUNCTION OF COLLECTOR - EMITTER BREAKDOWN VOLTAGE. THIS CURVE WAS DERIVED DIRECTLY FROM CURVES a, b AND c ON FIGURE 2.13 AND IS FOR TRANSISTORS WITH $\eta_{FE} \approx 100$

drop in BV_{CEO} increases rapidly if layers of thickness less than $W_D/4$ are used, as the value of n does not change significantly, and it is difficult to achieve higher resistivities in epitaxy.)

2.6.4 The gate associated transistor (GAT)

In Section 2.5 it was noted that for the purpose of the high-temperature surge test, the TR2A geometry which was only 1 mm square was adequate. In production a 1.27 mm x 1.27 mm device (i.e. 61 per cent greater in overall area) was used to ensure a low collector resistance, R_C , and hence a good yield on the knee voltage, V_{CEK} .

The gate associated transistor (GAT), first described by Kondo et al.²⁷, apparently offered a means of increasing BV_{CEO} relative to BV_{CBO} without prejudicing any other parameters. This being the case, it appeared that an epitaxial layer with a lower resistivity and thickness than the one in use for the PT014 might be used with a GAT structure with typical BV_{CEO} values of > 250 V being maintained. This would make possible a significant reduction in area and hence cost of the PT014, without increased collector resistance.

Experiments were carried out that were aimed at testing the design rules given for the GAT and to establish possible drawbacks in the use of the structure.

2.6.4.1 Principle of operation

Figures 2.15a and 2.15b (page 45) show sections of a GAT and static induction transistor (SIT), described by Nishizawa²⁸. The GAT is a standard transistor with an additional deep P-diffusion. In common with the SIT this forms the gate of a vertical symmetry field effect transistor. In the GAT, at high values of collector-base voltage, the standard base region is shielded by extended depletion around the deep P-diffusions, and the base width is effectively increased. The author had already investigated the SIT in available bipolar technology (Smithies²⁹) and appreciated that seemingly simple vertical structures were in fact frequently difficult to realize.

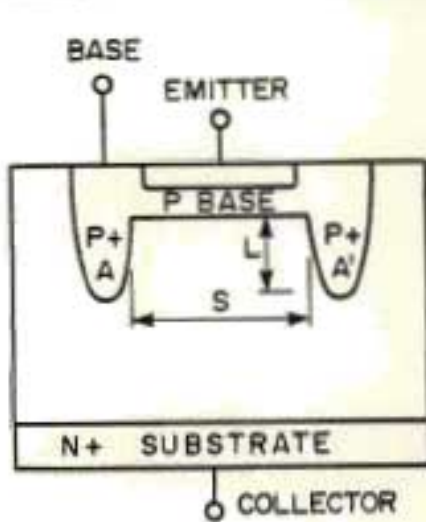


FIGURE 2.15a THE GATE ASSOCIATED TRANSISTOR (GAT)

A AND A' ARE THE DIFFUSED GATE ELECTRODES

L IS THE CHANNEL LENGTH

S IS THE GATE SPACING

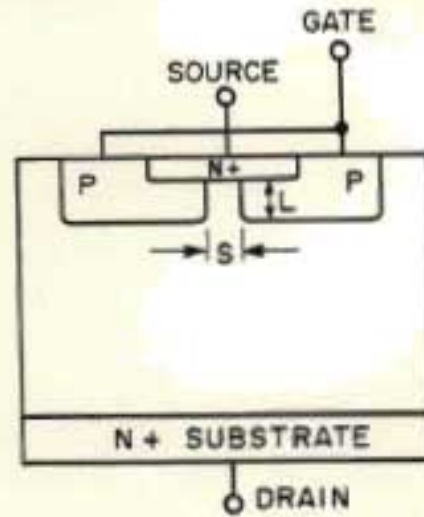


FIGURE 2.15b THE STATIC INDUCTION TRANSISTOR (SIT)

L AND S ARE AS FOR THE GAT

THE SIT IS A VERTICAL SYMMETRY FIELD EFFECT TRANSISTOR

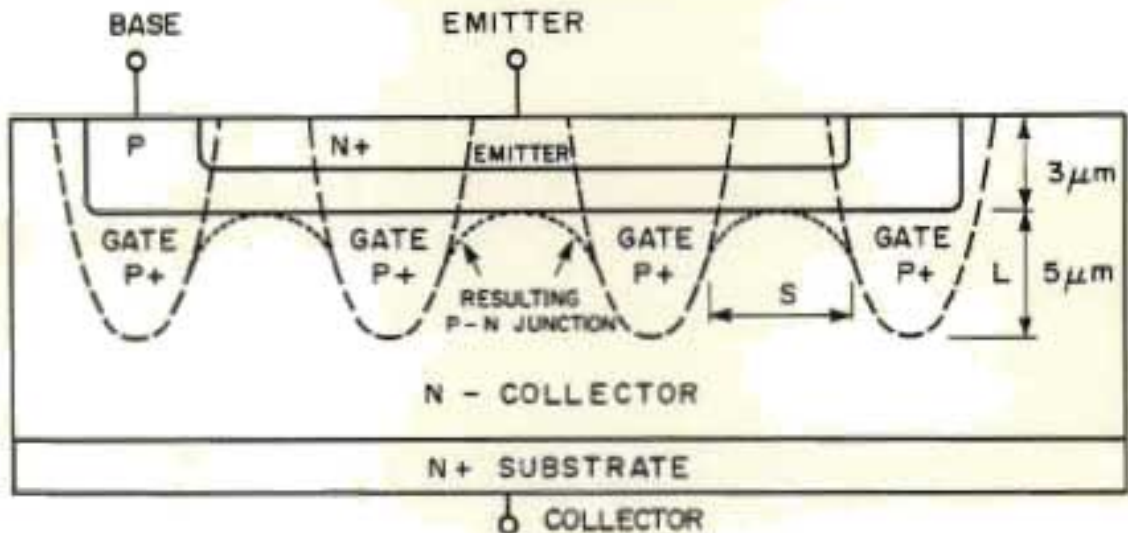


FIGURE 2.16 THE ADDITION OF A SINGLE DEEP P+ DIFFUSION TO THE STANDARD $\times/014$ GEOMETRY TRANSISTOR TO FORM A GATE ASSOCIATED TRANSISTOR (GAT). VALUES FOR S OF 20, 28 AND 38 μm WERE USED. (N.B. THE JUNCTION DEPTHS SHOWN DO NOT CORRESPOND WITH THOSE USED FOR THE P \times 014 TRANSISTOR)

2.6.4.2 Experimental structure

Figure 2.16 (page 45) shows a section of the experimental structure adopted by the author as applied to the standard PT014 geometry. The fact that an unbroken emitter diffusion was used is not important, as the effective base width of the parasitic NPN transistors formed by the deep P-diffusions was about 6 μm, sufficiently great to ensure that their gains would be low enough not significantly to influence BV_{CEO} of the GAT devices. Spacings between the deep P-diffusion stripes of 20, 28 and 38 μm were used in three separate adjacent devices as shown in Figure 2.17 (page 47). The fourth device, without the deep P-diffusion, was used as a standard reference transistor. In the process used, the shallow P-diffusion was about 3 μm and the deep P-diffusion about 8 μm, giving a channel length L of some 5 μm.

Kondo and Yukimoto³⁰ indicate that the increase in BV_{CEO} should follow the relationship

$$\begin{aligned}
 [BV_{CEO}]_{GAT} &= [1 + \exp(\pi \times L/S)] \times [BV_{CEO}]_{BIP} \\
 &= K' \times [BV_{CEO}]_{BIP} \qquad \dots\dots\dots 2.6C
 \end{aligned}$$

where

- [BV_{CEO}]_{GAT} is the collector-emitter breakdown of the GAT;
- [BV_{CEO}]_{BIP} is the collector-emitter breakdown of the standard bipolar device;
- L is the channel length;
- S is the separation of the deep P-diffusions;
- K' is termed the breakdown voltage incremental factor.

In these devices the anticipated increases in BV_{CEO} were :

Type	DP38	:	K'	=	1,51
	DP28	:	K'	=	1,75
	DP20	:	K'	=	2,19.

To cover as broad a base as possible, tests were carried out simultaneously on plain silicon substrates of resistivity 1 ohm.cm and 10 ohm.cm as well as some of the standard epitaxial substrates for the

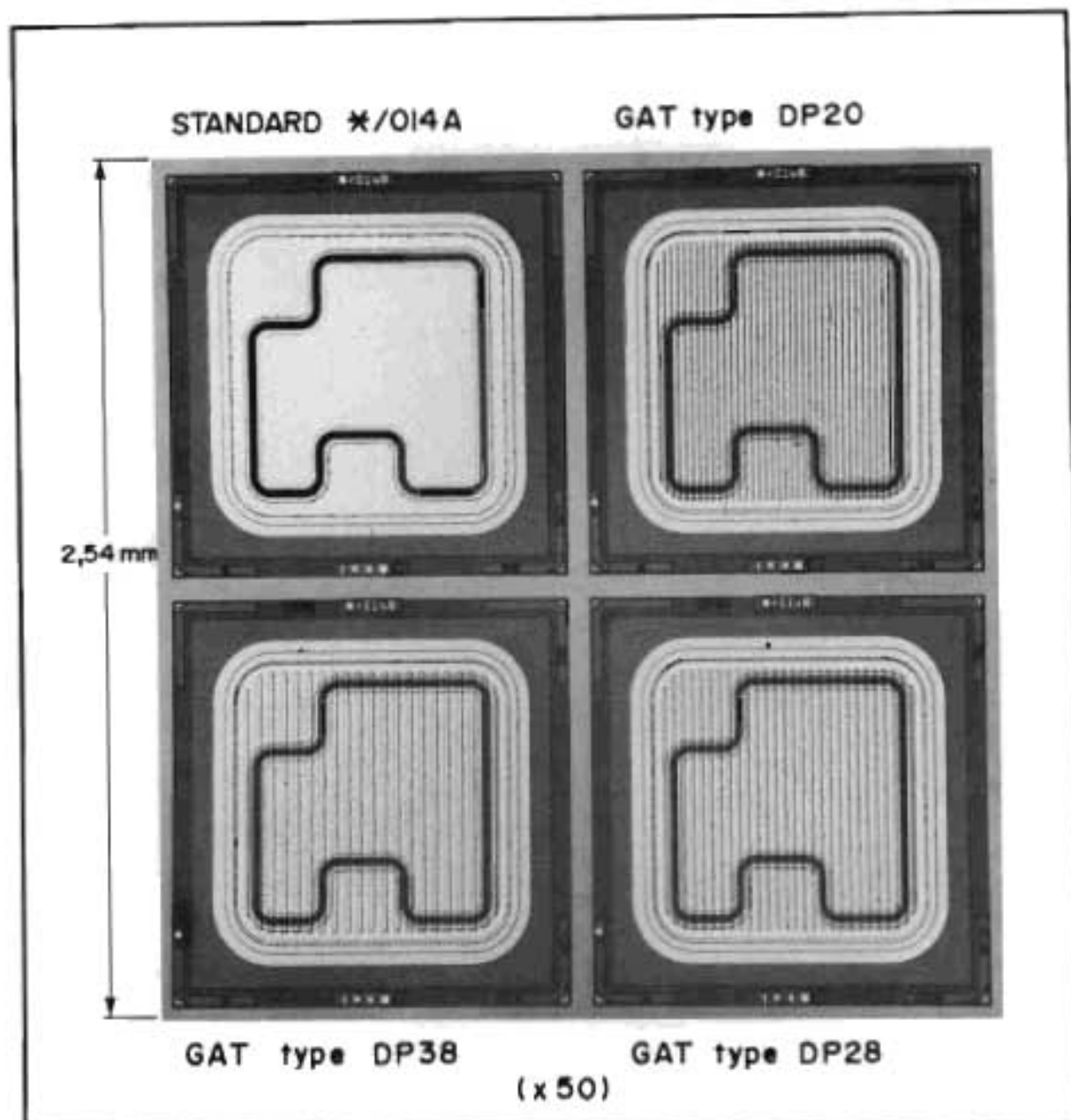


FIGURE 2.17 TRANSISTORS USED IN THE GATE ASSOCIATED TRANSISTOR (GAT) EXPERIMENTS.

AN ADDITIONAL DEEP P DIFFUSION MASK FOR THE GATE ELECTRODES WAS ADDED TO THE STANDARD FOUR-MASK SET FOR THE #/014A. ONE STANDARD TRANSISTOR WAS RETAINED FOR CONTROL PURPOSES, AND THREE DIFFERENT GAT DEVICES WITH DIFFERENT GATE SPACINGS WERE INCLUDED. THE SPACINGS, S , WERE:

- DP38 : $S = 38 \mu\text{m}$
- DP28 : $S = 28 \mu\text{m}$
- DP20 : $S = 20 \mu\text{m}$.

PT014 transistors. Both $\langle 111 \rangle$ and $\langle 100 \rangle$ orientations were used for the 10 ohm.cm material and in all other cases the orientation was $\langle 111 \rangle$.

2.6.4.3 Experimental results

The results, obtained from automatic test data summarized in Appendix 2.5 (page 234), are presented in a reduced form in Table 2D (page 49). In all cases the GAT structures exhibited decreased gain, owing to some degree of overlap of the deep P-gates, the result of lateral diffusion. As a basis of comparison, the mean K' -values and the associated n -values are given from equation 2.5A (page 20), relating BV_{CEO} , h_{FE} and BV_{CEO} . These values may be compared with the predicted K' - and n -values presented in the first row, labelled 'Predicted Results' in Table 2D (page 49).

2.6.4.4 Discussion of results

The results clearly indicate the following.

- (a) The GAT structure did yield a worth-while increase in BV_{CEO} relative to a standard transistor. The maximum value recorded of K' , the incremental factor, was 1.46 which represented an increase in BV_{CEO} of 46 per cent; however other values of K' were generally nearer to 1.2 indicating a 20 per cent increase in breakdown.
- (b) In all cases, values of K' were lower than those predicted by Kondo et al.³⁰ For the devices evaluated in this exercise, K' was thus not given accurately by the simple geometrical relationship of equation 2.6C (page 46).
- (c) In the cases observed, K' was a function of substrate resistivity and orientation. On the lower-resistivity substrates the value of K' increased more consistently with decreased stripe spacing. The wafers with $\langle 100 \rangle$ orientation showed very little difference in K' for different spacings, and increases of less than 20 per cent in breakdown were obtained.
- (d) With reduced values of spacing, S , K' actually decreased in two cases, and in other cases remained virtually constant.

Table 2D : A comparison of GATs and standard bipolar transistors

Substrate			Standard #/014		DP38		DP28		DP20	
no.	(ohm.cm)	orient.	K'	n	K' ⁽¹⁾	n ⁽²⁾	K'	n	K'	n
Predicted Results →			<u>1</u>	<u>5</u>	<u>1,51</u>	<u>9,05</u>	<u>1,75</u>	<u>12,7</u>	<u>2,19</u>	<u>18,3</u>
3	1	<111>	1	4,69	1,09	5,13	1,24	6,13	1,31	7,45
6	1	<111>	1	4,12	1,07	4,44	1,28	5,89	1,31	6,66
2H	10	<111>	1	5,85	1,23	8,19	1,21	8,18	1,16	7,85
3H	10	<111>	1	5,35	<u>1,46</u>	8,12	1,44	8,83	1,30	8,32
4H	10	<111>	1	5,04	1,22	6,92	1,33	8,73	1,32	9,35
14H	10	<111>	1	5,14	1,16	6,86	1,18	7,35	1,17	7,51
2T	10	<100>	1	5,52	1,11	7,01	1,12	7,34	1,12	7,62
3T	10	<100>	1	5,40	1,21	7,82	1,23	8,56	1,27	10,2
5T	10	<100>	1	5,92	1,14	9,03	1,19	11,3	1,19	12,8
3E ⁽³⁾	40	<111>	1	5,57	1,26	7,23	1,25	7,63	1,18	7,50

Notes relating to Table 2D :

- 1 The K'-values for the GAT devices have been normalized and relate to a standard transistor of the same gain as the measured GAT.
- 2 In computing the n-values for the GAT transistors in the first row, it was assumed that n for a standard device was 5.
- 3 Epitaxial wafer as used for PT014.

2.6.4.5 Observations on other results obtained

Device gain was very difficult to control as it was additionally dependent on

- (a) consistency of the critical spacing between deep P-diffusions, which required particularly tight process control over photolithography; and
- (b) the deposition resistivity and diffusion depth control of the deep P-region.

The inclusion of the deep P-diffusion had little effect on the measured values of collector resistance of the devices on epitaxial substrates, so an overall reduction in device area of about 10 to 20 per cent would have been possible.

2.6.4.6 Decision not to produce GAT devices for the PT014 application

In comparison with the PT014, a device that more than adequately met the electrical design objectives and was produced at an acceptable cost, the marginal improvements offered by the GAT were quite offset by a number of negative factors, as follows.

- (a) Design data were both inadequate and inaccurate in the cases investigated, implying that a considerable additional development effort was required.
- (b) Control of gain was dependent on the additional variables listed above, where the difficulty of instituting suitable process controls was considerable.
- (c) The cost of instituting an additional masking step would offset the anticipated advantage of a 20 per cent decrease in the active area of the device.

Nevertheless, the foregoing experiments have shown that, in principle, the GAT operates as originally described, and thus other benefits claimed for

the structure could be of importance in different applications. If, for example, devices with the combined properties of high breakdown voltage, fast switching speeds and minimum collector resistance were required, further development of the GAT should be worth while.

2.7 CONCLUSION

In this chapter the proved design methodology has been documented for a highly specialized high-voltage surge-resistant planar transistor, developed for use in the Protea telephone. The aim of the project was achieved with outstanding success, and almost 1,5 million PT014 transistors have been produced for the application.

What is even more important, however, is that the investigations have yielded a number of new valuable findings relevant to transistor design. These are listed below.

- (a) The punchthrough collector design provides a method of achieving stable breakdowns controlled only by a geometrical factor without recourse to complex junction termination procedures.
- (b) Interdigitated emitter structures should not be resorted to automatically, but should be considered only if high-injection levels are anticipated. With simple emitter structures the gain remains virtually constant over a wider range of collector currents; and higher yields on emitter-base leakage current may be obtained.
- (c) Note was taken of a previously unobserved reversible leakage phenomenon, and a light emission phenomenon associated with the former, these being the result of the inclusion of small P-diffused areas in the lateral collector depletion region. This depletion region must be clear to the equipotential ring if no P-guard rings for field distribution are included.
- (d) It was proposed that by means of equation 2.6B (page 37) a peripheral correction should be made to the emitter area when calculating the corrected collector resistance of a transistor, this correction factor being found to be more accurate than existing ones used to compensate for parasitic collector resistance. As the proposed

factor is a peripheral correction it is of application to virtually any emitter geometry and any thickness of silicon below the emitter-base junction.

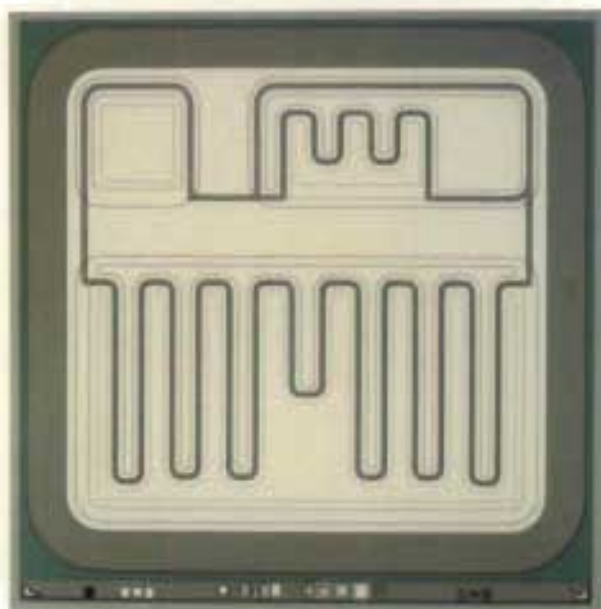
- (e) It was found that the finger spacing on most commercial high-voltage, medium-power devices is too large, and the effective active area is reduced, resulting in increased collector resistance. The spacing between the emitter fingers should be less than the minimum epitaxial layer thickness. (This may be deduced from Figure 2.12c on page 38.)
- (f) Useful design curves for a very wide range of epitaxial layers were obtained. With these curves it becomes a simple matter for a designer to derive a specification for an epitaxial layer thickness and resistivity once the required transistor gain and collector-emitter breakdown voltage are known.
- (g) The gate associated transistor has been shown to provide a useful increase in BV_{CEO} over that anticipated from a standard transistor structure. Design data for the GAT are inadequate and the design equations were not accurate within the limits used in the experiments.

The area where questions may arise concerning the design of the PT014 is in the target values of breakdown voltage and gain that were used in Sections 2.5.1.2 and 2.5.1.3 for the epitaxial layer specification. Whilst for practical purposes the generous allowances that were made have proved to be more than adequate during the production phase, a sounder basis for judging such target values is desirable. In Chapter 4 of this thesis, where numerical analysis techniques are described that were developed to model saturation in high-voltage transistors, the computer programs developed are directly applicable to the determination of epitaxial layer specification limits from worst-case transistor parameters.

PLATE 2 : THE LOREA AND DISA PUSH-BUTTON DIAL TELEPHONES
AND THE PT018 INTEGRATED DARLINGTON TRANSISTOR DIE



The Lorea and Disa impulse push-button dial telephones for loop disconnect dialling, and the die of the PT018 high-voltage high-gain integrated Darlington transistor that was developed for use in the dial circuits of both of these telephones.



(Die size is 1,4 x 1,4 mm)

CHAPTER 3

HIGH-VOLTAGE DARLINGTON TRANSISTOR TYPE PT018 FOR THE IMPULSE
PUSH-BUTTON DIAL TELEPHONE

3.1 SUMMARY OF CHAPTER

Details are given of an unprecedented success in South African micro-electronics. A high-voltage integrated Darlington transistor was developed incorporating several unique features, to meet the electrical requirements of an electronic impulse push-button dial telephone that had been designed for use in the national telephone network.

This undertaking was handled in a manner unique in the local context. For very sound reasons the approach avoided was that of making an integrated equivalent of the two discrete transistors used during dial development, which transistors had parameters not necessarily related to the application. The new device was developed to meet an electrical specification that was drawn up to satisfy the combined requirements of the dial circuit and telephone system. This novel approach resulted in a highly cost-effective design that was better suited to the dial application than the two discrete transistors used originally.

Another advantage of this initiative taken in developing an integrated device, only marginally larger than any one of the two discrete transistors was that it obviated the necessity of demanding from the NEERI IC Facility that an unrealistically large volume of devices should be produced. This facility had the planar high-voltage transistor process developed for the PT014, and although the devices that could be manufactured by means of this process differed in a number of respects from the transistors used during the development of the dial, the process proved to be well suited to the production of integrated Darlington transistors for the application.

A further advantage was that the thorough investigations undertaken also highlighted the key failure mechanisms likely to be encountered in service. As a result it was possible to design a device immune to external breakdown, one of the major failure modes of high-voltage transistors subjected to the surge conditions commonly occurring in the field.

A number of aspects of this work, mentioned below, led to considerations regarded as important contributions to the art of designing high-voltage Darlington transistors.

(a) Optimization of the active area of the device

For economic reasons it was vital to minimize the active area of the transistor without reducing the combined yield on low-voltage gain at the upper current limits and the high breakdown voltages that were essential to the application. Here the methods used were particularly successful.

(b) Partitioning of the active areas of the driver and output stage

In integrated Darlington transistors the industry traditionally allows for area ratios of the output stage to the driver stage that are as high as twenty-five to one. For the operating conditions in this design it was found that, when quasi-saturation conditions were taken into account, optimum saturation performance was obtained with an area ratio of only six to one.

(c) Development of the 'Inverted Metallization' (IM) structure

Critical evaluation of external breakdown phenomena in high-voltage transistors showed that this was an aspect that had been given too little attention by transistor designers. The findings led to the development of a revised transistor layout technique with an 'Inverted Metallization' (IM) structure where the emitter metal rather than the base metal was used to surround the whole device and act as a combined field plate and external electrostatic guard ring. Devices made using this layout technique have shown both remarkably stable and extremely low leakage currents at reverse-bias voltages of several hundred volts.

(d) A unique clamp circuit

A further development was the incorporation into the Darlington transistor of a novel clamp circuit to equalize the values of BV_{CEO} , BV_{CBO} and BV_{CBS} . This innovation made it possible to reduce the chip area significantly by reducing the clearances required to prevent external breakdown phenomena.

(e) Device quality specification

The author was intimately involved when a comprehensive Quality Assurance specification was drawn up for the integrated Darlington transistor, this being the first such specification ever drawn up for a locally designed and developed semiconductor component.

3.2 PROJECT PROPOSAL FOR THE USE OF A HIGH-VOLTAGE INTEGRATED DARLINGTON TRANSISTOR IN THE IMPULSE PUSH-BUTTON DIAL TELEPHONE

On the instructions of the South African Department of Posts and Telecommunications, an impulse push-button dial (IPB) telephone for loop disconnect dialling had been developed by a local commercial company for use in the South African telephone system.

Figure 3.1 (page 57) shows a simplified diagram of the telephone. The transistors TR1 and TR2 as well as TR3 and TR4 are connected in Darlington configuration and form buffers for the CMOS dial circuit. Initially the CSIR was requested to investigate the feasibility of diffusing high-voltage, medium-power transistors equivalent to the type 2N3439 devices that were used during dial development. As the PT014 transistor development and production programmes had been extremely successful the author, who had steered these, was appointed to head this project. As will be seen below, the development of an integrated Darlington transistor to take the place of both of the discrete transistor pairs was finally agreed to and became the subject of the development programme undertaken.

3.3 REASONS FOR DEVELOPING THE PT018 INTEGRATED DARLINGTON TRANSISTOR

3.3.1 Defining the target parameters of the buffer stages

A careful analysis of the project proposal revealed that it was unrealistic to attempt to employ the CSIR planar epitaxial process to make a direct equivalent of the transistor type 2N3439, a device that was made in Mesa technology. Further, the 2N3439 type had been used in the dial only because it was a readily available commercial device that seemed to perform the function satisfactorily, but was one that had never been field-proved, hence the actual circuit requirements still had to be accurately defined and a detailed specification drawn up for the Darlington buffer stages.

SIMPLIFIED DIAGRAM OF THE LOREA IMPULSE PUSH-BUTTON
DIAL TELEPHONE IN THE OFF-HOOK CONDITION

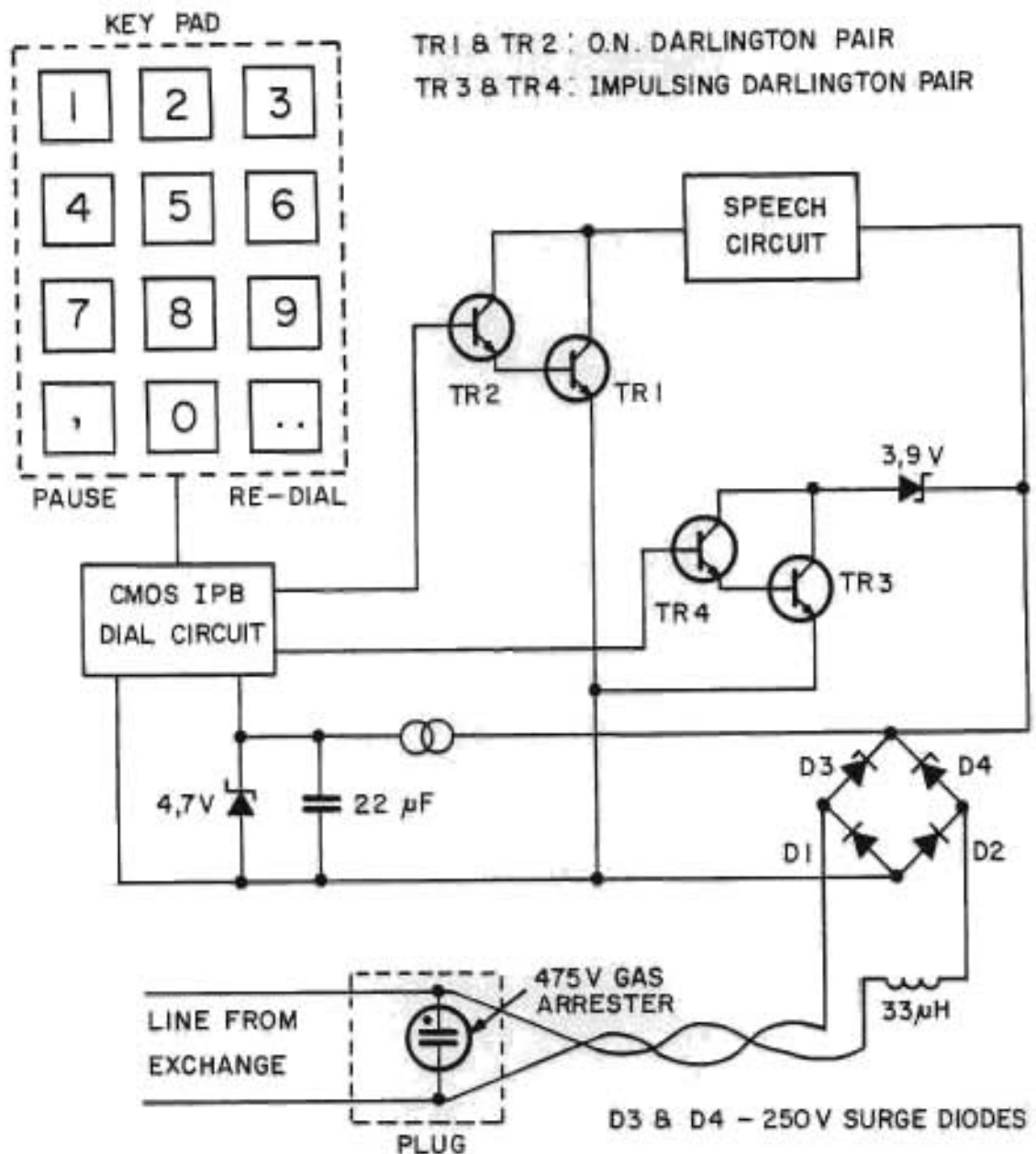


FIGURE 3.1 SIMPLIFIED LOREA IPB DIAL TELEPHONE IN THE OFF-HOOK CONDITION SHOWING THE O.N. AND IMPULSING DARLINGTON PAIRS AND THE BASIC SURGE PROTECTION CIRCUITRY CONSISTING OF A GAS ARRESTER, INDUCTOR AND SURGE DIODES.

The author proposed that the following essential activities be undertaken.

- (a) The telephone manufacturer should carry out in-circuit measurements on the buffer stages, regarding each stage as a three-terminal device, at the limiting conditions of operation of the telephone. The results would establish the essential saturation limits and gain minima required for each buffer stage.
- (b) Impulse voltages across the buffer stages, encountered during dialling and under surge conditions, should be recorded to establish the minimum breakdown voltages required.
- (c) Data pertinent to the limiting operating currents of both the telephone and exchange should be made available to enable maximum leakage currents for the Darlington pairs to be established.

Appendix 3.1 (page 235) records the data supplied by the telephone manufacturer. Whilst the information regarding (a) above was exhaustive and partially complete regarding point (b), the data mentioned in (c) was not supplied. After receipt of this document the aim was to provide a device to meet the electrical requirements both economically and in a form that could be produced in suitable volumes by the NEERI IC Facility. The various steps taken towards this goal are described below.

3.3.2 Evaluation of the PT014 in the buffer application

To verify that the planar process in use for the PT014 would be suitable for the production of a high-voltage buffer, PT014 devices, which by coincidence had the same approximate area as the 2N3439 but a rather lower breakdown voltage, were evaluated for application in the buffer stages.

From the data supplied in Appendix 3.1 (page 235), a skeleton specification was drawn up, covering the most important electrical requirements for a discrete transistor for use in a Darlington configuration in the buffer stages of the the dial. This specification is reproduced in Appendix 3.2 (page 237). Four specially selected PT014 transistors with limiting values of lower and upper gains, in terms of the TR2 - Issue 3 specification, were

connected as Darlington pairs and measurements were made to evaluate conformance with the skeleton specification. The results presented in Figure 3.2a and 3.2b (page 60) clearly show that the PT014 met the gain requirements admirably. It should also be noted that the gain performance of a sample pair of 2N3439 devices supplied by the telephone manufacturer was not as good, and that these devices could not satisfy one of the fault conditions specified.

Tests carried out in the telephone showed that pairs of uprated PT014 transistors, specially processed to meet the higher breakdown requirements of the skeleton specification reliably, performed in exemplary fashion. No failures occurred when the telephone was subjected to the 4 kV surge test of 1,2 microsecond risetime and 50 microsecond duration that had been specified for lightning simulation. Under these surge conditions the 475 V gas arrester in the plug of the telephone always struck in just over 1 μ s, and devices with a $BV_{CEO} > 300$ V were found to be adequate, as additional protection was afforded by the 250 V surge diodes on the dial printed circuit board (Holmes, pers. comm.⁸).

3.3.3 Proposal for the integrated Darlington transistor

An uprated PT014 could not be produced in sufficient volume at the CSIR, nor could the cost target be met. For these reasons, and also because it offered the advantages listed below, an integrated high-voltage Darlington transistor was proposed.

- (a) The Darlington would meet the required electrical performance with a die that would be only some 20 per cent larger than a discrete device.
- (b) The overall cost of components in the telephone would be reduced since only one instead of two transistor packages would be employed, the increased die cost being more than offset by the use of one package.
- (c) The component inventory for both the manufacturer and the Post

⁸R Holmes (1980) Telephone Manufacturers of South Africa (Pty) Ltd, P O Box

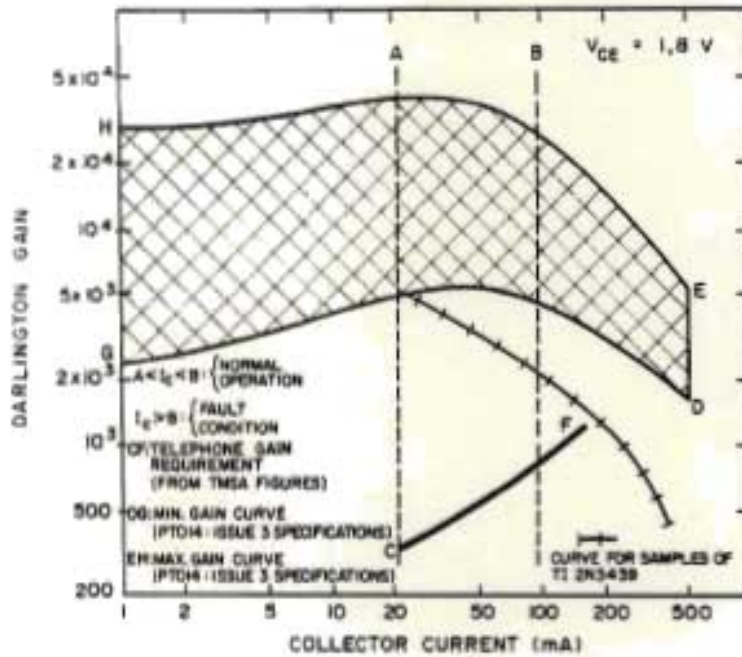


Figure 3.2a

O.N. condition

THE CROSS-MATCHED REGION SHOWS THE GAIN ENVELOPE WITHIN WHICH THE DARLINGTON GAIN OF TWO PTO14 TRANSISTORS (SORTED TO THE TR2-ISSUE 3 SPECIFICATION) SHOULD LIE.

LINE CF IS THE MINIMUM GAIN REQUIREMENT OF THE TELEPHONE FOR THE FULL RANGE OF OPERATING CONDITIONS. THE PTO14 DEVICES WILL EXCEED ALL THE GAIN REQUIREMENTS OF THE TELEPHONE.

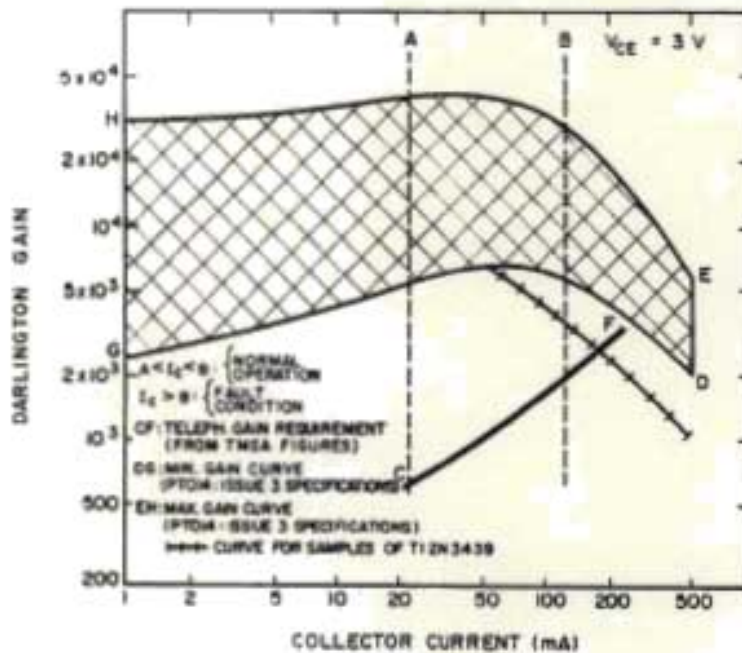


Figure 3.2b

Impulsing condition

THE DESCRIPTION OF THE CURVE IS AS IN FIGURE 3.2a

IT SHOULD BE NOTED THAT THE DARLINGTON MADE OF TWO PTO14'S AGAIN EXCEEDS THE MINIMUM GAIN REQUIREMENTS OF THE TELEPHONE. THIS IS NOT THE CASE FOR THE SAMPLE 2N3439 DEVICES.

Office Service Department would be reduced, also the parts count on the dial boards; this would automatically improve the reliability of the telephone.

- (d) Electrical tests at all stages of manufacture would be both simplified and reduced.
- (e) The NEERI IC Facility could meet the production demanded.

All parties agreed that an integrated device should be developed, and finally it may be observed that the fact that the device was unique and that no similar high-voltage device existed obviated the need, when the specification was drawn up, to consider extraneous factors that would be irrelevant for this specific purpose.

3.4 THE ELECTRICAL SPECIFICATION FOR THE PT018 INTEGRATED DARLINGTON TRANSISTOR

Table 3A on page 62 gives the final electrical specification for the PT018 Darlington drawn up by the author and accepted by all parties. A short discussion of the origin of each set of test conditions listed in the specification follows the table, as does a consideration of temperature effects.

3.4.1 A discussion of the specified tests in Table 3A

Test 1 Functional tests

The two tests for $V_{BE(SAT)}$ and $V_{CE(SAT)}$ included in Test 1 are termed 'functional tests' and are carried out at the beginning of an automatic test procedure simply to ensure that a device is actually being tested and that good electrical contact has been made. The test listing enabled either re-tests to be decided upon or test statistics to be corrected.

Test 2 The sustaining voltage - $V_{CEO(SUS)}$

The figure of 300 V was suggested by the telephone manufacturer (see Appendix 3.1 from page 235), presumably on the basis of measurements

Table 3A : The primary electrical specification for an integrated Darlington transistor at $25 \pm 5^\circ\text{C}$

Test No.	Parameter	Test condition	Value		Unit
			Min	Max	
1	$V_{BE(SAT)}$	$I_C = 100 \text{ mA}$		2	V
	$V_{CE(SAT)}$	$I_B = 1 \text{ mA}$		1,6	V
2	$V_{CEO(SUS)}$	$I_C = 10 \text{ mA}$ $I_B = 0$ Time < 250 ms	300		V
3	BV_{CBO}	$I_C = 100 \mu\text{A}$ $I_E = 0$	300		V
4	BV_{EBO}	$I_B = 20 \mu\text{A}$ $I_C = 0$	10		V
5	I_{CEO}	$V_{CE} = 240 \text{ V}$ $I_B = 0$		500	μA
6	I_{CBS}	$V_{CB} = 240 \text{ V}$		100	μA
7	I_{CBO}	$V_{CB} = 240 \text{ V}$ $I_E = 0$		5	μA
8	I_{EBO}	$V_{EB} = 6 \text{ V}$ $I_C = 0$		1	μA
9	$h_{FE(1)}$	$I_C = 100 \text{ mA}$ $V_{CE} = 1,8 \text{ V}$	800		-
10	$h_{FE(2)}$	$I_C = 125 \text{ mA}$ $V_{CE} = 3 \text{ V}$	1 800		-

(Test 2 continued)

made. The author later found that this figure was questionable and thus an additional safety margin was built into the PT018. A test current of 10 mA was adopted, as this could easily be sustained by the device for periods of up to 1 s and as the

magnitude of the current was not really relevant to the application, as leakage currents at 240 V were defined. At a later stage, as discussed in Section 3.9.3, it was found that the sustaining current of 10 mA did indeed highlight an assembly problem.

Test 3 Collector base breakdown - BV_{CBO}

A value of 300 V was indicated in Appendix 3.1 (page 235) and was agreed to, as there was no circuit requirement suggesting that the collector-base breakdown voltage should be higher than the collector-emitter value. A test current of 100 μ A was used, as this would help ensure 'hard' or low leakage junctions with a sharply defined breakdown characteristic.

Test 4 Emitter-base breakdown voltage - BV_{EBO}

From Appendix 3.1 (page 235) a figure of 7 V was suggested. However, as the dial was fed via a bridge rectifier, there was no actual circuit requirement suggesting the necessity for a reverse breakdown specification. For a Darlington pair with no pull-down resistors between the emitter and base of the output stage, the emitter-base breakdown voltage is twice that of a discrete device. In the planar process that was used, the value of BV_{EBO} of the PT014 type transistor was typically about 9 V. A test figure of 10 V for the integrated Darlington was specified, so that the integrity of the emitter-base junctions of both stages could be checked. An associated test current of 10 μ A was used, as this would ensure that only 'hard' junctions were accepted and as it was a current level that could be handled easily at the probe stage, if required.

Test 5 Collector-emitter leakage current - I_{CEO}

In accordance with standard practice, measurement was made at 240 V, which is 80 per cent of the rated collector-emitter voltage. There was no apparent circuit requirement for an I_{CEO} test, as the base of the driver was at emitter potential with the device off. In this condition only the leakage of the output stage would count. For device integrity, however, a test was introduced. The test limit was set by comparison with a Darlington transistor pair made from

two discrete 2N3439 devices where $h_{FE} \times I_{CEO}$ could exceed 2 mA at 240 V. The driver stage of the integrated Darlington was to be less than one quarter of the area of a 2N3439, hence an upper limit of $I_{CEO} = 500 \mu\text{A}$ was imposed as the amplified leakage current of the driver stage predominated.

Test 6 The collector-base (short) leakage current at 240 V - I_{CBS}

I_{CBS} was an important parameter from the point of view of the dial, as this figure corresponded with the device being off but across the line in the Lorea telephone. It was important that the value of I_{CBS} should be set sufficiently low to obviate interference with key functions. To ensure this, the following had to be taken into account.

- Exchange operation : experiments conducted by the author showed that currents as high as 2 mA could be drawn from the exchange at the subscriber terminal and that such loading had no apparent effect on exchange operation.
- Telephone operation : high leakages could be tolerated here, but a subjective limit of a few hundred μA was indicated, as clicks during dialling became prominent with exchange back-E.M.F.'s that commonly reached 250 V.
- Line testing : lines were tested with a 250 V megger and it was important that these measurements should not be interfered with. Figure 3.3 (page 65) shows a simplified version of the dial circuit that was used in the Lorea and Disa telephones. The 1 megohm resistor R2, which supplies the dial memory continuously, would pass about 240 μA at 240 V, hence a limit of 100 μA was agreed upon as being acceptably low.

The permissible value of I_{CBS} is discussed further under temperature effects.

Test 7 The collector-base (open) leakage current at 240 V - I_{CBO}

This parameter was not included in the dial requirements but was primarily used as a measure of the quality of the collector-base

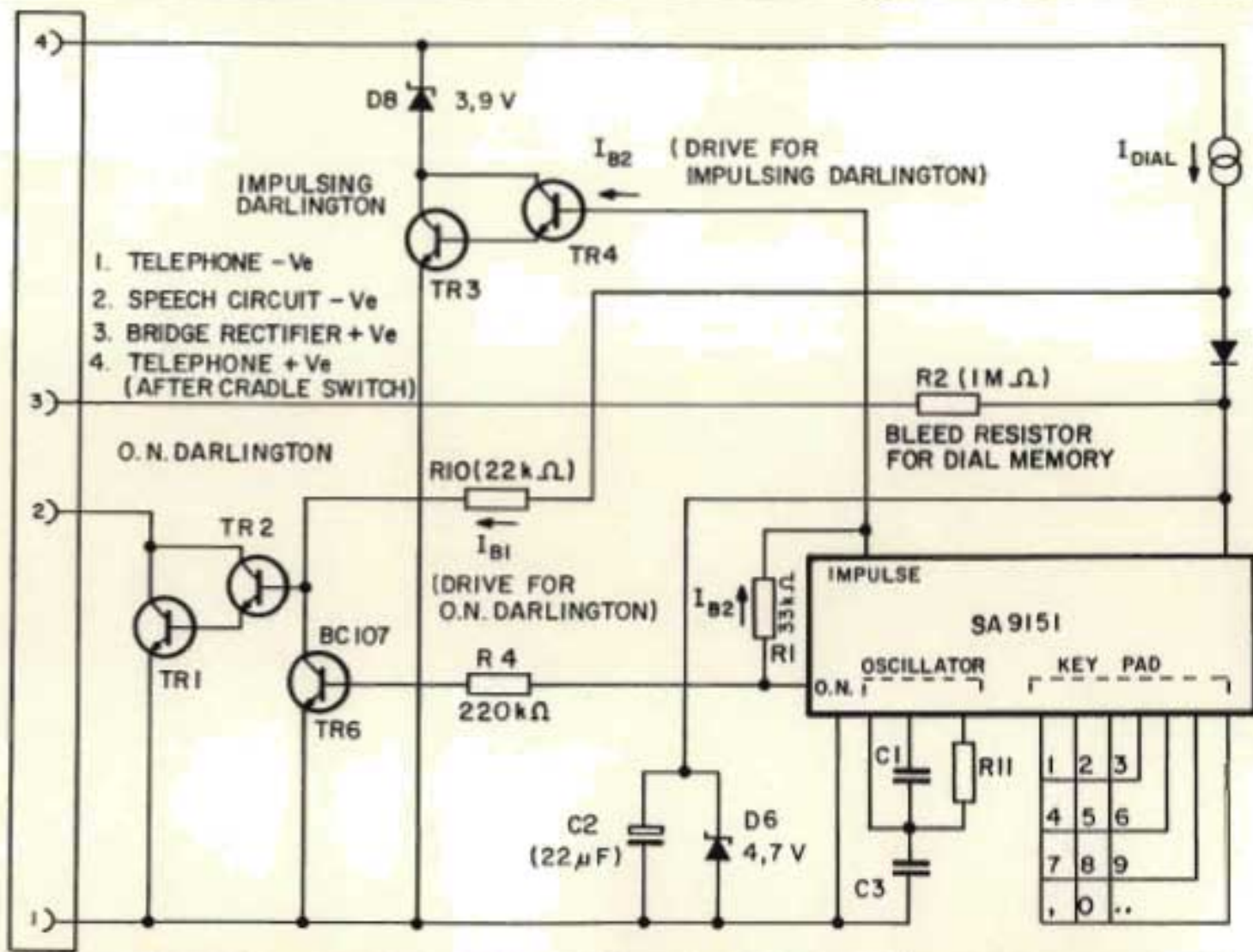


FIGURE 3.3 IMPULSE PUSH-BUTTON DIAL CIRCUIT SHOWING KEY COMPONENTS

junctions of both the driver and output stage in the PT018. As will be seen later, it also provided a measure for the collector-emitter leakage current of the clamp transistor used in the PT018. A limit of $5 \mu\text{A}$ at 240 V was agreed upon as being a value that would be readily applicable on the test gear and would be a useful screen on the device.

Test 8 The emitter-base leakage current - I_{EBO}

As was the case for the emitter-base breakdown voltage, there was no actual circuit requirement for a reverse leakage current test on the emitter-base junction. From experience, the author knew that leaky emitter-base junctions could be readily associated with gain crowding at low collector currents. For this reason a low limit of $1 \mu\text{A}$ was used. The test voltage of 6 V was used in agreement with the customer.

Tests 9 and 10 Gains - $h_{\text{FE}(1)}$ and $h_{\text{FE}(2)}$

These gain limits were derived directly from the short-line condition only, given in Appendix 3.1 (page 235) and have safety margins or 'insets' included.

The short-line condition alone was considered, as this placed the most stringent requirements on the buffers. From Figure 3.2 (page 60) it is clear that the telephone and exchange requirements only approached the gain limits of the device for this condition. A test, for use on a sample basis only, was proposed by the author to ensure the devices were suitable for long-line conditions.

On the instructions of the telephone manufacturer, the line-earthed fault condition where collector currents could almost double was not considered, as this condition could only result in the device being pulled out of saturation and no cases of transistor failure had been observed under such conditions of increased thermal dissipation.

3.4.2 Temperature dependence of leakage currents

Leakage currents are highly temperature-dependent and were not overlooked for the purposes of the specification. The maximum ambient temper-

ature of the telephone was specified as 55 °C, and under these conditions the only critical leakage current, I_{CBS} , should not exceed a value that would interfere with either exchange or telephone operation. As this case would be exceptional it was not considered vital if the 250 V megger readings indicated high leakage.

Figure 3.4 (page 68) shows I_{CBS} as a function of temperature. A tenfold increase in I_{CBS} was recorded for every twenty degrees Celsius increase in temperature, which was anticipated.

Equation 1.288 from Burger and Donovan³¹ gives the leakage current of a reverse-biased diode as :

$$I_{\text{reverse}} = K_1 \times T^{3/2} \times \exp(-E_g/2kT)$$

where K_1 is a device constant;

E_g is the band-gap of silicon;

k is Boltzmann's constant; and

T is the absolute temperature.

For a reverse-biased PN junction this gives an approximately tenfold increase in leakage current for every 30 degrees increase in temperature. In this case the leakage current measured is primarily the leakage current appearing in the base circuit of the Darlington output stage. The gain of this transistor must thus be included in the leakage equation. As shown in equation 1-290³¹, transistor gain has a significant positive temperature coefficient, thus the measured rate of increase of leakage current was realistic.

Returning to the application in the telephone, it was expected that the leakage current in a worst-case device at 240 V could rise to a limit of about 3 mA per device at a temperature of 55 °C with the telephone on-hook, giving a total for the instrument, with two Darlington transistors, of some 6 mA. This would give rise to an unsatisfactory reading on a megger test but would not interfere with telephone operation at an exchange voltage of 50 V : measurements made on a number of prototype PT018 devices showed that the leakage current would drop by a factor of about ten or more when the applied voltage was reduced from 240 to 50 V, giving an acceptable total leakage current for the telephone of less than 0,7 mA at 55 °C.

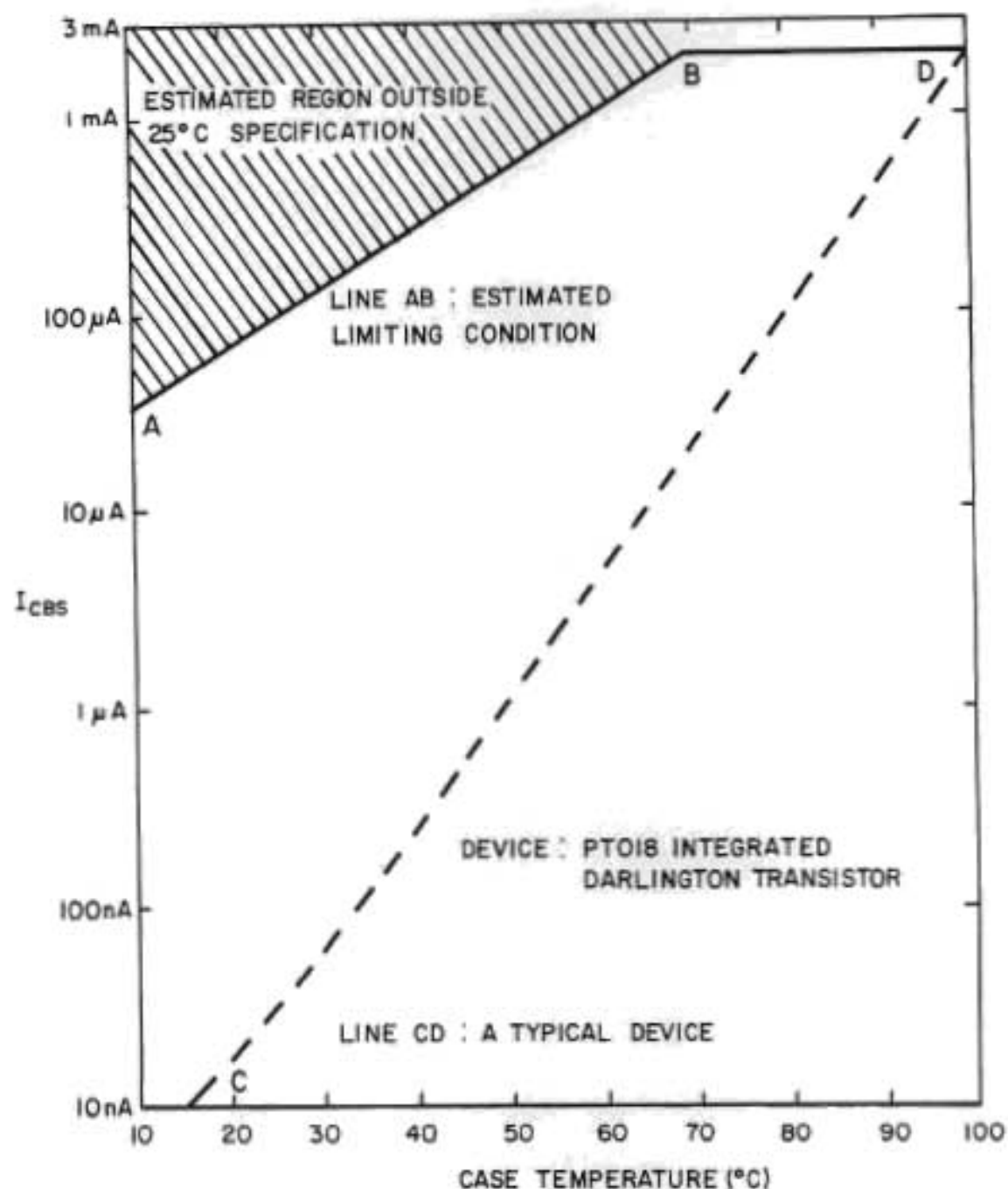


FIGURE 3.4 I_{CBS} AS A FUNCTION OF TEMPERATURE FOR A PTO18 INTEGRATED DARLINGTON TRANSISTOR, TOGETHER WITH THE ESTIMATED LIMITING CONDITION. THE LEAKAGE CURRENTS ARE A STRONG FUNCTION OF TEMPERATURE AND REPRESENT THE LEAKAGE CURRENT OF THE CLAMP TRANSISTOR AMPLIFIED BY THE OUTPUT STAGE.

3.5 TEST VEHICLES USED IN THE DESIGN, DEVELOPMENT AND EVALUATION OF THE PTO18 HIGH-VOLTAGE INTEGRATED DARLINGTON TRANSISTOR

Before the design of the prototype Darlington devices is considered, some of the test structures included on the same photomasks are described.

3.5.1 A discrete device

It was decided to include on the test wafer the #/014 transistor geometry to act as a control transistor, as the device had been extremely well characterized and was capable of fulfilling the requirements of a discrete device for the Darlington stages. It was anticipated that with a modified epitaxial layer giving an increase in BV_{CEO} from 250 V to 350 V, which was regarded as a good target value for the prototype Darlington transistors, the #/014 transistor would exhibit poorer, but adequate, saturation characteristics. Breakdown stability was, however, the only difficulty with the #/014 transistor layout. Unstable collector-base characteristics at reverse voltages of over 500 V had occasionally been noted with this die when tested in air, particularly at high relative humidity levels. (See Section 2.5.6, page 30.) These effects had not been observed on devices when tested either under a dry nitrogen blanket or after encapsulation in hermetic packages. As a result it was anticipated that with the increased values of BV_{CBO} that were expected, instabilities might occur. No instability in BV_{CEO} was anticipated at 350 V, however.

3.5.2 A test structure for high-voltage requirements

The #/118T test structure shown in Figure 3.5a (page 70) was designed in order to evaluate :

- (a) oxide dielectric strengths available in the process;
- (b) lateral depletion requirements for the collector-base junction; and
- (c) clearances required between metallization and the scribe channel.

This test structure confirmed that the dielectric properties of the process oxides were excellent, and in addition the isolated aluminium pads

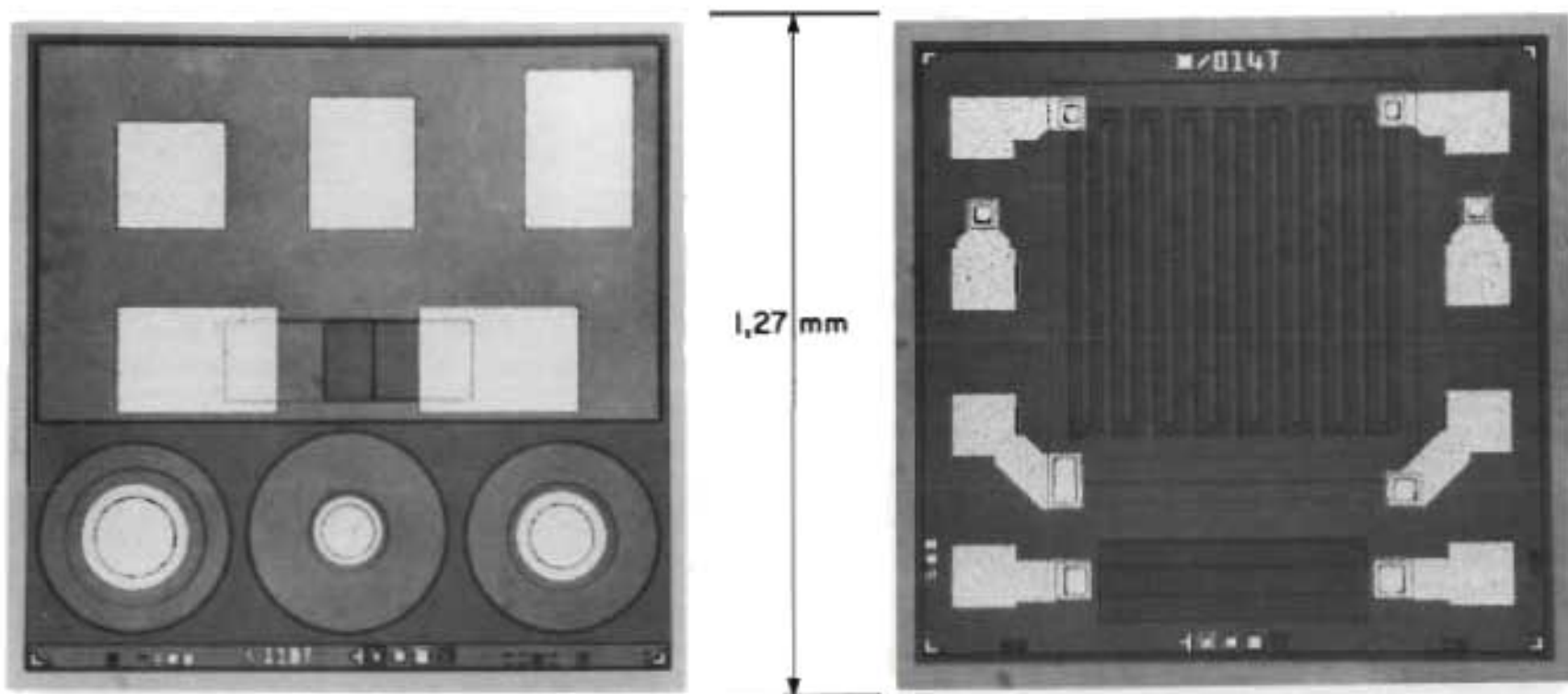


FIGURE 3.5a TEST STRUCTURE USED ADJACENT TO PROTOTYPE DARLINGTON TRANSISTORS TO EVALUATE:

- a. OXIDE DIELECTRIC STRENGTHS USING THE TWO RECTANGULAR PADS IN CENTRE OF PATTERN;
- b. LATERAL DEPLETION CLEARANCE. (CLEARANCES OF 50, 75 AND 100 μm WERE USED IN THE CIRCULAR DIODES AT THE BASE OF THE PATTERN);
- c. METAL TO SCRIBE CHANNEL CLEARANCE REQUIRED (ISOLATED PADS AT TOP OF PATTERN WERE 50, 100 AND 150 μm FROM THE SCRIBE CHANNEL RESPECTIVELY).

FIGURE 3.5b DROP-IN TEST STRUCTURE FOR PROCESS CONTROL. USED WITH PROTOTYPE AND PRODUCTION DARLINGTONS. COMPONENTS:

- a. A 500 SQUARE EMITTER RESISTOR (TOP);
 - b. A 20 SQUARE BASE RESISTOR (CENTRE);
 - c. A 10 SQUARE PINCH RESISTOR (BOTTOM).
- ALL PARAMETERS SUCH AS GAIN AND BREAKDOWN VOLTAGES MAY BE MEASURED WITH THIS STRUCTURE.

on the $1,3 \mu\text{m}$ thick field oxide yielded the following most significant finding : External field strengths of 50 kV/cm could be sustained without any discharge on the two pads that were 50 and $100 \mu\text{m}$ from the bare N^+ scribe channel. A field strength of only 40 kV/cm could be sustained on the pad that was $150 \mu\text{m}$ from the scribe channel, indicating that for collector-base breakdown voltages exceeding 500 V , lower critical field-strengths were applicable.

3.5.3 A process-control test structure

For the purposes of monitoring process uniformity and repeatability, a test structure, the $\#/014\text{T}$, was included on the photomasks. Figure 3.5b (page 70) shows this device, which was merely a refined version of the test circuit that was used in the development of the PT014 (Figure 2.7d page 26).

3.6 DESIGN CONSIDERATIONS FOR THE PROTOTYPE INTEGRATED DARLINGTON TRANSISTORS

3.6.1 External breakdown phenomena : The inclusion of a clamp transistor to limit external fields and to reduce the total area of the Darlington

In designing the integrated Darlington transistor it was essential to eliminate possible environmentally-dependent breakdown instabilities as experience had revealed susceptibility of the $\#/014$ to instabilities in the BV_{CBO} characteristic, described above, and a detailed field failure analysis study of TR2-type transistors from the Protea telephone carried out by the Dept of Posts and Telecommunications and reproduced in Appendix 3.3, (page 238) had shown that a number of transistors had failed owing to external breakdown phenomena. Figure 3.6 (page 72) shows a device that failed in service as a result of external breakdown phenomena when the field between the N^+ scribe channel and base metallization had become too great.

In the case of many devices it happens in practice that as the collector-emitter voltage is increased rapidly with the base circuit open, the collector-emitter voltage reaches a value approaching BV_{CBO} before the breakdown voltage suddenly collapses to the value of the lower collector-emitter breakdown voltage. This effect is termed 'latchback', and devices

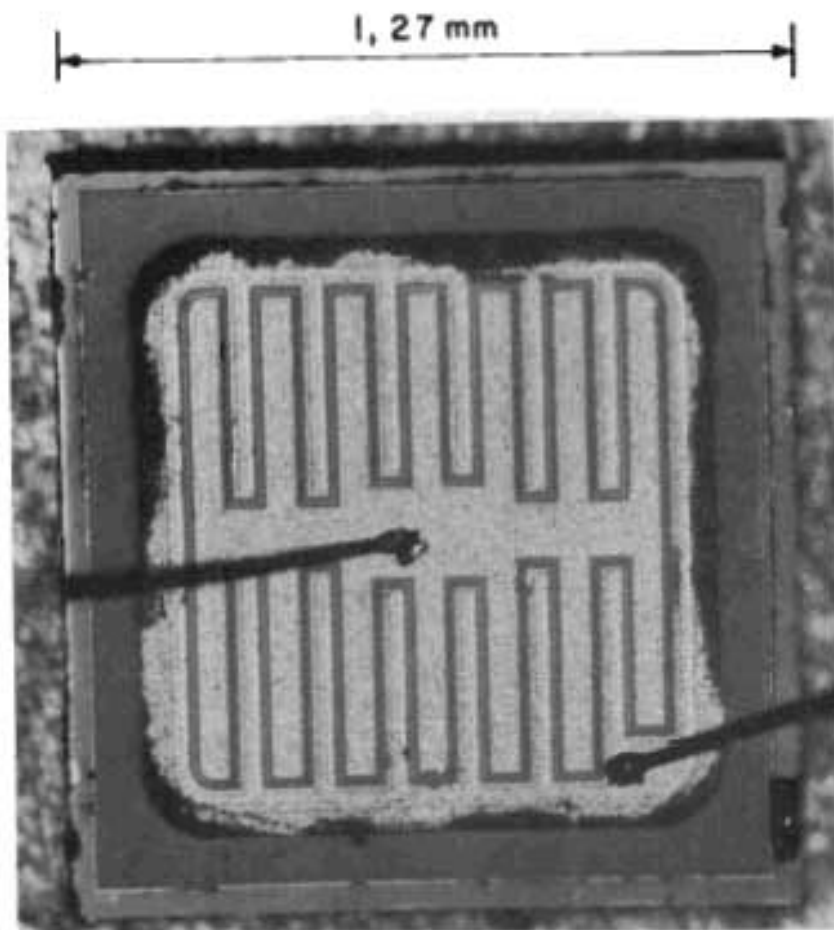


FIGURE 3.6 A TEXAS INSTRUMENTS TRANSISTOR THAT FAILED IN SERVICE, IN A PROTEA TELEPHONE, DUE TO EXTERNAL BREAKDOWN BETWEEN THE SCRIBE CHANNEL (AT COLLECTOR POTENTIAL) AND THE BASE METALLIZATION. THE DEVICE SHOWED A LOW COLLECTOR - EMITTER IMPEDANCE. AFTER CLEANING IN A SOLVENT, THE DEVICE OPERATED AGAIN AND MET THE TR2 - ISSUE 3 SPECIFICATION.

(FAILED DEVICE SUPPLIED BY THE QUALITY ASSURANCE INSPECTORATE, DEPT. OF POSTS AND TELECOMMUNICATIONS, PVT. BAG X 74 PRETORIA 0001, SOUTH AFRICA).

exhibiting this phenomenon are far more likely to suffer a destructive external collector-base discharge than devices in which the effect is minimal. Experience with the PT014 had shown that latchback effects were essentially absent in both the process and layout used. Nevertheless external breakdown between the collector and base was a phenomenon that had been frequently observed by the author on a large number of high-voltage, medium-power transistors. In the case of a working device similar to the failed transistor shown in Figure 3.6 (page 72), a reverse-bias stress of only $100 \mu\text{A}$ at 500V on the collector-base junction was sufficient to cause a collector-base short owing to external breakdown and tracking. (BV_{CBO} for this device was over 650V and the clearance from metal to scribe channel was about $80 \mu\text{m}$.)

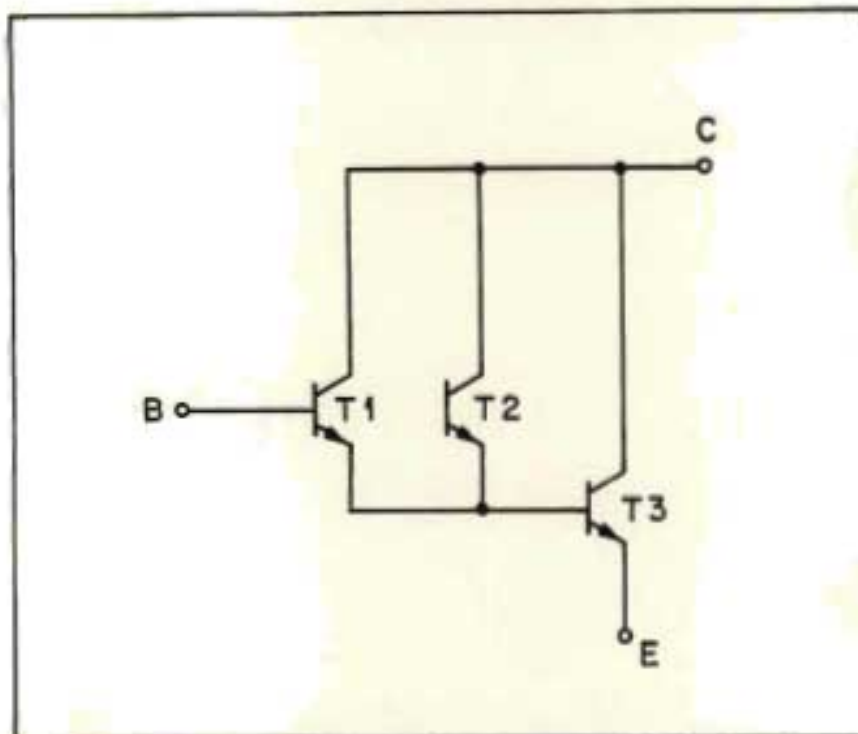
A subsequent investigation on 2N3439 devices from six different manufacturers showed that in five cases a small stress on the collector-base junction was sufficient to either destroy or degrade the transistor. In no case could these junctions be stressed to more than a few mA before external breakdown took place, despite the fact that the 2N3439 had a rated $V_{\text{CEO(SUS)}}$ of 350V at 50mA !

It was only well after this development work had been completed that useful publications appeared dealing with junction termination that included external conditions as well. A review by Baliga³² described the state of the art in 1982; edge effects on glass-passivated collector-base junctions were reported on by Savini et al.³³, and more specific attention was given to planar junction termination by Yasuda and Yonezawa of Toshiba³⁴. The 1983 Toshiba 'Supreme Power Transistor' catalogue³⁵ was the first trade publication encountered by the author in which were described commercially available products, both bipolar and MOS, that had been designed with due precautions for the elimination of external junction termination problems. None of the techniques described for junction termination was readily applicable to the NEERI high-voltage planar technology.

3.6.1.1 Limiting external fields with a clamp transistor

To reduce external fields, a clamp transistor was incorporated as shown in Figure 3.7 (page 74), and it had the effect of equalizing BV_{CEO} , BV_{CBS} and BV_{CBO} to within the BV_{EBO} value of the driver, T1. It had been

FIGURE 3.7 THE BASIC INTEGRATED DARLINGTON TRANSISTOR .



THIS SCHEMATIC SHOWS THE CIRCUIT CONFIGURATION OF THE INTEGRATED DARLINGTON TRANSISTOR USED IN BOTH THE PROTOTYPE AND PRODUCTION DEVICES DESCRIBED IN THIS CHAPTER

- T 1 - THE DRIVER TRANSISTOR
- T 2 - A CLAMP TRANSISTOR (TO EQUALIZE BV_{CEO} BV_{CBO} AND BV_{CBS})
- T 3 - THE OUTPUT TRANSISTOR

NOTE: NO PULL-DOWN RESISTORS OR COLLECTOR DIODES ARE INCLUDED.

found on the PT014 that external field strengths of 50 kV/cm could be tolerated with the transistor in dry nitrogen, a rather higher figure than the 43 kV/cm reported by Zoroglu and Clark²¹. In the design of the prototype Darlington transistors, nominal clearances of about 100 μm between metallization and scribe channel were adopted, and it was later shown that values of BV_{CEO} of up to 500 V with no instabilities could be achieved in air.

The decision to include in the design a clamp transistor that could sink reverse currents greater than 10 mA for periods of 1 second or more, was obviously well justified as it had the effect of limiting external fields both simply and reliably. The high-voltage failure mode was no longer found to be external in any cases observed, and in the case of all surge test failures only the output transistor was damaged.

3.6.1.2 Effect of the clamp transistor on leakage currents

Although it was clear that when measuring I_{CBO} in the integrated Darlington transistor the I_{CEO} value of the clamp transistor would predominate and that I_{CBS} would be approximately $h_{\text{FE}} \times I_{\text{CEOCL}}$, it was found in later production that at 240 V, values of I_{CBO} and I_{CBS} were typically in the low nA region or even less than 1 nA at room temperature.

3.6.1.3 High-temperature effects

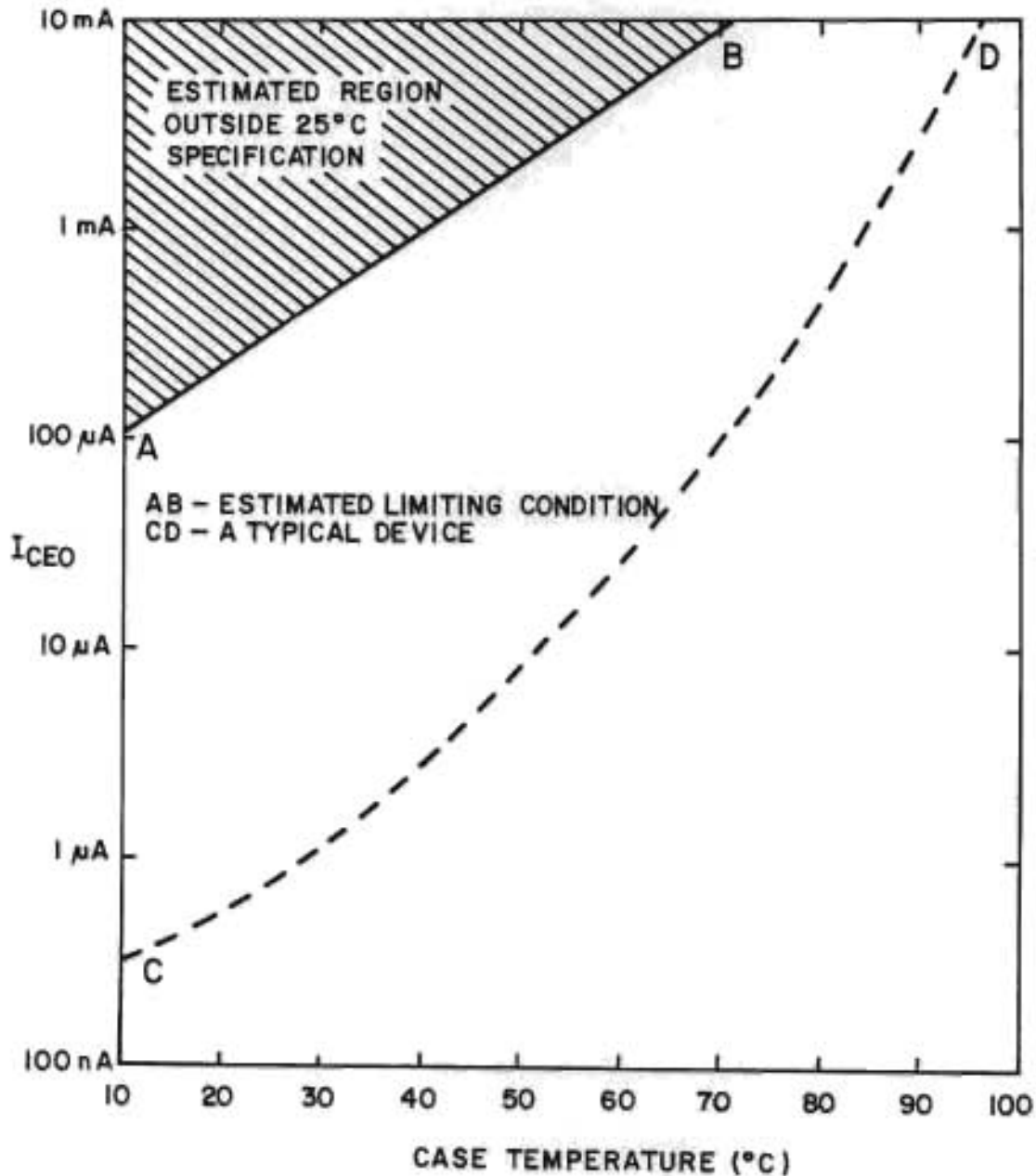
Where junction temperatures greater than 100 $^{\circ}\text{C}$ are expected, use of such clamp devices without pull-down resistors must be considered carefully, as leakage currents across the collector-emitter terminals of the Darlington are a very strong function of temperature, as shown in Figure 3.8 (page 76). Junction temperatures in the region of 90 $^{\circ}\text{C}$ maximum were projected for the practical application of this device, and the reverse-bias accelerated-life testing was limited to 100 $^{\circ}\text{C}$ in order to prevent thermal runaway in the case of devices with leakage currents near the specified limits.

3.6.1.4 The clamp device to reduce the total Darlington area

For the economic reason of having as many integrated devices per wafer as possible, it was essential that the integrated device should not be

FIGURE 3.8

COLLECTOR-EMITTER LEAKAGE CURRENT OF A PTO18 TRANSISTOR AS A FUNCTION OF CASE TEMPERATURE. THE STRONG TEMPERATURE-DEPENDENCE IS DUE TO THE LACK OF ANY PULL-DOWN RESISTORS IN THE BASE CIRCUIT OF THE OUTPUT STAGE.



significantly larger than the $\mu/014$. The value of BV_{CEO} was to be increased to 350 V, and using equation 2.5A (page 20), to relate gain and breakdowns, with $n = 5$ and a gain of 100 the projected value of BV_{CBO} was almost 900 V. Here it was anticipated that the clearance from metal to scribe channel would have to have been increased from 100 μm to at least 180 μm if the clamp transistor were left out. On a die of dimension 1,27 x 1,27 mm this would have resulted in a loss of active area of 0,4 mm^2 - a large portion of the die indeed.

The clamp transistor used had a base area of less than 0,05 mm^2 , and when the lateral depletion regions of 96 μm were included, the total area used for the clamp structure was about 0,14 mm^2 . A net saving of over 0,25 mm^2 of usable silicon was thus realized.

3.6.2 A further measure to provide a greater usable silicon area

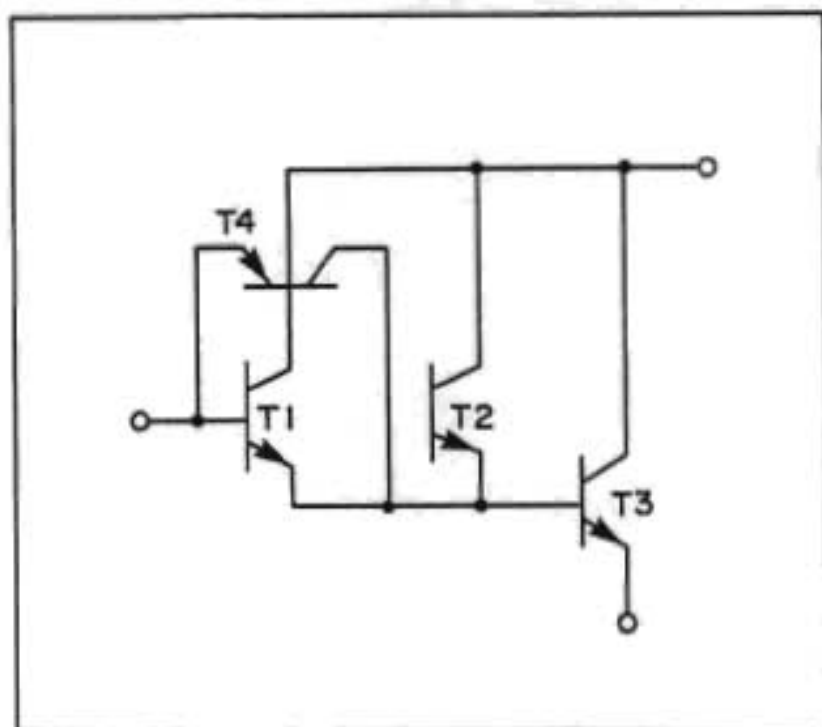
The use of a modified scribe margin layout yielded more usable silicon active area. In the $\mu/014$ transistor layout, the scribe margin consisted of a 52 μm N^+ diffusion surrounding the device that consumed about 0,25 mm^2 of potentially usable silicon area. This layout was on the traditional lines used for integrated circuits, with all the data normally required for resolution targets and alignment and issue marks incorporated into the surrounding scribe margin. In the prototype Darlington transistors all these features were included in one 68 μm strip along the base of the device. On the other three sides of the device, the scribe margin was reduced to 16 μm . A total of 0,16 mm^2 of usable silicon area was saved in this way.

3.6.3 Isolation of the Darlington stages

In an integrated Darlington transistor the base regions of the driver and the output transistor form a parasitic lateral PNP device with the N epitaxial layer forming the base. This parasitic device is shown in Figure 3.9 (page 78). Elaborate precautions are commonly taken to minimize the effect of this parasitic element, which could become active when the Darlington approaches saturation or is reverse-biased, and such measures include :

- (a) the separation of the driver and output base regions by a long meander path as often seen in Mesa technology; and

Figure 3.9
The integrated Darlington transistor



THIS REALIZATION OF THE INTEGRATED DARLINGTON TRANSISTOR, SHOWING REAL AND PARASITIC TRANSISTORS

- T1 - THE DRIVER TRANSISTOR
- T2 - THE CLAMP TRANSISTOR (TO EQUALIZE BV_{CE0} , BV_{CB0} AND BV_{CB5}).
- T3 - THE OUTPUT TRANSISTOR
- T4 - A PARASITIC PNP DEVICE (BETWEEN THE BASE DIFFUSIONS OF T1 AND T3) THAT IS INHERENT IN A MONOLITHIC DARLINGTON STRUCTURE.

- (b) the inclusion of a separate P diffusion to form a collector diode connected to the emitter of the output transistor to prevent reverse-bias operation, where T^4 is active.

Fields³⁶ has shown how the parasitic PNP may be used to advantage in improving the saturation performance of integrated Darlington transistors. Referring to Figure 3.9 (page 78), the base of the driver transistor forms the emitter of the parasitic PNP, the Darlington collector forms the base region of the PNP, and the base of the output transistor forms the collector region of the PNP. As the Darlington transistor approaches saturation, the emitter-base junction of the parasitic PNP becomes forward-biased, and if the gain of this parasitic PNP is increased, more current is forced into the base of the output stage (collector of the parasitic PNP). This enables the minimum saturation voltage of the Darlington transistor to be reduced from the traditional limit, which is in the region of 0,8 V, to less than 0,3 V.

This effect was not observed on any of the transistors fabricated during the development programme and, indeed, such effects would not have been welcomed by the customer as they would have represented a deviation from the design objectives.

3.6.3.1 Usable area : Inclusion of a collector diode?

Despite the ease with which a diode, as in 3.6.3 item b, above, could have been included in the structure, it was essential to minimize the device area if cost objectives were to be met. As the integrated Darlington transistor was fed from the exchange via a bridge rectifier, it was not expected that in practice any significant reverse bias conditions, enhancing the operation of the parasitic PNP would be encountered. No diode was included in either the prototype or production Darlington.

3.6.3.2 Isolation techniques adopted

Two simple techniques of isolation were included in the designs for the prototype Darlington transistors. The first was 'Resistive Isolation' (RI). This technique is used in integrated circuit layouts, and simply

relies on a sufficiently large clearance between the two P base diffusions to reduce the gain of the parasitic PNP to an insignificant level.

The second isolation technique was the use of the N+ emitter diffusion in the N- collector region to effectively nullify the lateral PNP effect between the base regions of the driver and output stages. This was analogous to the so-called 'channel stop' diffusions commonly used in MOS technology. The disadvantage of this N+ Isolation (NI) technique in high-voltage devices was that an adequate lateral depletion clearance for the P base diffusions was required on both sides of the N+ diffused region, which would consume usable active area.

3.6.3.3 Dielectric strength of oxide over N+ isolation

The oxide above the emitter area was the thinnest of all the oxides grown, having a thickness of only 0,5 μm in the process used. It was anticipated that voltages of only some 300 V could be tolerated across this layer before destructive breakdown would occur (Smithies⁷). In the case of a 500 V device this would automatically imply either a long meander pattern for the connection between driver and output device, or a short break in the N+ diffusion over which the interconnect layer passed. The latter approach was adopted.

The RI and NI versions of the prototype *118 Darlington transistors are shown in Figures 3.10a and 3.10b respectively (page 81). For the RI device, a depletion clearance of 100 μm was used between all the P base diffusions and the N+ equipotential ring around the transistors. A clearance of 96 μm was used between the metallization and the N+ scribe channel.

In the case of the NI device, the break in the N+ diffusion, over which the aluminium interconnect passed, was located in such a way as to provide the largest distance between the driver, clamp and output transistor base diffusions. The clearance between the P base diffusions and the N+ equipotential ring was only 84 μm , and the metal to scribe channel minimum clearance was 80 μm . These smaller clearances were adopted in order to preserve the area of the driver and output transistors so that the gain requirements of the NI device would be met.

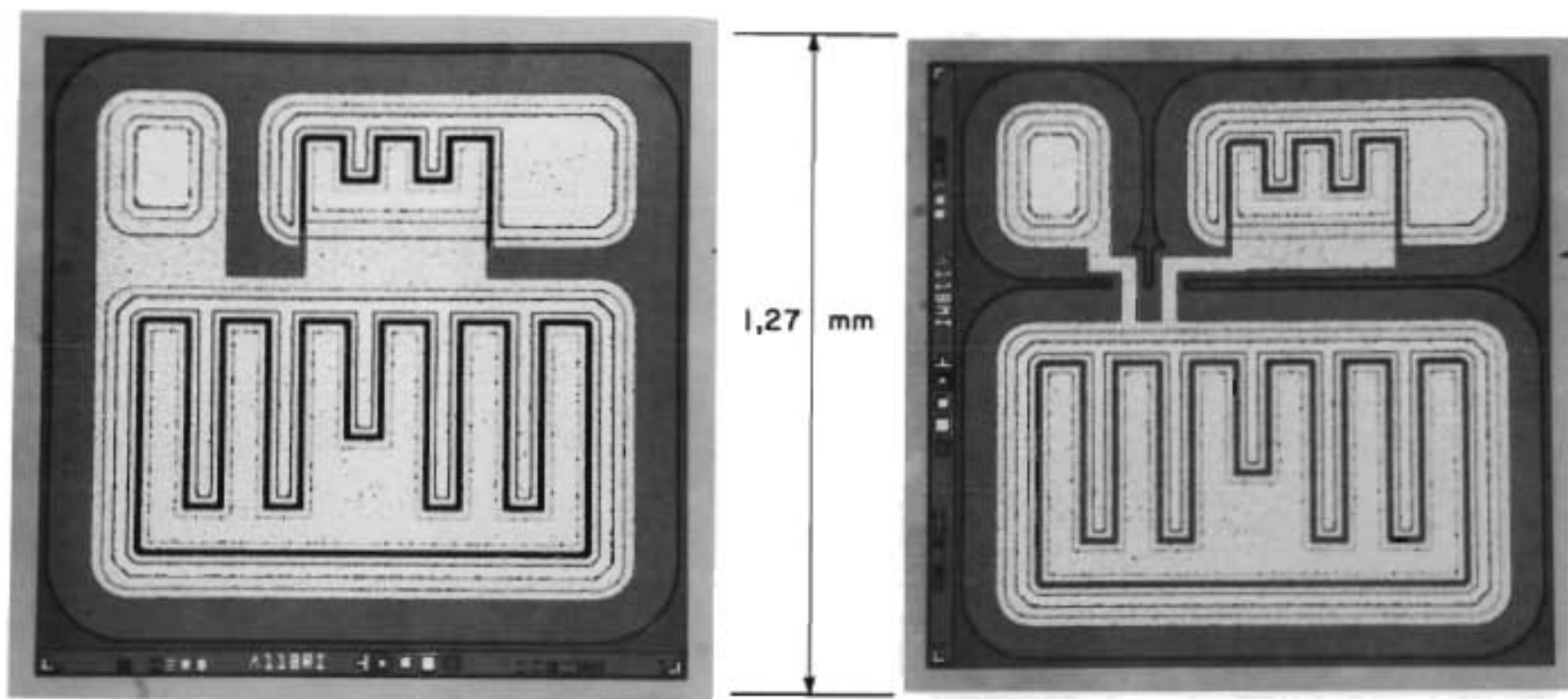


FIGURE 3.10 a THE PROTOTYPE INTEGRATED DARLINGTON TRANSISTOR TYPE * /118R1, INCORPORATING RESISTIVE ISOLATION (RI) BETWEEN THE P BASE DIFFUSIONS. THE CLAMP TRANSISTOR IS IN THE TOP LEFT-HAND CORNER.

FIGURE 3.10 b THE PROTOTYPE INTEGRATED DARLINGTON, TYPE * /118NI, INCORPORATING N+ EMITTER DIFFUSION ISOLATION (NI). THE CLAMP TRANSISTOR IS IN THE TOP LEFT-HAND CORNER. A SMALL BREAK IS MADE IN THE N+ DIFFUSION TO ALLOW THE ALUMINIUM INTERCONNECTIONS TO PASS OVER THE THICKER FIELD OXIDE. NOTE: THE EXTRA AREA CONSUMED BY THE N+ DIFFUSION.

3.6.4 Apportioning the driver and output transistor areas

As there were no precedents to follow in the design of the prototype transistors, and as there were certainly no suitable modelling programmes with direct application to the problem in hand, the approach taken was to consider first the actual telephone requirements, and to continue from there on as described below.

3.6.4.1 Load impedance of the buffer stages

The Darlington transistor was not only required to make good certain gain conditions at specified voltages but also to form a low-impedance path for both the speech amplifier in the O.N.[#] position and the dial in the impulsing position and the exchange. This factor had been totally ignored in the telephone manufacturer's requirements given in Appendix 3.1 (page 235). Measurements by the author on the 2N3439 type device then in use had shown that, certainly for short-line conditions, these transistors were not truly saturated. When dV/dI measurements were made on the collector terminal of a 2N3439 in the O.N. position at $I_C = 100 \text{ mA}$ and $V_{CE} = 1,8 \text{ V}$, impedance values as high as 200 ohms were not uncommon. Figure 3.11 (page 83) shows a typical I_C vs V_{CE} characteristic of a 2N3439. Quite clearly the output device could operate below the knee voltage (certainly not above) in quasi-saturation rather than true saturation. The performance of the driver was thus most important, as the output device should be driven as hard as possible towards saturation to minimize the impedance of this stage.

3.6.4.2 Design information from discrete Darlington pairs

Three transistors with 1,27 mm x 1,27 mm die were investigated, and normalized h_{FE} vs I_C plots are given in Figures 3.12a, b and c (page 85).

[#]The O.N. or 'On Normal' transistor is used to turn on the speech amplifier in a telephone and is analagous to the 'Off Normal' dial switch in a rotary dial telephone which shorts across the speech circuit during dialling.

A Dawson, pers. comm. (1980) Post Office Teletronic Institute, (Potelin) Private Bag X74, Pretoria 0001, Republic of South Africa.

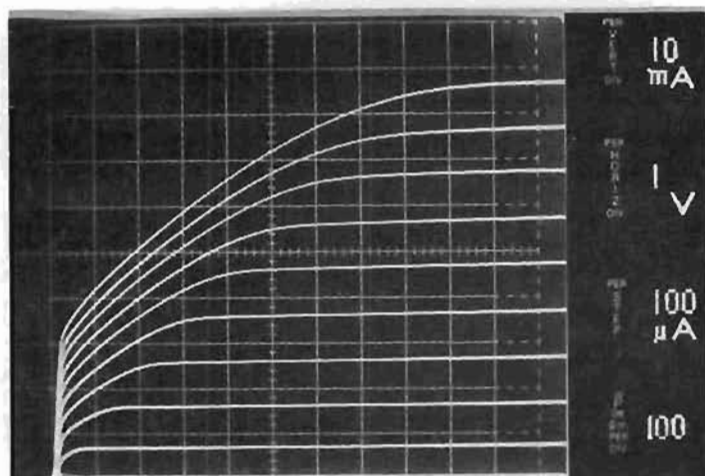


Figure 3.11

Saturation characteristics of a 2N3439 transistor. ($V_{CE0(sus)} \geq 350$ V). It is clear that the operating conditions fall into three distinct regions, which are

Region 1 : true saturation below $V_{CE} = 0,3$ V

Region 2 : quasi-saturation, below the knee voltage, V_{CEK}

Region 3 : normal operation above V_{CEK}

(See Figure 2.2 page 13 for a definition of V_{CEK})

(Device code : CCSA 2N3439L. Date of manufacture: 80/27).

The three transistors consisted of two 2N3439 type devices, one manufactured by RCA and the other by Texas Instruments, the third being a PT014. The 2N3439 types had BV_{CEO} values of about 400 V, some 100 V higher than the PT014. In the integrated Darlington transistor it was to be anticipated that the resistivity and thickness of the epitaxial layer would increase, and the active area of the output device apparently inevitably decrease; therefore it would have been unrealistic to base the design on the small gain drop at high collector currents measured on the PT014 and consequently for the calculations below use was made of the curve for the RCA 2N3439, in Figure 3.12a (page 85), in which this effect was very pronounced.

(a) The impulsing gain condition

Here $h_{FED} > 1800$ at $V_{CE} = 3$ V and $I_C = 125$ mA
 where h_{FED} is the gain of the Darlington pair.

The collector current is given by $I_C = h_{FED} \times I_B$, and

$$h_{FED} = (1 + h_{FE1}) \times h_{FE2} + h_{FE1} \quad \dots\dots\dots 3.3A$$

where h_{FE1} is the driver gain and h_{FE2} is the output device gain.

For the 2N3439 at 3 V and 125 mA (Figure 3.12a, page 85)

$$h_{FE2} = 0,25h_{FEM}$$

where h_{FEM} is the peak gain measured in the normal operating region above the knee voltage.

Assuming $h_{FE1} = 0,9h_{FEM}$ (Figure 3.12a, page 85) and

$h_{FED} = 1800$, it may be shown using equation 3.3A that

$$h_{FEM} = 87.$$

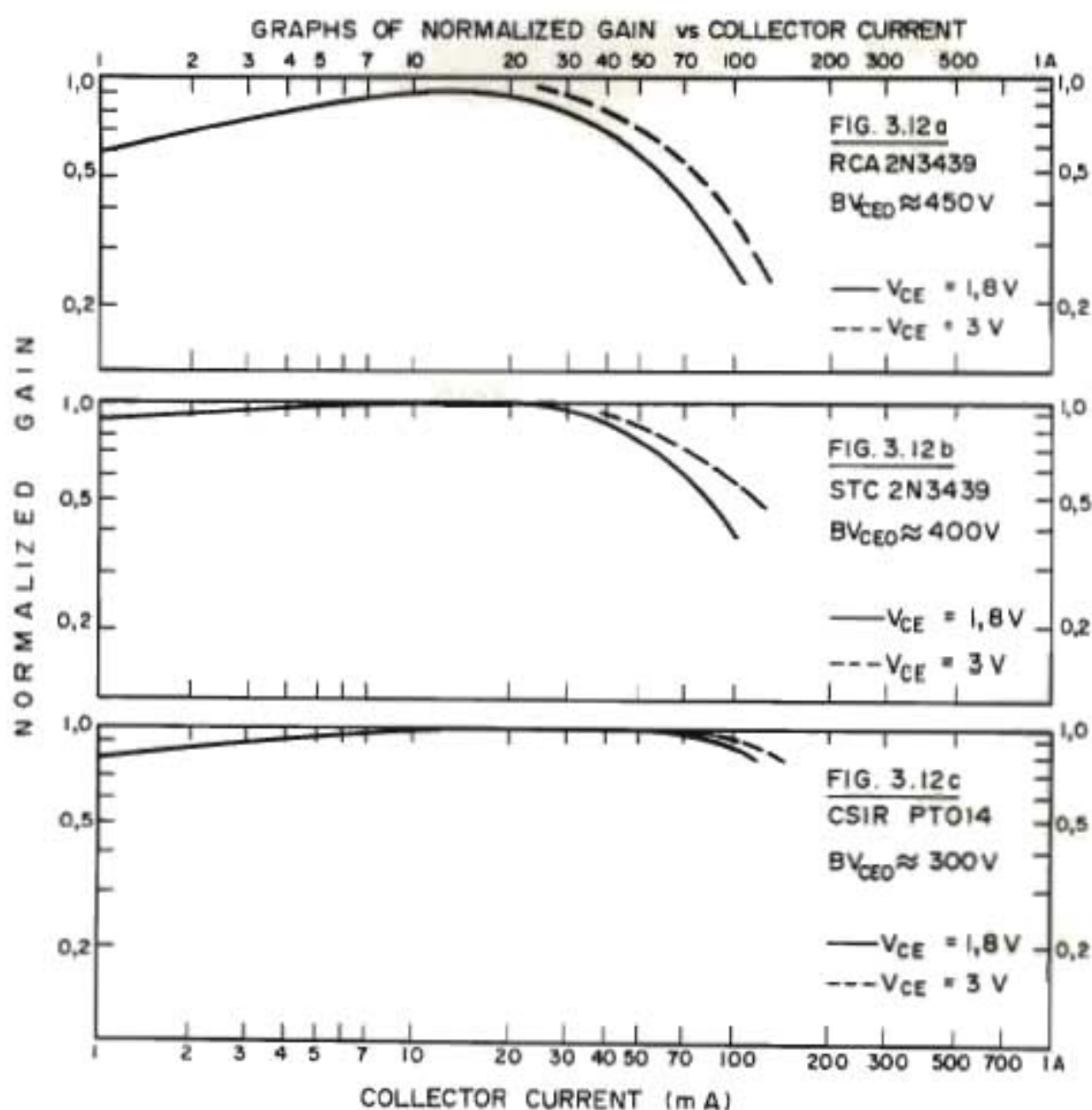
(b) Maximum permissible collector resistance of the driver R_{C1}

With the figures above and a Darlington collector current of

Figure 3.12

Normalized gains of three high-voltage transistors as a function of collector current.

(All three devices had die sizes of approximately 1,27 mm x 1,27 mm)



125 mA, equation 3.3A gives the collector current of the driver :

$$I_{C1} = 5,5 \text{ mA.}$$

From data on the 2N3439 at a base current of 5,5 mA, V_{BE} was about 0,8 V, hence $V_{CE1} = 2,2 \text{ V}$ and

$$R_{C1} = 2,2/0,0055 = 400 \text{ ohms maximum.}$$

3.6.4.3 Thickness and resistivity of epitaxial layer

Figure 2.13 (page 42) gives curves for the thickness and resistivity of the epitaxial layer vs BV_{CEO} for $h_{FEM} = 100$. Use of the assumed value of BV_{CEO} of 350 V and a gain of 100, rather than 87, with a $W_D/4$ punch-through collector yields :

$$\begin{aligned} r_{epi} &= 50 \text{ ohm.cm; and} \\ t_{epi} &= 40 \mu\text{m below the base region.} \end{aligned}$$

These figures, corrected for the thickness of silicon used in the processing, were used for the prototype Darlington experiments. Taking into account that at that stage the silicon manufacturer could guarantee a spread of only +/- 20 per cent on both resistivity and thickness of epitaxial layer, the following limits were agreed to :

$$\begin{aligned} r_{epi} &= 50 - 70 \text{ ohm.cm; and} \\ t_{epi} &= 45 - 65 \mu\text{m.} \end{aligned}$$

An evaluation lot of 20 wafers was obtained.

3.6.4.4 Active collector area of the driver

The active collector area of the driver, A_{dr} , was given by the relationship $r_{epi} \times t_{epi} / R_{C1}$

$$A_{dr} = 50 \times 0,004/400 \times 100 = 0,05 \text{ mm}^2 \text{ (minimum).}$$

The emitter areas used in the prototype designs for the driver for

both the NI and RI types were approximately $0,044 \text{ mm}^2$, and these, corrected for the epitaxial layer thickness (equation 2.6B on page 37), gave effective collector areas of $0,052 \text{ mm}^2$ for both devices.

3.6.4.5 The O.N. condition

Although in the foregoing discussion the O.N. condition ($h_{FE} > 800$ for $V_{CE} = 1,8 \text{ V}$ and $I_C = 100 \text{ mA}$) was neglected, it was possible to estimate the value of the O.N. Darlington gain by using Equation 3.3A with $V_{CE1} = 1 \text{ V}$, $h_{FEM} = 87$ and assuming h_{FE1} had dropped by 50 per cent, owing to the driver moving into quasi-saturation.

The estimated value of gain was

$$h_{FED} = 912$$

which was well above the specified limit of 800.

It was found in practice that this estimate was very pessimistic, and that with #/118RI prototypes delivered for evaluation, the largest drop in gain in moving from the impulsing to the O.N. condition was 27 per cent, whilst the average drop was 12 per cent for the batch. Thus a device just meeting the impulsing gain lower limit of 1800 would have had a gain greater than 1300 for the O.N. condition.

3.6.4.6 Remaining area for the output device

The addition of a base bonding pad about $0,25 \text{ mm}$ square and a $96 \mu\text{m}$ clearance for depletion and isolation meant that the total area including the active areas used by the driver and clamp transistor was $0,51 \text{ mm}^2$. This left approximately $0,78 \text{ mm}^2$ for the output transistor.

In the RI layout the corrected collector area of the output transistor was $0,36 \text{ mm}^2$, giving a collector region resistance of :

$$R_C = r_{epi} \times t_{epi} / 0,36 = 56 \text{ ohms.}$$

For the NI version these figures were $0,33 \text{ mm}^2$ and 61 ohms respectively.

3.6.4.7 Collector impedance

In accordance with the above figures for the collector resistance of the output stages of these Darlingtons, they would be operating in the quasi-saturation region below the knee voltages, which would be above 5 V for the short-line impulsing condition. A number of dV/dI measurements for both the short-line impulsing and O.N. conditions gave impedances of between 100 and 150 ohms.

Measurement of the collector impedances under both medium and long-line conditions showed that the integrated Darlingtons approached full saturation, and that the collector impedance tended to drop even lower.

3.6.4.8 Use of an interdigitated emitter structure

When laying out the prototype */118 Darlington transistors interdigitated emitter structures were used for the following reasons.

- (a) The emitter injection levels anticipated were higher than those on the PT014. At a maximum collector current of about 66 mA at 6 V the current density in the PT014 was $0,15 \text{ A/mm}^2$, and departures from ideal transistor operation were minimal. In the case of the RI Darlington the impulsing current density at 125 mA was $0,35 \text{ A/mm}^2$ and in the line-earthed fault condition this could rise to $0,7 \text{ A/mm}^2$. A comparison of the PT014 with a simple emitter and a Texas Instruments TR2 device with an interdigitated emitter structure indicated that at these higher-current densities the dV/dI characteristic in the latter should be steeper, resulting in a lower collector impedance. In addition, transition to normal active transistor operation above the knee voltage, where the collector impedance characteristic is high, should be more rapid and better defined.
- b) With an interdigitated emitter structure, the forward base-emitter voltage, V_{BE} , of the output stage of the Darlington transistor could be reduced. V_{BE} vs I_B measurements made on the PT014 indicated a larger resistive component in the V_{BE} characteristic than that on interdigitated devices that were tested. These results were confirmed by measurements made on both Texas Instruments TR2

devices and 2N3439 devices operated at the short-line impulsing condition of $I_C = 125 \text{ mA}$ and $V_{CE} = 3 \text{ V}$.

As V_{BE2} for the output device affects V_{CE1} of the driver, it was important that V_{BE2} should be minimized to improve driver performance and hence the saturation characteristics of the device as a whole. An interdigitated structure was thus indicated for this reason as well.

No publication was noted wherein the importance of reducing V_{BE} in the output stage was mentioned as a factor in either discrete or integrated Darlington design.

3.7 FABRICATION AND EVALUATION OF THE PROTOTYPE INTEGRATED DARLINGTON TRANSISTORS, AND FINDINGS RELEVANT TO THE PRODUCTION VERSION

3.7.1 Fabrication of the prototypes

The specification given in Table 3A (page 62) was used as a basis for the manual probe evaluation of two batches of five laboratory-produced wafers. Two wafers were sent for assembly, one as a control medium to ensure that assembly procedures were correct. A total of 473 devices, 230 RI types and 243 NI types, were returned to the CSIR and were fully evaluated at room temperature.

3.7.2 Analysis of test results on prototypes

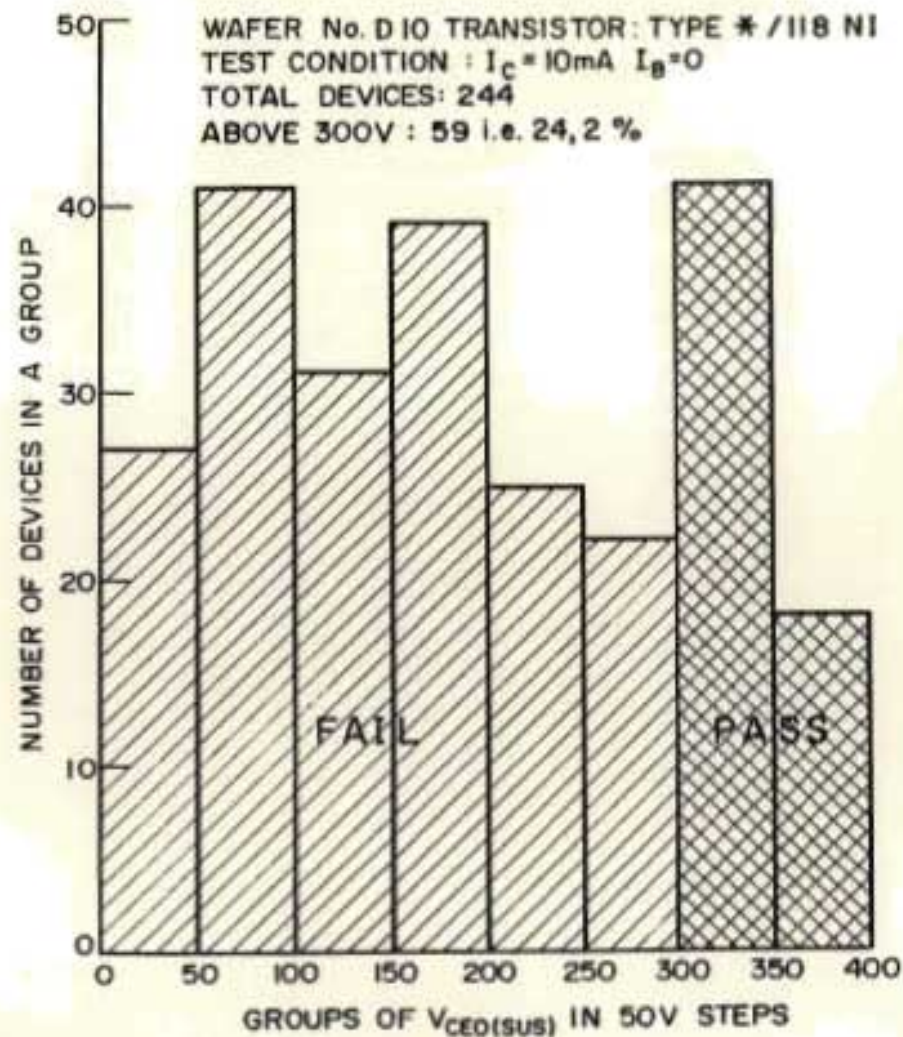
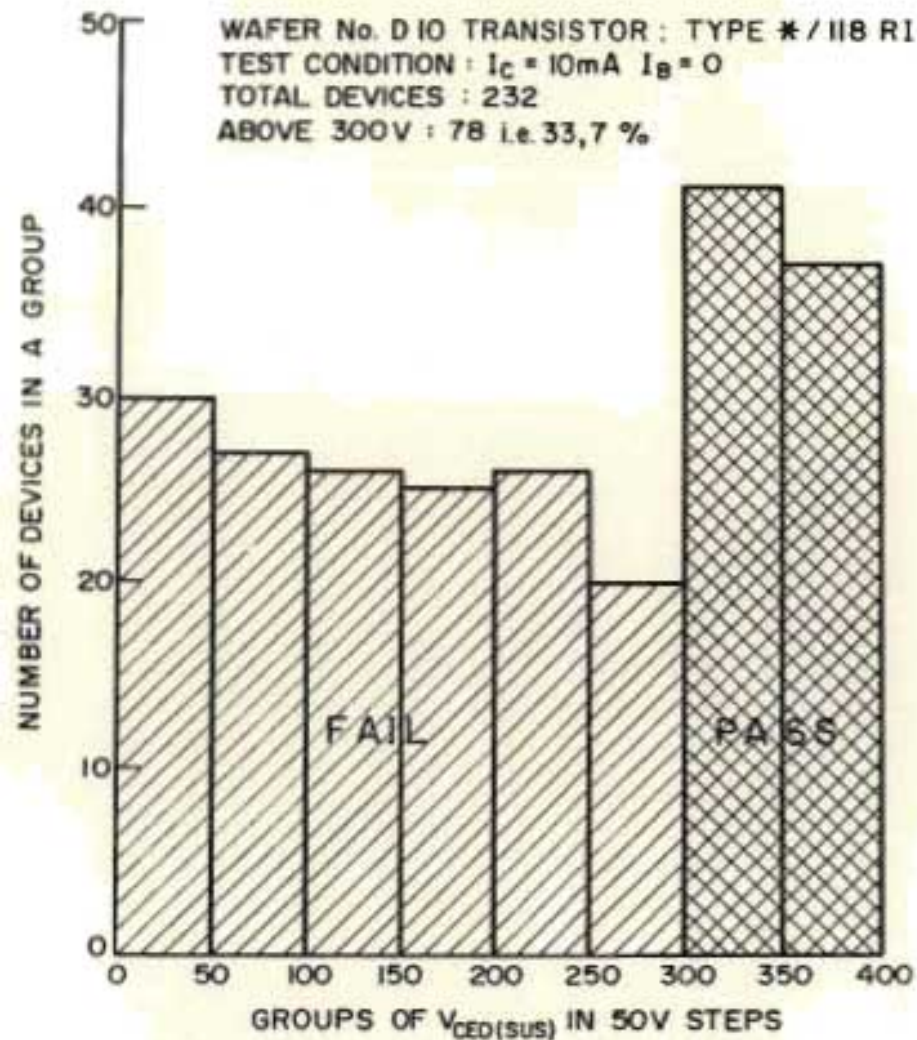
(a) The sustaining voltage - $V_{CEO(SUS)}$

The results of the tests are given in Figures 3.13a and 3.13b (page 90).

RI types - 33,7 per cent passed the test of $V_{CEO(SUS)} > 300 \text{ V}$

NI types - 24,2 per cent passed the same test.

The lower yield on the NI type had been expected, as only $84 \mu\text{m}$ was allowed for lateral depletion in the collector region and $80 \mu\text{m}$ between metal and the scribe channel, compared with $100 \mu\text{m}$ and $96 \mu\text{m}$ for the RI type. The larger clearances were thus important and



NOTE : POOR YIELDS ABOVE 300 V

Figures 3.13a & 3.13b

Population distributions of $V_{CE0(sus)}$ for prototype integrated Darlington transistor

were further increased for the production geometry.

At the time it was not clear why the distribution of $V_{CEO(SUS)}$ was not Gaussian in nature below 300 V. Subsequent investigations on the production geometry of the PT018 indicated that contamination, probably occurring during the assembly phase, was the most likely cause of this.

(b) Collector-base breakdown voltages - BV_{CBO} and BV_{CBS}

In all cases the measured values were within about 10 V of the recorded values for $V_{CEO(SUS)}$.

(c) Emitter-base breakdown - BV_{EBO}

Figure 3.14 (page 92) shows the excellent characteristics of this parameter, both the RI and NI types displaying a sharp peak between 18 and 20 V.

(d) The O.N. gain - $h_{FE(1)}$

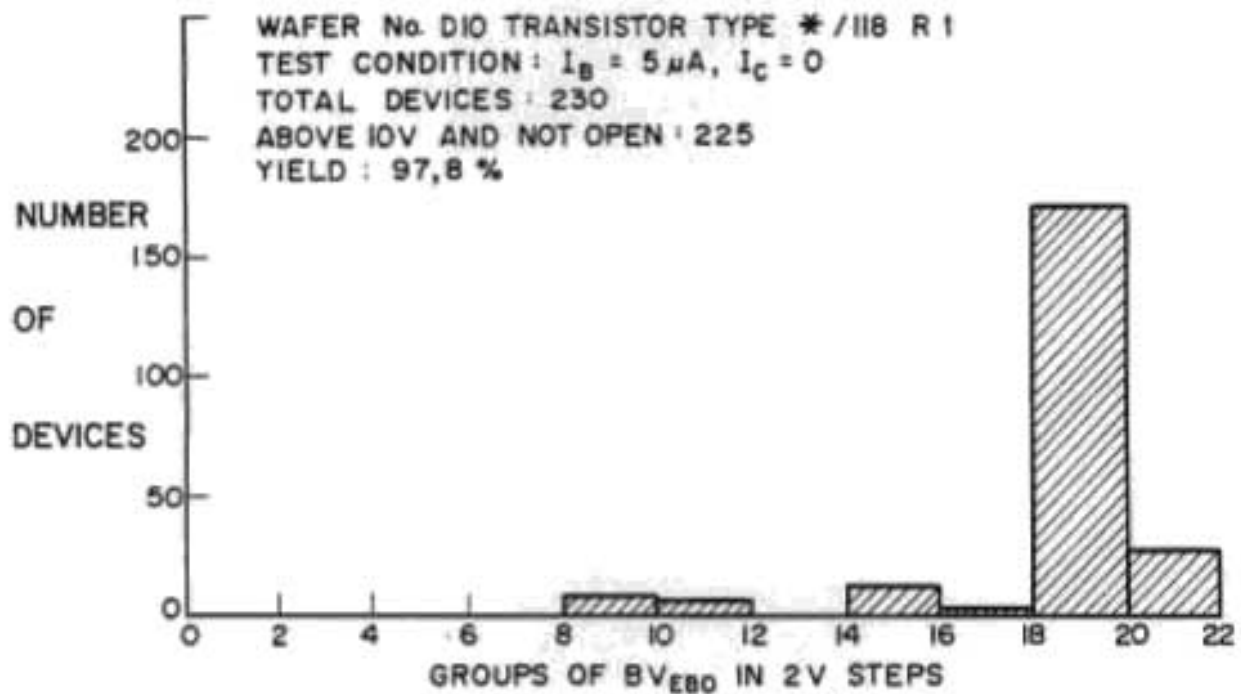
The gain histograms shown in Figure 3.15a and 3.15b (page 93) indicate a good Gaussian-type distribution with yields of 92 per cent for both the RI and NI types.

(e) The Impulsing gain - $h_{FE(2)}$

Again it may be seen from Figure 3.16a and 3.16b (page 93) that a good Gaussian-type distribution was obtained with yields again above 92 per cent.

(f) Leakage currents

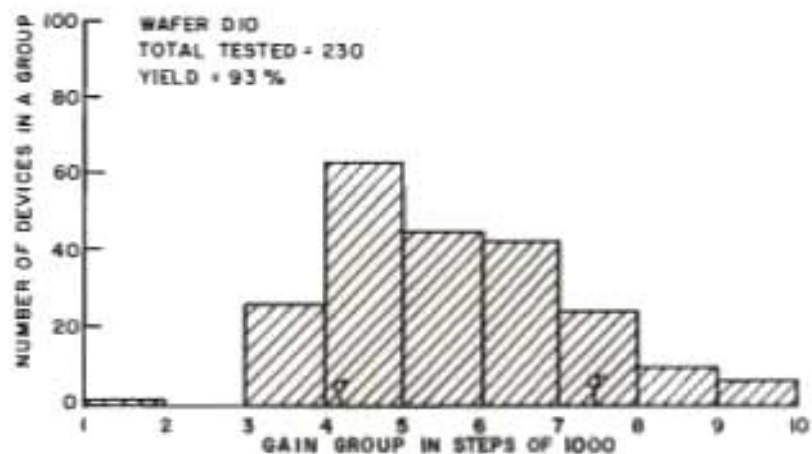
A 10 per cent sample of the NI and RI types was checked against the specification in Table 3A (page 62). Consistently high values of I_{CEO} and, to a smaller extent, I_{CBS} were measured, and this indicated a potential yield problem. A relaxation and stabilization of I_{CEO} was also noted when V_{CE} was adjusted, but this did not appear as a marked effect when I_{CBS} was measured, thus indicating that the



* / I18 POPULATION DISTRIBUTION OF BV_{EBO}

Figure 3.14

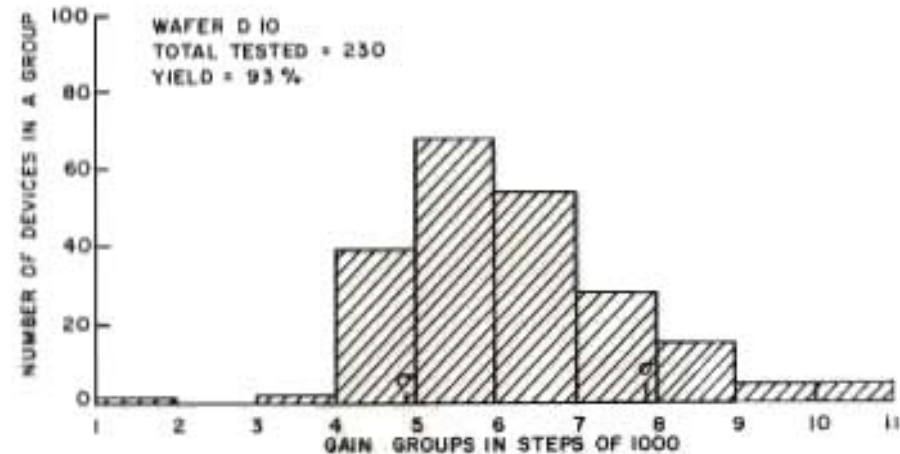
BV_{EBO} distribution for prototype integrated Darlington transistor. Both the RI and NI types showed excellent yields (in the region of 98%) on this parameter.



* / 118 POPULATION DISTRIBUTION OF $h_{FE(1)}$

Figure 3.15a

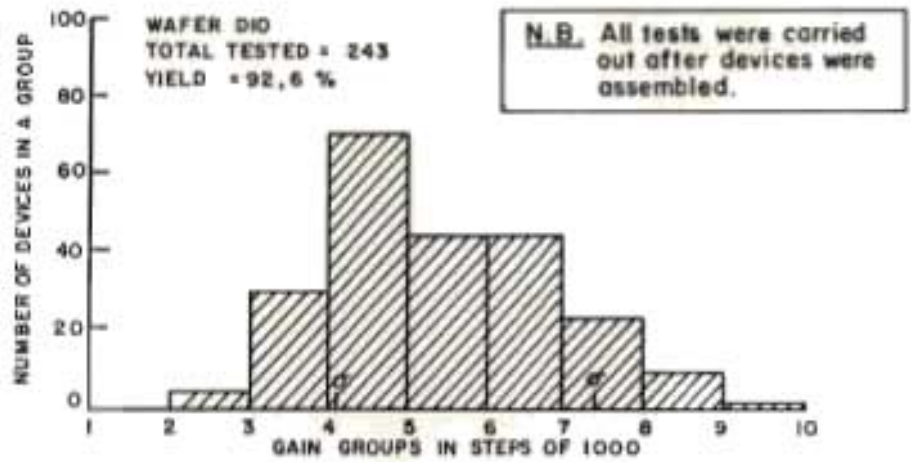
The gain distribution of the RI prototypes - O.N. condition
 O.N. TEST: $I_C = 100 \text{ mA}$, $V_{CE} = 1.8 \text{ V}$
 To pass: $h_{FE} > 800$



* / 118 POPULATION DISTRIBUTION OF $h_{FE(2)}$

Figure 3.16a

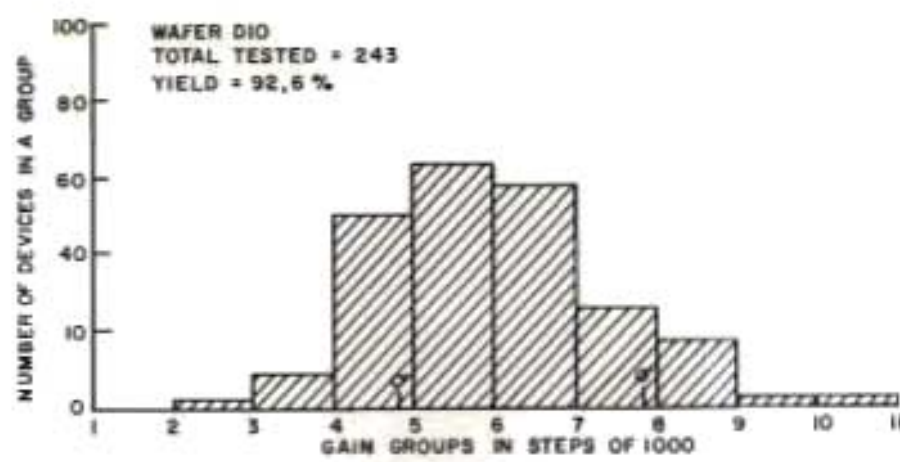
The gain distribution of the RI prototypes - Impulsing condition
 IMPULSING TEST: $I_C = 125 \text{ mA}$, $V_{CE} = 3 \text{ V}$
 To pass: $h_{FE} > 1800$



* / 118 POPULATION DISTRIBUTION OF $h_{FE(1)}$

Figure 3.15b

The gain distribution of the NI prototypes - O.N. condition



* / 118 POPULATION DISTRIBUTION OF $h_{FE(2)}$

Figure 3.16b

The gain distribution of the NI prototypes - Impulsing condition

major contributor to this effect was the driver transistor rather than the clamp transistor, which had no external base connection.

Values of I_{CBO} and I_{EBO} were generally well below the specified limits, and were stable.

The problem with high leakage currents had not been encountered at the wafer probe stage. Several of the assembled devices showing high leakages were de-topped, and visual inspection showed severe particulate contamination. As reported later in the chapter, this problem was only thoroughly investigated during early production of the PT018.

3.7.3 Evaluation of the prototypes in the IPB dial telephone

Twenty devices, covering a wide range of gains and a range of breakdown voltages above 300 V, were selected and fully characterized according to the specification. Ten were RI type devices and the other ten NI types.

These prototypes having been fitted to the IPB dial telephone, their performance under all line conditions was evaluated by the telephone manufacturer³⁷, and found to be adequate in the case of both types, whilst there appeared to be no marked difference between the NI and RI types.

A 4 kV surge test caused three of the NI type devices to fail, but the breakdown characteristics of the RI type were degraded only slightly, the leakage currents having been increased.

It was thus evidently advisable to employ the resistive isolation technique in the production device.

3.8 THE FINAL DESIGN OF THE PT018 FOR PRODUCTION

3.8.1 Upgrading the breakdown voltages

As the upper limit on BV_{CEO} did not extend beyond 400 V on the prototype Darlington, and as the peak of the spread in the acceptable BV_{CEO} distribution was between 300 and 350 V for both types, it was clear that a

more systematic approach was required to provide a revised limit in order to ensure an adequate production yield.

From the point of view of test limits, the required value of BV_{CEO} would be increased above 300 V. It was known that after insets had been applied by the transistor assembler, quality assurance during assembly and probe testing (each 2 per cent) the BV_{CEO} should exceed 318 V. From experience gained on the PT014 project, the gain in the high-voltage process would range between about 100 and 300. Applying equation 2.5A (page 20) with $n = 5$, a breakdown of 318 V and a gain of 300, the collector-emitter breakdown associated with a device of gain 100 was :

$$BV_{CEO} = 318 \times (3)^{1/5} = 396 \text{ V.}$$

The use of Figure 2.13 (page 42) with this new breakdown limit gave

$$r_{epi} = 55 \text{ ohm.cm}$$

$$W_D/4 = 45 \text{ } \mu\text{m}$$

and, after adding a conservative 10 μm for silicon used in processing,

$$t_{epi} = 55 \text{ } \mu\text{m.}$$

These, then, were taken as the lower limits of the epitaxial layer specification. After negotiation with the silicon manufacturer, who was then able to offer a +/- 10 per cent spread on layer thickness and a +/- 20 per cent spread on resistivity, the following limits were agreed to :

$$r_{epi} = 55 - 75 \text{ ohm.cm}$$

$$t_{epi} = 58 - 70 \text{ } \mu\text{m}$$

The silicon specification is reproduced in Appendix 3.4 (page 239).

3.8.2 Increase in Darlington area - a limit imposed by economics

Quite clearly this new epitaxial layer specification necessitated an area increase for the production Darlington in order that the gain requirements should be met. The prototypes were diffused on silicon as specified

in Section 3.6.4.3, and a highly satisfactory 92 per cent yield on the gain tests was obtained, despite the fact that collector resistance values would meet the design values only at the lower resistivity and thickness end of the epitaxial layer specification.

In the production geometry, it was decided that the R_C values should rather be met in the middle of the new epitaxial layer specification. The increase in area required was given by the ratio between the new epitaxial layer parameters and the old :

$$\begin{aligned} A_{\text{NEW}}/A_{\text{OLD}} &= (55 + 75)/(2 \times 50) \times [(58 + 70)/2 - 8]/(45 - 8) \\ &= 1.97. \end{aligned}$$

(The figure of 8 μm , which was the approximate base junction depth, was subtracted from the full epitaxial layer thickness to give the actual thickness of the collector region.)

An enormous increase of 97 per cent in active area was thus required to ensure that both breakdown and gain requirements would be met, but as production costs were the overriding consideration in this programme this increase could not be accommodated since the area of the device would have become too great for economically viable manufacture.

A two-inch wafer process was in use, and in terms of an internal costing report³⁸, the processing cost for the high-voltage transistor wafers, irrespective of the transistor geometry, was constant, and was in the region of R150. For the PT014, as noted in the data management section of Chapter 5, total wafer losses during processing and rejections in testing were in the region of 35 per cent. From data recorded during the prototype runs, it was reliably assumed that a similar figure for wafer rejects would apply to the integrated Darlington transistor and this would bring the actual cost of a wafer to about R230.

If a 50 per cent yield could be maintained, then, for a die price of 50 cents, which was the practical limit, no less than 920 transistor dies would have to be diffused on a single two inch wafer. From this figure a practical upper limit on the die size was 1.4 x 1.4 mm representing an increase in overall area of only 22 per cent when compared with the prototypes.

3.8.3 The increased active area of the production PT018 Darlington

The key task was to increase the active area of the device as much as possible within the 22 per cent increase in total area of the die so as to approach the required increase of 97 per cent.

Figure 3.17a (page 98) shows the layouts of the emitter and base diffusions adopted for the production geometry, together with the key clearances used. With the new 58 μm nominal epitaxial layer thickness under the base, the active areas, corrected using equation 2.6B (page 37), are given below, together with the increase in area relative to the RI prototype :

$$A_{\text{dr}} = 0,092 \text{ mm}^2 \quad (\text{increase of 77 per cent in area})$$

$$A_{\text{out}} = 0,58 \text{ mm}^2 \quad (\text{increase of 61 per cent in area}).$$

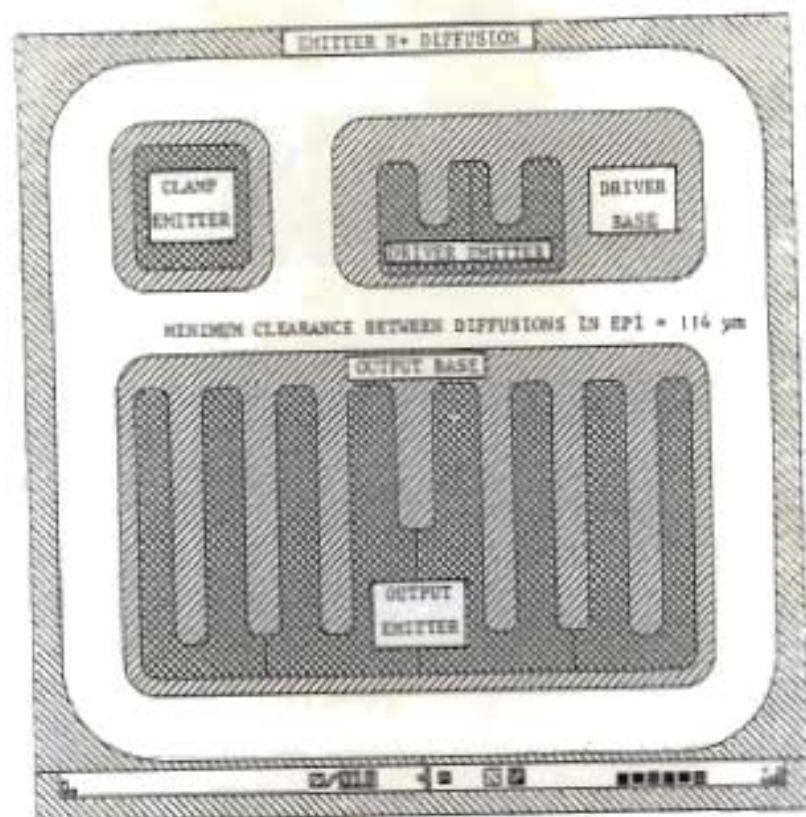
Larger increases would have been possible if overlap clearances between subsequent mask layers had been reduced. From the experience gained with the PT014 it was decided that generous clearances were desirable in order to limit to less than five per cent the wafer rejects due to bad registration, undercutting and other photolithography-related problems.

In practice it turned out that an outstanding compromise had been achieved on the PT018 with excellent simultaneous yields of between 50 and 70 per cent being obtained on both breakdown voltages and gains.

3.8.4 Clearances and oxide dielectric strengths

The */118T structure shown in Figure 3.5a (page 70) was used as a vehicle to evaluate the metal to scribe channel clearance requirements and the adequacy of the existing process oxide dielectric strengths.

As it had been shown that the clamp transistor limited all breakdown voltages to values close to the BV_{CEO} of the output stage, which should not exceed 500 V in practice, and the metal pads floating on the oxide of the */118T test circuit showed that a 100 μm clearance was adequate for operation up to this voltage, a conservative figure of 110 μm was adopted in the final layout, together with a field plate overlap of 20 μm over the base diffusion.



*018 DARLINGTON TRANSISTOR

FIGURE 3.17a The layout of the emitter and base diffusions are shown in the cross-hatched areas. The clear area inside the device represents the plain (oxide-coated) epitaxial layer. The clearance for lateral depletion in the collector region and for isolation of the three P-type base regions is $114 \mu\text{m}$.

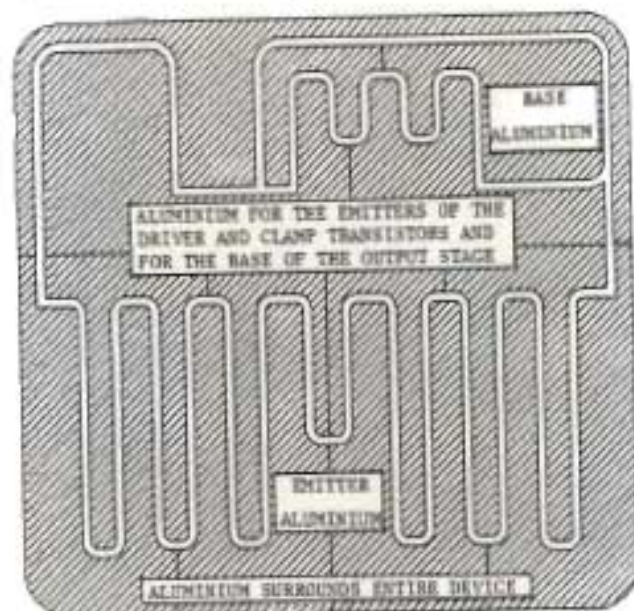


FIGURE 3.17b The aluminium layer of the Darlington transistor that covers and surrounds the diffusions shown in Figure 3.17a. (The contact windows are not shown.) The key feature of this 'inverted metallization' structure is that the metal surrounding the active elements of the transistor is electrically connected to the collector.

For lateral depletion in the N-collector region a conservative figure of $114 \mu\text{m}$ was used, as clearances below $100 \mu\text{m}$ on the */118T test structure did not give stable and 'hard' breakdown characteristics.

The resistive isolation (RI) technique was used in the PT018 layout as it had been the most successful in the prototype devices, and as all the metallization surrounding the device was on the $1,3 \mu\text{m}$ field oxide, no difficulties were experienced with inadequate oxide dielectric strengths.

3.8.5 Leakage currents and the 'inverted metallization' (IM) structure

As I_{CEO} was the problem parameter on the prototype devices, and as some relaxation effects had been noticed when V_{CE} was varied, particularly on devices with gains of over 10 000, it appeared that the sensitive base region would benefit from some form of electrical shielding. This was achieved by using the field plate metallization, partially surrounding the output transistor, to surround the whole device, including the sensitive base contact metallization of the input stage. Totally contrary to convention, this electrostatic guard ring was electrically connected to the emitter of the output stage rather than the base, and was hence always very close to ground potential. This layout was termed an 'inverted metallization' (IM) structure by the author and the layout is shown in Figure 3.17b (page 98). A photograph of the */018 Darlington die incorporating the IM structure is shown in Figure 3.18 (page 100).

The benefit noted in the production of PT018 Darlington transistors was that highly stable and extremely low-leakage currents, typically of the order of a few nA at 240 V, were recorded even with devices exhibiting peak gains approaching 10^5 .

3.8.6 Further benefits of the inverted metallization structure

Referring to Figure 3.6 (page 72), showing a field failure due to external discharge, it is clear that in the event of external breakdown conditions arising - certainly an unlikely event in the PT018 Darlington due to the inclusion of the clamp transistor - the surge energy would be diverted into the emitter circuit, preventing possible destructive damage to the sensitive input stage of the Darlington and even the drive circuitry.

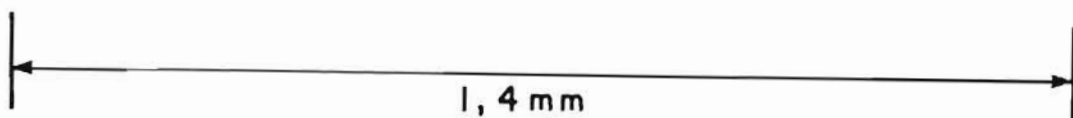
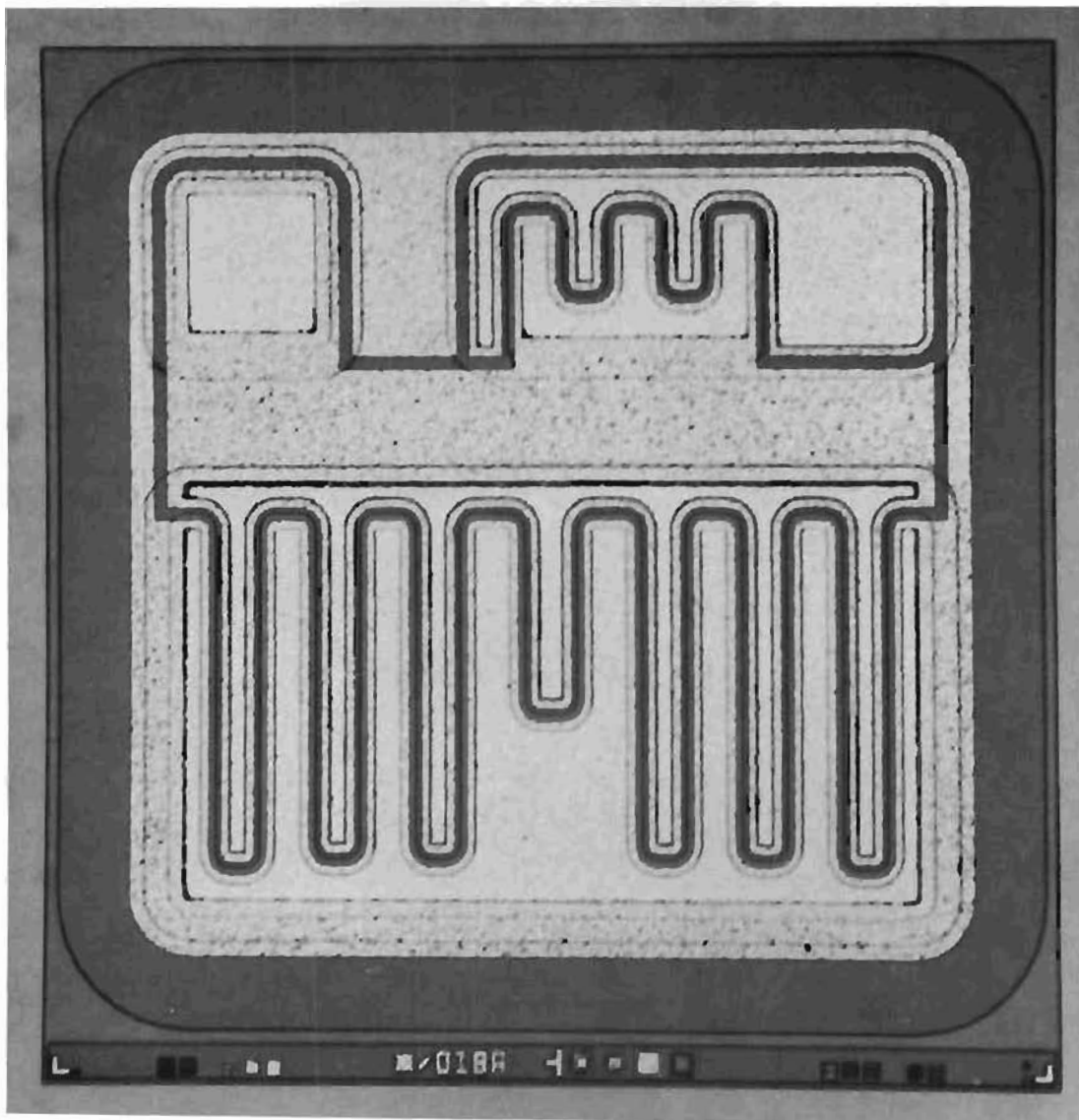


FIGURE 3.18 A 100x PHOTOGRAPH OF A PRODUCTION PTO18 INTEGRATED DARLINGTON TRANSISTOR. ALL THE LAYERS OF THE DEVICE MAY BE SEEN, AND IT IS CLEAR THAT THE METAL FIELD PLATE, CONNECTED TO THE EMITTER OF THE OUTPUT STAGE, ACTS AS AN ELECTROSTATIC SHIELD OR GUARD RING FOR THE WHOLE DEVICE .

Although numerous transistor dies from most of the major manufacturers were inspected during the development exercises for the PT014 and PT018, no layout technique similar to the IM structure was found on any device. The IM structure could also be applied with ease to discrete transistors when highly stable electrical characteristics are required. As with the PT018, the emitter electrode would act as a combined field plate and external electrostatic guard ring shielding the base region.

3.9 A CRITIQUE OF THE DESIGN OF THE PT018 TRANSISTOR

Data gathered during pre-production runs for the PT018 indicated that the basic transistor design was sound and that all the design objectives had been more than adequately met. Despite this, in order to note any shortcomings, the author critically considered the device and analyzed the comments of users of the die, also evaluating other information gathered during processing, besides data gathered from the various tests and trials that the device had been subjected to.

3.9.1 Outstanding performance of the PT018 Darlington transistor

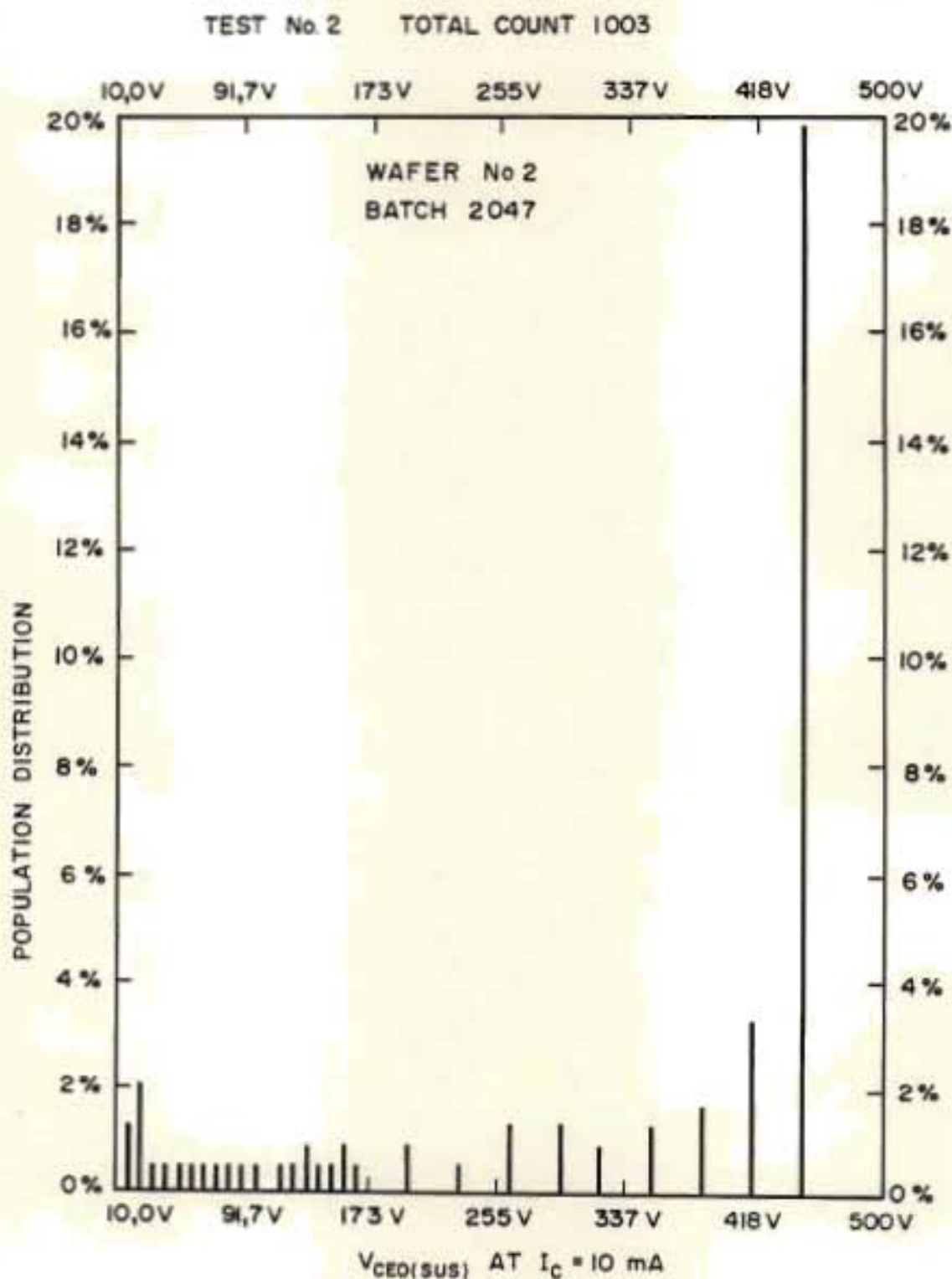
During the production run-up of the PT018, several batches of the transistors were processed and more than two thousand devices were assembled for the formal 'Qualification' exercise, where tests against the full specification described in Section 3.9.8 were carried out as part of the acceptance criteria for introduction of the device into service. A comparison of the parameters with those of the prototype devices follows.

(a) Improved $V_{CEO(SUS)}$ characteristics

The first comparison is with the $V_{CEO(SUS)}$ histograms given in Figures 3.13a and b (page 90) for the prototype devices. Figure 3.19 (page 102) gives the probed results from a typical production wafer. The most striking difference is that only 14 per cent of the PT018 devices had sustaining voltages of less than 318 V compared with more than 66 per cent of the RI, and over 75 per cent of the NI prototypes that had values of less than 300 V.

Figure 3.19

$V_{CE0(sus)}$ population on probing of wafer 2, Batch 2047



NOTE 1 CONSIDERABLE IMPROVEMENT WHEN COMPARED TO RESULTS IN FIGURES 3.13a AND 3.13b FOR PROTOTYPES

NOTE 2 DISTRIBUTION DISTORTED AT HIGH VOLTAGE END AS THE TESTER LIMITED AT 450 V.

The probed results showed that eighty per cent of the PT018 production geometry devices had sustaining voltages of greater than 380 V. (It should be noted in Figure 3.19 that values in excess of 450 V were not recorded, as this was the upper voltage limit used on the tester.)

(b) Extremely low-leakage currents

A sample of eighty assembled devices, issued by the transistor assembly plant on a non-selective basis after final electrical testing, was fully characterized on the NEERI automatic transistor tester, and all devices were found to comply with the specification given in Table 3A (page 62).

I_{CEO} was measured at $V_{CE} = 240$ V and $T = 25$ °C, and here the minimum recorded value of this parameter was 870 pA and the maximum value was 120 μ A, which was well below the specified limit of 500 μ A. Of these 80 devices, 70 had values of I_{CEO} smaller than 1 μ A. This result can be regarded as outstanding when it is considered that many of these devices exhibited peak gains considerably greater than 10^4 outside the quasi-saturation region.

All other leakage currents measured were well below the specified limits, many below 1 nA.

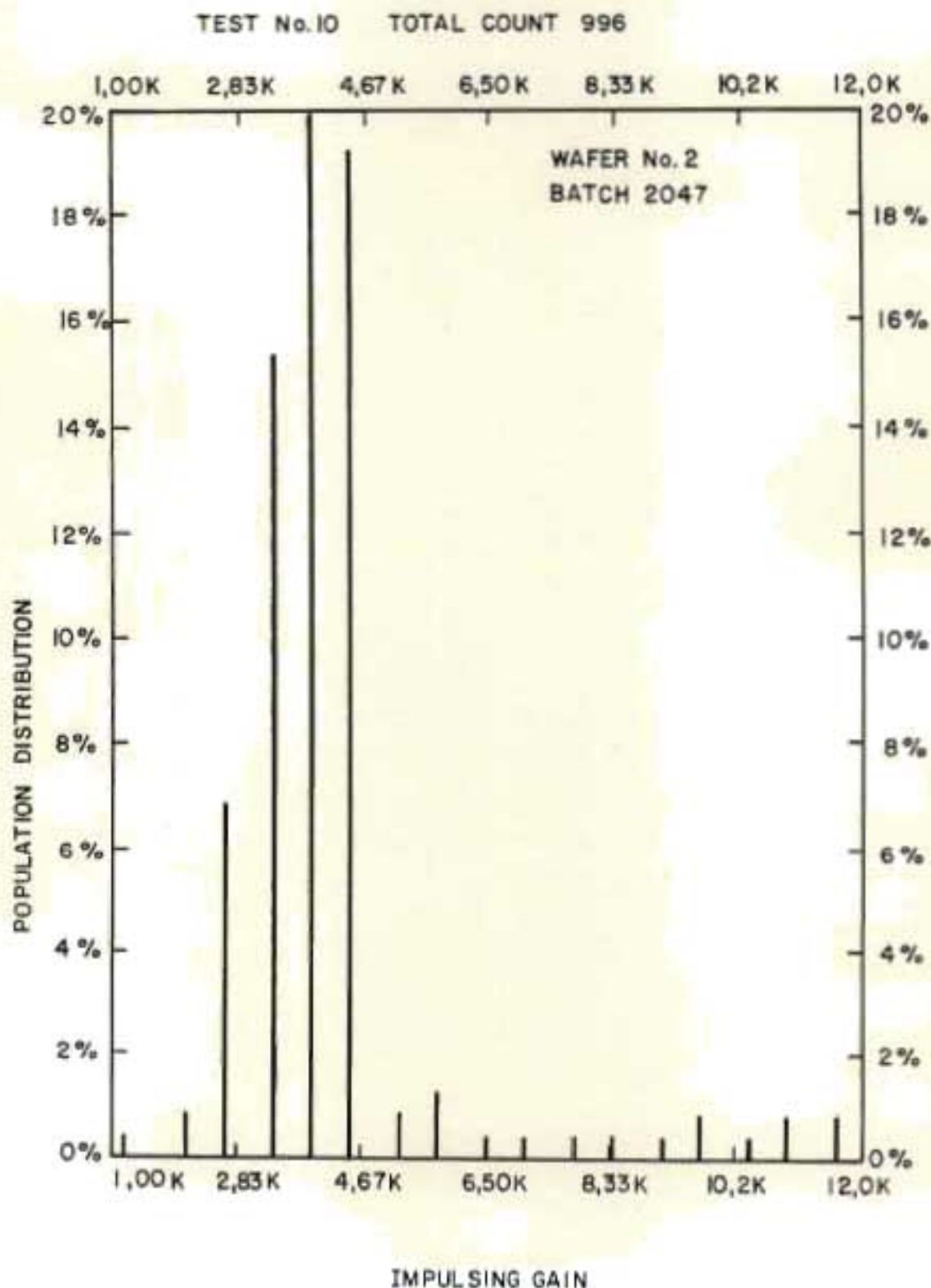
The conclusion drawn by the author was that the outstanding success achieved in the PT018 devices with both their extremely low leakage currents and also high stability could be attributed firstly to the use of the IM technique, where the metal interconnection layer was used as a field shielding guard ring to surround the sensitive areas of the device, and secondly to the processing of the devices on epitaxial silicon, manufactured to the revised specification.

c) Comparison of the gain spreads

Figure 3.20 (page 104) shows the distribution in gains on the same wafer, measured at $V_{CE} = 3$ V and $I_C = 100$ mA.

Approximately 85 per cent of the gain values measured were in the

Figure 3.20 Gain distribution for the impulsing condition ($V_{CE} = 3V$ and $I_C = 125\text{ mA}$). The spread is somewhat smaller than for the prototypes shown in Figures 3.16a and 3.16b, due to tighter process control measures. Without dropping the gains, a considerably improved breakdown yield is shown for this wafer in Figure 3.19

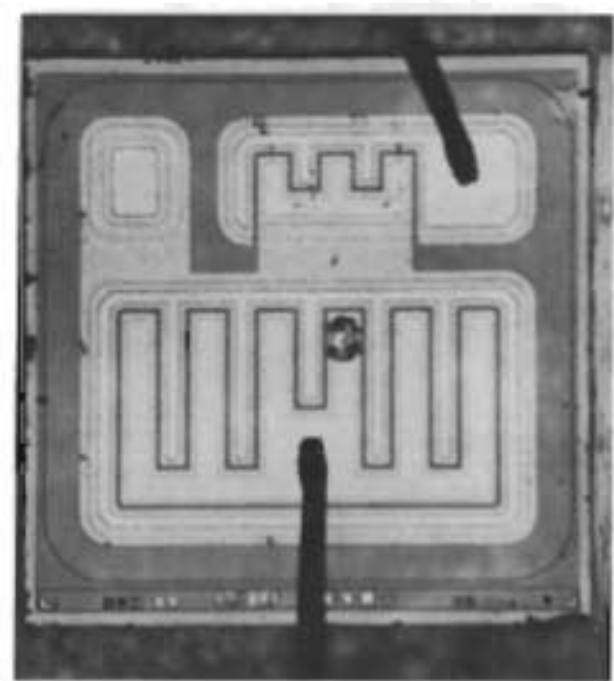


region between 2 000 and 5 000. This represents an only marginal improvement in the spread obtained for the prototypes shown in Figures 3.16a and 3.16b (page 93), but does demonstrate that the combination of both adequate gains and breakdown voltages could be achieved with the production layout and the revised silicon specification.

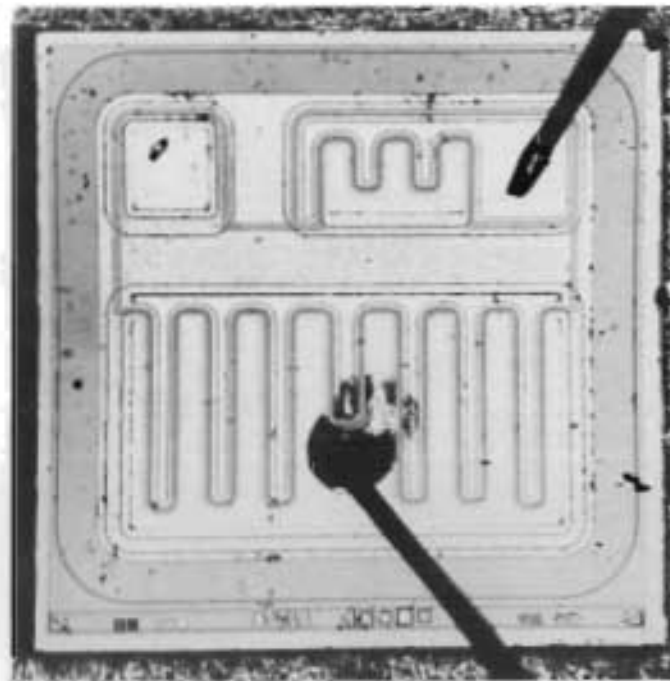
3.9.2 Surge failure mechanisms

The only specified parameter contributing really significantly towards the aim that the Darlington transistors should be resistant against surge failure in the telephone was the high collector-emitter breakdown, greater than 300 V. When surge testing the prototype integrated Darlington transistors, the telephone manufacturer³⁷ had applied a 4 kV surge to an off-hook Lorea test telephone. The O.N. transistor, which was conducting, was thus severely stressed in the 1 μ s or so before the gas arrester struck and reduced the surge voltage to less than 20 V. Three of the NI types submitted for evaluation had failed, and displayed a collector-emitter short, whilst five of the RI types had shown some degradation in $V_{CEO(SUS)}$. Inspection of the failed NI types clearly showed that failure was due to damage in the centre of the emitter region of the output transistors.

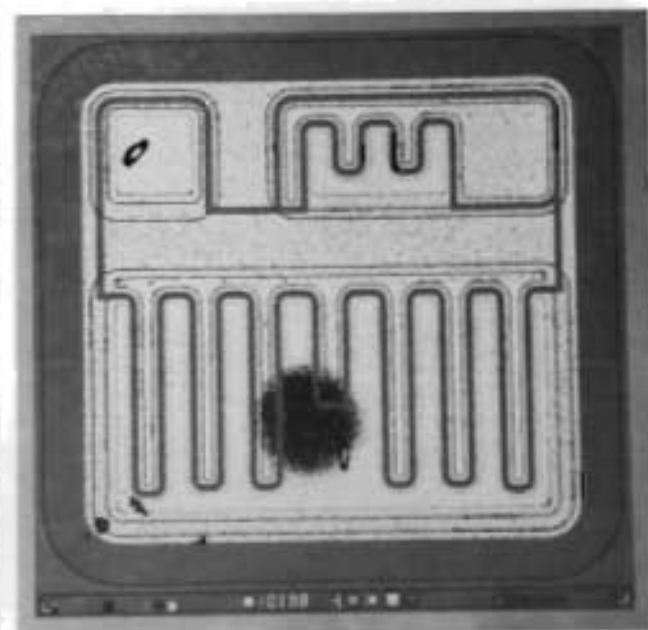
A limited number of prototype RI Darlington transistors were installed into pre-production Lorea telephones for field trial, and one device failed during a storm whilst in the on-hook condition. Again a collector-emitter short of the Darlington output stage had occurred, and the failed device is shown in Figure 3.21 (page 106). Measurements carried out on the telephone by the author, later confirmed by Parsley, pers. comm.⁸, indicated that the protection afforded by the surge diodes in the dial circuit was inadequate, particularly when the voltage appearing across the terminals of the telephone was too low to strike the 475 V gas arrester originally installed in the Lorea model of telephone. In this case, surge voltages of 400 V or more could appear across the Darlington transistors, a voltage that was higher than the collector-emitter breakdown voltage of these devices, stressing them into a destructive failure mode. In view of this, the increase in BV_{CEO} to a target minimum of 400 V for the PT018 was a positive step to counter this type of failure in the Lorea telephone.



1,27 mm



1,4 mm



1,4 mm

FIGURE 3.21 FIELD FAILURE OF A PTO18 DARLINGTON IN A LOREA TELEPHONE WHICH WAS ON-HOOK AND THE TRANSISTOR SWITCHED OFF. V_{CE} INCREASED TO BEYOND $V_{CEO(SUS)}$ AND DESTROYED THE TRANSISTOR BY A REVERSE SECOND BREAKDOWN MECHANISM. THE MARK ABOVE THE EMITTER BONDING WIRE IS FUSED ALUMINIUM AND SILICON.

FIGURE 3.22 LABORATORY-SIMULATED SURGE FAILURE OF A PTO18 IN A DISA TELEPHONE IN THE OFF-HOOK CONDITION. THE TRANSISTOR WAS CONDUCTING, AND THE SURGE ACROSS THE TRANSISTOR WAS 240 V AT 2 A FOR 1 ms. A COLLECTOR-EMITTER SHORT RESULTED FROM LOCALIZED HEATING UNDER THE EMITTER BONDING WIRE. (TESTS: SMITHIES³⁹ AND PARSELEY⁴⁰).

FIGURE 3.23 A REVERSE-BIAS STRESSED PTO18 TRANSISTOR. THE COLLECTOR-EMITTER VOLTAGE WAS 400V AT A COLLECTOR CURRENT OF 50 mA. THE CURRENT WAS INJECTED AT THE BOTTOM LEFT-HAND SIDE OF THE EMITTER, BUT THE HOT SPOT WAS FORMED IN THE CENTRE OF THE DEVICE. (TEST CONDUCTED AT NEERI).

In the newer Disa telephone, the problem was somewhat different, as the dial and speech circuits were switched off in the on-hook condition. Nevertheless failures of the O.N. Darlington, that conducted in the off-hook mode, occurred. These failures could simply be attributed to the fact that if the surge voltage was insufficiently high to strike the gas arrester, the full current of the surge could pass through the O.N. Darlington. Figure 3.22 (page 106) shows a laboratory-induced failure of an O.N. PT018 from a Disa Telephone. Again, failure occurred in the emitter region of the transistor, near the bonding wire.

Failure of both discrete 2N3439 transistors and PT018 devices in the the Disa telephone was due to the same mechanism, and such failure took place at similar voltage and current levels. The failures could certainly not be attributed to any shortcomings in the design of these devices, but rather to inadequate protection in the Disa telephone. Suitable protection systems for the Disa were proposed and evaluated by Smithies³⁹ and Parsley⁴⁰.

3.9.3 Failure mechanisms and their influence on device layout

Neither the driver nor the clamp transistors in the PT018 had suffered any apparent damage during any of the failures encountered, hence significant changes in the design of these two devices were not called for.

Further testing of the PT018 in the laboratory has shown that the only major failure mechanism is the thermal destruction of the output stage during surges. With additional protection, the surges in the O.N. stage of the Disa telephone were reduced but not eliminated, and it was found that on one pre-production batch of PT018 transistors, significant device degradation did take place on surge testing. In this batch of transistors the cause of the problem was found to be the use of over-hard bonding wires during assembly. Bond strength testing resulted in the removal of silicon fragments from the die, and microscopic examination showed that the damage penetrated into the junction region. That this damage was the cause of the degradation was confirmed when a batch of devices, assembled with softer bonding wires, was surge tested in the telephone and subsequent measurements revealed no degradation of the devices (Smithies⁴⁰).

Devices assembled with the harder bonding wires showed unstable $V_{CEO(SUS)}$ characteristics at 10 mA, clearly visible on a curve tracer but

passed by the automatic test gear.

In any future design, or revision of the existing design, two additional factors in locating the emitter bonding pads should be considered.

- (a) The bonding pad should be remote from the thermal stress region, and this could be done with the $\ast/018$ die. Figure 3.23 (page 106) shows a case where emitter current was injected at one side of the emitter metallization and the site of localized heating remained in the middle of the emitter region.
- (b) For better surge resistance, the location of the emitter bonding pad and layout of the emitter should provide a larger and less localized 'hot spot'. This location would necessitate numerous experimental structures as the process of hot spot formation in bipolar transistors is still not fully understood, and design data are lacking (Webb⁴¹).

3.9.4 Improved bonding pad placement for the $\ast/018$

In the case of the $\ast/018$ die, a diagonal placement of the device on the header was necessary and could have been avoided if the bonding pads for both base and emitter had been situated to one side of the die.

3.9.5 Contamination susceptibility of the PT018

The PT018 was an unpassivated device, primarily because no proved passivation technique suitable for medium-power high-voltage device production was locally available. Time and cost weighed heavily against the development of a passivation process, but use of an unpassivated device could be justified, for the following reasons

- (a) the device was to be encapsulated in a metal hermetic package only and would be in a dry nitrogen atmosphere; and
- (b) many millions of unpassivated transistors, assembled in this manner over a period of some twenty years, were in successful operation in subscriber equipment throughout the country.

Although point (b) was a most attractive precedent for the use of an unpassivated die, it did not offer a sound guarantee of reliability, as failure statistics did not exist for unpassivated devices manufactured at the assembly plant.

During 1981 the Quality Assurance Inspectorate of the Department of Posts and Telecommunications performed two comprehensive failure analysis studies on transistors removed from failed Protea telephones and forwarded from the country-wide field service stations. Appendix 3.3 (page 238) gives a summary of the report on the analysis of 602 type 'TR2 - Issue 3' unpassivated high-voltage transistors dating in manufacture from 1977 to 1981. Visual inspection of 476 transistors led to 46 per cent of the failures being attributed to assembly faults, and 18 per cent of the latter failures in turn being attributed to contamination.

To assess further the effects of assembly contamination on the PT018 Darlington, the author carried out an independent investigation on an early batch of these devices. The findings are presented in detail in Appendix 3.5 (page 240), measurements before and after assembly showing conclusively that contamination was a major factor leading to increased leakage currents and consequently a dramatically low assembly yield.

On presentation of the data in these reports, the transistor assembly plant, in collaboration with the Department of Posts and Telecommunications, radically revised their assembly procedures and screens, with the result that the quality of the devices after assembly improved very markedly.

3.9.6 Future need for a passivation layer?

The information gathered for the previous section clearly set a requirement for high assembly standards for the unpassivated Darlington transistor. Provided these standards were maintained and the devices were assembled in hermetic packages, there appeared no necessity for passivation.

At present there is a move in the telecommunications industry towards the use of plastic-encapsulated devices, particularly in systems serving only one or a few non-critical circuits, for example subscriber lines. If at some future stage, it were desired to assemble the Darlington in plastic

packages, a passivation layer would, in all probability, have to be developed and a number of further investigations become necessary, indicated below.

- (a) The layer would have to adhere well to the die and remain intact during extreme thermal stresses occurring during assembly and electrical operation of the device.
- (b) The layer would have to be able to withstand any extremes of temperature and humidity that would be encountered in both testing and in service and be capable of protecting the device against these.
- (c) Simple, economical and reliable processing techniques would have to be developed for depositing the layer.
- (d) The layer would have to have excellent stability under the influence of high electric fields, with no degradation of device reliability.
- (e) Layers should offer no degradation of the internal processes in the device and maintain the good resistance to external breakdown phenomena displayed by existing device designs.
- (f) Layers would have to be compatible with plastic encapsulants.

3.9.7 Reducing the critical clearances on the #/018 layout

With the excellent results obtained on leakage currents and breakdown stability of the PT018, it would be inadvisable to reduce any clearances that would affect these parameters. One aspect not covered in the development programme was the optimization of the clearance of $114 \mu\text{m}$ used between the P diffusions of the adjacent bases of the driver, clamp and output transistors.

Measurements made on unmetallized #/018 devices showed that the gain of the parasitic PNP transistors, using the collector of the Darlington as the N base region, was typically less than 0,2. Indeed during none of the tests and measurements conducted, did lateral PNP transistor action manifest itself in any way deleterious to the operation and reliability of the device. In the light of this it appeared that a decrease in the clearance between the P diffusions could be evaluated with a view to enlarging the active areas of

the driver and output stages and to improve the saturation performance of the output stage in particular. This would allow devices processed with a lower gain, measured above the knee voltage, to meet the Darlington gain requirements, resulting in improved yield figures. The cost of introducing a proved change would be low, as changes in mask layout alone would be required. The overriding factor to be borne in mind would be the requirement that lateral PNP gains should be prevented from becoming too high thereby reducing the saturation voltage in the manner described by Fields³⁶.

If additional process steps were decided upon, together with the inclusion of a passivation process, then some decrease in the P to N-depletion clearance could be considered. Two possible approaches to the problem of providing stability with reduced clearances can be suggested. One would be to implant an electric field shielding layer into the upper layer of the oxide in a manner similar to that used in buried SiO₂ layer MOS structures described by Nakashima et al.⁴². The second approach would be to modify the silicon surface doping level by ion implantation as indicated by Baliga³². The adoption of either technique in the present case would have necessitated considerable experimental work and involved extra processing steps that could not have been carried out on site at NEERI.

3.9.8 The specification for the PT018 transistor and life testing

A full specification for the PT018 was drawn up in a joint effort by the author, the Engineering and Quality Assurance sections of the transistor assembly plant, the Quality Assurance section of the Department of Posts and Telecommunications and the Quality Assurance Division of the telephone manufacturer. It is important to note that this was the first time that a specification of this nature, relating primarily to the quality of a semiconductor component, had been drawn up locally. This was indeed an event of particular local importance as the device had no commercial equivalent and there was hence no equivalent specification.

This specification, reproduced in Appendix 3.6 (page 243), not only gives the primary electrical specification for the PT018, as listed in Table 3A (page 62), but lists the 'end of life' parameters that may not be passed. These parameters gave a clear indication of the permitted parameter drifts

between measurements on the device after assembly and at the termination of a 1 000-hour, high-temperature accelerated life test.

Two samples of 40 transistors have been evaluated according to the specification, one batch at the transistor assembly plant and one at NEERI. The devices were subjected to the accelerated life test, as specified. Only one device at NEERI failed (parametrically out of specification) during the first 48 hours. Beyond this, there were no failures over the 1 000-hour period, and parametric changes were negligible. Calculations by Schoombie, pers. comm.[#], indicate a mean time to failure of almost 3 million hours at 45 °C for reverse bias stressed devices and over 4 million hours for the forward biased condition at the same temperature. Any such prediction of the in-service failure rate, based on such limited data as was available, is not reliable as the acceleration factors depend critically on the failure mechanism(s) for the device, and these had still to be established. As the accelerated life tests were to be carried out on a regular basis and, where failures occurred, failure analyses were to be carried out to help provide more reliable lifetime data. In order more rapidly to establish the failure mechanisms likely to occur in the device, the author has suggested stressing additional batches of test devices at successively higher temperatures until failures were induced.

On the basis of data thus gathered an accurate reliability record would, for the first time on the local scene, be provided. This would enable timeous action to be taken to modify or improve both the process technologies and the design of the device, if required.

3.10 CONCLUSION

The successful development of a unique high-voltage integrated Darlington transistor proved that the methodology applied in the design was sound. The development period from inception to completion of the final component design was only about nine months, and in the long evaluation period of almost two years before the component was put into production, no design changes of any form were found to be necessary. As indicated in the sub-sections of 3.9, a number of minor changes and improvements could be made to the PT018, but these would not be undertaken unless there were

[#]F Schoombie (1984) Quality Assurance Inspectorate, Dept of Posts and Tele-

strong reasons for doing so.

The most important, and indeed highly successful innovations in the device design were the incorporation of a clamp transistor to minimize external fields and the development of the 'Inverted Metallization' (IM) layout technique to shield sensitive circuit elements from high external fields.

Should any subsequent designs be undertaken, a well-defined and more general design procedure would be of the greatest assistance, particularly for devices exhibiting quasi-saturation effects. Here, the design of the PT018 was primarily empirical, with major decisions on the layout and active areas required being based on the properties of known or pre-production prototype devices.

Numerical methods to assist in the design were not available, and attempts to model quasi-saturation using the simulation programme 'SPICE' met with failure. If a method of modelling two-region saturation had been available, it would undoubtedly have been possible to optimize the active areas of the devices without recourse to a second layout iteration, and it is likely that the other design details decided upon after the prototype fabrication exercise was completed could have been introduced as refinements to an almost complete design. This lack of a suitable modelling method acted as the catalyst for the development of the graphical and numerical modelling procedures presented in Chapter 4.

CHAPTER 4

A VERSATILE GRAPHICAL MODEL FOR THE ACCURATE NUMERICAL PREDICTION
OF THE OPERATING CONDITIONS OF BIPOLAR TRANSISTORS IN BOTH THE
QUASI-SATURATION AND CUT-OFF REGIONS

4.1 INTRODUCTION AND SUMMARY OF CHAPTER

Chapter 2 covered the successful design of a high-voltage transistor, the PT014, that had to operate in the normal region in which quasi-saturation played an insignificant role. In Chapter 3, however, the success of the design of the integrated Darlington transistor, the PT018, relied on the fact that for acceptable performance in the telephone the output stage of the device had to operate either in full saturation or quasi-saturation. Indeed, when successfully optimizing the area of the PT018, which was essential for a cost-effective device, the key requirement borne in mind was that the output stage should operate in quasi-saturation at the upper limiting current conditions. The methods used in designing the PT018 relied chiefly on measurements made on similar discrete devices, and the design was evaluated by using a prototype integrated Darlington. No available systematic design method was found to be applicable for dealing with the requirements of the PT018 integrated Darlington.

In order to fulfil the requirement for a general and straightforward design technique for predicting operation in quasi-saturation and cut-off in bipolar transistors, a radically new graphical design technique was developed, introducing two entirely new parameters to quantify conditions in these regions. This design technique is presented in this chapter. The two parameters, the **Quasi-saturation Resistance, R_{QS}** , and the **Cut-off Voltage, V_{CO}** , were both easy to measure and the methods by which they could be applied were suitable for use by either the device technologist or the circuit designer. It was confirmed experimentally that for devices operating at low to medium injection levels, operation in the quasi-saturation region could be adequately characterized using the new parameter R_{QS} . Extension of the model to include both high-injection levels and temperature effects widened the field of application considerably.

Whilst the model was developed primarily as a design aid for high-voltage transistors, it was observed at a very early stage that the method

could be used to predict saturation operation in virtually any transistor. When gain crowding at high-injection levels was included, the graphical model was successfully applied, as an example, to a design evaluation of the PT018 integrated Darlington transistor. This evaluation covered both the specified operating conditions and what is more the limits of operation of the device at both high-voltage and high-current levels. Presented in this chapter is a comprehensive set of computed performance curves relating to the PT018 and the fabrication process used. In addition to showing that the design of the PT018 was far more conservative than originally supposed, the curves serve to demonstrate the large number of variables to be considered in the design of a Darlington transistor and demonstrate, for the first time, how it is possible reliably to predict optimized saturation performance for a Darlington transistor in any given fabrication process and for any set of operating conditions.

In the wider context, the author strongly feels that owing to its inherent simplicity and accuracy, the saturation model presented here should be readily applicable to common integrated circuit analysis programs, and become available for this purpose.

4.2 MODELLING SATURATION IN HIGH-VOLTAGE DISCRETE TRANSISTORS

4.2.1 Regions of operation in high-voltage bipolar transistors

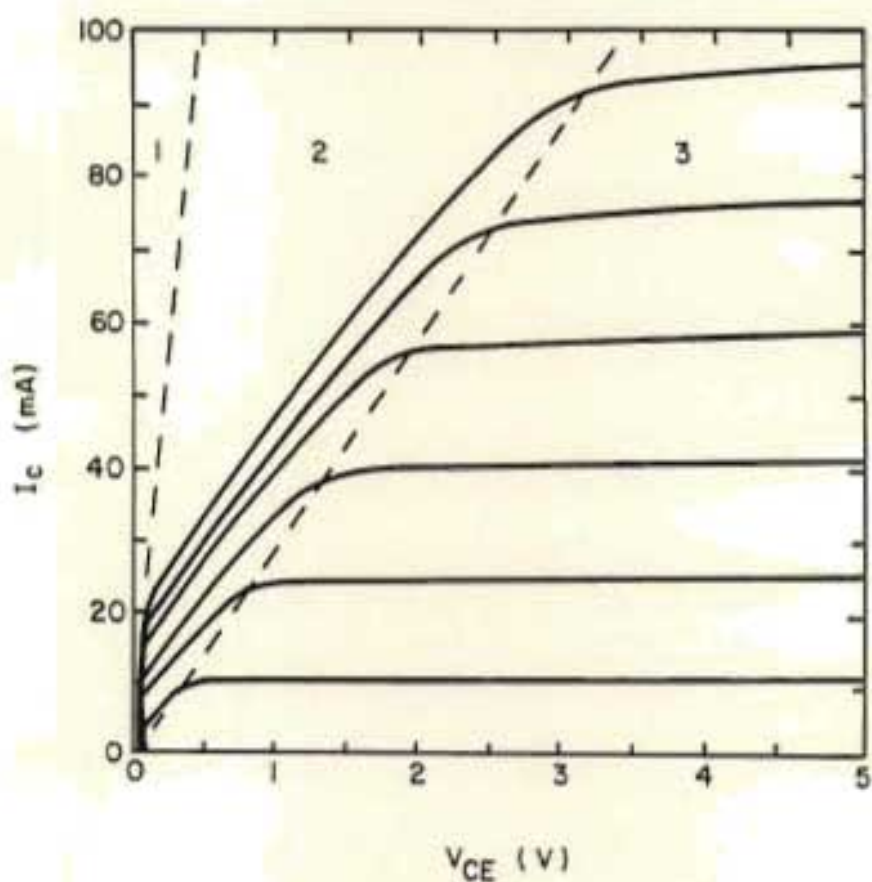
As noted in the preceding section, Chapter 2 dealt with the design of a transistor that had to operate in the normal region, whilst Chapter 3 was concerned more closely with operation in the quasi-saturation region but did not cover the transition in operating point from saturation to quasi-saturation. This section further describes the regions of operation in order to clarify the reasoning behind the proposals for the saturation models.

Figure 4.1 (page 116) is a tracing of a family of I_C vs V_{CE} curves from a curve tracer, with the regions of operation marked. These regions, not to be confused with similar terms used in modelling with the program 'SPICE' are the following.

Region 1 The true saturation region

At high-injection levels the collector is saturated with majority

Figure 4.1 Saturation regions of a transistor meeting the PTO14 electrical specification



REGIONS 1, 2 AND 3 ARE DESCRIBED IN THE TEXT.

carriers and behaves essentially as a conductor. At lower levels of injection, transistor action modulates the resistance of this region, and at the low collector-emitter voltages normally associated with saturation the transistor, for the purposes of this chapter, is considered to be operating in the collector cut-off region.

Region 2 The quasi-saturation region

Owing to high collector-region resistance, the collector-base junction itself is not necessarily reverse-biased and the collector region only partially saturated with majority carriers. As a result, the collector resistance is modulated, producing the steep characteristics observed.

(Note : The Collector Resistance R_C , referred to frequently in this chapter, is the passive resistance associated with the collector region of a transistor. Collector resistance is not measured directly, and is usually calculated from the slope of the the line separating regions 2 and 3 on the I_C vs V_{CE} characteristic.)

A fuller discussion of quasi-saturation is given by Ghandi⁴³.

Region 3 Normal bipolar transistor operation

Here the collector-base junction is reverse-biased, and normal bipolar transistor operation applies, as characterized by the Early voltage.

4.2.2 Operation in the quasi-saturation region and the need for a model

Quasi-saturation is commonly encountered in a wide range of small-signal devices. To demonstrate this, the typical characteristics of a BC107, a small-signal 45 V NPN Jevise, and a 2N3439, a medium-power 350 V NPN device, are given in Figures 4.2a and 4.2b (page 118) respectively. Both devices exhibit the effect, but it is more marked in the higher-voltage transistor. The chief features of quasi-saturation pertinent to this chapter are listed below.

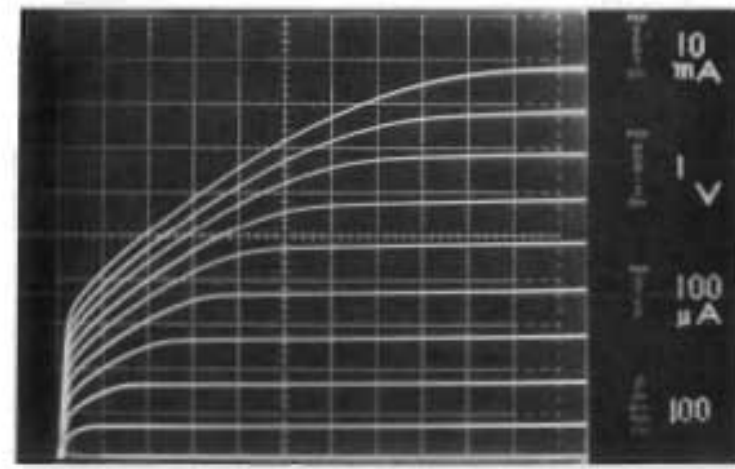
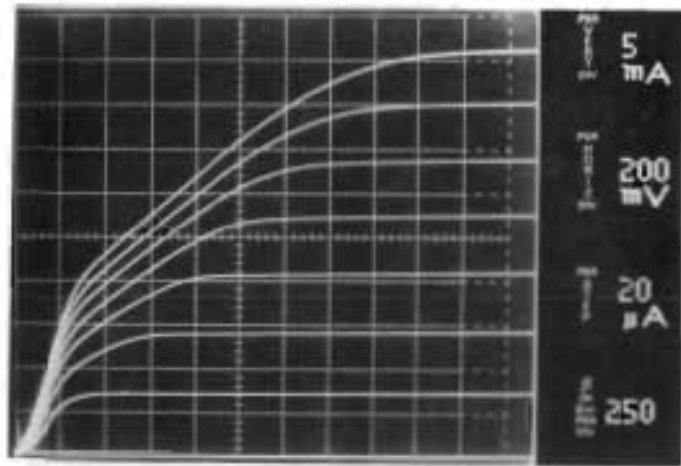


FIGURE 4.2a A LOW-VOLTAGE TRANSISTOR:
SATURATION CHARACTERISTICS OF A BC107
SMALL-SIGNAL TRANSISTOR WITH A $V_{CE0(SUS)}$
OF ONLY 45 V.
THE DEVICE SHOWS QUASI-SATURATION OPE-
RATION AT WELL BELOW THE DISSIPATION
LIMIT OF 300 mW. IT IS CLEAR THAT QUASI-
SATURATION OPERATION SHOULD BE CONSI-
DERED IN THE APPLICATION OF THIS DEVICE.

(DIE TYPE */003. MANUFACTURER: NEERI).

FIGURE 4.2b A HIGH-VOLTAGE TRANSISTOR:
SATURATION CHARACTERISTICS OF A 2N3439
MEDIUM-POWER TRANSISTOR WITH A $V_{CE0(SUS)}$
OF 350 V.
QUASI-SATURATION OPERATION IS VERY
MARKED IN THIS DEVICE EVEN THOUGH THE
DIE AREA WAS APPROXIMATELY TEN TIMES
GREATER THAN THAT OF THE BC107.

(DEVICE CODE : CCSA 2N3439L. DATE OF
 MANUFACTURE 1980, WEEK 27. THIS IS THE
 SAME DEVICE USED FOR FIGURE 3.11, PAGE 83).

- (a) Quasi-saturation is a characteristic that transistor manufacturers generally ignore in any transistor specification, although it is so commonly encountered. To avoid the problem of having to consider it directly, the usual approach is simply to guarantee minimum gains at fixed operating points, generally outside the quasi-saturation region.
- (b) Quasi-saturation is a phenomenon that is not modelled by the widely used simulation program 'SPICE', incorporating the Gummel-Poon model for the bipolar transistor⁴⁴. The measured quasi-saturation characteristic of a PT014 transistor, and saturation as predicted by 'SPICE', are compared in Figure 4.3 (page 120). (The reason for the very large gain difference between measured and predicted characteristics, once the device has reached the normal operation region, is that the gain measurements for the SPICE simulation were made at zero collector-base voltage at the terminals of the PT014. Although it may be common practice to characterize small integrated circuit transistors at zero applied collector-base voltage, the method is obviously quite unsuitable where the transistor has a substantial collector-region resistance.)

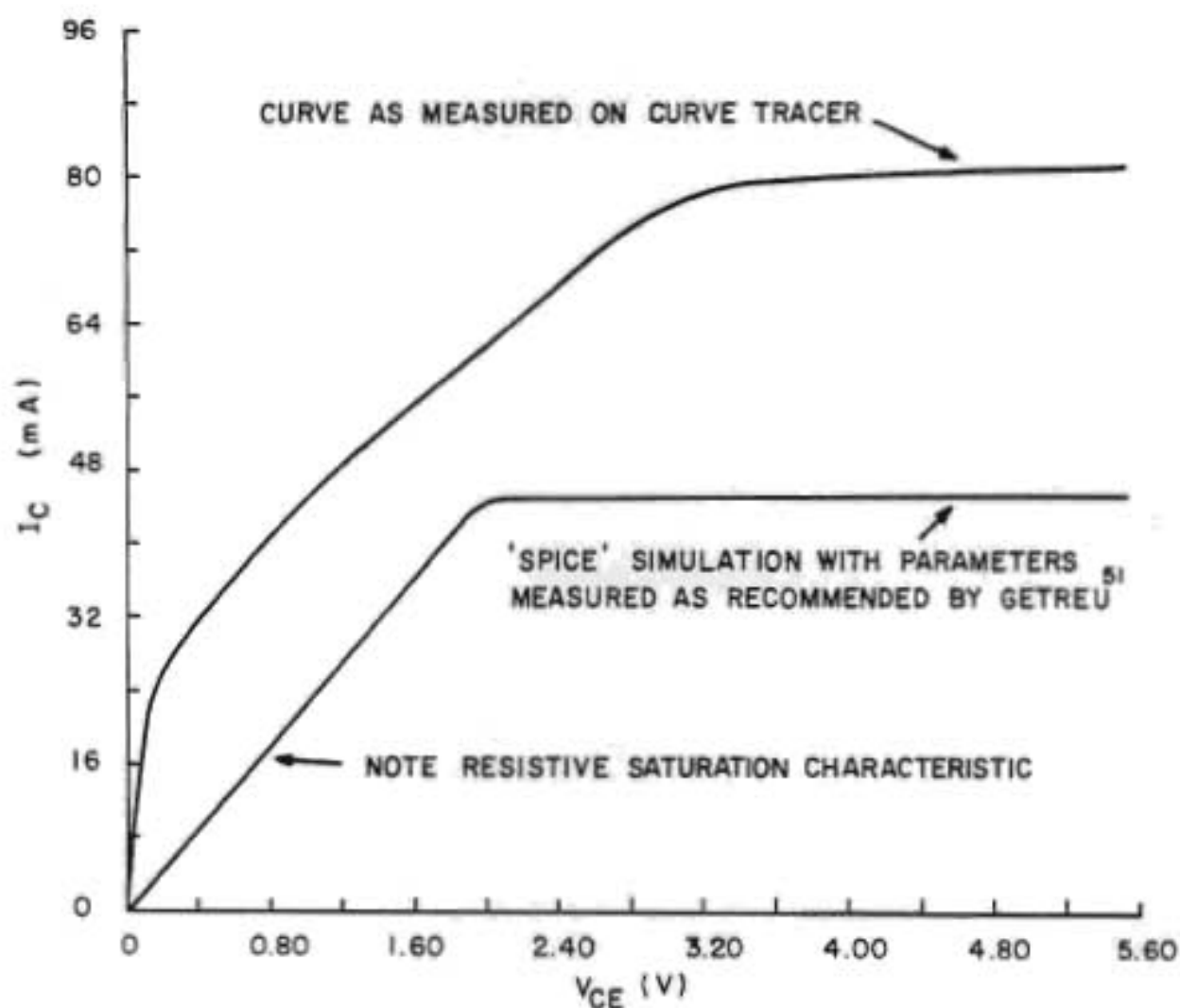
In conclusion it is useful to highlight a paragraph taken from Getreu⁴⁴ who, in discussing the bipolar transistor models used in SPICE, states 'Probably the most significant limitations of the models described here are a lack of modeling of three dimensional effects, junction breakdown and an accurate saturation model.'

4.2.3 Non-availability of a numerical method to quantify quasi-saturation

Kurata⁴⁵ discusses the physical aspects of quasi-saturation and indicates how a numerical technique, of some considerable complexity, can be developed to model the effect. The methods described are certainly not user-orientated and would be extremely difficult to apply by a designer who did not have available considerable information on both the process parameters and the various physical values that would be required to use the technique.

The need for a simple user-orientated model to quantify two-region saturation is now obvious, and in Sections 4.3 and 4.4 two simple graphical models are proposed for simulating the phenomenon.

Figure 4.3

PT014: I_C vs V_{CE} : SATURATION CHARACTERISTICS

N.B. GAIN OUTSIDE SATURATION IS FAR LOWER IN THE 'SPICE' SIMULATION AS THE PEAK GAIN WAS RECORDED AT $V_{CB} = 0$ V ON THE TRANSISTOR TERMINALS.

4.3 THE FIRST GRAPHICAL MODEL, 'MODEL 1'

Two graphical models were developed in this study, and although the second was preferred to the first because it proved to be more simple to use and was more accurate, the first model is also presented as it does satisfy most of the objectives laid down for a graphical model. A suitable model should

- (a) be simple but nevertheless fairly accurate;
- (b) have model parameters that relate simply to easily measurable device parameters; and
- (c) be of use to both device and circuit designers.

4.3.1 A description of 'Model 1'

As a basis of the first model, it was assumed that extension of the I_C vs V_{CE} curves in region 2 should intercept at some, hopefully unique point, typically where the values of V_{CE} and I_C are negative. The intercept values are termed the **Quasi-saturation Voltage, V_{QS}** , and the **Quasi-saturation Current, I_{QS}** . 'Model 1' is shown in Figure 4.4 (page 122). The collector cut-off characteristic is the classical model given by Burger and Donovan⁴⁶, and this part of the characteristic is shown in more detail in Figure 4.5 (page 122).

4.3.2 Shortcomings of 'Model 1'

In use, Model 1 had a number of shortcomings, listed below.

- (a) Difficulty was experienced in measuring V_{QS} and I_{QS} . There was no direct method of obtaining these values and it was necessary to extrapolate from I_C vs V_{CE} measurements. It was also found that the values obtained varied greatly according to which operator performed the measurements.
- (b) The values of V_{QS} and I_{QS} were valid for less than a tenfold change in collector current I_C before new estimates had to be made. The error was greatest near the cut-off region, and

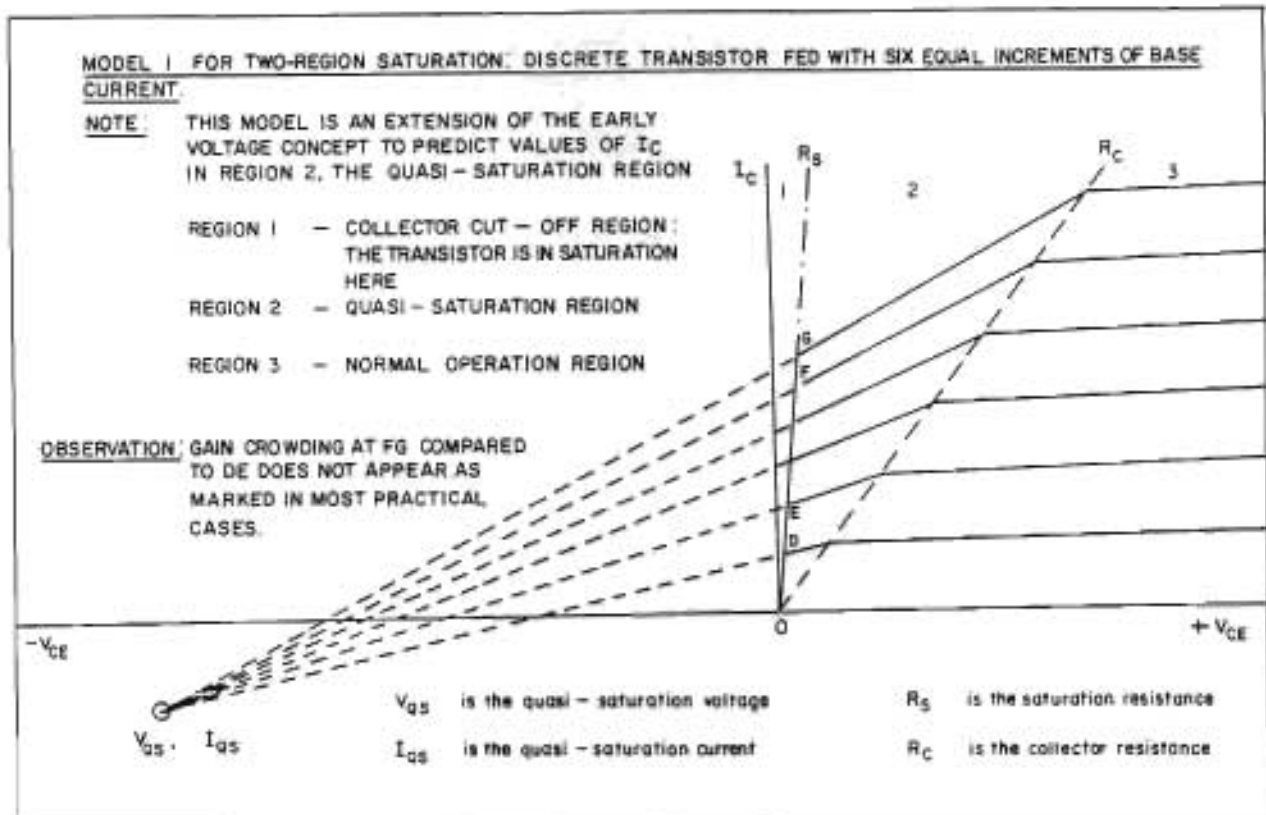


FIGURE 4.4 FIRST MODEL FOR TWO REGION SATURATION

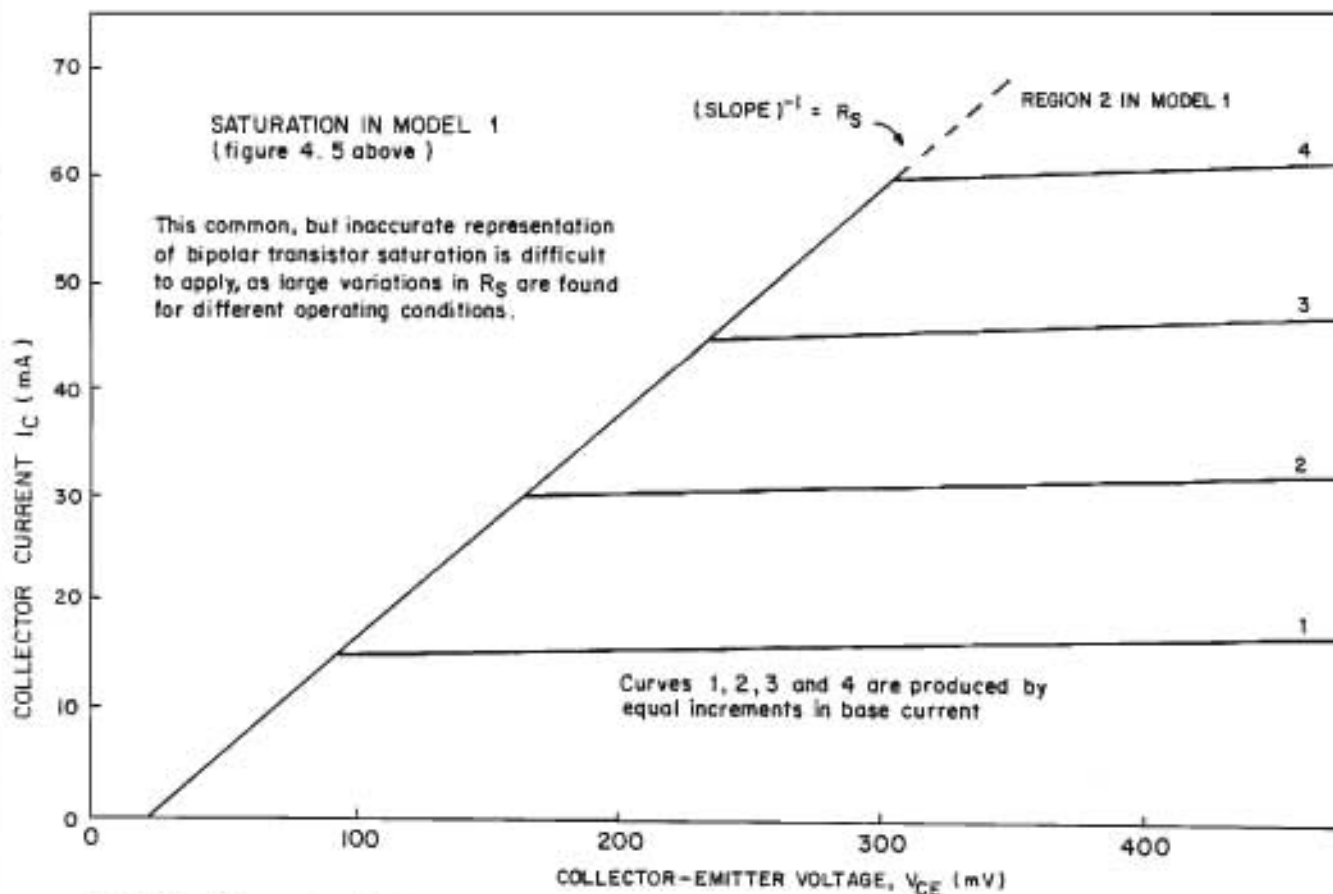


FIGURE 4.5 THE CONSTANT SATURATION RESISTANCE REPRESENTATION OF SATURATION

in practice it was also found that the slope of the actual quasi-saturation characteristic tended to decrease at higher current levels, instead of increasing as indicated in this model.

- (c) No unique value of saturation resistance R_S could be determined in the high-voltage transistors investigated, where emitter current densities did not exceed about $0,5 \text{ A/mm}^2$. This inconsistency was the result of differing drive conditions causing variations in R_S .
- (d) The model had no physical basis that could be cited as a justification for assuming that convergence to a unique set of values of V_{QS} and I_{QS} should occur.

4.4 'MODEL 2', A SIMPLER AND MORE ACCURATE GRAPHICAL MODEL

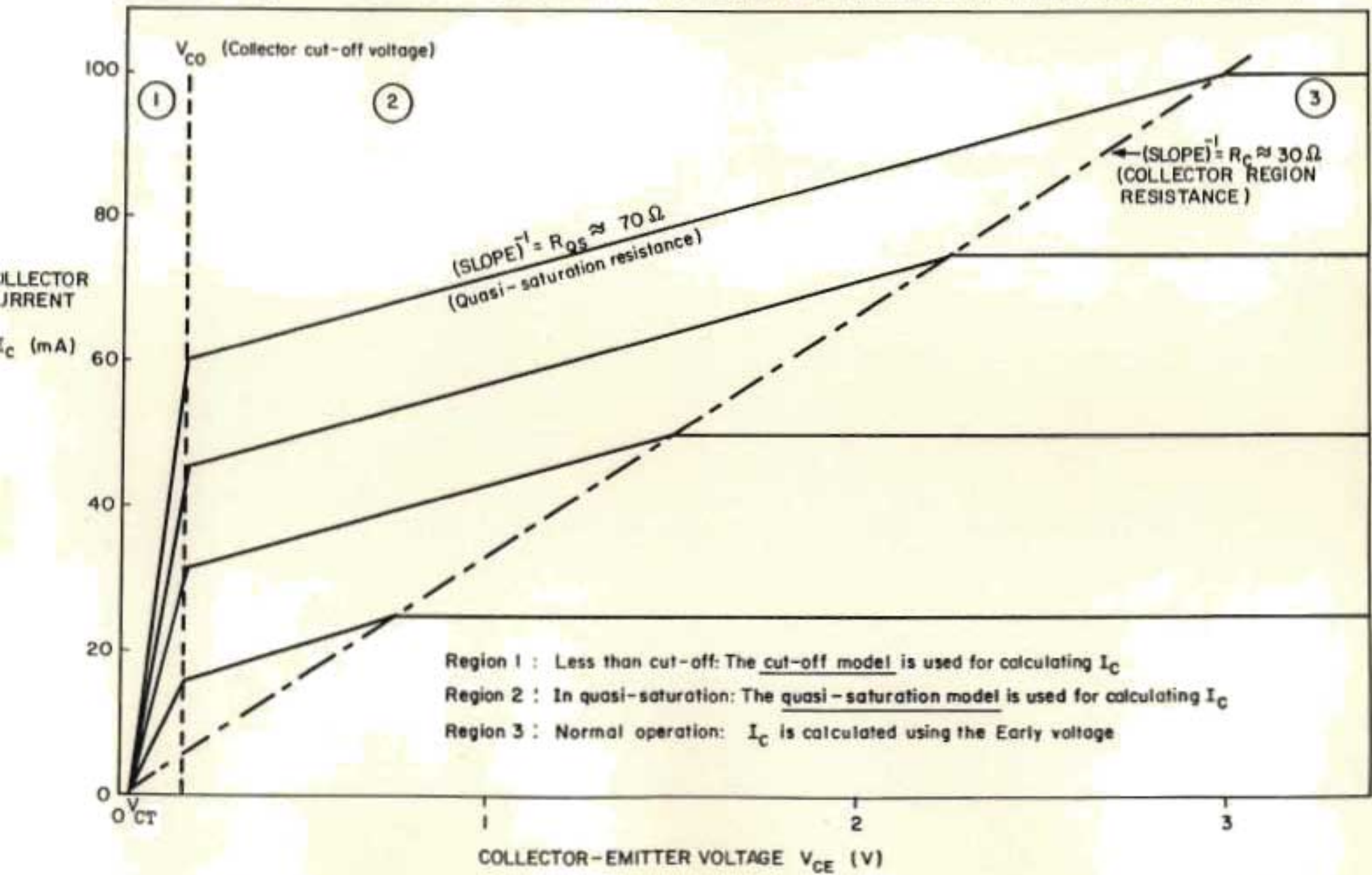
In view of the potential value of Model 1, a second graphical model with fewer shortcomings than Model 1 was proposed in order more adequately to meet the requirements listed at the beginning of Section 4.3. This model, termed Model 2, covered all three regions of operation of a transistor below breakdown. Model 2 is shown in Figure 4.6 (page 124). As the equations for operation extend downwards from normal operation through quasi-saturation into cut-off, the model is described in this order. In more general application of the model, to prevent unrealistically high collector currents from being predicted, a correction factor was included for gain crowding at high-injection currents. Compensation for temperature effects was also included into the model.

4.4.1 Region 3 : Normal operation characterized by the Early voltage, V_E

Referring to Figure 4.6 (page 124), the normal operation region is that where $V_{CE} > R_C \times I_C$, for any given value of I_C , and the collector current is calculated using the classical Early voltage equation⁴⁷ :

$$I_C = h_{FEM} \times I_B \{ 1 + (V_{CE} - V_K) / (V_E + V_K) \} \quad \dots\dots\dots 4.4A$$

FIGURE 4.6 DISCRETE TRANSISTOR: TWO-REGION SATURATION GRAPHICAL MODEL: MODEL 2



where

h_{FEM} is termed the 'Process Gain' and is the common emitter current gain at the transition to region 3;

I_B is the base current;

I_C is the collector current;

V_{CE} is the applied collector-emitter voltage;

V_E is the Early voltage; and

V_K is the 'Model 2 Knee voltage' at the transition to normal operation in region 3; it is a function of the collector current I_C and the collector resistance R_C .

(V_K should not be confused with the knee voltage V_{CEK} , defined specifically for the TR2 - Issue 3 Specification, as shown in Figure 2.2 (page 13), because V_{CEK} is not related in definition to the collector-region resistance, R_C .)

4.4.2 Region 2 : Quasi-saturation operation

Although good physical analyses of saturation, including quasi-saturation effects, have been given by Clark⁴⁸, Chudobiak⁴⁹ and Hower⁵⁰, none of these analyses was suitable for simple numerical modelling, owing to the large number of physical parameters that would need to be measured or estimated. At best, only the device designer would be able to use these models, and even then only in a sufficiently well-characterized process.

4.4.2.1 An entirely new parameter : The Quasi-saturation Resistance, R_{QS}

Observation of the quasi-saturation characteristics of a large number of devices under emitter injection conditions of less than $0,5 \text{ A/mm}^2$ led to the conclusion that the best graphical approach was to assume that the I_C vs V_{CE} characteristics formed a family of parallel lines in region 2, the quasi-saturation region. This conjecture is certainly plausible if Figure 4.1 (page 116) and Figures 4.2a and 4.2b (page 118) are considered. Assuming this, the inverse of the slope of the collector characteristic has the dimensions of resistance : a constant resistance in fact, if the lines are parallel. This is an entirely original proposition, and this resistance is termed the

'Quasi-saturation Resistance', R_{QS} . Figure 4.6 (page 124) shows the graphical representation of this parameter.

Except at high-injection levels of greater than 1 A/mm^2 , where the collector characteristics may be very distorted, it is a simple matter to measure R_{QS} . The method found to be most successful and repeatable with a number of different operators was to take the gradient between two points on the I_C vs V_{CE} characteristic. These points were at 20 per cent and 80 per cent along the quasi-saturation characteristic and were measured at the onset of quasi-saturation at low-injection levels.

It was also found that one value of R_{QS} was sufficient to characterize quasi-saturation operation accurately enough for the full range of current densities encountered for both the PT014 discrete transistor and the PT018 integrated Darlington transistor at all specified operating conditions.

4.4.2.2 A second constant : The Process Constant, PC

Since R_{QS} was being assumed constant, and the collector resistance R_C was a constant proportional to the area of the device, the ratio of R_{QS}/R_C was a constant. This quantity is termed the Process Constant, PC. In practice it was found that the value of PC ranged from about 1.2 to 2.4 depending on both type and manufacture of the device. From a number of measurements made on the four different transistor patterns available at NEERI, it was also found that the geometry and area of devices, when these were made by the same process, did not have any effect on the value of PC : the process used was the major factor influencing PC.

4.4.2.3 Calculation of collector current in region 2 using R_{QS}

From Figure 4.6 (page 124), considering regions 3 and 2 :

$$\begin{aligned} I_C &= h_{FEM} \times I_B - (h_{FEM} \times I_B \times R_C - V_{CE})/R_{QS} \\ &= h_{FEM} \times I_B (1 - R_C/R_{QS}) + V_{CE}/R_{QS} \quad \dots\dots\dots 4.4B \end{aligned}$$

where the symbols are as given in Section 4.4.1 for region 3, and R_{QS} is the newly defined parameter, the Quasi-saturation Resistance.

4.4.3 Modelling the saturation and cut-off regions

It was noted in Section 4.3.2 that there was no uniquely defined saturation resistance R_S that was acceptable for modelling. Therefore a new model termed the **Constant Cut-off Voltage Model** was proposed, and this is described below.

4.4.3.1 The Constant Cut-off Voltage, V_{CO}

Measurements were made on a wide range of medium-power devices, some exhibiting marked quasi-saturation effects, and others not. The results have shown that the transition from cut-off to active transistor operation takes place at a virtually constant voltage, generally in the region of 0,15 to 0,3 V. This held for virtually all collector currents below the injection level of $0,5 \text{ A/mm}^2$. Figure 4.7 (page 128) illustrates that the voltage at which the transition occurs from cut-off to normal transistor operation or quasi-saturation operation, was virtually constant over more than four decades of collector current. This 'constant voltage' was termed the **Constant Cut-off Voltage** and is represented by the symbol V_{CO} .

4.4.3.2 The Conduction Threshold Voltage, V_{CT}

Active transistor action was found to cease at a threshold voltage in the region of 25 mV ($\approx kT/q$) at low-injection levels. This 'constant voltage' was termed the **Conduction Threshold Voltage, V_{CT}** .

At higher values of base current there is a tendency for V_{CT} to decrease, but this decrease was neglected as it was found during the computation of I_C vs V_{CE} for the Darlington transistor (described in Section 4.6.4, page 151) that the cut-off conditions matched the measured values very well in terms of the general requirements for a model, as given in Section 4.3.

4.4.3.3 The graphical cut-off model for region 1

The cut-off model for region 1 is shown in Figure 4.8 (page 129), and it incorporates the two new parameters: the cut-off voltage V_{CO} and the conduction threshold voltage V_{CT} . The collector current in the

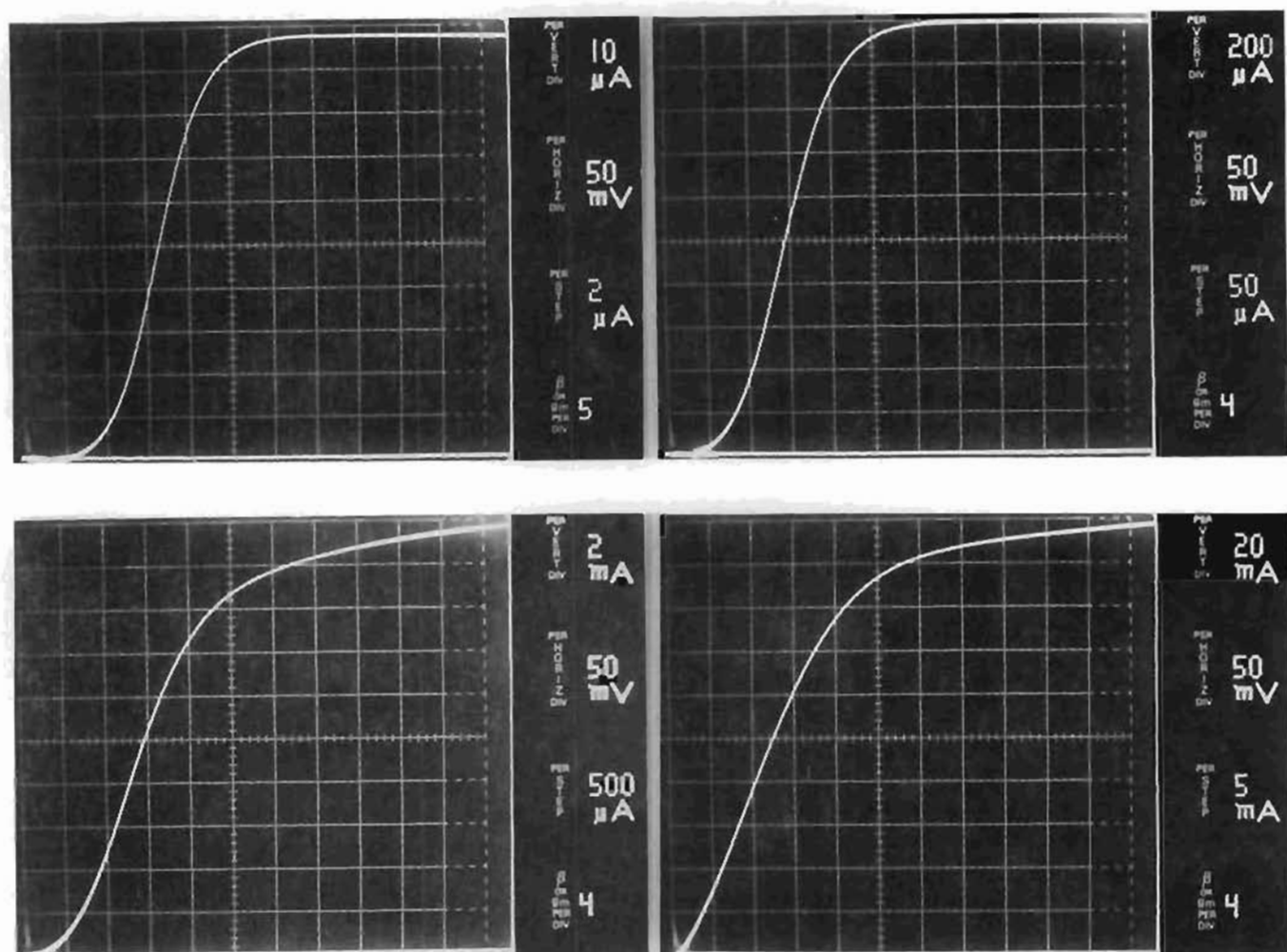
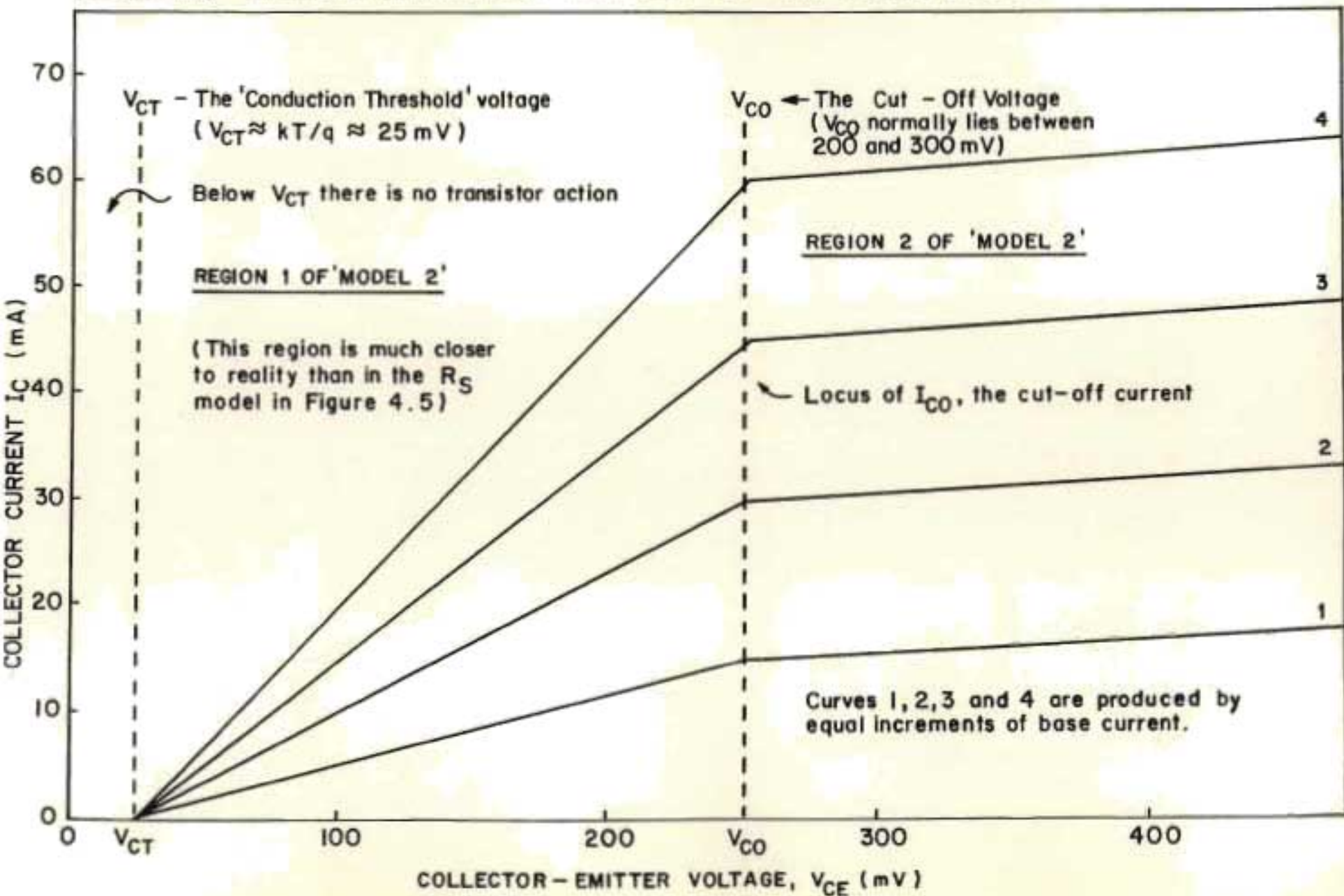


Figure 4.7

Collector cut-off characteristics of a PTO14 transistor. The four figures, spanning over four decades of collector current, show quite clearly that the transition to normal operation (or quasi-saturation at higher collector currents) takes place at an almost constant voltage which, for the large number of device types tested, was generally between 200 mV and 300 mV.

FIGURE 4.8 DISCRETE TRANSISTOR: CONSTANT CUT-OFF VOLTAGE MODEL



cut-off region is calculated as follows. Starting with equation 4.4B, the current I_{CO} at the transition from cut-off to quasi-saturation is given by

$$I_{CO} = h_{FEM} \times I_B (1 - R_C/R_{QS}) + V_{CO}/R_{QS}.$$

As the transistor is assumed to cease operation at

$$V_{CE} = V_{CT} = 25\text{mV}, \text{ which is } kT/q, \text{ then :}$$

$$I_C = I_{CO} \times (V_{CE} - kT/q)/(V_{CO} - kT/q). \quad \dots\dots\dots 4.4C$$

In practice a default value of $T = 300^\circ\text{K}$ (27°C) was used.

4.4.4 Correction for high-injection operation

Model 2 in its basic form was found to be quite adequate for simulating the operation of the PT014, and later the PT018 Darlington transistor, under their specified operating conditions. In order, however, that the model should be of more general application, it was necessary to include the effects of decrease in gain at high-injection levels, so as to obviate the likelihood of unrealistically high currents being predicted. As quasi-saturation was not normally encountered at very low injection levels, where Model 2 simply excludes the phenomenon by showing a normal transistor characteristic with immediate transition from region 1 to region 3, no attempt was made to cover gain crowding at very low collector currents.

4.4.4.1 The gain droop equation at high-injection levels

It was noted that the transition from region 2, quasi-saturation, to region 3, normal operation, became ill-defined, particularly at injection levels above 0.5 A/mm^2 . As the collector resistance R_C was a necessary constant in Model 2, a further graphical model, compatible with Model 2, was developed to compensate for high injection and to enable use to be made of values of collector resistance R_C measured at lower injection levels.

The gain of a number of high-voltage transistors was measured over a wide range of collector currents, with the collector-emitter voltage equal to the knee voltage, as given by

$$V_{CE} = V_K = R_C \times I_K \quad \dots\dots\dots 4.4D$$

For the PT014 and both the driver and output stages of the PT018 (measured separately) the gain was constant up to about $0,3 \text{ A/mm}^2$ and was simply the same as the value of the process gain, h_{FEM} , used in Model 2.

Figures 4.9a and 4.9b (page 132) show the normalized gains of the PT014 and PT018 measured as a function of current density. On the log-log scales used, it is seen that above a collector current density J_C of about 1 A/mm^2 the decrease in gain becomes linear and is of the form :

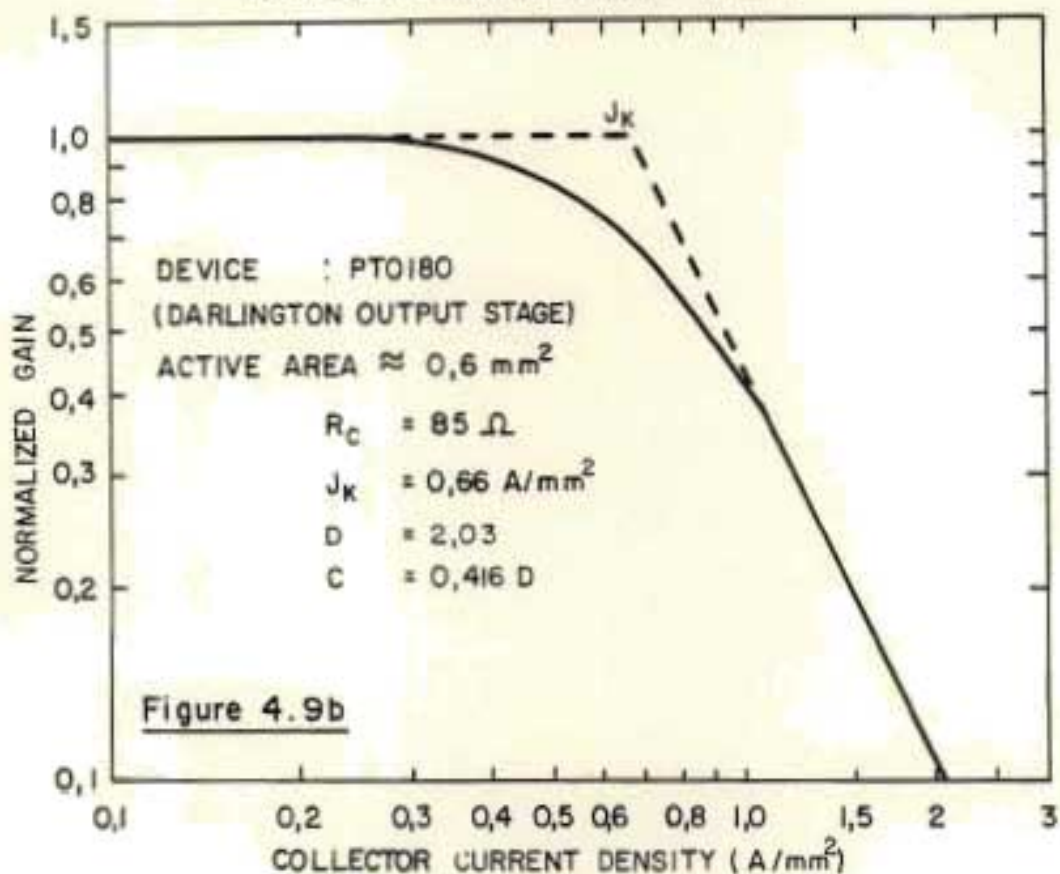
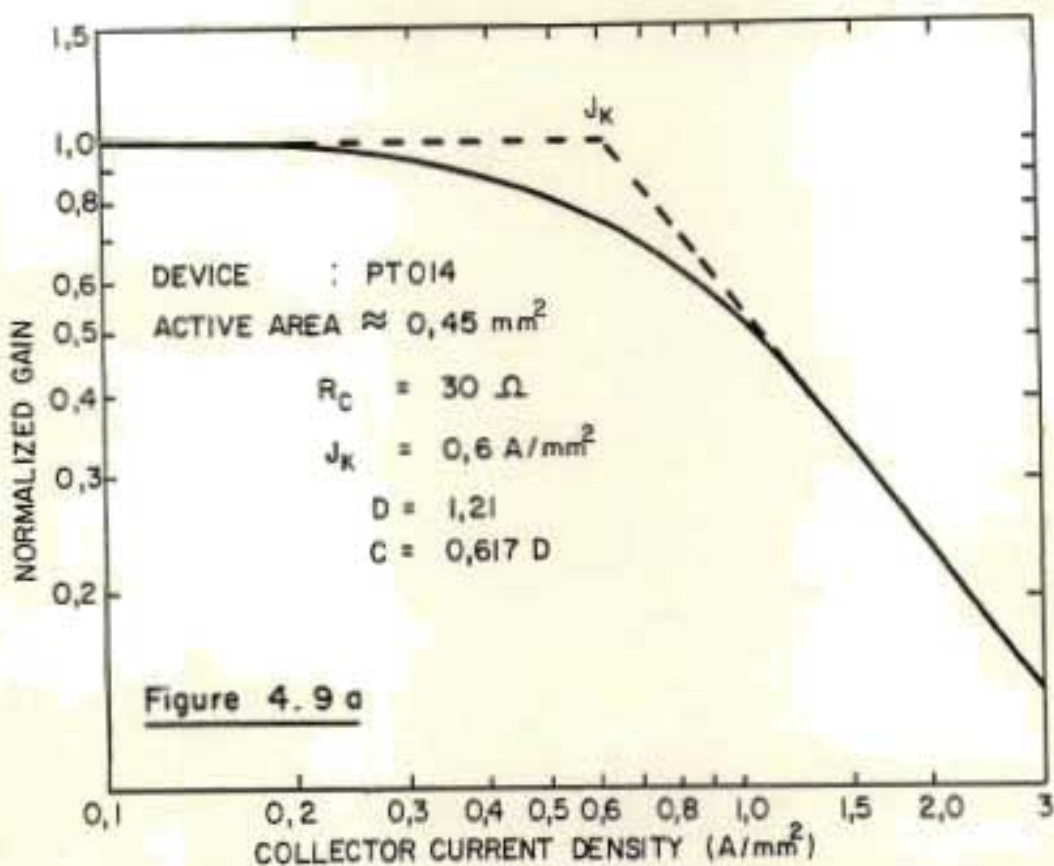
$$\ln(h_{FE}) = D \times \ln(J_C) + C \quad \dots\dots\dots 4.4E$$

where h_{FE} is the gain at collector current density J_C , and both D and C are constants for the device.

By extrapolating the linear portions of the graphs to meet unity normalized gain at a limiting collector current density termed the 'Knee Current Density' J_K it was possible to use equation 4.4E to calculate the gain of the transistor in the gain droop region for current densities exceeding J_K .

The Knee Current Density J_K , when divided by the corrected collector area of a transistor, is equivalent, in principle, to the Knee Current I_K used for approximating high-current injection in the modelling program 'SPICE'⁵¹. The two are equivalent only provided that the measurement is carried out in accordance with equation 4.4D above. This fact is easily overlooked when the knee current of a transistor is measured, and can lead to values of I_K which, when measured at an applied $V_{CB} = 0 \text{ V}$, are more than ten times too low for many high-voltage transistors. Reference to Figure 4.3 (page 120) shows how grossly misleading results can be arrived at if equation 4.4D is disregarded.

For computation, only the slope D is required, together with the Knee Current Density J_K such as shown in Figures 4.9a and 4.9b (page 132). A number of measurements that were made have shown that J_K (or I_K , if the active area of the the device is not known) may be found using $h_{FE} = 0,7h_{FEM}$ measured at a collector voltage level that is in accordance with equation 4.4D.



LINEAR APPROXIMATION FOR GAIN DROOP AT HIGH-INJECTION LEVELS

4.4.4.2 Dependence of the 'Knee Current Density' on process and layout

A comparison of Figures 4.9a and 4.9b (page 132) for the PT014 and the PT018 output stages respectively, reveals that, despite the considerable differences in layout and epitaxial layer thickness and resistivity, the knee current densities are very similar, whereas the slopes of the gain fall-off characteristics differ greatly. This behaviour was also confirmed with medium-power, high-voltage devices from other manufacturers. For the purposes of the computations described later in this chapter, default values of $J_K = 0,65 \text{ A/mm}^2$ and $D = 2$ were used, so that direct comparison with measurements on PT018 devices was possible.

4.4.5 Temperature correction for Model 2

The temperature dependence of h_{FEM} , R_C , R_{QS} and PC was investigated, and methods for temperature compensation of these parameters are presented in this section.

When measured in the normal operating region (region 3 of Model 2) the gains of a number of transistors increased with temperature, with a linear coefficient of about $5 \times 10^{-3}/^\circ\text{C}$, as may be seen in Figure 4.10a (page 134). This behaviour was in accordance with the figure presented by Burger and Donovan³¹. A totally different state of affairs was encountered when gain was measured as a function of temperature with the devices operating in region 2, quasi-saturation. Figure 4.10b (page 134) shows that in this condition both negative and positive temperature coefficients may be encountered. For this reason it was important to consider all the key parameters introduced with Model 2, so that meaningful temperature corrections might be computed.

4.4.5.1 Temperature corrections for R_C , the theoretical aspects

If temperature-compensated gains were to be calculated, it was necessary to introduce a temperature correction factor to relate the collector resistance R_C and the quasi-saturation resistance R_{QS} to temperature. In this sub-section it is shown that a logarithmic correction factor is the most appropriate for these two parameters.

Figure 4.10a

Normalized gain as a function of temperature
 Devices operating in region 3: normal operation

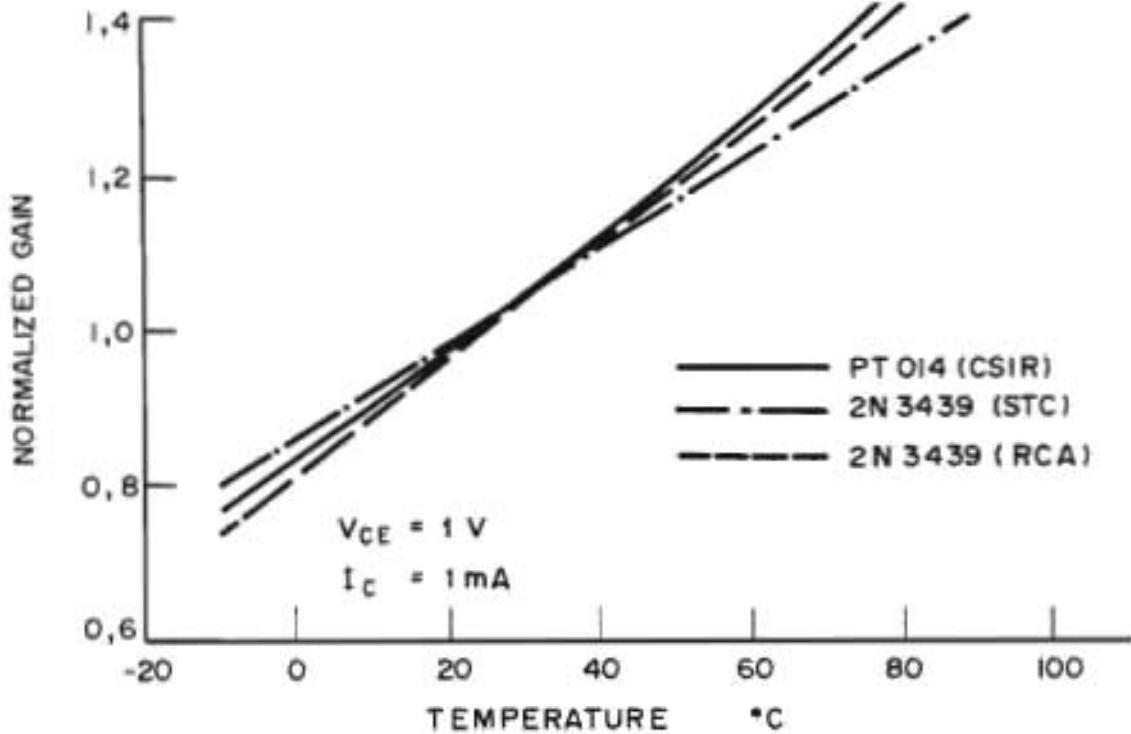
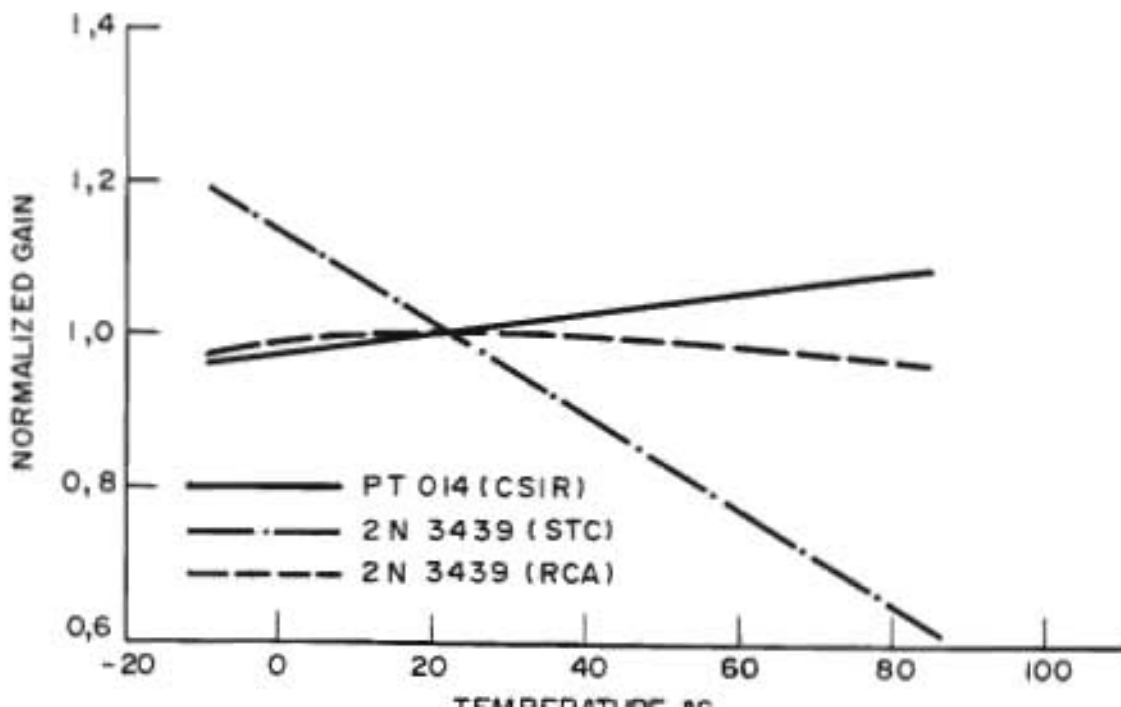


Figure 4.10b

Normalized gain as a function of temperature
 Devices operating in region 2 - quasi-saturation



Hamilton and Howard⁵² provided useful data on the thermal behaviour of the properties of bulk silicon. In their Figure 8.3a the conductivity of N-type silicon was plotted as a function of temperature over the range -50°C to 250°C . For silicon with a bulk resistivity of between 1 and 100 ohm.cm the resistivity increased with increasing temperature. Under these conditions a power series, shown in equation 8.9 of this reference, was simplified to a first-order approximation :

$$R(T) = R(T_0) \times \{1 + d \times (T - T_0)\} \quad \dots\dots\dots 4.4F$$

where

$R(T)$ is the silicon resistance at temperature T ;

$R(T_0)$ is the silicon resistance at temperature T_0 ; and

d is the temperature coefficient of resistance for the temperature range being considered.

This equation could be used to compute the collector resistance R_C of a high-voltage transistor. The main disadvantage of equation 4.4F was the fact that it was accurate over only a relatively small temperature range. Figure 8.5 in Hamilton and Howard⁵² shows that for an epitaxial resistor, the coefficient d drops by a factor of almost two over the temperature range 30°C to 130°C .

As an alternative approach, Martinelli et al.⁵³ have made use of an exponential equation of the form

$$R_T = R_{300} \times \text{Const} \times \exp(-E_a/kT) \quad \dots\dots\dots 4.4G$$

where

kT is the product of Boltzmann's constant and absolute temperature;

E_a is an empirically determined activation energy for the particular resistive property of the device;

R_T is the resistance at temperature T ;

R_{300} is the resistance at 300°K .

Equations 4.4F and 4.4G differ in form, but do express an increase in R_C with temperature, and in principle both could be used for computing R_C at a given temperature. No direct information could be deduced on the temperature dependence of the quasi-saturation resistance R_{QS} , so this relationship was investigated experimentally.

4.4.5.2 Evaluation of R_C , R_{QS} and PC as a function of temperature

As predicted in the section above, and in accordance with the physical model of Chudobiak⁴⁹, the value of R_C was found to increase with temperature. In the measurements made, the best linearity was obtained when the logarithms of both R_C and R_{QS} were plotted as a function of temperature. Figure 4.11 (page 137) shows the results for a PT014.

Here further confusion arose, as neither equation 4.4F nor 4.4G was equivalent to such a logarithmic function. The difference between the two theoretically derived equations and the experimentally derived relationship could be reconciled only if it was accepted that R_C over the temperature range 20 °C to 170 °C changed absolutely by a factor of only about two, and that under these conditions any of the three relationships would be sufficiently accurate.

Figure 4.12 (page 137) shows the process constant PC plotted as a function of temperature on a linear scale. A general downward trend with increased temperature is obvious.

4.4.5.3 Process Gain, h_{FEM} , as a function of temperature

Process Gain, h_{FEM} , was also temperature-dependent and could be compensated for using a linear equation similar to that given for collector resistance in equation 4.4F. Two main precautions were observed in making measurements for the temperature coefficient: first, it was necessary to ensure that the transistor was operating at a collector current close to the value for peak current gain, and secondly the collector-emitter voltage was set to a value slightly above the knee voltage V_K , using equation 4.4D. In practice the measured temperature coefficients did not differ markedly from the figures of $5 \times 10^{-3}/^{\circ}\text{C}$ given by Burger and Donovan³¹, and $8 \times 10^{-3}/^{\circ}\text{C}$ given by Hamilton and Howard⁵².

Figure 4.11
 R_{OS} and R_C vs temperature

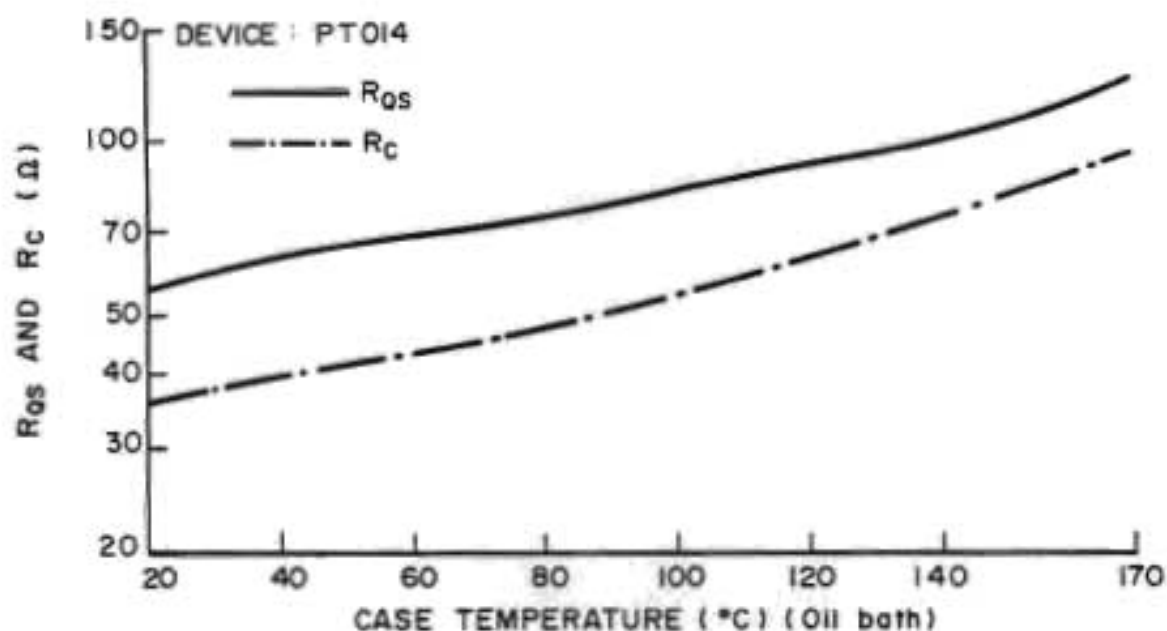
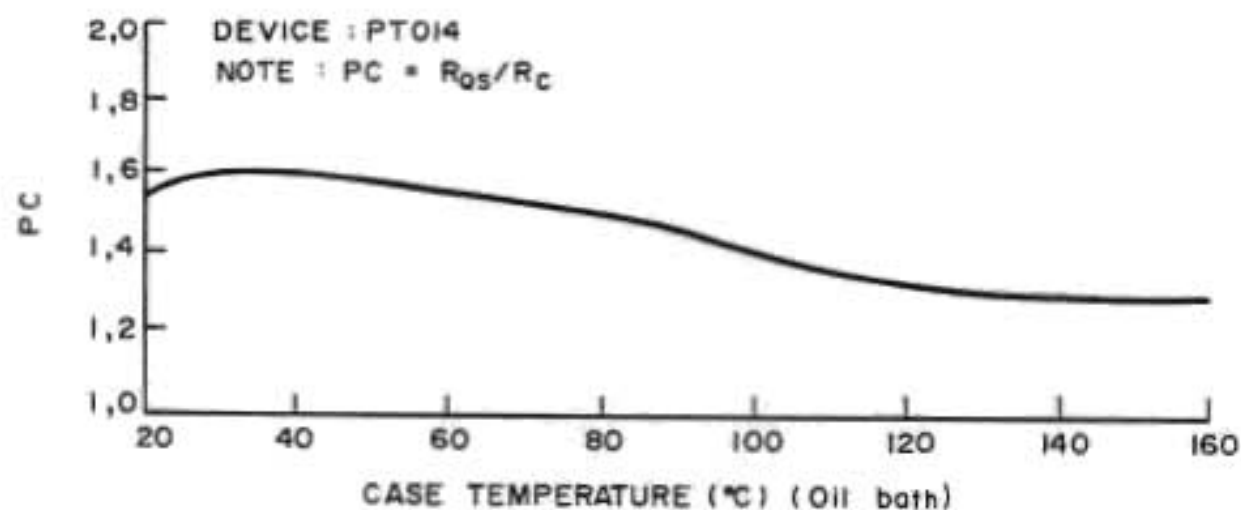


Figure 4.12
 Process Constant (PC) vs temperature



4.5 NUMERICAL SIMULATION USING MODEL 2

Model 2 as also the associated equations derived in Section 4.4, lent themselves to numerical simulation. Figure 4.13 (page 139) shows a flow diagram of the computer program written to calculate the collector current of a transistor operating in any of the three regions described, and the FORTRAN listing is presented in Appendix 4.1 (page 247).

4.5.1 Simulation of the output stage of the PT018 transistor

As an example of the use of the numerical model, the collector characteristics of the output stage of a PT018 transistor were simulated using the parameters as listed in Appendix 4.2 (page 248), and the results were plotted as shown in Figure 4.14a (page 140). The results of the program were in accordance with Model 2 and in addition, gain crowding at higher-injection levels may be seen. Figure 4.14b (page 140) shows how numerical smoothing of the data used for Figure 4.14a produced a set of collector characteristic curves that compared well with actual measurements made on the output stage of a PT018, shown by dotted lines.

4.5.2 Temperature effects

To ensure that the numerical model handled variations in temperature adequately, measurements were made on a PT014 transistor at 25 °C and 125 °C, and the measured collector current curves are presented in Figure 4.15 (page 141) together with the curves computed from data for the PT014 given in Appendix 4.2 (page 248). Clearly the numerical model provides data that are sufficiently accurate for the majority of applications.

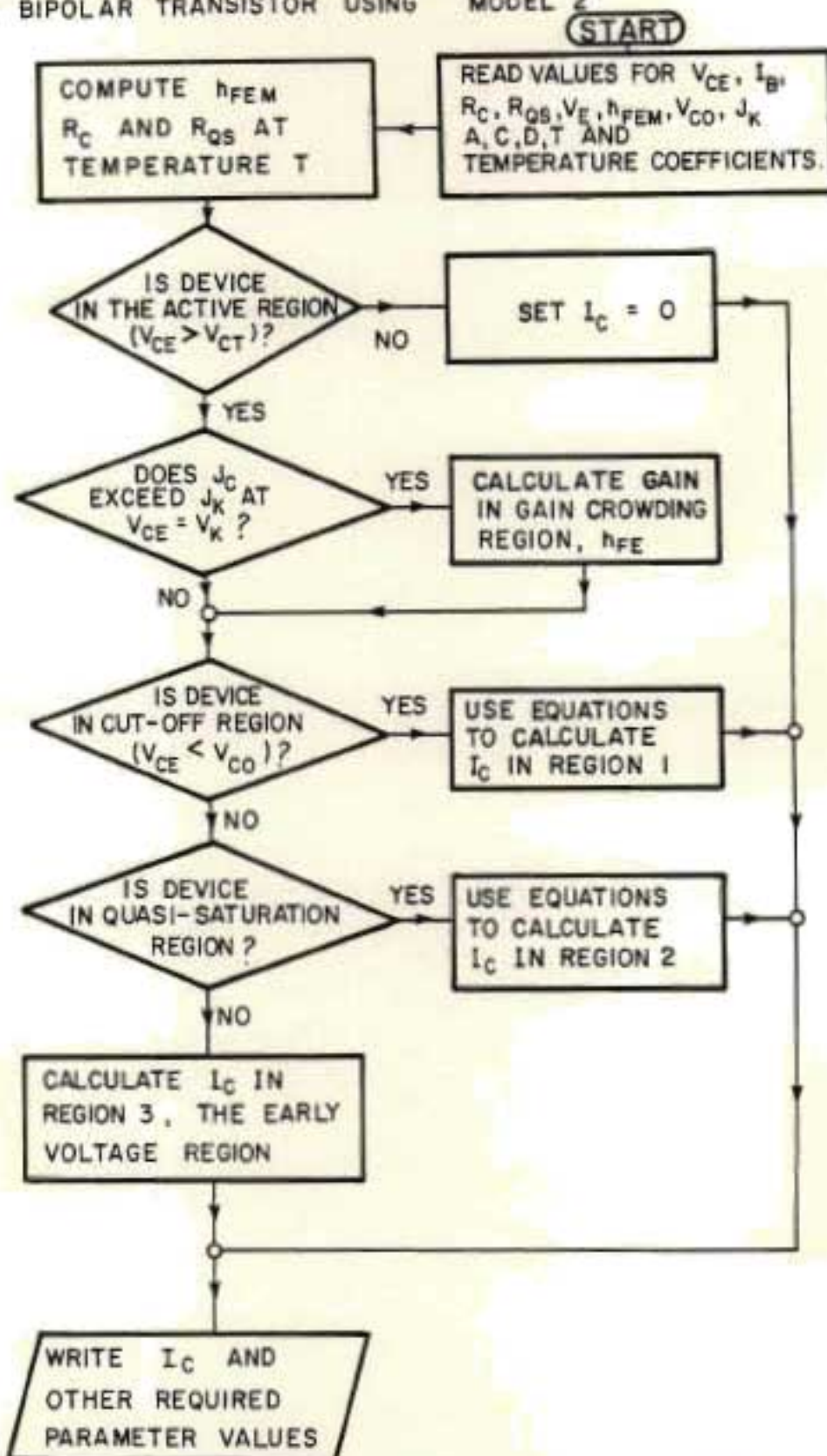
4.5.3 Merits of Model 2

Model 2 was set up with a specific objective in mind, viz that of modelling quasi-saturation effects in medium-power, high-voltage transistors in order to predict the DC operating conditions. Considerable success with this aim was achieved, as detailed in the following list.

(a) Model 2 had none of the shortcomings of Model 1, as listed in Section

FIGURE 4.13

FLOW DIAGRAM OF A COMPUTER PROGRAM TO CALCULATE THE COLLECTOR CURRENT OF A BIPOLAR TRANSISTOR USING 'MODEL 2'



NOTE: EQUATIONS 4.4A, 4.4B, 4.4C AND 4.4E WERE USED TOGETHER WITH A LINEAR TEMPERATURE COEFFICIENT FOR h_{FEM} AND A LOGARITHMIC TEMPERATURE COEFFICIENT FOR R_C AND R_{QS} .

FIGURE 4.14a

MODEL 2 SIMULATION OF THE OUTPUT STAGE OF A PTO18 INTEGRATED DARLINGTON WITH CORRECTION FOR HIGH-INJECTION EFFECTS.

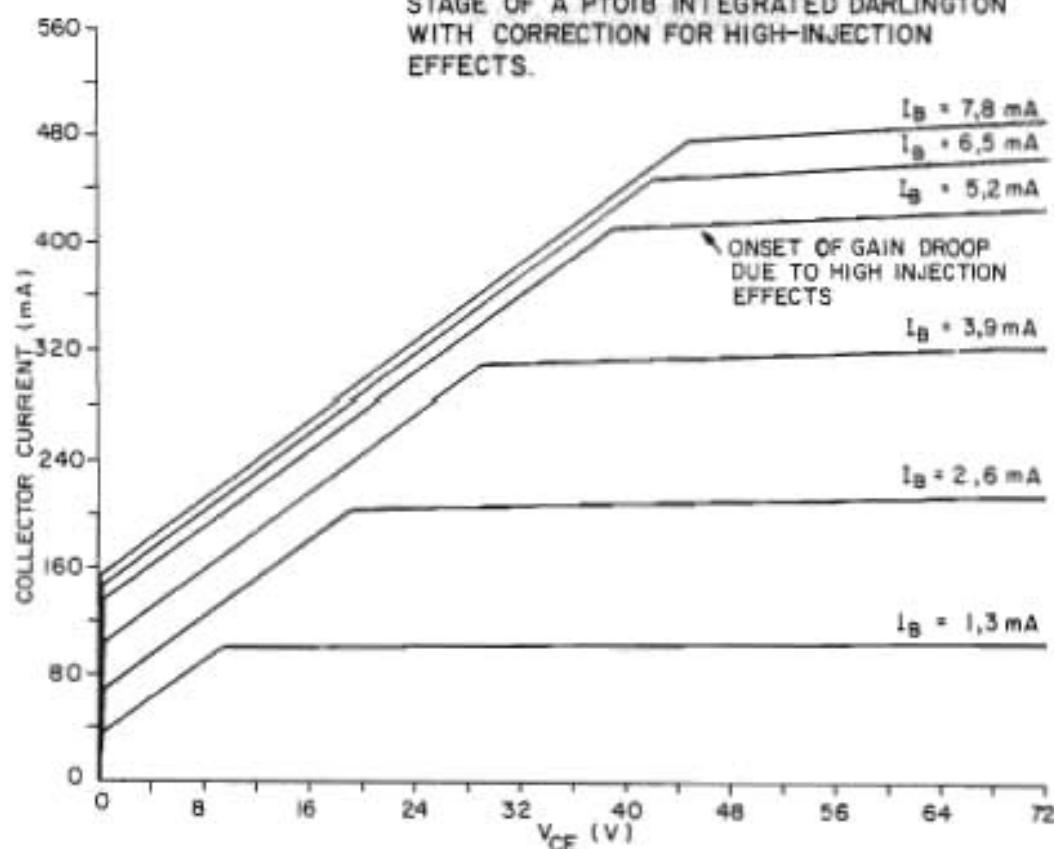
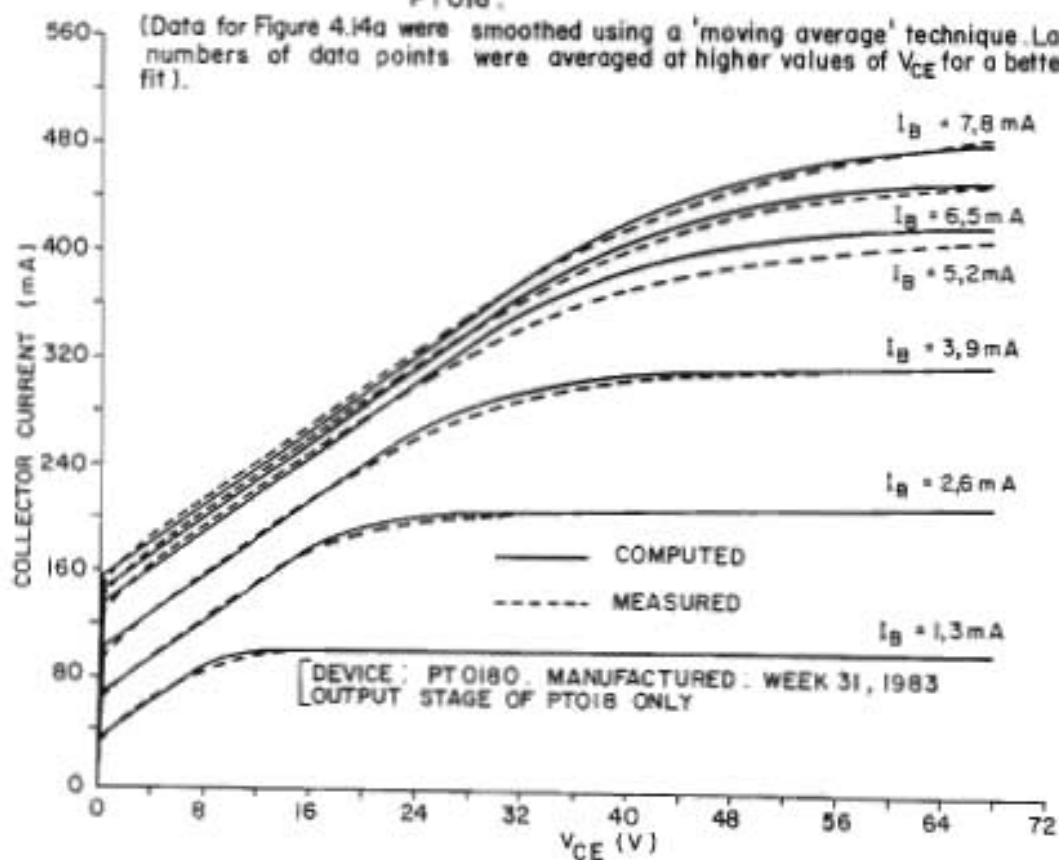


FIGURE 4.14b

SMOOTHED DATA FROM 'MODEL 2' AND ACTUAL MEASUREMENTS MADE ON THE OUTPUT STAGE OF A PTO18.

(Data for Figure 4.14a were smoothed using a 'moving average' technique. Larger numbers of data points were averaged at higher values of V_{CE} for a better fit).



Computation constants

$$V_{CT} = kT/q$$

$$V_{CO} = 200 \text{ mV}$$

$$V_{BE} = 1000 \text{ mV}$$

$$h_{FEM} = 77$$

$$R_C = 95 \Omega$$

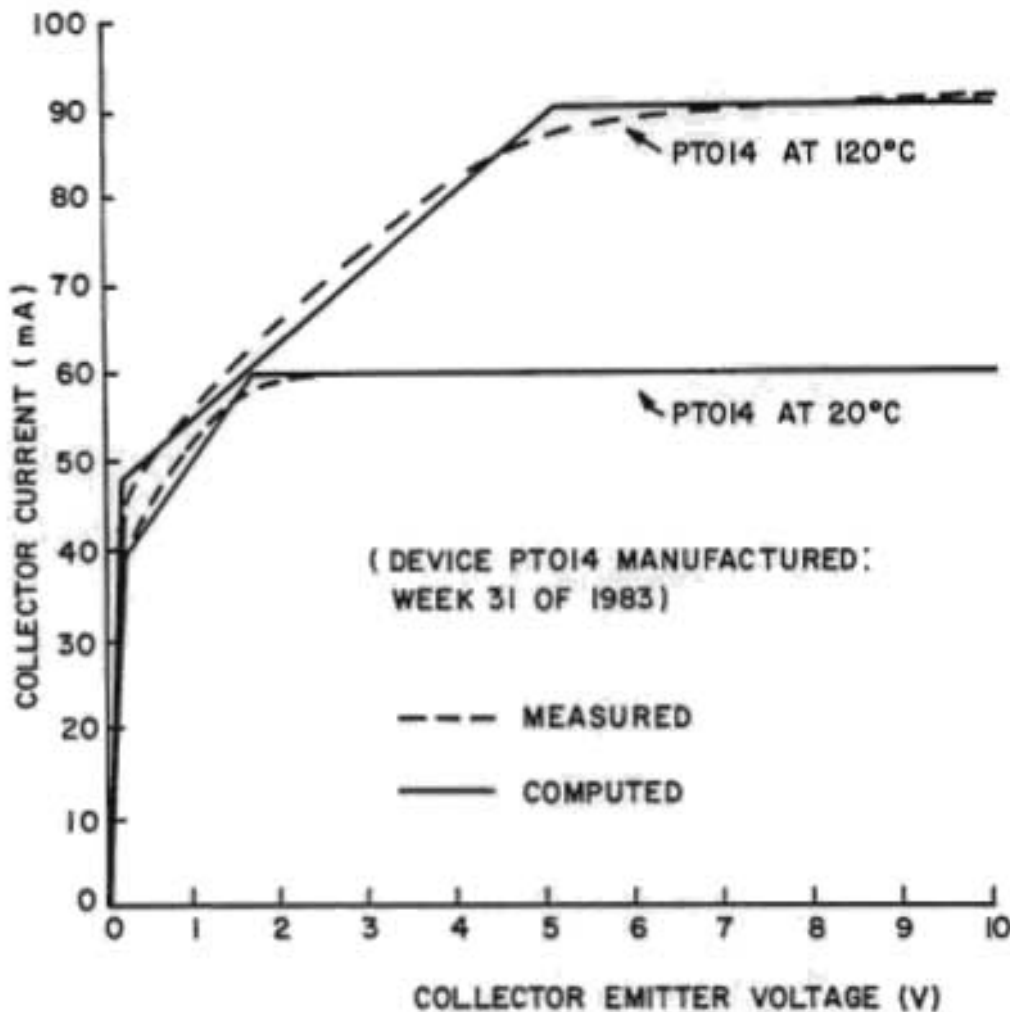
For high injection:

(See page 131)

$$A_{\text{res}} = 0,6 \text{ mm}^2$$

$$J_{C(\text{CRIT})} = 0,65 \text{ A/mm}^2$$

Figure 4.15 Saturation as a function of temperature for a PTO14 computed using Model 2.



COMPUTATION CONSTANTS:

1. MODEL 2 CONSTANTS

$$V_{CT} = kT/q$$

$$V_{CO} = 200 \text{ mV}$$

$$R_C = 28 \Omega$$

$$R_{QS} = 70 \Omega$$

$$h_{FEM} = 120$$

$$I_B = 0,5 \text{ mA}$$

$$T = 20^\circ \text{C}$$

$$V_E = 10^3 \text{ V}$$

2. TEMPERATURE CORRECTION CONSTANTS

$$h_{FEM}(T_1) = h_{FEM}(1 + K_1 \Delta T)$$

$$K_1 = 5 \times 10^{-3} / ^\circ \text{C}$$

$$R_C(T_1) = R_C \exp(K_2 \Delta T)$$

$$K_2 = 7 \times 10^{-3} / ^\circ \text{C}$$

$$R_{QS}(T_1) = R_{QS} \exp(K_3 \Delta T)$$

$$K_3 = 5 \times 10^{-3} / ^\circ \text{C}$$

$$T_1 = 120^\circ \text{C}$$

$$\Delta T = T_1 - T = 100^\circ \text{C}$$

4.3.2 (page 121) except that the physical basis might still be argued. Experimental results from a wide range of tests on NPN transistors have shown this to be a readily usable and sufficiently accurate model.

- (b) Only two parameters, viz R_C and R_{QS} , both of which are easily measured, were required uniquely to define quasi-saturation operation of a transistor.
- (c) The new parameters V_{CO} , the cut-off voltage, and V_{CT} , the conduction threshold voltage, required to characterize operation in the collector cut-off region, were both found to be virtually constant, so that default values gave good accuracy.
- (d) Although the model was a straight-line approximation, it yielded accurate results and, indeed, as will be seen when the modelling of the integrated Darlington transistor is described, the linear nature of the model has merit, as transitions between the operating regions of transistors may be seen clearly, and this readily simplifies design optimization of a device.

The model has subsequently been shown to have far wider application, ranging from small low-voltage devices through high-voltage power devices to integrated devices such as the Darlington transistor. A detailed analysis of the Darlington transistor is given in Sections 4.6 and 4.7.

4.5.4 Limitations of Model 2

It has been found that the application of Model 2 has its limitations and caution should be exercised in applying the model to the cases listed below.

- (a) If Model 2 is used for the A.C. analysis of circuits, this will lead to incorrect results when distortion products are calculated, owing to the linear nature of the model. The problem would be particularly manifest when transitions from regions 1 to 2, and 2 to 3 are encountered. It should be noted here that the simulation program 'SPICE' was not blameless in this area either, as may be

seen from Figure 4.3 (page 120), showing only a small amount of rounding of the transition from the resistive saturation region to normal operation.

When Smithies^{5a}, used 'SPICE' to analyze a multi-frequency (MF) dial amplifier incorporating high-voltage transistors, it was found that the measured and predicted AC harmonic analyses did not agree at all well. This was doubtless the result of both poor modelling of saturation by 'SPICE', and the rather abrupt transition from saturation to normal operation predicted by this program.

Numerical shaping could be applied to the results from Model 2, as was shown in Figure 4.14b (page 140), but this would certainly, as a first move, entail computing the collector characteristics at a number of points surrounding the particular operating point. This computation would be a slow procedure in a sequential analysis of collector currents, as was performed for the MF dial, unless data from the computation of sequential points were re-used and an interpolation technique applied to round off the transitions.

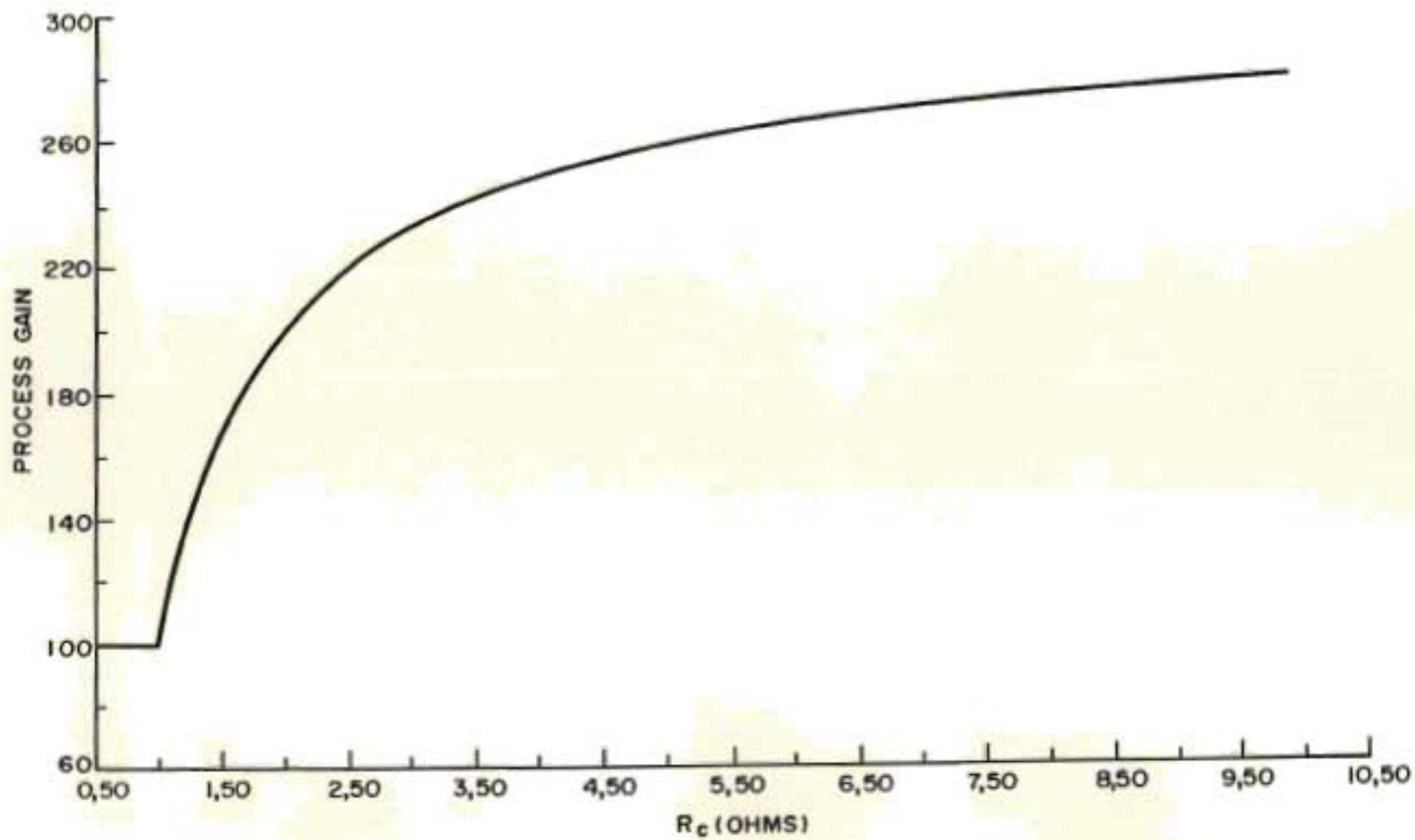
- (b) If no correction for high-injection levels is applied, the use of Model 2 has an arithmetical limitation that must be guarded against, and which is described below.

The limitation was encountered when it was attempted to use Model 2 to minimize the area of a device that should meet given operating conditions in quasi-saturation. Figure 4.16 (page 144) shows a plot of h_{FEM} vs R_C for a hypothetical transistor with a process constant PC of 1.5, a base drive of 10 mA, $V_{CE} = 1$ V and $I_C = 1$ A. It is seen that initially as R_C increases, the increase in h_{FEM} necessary to yield the required collector current is also large. The curve, however, flattens out, indicating an unrealistic condition of virtually no increase in required process gain to meet the operating conditions for increasing values of R_C .

Although the limitation mentioned did not manifest itself in computations of collector current as a function collector-emitter voltage for the values of gain and current density that were used in the design of both the PT014 and PT018, it will be seen in the detailed analyses of the PT018

Figure 4.16

Process Gain vs R_c



that follow in Sections 4.6 and 4.7, that the incorporation of a correction for high-injection levels adequately compensated for this shortcoming in the basic model.

4.5.5 Possible wider application of Model 2

In the case of a large variety of low to medium-voltage devices covering the whole power spectrum, the onset of high-injection effects may almost coincide with the onset of quasi-saturation, and indeed gain crowding due to high-injection effects might be greater. The application of Model 2 has not as yet been thoroughly pursued for these conditions and further investigation is required to determine its full scope. However, high-resistivity silicon epitaxial wafers may be procured with ease, and the author has noted that the collector-emitter breakdown voltage limits specified for modern transistors are regularly exceeded, often by as much as a factor of two. In these cases the probability of a significant modification to the saturation performance of a device owing to quasi-saturation should not be overlooked, and use of Model 2 would make it possible to predict operating conditions more accurately.

4.6 MODELLING THE INTEGRATED DARLINGTON TRANSISTOR WITH 'MODEL 2'

In this section is described the very successful application of Model 2 to a design verification of the PT018, it being found that the design of the device was well optimized.

4.6.1 Precedents in designing Darlington transistors

A comprehensive analysis of Darlington transistor design was published by Wheatley and Einthoven⁵⁵ in their classic paper on how the area of multi-stage Darlington power transistors should be proportioned. That this paper is of great value to the designer of low-voltage, high-power devices is undisputed, but the analysis presented was general in nature and fall-off in gain was dealt with only in terms of the drop that occurs at high emitter-injection levels. Collector effects leading to quasi-saturation operation were not considered. In addition, a number of parameters introduced in this publication would not be available to a circuit designer, nor would they be of interest.

4.6.2 Background information for modelling the PT018 using Model 2

A cost-effective design for the PT018 Darlington transistor was achieved by minimizing the area of the device by operating the output stage in quasi-saturation at the specified upper current limits. For the operating conditions encountered, the active area of the device was such that operation was always below the knee current I_K . Armed with Model 2, it was possible to simulate a wider range of conditions than those considered in Chapter 3, but in order that a design verification exercise could be carried out on the PT018, it was first necessary to confirm or establish the information listed in the following sub-sections.

4.6.2.1 Proportionality of collector resistance to active device area

The collector resistance R_C should be proportional to the active area of the device. Measurements made on both discrete high-voltage devices and the driver and output stages of integrated Darlington transistors, all fabricated on the same wafer, have shown that if the correction for active area given in equation 2.6B (page 37) is applied, the measured and predicted values of collector resistance are in close agreement. This observation covered a range of devices that had corrected areas differing by a factor of up to nine.

4.6.2.2 Process constant PC to be independent of device area and layout

The process constant PC, which is equal to the ratio R_{QS}/R_C , should be a constant independent of the active area and geometry of the device. It could be shown that this was the case for both the prototype and production versions of the integrated Darlington and the adjacent discrete drop-in test transistors, but it should be borne in mind that planar epitaxial structures had been used, where the N+ substrate served as the collector contact. Integrated circuit transistor layouts, where there is a passive element of collector resistance dependent on the layout of the transistor, could easily show a layout-dependent value of PC.

4.6.2.3 The base-emitter voltage of the output stage of the Darlington

The value of the base-emitter voltage (V_{BE2}) of the output device had to be determined in order that the collector-emitter voltage of the driver transistor (V_{CE1}) could be calculated. The relationship between V_{BE2} and the base current of the output stage, I_{B2} , is derived in Appendix 4.3 (page 250) and is

$$V_{BE2} = kT/q \times \ln(I_{B2}) + R_{B2} \times I_{B2} + K \quad \dots\dots\dots 4.6A$$

where

- k is Boltzmann's constant;
- K is a constant for the output device when operating with collector current flowing;
- q is the electronic charge;
- R_{B2} is the passive base resistance of the output stage;
- T is the absolute temperature.

In practice it was found that equation 4.6A gave a better fit to measured V_{BE2} characteristics if a factor ℓ was included as $kT/\ell q$. The value of ℓ was typically about 0,8 for a transistor operating in the active region. (Sukheeja⁵⁶ has reported the use of a constant such as ℓ for the case of diodes or the emitter-base junctions of transistors operating with no collector current. The principle of inclusion of the constant ℓ into equation 4.6A has been found to be equally applicable in the calculation of the base-emitter voltage for an active transistor.)

In early measurements made on discrete devices exhibiting quasi-saturation, it was noted that with constant base current, the base-emitter voltage increased rapidly as the device passed through region 1 to region 2. In region 2 the base-emitter voltage varied only slightly, and then tended to approach a constant value only when the device reached normal operation in region 3. Values for K and R_{B2} that were used were measured at the transition to region 3. Nevertheless, agreement between measured and modelled results for the PT018 was excellent, with collector-emitter voltages even as low as 1 V.

4.6.3 Simulation of the PT018 integrated Darlington transistor using Model 2

The equivalent circuit of the Darlington used in the simulation is shown in Figure 4.17 (page 149). It consists of two transistors with the same process constant PC and values of collector resistance that can be scaled according to the active areas of the devices. The scaling factor was the Area Ratio N' , the ratio of the active area of the output stage to the active area of the driver stage. As the devices were adjacent, the gains were identical. The computer program referred to in Section 4.5 was of immediate application in the computation of the collector current of the Darlington transistor.

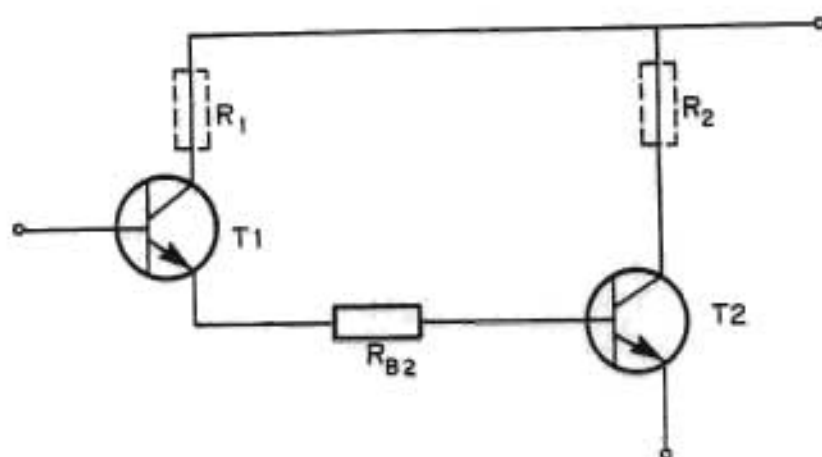
The only difficulty that arose in this simulation was in calculating V_{BE2} directly, using equation 4.6A (page 147). A regression technique was adopted, a rather low estimate of V_{BE2} (0,45V) being made in the first iteration to ensure that the driver was in the active region. With a given value of I_B and V_{CE} a first estimate was obtained of the driver emitter current I_{E1} . Using equation 4.6A a new value of V_{BE2} (and hence V_{CE1}) was obtained. This procedure was repeated until the change in V_{BE2} on successive iterations was less than 0,1 mV. For further iterations in the progress of the program it was possible to use as a starting value a better estimate of V_{BE2} , derived from earlier iterations. It was important that this regression should be carried out rapidly if program times were to be minimized. If large changes in V_{BE2} were allowed during the regression, then instability could occur. It was necessary to test for stability and to relax the change in V_{BE2} to a value small enough to ensure stability and yet provide rapid regression to an accurate value.

Once V_{BE2} had been established, it was a straightforward matter to calculate the operating conditions of the driver and output stages, and thus of the Darlington transistor as a whole.

The flow diagram of the program used to compute the collector current of the integrated Darlington transistor as a function of collector-emitter voltage is given in Figure 4.18 (page 150). The FORTRAN listing of the program is presented in Appendix 4.4 (page 251).

FIGURE 4.17

Simulation of the integrated Darlington transistor

EQUIVALENT CIRCUIT

T1 is the driver transistor.

T2 is the output transistor, having an area greater than that of the driver T1 by a factor N' .

R_2 represents the Model 2 parameters for the collector resistance of T2 (R_C) and the quasi-saturation resistance of T2 (R_{QS}).

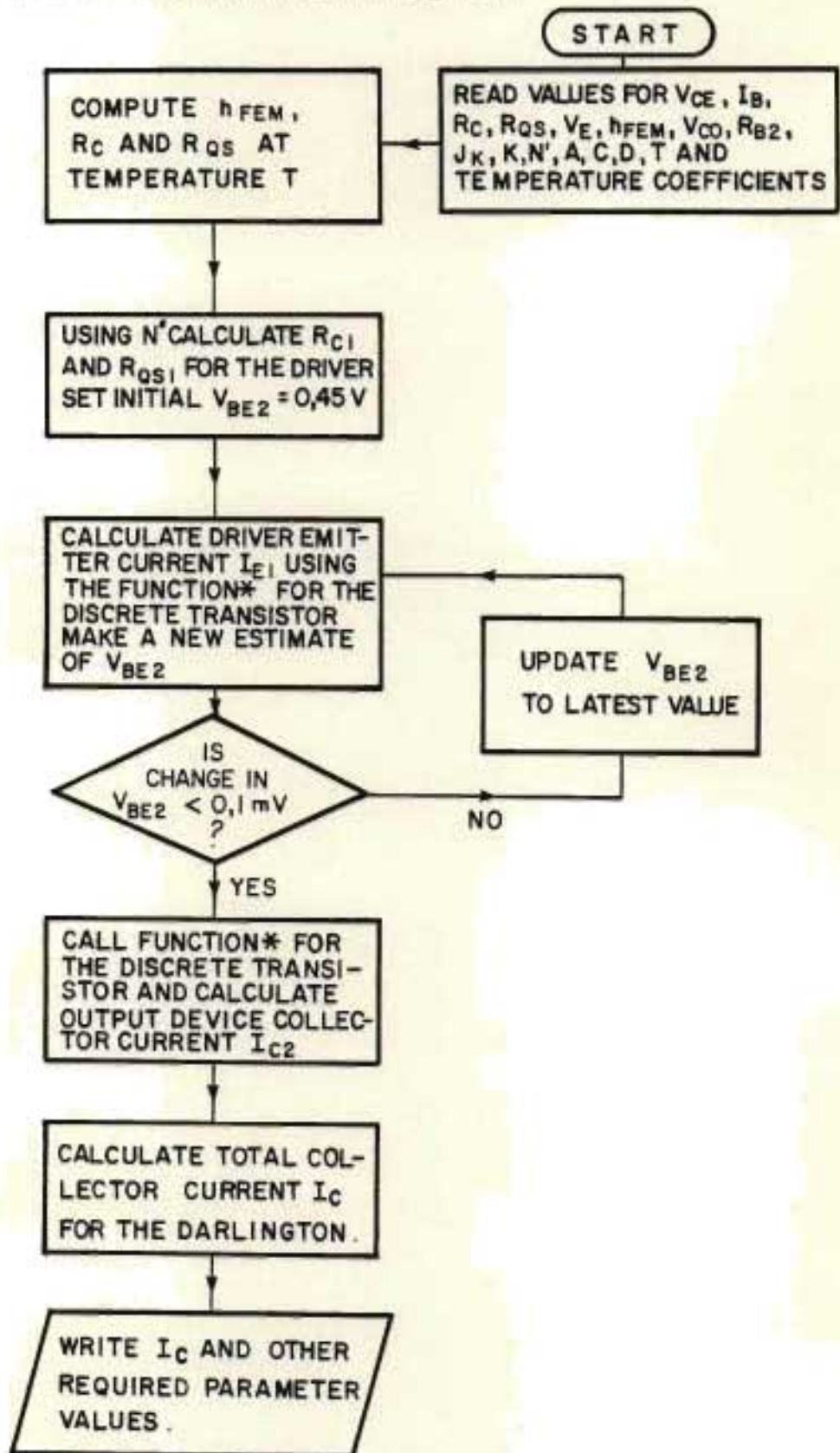
R_1 represents the scaled values of collector resistance and quasi-saturation resistance of the driver, T1. The values are $N' \times R_C$ and $N' \times R_{QS}$ respectively.

R_{B2} is the base resistance of T2, and the voltage drop across R_{B2} plus the forward emitter-base junction voltage of T2 are subtracted from the Darlington collector-emitter voltage to give the collector-emitter voltage of T1.

EACH TRANSISTOR STAGE IS MODELLED SEPARATELY USING
MODEL 2

FIGURE 4.18

FLOW DIAGRAM OF A COMPUTER PROGRAM TO CALCULATE THE COLLECTOR CURRENT OF AN INTEGRATED DARLINGTON TRANSISTOR.



* THE 'FUNCTION' IS A PROGRAM SIMILAR TO THAT IN FIGURE 4.13 FOR CALCULATING THE COLLECTOR CURRENT OF A BIPOLAR TRANSISTOR USING MODEL 2.

4.6.4 Computed and measured I_C vs V_{CE} characteristics of the PT018

To verify that it would provide the D.C. transfer characteristic of the PT018, the simulation program was run with the parameters listed in Appendix 4.2 (page 248). Figure 4.19 (page 152) shows the measured and computed curves of I_C vs V_{CE} . Agreement was better than 10 per cent over the range 0,8 V to 100 V, the upper limit that could be reached at the NEERI Laboratory before thermal effects caused large errors.

Later measurements by Smithies³⁹ and Parsley⁴⁰, on the O.N. transistor in the Disa telephone with surge tests of up to 350 V, using equipment for high-voltage transient testing at the Post Office Telegraphic Institute, gave measured collector currents that were in good agreement with those predicted by the model.

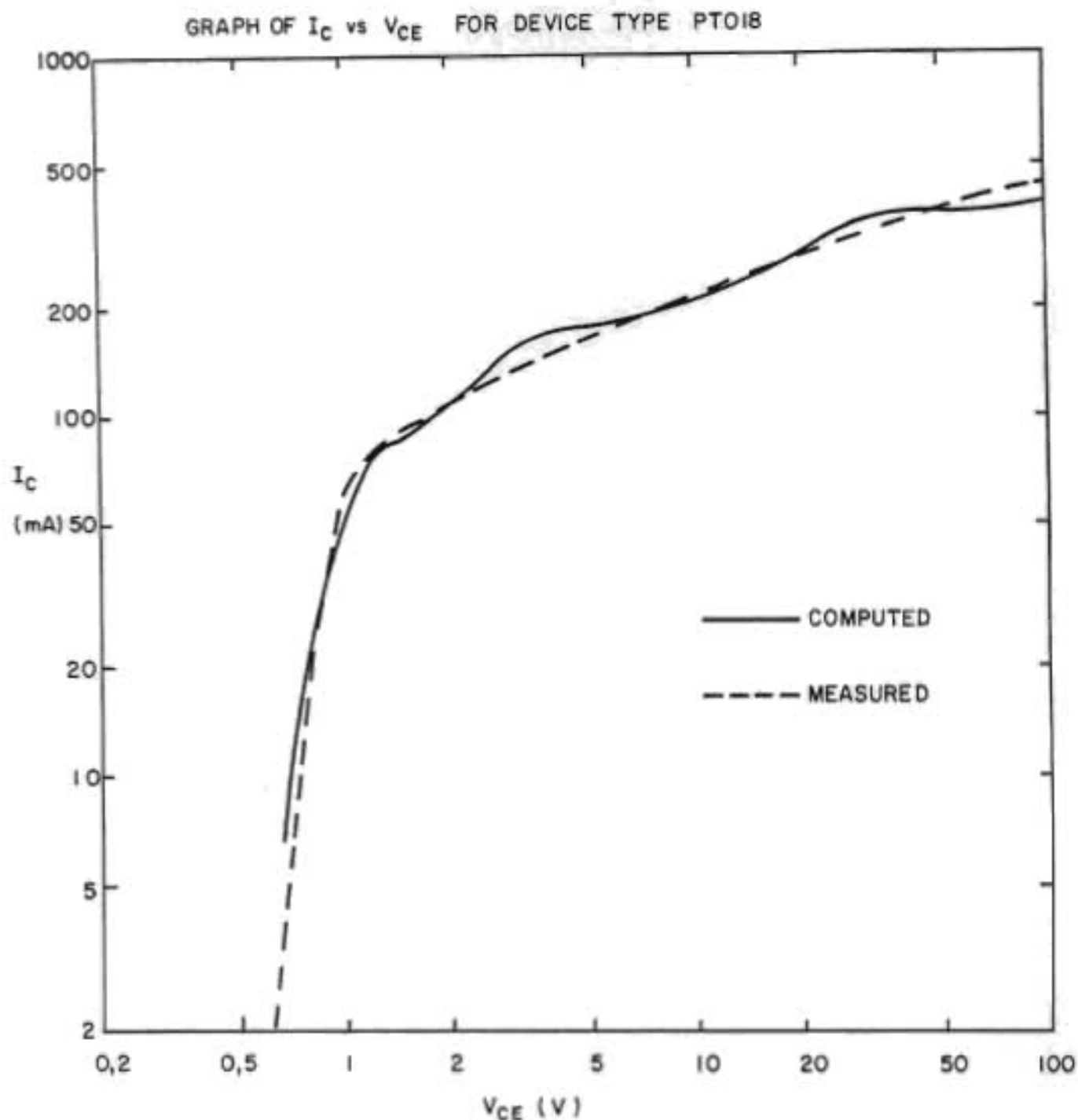
Model 2, initially developed to model saturation effects, was thus also able accurately to predict the transfer characteristics of the Darlington transistor over almost three decades of applied collector-emitter voltage, making it a useful tool in predicting currents that would be measured during transient overvoltage conditions.

The computed curve in Figure 4.19 (page 152) shows small irregular changes in the slope of the collector current curve over this wide range of voltages. It will be shown in Section 4.7.1 that this is a useful property of the model which makes it possible easily to identify the operating regions of both stages of the Darlington.

4.6.5 Use of Model 2 to minimize the area the Darlington transistor

Here the simulation program for calculating the collector current of a Darlington transistor was used together with a process constant PC of 1,5 and an area ratio N' of output to driver of 6, being the actual ratio used in the PT018. The value of h_{FEM} , or the 'Process Gain' as it was termed, was calculated as a function of the collector resistance of the output stage R_{C2} to obtain a value for the Darlington gain that would meet the O.N. and impulsing gain requirements for the IPB telephone, as listed in Table 3A (page 62).

Figure 4.19



MODEL: COMBINED 3 REGION FOR DARLINGTON USING 'MODEL 2'.

BASIC TRANSISTOR PARAMETERS MEASURED AND USED IN THE COMPUTATION:

$$R_C = 80 \Omega \quad R_{QS} = 120 \Omega$$

$$h_{FEM} = 68 \quad N' = 6$$

$$V_E = 1000 \text{ V}$$

BASE CURRENT = $69 \mu\text{A}$

Figures 4.20a and 4.20b (page 154) show the process gain as a function of collector resistance. Both these curves have the same basic form and there are five distinct segments as listed below.

- (a) The flattest segment of the curve, AB, corresponds to the condition where both the driver and output stage are in region 3, normal operation.
- (b) In segment BC where the process gain begins to rise fairly slowly, and the output stage is in region 2, quasi-saturation.
- (c) The third segment, CD, is that where the process gain rises even more rapidly owing to the driver moving into region 2, quasi-saturation.
- (d) For the fourth segment, DE, high-injection gain droop commences in the output stage, above the knee current density J_K , and further compounds the increase in required process gain.
- (f) For the fifth segment, EF, high-injection gain droop commences in the driver, resulting in the greatest increase in process gain.

In choosing an appropriate value of collector resistance, it was clear that the decision to operate the driver in region 3, normal operation, and the output stage in region 2, quasi-saturation, was a sound decision, as any attempt to put R_C above about 80 ohms would have had two consequences: firstly it would have been necessary to have had exceptionally good process control to meet both gain and breakdown requirements, and secondly the quasi-saturation resistance would have increased proportionately to collector resistance and materially added to the impedance of the telephone, to the detriment of transmission performance.

4.6.6 The PT018 shown to be an unexpectedly conservative design

The active area actually required was determined by using the upper limits for epitaxial layer resistivity and thickness given in Section 3.8.1 (page 95) and calculating the collector area, A_{out} , that was required to give $R_C = 80$ ohms, using the relationship

$$\begin{aligned} A_{out} &= 100 \times \{r_{epi} \times (t_{epi} - 8)\} / 80 = 100 \times (75 \times 62 / 80) \\ &= 0,582 \text{ mm}^2 \end{aligned}$$

Figure 4.20 a

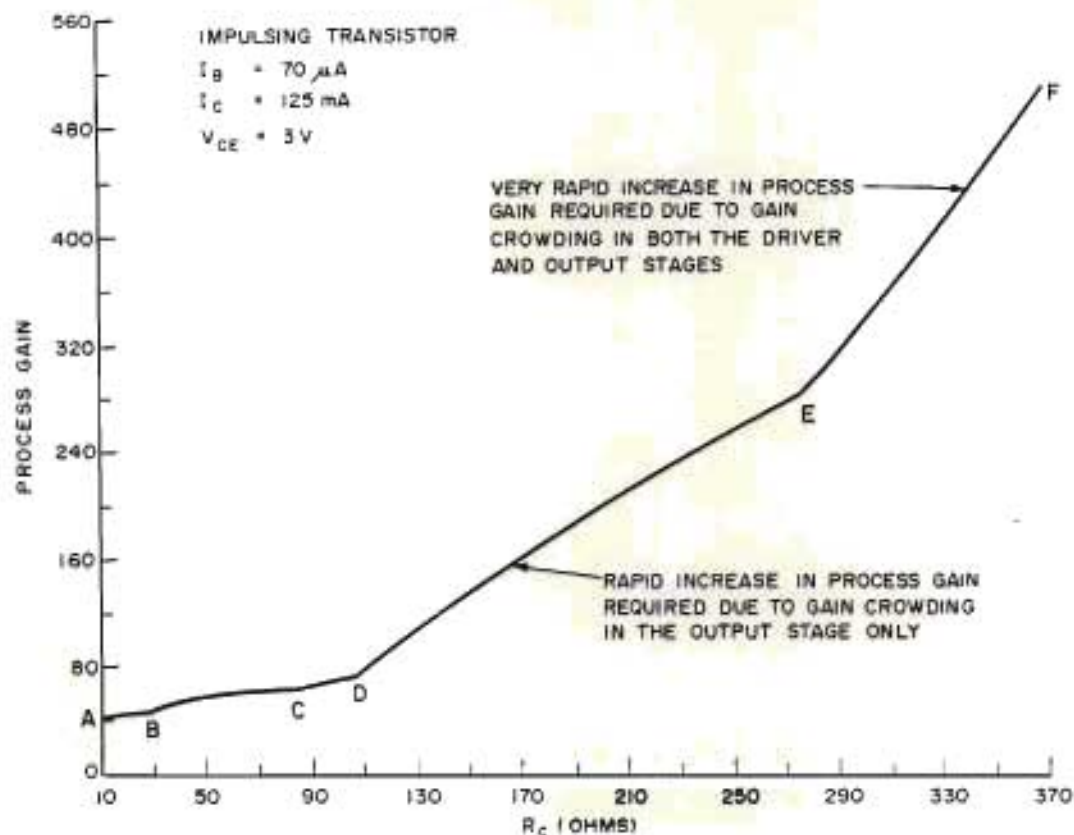
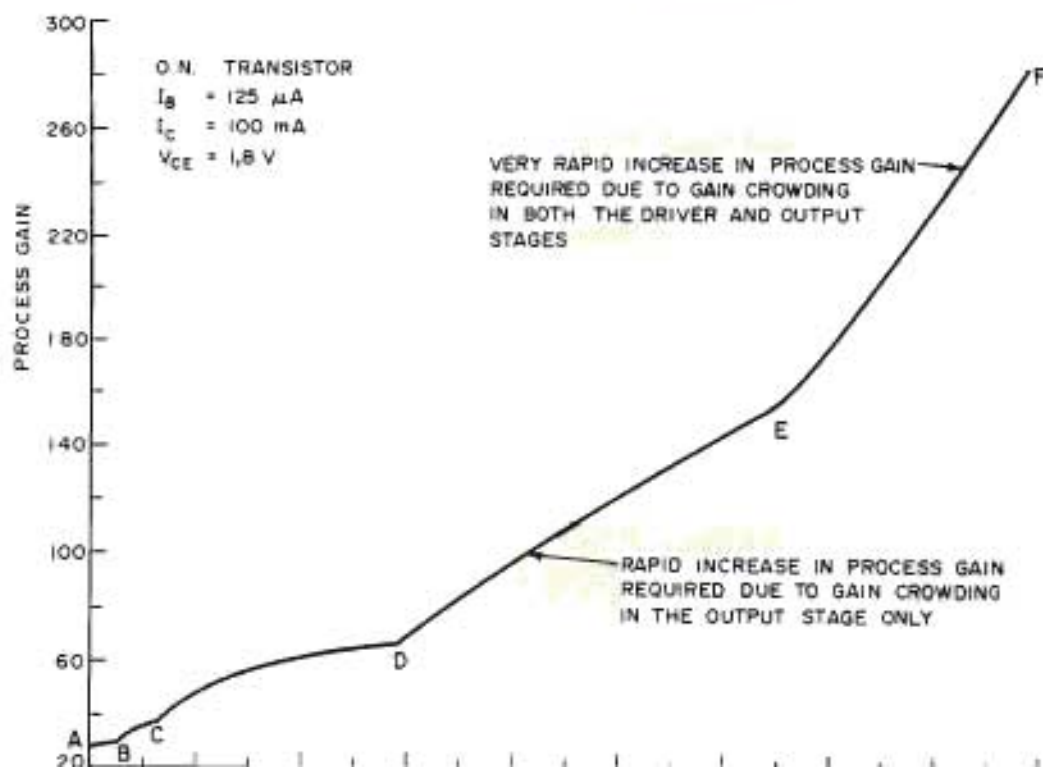
Darlington process gain vs R_C with the correction for high injection levels included

Figure 4.20 b

Darlington process gain vs R_C with the correction for high injection levels included

where $8 \mu\text{m}$ is the epitaxial layer thickness used in processing.

In calculating the area of the driver, it should be noted that the figures obtained from measurements of R_{C2} and R_{C1} , the collector resistances of the output and driver stages respectively, yielded a ratio of approximately 6 for R_{C2}/R_{C1} . Using $N' = 6$ the driver area should be :

$$A_{dr} = 0,097 \text{ mm}^2.$$

In Table 4A below, these computed areas are compared with the actual areas of the PT018, corrected using equation 2.6B (page 37).

Table 4A : Computed and measured active areas of the PT018

Output transistor PT018		Driver transistor PT018	
Area (mm^2)	Periphery (mm)	Area (mm^2)	Periphery (mm)
0,3393 [#]	8,43	0,0532 [#]	1,36
AS USED	Eqn 2.6B & $62 \mu\text{m}$ epi $A_{out} = 0,60 \text{ mm}^2$	Eqn 2.6B & $62 \mu\text{m}$ epi $A_{dr} = 0,095 \text{ mm}^2$	
SIMULATED	From 'Model 2' simulation $A_{out} = 0,582 \text{ mm}^2$	$A_{dr} = A_{out}/6$ $A_{dr} = 0,097 \text{ mm}^2$	

[#]The actual geometrical area of the emitters before correction.

The agreement is excellent between the predicted areas required for the PT018 and those areas that were used in the actual layout. A most important point to note is that in Section 3.8.2 (page 95) it was shown that the actual active area of the Darlington that could be used was less than that actually required, solely for economic reasons. The surprising finding from the simulation using Model 2 was that at a process gain of only 60, the area of the PT018 was sufficient to meet the saturation requirements at the upper limits for epitaxial resistivity and thickness. This was quite contrary to expectations, and the PT018 design was thus shown to be far more conservative than originally thought.

Measurements made during the production of the PT018 confirmed that a minimum process gain of 60 was required in order that the device should meet the impulsing gain condition, thus lending considerable weight to the validity of the model.

4.6.7 PT018 production controls derived from the simulation

During production it was found that the most critical step was that of 'targetting' the gain of the Darlington transistors accurately, using two 'pilot' wafers to obtain the emitter diffusion time. Only after this step had been successfully completed could the balance of the batch pass through emitter diffusion. A major difficulty was experienced in attempts to measure the gains of the Darlington transistors accurately at the specified 3 V at 125 mA and 1,8 V at 100 mA. This could not be done with the simple probing equipment in the diffusion area, as tests at these low voltages required 'Kelvin' probes, where the current is forced in through two probes and voltages are sensed on another two. In addition the operation had to be carried out in darkness, because under ambient lighting conditions large photocurrents were produced in the high-gain Darlington transistors.

To solve this problem it was decided to measure the process gain of the output stage of the Darlington by itself. This was easily achieved with the simple probing equipment available. A lower limit of 65 for the process gain was used, derived using Model 2 with a small safety margin added. Measurements were made outside the quasi-saturation region at $V_{CE} = 10$ V and $I_C = 60$ mA. Under these conditions it was found that no special precautions were required with the probes used, and that it was not necessary to keep the device in total darkness.

In Section 3.8.1 it was estimated that, in production, the process gain would range between 100 and 300. This, in view of the results from the modelling, was revised to a range of 65 to 200. The net effect was that the peak in the distribution of $V_{CEO(SUS)}$ values moved from the anticipated value of 400 V to approximately 450 V, as may be seen in the distribution given in Figure 3.19 (page 102).

4.6.8 Discussion of the PT018 design verification exercise

The exercise has shown conclusively that the use of Model 2 coupled with information on the epitaxial layer specification, originally derived from Figure 2.13 (page 42), has not only verified the Darlington design, but has yielded results that were far closer to the data obtained in production than the initial estimates made during the design of the Darlington.

It still remained important to establish that N' , the ratio of the active area of the output stage to that of the driver, had been optimized in the PT018 design. From Figure 4.20b (page 154), computed using the more stringent requirements for gain for the impulsing condition, it can be seen that with a maximum collector resistance of 80 ohms the driver is only just moving into the quasi-saturation region. Should N' be increased beyond the value of 6 that was used, it is certain that the performance of the Darlington would suffer, as the net gain of the driver would drop. Conversely, if N' were decreased significantly by increasing the area of the driver, this would also yield little benefit, as the Darlington would increase in overall size but would not offer enhanced performance. The choice of $N' = 6$ thus appeared to have been extremely well founded.

To conclude Section 4.6, it may be confidently stated that the optimization of the PT018 design required, as essential inputs, an accurate knowledge of both the in-circuit operating conditions and a well characterized process technology. Lack of information in either direction would have led to the development of a device that would either not have met the electrical requirements consistently or have been wasteful of silicon area. Both cases would have proved financially embarrassing.

Certainly, it is now clear that the only way successfully to design a Darlington is first to undertake a complete evaluation of the process(es) available, and follow this evaluation by a thorough device design exercise, using Model 2 as an aid.

4.7 MORE GENERAL APPLICATION OF MODEL 2 TO DARLINGTON DESIGN

The purpose of this section is to demonstrate how Model 2 may be used in a more general sense in the design of Darlington transistors. To offer full generality would present a task of enormous proportions, thus parameters relating to the well-characterized PT018 integrated Darlington were used where required, and it is essential to appreciate that the computed curves refer specifically to the production process and layout methods used for the PT018, no unjustified and possibly misleading generalizations being made.

In fact, from the data presented, it is clear that as far too many variables can play an important role in Darlington transistor design, the use of a general simplified approach is precluded. To reinforce the view expressed at the end of Section 4.6 it must be stated that any design exercise for a Darlington should be carried out in the full knowledge of the intended application(s) together with a knowledge of the production process characteristics.

In all cases presented in this section, the approximation for high-injection levels was included in the computer programs used. If this were not done, unrealistic results stemming from impossibly high collector currents would have grossly distorted the results, particularly where optimization of current-handling ability was computed. All the values of the parameters used in the computations refer specifically to the PT018, and are listed in Appendix 4.2 (page 248). Case-specific parameter values are given on the graphs.

From the examples given, use of the programs developed should make it an easy matter to analyze other transistor designs and applications, using the techniques described in this section. The parameters required for the simulations may be readily measured with standard, unsophisticated laboratory equipment.

4.7.1 I_C vs V_{CE} characteristics

Using constants given in Appendix 4.2 (page 248), I_C was computed as a function of V_{CE} for $I_B = 125 \mu A$. As a contrast to Figure 4.19 (page 152),

graphs were drawn of the gains of the driver stage, output stage and the device as a whole, and these curves are presented in Figure 4.21 (page 160). This was done in order to gain a better understanding of the mode of operation of each stage of the Darlington. (It should be noted that owing to the wide range of operating voltages and currents presented, logarithmic scales were used on the abscissa and ordinate. These scales obscure the linear nature of the curves in the operating regions encountered in Model 2.)

A discussion of the regions of operation of both transistor stages follows.

(a) Driver transistor operating regions

The driver passes predictably from V_{CT} , the conduction threshold voltage occurring at a Darlington collector-emitter voltage V_{CE} of about 0,7 V, into region 1, the cut-off region. At a V_{CE} of about 1 V the driver passes into region 2, quasi-saturation, and at a V_{CE} of 3 V reaches region 3, normal operation.

(b) Output transistor operating regions

Owing to the very low collector current the output device, contrary to expectation, commences operation in region 3, normal operation, and the gain drops rapidly with increased collector current as the device moves into region 2, quasi-saturation. The output transistor returns to operation in region 3 only when the collector-emitter voltage exceeds about 30 V.

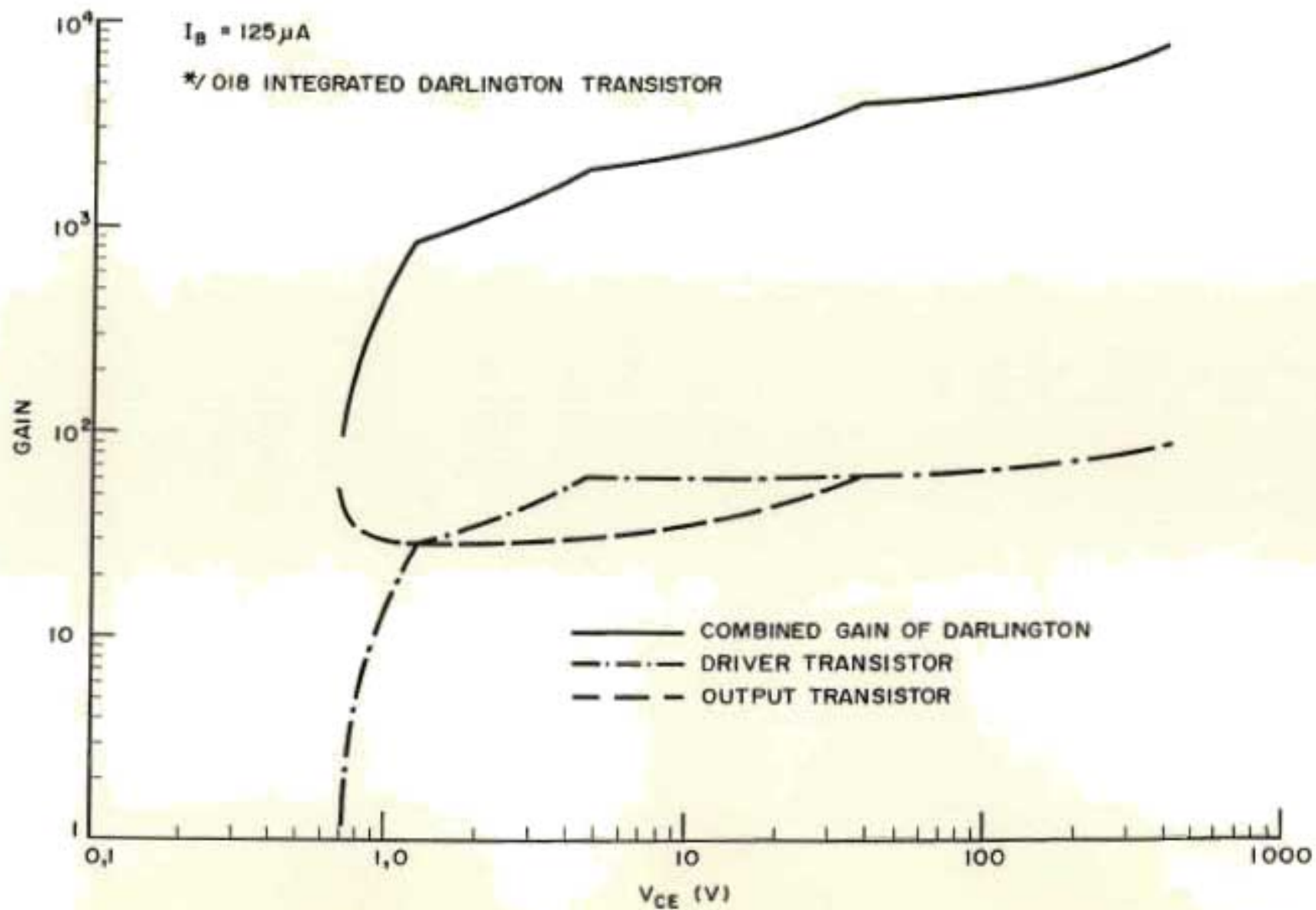
(c) The combined curve for the Darlington gain

Four regions of operation are shown, and these are

- cut-off (driver transistor in region 1);
- driver transistor in region 2 and output transistor moving from region 3 to region 2;
- driver transistor in region 3 and output transistor in region 2;
- both devices operating in region 3; in this case it is worth while noting that the measured Early voltage of a two-stage Darlington transistor is just half that of a single transistor stage.

Figure 4.21

Combined plot of component and product gain figures



4.7.2 Effects of the base resistance R_{B2}

In this instance the collector current of the Darlington transistor with $I_B = 125 \mu\text{A}$ was computed for different values of R_{B2} and plotted as a function of V_{CE} . The results are given in Figure 4.22 (page 162), from which it is clear that the value of R_{B2} has a significant effect on the saturation performance of the Darlington, and that at 3 V and lower the gain is reduced markedly with increasing values of R_{B2} . This is due to a reduction in the collector-emitter voltage of the driver, V_{CE1} , which moves this stage from region 2 to region 1, the cut-off region.

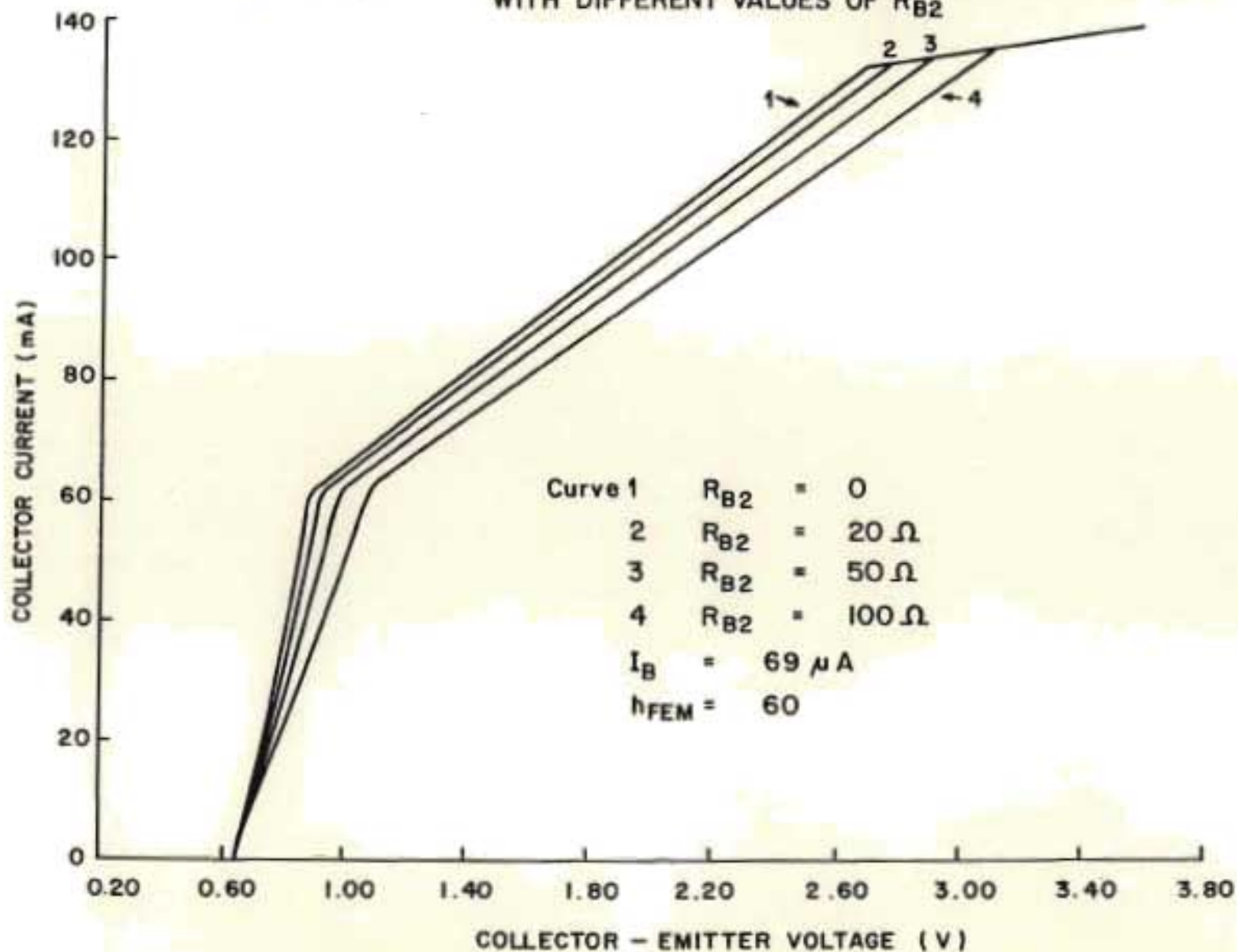
In Section 3.6.4.8 (page 88) it was mentioned that one reason for using an interdigitated emitter structure was the possibility that the base resistance of the output stage could affect the saturation performance of the Darlington. Probed measurements on the drop-in *014 discrete transistors on a wafer with the Darlington transistors indicated, after scaling of the active area to equal the PT018, that the figure of R_{B2} would have increased from about 6 ohms to 10 ohms if an interdigitated structure had not been used. From Figure 4.22 (page 162) it may be seen that at collector currents of even below 150 mA this would have made a small but definitely detrimental difference to the saturation performance of the PT018 Darlington.

4.7.3 Current handling limits of the Darlington

In practice a circuit designer may have control only over the collector-emitter voltage and the base drive current of the Darlington, and may wish to use the device in a condition where one or both of the stages of the device are in a region where gain drops rapidly. A parameter over which the designer would not normally have control would for instance be the process gain, where the device would simply meet specified upper and lower boundary limits and the designer would have no direct information on how the device would perform at such high current levels. In the subsections following it is shown, with the aid of Model 2, how the current-handling capability is affected, firstly by the applied collector-emitter voltage - an external variable - and secondly by process gain, solely a property of the device.

FIGURE 4.22

COMPUTED SATURATION CHARACTERISTICS OF A PT018
WITH DIFFERENT VALUES OF R_{B2}



4.7.3.1 Current-handling limits as a function of V_{CE}

In this section a process gain of 60 was used and the Darlington gain computed as a function of collector current by increasing I_B at four fixed values of V_{CE} . The gains are recorded as a function of I_C for values down to a lower limit of 10, and are shown in Figure 4.23 (page 164).

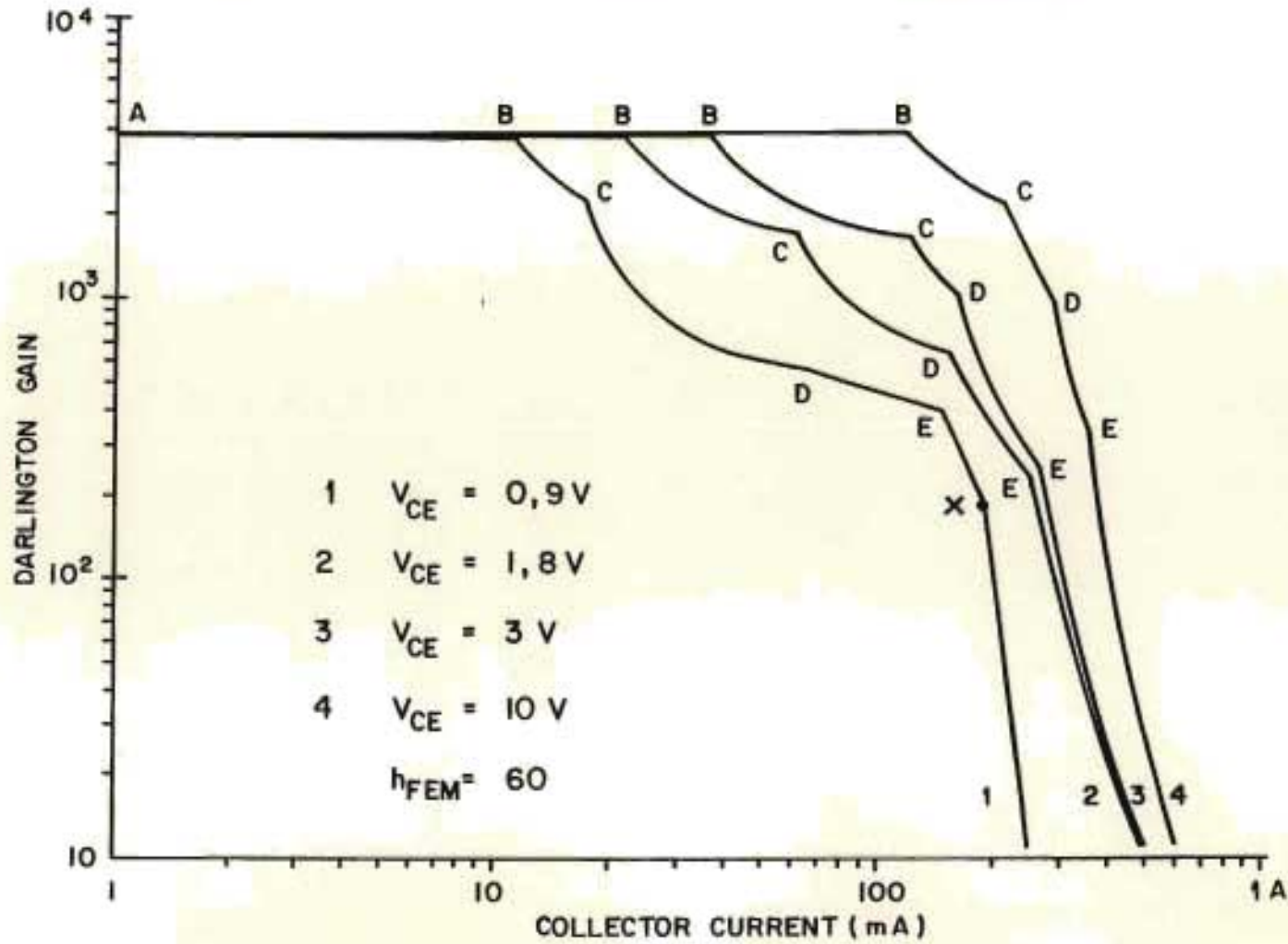
Before commencing a discussion on the importance of the whole curve, it is useful to explain the nature of the various regions of operation that the stages of the device pass through as the Darlington gain decreases. The explanation is a parallel to that given in Section 4.6.5 (page 151), where process gain was computed as a function of collector resistance R_C . Here, a sixth mode of operation is considered for low values of collector-emitter voltage. The operating regions are listed below.

- (a) Segment AB, the flat segment, where the Darlington gain is approximately equal to the square of the process gain.
- (b) Segment BC, where the output stage operates in region 2, quasi-saturation, and the driver in region 3, normal operation.
- (c) Segment CD, where both the driver and output devices operate in quasi-saturation, thereby compounding the drop in gain.
- (d) Segment DE, where gain droop due to high-injection effects in the output device contributes to the overall drop in gain.
- (e) Segment EF, where high-injection effects commence in the driver stage, further compounding the gain droop.
- (f) Segment FG, which is applicable only at low values of the collector-emitter voltage. Here, as the base-emitter voltage of the output device increases, the driver moves from quasi-saturation into the cut-off region. The start of this region on the curve for $V_{CE} = 0,9$ V in Figure 4.23 (page 164) is indicated by the symbol 'X'.

The sequence in which these various regions of operation begin may not always be the above as it depends, *inter alia*, on the geometrical design of the device, the properties of the epitaxial layer, the process gain, and even the operating conditions.

FIGURE 4.23

GAIN VS COLLECTOR CURRENT FOR THE PTO18
 COMPUTED FOR FOUR VALUES OF COLLECTOR-EMITTER VOLTAGE



The curves in Figure 4.23 on the previous page show what is probably the most marked difference from those presented by Wheatley and Einthoven⁵⁵. In the case presented here, gain crowding owing to the effects of the collector region resistance is the predominant reason for the initial fall in Darlington gain. Only at higher collector currents do the effects of high injection contribute significantly to the fall in gain. It will also be noted on these curves that the value of the collector-emitter voltage plays a most important role in determining the current level at which the gain begins to fall, a point that is given scant attention by the above authors. According to them, the applied collector-emitter voltage should have a much smaller effect on the gain, but in fact this is only true at the upper limiting currents. For optimum saturation performance, the curve for $V_{CE} = 0,9$ V does reinforce the finding in Section 4.7.2 that the minimization of V_{BE} in the output stage plays an important role in optimizing saturation in a Darlington transistor.

Quasi-saturation operation has thus been shown to be a vital factor in determining the maximum current level at which a certain minimum gain may be obtained from a Darlington, particularly at low collector-emitter voltages.

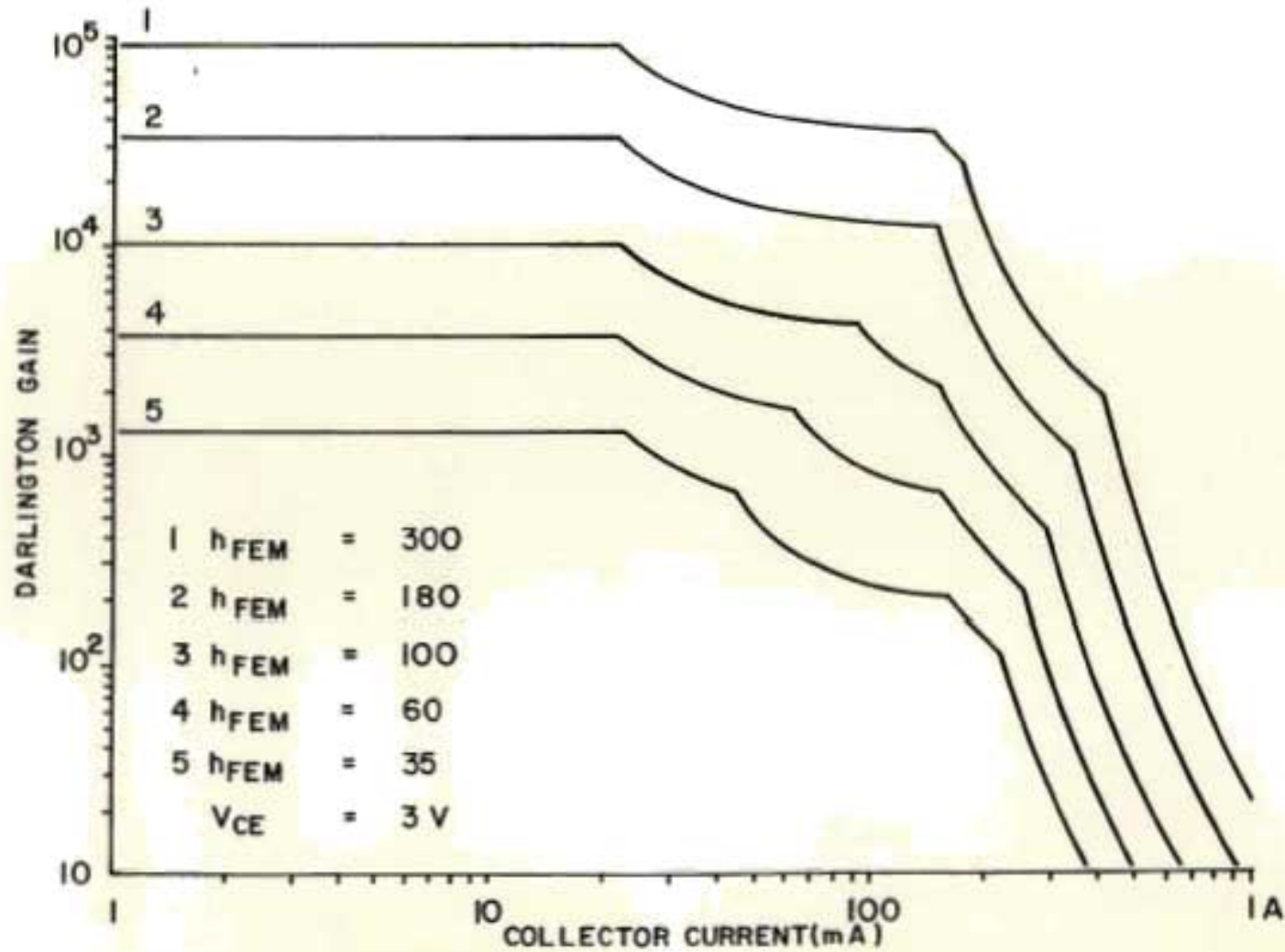
4.7.3.2 Limiting Darlington gain as a function of process gain, h_{FEM}

Figure 4.24 (page 166) shows the Darlington gain computed, as in the previous section, for five different values of process gain, with the collector-emitter voltage fixed at 1,8 V. Noteworthy features that emerge are listed below.

- (a) Although as had been anticipated, with the process gain increasing from 35 to 300, the peak gain of the Darlington transistor increases by a factor of almost 100, at high-injection levels the value of the collector current at which the Darlington gain drops to 10 increases from 0,38 A to only 1,1 A, i.e. by a factor of less than three.
- (b) For higher gains, the onset of gain droop owing to high-injection effects in the output stage may occur before the driver moves into quasi-saturation operation.
- (c) The value of the collector current at which the gain begins to fall is quite independent of the process gain.

FIGURE 4.24

GAIN OF THE PTO18 DARLINGTON AS A FUNCTION OF COLLECTOR CURRENT FOR FIVE VALUES OF PROCESS GAIN



4.7.4 Effect on Darlington gain of the area ratio, N'

At $V_{CE} = 3V$, which is the maximum operating voltage of the PT018 for the more stringent impulsing condition, the Darlington gains were computed for three values of N' , viz 1, 6 and 25, and the results are plotted in Figure 4.25 (page 168). In performing these computations the total active area for the Darlington (i.e. the sum of the active areas of the driver and output stages) was kept constant and equal to that of the PT018 transistor. The process gain h_{FEM} was held constant at 60, as this value was the lower limit initially used to meet the minimum specified gain of the PT018 during manufacture.

The total area under the curve with $N' = 6$ is the greatest, and offers the widest possibility of meeting specific gain requirements at high collector currents. In addition, the curve for $N' = 6$ drops more smoothly than is the case for the curves with N' values of 1 or 25.

4.7.4.1 Comparison with practical results

For the case where $N' = 6$ it was possible to confirm good accuracy for the curves, as this was the ratio for a PT018. For the case of $N' = 1$, only the output stages of two similar PT018 transistors, assembled specially for the test with bonding wires to this stage alone, were connected in a Darlington configuration and the measured current values halved so that the results could be compared with the computed curve. Again good agreement with the computed curves was obtained.

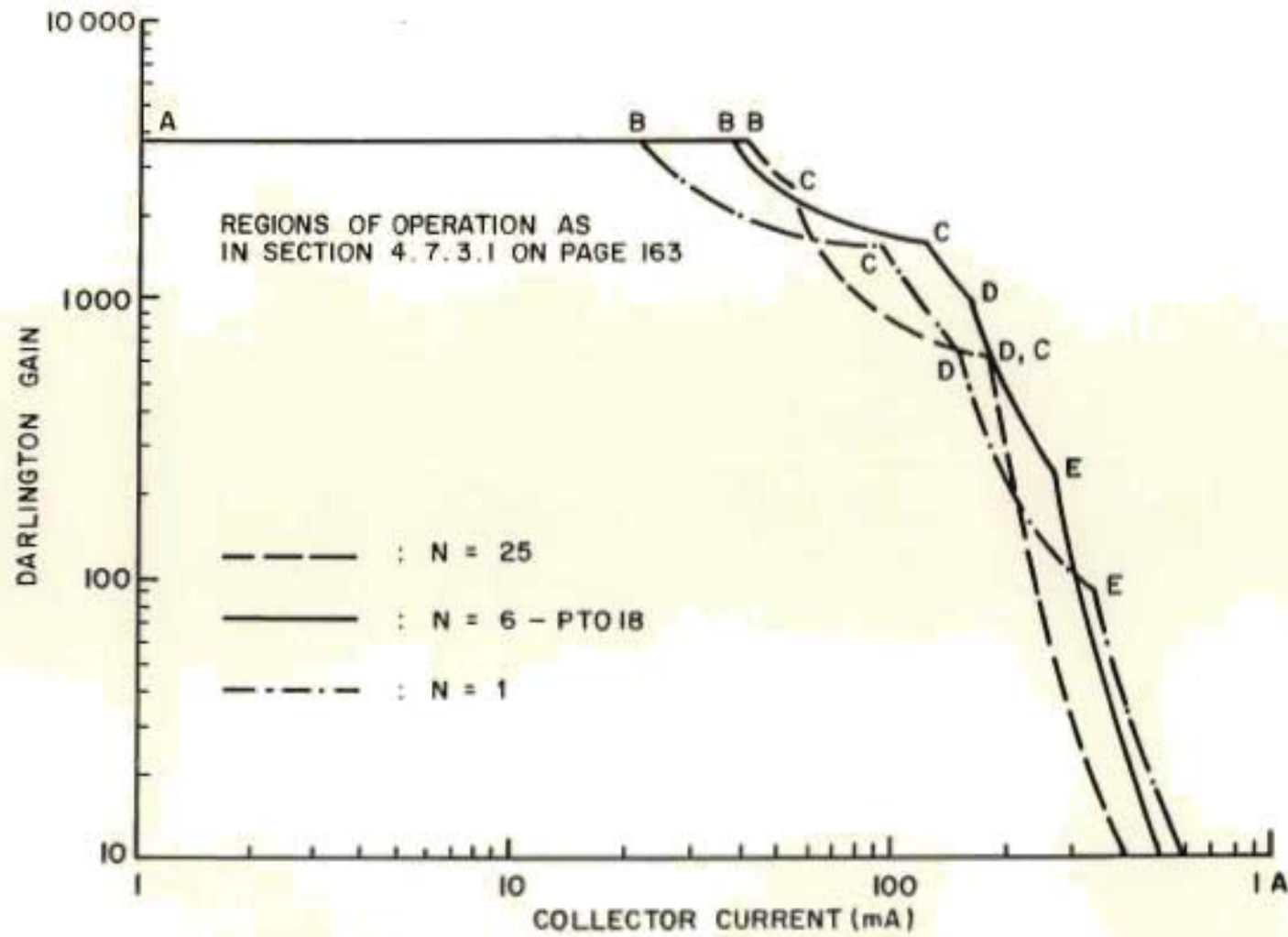
It was not possible to confirm experimentally the validity of the curve for $N' = 25$, as another set of photomasks would have been required for this exercise.

4.7.4.2 An unexpected result

Intuitively it had been expected that as N' increased, the collector current at which the gain of the Darlington would reach a lower limit of, say, 10 would increase owing to the increased area of the output stage.

Figure 4.25

Darlington gain vs collector current at $V_{CE} = 3V$ for three values of area ratio N' .



Quite the converse occurred, and a small decrease in this limiting current was computed. This decrease was ascribed to the fact that, as the area of the driver was decreased, the gain of this stage decreased more rapidly because high-injection effects became the predominating factor. This made it impossible to take advantage of the increased area of the output stage. That this observation was indeed due to gain crowding effects was demonstrated by removing the correction for high injection from the simulation program. In this case the peak current increased continuously with N' .

In concluding this section, it may be said that it would appear that the value of only 6 for the area ratio N' in the case of the PT018 has again been shown to have been well chosen. The fact that much higher values of N' are encountered in commercial devices indicates that it would be difficult to make any generalized rules on the partitioning of the areas of Darlington transistor stages at this point. To gain further insight into area partitioning, the importance of the area ratio N' is analyzed in greater detail in the following section.

4.7.5 Optimizing the area ratio N'

It was shown in Section 4.7.4 that the area ratio N' had only a small effect on the peak current-handling capability in the gain droop region of a Darlington, but had a marked effect on the shape of the gain droop curve. For a Darlington transistor exhibiting this type of characteristic, it was decided that the total area under the gain versus collector current curve, termed the 'gain integral', would provide a good figure of merit for comparing devices with different N' values.

Starting with $N' = 1$, the gain integral was computed above a threshold collector current at which there was no gain droop (1 mA for the PT018). In the computation the base current was increased in small geometrical steps and the increase in collector current at each step multiplied by the Darlington gain at that step to form an element of area under the gain curve. By summation of all the area elements between $I_C = 1$ mA and the limit of collector current, where the Darlington gain had dropped to 10, yielded the total area for the gain integral associated with $N' = 1$ and this was recorded. The same procedure for calculating the gain integral was carried out using a geometrical increase in N' , the area again being recorded. Although a wide

range of N' values was used, the total active area of the device was held constant, so that the resulting 'normalized gain integrals' could be compared as a function of area ratio, N' . In these computations the process gain h_{FEM} was held at the minimum value of 60.

Figures 4.26a and 4.26b (page 171) show the curves for the normalized gain integral and peak current-handling capability of the device for a gain of 10, computed at the same time, for $V_{CE} = 3$ V and 1,8 V respectively. Comparison of these two graphs shows that the optimum area ratio appears to be a function of the collector-emitter voltage. At $V_{CE} = 3$ V, the optimum value of N' is approximately 5, and at 1,8 V it is about 3. This strong dependence on collector-emitter voltage was not anticipated, and is analyzed in more detail in Section 4.7.6 (page 172).

The normalized gain integral, peaking at $N' = 5$, for $V_{CE} = 3$ V, actually refers to the current-handling capability of the device, up to limiting collector currents many times greater than the 125 mA limit for the impulsing condition. It may be seen from Figure 4.26a that for the PT018 with $N' = 6$, the gain integral was only 2 per cent below the value for optimized operation down to a Darlington gain of 10. At 1,8 V, where N' peaks at 3, a reduction of only 6 per cent in gain integral may be measured from Figure 4.26b. From these results it is clear that 6 was indeed an excellent value of N' to have used in the PT018 design, as the device was not only optimized for the specified operating conditions, but also well optimized for operation over a very wide range of collector currents even up to limiting values at high-injection levels.

It is also worthy of note that the optimum current-handling capability of a Darlington made in the PT018 process occurs for an area ratio of about 1,1 in Figure 4.26b, the $V_{CE} = 1,8$ V curve. Thereafter this capability decreases as N' increases. A peak in the collector current-handling capability does not appear on the 3 V, curve which does not give results for values of N' less than 1 where this peak occurs.

These results were not verified experimentally, but the simplest and least expensive manner in which this could have been done would have been to provide, say, a 5 x 5 matrix of small discrete transistors that could be connected in Darlington configuration with a sufficient variety of interconnection patterns to provide area ratios ranging between 0,25 and 24.

FIGURE 4.26 a
 NORMALIZED GAIN INTEGRAL AND PEAK CURRENT
 LIMIT AS A FUNCTION OF AREA RATIO N'

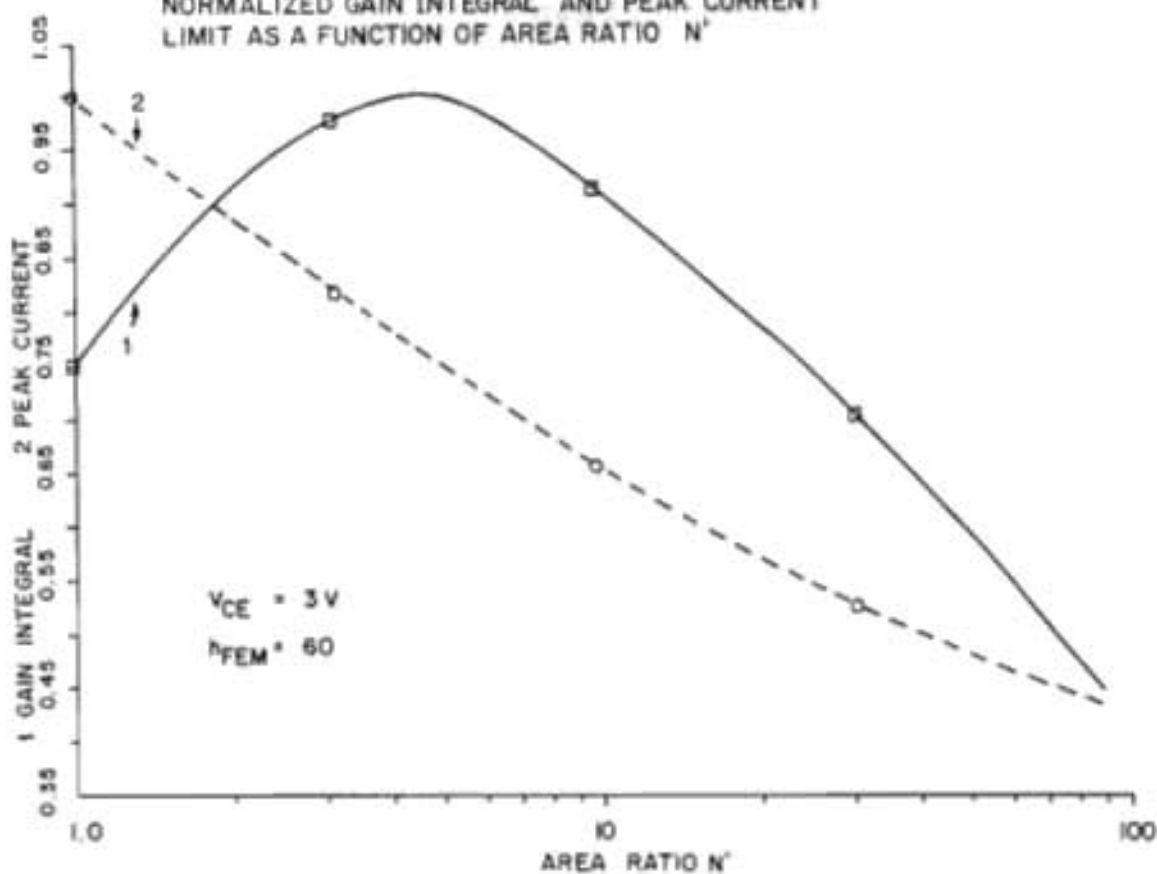
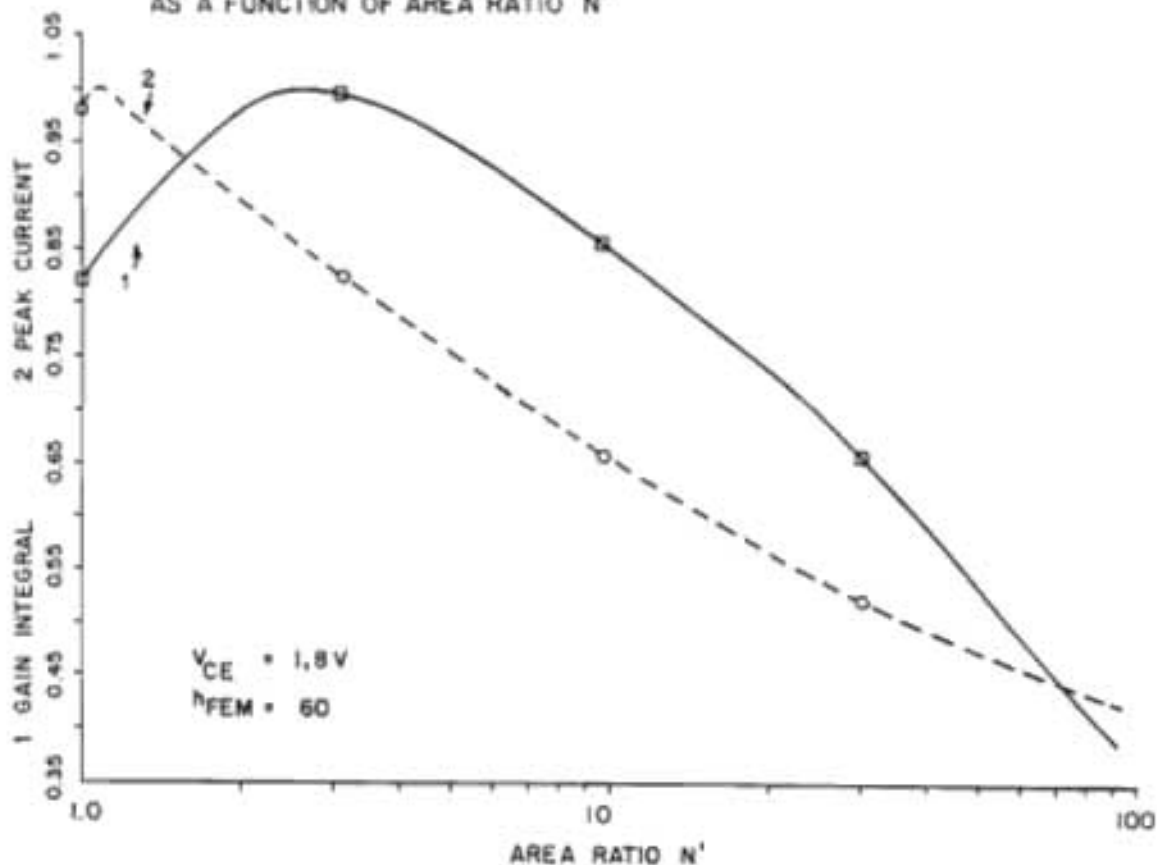


FIGURE 4.26 b
 NORMALIZED GAIN INTEGRAL AND PEAK CURRENT LIMIT
 AS A FUNCTION OF AREA RATIO N'



4.7.6 Peak N' as a function of three different variables

In this section the computed peak values of N' are presented as functions of three separate variables : the collector-emitter voltage V_{CE} , the process gain h_{FEM} and the process constant PC.

4.7.6.1 Peak N' as a function of V_{CE}

To compute values for the curve, the collector-emitter voltage was increased in geometrical steps from just above the voltage at which the Darlington commenced operation, and the optimum value of N' computed for each value of the voltage.

Figures 4.27a and 4.27b (page 173) show the peak value of area ratio as a function of collector-emitter voltage, for values of process gain of 60 and 180, respectively. For a gain of 60 there is a slight increase in N' as the transistor commences operation, leading to an initial peak value of N' that was just under 5. A drop then follows to $N' = 2,5$ at 1,5 volts. Thereafter the value of N' increases steadily and the curve flattens out at a value of about 14,5 at 30 V. The second curve shows no drop in N' at low voltages, but again flattens out at about 30 V, this time to a peak of $N' = 24$.

Certainly the major implication when designing a Darlington in the the PT018 process appears to be that, at lower voltages, lower values of N' are required for optimum Darlington gain characteristics. When optimum saturation characteristics are aimed at, low values of N' , certainly values below 8, are called for, irrespective of the process gain. It should be noted that for the lower value of h_{FEM} lower values of N' are required to ensure optimum Darlington gain performance at low collector-emitter voltages.

4.7.6.2 Area ratio as a function of the process gain

The only control that a circuit designer normally has over the process gain is an accept/reject criterion against an electrical test. If, however, it should be desired to evaluate the Darlington device for applications other than those for which it was designed and where different process gain limits would apply, the following computation would be of use,

FIGURE 4.27 a

OPTIMAL VALUE OF AREA RATIO N^* AS
A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

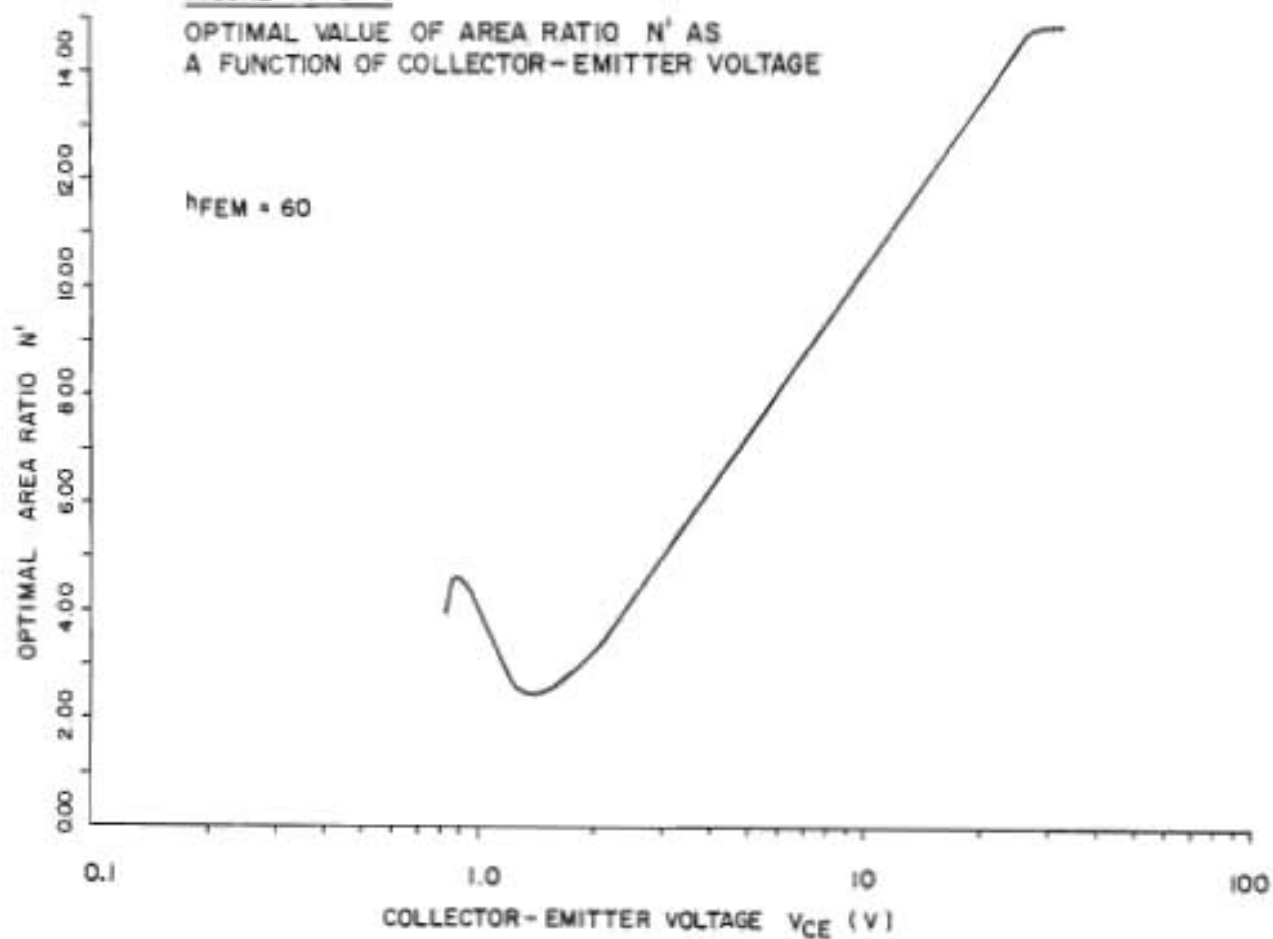
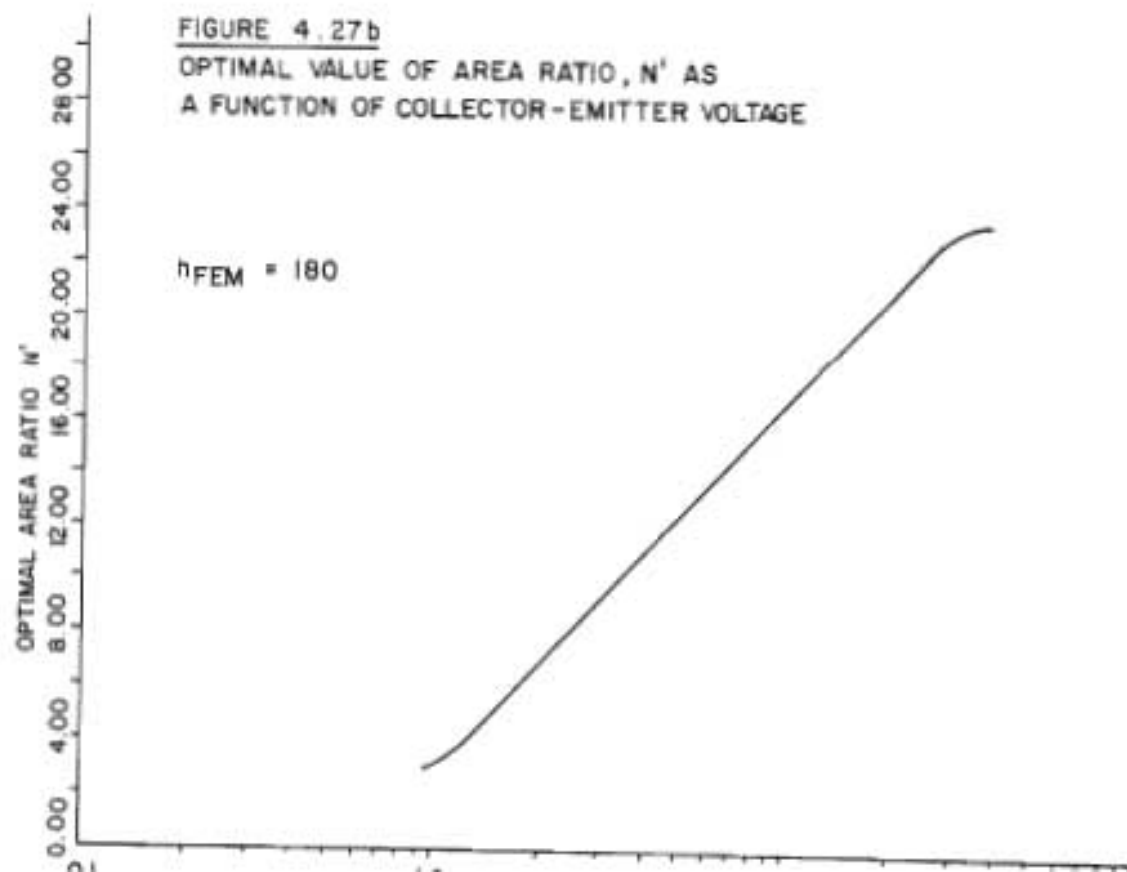


FIGURE 4.27 b

OPTIMAL VALUE OF AREA RATIO, N^* AS
A FUNCTION OF COLLECTOR-EMITTER VOLTAGE



giving the optimum area ratio as a function of process gain.

Figures 4.28a and 4.28b (page 175) show the variation of N' with process gain at collector-emitter voltages of 3 V and 1,8 V respectively. These curves reveal that the increase in N' with process gain is rapid initially, but the rate of increase drops at the higher-gain end of the curves.

Referring again to the PT018 transistor, with $V_{CE} = 3$ V, Figure 4.28a shows that for $N' = 6$, the associated process gain for optimum performance over the widest range of collector currents would be 80. From Figure 4.28a, for $V_{CE} = 1,8$ V, the PT018 would be optimized at a process gain of 180. Both these process gains are within the normal production limits for the device, thus it would be possible to select devices with optimum gain integrals for either of these operating voltages if such were required.

4.7.6.3 Optimum area ratio as a function of the process constant, PC

The process constant PC is simply the ratio R_{QS}/R_C and has been found to vary very little for a given discrete transistor production process. An investigation of over 20 different transistor types from various manufacturers, has shown that the range of values for PC was between 1,2 and 2,4 at ambient temperatures. The value of PC for the NEERI high-voltage transistor process was approximately 1,5.

PC is an important variable for the following two reasons.

- (a) It is temperature-dependent, decreasing with increasing temperature for the NEERI process, as indicated in Figure 4.12 (page 137), implying that a value of N' should be chosen suited to the operating temperature of the device.
- (b) If it should be necessary to find a second source for the PT018 Darlington transistor, it is probable that even if the same set of masks were used in another manufacturer's process, a different process constant might adversely affect device performance.

FIGURE 4.28 a
OPTIMAL AREA RATIO N' AS
A FUNCTION OF PROCESS GAIN h_{FEM}

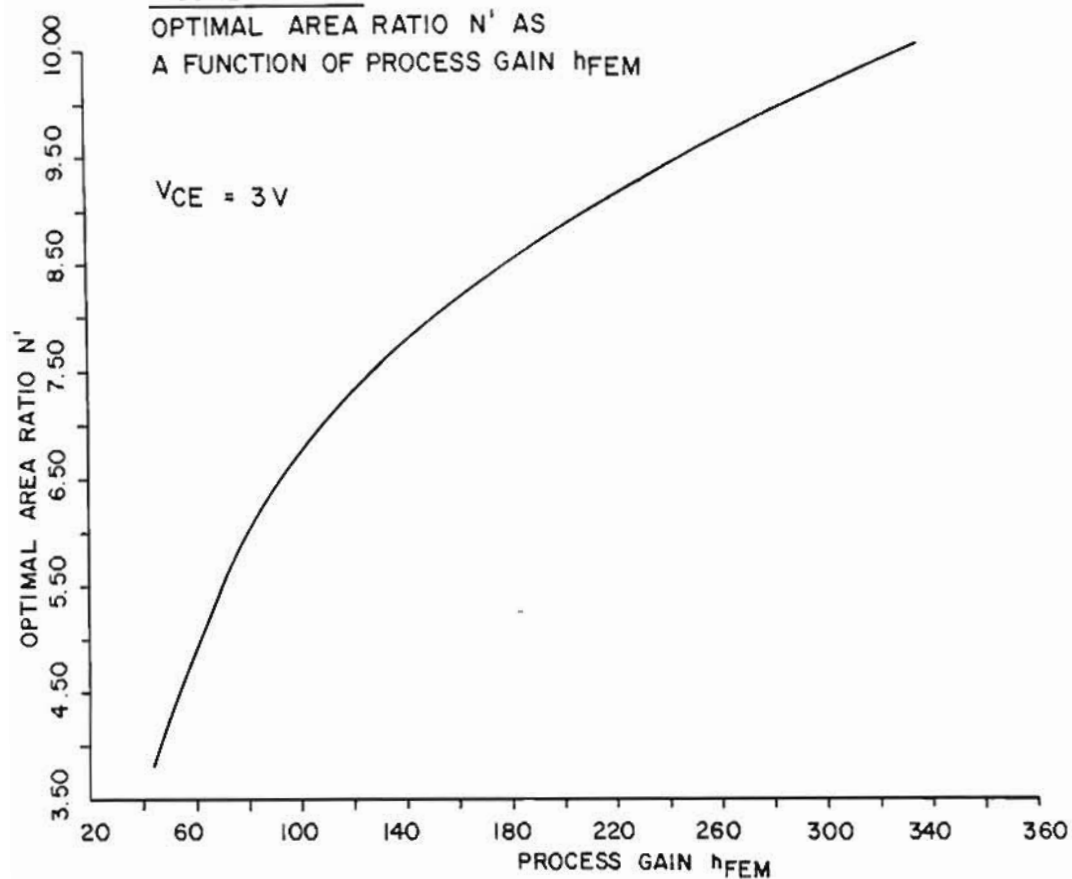
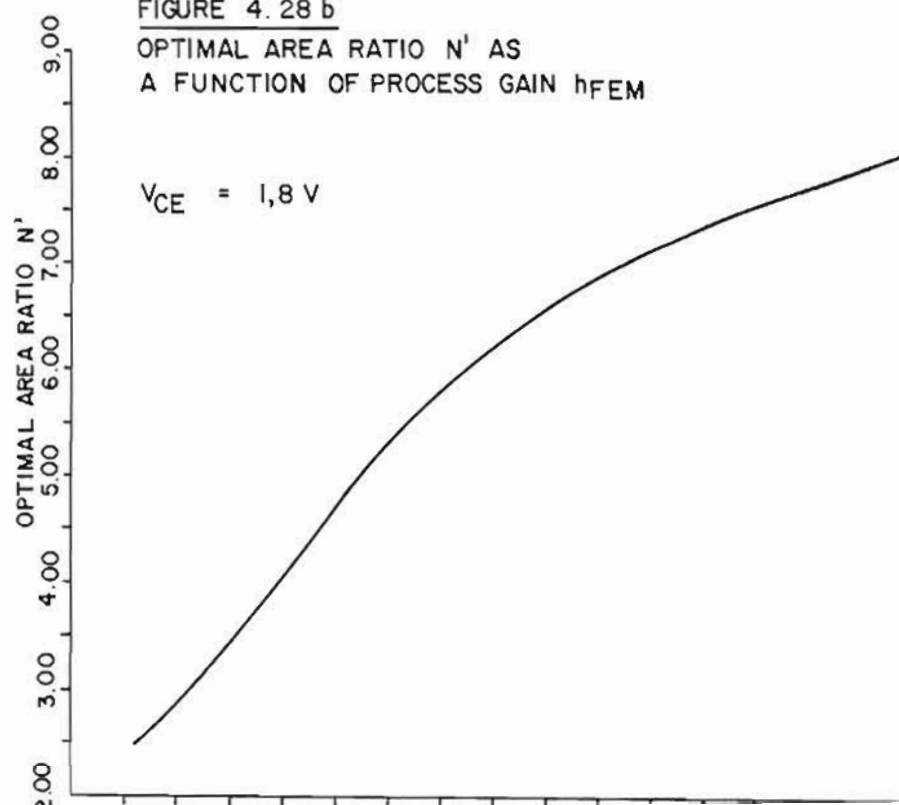


FIGURE 4.28 b
OPTIMAL AREA RATIO N' AS
A FUNCTION OF PROCESS GAIN h_{FEM}



To investigate (b) further, Figure 4.29 (page 177) was plotted and shows N' , calculated as a function of the process constant over the range from 1,1 to 3, for a device with a process gain of 60 at an applied collector-emitter voltage of 3 V.

It is clearly seen that for any value of the process constant below 1,2, a high value of N' is indicated, but above $PC = 1,2$ very little change in N' is required for values of PC up to 3. There would thus appear to be no objection to the use of another manufacturer's technology, provided that the process constant were above 1,2, bearing in mind, of course, that PC is reduced at high temperatures (see Figure 4.12, page 137). It would now appear that the major considerations would be to ensure that appropriate values of collector resistance and collector-emitter breakdown voltage were achieved in an alternative technology.

4.8 CONCLUSION, AND DISCUSSION OF THE VALUE OF MODEL 2

4.8.1 Deductions from the use of Model 2

Model 2 was initially developed to characterize saturation and quasi-saturation operation in high-voltage transistors, and it has been shown to be a viable tool that provides gratifyingly accurate numerical predictions of operation in these regions.

Only two radically new parameters were introduced, these being the 'Quasi-saturation Resistance' R_{QS} and the Cut-off Voltage V_{CO} , although the Conduction Threshold Voltage V_{CT} ($= kT/q$) used in Model 2 is at least new in name. Measurement of the parameters for Model 2 is generally simple, rapid and accurate, and values can be obtained without the aid of expensive equipment. It was found that default values of $V_{CO} = 200$ mV and $V_{CT} = 25$ mV gave good agreement between measured and computed curves. This implied that if a rapid assessment of the saturation and quasi-saturation performance of a transistor is required it should be necessary to measure only R_C , R_{QS} and h_{FEM} .

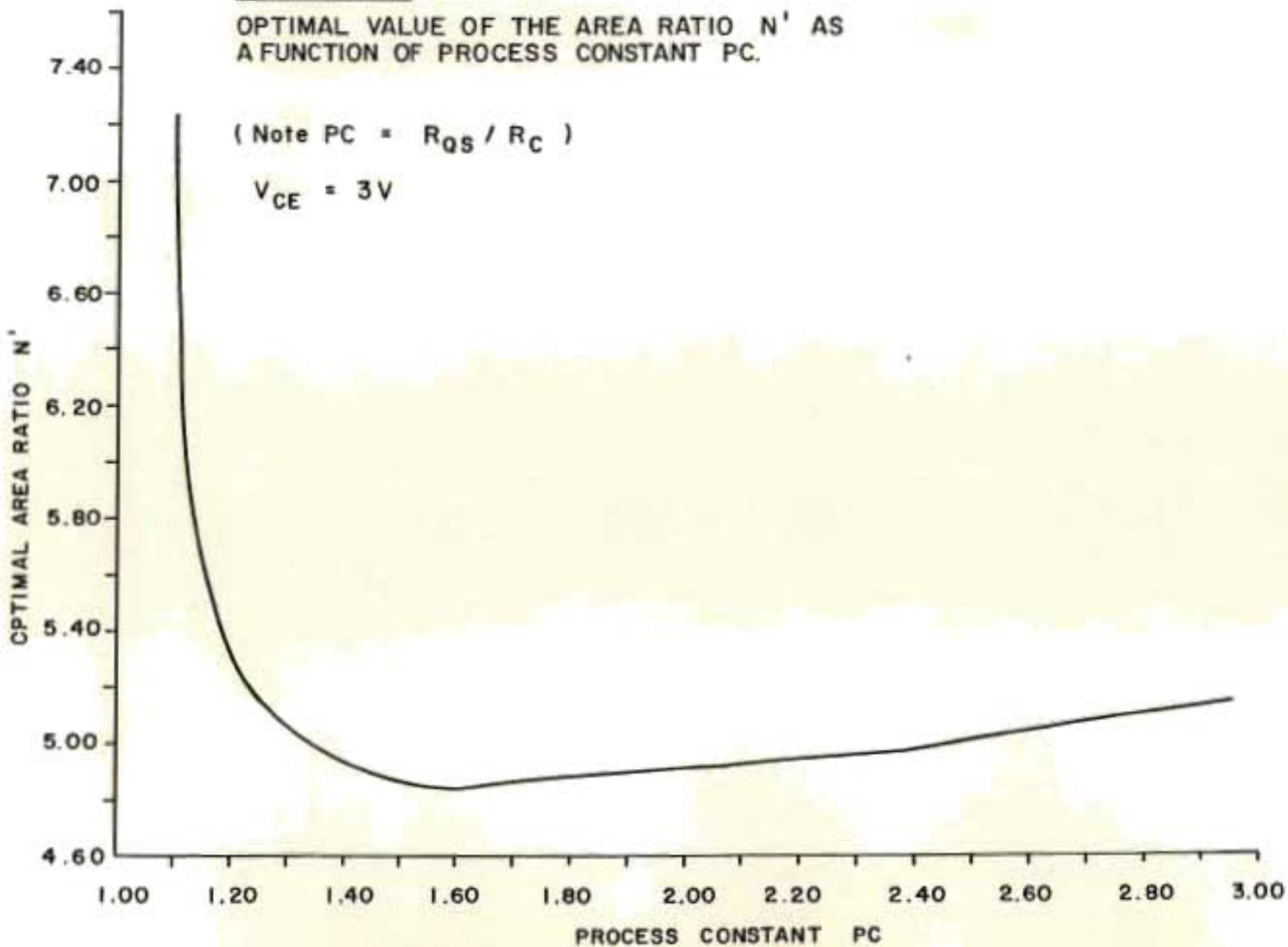
The applicability of Model 2 was demonstrated for the specific case of the PT018 integrated Darlington. The modelling procedure is, however, confidently believed to have far wider application, provided the following

FIGURE 4.29

OPTIMAL VALUE OF THE AREA RATIO N' AS
A FUNCTION OF PROCESS CONSTANT PC .

(Note $PC = R_{QS} / R_C$)

$V_{CE} = 3V$



precautions are observed.

- (a) The numerical limitations of Model 2 should be appreciated.
- (b) Current densities should be used for which Model 2 is a valid arithmetic tool, or a valid correction for high-current injection should be introduced into the calculations.
- (c) Operating points chosen for computations should be realistic and such as do not violate points (a) and (b) above. It has been found a simple matter to do this in certain cases either by moving the operating points or adjusting device parameters, such as the process gain.

4.8.2 Application of Model 2 in more general simulation programs

If it were wished to apply Model 2 directly in a designer-orientated simulation program for integrated circuits, such as 'SPICE', it would be necessary to consider the following.

- (a) A simple and rapid numerical method should be devised for rounding of the transitions between the three regions of operation, so as to obviate harmonic products of unrealistically high order being calculated in AC analyses.
- (b) Additional parameters suitable for Model 2. In addition to those normally used in 'SPICE' the only other parameter would be the quasi-saturation resistance R_{QS} measured in the manner required for Model 2. As noted in Section 4.6.2.2 (page 146), the parameter R_C in an integrated circuit transistor would have components from both the active transistor area and the path to the collector contact. This would only mean that the method of measuring R_C should relate to the total value, instead of just the parasitic resistance measured with the transistor driven hard on, which is present practice. As the value of R_C would depend on the layout of the transistor, the ratio R_{QS}/R_C would no longer be a constant, and the concept of a process constant would no longer be valid.

- (c) It would be necessary to assess the limits of the performance of Model 2 at higher frequencies. The only such experience with the model was in the case of surges of duration of about 1 microsecond, where the predicted values of collector current agreed well with those measured during surge testing of the PT018 in the Disa telephone. (See Section 4.6.4 on page 151.) Here the results referred to operation outside the saturation regions, where voltages of up to 350 V were applied to the device. As the PT018 had a transition frequency f_T in excess of 10 MHz, Model 2 was found to be accurate for these surge conditions. Chudobiak⁵⁷ has demonstrated the time-dependence of saturation, and the effects of the collector epitaxial layer in high switching-speed transistors were considered by Tang et al.⁵⁸ These studies could well form the basis for the extension of Model 2 to prediction of saturation at high frequencies.

In concluding Section 4.8 it may be said that from the results derived during the production of the PT018, the soundness of Model 2 as a design tool for steady-state saturation prediction has been borne out, and, viewed as a whole, the model has been shown to be an original concept. Having been developed on the basis of conclusions drawn from experimental data, Model 2 forms a tool that promises to find wide application, particularly in view of the ease with which it may be applied and the accuracy it can provide.

To summarize the design techniques developed in Chapters 2, 3 and 4 a flow diagram is presented in Appendix 4.5 (page 254) giving a possible sequence of steps in the design of a transistor.

CHAPTER 5

PROCESS TECHNOLOGY DEVELOPMENT, TECHNOLOGY TRANSFER AND
DATA MANAGEMENT FOR THE PT014 AND PT018 PROJECTS

5.1 INTRODUCTION AND SUMMARY OF CHAPTER

The preceding three chapters have covered certain research findings and development activities associated with contracts for the development of two high-voltage transistors. The whole programme spanned more than five years. To date almost two million working devices have been successfully produced, processing being handled in a small integrated circuit facility that was not initially intended for the manufacture of devices of these types. The success of these undertakings represents a unique record in the history of South African micro-electronics. In analysing the programmes as a whole, it turns out that almost 40 per cent of the time was devoted to device and process development and the associated research. The balance of the activity was essentially of a technical administration nature, as it was necessary to liaise impartially at all levels and stages with the die manufacturing personnel, and at more senior levels through the production chain to the purchaser of the subscriber telephone. With the object of improving device quality and system reliability, and reducing cost, data were gathered at all stages of the programme from whatever sources were available, and the necessary refinements, both technical and procedural, made on a continuous basis.

A brief sketch of the chronology of the programmes is given, and this is followed by a discussion of three key aspects of the undertaking :

- (a) process development, including the specific constraints relating to the production activity;
- (b) transfer and industrialization of the process technology; and
- (c) data acquisition and data management as an aid to production.

5.2 CHRONOLOGY OF THE PROGRAMMES FROM DEVELOPMENT TO PRODUCTION

The transistor development programmes embraced a large number of activities, and the purpose of this section is to list the major ones in chronological order, while imparting some conception of the breadth of the undertaking to complement the depth detailed in the previous three chapters.

Figure 5.1 (page 182) is in the form of a flow diagram and shows the major constituent activities from the inception of the programmes.

5.3 FACILITIES AVAILABLE FOR PROCESS DEVELOPMENT

In the development of the process technology for the high-voltage transistors, the author had laboratory equipment available dating in design from the late 1960s whilst more advanced technologies, such as ion implantation, were not available. The NEERI Integrated Circuit Facility (ICF) had in use a planar bipolar integrated circuit process dating from about 1968, used for the manufacture of integrated circuits with a maximum collector-emitter breakdown of 20 V.

Resources related to analytic tools and available at the CSIR were good, comprising most of the modern surface analysis techniques. Frequent use was made of the scanning electron microscope (SEM), both during development and for trouble-shooting during production. The process control measurement facilities available for production were not advanced; they included good optical microscope facilities, a groove and photo-chemical stain method for junction depth determination, and a four-point probe for the control of boron and phosphorus depositions.

In order briefly and clearly to compare the requirements for the development programmes with the resources available, a tabular approach has been adopted, the main considerations appearing in the first three tables that follow.

Table 5A (page 183) compares available facilities and processes with those required for high-voltage transistors, and indicates each type of change that was required. Table 5B (page 184) deals with the required process changes in more detail, and Table 5C (page 185) compares the available and required inspection and quality screens.

Table 5D (page 186) is not directly related to the development programmes as initially set out, but does show how the total involvement of the author extended into related areas of high-voltage transistor activities outside the CSIR, and how these considerations led to positive contributions to other aspects of the undertaking.

FIGURE 5.1 THE DEVELOPMENT OF THE PTO14 AND PTO18. THIS DIAGRAM SHOWS THE CHRONOLOGICAL SEQUENCE OF EVENTS IN THE DEVELOPMENT PROGRAMMES FOR THE PTO14 AND PTO18 TRANSISTORS.

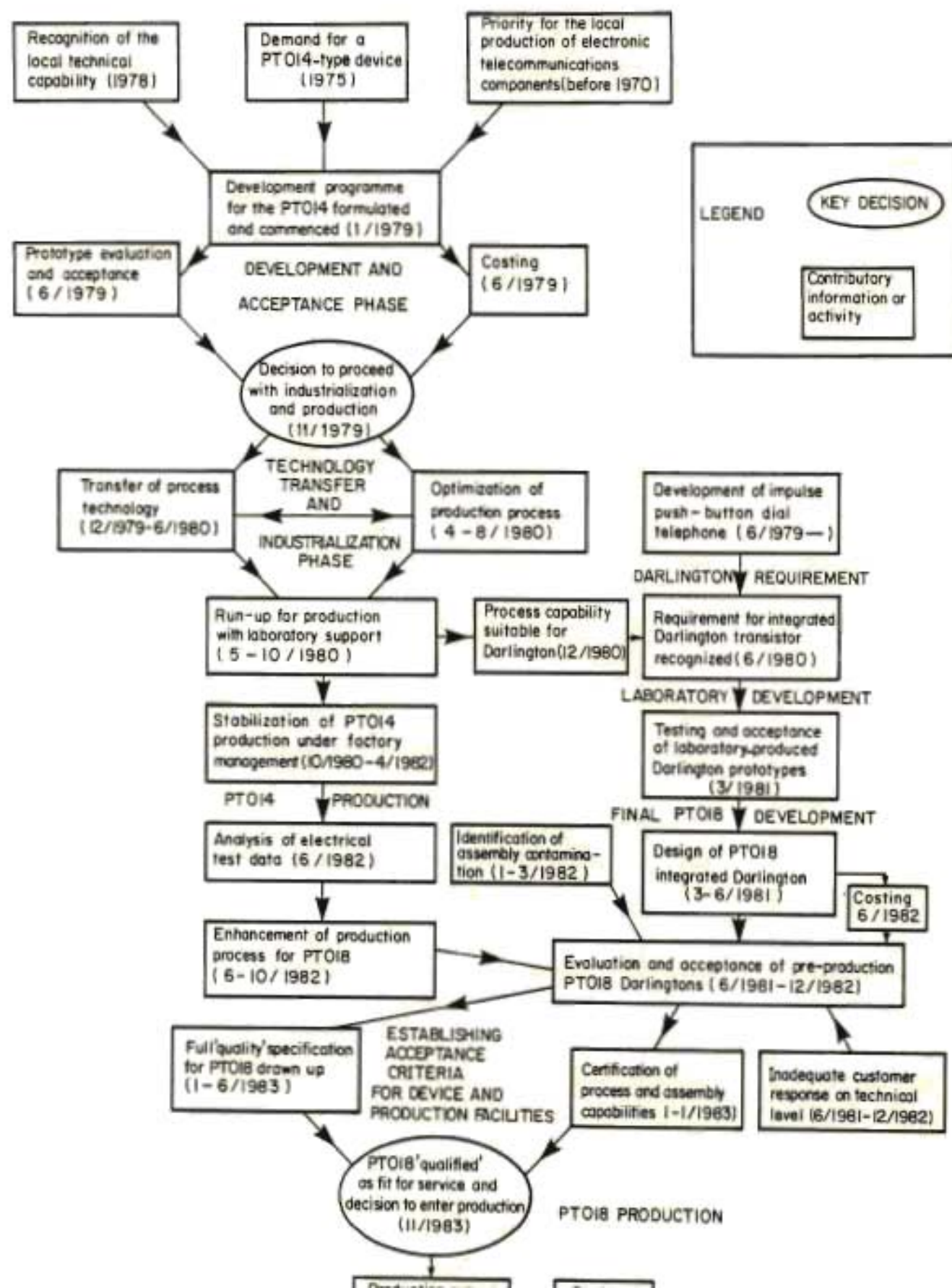


Table 5A : A comparison of required and available process capabilities

Item	Required	Available on site	Change	Nature
1	Epitaxial silicon 33-50 ohm.cm 45 μ m thick	Epitaxial silicon 5 ohm.cm 18 μ m thick	Yes	Specification
2	Deep diffusions for $BV_{CB} = 500$ V	Shallow diffusions $BV_{CB} = 150$ V	Yes	Process
3	Stable I_{EBO} characteristics after reverse-bias stress	Instability in I_{EBO} after stress	Yes	Process
4	High reverse emitter-base breakdown > 7 V	$BV_{EBO} < 7$ V	Yes	Process
5	Oxides with high breakdown-voltages and low Q_{ss}	Emitter oxide inadequate	Yes	Process
6	Large active area ($\approx 0,4$ mm ²)	Small active area ($0,04$ mm ²)	Yes	Layout
7	Ability to handle 2 000 wafers p.a.	Only 500 p.a. handled	Yes	Equipment Organization
8	Electrical testing to 300 V then 450 V	Testing to 100 V	Yes	Revised and later, new test gear
9	Quality assurance & process control	Quality assurance & process control	Yes	New limits

Items 2 to 5 imply considerable process changes were required, and some key features of these changes are covered in Table 5B on the next page.

Table 5B : Details of changes for high-voltage transistor process

Item	Process requirement	Process available	Type of change made
1	Field oxide > 1 μm	First oxide 1,2 μm	No change
2	Base deposition (high sheet-resistivity)	90 ohm/square	No change
3	Base drive-in to approx. 7 μm	Base drive-in to 3 μm at 1150 $^{\circ}\text{C}$ (2 hours)	Use of isolation tube at 1180 $^{\circ}\text{C}$ (5 hours)
4	Emitter deposition and drive-in	Emitter drive-in at 1050 $^{\circ}\text{C}$ (1/2 hour) to 2 μm	Use of spare emitter tube for up to 5 hours at 1050 $^{\circ}\text{C}$ for 6 μm (later modified to 1080 $^{\circ}\text{C}$)
5	Post-emitter anneal with oxide regrowth	Post-emitter anneal at 900 $^{\circ}\text{C}$ in N_2	Oxidation system added to existing anneal tube, use dry-wet-dry oxidation and N_2 anneal
6	Metal : 1 μm Al	Metal : 1 μm Al	No change
7	Sinter 500 $^{\circ}\text{C}$	Wet sinter 500 $^{\circ}\text{C}$ N_2 via 25 $^{\circ}\text{C}$ water	No change
8	Photo-engage : all stages	Base, emitter, contact & metal photo-engage exist	Etch times modified (only single masking step on emitter used)
9	Lapping and gold backing	None available	Lapping and gold sputtering equipment constructed

Changes to existing inspection screens and tests were made where required, and standard inspection screens adopted where possible. Details of the action taken are given in Table 5C (page 185).

Table 5C : Inspection screens available and modifications made
as a result of initiatives taken by the author

Item	Screens required	Screens available	Changes or additions
1	Incoming silicon inspection	Optical and visual	Optical and visual as per manufacturer's specification. Add : (a) Fracture test for orientation (b) Groove and stain for epitaxial thickness
2	Oxide thickness	Measurement on Dektak instrument	New limits set for base oxide and emitter oxide after anneal
3	Four-point resistivity probe for (a) Base deposition (b) Base drive-in (c) Emitter dep.	Four-point resistivity probe	New limits set for base drive-in and emitter deposition
4	Visual inspection (a) Etch limits (b) Alignment limits (c) Final visual inspection	(a) Screens as for bipolar ICs (b) Alignment limits (c) Final visual inspection	(a) No change (b) No change (c) New specification
6	Electrical tests (a) In-process tests (b) Final electrical probe test	Electrical tests (a) In-process tests for low-voltage devices (b) Low-voltage probe test	(a) Measuring conditions changed (b) Test gear modified and constructed
8	Field failure analysis	Not available	System set up for recovering devices and analysing failures

Table 5D : Contributions by the author to programme-related activities outside the CSIR

Key : (1) Direct interaction with author (2) Indirect interaction with author

Item	Process and screen requirement	Processes and screens available	Additions and changes
1	Accurate test for knee voltage at probe and final test (PT014)	Existing screens not reliable for knee-voltage testing (PT014)	Accurate sorting limits computed (1)
2	Contamination reduction in assembly	Methods not suited to minimizing contamination	Contamination sources identified (1) Procedural changes instituted (2)
3	Die bond improvement required	Gold backing process not characterized	Suitable specification for gold layer derived (1) Gold plating investigated (2)
4	Pre-encapsulation visual inspection to be improved	Inadequate equipment and documentation	Assistance given in setting up new inspection documentation (2)
5	Specification for electrical parameters and device quality. Accelerated life test specification	Specification of electrical parameters	Complete component quality specification produced with accelerated life test specification and end-of-life parameters (1) and (2)
6	Surge testing and the identification of failure modes	Surge testing available at Potelin	Failure modes of transistor identified, and recommendations made for telephone protection (1)

5.4 DETAILED SECTION COVERING PROCESS DEVELOPMENT

This section relates primarily to Tables 5A (page 183) and 5B (page 184) and elaborates on the most important processes for the high-voltage transistors developed in the laboratory.

5.4.1 Base diffusion process

This was a key process step in the fabrication of the PT014, and later the PT018. Both devices required very good control and repeatability of gain. For the PT014 alone a high reverse value of BV_{EBO} was required, preferably exceeding 8 V, as it had been found experimentally by Heeson¹⁰ that this was a desirable property for the device.

Process development was experimental, but guidance was taken from Slotboom and De Graaff⁵⁹ in adopting a low level of boron concentration that would not degrade device performance owing to bandgap narrowing in the base region. A summary of the final base process follows, covering both base deposition, using boron nitride disc sources, and drive-in at a higher temperature.

- (a) Base deposition was carried out in dry argon at 915 °C using oxidized boron nitride ceramic discs. The deposition value was 90 plus or minus 5 ohms per square. (This represented the lowest concentration available in a characterized process in the IC Production Facility.)
- (b) The base drive-in was carried out at a temperature of 1180 °C, as the spare isolation diffusion drive-in tube had to be used and was set at this temperature. The drive-in sequence was as follows.
 - One hour in dry oxygen to drive the junction uniformly in to about 4 μm without depleting the surface concentration rapidly and thereby causing large spreads in resistivity.
 - One hour wet oxidation to reduce the boron surface concentration for increased BV_{EBO} . (The partition coefficient favours an increase in boron concentration in the oxide rather than in silicon during oxidation processes. During wet oxidation the

boron is leached rapidly from the silicon surface.) After the significant drive-in of boron in the previous step, the subsequent wet oxidation process had little effect on boron concentration in the active region near the junction.

- Three hours in dry oxygen to drive the junction in to about $7 \mu\text{m}$.
- Fifteen minutes in dry nitrogen to reduce Q_{ss} .

As the base drive-in process was highly reproducible, variations in sheet resistivity were generally the result of variations in the boron deposition process. No provision was made in the drive-in step for varying the time of the wet process in order to modify the sheet resistance, as it was found that after the one-hour drive-in in dry oxygen, compensation in this manner did not necessarily modify the transistor gains in a predictable manner.

5.4.2 The emitter-diffusion process

The emitter-diffusion process was a compromise, as only one tube was available and it was desired to carry out the deposition and diffusion in a single step. To decrease phosphorus concentration, the measures indicated by Morris and Katz⁶⁰ were adopted as far as was possible. The purpose of reducing the phosphorus concentration was to reduce the density of diffused-in defects (DID) and emitter edge defects (EED) that can degrade the electrical properties of the emitter. Stojadinanovic and Popovic⁶¹ have indicated that an over-reduction in emitter phosphorus concentration can, whilst virtually eliminating DID and EED, result in reduced gains at lower values of collector current. However the method described by them for eliminating EED includes performing a shallow boron diffusion before the emitter diffusion, and was not suitable, as additional processing would have had to be added. Morris⁶³ emphasizes the importance of a slow cooling-rate after the emitter diffusion to optimize the gain of integrated injection logic transistors, as this considerably reduces the magnitude of edge dislocation grids (EDG) between the N+ and P diffusions.

The process adopted for emitter diffusion was optimized for a short deposition time in order to yield the lowest reproducible concentration of phosphorus from a liquid POCl_3 source, followed by a long drive-in time and

a slow cooling-rate. Figure 5.2a (page 190) shows the deposition sheet resistivity as a function of percentage of the oxygen carrier gas passed through the source bottle. From the flatter part of the curve a value of 16 per cent was used. Figure 5.2b (page 190) shows the deposition resistivity as a function of the deposition time, and here ten minutes was found to be adequate. In a separate study, carried out by Niewoudt⁶⁴ under the direction of the author, the emitter process was optimized for the production of the PT018 Darlington.

The following is a summary of the process sequence adopted.

- Load wafers into furnace at 1050 °C (later 1080 °C) over a period of 5 minutes, and allow to reach thermal equilibrium over a further 20 minutes in an oxygen atmosphere.
- Deposit phosphorus for 10 minutes.
- Drive-in for a pre-determined period derived from a test run using two 'pilot' wafers to obtain the correct gain.
- Remove wafers from furnace over a period of 15 minutes.

5.4.3 The post emitter-anneal process

Post emitter-diffusion anneal followed by the aluminium alloy process (described in Section 5.4.4 on page 192) are essential processes for the optimization of the properties of double-diffused transistors. One of the parameters most strongly influenced is normally device gain, and the discussion centres mainly on this.

It is standard practice to apply a thermal oxidation process during the emitter diffusion, and to follow this by a nitrogen anneal step at a lower temperature, typically in the region of 900 °C. This was the case for the NEERI integrated circuits and low-voltage transistors. Unfortunately in this process the oxide thickness over the emitter region was only slightly greater than 100 nm and highly phosphorus-doped, the latter being shown by the difficulty in controlling the rate at which this oxide layer was etched. A further problem was that considerable gain changes always occurred if the emitter-base junction was ever reverse-bias stressed.

FIGURE 5.2a EMITTER DEPOSITION PROCESS

Deposition sheet resistance, P_s , as a function of the percentage of total oxygen passed through the $POCl_3$ source bottle.

Substrate: 1 Ω . cm R-type, boron-doped
Furnace temperature: 1080°C
Deposition time: 10 minutes

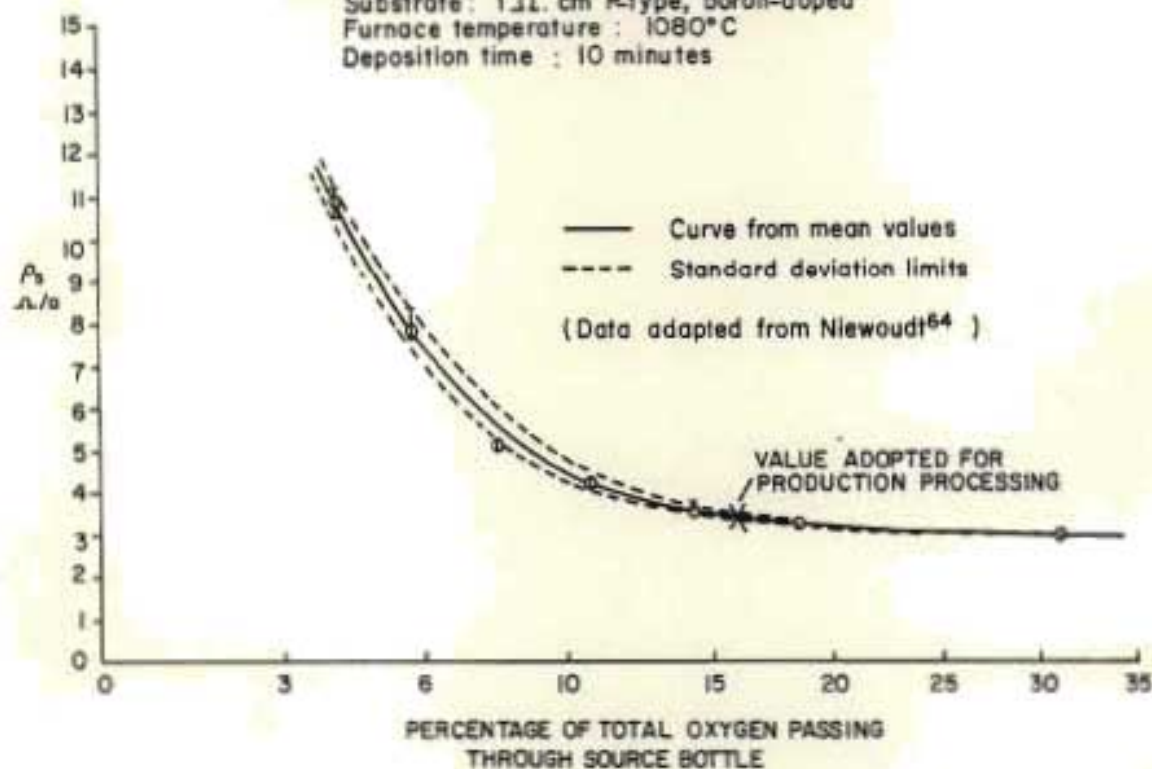
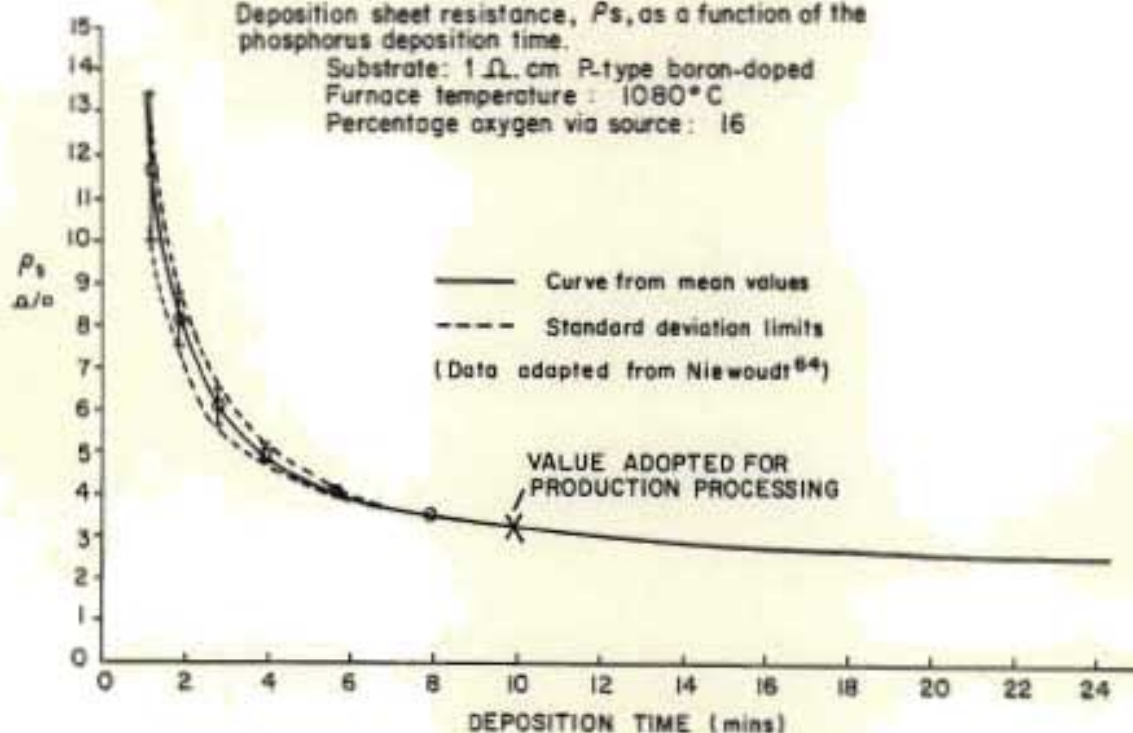


FIGURE 5.2b EMITTER DEPOSITION PROCESS

Deposition sheet resistance, P_s , as a function of the phosphorus deposition time.

Substrate: 1 Ω . cm P-type boron-doped
Furnace temperature: 1080°C
Percentage oxygen via source: 16



Note: For both curves

Wafer insertion time: 5 minutes
Thermal stabilization time: 20 minutes (before deposition)
Soak after deposition: 30 minutes

For the PT014 application susceptibility to reverse emitter-base bias stress was totally unacceptable, as the device might be subjected to reverse emitter-base bias stress when fitted to older telephones without a series diode in the base circuit.

In an effort to overcome both these problems, the author decided that part of the anneal cycle at 900 °C should be an oxidation step to provide a thicker oxide with a lower concentration of phosphorus that would etch in a controlled manner and would have good dielectric properties. Conventional thermal oxidation during this step was generally regarded as undesirable, owing to phosphorus pile-up at the oxide-silicon boundary (on the silicon side, as the partition coefficient favours this). Eernisse⁶⁵ has shown that for a process temperature of 900 °C oxidation can cause stress at the oxide-silicon interface, and it was conceivable that this stress combined with silicon lattice deformation due to pile-up could degrade transistor gain.

The approach adopted by the author was to add a wet oxidation step during the anneal process, as it was known that wet oxides are less dense and would therefore be more likely to take up this stress. This procedure would also cause a stable passivating layer to be grown, with a lower concentration of phosphorus. It was known from earlier experiments (Smithies⁷) that reproducible dielectric strengths of 6 MV/cm could be expected from such an oxidation process. A target oxide thickness of 0,5 µm was set, to provide an oxide dielectric capable of handling voltages of up to 300 V, in case more complex circuits with metal crossovers should ever be required.

Once again the importance of a slow cooling-cycle was taken into account to help anneal out dislocation grids at the end of the anneal cycle.

A summary of the wet oxide anneal process is given below.

- Slow insertion into process tube over 30 minutes in oxygen;
- dry oxidation for 30 minutes;
- wet oxidation for 60 minutes;
- dry oxidation for 30 minutes;
- dry nitrogen anneal for 30 minutes to reduce Q_{ss} (Smithies⁷);

- withdrawal in dry nitrogen over a period of 30 minutes.

At the end of the anneal process the phosphorus sheet resistance had increased by 10 to 20 per cent compared with the value measured immediately after diffusion, indicating that the wet oxidation did not result in further phosphorus being absorbed into the silicon. In addition the etching of the oxide has at all times been well controlled, indicative of a less than critical concentration of phosphorus in the oxide. The total oxide thickness was nominally 0,5 μm , and the dielectric strength, as measured on the #/118T test circuit (Figure 3.5a page 70), generally exceeded 7 MV/cm.

5.4.4 Sintering or alloying of the aluminium layer

The alloying step was vital in providing good ohmic contact to the diffused device, and the results of numerous experiments indicated that the gains measured before and after alloying increased by a factor of between 3 and 8. The mechanism of gain increase has been ascribed by Krishna⁶⁶ to a powerful scavenging effect produced by the alloying process.

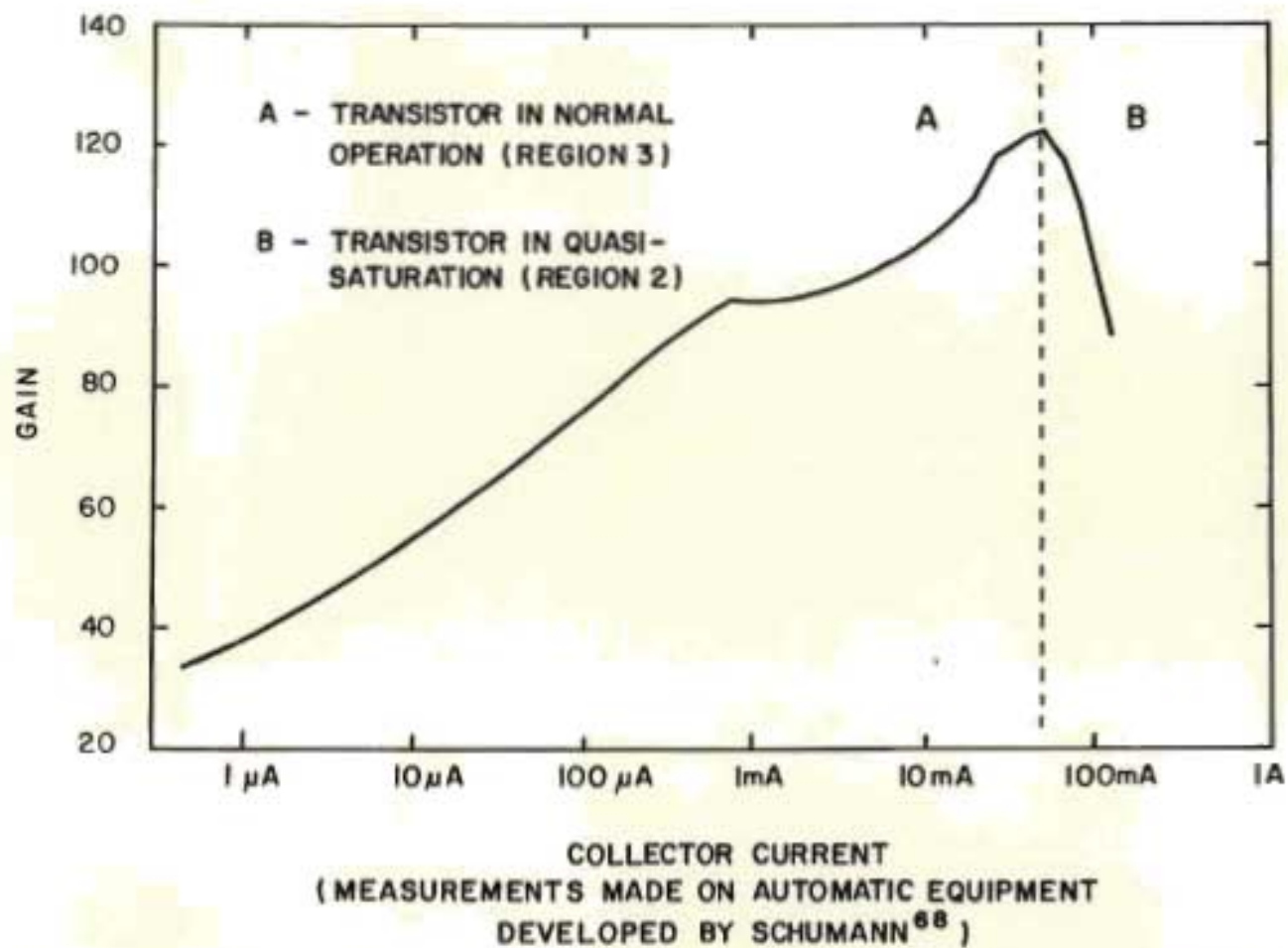
The alloy process adopted for the high-voltage transistors was one already available in the NEERI IC Facility, carried out at 500 °C for 15 minutes in nitrogen that had been bubbled through water at 25 °C.

The advantages of 'wet' sintering were investigated by Stulting⁶⁷, and in the case of the PT014 transistors it was found that the gains were boosted by 10 to 20 per cent when compared with the gains of those devices sintered in dry nitrogen.

5.4.5 Evaluation of PT014 devices produced with the new processes

Measurements made on PT014 devices showed that the gains were extremely stable, and not affected by reverse-bias stress on the emitter-base junction. Tests carried out on the equipment described by Schumann⁶⁸ for bipolar transistor parameter evaluation showed that despite the relatively large area of the PT014, the gain of the transistor dropped to 30 per cent of its peak gain at a collector current less than 1 μA , as shown in Figure 5.3 (page 193), this being an extremely small drop in gain for a device with an active area of approximately 0,45 mm^2 .

FIGURE 5.3 GAIN VS COLLECTOR CURRENT FOR A PTO14 AT $V_{CE} = 1V$



To reveal defects in the silicon, a wafer with a high yield of PT014 devices was stripped of aluminium in a mixture of concentrated sulphuric acid and hydrogen peroxide. Next, all the oxide was removed in a buffered oxide etch containing hydrofluoric acid, and then the whole wafer etched for 30 seconds in a 'Sirtl' etch consisting of a mixture of chromic and hydrofluoric acid. Figure 5.4a (page 195) shows the secondary electron image (SEI) of an area of a device extending from the emitter of a PT014 to the scribe channel. It can be seen that the scribe channel, where there was no boron diffusion but only phosphorus emitter diffusion for the equipotential ring, was singularly free of defects. The emitter region, however, shows a very high density of defects, but these tend to disappear towards the edge of the emitter in the region that remained under the thermal oxide. Figure 5.4b (page 195) shows an electron micrograph made in two sections, the first of which is a standard SEI picture and the second an electron-beam induced contrast (EBIC) image. When the SEI and EBIC images are compared it is quite clear that there is significant lateral diffusion of the emitter into the base region and that in this case the defects shown in Figure 5.4a would not reach the emitter edge. That these defects were not emitter edge defects and that they were not electrically active was supported by the finding that the device exhibited good gain properties at low collector currents.

The origin of the defects was something of a mystery. They were absent in the scribe channel, where there was no boron diffusion, and yet they also tended to disappear under the thermal oxide in the emitter region, where no aluminium was present. It was concluded that the aluminium alloying process had played some part in the formation of the defects, a view that has not been offered elsewhere in the literature. As the devices performed admirably, further investigations to substantiate this effect await a more convenient opportunity.

Summarizing Section 5.4, it may be said that the process technology developed for the PT014 and later used for the PT018 was highly successful, and specifically the wet oxidation anneal procedure vital towards producing high-stability devices, with minimal parametric deviation after any electrical stress.

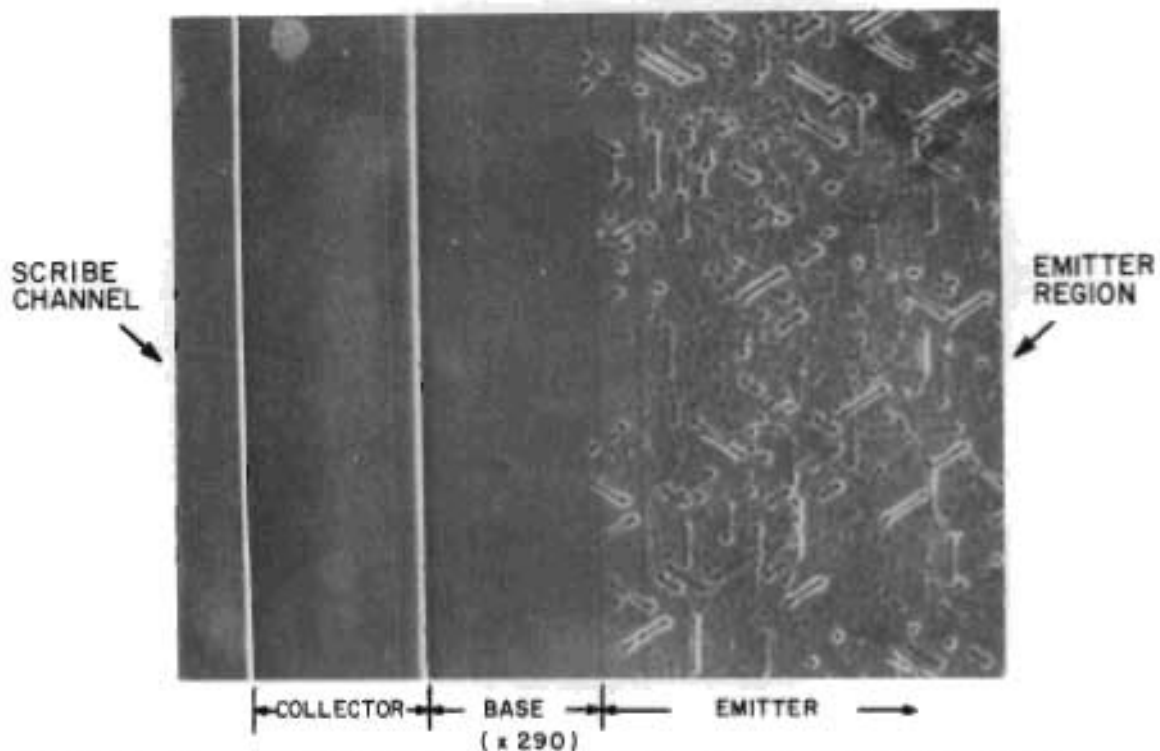


FIGURE 5.4a SECONDARY ELECTRON IMAGE (SEI) OF A SIRTLETTED $\ast/014$ TRANSISTOR. THERE IS A HIGH DENSITY OF DEFECTS IN THE N^+ EMITTER REGION BUT NO DEFECTS ARE VISIBLE IN THE N^+ SCRIBE CHANNEL.

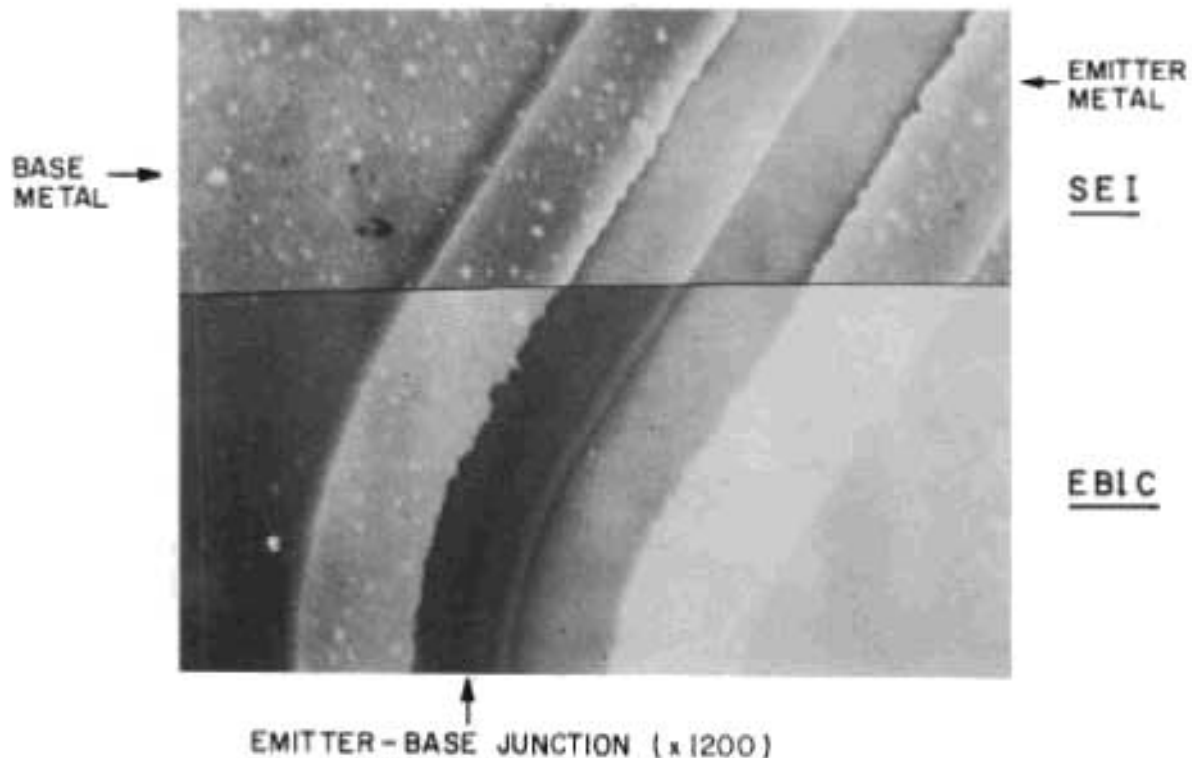


FIGURE 5.4b SEI AND ELECTRON-BEAM INDUCED CONTRAST (EBIC) IMAGE OF THE EMITTER-BASE REGION OF A $\ast/014$ TRANSISTOR. THE JUNCTION IS SITUATED ABOUT $6 \mu\text{m}$ BEYOND THE DIFFUSION MASK INTO THE BASE REGION. EMITTER DEFECTS DO NOT EXTEND THIS FAR.

5.5 TRANSFER OF THE PROCESS TECHNOLOGY AND INDUSTRIALIZATION

5.5.1 Precedents for production activities within the CSIR

By its fundamental terms of reference the SA CSIR was not established with the aim of mass-producing high-technology items. Only in the case of the SA private sector not being in a position to produce a specific product essential to the economy of the country, would the CSIR consider production if the resources were available. This was the case with the PT014 and PT018.

5.5.2 Earlier experiences with technology transfer

The author had experience of two efforts aimed at the transfer of technology for microcircuit production, one successful and the other much less so.

The former exercise was the transfer of the technology for the production of bipolar integrated circuits from the United Kingdom to NEERI. This was commenced in 1974 and the author⁶⁹ was involved in early planning work. By 1978 stable production of the bipolar integrated circuits had been achieved.

In the opinion of the author, the success of this transfer was due to the dedicated involvement of three individuals seconded to the project. The first was a management specialist, the second a technologist familiar with the process technology, and the third a quality assurance officer who was familiar with the screens used for the particular production activity. Undoubtedly the most difficult task of adaptation in the whole undertaking was that of comparing the goals of a Civil Service style laboratory management and administration system with needs of a successful production operation, and matching the two.

The task of transferring the technology for an integrated injection logic (I²L) process from the laboratory into production in the NEERI IC Facility was accomplished less well, despite the important impact that a success would have had for local designers. Although the process technology developed in the laboratory was highly successful, the technologists

concerned with the transfer, having no stipulated pre-requisite requirement for a commercial success of the venture, carried out their task on a non-dedicated basis, and the time spent could rather have been classed as a part-time charitable effort.

5.5.3 Transfer and industrialization of the high-voltage transistor process

Although the author was a laboratory staff member, lacking training in production disciplines, the transfer procedure of the high-voltage transistor process was undertaken with complete dedication.

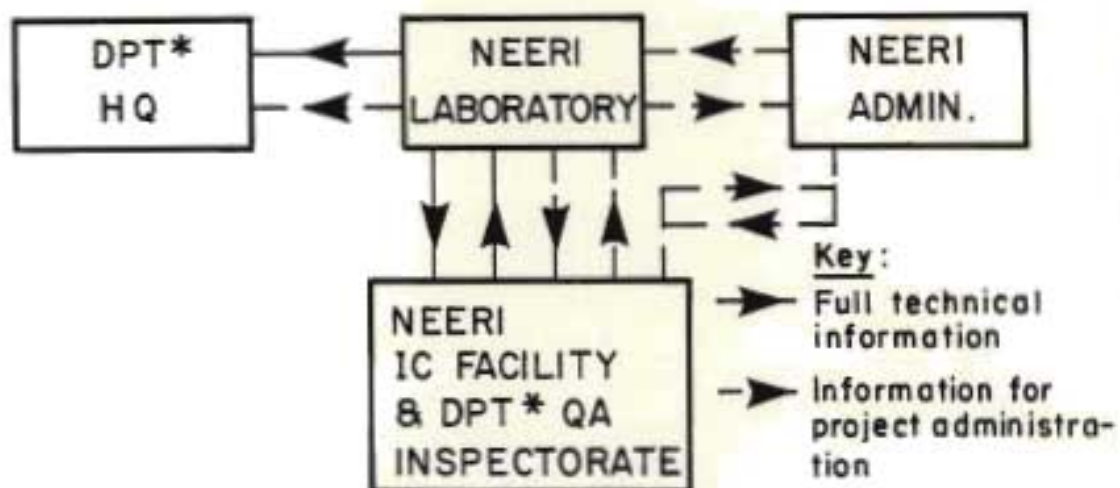
However, it was far easier to find weaknesses in the production environment than it was to make constructive suggestions for improving procedures, but armed with an understanding of the problems that existed in the production system it was possible to tackle each one as it arose.

At the outset a number of important principles, detailed below, were adopted in the transfer exercise.

- (a) There should be no interference with any existing production procedures and screening techniques. Existing processes and screens should be used where applicable, new ones being added only where essential.
- (b) Communication based on the usual hierarchical system typical of a Civil Service-type operation was improved by adopting a 'Lateral Information' flow scheme aimed at keeping all individuals, whether directly or indirectly involved in the transfer, rapidly informed and fully abreast of current status. Figure 5.5 (page 198) shows the flow pattern of information during the development and transfer phases of the project.
- (c) End user involvement was encouraged, and the Quality Assurance Section of the the Department of Posts and Telecommunications became actively involved and seconded two technicians to assist with the transfer operation.
- (d) Provisional specifications for use during the transfer phase were prepared for each step. Written communications were found to be vital, and were employed for communications of any nature. In the the interests of speed, which was an important factor, copies of handwritten memoranda were distributed to all parties.

FIGURE 5.5

INFORMATION FLOW DURING TECHNOLOGY TRANSFER
AND INDUSTRIALIZATION PHASES



COMMUNICATION Regular written communications and informal meetings played a vital role.

Most concentrated communication between:

NEERI: Micro-electronics Dept, Technology division and

1. IC Facility — Management
— Engineering
— Quality Assurance
— Production
— Test section

2. DPT* — QA Inspectorate
(2 seconded officers).

* DEPARTMENT OF POSTS AND TELECOMMUNICATIONS

- (e) A policy was adopted excluding virtually all intervention by laboratory staff in process operations after these had been instituted for production. This rule was deviated from only when help was specifically requested or data had to be gathered leading to the setting-up of production guidelines.
- (f) Continuous interaction was maintained at the quality assurance and process engineering levels in order to monitor progress of the transfer. The production supervisory staff, when unable to attend the regular informal discussions, were again kept informed of progress by short handwritten memoranda. During the early production phase, more active communication with the production supervisory staff was encouraged.
- (g) The final Production Process Specifications, binding on all production stages, were issued only after four months of early production had been completed successfully.

5.5.4 Fundamental issues hindering the technology transfer undertaking

The views given in this section are purely those of the author and were arrived at after due consideration.

Perhaps the factor influencing most negatively the whole transfer and production exercise in the NEERI IC Facility was the circumstance that the operation was being handled in an environment where financial viability was considered of secondary importance as compared with simply the capability of fabricating microcircuits. In addition, the benefits derived by the IC Facility from implementation of the two highly successful transistor production programmes were too few. Some of the benefits are listed below.

- (a) The additional income generated from the sale of transistors slightly increased bargaining power when additional funds were requested with the aim of updating technology.
- (b) The constant base load had the effect of stabilizing processes.
- (c) A wider range of components could be manufactured.

Listed below are various factors, negative in the opinion of the author, that became obvious during the evolvement of the high-voltage transistor programmes.

- (a) During the transfer phase the number of qualified staff in the IC Facility was only just sufficient to carry out the necessary operations, since there was no redundancy in respect of staff capabilities. Operations were held up when certain key staff members were absent.
- (b) The whole development and transfer operation took place under conditions that made impossible the implementation of more advanced processing techniques.
- (c) Numerous facilities, highly desirable for the operation, were either inadequate or totally lacking.
- (d) The fact that the production of transistors involved additional work from the same number of staff members appeared, in the eyes of the author, not to be uniformly welcomed, particularly by employees without special skills, who were offered no specific incentives to spur them to greater efforts.
- (e) Although two successful and financially viable transistor production programmes had been evolved, the achievement did not appear significantly to influence the possibility of gaining authorization for any expenditure incurred towards improvements to the laboratory and manufacturing facilities. The author subscribes most strongly to the view that policy in this respect should be favourably reviewed.

Despite these observations the author is pleased to record that success was ensured by the selfless assistance and interest of the key individuals involved in the projects, from the NEERI Directorate down.

5.6 DATA MANAGEMENT

5.6.1 Objectives of Data Management

In undertaking this study associated with the PT014 project, the author set the following overall objectives for Data Management.

- (a) It had to be ensured that the components supplied met programme requirements.
- (b) In order to achieve early production maturity, data enabling enabling effective corrective action to be taken without delay, had to become available in time.
- (c) Methods of recognizing trends should be improved, making it possible for management to take the right action at the appropriate time.
- (d) Data management should act as a barometer for the quality and reliability of a product.
- (e) Data management should provide a historical data base making possible reliable costing and reliability prediction for a device.
- (f) Data management should provide a data reduction service enabling the most relevant data to be presented in an easily understandable form.
- (g) Production problems should be pinpointed and highlighted, and their probable effect indicated.
- (h) Changes of output quality or quantity should be correlated with historical factors such as the use of new or modified processes, the use of different batches of process materials, and even staff matters.

5.6.2 A data management exercise using test data from the PT014 programme

Data management through most of the PT014 project was either non-existent or only incompletely handled. The author initiated an investigation to demonstrate how the vast accumulation of electrical test data could be used to optimize the cost-effectiveness of the programme, and he wishes to express his gratitude to Mr F Schocmbie of the Department of Posts and Telecommunications for the collection of data necessary for the following analysis.

Table 5E (page 202) shows the summary of tests on a single wafer from a batch of ten, and Table 5F (page 202) shows the analysis presented for each batch by the quality assurance officers of the Dept of Posts and Telecommunications. At the wafer probe level, the key tests that were failed are clearly shown, and the batch analysis is simply the average for the whole batch. This first stage of data reduction totally eliminated one key item

TABLE 5E : SUMMARY OF RESULTS OF A PROBE TEST ON A PT014 WAFER
(Computer output)

CIRCUIT TESTED :	TR2 (* / 014)	DATE:	81/08/13				
TEST SPEC. :	PT014	PROBE TEST ISSUE:	1				
BATCH/WAFER :	924/WAFER-10						
PACKAGE :	WAFER						
TESTED BY :	S VENTER						
STATISTICS							
NUMBER OF DEVICES TESTED:	99						
PASSED:	80						
FAILED:	19						
YIELD:	81 %						
TEST NO.	MIN.	MAX.	MEAN VALUE	STD DEV.	PARAMETER		
1	86,39	155,64	98,21	9,15	HFE(1)		
2	73,26	139,86	86,42	8,17	HFE(2)		
3	204,50	205,00	204,54	0,13	BVCEO		
4	205,00	210,00	205,50	1,50	VCBO		
5	9,97	10,24	10,21	0,06	BVEBO		
6	0,46	0,73	0,65	0,07	VCE(SAT)		
7	2,17	3,03	2,62	0,19	VCEK		
FAILURE ANALYSIS							
TEST NUMBER	NUMBER FAILED	PER CENT OF FAILURES					
		0	20	40	60	80	100
		I +	I +	I +	I +	I +	I
1	7	I*****					
2	10	I*****					
3	2	I****					
4	0	I					
5	0	I					
6	0	I					
7	0	I +	I +	I +	I +	I +	I

TABLE 5F : BATCH ANALYSIS OF THE DEPT OF POSTS AND TELECOMMUNICATIONS

DATE	:	82/8/26
BATCH	:	924
WAFERS	:	10
YIELD (%)	:	51,6
(Note : Results below are failure percentages)		
1-HFE(1)	:	20,6060%
2-HFE(2)	:	22,9292%
3-VCEO	:	2,32323%
4-VCBO	:	0,10101%
5-VEBO	:	0%
6-VCE(SAT)	:	1,81818%
7-VCEK	:	0,10101%
DIE TESTED	:	990

of information, viz the very large spread of wafer yields in the batch. Figure 5.6 (page 204) shows that wafer yields varied enormously within the batch, ranging from about 10 per cent to about 80. This observation had not been made during the production of the first half-million transistors, and it was the first indication of any problems in the area of process control.

To provide a more meaningful first reduction in data, the batch test was repeated to give the total number of failures for all parameters. This was done because the test was normally stopped as soon as a parametric failure had been encountered, and hence the figures for percentage rejects shown in Table 5F (page 202) do not give a true picture of the situation. Figure 5.7 (page 204) shows these new results, and it is immediately obvious that the major problem in process control was a reduction in the gain spread alone.

During the next stage in the investigation the batch yields were plotted as a function of time. Figure 5.8 (page 205) shows the wildly varying yields obtained from 158 batches comprising 1058 wafers that were shipped for assembly. Viewed by themselves, the batch yields are difficult to interpret; however, the superimposed average yield curve is enlightening. Until the end of October 1980, after which time Laboratory and Post Office staff were no longer directly involved with the production activity, the batch yields increased and then stabilized at about 60 per cent. Thereafter the process was under the entire control of the IC Facility and the average yield began slowly to decrease, stabilizing at about 37 per cent only after almost two years had passed.

When the total number of batches processed was compared to the number of wafers shipped, it was clear that a large number of wafers were being 'lost' during production and testing. Figure 5.9 (page 205) shows that only 9 per cent of the wafers were lost in processing, a perfectly acceptable figure. However at testing, where a lower yield-limit of 10 per cent was required for the wafer to be shipped, the total wafer mortality increased to 33 per cent. The major implication from this finding was that the cost of manufacturing a transistor was considerably higher than had been originally anticipated. In addition, the earlier conclusion that process control required attention was reinforced. After the process problems had been isolated, rigorous action was instituted by the IC Facility to improve the base deposition process, and the emitter diffusion process was revised by Niewoudt⁶⁴ of the Laboratory staff. These measures had the desired effect of reducing the proportion of rejected wafers to about 10 per cent.

FIGURE 5.6 YIELD DISTRIBUTION WITHIN A TYPICAL BATCH

BATCH 924
 PROBED AT NEERI
 DATE 1982/08/13

AVERAGE YIELD: 51,6 %
 BATCH SIZE : 10 WAFERS
 NUMBER OF DIE TESTED : 100/WAFER

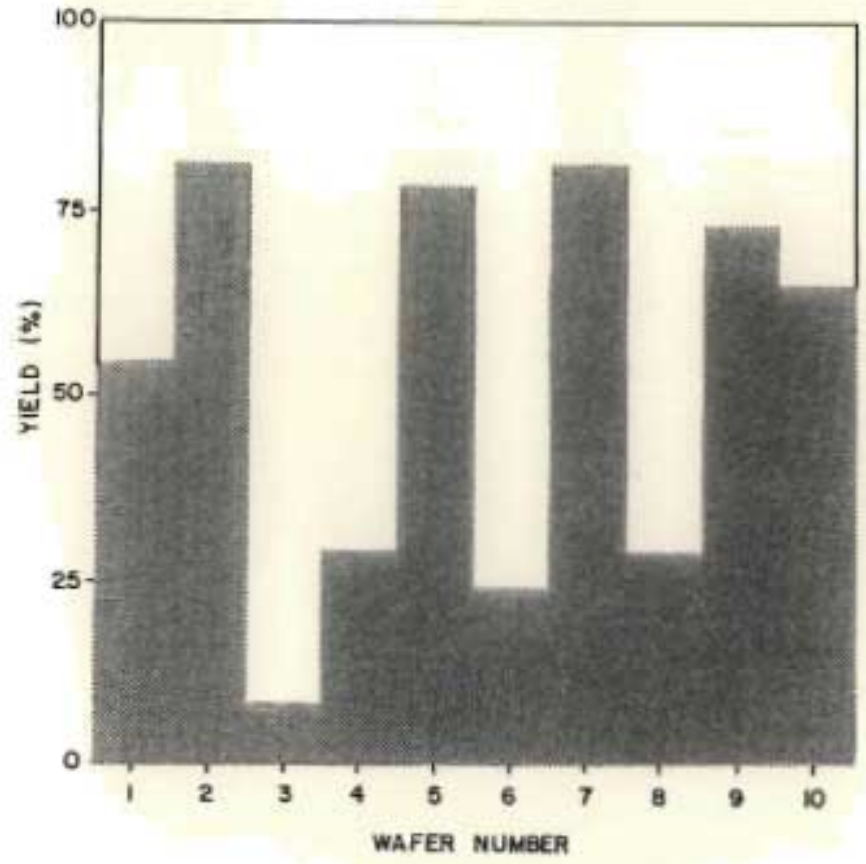
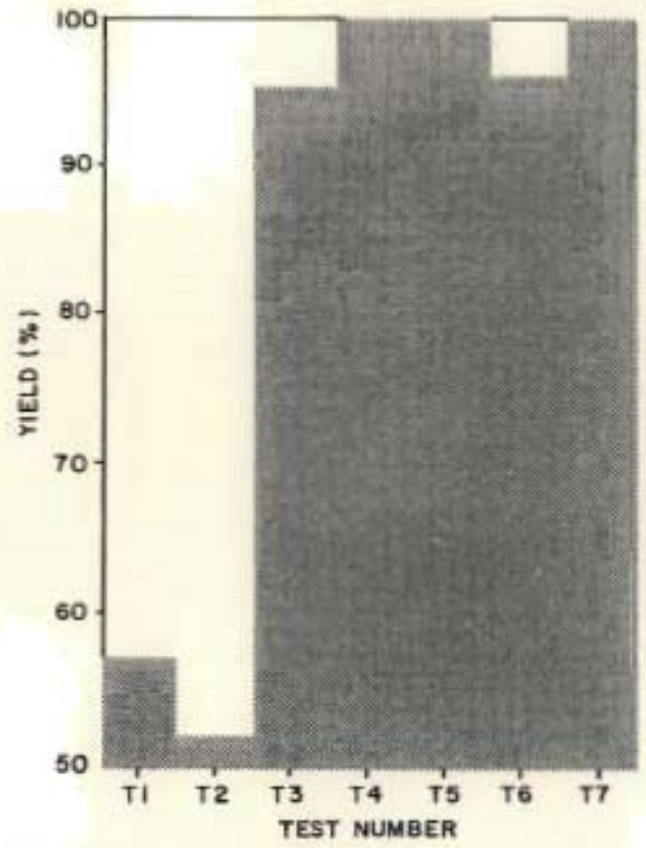


FIGURE 5.7 MODIFIED BATCHYIELD ANALYSIS: YIELD VS TEST

BATCH 924 (OTHER DATA AS FOR FIGURE 5.6)
 (THIS FIGURE GIVES THE TOTAL YIELD ON EACH TEST FOR ALL DEVICES PROBED)



Test identification: T 1 - $h_{FE(1)}$ T 4 - BV_{CBO}
 T 2 - $h_{FE(2)}$ T 5 - BV_{EBO}
 T 3 - BV_{CEO} T 6 - $V_{CE(SAT)}$
 T 7 - V_{CEK}

FIGURE 5.8 BATCH YIELD AS A FUNCTION OF BATCH (TIME) FOR * /014 TRANSISTORS

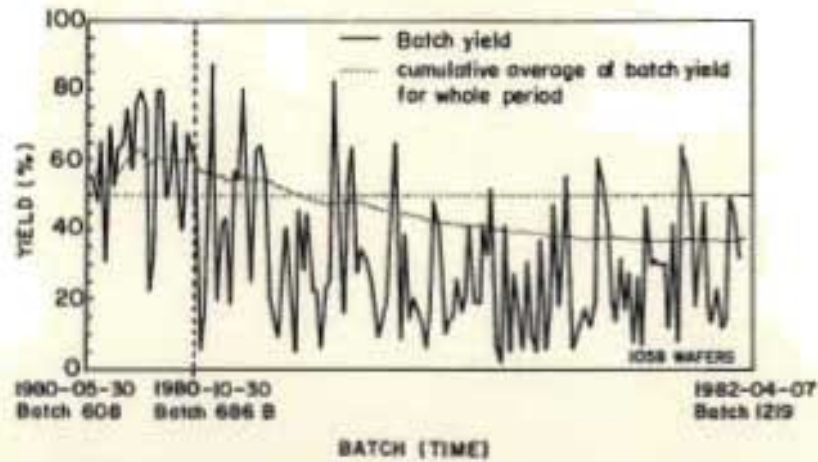
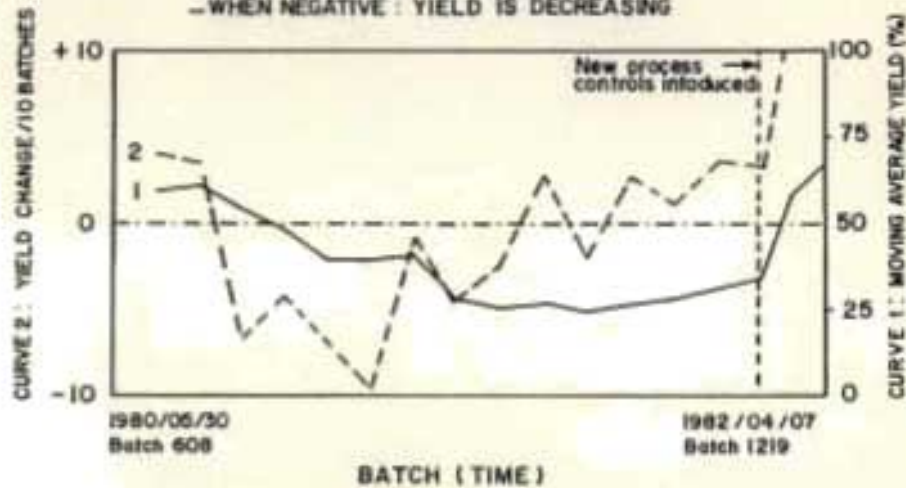


FIGURE 5.10 A SENSITIVE TEST FOR TRENDS IN YIELD

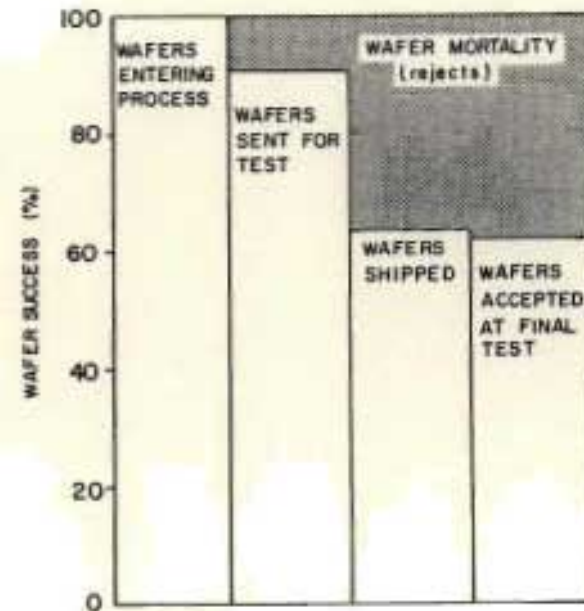
CURVE 1 : MOVING AVERAGE YIELD*
 CURVE 2 : FIRST DERIVATIVE OF CURVE 1 W.R.T. BATCH
 - WHEN POSITIVE : YIELD IS INCREASING
 - WHEN NEGATIVE : YIELD IS DECREASING



(* INTERVAL = 20 BATCHES = 220k DIE: PLOTTED FOR EACH INCREASE OF 10 BATCHES)

FIGURE 5.9 WHERE WAFERS WERE REJECTED

How the number of wafers starting process were reduced by accept/reject steps and breakages before reaching final assembly



5.6.3 A test for early warning of reduced yields

In this section a more sensitive test is described that was developed to provide an early warning of deviations or trends in yields. The data provided in Section 5.6.2 are used in the demonstration of the technique.

Figure 5.10 (page 205) shows two curves. The first is a moving average yield of the data presented in Figure 5.8 (page 205). The yield was averaged over 20 batches and has been plotted for each increment of 10 batches. This gives a better indication of progress than the cumulative average curve presented in Figure 5.8 (page 205), and shows that a small upswing in yield occurred towards the end of the two-year period.

The first derivative of the moving average, as shown in Figure 5.10 (page 205), provided an extremely sensitive test for the trend in yields. When points on this curve are below the abscissa, the yield is dropping, and when above the abscissa, the yield is increasing. The sharp rise of both curves at the end of the two-year period was the result of the improvements introduced in both the base and emitter processes.

5.6.4 Use of Data Management on a wider scale at NEERI

The analyses of test data presented in Sections 5.6.2 and 5.6.3 could well have been applied within six months of the commencement of production of the high-voltage transistors, with the result that negative trends would have been observed. More consistent recording of data on each high-voltage device type was instituted, making it possible to observe trends with considerably more success.

The above section gave an example of a specific case of the successful use of data management techniques. In the view of the author, the wider use of data, already available on a very broad base as part of the production activity, coupled with appropriate reduction and visibility enhancement procedures, will be essential steps if the success of future production programmes is to be ensured.

5.6 CONCLUSION

Chapter 5 has described the wide base upon which the transistor development projects were handled. Process development followed the critical analysis of available and required facilities. In addition considerable assistance was lent to activities outside the CSIR that were beyond the scope of the project as originally defined. These activities contributed materially to the outstanding success achieved.

Process development has shown that carefully considered use of classical processing techniques can yield devices exhibiting outstanding stability when subjected to stress conditions. In addition, experimental results indicate that there is a possibility that the aluminium alloying process may be associated with non-electrically active emitter defects.

It became evident that during the transfer and industrialization of the process technology regular and direct 'lateral communication' of copies of handwritten information to all parties involved was important, in that interest and a feeling of involvement were maintained, these being among essential factors ensuring the success of this operation.

A vivid example was given of the importance of the use of data management techniques in highlighting production problems, and this investigation has led to the more systematic and analytic use of electrical test data.

Whilst the author took the initiative in instituting the measures noted in this chapter, the co-operation of numerous colleagues and associates, freely given, was essential to the success of the undertaking.

CHAPTER 6

A POSTSCRIPT : FURTHER DIRECTION FOR RESEARCH IN HIGH-VOLTAGE DEVICES

6.1 SUMMARY OF CHAPTER

This chapter presents some thoughts, substantiated by measurements already made, on possible future developments in high-voltage devices that could be applicable to the telecommunications industry in South Africa.

6.2 SURGES ON TELEPHONE LINES : A PERSONAL EXPERIENCE

On a January day in 1967 the author was ankle-deep in swamp water repairing a fallen telephone line, about 50 km from the rural settlement of Mulobezi, in Zambia. Despite the cloudless sky, jolt after jolt of static electricity induced in the line made repair work both painful and slow.

The telephone line was some 200 km long and consisted of a single conductor, the earth being used as the return circuit. To counter high background noise and significant line attenuation, amplifiers using the latest high-voltage transistors had been fitted to the microphone circuits of each telephone in the system. Within a few weeks all the amplifiers had been put out of action by line surges, and the whole system was rendered useless. This lesson imprinted on the author's mind the direct incompatibility of standard semiconductor devices and significant lengths of conducting lines.

6.3 THE PRESENCE OF SURGES IN MODERN TELECOMMUNICATION SYSTEMS

Today, telecommunication systems are a far cry from the simple installation described above. In the Republic, the major trunk routes are handled by microwave systems, and in the not too distant future the optical fibre link will do much to reduce the proportion of conducting connections between metropolitan exchanges. Optical links to subscribers, capable of handling considerable volumes of data, or installed for other purposes, such as video, are fast becoming a reality. Despite the advance of optical techniques, conducting links predominate at present, and very many existing routes will be optimized with the aid of digital techniques.

Prinn⁷⁰ has measured the magnitude of surges on underground cables, and Debbo⁷¹ has shown that whilst surges may be non-destructive to the electronic systems in use for pulse code modulation (PCM) links, these systems have to be so designed that interference with the digital signal does not cause data corruption. The author did not pursue the matter of surges on inter-exchange links, as local data were still being gathered. However the large-scale production of standard telecommunications cables has shown no decline (Brice, pers. comm.⁶) and it may be logically concluded that for many years to come the necessary overvoltage protection for surges arising on the link between electronic exchange and subscriber will be required.

6.4 SURGE CONDITIONS ON THE SUBSCRIBER LOOP

The author addresses this chapter to the problems associated with surges on subscriber loops, about which considerable information was accumulated as a result of the investigations carried out for this thesis. From both personal experience and interaction with the staff of the Department of Posts and Telecommunications it was known that in this country the protection of electronic systems in these loops presented severe problems, and that damage to telephones due to surges was commonplace. Before returning to the development of devices for the protection of electronic telephones, the status of high-voltage technology for electronic exchanges is reviewed briefly.

In other parts of the world, the advent of the fully electronic digital exchange with analogue subscriber lines has in no way affected the need for semiconductor devices capable of blocking high voltages. Ballantyne⁷² has stated that integrated circuits for switching subscriber lines in the USA should be able to withstand surges of up to 530 V. In Japan, Kawarada et al.⁷³ have developed receive-transmit (RT) interface circuits capable of blocking 320 V surges. According to Ballantyne et al.⁷² there is a need for the ability to block these high-voltage levels because 'Protector devices in the central office limit the voltages, and decrease - but do not eliminate - the currents resulting from these surges'. The figure of 530 V given by Ballantyne et al.⁷² is entirely in line with the experience of Parsley⁴⁰ and the author³⁹, according to which gas arresters, rated at 350 V and capable of sinking surges as high as 10 kA, could take more than 1 μ s to strike, whilst short-duration voltages approaching 500 V were recorded during tests.

As the RT interface circuits must be able to conduct in both directions owing to the use of AC signalling, gated diodes with 'on' resistances as low as 5 ohms are commonly used in parallel but reversed pair configuration, one pair for the forward line and another for the return line. In order to integrate these devices, an oxide isolation technique is employed, and an example of a gated diode is shown in Figure 6.1 (Page 211). In this case a total of four identical diodes would make up the RT switch. The gated diode is kept turned off with the application of a high voltage to the gate electrode. To connect a loop, the gate bias voltage is reduced so that the diodes are turned on to give a low-impedance path between the subscriber line and the subscriber line interface circuit (SLIC). Danneels et al.⁷⁴ have demonstrated that the SLIC can include protection against sinking or sourcing of excessively high currents. With the RT circuit switched on, the SLIC must be protected from transient overvoltages by the addition of extra protection circuitry, either included as an additional discrete component, as described by Smithies³⁹ for the LS5000 type 'crowbar' device, or possibly integrated into the RT switch. In view of this Ballantyne et al.⁷² indicate that it is necessary for the RT switch to be able to withstand short, high-current surges. In Section 6.7 is discussed a possible means of overcoming this problem, which places physical limitations on the minimum size of both the RT circuit and the size of bonding wires that must be used.

6.5 APPLICATION OF NEGATIVE-RESISTANCE DEVICES

Whilst no local technology is available for manufacturing oxide-isolated switches, an important contribution to high-voltage switch technology, with immediate application to telephone protection, could nevertheless be made if devices exhibiting negative-resistance characteristics were employed.

Four different new devices with negative-resistance characteristics at high voltages have been reported on by Fursin⁷⁵, Wu and Lai⁷⁶, Wu and Wu⁷⁷ and Galuzo and Matson⁷⁸. Of these four devices, the 'Lambda Bipolar Transistor' (LBT) described by Wu and Wu⁷⁷ is of direct application.

Figure 6.2a (page 213) shows a section of an LBT, and it is clear that the device could be made in standard bipolar transistor technology. In this transistor the two emitter diffusions form the source and drain of

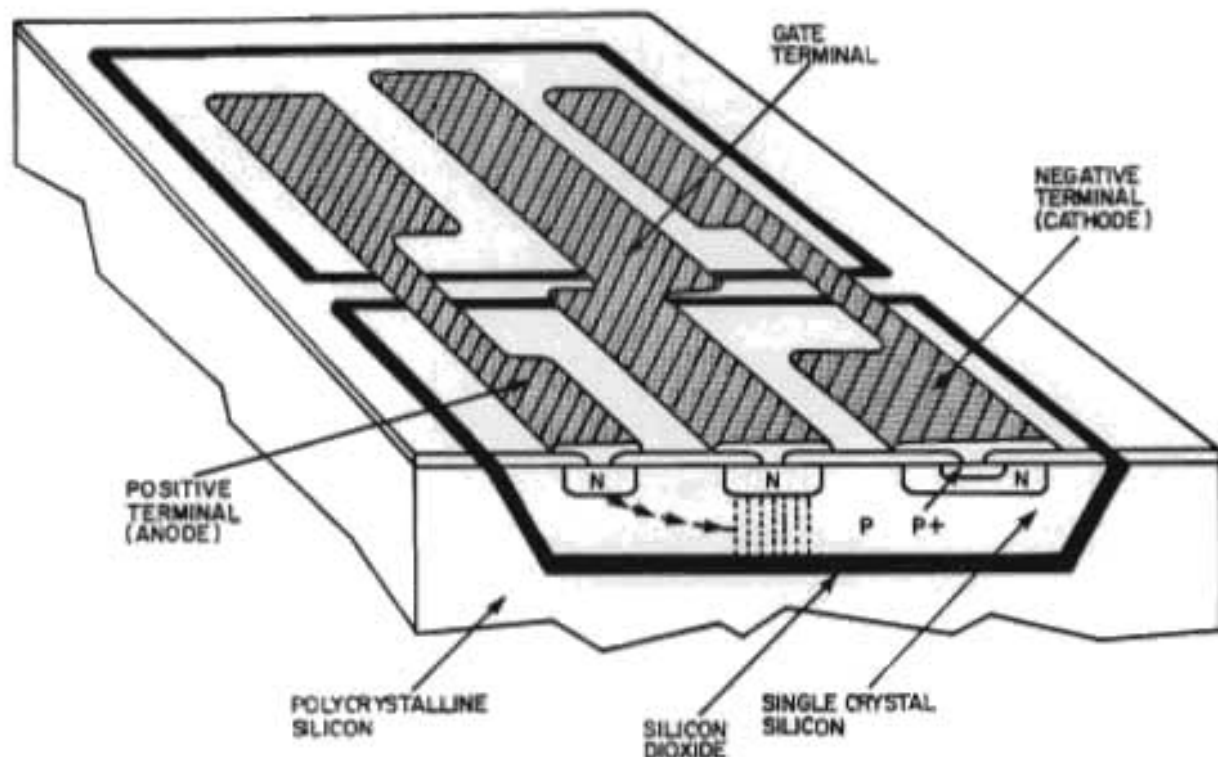


FIGURE 6.1 THE GATED DIODE SWITCH

A cross-section of the gated diode switch, as presented by Ballantyne et. al⁷². The switch is fabricated using oxide isolation (OXIS) technology with islands of P-type silicon surrounded by an isolating layer of silicon dioxide, all buried in a polysilicon substrate. The dielectric strength of the isolation oxide exceeds 600 V. To provide conduction in both directions, pairs of diodes are connected in parallel but are reversed with respect to each other.

The diode is similar to an N-P-N-P four-layer diode, but unlike a thyristor it is normally conducting. To keep the diode 'off', a high positive voltage is maintained on the gate electrode, and this depletes the conducting channel between the anode and cathode diffusions. To switch the diode on, the gate electrode voltage is reduced.

a field-effect transistor. The gate is held at collector potential, and as the collector voltage increases, the P-base region under the gate is inverted to form an N-channel between the source and drain. This has the effect of passing base current into the emitter circuit and turning the device off. The equivalent circuit of the LBT is shown in Figure 6.2b (page 213), and the collector characteristics are shown in Figure 6.2c (page 213).

Clearly, a device with these properties would have immediate application in the Disa telephone, where current is being passed through the O.N. Darlington in the off-hook condition. Parsley⁴⁰ has shown that failure of this device can occur with applied surges of less than 350 V.

In an experiment conducted at Potelin the author showed that a 100 pF capacitor connected from the positive side of the bridge circuit in the Disa telephone to the base of the transistor TR6, in the dial circuit, would turn off the O.N. transistor for the duration of the surge, thus preventing failure of the Darlington. Figure 6.3 (page 213) shows key components in this protection scheme. (A more complete circuit diagram of the dial was given in Figure 3.3, page 65.)

An LBT Darlington could, in principle, form a direct replacement for the PT018 and would involve no engineering changes to the actual telephone. The author undertook a series of experiments to evaluate the use of a simulated LBT in the telephone. Figure 6.4a (page 214) shows the circuit used to simulate an LBT, and Figure 6.4b (page 214) shows the electrical characteristics of the circuit, which indicate that the device turned off rapidly at about 80 V. When tested in the O.N. and impulsing stages of the telephone dial, no impairment of telephone operation was detected. It was, however, possible to subject the telephone to sustained high voltages of up to 350 V without any damage to either of the modified Darlington.

Only one possible drawback of this circuit was obvious, it being possible to destroy PT018 Darlington transistors by running them at collector currents approaching 1 A at a collector-emitter voltage of 50 V. This was not a condition that could be induced in the telephone, as the drive currents to the bases of both the O.N. and impulsing Darlington were limited, but it could be a consideration in other applications. Figure 6.4c (page 214) shows a circuit that limited the collector current to about 160 mA. This circuit with both a negative-resistance and current-limiting characteristic was found to operate well in the telephone, and it was not

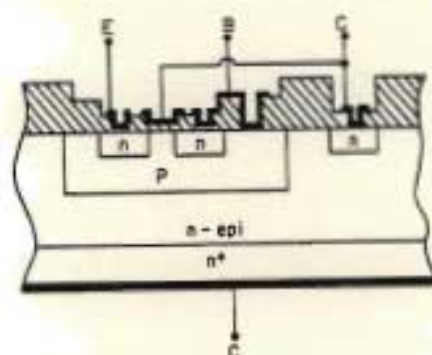


FIGURE 6.2a

THE BASIC DEVICE STRUCTURE OF AN NPN LAMBDA BIPOLAR TRANSISTOR
(AFTER WU AND WU⁷⁷)

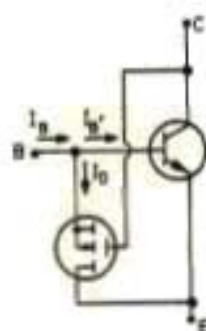


FIGURE 6.2b THE EQUIVALENT CIRCUIT OF A LAMBDA BIPOLAR TRANSISTOR. AS V_{CE} INCREASES, I_D INCREASES AND REDUCES THE BASE CURRENT I_B , THUS IMPARTING THE NEGATIVE RESISTANCE CHARACTERISTIC

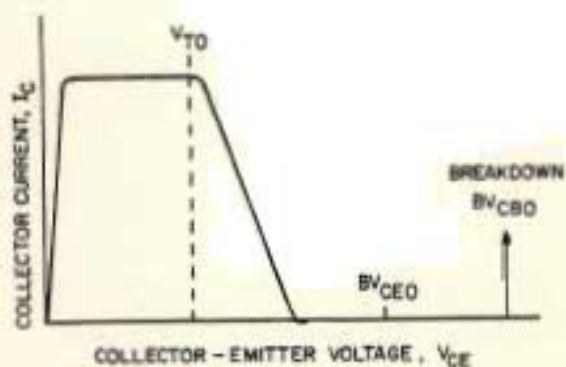


FIGURE 6.2c COLLECTOR CHARACTERISTICS OF THE LAMBDA BIPOLAR TRANSISTOR. BELOW V_{TO} THE CHARACTERISTICS ARE IDENTICAL TO A STANDARD BIPOLAR TRANSISTOR AND ABOVE V_{TO} THE COLLECTOR CURRENT DROPS. BREAKDOWN IS HIGHER THAN BV_{CEO} AND APPROACHES BV_{CBO} .

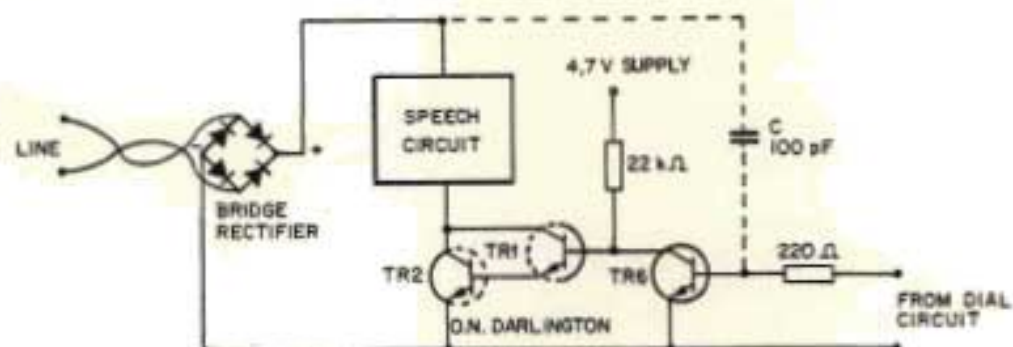


FIGURE 6.3 SURGE PROTECTION OF THE O.N. DARLINGTON BY THE ADDITION OF THE 100 pF CAPACITOR, SHOWN IN THE DOTTED LINE PART OF THE CIRCUIT. IN THE PRESENCE OF A RAPIDLY RISING SURGE ACROSS THE TELEPHONE, THE CURRENT VIA C TURNS ON TR6 WHICH TURNS OFF THE O.N. DARLINGTON, COMPRISING TR1 AND TR2.

FIGURE 6.4 a

CIRCUIT USED TO SIMULATE THE LAMBDA BIPOLAR TRANSISTOR.

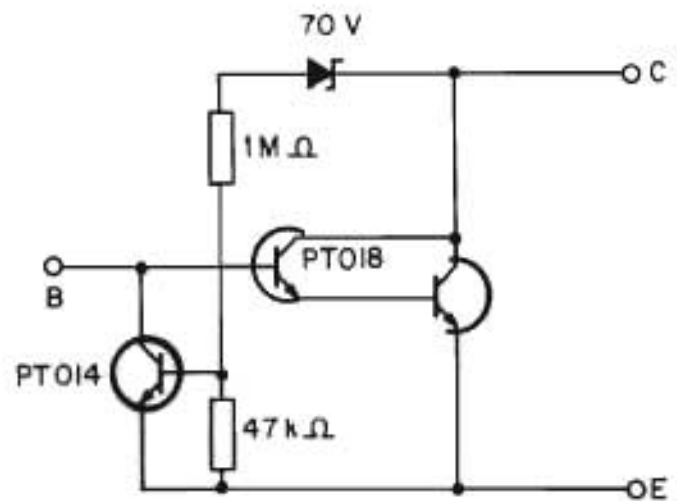


FIGURE 6.4 b

COLLECTOR CHARACTERISTICS SIMULATED BY THE CIRCUIT IN FIGURE 6.4 a. NOTE THE SHARP CUT-OFF AT ABOUT 80V.

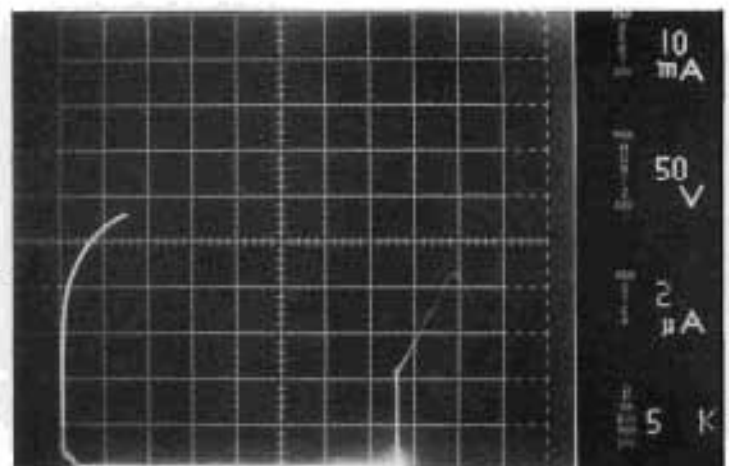
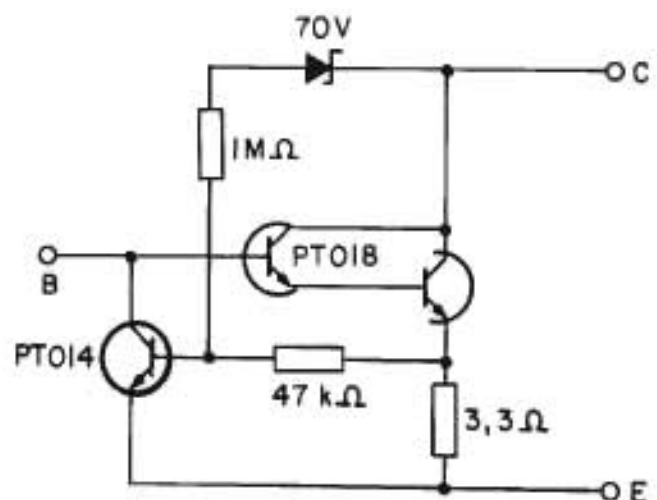


FIGURE 6.4 c

THE INCLUSION OF A 3.3Ω RESISTOR IN THE EMITTER OF THE PTO18 DARLINGTON LIMITED THE COLLECTOR CURRENT TO ABOUT 160 mA.



destroyed by the application of a high base-current at a collector-emitter voltage of 50 V.

Without recourse to an IC technology, it would appear to be difficult to realize an integrated Darlington with current-limiting capability. However, the use of distributed emitter ballast resistors in the output stage would be beneficial. Figure 6.5 (page 216) shows a distributed-element equivalent circuit of a Darlington transistor with emitter ballasting. At higher current levels significant voltages would appear across the emitter ballast resistors, and more current would be forced into the bases of the transistors with lower values of ballast resistance. By appropriate emitter ballasting, the gain of the transistor would be limited to a certain extent at high current levels and, what is more important, it should be possible to distribute the resistors in such a way that there would be no destructive hot-spot formation. Whilst this measure might not fulfil the requirements of an ideal current-limiting circuit, it would provide a transistor with a considerably greater surge immunity, and one that could be integrated with an LBT.

Figure 6.6 (page 216) shows how the LBT could be combined with emitter ballasting in a Darlington transistor in order to provide a combination of safe current-limiting at low to intermediate voltages, and the negative-resistance characteristic at higher voltages. A potential advantage of the structure, when compared with the GAT evaluated in Chapter 2, is that with the base and emitter shorted by the FET it should be possible to realize a value of BV_{CEO} equal to BV_{CBO} and BV_{CBS} . This would mean that the clamp transistor used in the PT018 could be dispensed with and that for the same breakdown voltage the epitaxial layer resistivity and thickness could be decreased. It would be an additional benefit that a smaller active area would be required for the same collector resistance R_C , and this would offset the extra area required in the circuit for the FET and the additional resistors.

6.6 TECHNOLOGICAL IMPLICATIONS

When Wu and Wu⁷⁷ developed their device, they were aiming not at a high collector-emitter breakdown, but rather at a single device with a negative-resistance characteristic. In a later publication by Wu and Sheng⁷⁹, the light-sensitive characteristics of the device were investigated. Nevertheless, the original LBT devices that were made in a 40 V IC process,

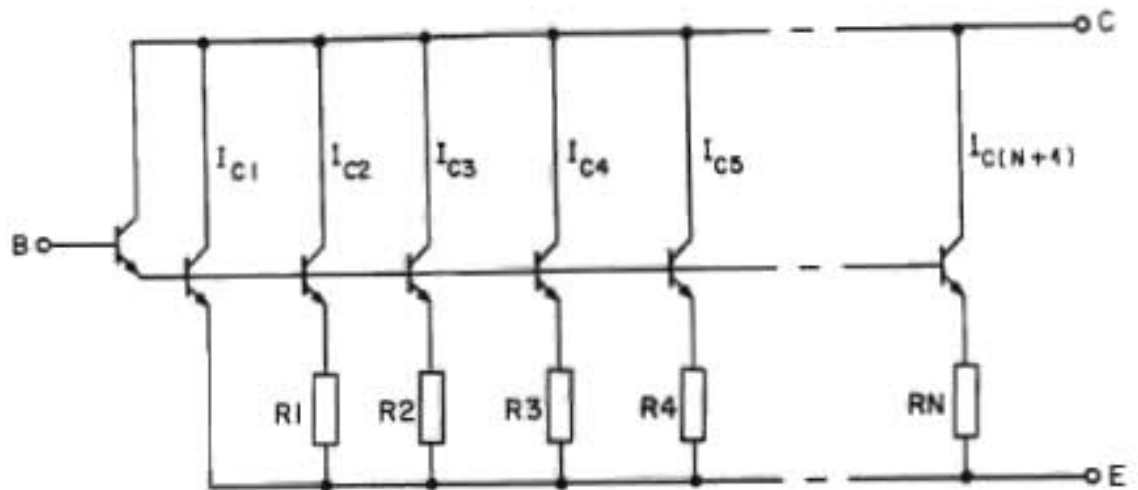


FIGURE 6.5 DISTRIBUTED-ELEMENT APPROXIMATION FOR AN EMITTER-BALLASTED DARLINGTON TRANSISTOR. $R_2 > R_1$, $R_3 > R_2$ ETC. AND $I_{C2} < I_{C1}$, $I_{C3} < I_{C2}$ ETC.

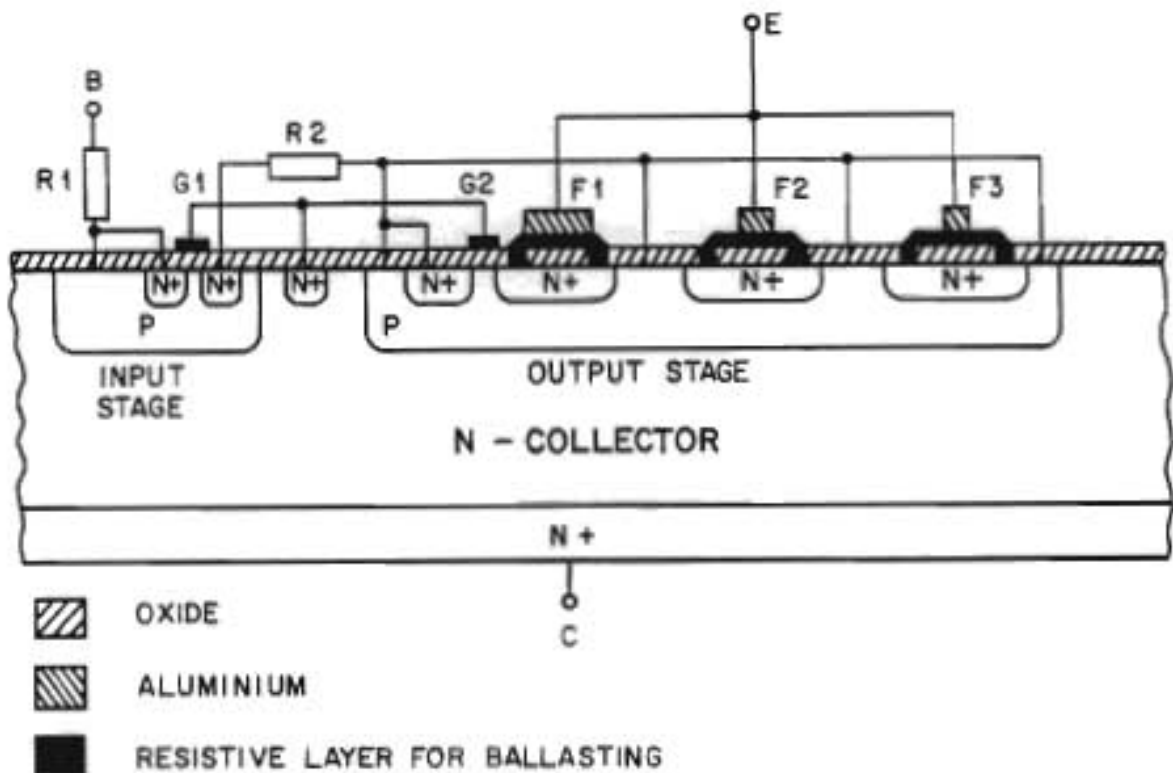


FIGURE 6.6 A LAMBDA BIPOLAR DARLINGTON TRANSISTOR WITH EMITTER BALLASTING. R_1 AND R_2 ARE DIFFUSED RESISTORS FOR ENHANCING THE OPERATION OF THE TWO FET'S CONTROLLED BY G_1 AND G_2 . TURNING OFF THE DRIVER AND OUTPUT STAGES ENABLES BV_{CE0} TO APPROACH BV_{CBO} . THE INTERDIGITATED FINGERS F_1 , F_2 AND F_3 HAVE DIFFERENT WIDTHS TO CHANGE THE VALUES OF BALLAST RESISTANCE.

exhibited values of BV_{CEO} of 100 V. To extend BV_{CEO} to 500 V in discrete transistor technology would not appear a problem but if it were desired to use the device in the telephone application where exchange voltages of typically 50 V were to be switched, it would be necessary to control the value of the turn-off voltage V_{TO} accurately. Accurate control of V_{TO} would require either accurate base pre-deposition or subsequent threshold adjustment. Ideally this should be done using ion implantation which, for the purposes of development, could be carried out at a number of local facilities. As part of a production programme, the purchase of a dedicated implanter is regarded as essential.

Emitter ballasting falls into the same category as ion implantation, since laboratory apparatus for sputtering suitable metals or silicides is readily available, but dedicated equipment for production would have to be purchased.

6.7 APPLICATION OF THE LAMBDA BIPOLAR TRANSISTOR (LBT) PRINCIPLE TO GATED DIODES.

Figure 6.1 (page 211) shows that in principle the gated diode used in the RT circuit is similar to a bipolar transistor, except that two additional diffusions have been added to the collector region and the device as a whole is in an oxide dielectric. As the resistance of a gated diode when turned on is only a few ohms, very large currents would have to flow through the device in order to generate a voltage large enough for LBT action. However, when it is considered that the RT switch handles both the forward and return lines to the subscriber loop, large differential voltages, potentially damaging to the SLIC, could be used to turn off the gated diode in order to block the high voltage.

Investigation of this possible application of the LBT principle could be carried out in discrete device technology using N-type epitaxial layers on P-type substrates, initially obviating recourse to an oxide isolation process. In this manner a valuable research objective with far-reaching implications could be pursued, as in the new generation of electronic exchanges being introduced into service in the Republic use is still being made of relays as the interface between the exchange and subscriber line. (Vlok, pers. comm.⁶)

6.8 CONCLUSION

The application has been highlighted of interface devices and integrated circuits in the switching, isolation and protection of the complex and sensitive electronic circuits used in modern telephones and digital telephone exchange systems.

The Lambda Bipolar Transistor (LBT) was identified as a component that would be of immediate application in telephone dials, and one that could be developed with existing facilities. Experiments with a simulated LBT indicated that it was able to withstand sustained high-voltage surges without degradation of the device itself or telephone performance. It was shown that if the device were operated at an intermediate voltage and high collector current, it could still be destroyed. As it would be difficult to incorporate a current-limiting circuit using only discrete transistor technology, a compromise solution was proposed where emitter ballasting could be used to drop gain at higher current levels and distribute the thermal load more evenly across the device, thereby providing a greater measure of overload immunity.

To address the need for exchange protection that could be incorporated into RT interface circuits, it was suggested that the LBT principle be applied to gated diodes in order to turn them off in the presence of high differential-voltages. Standard bipolar transistor technology could be used for preliminary investigations.

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SECTION 8 : APPENDICES

SPECIFICATION FOR TRANSISTOR TR2 IN PROTEA TELEPHONE WITH 1N914B DIODE IN SERIES WITH BASE. ISSUE 3, DECEMBER 1977

TELECOMMUNICATION HEADQUARTERS
OFFICE OF THE CHIEF ENGINEER
CUSTOMER SERVICES SECTION (3B613)

1.0 TYPE, PACKAGE AND LEAD CONFIGURATION

- 1.1 Type: NPN Silicon
1.2 Package: JEDEC TO-5 or TO-39
1.3 Lead Configuration:



2.0 RATINGS AT 25 °C AMBIENT TEMPERATURE

No.	Parameter	Test Condition	Minimum	Maximum	Unit
2.1	$V_{CE0(SOS)}$	$I_C =$ (to be specified by manufacturer)	140		V
2.2	$V_{(BR)CBO}$	$I_C = 100 \mu A$	160		V
2.3	$V_{(BR)EBO}$	$I_E = 100 \mu A$	5		V
2.4	$I_{CH(PK)}$		1		A
2.5	$I_{CH(AV)}$		150		mA
2.6	I_{CBO}	$V_{CB} = 140 V$	20		μA
2.7	I_{EBO}	$V_{EB} = 4,5 V$	10		μA
2.8	$V_{CE(sat)}$	$I_C = 30 mA; I_B = 1,5 mA$		0,4	V
2.9	V_{CEX}	$I_C = 60 mA; I_B =$ value for which $I_C = 66 mA$ at $V_{CE} = 8 V$		4	V
2.10	$h_{FE(1)}$	$V_{CE} = 7 V; I_C = 60 mA$	60	250	-
2.11	$h_{FE(2)}$	$V_{CE} = 4 V; I_C = 20 mA$	70	200	-
2.12	h_{fe}	$V_{CE} = 7 V; I_{CB} = 60 mA$ $f = 1 kHz$	60		-
2.13	f_T	$V_{CE} = 4 V; I_C = 20 mA$	0,5		MHz

TRANSISTOR SPECIFICATION TR2 - ISSUE 3, DECEMBER 1977

3.0 RATINGS AT 95 °C CASE TEMPERATURE (Heat sink 50 °C/W fitted)

No.	Parameter	Test Condition	Minimum	Maximum	Unit
3.1	T_{jmax}	(P_{TOT})		150	°C
3.2	P_{TOT}	$V_{CE} = 13 V; I_C = 70 mA$ Dissipation time = 5 hours	1		W
3.3	$P_1(PK)$	$V_{CE} = 50 V; I_C = 300 mA$ Dutyfactor = 6% Pulse repetition frequency = 2,5 kHz. Total dissipation time = 100 ms	15		W
3.4	$P_2(PK)$	$V_{CE} = 130 V; I_C = 750 mA$ Dutyfactor = 0 Dissipation time = 10 μs	100		W

4.0 ALLOWABLE CHANGE IN PARAMETERS AFTER PARAGRAPHS 3.0 TESTS HAVE BEEN CONDUCTED

	Parameter	Allowable change
4.1	$h_{FE(1)}$	+/- 20% of originally measured value
4.2	$h_{FE(2)}$	+/- 20% of originally measured value
4.3	h_{fe}	+/- 20% of originally measured value
4.4	I_{CBO}	+ 100% of originally measured value
4.5	I_{EBO}	+ 100% of originally measured value
4.6	All other parameters of paragraph 2.0 should meet the original requirements.	

APPENDIX 2.2

DESIGN OF THE PUNCHTHROUGH COLLECTOR USING DATA FROM A 1700 V DIODE DESIGN

Case 4, marked '*', was scaled for the PT014 collector design as the use of a collector region with a width of approximately one quarter of the full depletion width at the avalanche voltage was found to provide a good compromise between epitaxial layer thickness and resistivity for the PT014 collector.

W_D is the avalanche depletion width and W_C the collector width, in the table.

Table 2.1 Alternate Designs for a 1700 V Diode

N_a (atoms/cm ³)	BV_{PN} (V)	$\frac{BV_{PT}}{BV_{PN}}$	η	W_D (μm)	W_C (μm)
8×10^{13}	1700	1	1	160	160
7×10^{13}	1850	.918	.714	180	129
5×10^{13}	2400	.708	.460	240	110
* 3×10^{13}	3600	.472	.273	380	104
2×10^{13}	5100	.333	.183	560	102
1.5×10^{13}	6500	.262	.140	740	103.6
1×10^{13}	9000	.189	.099	1100	109

Table from Ghandi¹⁶.

(Ghandi S K (1977) Semiconductor power devices. New York : Wiley Interscience, ISBN 0-471-02999-8, page 48.)

APPENDIX 2.3 : PTO14 WAFER SPECIFICATION

High resistivity silicon, monocrystalline epitaxial wafersSubstrateStandard polished wafer

Dopant:	Antimony (n type)
resistivity:	0,007 ohm.cm min. to 0,020 ohm.cm max.
orientation:	1-1-1 off 1,5 +/- 0,5 degrees
diameter:	50,8 +/- 0,4 mm
thickness:	280 +/- 25 μ m
bow:	max. 25 μ m typical 10 μ m
taper:	max. 13 μ m typical 8 μ m
surface flatness:	max. 10 μ m typical 4 μ m
primary flat:	orientation 1-1-0 +/- 1 degree width 15,9 +/- 1 mm
secondary flat:	none
dislocation density:	500/cm ² max.

Polished surface

(a) Scratches	90% of all slices free of scratches. Balance max. 3 scratches per slice, total accumulative length not to exceed 12,5 mm.
(b) Orange peel	Free of orange peel.
(c) Haze	Free of haze.
(d) Dimples	Free of dimples.
(e) Edge rounding	7-21 μ m maximum penetration 2 mm.
(f) Chips	No chips with apex or penetrating the entire thickness of the slice. 95% of all slices free of chips. Balance max. 2 chips not extending further than 0,5 mm towards centre of slice. Chips extending less than 0,25 mm towards centre of slice not considered chips, but not to exceed 3 in number.
(g) Subsurface	No damage shall be revealed due to insufficient stock removal after one minute Sirtl etch.
(h) Cleanliness	No more than 3 light reflecting particles which cannot be blown off with antistatic nitrogen blow. 80% of all slices free of particles after nitrogen blow.
<u>Reverse side</u>	Specially treated matte reverse side.
(a) Saw marks	90% of all slices free of saw marks. Balance very light saw marks, < 10 μ m depth.

APPENDIX 2.3 CONTINUED : PTO14 WAFER SPECIFICATION

(b) Cleanliness	Free of contamination which cannot be removed by standard cleaning methods commonly used in the industry.
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AQL of 1,0% applied to all mentioned parameters.
At least 75% of all slices are within the typical values.

Epitaxial layer

Dopant	phosphorus (n type)
Resistivity	33-50 ohm.cm (Measured by cap. method min. AQL 1,5%)
Thickness	38-52 μ m (Corrected I.R. measurement min. AQL 1,5%)

Inspection of epitaxial slices

Visual, unaided, carried out on 100% of wafers. This applies to the whole wafer except an outer annulus of 3 mm, excepting where otherwise specified.

Scratches:	90% of wafers scratch free, the balance three scratches per wafer, cumulative length less than 12,5 mm.
Edge chips:	95% of all slices free of any kind of chips. Balance max. 2 chips not extending further than 0,5 mm towards the centre of the slice. Maximum length 5 mm and total cumulative length not to exceed 12,5 mm.
Protrusions:	Max. 5 per slice.
Edge crown:	No visible edge crown.
Haze:	None.
Stains:	None.
Orange peel effect:	None.
Ripples:	None.
Pits and dimples:	None.
Cracks, fractures, Crow's feet:	None.
Foreign matter:	80% of all slices free of particles after nitrogen blow. Remainder - no more than three particles per wafer.
Slip and/or lineage:	< 5 lines (after Sirtl etch).

Microscopic examination

One wafer from each batch is to be Sirtl etched and examined under a microscope:

Stacking faults:	< 50/cm ² .	Etch pit density:	< 2 000/cm ² .
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REPORT ON ELECTRICAL TESTS OF TRANSISTOR

T12 FROM C.S.I.B.

27th June, 1979

EQUIPMENT USED:

On-line tester type T354 with programmes DT 9120 - 93
TT 9121 - 93

Oscilloscope Tektronix type 7633

PULSE TEST JIG

SAMPLE RESULTS

TYPE 'A'

Total Tested	=	26	
Pass	=	25	96%
Reject	=	1	4%

TYPE 'B'

Total tested	=	18	
Pass	=	13	72%
Reject	=	5	28%

TYPE 'C'

Total Tested	=	18	
Pass	=	15	83.3%
Reject	=	3	16.7%

SAMPLE TESTING

Three devices of each type plus rejects were dataloggged during tests @ 25°C Temperature ambient.

Sampling results of TYPE 'A'.

Device No. 1

Test	Test	Test	Test
1, 238V	2, 240V	3, 11.6V	4, .99mA
5, .008A	6, 81mW	7, 686mV	8, 117.1
9, 117.1	10, 112.9	11, 112.9	12, 117.6
13, 114.5	14, 117.		

TEST CONDITIONS	
Test 1	$V_{CBO}(BUS) @ I_C = 10 \text{ mA}$
Test 2	$V_{(BR)CBO} @ I_C = 100 \text{ } \mu\text{A}$
Test 3	$V_{(BR)EBO} @ I_E = 100 \text{ } \mu\text{A}$
Test 4	$I_{CBO} @ V_{CB} = 140 \text{ V}$
Test 5	$I_{EBO} @ V_{EB} = 4.5 \text{ V}$
Test 6	$V_{CE}(SAT) @ I_C = 30 \text{ mA}$ and $I_E = 1.5 \text{ mA}$
Test 7	V_{BE} as for Test 6
Test 8	to Test 11 are for knee voltage acceptance.
Test 12	$h_{FE}(1) @ I_C = 60 \text{ mA}$ and $V_{CE} = 7 \text{ V}$
Test 13	$h_{FE}(2) @ I_C = 20 \text{ mA}$ and $V_{CE} = 4 \text{ V}$
Test 14	h_{FE} at 1 kHz as for Test 12

Device No. 2

Test	Test	Test	Test
1, 240V	2, 240V	3, 12.2V	4, .008A
5, .008A	6, 90mW	7, 681mV	8, 125.5
9, 125.5	10, 121.2	11, 121.2	12, 126.3
13, 124.4	14, 125.7		

Device No. 3

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.9V	4, 4.98A
5, .008A	6, 88mW	7, 684mV	8, 124.4
9, 124.4	10, 120.4	11, 120.4	12, 126.3
13, 123.7	14, 124.2		

Rejected - Failing parameters.

Test
3, 0V
8, 40.54
10, 18.55

Sampling results of TYPE 'B'

Device No. 1,

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.9V	4, .01 mA
5, .01 mA	6, 79mW	7, 656mV	8, 96.93
9, 96.93	10, 84.03	11, 84.03	12, 100
13, 96.3	14, 97.63		

Device No. 2,

Test	Test	Test	Test
1, 238V	2, 240V	3, 11.2V	4, 19 mA
5, 2.1 mA	6, 78mW	7, 658mV	8, 100.1
9, 100.1	10, 91.74	11, 91.74	12, 100
13, 99.5	14, 100.3		

Report on the surge testing of prototype TRI transistors by Messrs Standard Telephones & Cables

APPENDIX 2.4

Device No. 3.

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.9V	4, 5.28A
5, .008A	6, 78mV	7, 655mV	8, 100.3
9, 100.3	10, 87.71	11, 87.71	12, 100
13, 99.66	14, 100.7		

Rejects - failing parameters.

Test	Average	Average
10,	Average	62.23
12,	Average	75.45

Sampling results of TYPE 'C'

Device No. 1.

Test	Test	Test	Test
1, 171V	2, 199V	3, 12.2V	4, 3.58A
5, .008A	6, 82mV	7, 641mV	8, 117.8
9, 117.8	10, 102.5	11, 102.5	12, 114.2
13, 116.7	14, 118.7		

Device No. 2.

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.8V	4, .008A
5, .008A	6, 81mV	7, 647mV	8, 116.7
9, 116.7	10, 106.3	11, 106.3	12, 114.2
13, 115.8	14, 117.4		

Device No. 3.

Test	Test	Test	Test
1, 240V	2, 240V	3, 12.2V	4, .008A
5, .008A	6, 78mV	7, 642mV	8, 121.2
9, 121.2	10, 105.2	11, 105.2	12, 117.6
13, 120.2	14, 121.9		

Rejects - Failing parameters.

Test	Test
1, 20.9V	
2, 34.1V	
3, .57mA	

4. PULSE TEST

The same devices were subjected to pulse test, as per S.A.P.O. specification for TR2 Issue 3 December 1977, and retested on Teradyne.

a) Results of TYPE 'A'

Device No. 1

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.6V	4, .008A
5, .008A	6, 82mV	7, 688mV	8, 117.1
9, 117.1	10, 112.9	11, 112.9	12, 117.6
13, 116.5	14, 117		

Device No. 2.

Test	Test	Test	Test
1, 240V	2, 240V	3, 12.2V	4, .008A
5, .008A	6, 90mV	7, 685mV	8, 124.7
9, 124.7	10, 119	11, 119	12, 126.3
13, 123.7	14, 124.7		

Device No. 3.

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.9V	4, 4.58A
5, .008A	6, 88mV	7, 688mV	8, 122.9
9, 122.6	10, 118.3	11, 118.3	12, 123.7
13, 122.1	14, 123.1		

APPENDIX 2.4 (CONTINUED)

FNCZ/S.....

Results of TYPE 'B'

Device No. 1.

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.9V	4, .00NA
5, .00NA	6, 78mV	7, 662mV	8, 95.69
9, 95.69	10, 82.98	11, 82.98	12, 100
13, 95.38	14, 96.49		

Device No. 2.

Test	Test	Test	Test
1, 236V	2, 238V	3, 11.2V	4, 19 NA
5, .7 NA	6, 78mV	7, 660mV	8, 99.66
9, 99.66	10, 90.90	11, 91.74	12, 100
13, 99.17	14, 100		

Device No. 3.

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.9V	4, 4.4 NA
5, .00 NA	6, 78mV	7, 662mV	8, 99.66
9, 99.66	10, 87.71	11, 87.71	12, 100
13, 99.17	14, 100.3		

Results of TYPE 'C'

Device No. 1.

Test	Test	Test	Test
1, 178V	2, 210V	3, 12.2V	4, 3.1 NA
5, .00 NA	6, 81 mV	7, 645mV	8, 117.1
9, 117.1	10, 101.5	11, 101.5	12, 112.1
13, 116.2	14, 118.		

Results of TYPE 'C' (Cont'd)

Device No. 2.

Test	Test	Test	Test
1, 240V	2, 240V	3, 11.8V	4, .00 NA
5, .00 NA	6, 81mV	7, 648mV	8, 116.2
9, 116.2	10, 105.2	11, 105.2	12, 112.1
13, 115.6	14, 116.8		

Device No. 3.

Test	Test	Test	Test
1, 240V	2, 240V	3, 12.2V	4, .00NA
5, .00NA	6, 78mV	7, 648mV	8, 119.7
9, 119.7	10, 104.1	11, 104.1	12, 117.6
13, 119.2	14, 120.6		

APPENDIX 2.4 (CONTINUED)

V. SERRANO

APPENDIX 2.5 : RESULTS OF MEASUREMENTS ON GATE ASSOCIATED TRANSISTORS WITH THREE DIFFERENT GATE SPACINGS DIFFUSED IN A NUMBER OF WAFERS OF DIFFERING RESISTIVITY AND ORIENTATION

The test conditions for the automatic testing of the GAT wafers were :

1 h_{FE} at $V_{CE} = 1$ V and $I_C = 5$ mA

2 $V_{CE0(SUS)}$ at $I_C = 5$ mA

3 V_{CB0} at $I_C = 1$ mA

The values of n were calculated using equation 2.54 (page 20) and the values of E' for the GAT devices, as defined in equation 2.60 (page 46), were obtained by taking the ratio of V_{CB0} for the GAT to the calculated V_{CB0} of a standard transistor with the same gain as the GAT.

WAFER	BATCH	ORIENT.	RES.	TYPE	GAIN	V_{CB0}	V_{CE0}	n	E'
3	A	<111>	1	STD	370	60	17	4,69	----
				DP38	110	60	24	5,13	1,09
				DP28	70	60	30	6,13	1,24
				DP20	30	60	38	7,45	1,31
6	A	<111>	1	STD	120	56	17,5	4,12	----
				DP38	43	56	24	4,44	1,07
				DP28	30	57	32	5,89	1,28
				DP20	19	56	36	6,66	1,31
4B	A	<111>	10	STD	120	310	120	5,04	----
				DP38	43	310	180	6,92	1,22
				DP28	30	310	210	8,73	1,33
				DP20	20	310	225	9,35	1,32
2H	A	<111>	10	STD	300	305	115	5,85	----
				DP38	75	305	180	8,19	1,23
				DP28	48	305	190	8,18	1,21
				DP20	27,5	305	200	7,85	1,16

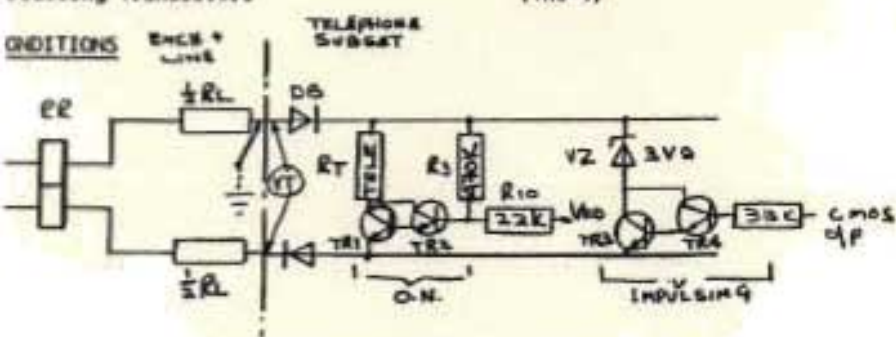
APPENDIX 2.5 CONTINUED : RESULTS OF MEASUREMENTS ON GAT TRANSISTORS

WAFER	BATCH	ORIENT.	RES.	TYPE	GAIN	V_{CB0}	V_{CE0}	n	E'
14B	A	<111>	10	STD	48	340	160	5,14	----
				DP38	19,8	340	220	6,86	1,16
				DP28	16	340	240	7,35	1,18
				DP20	12,5	340	250	7,51	1,17
3B	B	<111>	10	STD	2 000	290	70	5,35	----
				DP38	370	290	140	8,12	1,46
				DP28	145	290	165	8,83	1,44
				DP20	53	290	180	8,32	1,30
27	A	<100>	10	STD	33,5	340	180	5,52	----
				DP38	15,5	340	230	7,01	1,11
				DP28	12,9	340	240	7,34	1,12
				DP20	10,4	340	250	7,62	1,12
37	A	<100>	10	STD	72	320	145	5,40	----
				DP38	27	320	210	7,82	1,21
				DP28	20,4	320	225	8,56	1,23
				DP20	15,3	320	245	10,2	1,27
57	A	<100>	10	STD	20,6	320	192	5,92	----
				DP38	10	320	248	9,03	1,14
				DP28	8,4	320	265	11,3	1,19
				DP20	6,9	320	275	12,8	1,19
38	A	<111>	40 (EPI)	STD	1 130	600	170	5,57	----
				DP38	248	600	260	7,23	1,26
				DP28	96	600	330	7,63	1,25
				DP20	37,4	600	370	7,50	1,18

APPENDIX 2.5 SUMMARIZED RESULTS FROM THE AUTOMATIC PROBE TEST OF GAT WAFERS

PUSH BUTTON DIAL TRANSISTORS ZT435220

On Normal Transistors (TR1-2)
 Dialling Transistors (TR3-4)



- CONDITIONS
- VT = Voltage-Telephone
 - VB = Voltage-Battery = 46-52V
 - RR = Resistance-Relay = 200+200 OHMS
 - RL = Resistance-Line = 0 - 1300 OHMS
 - RT = Resistance-Telephone
 - VTR = VCE TR1+2 or TR3+4
 - VDB = Voltage Diode Bridge
 - VZ = Voltage Zener

Current resistances of the telephone ranges from + 135 ohm - zero line to 300 ohm at - 1800 ohm line N2 unit. (S.A.P.O. Report No. 90 Fig. 73).

Conditions were performed to find the currents and voltages on the following lines.

- Nominal (400 ohm)
- Long (1300 ohm)
- Zero (0)
- Fault (one leg to earth)
- High Voltage surges.

$$I_C TR = \frac{VB - VDB - VTR(\text{or } -VZ)}{RL + RR + RT}$$

ON NORMAL TRANSISTOR (TR1 - 2)

VB	VDB	VTR	VZ	RL	RR	RT	IC
V	V	V	V	ohm	ohm	ohm	mA
50	1,2	1	-	400	400	200	47,8
46	1,2	1	-	1300	460	300	21,2
52	1,2	1	-	0	380	134	96,8
52	1,2	1	-	0	190	134	154

IMPULSING TRANSISTORS TR3 - 4.

LINE	VB	VDB	VTR	VZ	RL	RR	RT	IC
	V	V	V	V	ohm	ohm	ohm	mA
NOMINAL	50	1,2	1	3V9	400	400	-	54,8
LONG	46	1,2	1	3V9	1300	460	-	22,6
SHORT	52	1,2	1	3V9	0	380	-	120,7
FAULT	52	1,2	1	3V9	0	190	-	241,6

NOTE :-

For above calculations it has been assumed that VTR = VCEsat = 1V and VD = VF = 0,6V x 2 = 1,2V and VZ = VZ = 3V9, no allowance has been made for parameters other than above. Resistors are assumed to be nominal. For dialling transistors the transistor are not biased on permanently. The maximum time that the impulsing transistors will be on will not exceed 800mS and never be less than 30mS.

- 800mS = 1DP or PDP
- 30mS = Make Pulse

BASE CURRENT Ib

ON NORMAL

The base current of TR2 is made up of the currents via R10 and R3. The Value VT is obtained from S.A.P.O. Report No. 90 Fig. 74.

MINIMUM Ib = Long Line (Blue Box) Ib

$$= \frac{VT - 2 \times VBE}{R3} + \frac{VDD - 2 \times VBE}{R10} \quad \mu A$$

$$= \frac{4,5 - (0,6 \times 2)}{470K} + \frac{2,5 - (0,6 \times 2)}{22K} = 66$$

MAXIMUM Ib = Zero Line

$$= \frac{12,5 - 1,2}{470K} + \frac{3,5 - 1,2}{22K} = 129$$

IMPULSING

MINIMUM Ib = $\frac{VDD - 2 \times VBE}{33K} = \frac{2,5 - 1,2}{33K} = 39$

MAXIMUM = $\frac{3,5 - 1,2}{33K} = 70$

NOMINAL = $\frac{3 - 1,2}{33K} = 55$

FAULT = $\frac{3,7 - 1,2}{33K} = 76$

APPENDIX 3.1 TELEPHONE MANUFACTURERS GUIDELINES FOR A DARLINGTON TRANSISTOR SPECIFICATION

OF Ic/Ib

Unit(s)	Ic mA	Ib µA	RATIO
ON	47,8	96	532
	21,2	66	312
	96,8	128,5	754
	154	130	1185
NG	54,8	55	996
	22,6	39	579
	120,7	70	1728
	241,6	76	3184

} $\theta V_{CE} = 1,8 V$

} $\theta V_{CE} = 3 V$

VOLTAGE

ut voltage to the telephone is limited by avalanche diodes DA1002 and re during high voltage spikes, such as back e.m.f. from relays during ng, and lightning overloads, the circuit will have to tolerate an excess ent for the time that this high voltage persists. It is assumed that anche voltage for the DA1002 will never exceed 300V. elling the time that the telephone, hence the transistor is subjected to h voltage is about 2m5 nominal. For the ON Normal tran- however, during lightning strikes, this time can be extended up to (TABLE 2.2 - FLASH PARAMETERS OF CSIR SPECIAL REPORT ELEK 165 by iksson, etc.), the gas protector will normally strike in less than 500µs ng upon dv/dt. he period that the telephone is subjected to these high voltages the in the circuit will be as follows :-

$$= \frac{V_{DD} - 2V_{BE}}{R_{10}} + \frac{V_T - 2V_{BE}}{R_3}$$

$$= \frac{3,6 - 1,2}{22K} + \frac{300 - 1,2V}{470K} = 745 \mu A$$

$$= \frac{V_T}{R_T} = \frac{300}{134} = 2,23A$$

calculation ignores effect of VCEsat.

imum Ic will only be limited by the base current of TR4 and the gain vices TR3 + 4.

VOLTAGE RATINGS

ALL TRANSISTORS

VCB	300V to be advised
VCEO	300V " " "
VEB	7V

NOTE :- VEB was observed in actual working model and no indication of any reverse voltage was noticed.

CURRENT RATINGS

	TR1	TR2	TR3	TR4
Ic	155mA		242mA	

Ic max. 2,23A

Ib	740µA	76µA
----	-------	------

VCEsat ALL TRANSISTORS

Ic mA	Ib µA	VCEsat V
1	55	0,2 max.
25	250	0,2 max.
250	2000	

DISCUSSION

The requirement for the On Normal transistor (TR1,2) is fairly simple although these transistors are subjected to long periods when they are switched on (talking).

These transistors are required to have a low VCEsat to prevent the changing of the characteristics of the Protea Telephone amplifier on long line workin the telephone speech performance must be very similar to that of a telephone with a rotary dial. These transistors can be subjected to very high dissipation problems such as lightning strikes of up to 2000m5.

The Impulsing transistors will be operated in an impulse type mode.

During short line impulsing it is not possible to provide high base drive to the impulsing transistor, this is due to the IC's parameters and circuit design.

This situation does not cause any problems as far as the exchange equipment is concerned but does aggravate the power dissipation problem of the impulsing transistors, this problem will also be encountered during lightning strikes when the collector current is limited only by the base current i.e the VCEsat is not a function of forced gain and TR3 comes out of saturation.

NEERI/Ev/11/3
NEERI/Ev/14/1

MICROELECTRONICS DEPARTMENT

'SKELETON' SPECIFICATION FOR PUSH-BUTTON DIAL TRANSISTORS

Information in the sheet 'Push button dial transistors Z7435220 drawn up by TMSA and verbal information from Mr R Holmes has been used to assemble a 'skelaton' specification for the pushbutton dialling transistor. Specifications for BPO28, BPO39 and 2K3439 have been disregarded at this stage, or simply used as a guide. The 'skelaton' specification gives the actual values that must be met by any transistor for use in the dialler. These figures may appear unrealistic and in fact they are just this as the circuit requirements have been used rather than measurements performed on devices found to be suitable.

Where values have been suggested, there is either little or no information: limits must be set and agreed to.

In the cases where parameters to be met do exist, then the manufacturing limits must be set as well.

Please note that device parameters are a strong function of temperature, hence this must be taken into account: For example the transistor gains drop with decreasing temperature and if insets are not made to the 25°C values, operation at say 0°C could be adversely affected. TMSA is requested to consider all other limiting factors as well.

When essential limits are agreed upon I shall translate these into a 'realistic' transistor specification with the following aims to:

- (1) Minimise number of parameter measurements at test.
- (2) Set realistic values of probe parameters.
- (3) Set final device acceptance parameters that are compatible with the probe parameters.

These specifications will be applicable to complete devices and devices to be assembled locally.

S.A. Smithies

S A Smithies
Semiconductor Technology Division
Microelectronics Department

SPECIFICATION FOR PUSHBUTTON DIAL TRANSISTORS

(Figures deduced from figures supplied by TMSA)
(Suggestions either from TMSA or CSTR)

No.	Parameter	Condition	Suggested?	Deduced?	Value		Unit
			Y - yes	Y - yes	Min	Max	
1	V_{CHD}	$I_C = 10\mu A$ $I_E = 0$	Y		300		V
2	$V_{CEO(SUS)}$	$I_C = 10mA$ $I_B = 0$	Y		300		V
3	V_{EBO}	$I_E = 10\mu A$ $I_C = 0$	Y		5		V
4	$V_{CE(SAT)}(1)$	$I_C = 100mA$ $I_B = 5mA$		Y		1.8	V
5	$V_{CE(SAT)}(2)$	$I_C = 125mA$ $I_B = 7.5mA$		Y		3	V
6	$V_{CE(SAT)}(3)$	$I_C = 160mA$ $I_B = 10mA$	Y	Y		4	V
7	$V_{CE(SAT)}(4)$	$I_C = 250mA$ $I_B = 10mA$	Y	Y		10	V
8	$V_{CE(SAT)}(5)$	$I_C = 5mA$ $I_B = 125\mu A$		Y		0.9	V
9	$h_{FE}(1)$	$I_C = 100mA$ $V_{CE} = 1.8V$		Y	25		
10	$h_{FE}(2)$	$I_C = 125mA$ $V_{CE} = 3V$		Y	25		
11	$h_{FE}(3)$	$I_C = 4mA$ $V_{CE} = 0.9V$		Y	35		
12	$h_{FE}(4)$	$I_C = 5mA$ $V_{CE} = 2.1V$		Y	75		

Note: The figures for $h_{FE}(1)$ and $h_{FE}(3)$ as well as $h_{FE}(2)$ and $h_{FE}(4)$ were estimated using gain curves for the 2K3439 so that the products are greater than 754 and 1728 respectively.

APPENDIX 3.2 SKELETON SPECIFICATION FOR A DISCRETE TRANSISTOR FOR DARLINGTON APPLICATION

APPENDIX 3.3

24 September 1981

Summary of results of a failure analysis exercise study on TR2 - Issue 3 transistors, returned from the field, carried out by the Quality Assurance Inspectorate of the Department of Posts and Telecommunications.

Transistor package : JEDEC TO-5 and TO-39

Time of Manufacture : 1977 to 1981 Quantity : 602

Out of the 602 TR2 - Issue 3 transistors 349 were on TO-39 (solid metal) headers, 126 of these the die was off ('popcorn effect') = 36.1% of this type.

1. Leak testing

1.1 Transistors failing gross leak :

Quantity tested = 602; quantity failed = 32 = 5,31%

1.2 Transistors failing fine leak (1×10^{-7} atm.cc/sec. He) :

Quantity tested = 570; quantity failed = 40 = 7,01%

2. Visual inspection (after opening transistors)

Quantity tested = 476

2.1 Foreign material = 86 = 18,06%

2.2 Metallization defects = 51 = 10,71%

2.3 Scribing and die defects = 45 = 9,45%

2.4 Wirebonding defects = 35 = 7,35%

2.5 Electrically damaged = 34 = 7,14%

2.6 Diffusion and underlying oxide layer faults = 5 = 1,05%

2.7 Die bonding defects = 4 = 0,84%

2.8 Die with no visual faults = 217 = 45,58%

Note : Graphs for distribution of failures in quantity/week and photographs of assembly and other faults are not included here.

Source of information : F Schoombie, QA Inspectorate, Dept of Posts and Telecommunications, Pte Bag X74, Pretoria 0001.

High resistivity silicon, monocrystalline epitaxial wafersSubstrate

Standard polished wafer

Dopant:	Antimony (n type).
Resistivity:	0,006 ohm.cm minimum to 0,020 ohm.cm maximum.
Orientation:	1-1-1 off 3 degrees +/- 0,5 degrees.
Diameter:	50,8 +/- 0,4 mm.
Thickness:	280 +/- 15 μ m.
Bow:	Maximum 25 μ m, typical 10 μ m.
Taper:	Maximum 5 μ m, typical 3 μ m.
Surface flatness:	Maximum 3 μ m.
Primary flat:	Orientation 1-1-0 within 1 degree. Width 15,9 +/- 1 mm.
Secondary flat:	None.
Dislocation density:	100/cm ² maximum.

Polished surface

(a) Scratches:	98% of all slices free of scratches. Balance: Maximum 2 scratches per wafer, accumulative length not to exceed 12,7 mm.
(b) Orange peel:	Free of orange peel.
(c) Haze:	Free of haze.
(d) Dimples:	Free of dimples.
(e) Edge rounding:	7-21 μ m penetration 2 mm maximum.
(f) Chips:	95% of all slices free of chips. Balance: Maximum 2 chips not extending more than 0,5 mm towards the centre of the slice.
(g) Subsurface:	No damage shall be revealed due to insufficient stock removal after one minute Sirtl etch.
(h) Cleanliness:	90% of all slices free of particles after nitrogen blow. Remainder up to 3 particles per slice.
<u>Reverse side</u>	Specially treated matte reverse side.

(a) Saw marks:	Free of saw marks.
(b) Cleanliness:	Free of foreign matter that cannot be removed by standard cleaning techniques.

(c) Edge chips: < 0,5 mm.

AQL of 1% applies to all given parameters.
At least 75% of all slices to be within typical values.Epitaxial layer

Dopant:	Phosphorus (n type)
Resistivity:	50-75 ohm.cm (AQL 1,5% measured by capacitive method.)
Thickness:	58-70 μ m (Corrected IR measurement. AQL 1,5%.)

Inspection of epitaxial slices

Visual unaided, carried out on 100% of wafers. This applies to the whole wafer except on outer annulus of 3 mm excepting where otherwise specified.

Scratches:	90% of wafers free from scratches. Balance may have a maximum of three scratches per wafer, cumulative length less than 12,7 mm.
Edge chips:	95% of all slices free of any kind of chips. Balance maximum 2 chips not extending further than 0,5 mm towards the centre of the slice.
Protrusions:	Maximum 5 per slice.
Edge crown:	No visible edge crown.
Haze:	None.
Stains:	None.
Orange peel:	None.
Ripples:	None.
Pits and dimples:	None.
Cracks, fractures, crow's feet:	None.
Foreign matter:	90% of all slices free of particles after nitrogen blow. Remainder up to 3 particles per wafer.
Slip and/or lineage:	Maximum 5 sources (after Sirtl etch).

Microscopic examination

One wafer from each batch is to be Sirtl etched and examined under a microscope.

Stacking faults: Maximum 5/cm². Etch pit density: Maximum 2 000/cm².

NEERI/De/9/11/3
NEERI/De/9/1A/1

22 February 1982

MICROELECTRONICS DEPARTMENT

CONTAMINATION OF DARLINGTON TRANSISTORS DURING ASSEMBLY

Related document: Progress report on Darlington transistor PTO18 from April 1981 to December 1981, File Ev/11/3. Date 11 December 1981.

1. SUMMARY

High reverse bias leakage currents measured on a number of Darlington transistors diffused at NEERI and assembled by STC may be ascribed to gross contamination.

Contaminants detected may be divided into three distinct categories which comprise two main groups:

- Loose particles which may be removed in an ultrasonic solvent wash. These are likely to affect some device parameters and will in addition form a reliability hazard.
- Contaminants included in or intimately attached to the silicon/silicon dioxide system. These are likely to account for the high leakage currents and temperature instability observed.

Based on this analysis, recommendations are made for clean working conditions to Federal Specification 209 and for the addition of two extra cleaning steps during assembly.

2. THE DARLINGTON TRANSISTOR PTO18 FOR THE PUSHERUTTON DIAL TELEPHONE

- Higher leakage currents may be expected in the PTO18 Darlington transistor when compared to a discrete transistor made in a similar process. This is simply due to amplification of the leakage currents in the first stage circuit by the output transistor.

Values of I_{CEO} and I_{CBO} can be expected to be about h_{FE} (about 100) times greater than in a discrete transistor of the same nature.

This can be overcome by the use of pull-down resistors in the base circuits of the transistors. However in the case of a long telephone line where base drive current is lower, inclusion of such resistors might impair operation of the dial.

- The specification proposed, see attached, takes this into account and includes realistic values for I_{CEO} and I_{CBO} which are, in fact, far lower than values that have been measured using a pair of 2N3639 transistors.

3. INCREASE IN LEAKAGE AFTER ASSEMBLY

The pre-production batch of PTO18 devices had a yield of 96% for leakage current at the probe stage and only 12% after assembly. Yield figures on other parameters were virtually unchanged. An investigation of assembled devices was indicated after further probing still indicated a gross anomaly.

4. INVESTIGATION

- Optical inspection of 20 de-capped transistors showed numerous particles on the surface of the devices and some stains. Some particles were removed by blowing with nitrogen.

The location of particles and other irregular marks on all devices was mapped.

4.2. SEM investigation4.2.1 Control sample

Wafer number 1 of batch 1062 (the batch from which the pre-production devices were assembled) was inspected and analysed in the SEM. See figure 1.

- No loose or fixed foreign particles were visible on the transistor surfaces.

1. No evidence of any contaminants was found using energy dispersive X-ray analysis.

4.2.2 Assembled samples

Numerous particles of size greater than 1 μm were found on the surface and some were included in the oxide.

The particles fall into three distinct categories:

1. Particles such as silicon and aluminium which could be associated with assembly processes such as scribing and wire bonding. These particles were mostly larger than 10 μm and were generally loose.
2. Loose particles which could be removed by an ultrasonic solvent rinse which contained some or all of the following elements:

K Ca Mn Fe Ni Zn Mg S

These particles were generally in the size range 1 - 20 μm . Figure 2 gives a view of a contaminated device.

3. Particles, generally of small dimensions ($\approx 3 \mu\text{m}$) were either intimately attached to the wafer or dissolved in the oxide.

Analysis indicated the main contaminant to be iron (Fe), with small traces of the elements listed in 2, being observed.

Figure 3 shows the surface of the same device as in 2, after cleaning.

5. DISCUSSION

Surface contaminants can greatly affect electrical properties of transistors by both direct and indirect means. It must be noted that diffusion of contaminants is not exclusively a high temperature

phenomenon, it can take place at operating temperatures. The effects of surface contaminants can be found, in chapter 9 of "Physics of Semiconductor Devices" by S.M. Sze (Wiley-Interscience, 1969).

5.1 Immediate effects

In brief, immediate degradation of devices will result mainly from:

1. Junction degradation through pulsing.
2. Formation of spurious conduction channels either by field effect or direct doping.
3. Degradation of the oxide dielectric leading to instabilities and high leakage currents.
4. Impurities contaminating the bulk of the device which can act as traps that seriously degrade carrier lifetimes thus affecting both small and large signal parameters. (Gain, for example).

5.2 Long term hazards

Long term degradation of the device is a further risk as of the contaminants found, most are fast interstitial diffusers.

These will diffuse even under normal operating conditions and degrade device performance.

5.3 Secondary failures

Where large conductive foreign matter is found, (pieces of aluminium and silicon in this case), mechanical handling, in service shock etc. may cause metallization bridging.

In this case both primary and induced or secondary component failure may result.

6. RECOMMENDATIONS

6.1 Clean environment

Degradation as in 5.1 and 5.2 due to particulate matter can be almost entirely eliminated by performing all storage and assembly

operations under HEPA filters. HEPA filters remove 99.97% (or greater) of particles 0.5 μ m and larger. This is the range of sizes found on the samples.

Federal specifications 209A and 209B for class 100 conditions apply here.

6.2 Cleaning steps

Two cleaning steps could be used with advantage in the existing assembly procedure.

6.2.1 Die cleaning

The contaminants in 4.2.2 section 3 will probably be found to be deposited before the hot (450°C) die bond step.

A die rinse before the bond (but after wafer fracturing) is recommended.

6.2.2 Pre-encapsulation clean

Most contaminants fell into the category of 4.2.2 sections 1 and 2, and here a pre-encapsulation ultrasonic rinse of assembled headers in a solvent such as Freon TF will prove highly effective.

Note: Suitable die rinsing jigs are available from Finerware Inc. (Local agent SAETRA (Pty) Ltd. P O Box 950, Pretoria, 0001). NERRI can supply details of another system whereby lots of die are held in position by vacuum for cleaning.

S.A. Smith

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Microelectronics Department
NATIONAL ELECTRICAL ENGINEERING RESEARCH INSTITUTE

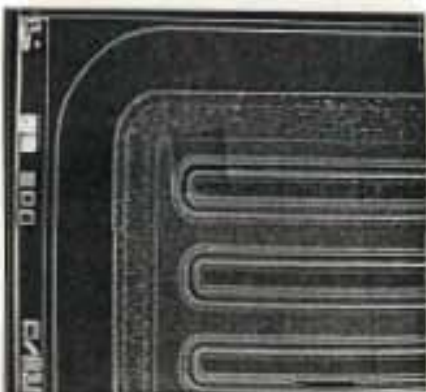


Figure 1 Wafer no. 1 from batch 1061. No evidence of contamination at wafer stage.

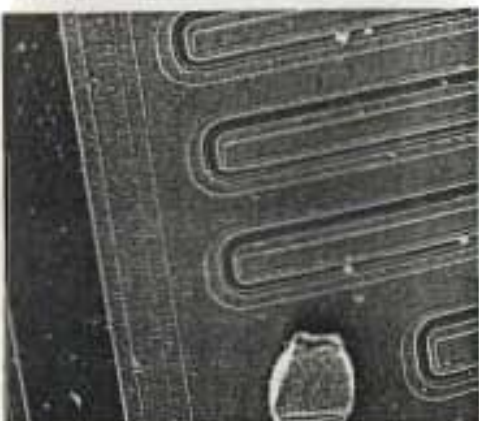


Figure 2 Assembled sample. Numerous contaminating particles. Contaminant in the outside is visible.

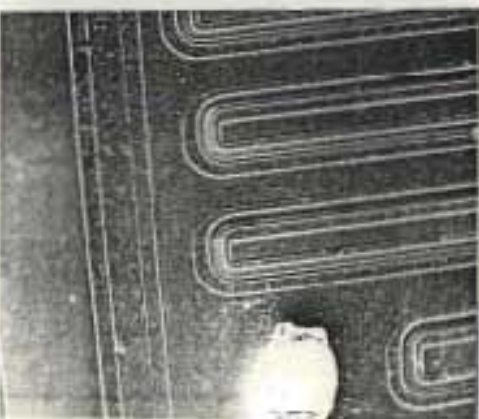


Figure 3 Same sample as in Figure 2 but after an ultrasonic solvent clean. Contamination was greatly reduced and remaining particles small. The oxide encapsulant remains.

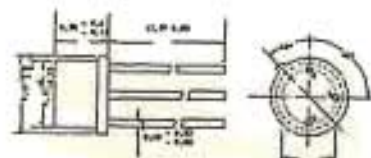
STC

ISSUE 1
PAGE 1

COMPONENTS DIVISION

P.O. BOX 286 BOKSBURG 1460
TEL: (011) 52-8311 TELEX B-3192 SA

STC

ELECTRONIC COMPONENTS OF ASSESSED QUALITY
BS CECC 50000 DETAIL SPECIFICATION
BASED ON CECC 50 000MANUFACTURER'S TYPE
NUMBER PTO18KPN SILICON CASE RATED
LOW FREQUENCY AMPLIFICATION
DARLINGTON CONNECTED
TRANSISTORS IN HERMETICALLY
SEALED METAL CASE

DIMENSIONS IN MILLIMETRES

10 - 39

ASSESSMENT LEVEL F

1. Limiting values (over the full temperature range unless otherwise stated).

	Min	Max	Unit
T_{case} Case operating temperature	-65,0	+125,0	°C
T_{stg} Storage temperature range	-65,0	+125,0	°C
V_{CB0} Collector-base continuous (direct) voltage		300	V
V_{CE0} Collector-emitter continuous (direct) voltage with zero base current		300	V
V_{EB0} Emitter-base continuous (direct) reverse voltage	10		V
I_C Continuous (direct) collector current		250	mA
P_{tot} Power dissipation: At $T_{case} = 25^\circ\text{C}$ *		1	W

* See fig. 1 - Derating curve

2/....

2. Characteristics at $T_{case} = 25^\circ\text{C} \pm 5^\circ$ unless otherwise stated.

Page 1

No.	PARAMETER	TEST CONDITION	VALUE		UNIT
			min	max	
1 ^a	$V_{BE(SAT)}$	$I_C = 100 \text{ mA}, I_B = 1 \text{ mA}$		2	V
2 ^a	$V_{CE(SAT)}$	$I_C = 100 \text{ mA}, I_B = 1 \text{ mA}$		1,6	V
3	$V_{CE(SUS)}$	$I_C = 10 \text{ mA}, I_B = 0$ $T < 250 \text{ ns}$	300		V
4	V_{CB0}	$I_C = 100 \text{ mA}, I_E = 0$	300		V
5	V_{EB0}	$I_B = 20 \text{ mA}, I_C = 0$	10		V
6	I_{CEO}	$V_{CE} = 240 \text{ V}, I_B = 0$		500	µA
7 ^b	I_{CBS}	$V_{CE} = 240 \text{ V}, V_{BE} = 0$		100	µA
8	I_{CBO}	$V_{CB} = 240 \text{ V}, I_E = 0$		5	µA
8 ^a	$I_{CBO(2)}$	$V_{CB} = 200 \text{ V}, I_E = 0$ $T_{case} = 100^\circ\text{C} \pm 3^\circ\text{C}$		500	µA
9	I_{EBO}	$V_{EB} = 6 \text{ V}, I_C = 0$		1	µA
10	$h_{FE(1)}$	$I_C = 100 \text{ mA}, V_{CE} = 1,8 \text{ V}$	800		-
11	$h_{FE(2)}$	$I_C = 125 \text{ mA}, V_{CE} = 3 \text{ V}$	1800		-

NOTES

- The saturation values in 1 and 2 are included to ensure that good contacts have been made to a device at probing and final test stages.
- A test for I_{CBS} has been included to ensure that the leakage in the clamp transistor is acceptable.

3/....

APPENDIX 3.6 THE FULL SPECIFICATION OF THE PTO18 ISSUED BY THE MANUFACTURER (ASSEMBLY PLANT)

MARKING

- Each transistor shall bear the following markings:
 - The manufacturer's type number: PT018
 - The factory identification code: S.T.C.
 - The date code.
- Each package containing one or more of these transistors shall bear all the above markings.
- Coding: PT018 indicates CS1R Die

Related documents

This specification shall be read in conjunction with:

BSE9000	'Specification of Basic Rules of Procedure.'
CECC 50000	'Harmonized system for quality assessment for electronic components: generic specification for discrete semiconductor devices'.

Ordering information

Orders for these transistors shall contain the following minimum information:

SILICON BIPOLAR DARLINGTON TRANSISTOR TYPE PT018

6. Test conditions and inspection requirements

NOTE: Devices subject to test marked 'D' shall not be accepted for release

EXCEPTION OR TEST	D NO	CECC 50000 ref.	Conditions at $T_{case} = 25^{\circ}C$ unless otherwise stated.	Inspection requirements				
				Quality level F				
				Limits		Units	IL	A.O.L.
Min.	Max							
<u>Subgroup A1</u>							1	1,5%
Visual inspection	ND	4.2.1.						
<u>Subgroup A2</u>							11	0,55%
Collector-base cut-off current $I_{CBO}(1)$	ND	4.3.4./ T-001	$V_{CB} = 240 V$ $I_E = 0$		5	μA		
Static value of Common-emitter forward-current transfer ratio $h_{FE}(1)$	ND	4.3.4./ T-006	$V_{CE} = 1,8 V$ $I_C = 100 mA$	800				
$h_{FE}(2)$			$V_{CE} = 3 V$ $I_C = 125 mA$	1800				
Base-emitter saturation voltage $V_{BE}(sat)(1)$	ND	4.3.4./ T-004	$I_B = 1 mA$ $I_C = 100 mA$		2,0	V		
<u>Subgroup A3</u>							1	2,5%
Collector-emitter saturation voltage $V_{CE}(sat)(1)$	ND	4.3.4./ T003	$I_B = 1 mA$ $I_C = 100 mA$		1,6	V		

APPENDIX 3.6 THE FULL SPECIFICATION OF THE PT018 (CONTINUED)

by lot.

Note: P = Periodicity in months, n = sample size, c = acceptance criteria

DESCRIPTION	D NO	CECC 50000 ref.	Conditions at T _{case} = 25°C unless otherwise stated	Inspection requirements					Explanation of test	D NO	CECC 50000 ref.	Conditions at T _{case} = 25°C unless otherwise	Inspection requirements								
				Quality level F									Quality level F								
				Limits		Units	IL	A.O.L.					Limits		Units	P	n	c			
Min.	Max.	Min.	Max.																		
Subgroup B1 Dimensions	ND	4.2.2.7 App. III	BS 3936 50-134					52	2,5%	Subgroup C1 Dimensions	ND	4.2.2./App. III							3	8	1
Subgroup B3 Bending	D	4.4.9	F = 2,5 N	No damage				53	2,5%	Subgroup C2b Collector-base cut-off current	ND	4.3.4/T-008	T _{case} = 100°C V _{CB} = 200 V	500	µA				3	18	1
Subgroup B4 Durability ageing	ND	BS 2011 Test Ta Method 1	16 h at 155°C dry heat	Good wetting				54	2,5%	Subgroup C3 Tensile strength	D	4.4.9	F = 2,5 N	No damage					3	8	1
Subgroup B5 Age of moisture removed by accelerated heat ageing (ferred)	ND	4.4.4.	-65 to + 125°C IEC 68-2-14, Test Na					54	2,5%	Subgroup C4 Resistance to soldering heat	D	4.4.8							3	18	1
Subgroup B5 Electrical tests (1)	ND	4.3.4/T-001 4.3.4/T-006	Conditions and limits as for subgroup A2							Electrical tests I _{BO} (1) I _{YC} (1)	ND	4.3.4/T-001 4.3.4/T-006	Conditions and limits as for subgroup A2.								
Subgroup B6 Electrical tests (1)	ND	4.3.4/T-001 4.3.4/T-001	Conditions as for subgroup A2					54	1,5%	Subgroup C6 Shock Vibration Electrical tests	ND	4.4.5 4.4.6	14 700 m/s² for 0,5 ms F = 100-2000 Hz at 196 m/s²						3	8	1
										I _{BO} (1) I _{YC} (1)	ND	4.3.4 /T-008 4.3.4/T-006	Conditions and limits as for subgroup A2								
								512 1152													

APPENDIX 3.6 THE FULL SPECIFICATION FOR THE PTO18 (CONTINUED)

NOTATION Attributes information for subgroups B3, B4, B5 and B6

P = Periodicity in months, n = sample size, c = acceptance criteria

Designation	D NO J.S.C	IEEE 50000 Ref.	Conditions at $T_{case} = 25^{\circ}C$ unless otherwise stated	Inspection requirements					
				Quality level F					
				Limits		Units	P	n	c
Min.	Max.								
Subgroup C7 Accelerated temp st	D	4.4.2	Method 1 20 cycles				3	10	1
Electrical tests B(1)	NO	4.3.4./ 1-001	Conditions and limits as for subgroup B8						
B(2)		4.3.4./ 1-006							
Subgroup C8 Electrical survival	NO	4.5	See page 10 for conditions of test. Duration 1000 hours.				3	34	2
Electrical Ea	NO								
Ea(1)		4.3.4./ 1-001	Conditions and limits as for subgroup B8						
Ea(2)		4.3.4./ 1-006							
Subgroup C9 Storage at high temperature	D	4.4.1	$T_{stg} = 125^{\circ}C$ Duration 1000 hours.				3	34	2
Electrical tests E(1)	NO	4.3.4./ 1-001	Conditions and limits as for subgroup B8						
E(2)		4.3.4./ 1-006							
REMARKS	Attributes information for subgroups C7, C8, C9 and C9 Measurements information for $I_{CBO(s)}$, $h_{FE(1)}$ and $h_{FE(2)}$ before and after subgroup C8.								

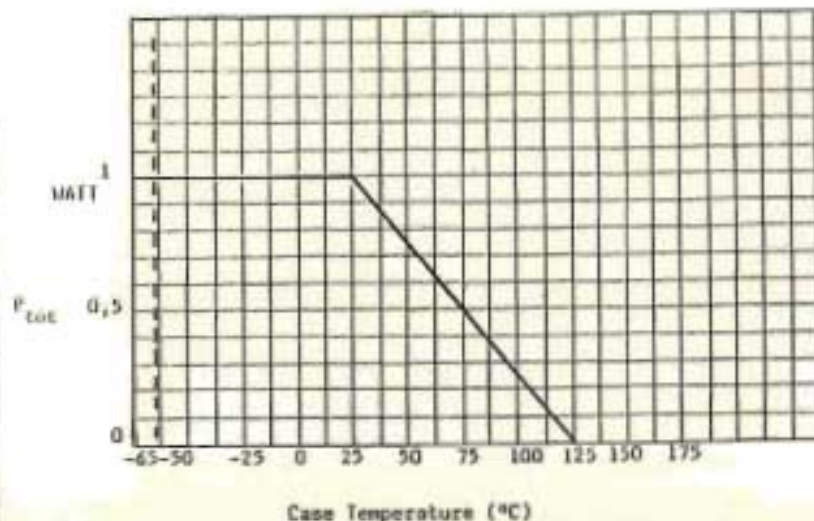


Fig. 1 - Derating curve

SOLDERING

Soldered connections may be close to the seals of the pins provided that care is taken to conduct excessive heat away.

The pin temperature during soldering should not exceed 235°C for a maximum period of 10 seconds.

The case should never be soldered to a heat sink as the heat required would permanently damage the transistor.

Equipment should be switched off before this transistor is either connected or disconnected in the circuit. Unless this precaution is taken the transistor may be permanently damaged by high transients.

Typ. Unit

Thermal resistance: Junction to case °C/W

Endurance Conditioning

Reverse bias (Half the samples). Temperature 100 ± 3°C in oil bath with reverse bias applied.

Forward bias (Half the samples). Ambient temperature to be set such that the junction temperature = 125°C when the transistor collector dissipation is 200 mW.

APPENDIX 3.6 THE FULL SPECIFICATION OF THE PTO18 (CONTINUED)

```

C *****PROGRAMME TO CALCULATE COLLECTOR CURRENT OF A DISCRETE*****
C *****TRANSISTOR AS A FUNCTION OF VCE USING MODEL 2 AND WITH*****
C *****CORRECTIONS FOR BOTH HIGH INJECTION AND TEMPERATURE EFFECTS***
C
C *****MODEL 2 CONSTANTS FOR A PTO14*****
VCO=0.2
RC=28.
RQS=70.
VE=1000
HFEM=112.5
C
C *****HIGH INJECTION CORRECTION PARAMETERS FOR A PTO14*****
AREA=.45
CJCRIT=0.6
B=-1.21
CC=D*.617
CJ=0.
C
C *****TEMPERATURE AT WHICH CONSTANTS WERE MEASURED*****
T0=20
C
C *****OPERATING TEMPERATURE AND TEMPERATURE COEFFICIENTS*****
T=120
DHFE=5.E-03
DRC=6.98-03
DRQS=5.E-03
C
C *****PROGRAMME CONSTANTS*****
EYEB=.000533
VCE=0.02
VCEINC=1.01
VSTOP=10.
EYECMVE=0.
EJ=0
C
C *****CORRECT HFEM, RC, AND RQS FOR TEMPERATURE*****
VCT=(T-273)*8.616E-5
IF(T.RQ.TD)GO TO 1
DELT=T-T0
HFEM=HFEM*(1+DELT*DHFE)
RC=RC*EXP(DELT*DRC)
RQS=RQS*EXP(DELT*DRQS)
WRITE(6,*)DELT, HFEM, RC, RQS, VCT
HFEMPREV=HFEM
HFEM1=HFEM
C
C *****SET ITERATIONS*****
DO 2 WHILE(VCE.LT.VSTOP)
K=0
C
C *****CHECK IF TRANSISTOR IS IN ACTIVE REGION*****
IF(VCE.LT.VCT)GO TO 3
C
C *****CALCULATE IC MAX*****
IF(EYECMVE.GT.0) GO TO 7

```

```

4 EYECM=HFEMPREV*EYEB
E=K+1
CJM=EYECM/AREA
C
C *****CHECK IF JC > JCCRIT FOR GAIN DROOP*****
IF(K.GT.1) GO TO 5
IF(CJM.LT.CJCRIT)GO TO 6
C
C *****CALCULATE GAIN ABOVE JCCRIT*****
CJ=CJM
IF(CJ.RQ.0.) GO TO 2
HFEM=HFEM1*EXP(D*LOG(CJ)+CC)
HFEM=(HFEM+9*HFEMPREV)/10
IF(HFEM.GT.HFEM1)HFEM=HFEM1
IF(SQRT((HFEMPREV-HFEM)**2).LT.0.01)GO TO 14
HFEMPREV=HFEM
GO TO 4
14 EJ=EJ+1
IF(EJ.LT.2)WRITE(6,*)'DEVICE ENTERING GAIN DROOP'
HFEMPREV=HFEM
EYECM=HFEM*EYEB
EYECMVE=(EYECM*RC+VE)*EYECM/VE
C
C *****CHECK IF IN QUASI-SATURATION*****
IF(VCE-(EYECMVE*RC))8,10,11
C
C *****CHECK IF IN CUT-OFF REGION*****
IF(VCE.LT.VCO)GO TO 9
C
C *****CALCULATE IC IN QUASI-SATURATION*****
EYEC=EYECMVE-(((EYECMVE*RC)-VCE)/RQS)
GO TO 12
C
C *****CALCULATE VALUE OF IC IN CUT-OFF REGION*****
EYECO=EYECMVE-(((EYECMVE*RC)-VCO)/RQS)
EYEC=(VCE-VCT)/(VCO-VCT)*EYECO
GO TO 12
C
C *****SET IC = TO ICMAI AT CHANGE TO NORMAL OPERATING REGION*****
EYEC=EYECMVE
GO TO 12
C
C *****CALCULATE IC IN NORMAL REGION USING EARLY VOLTAGE*****
EYEC=(VCE+VE-EYECMVE*RC)*EYECMVE/VE
GO TO 12
C
C *****SET IC = 0 BELOW CUT-OFF*****
EYEC=0.0
C
C *****PRINT RESULTS*****
10 WRITE(6,13)VCE,EYEC
WRITE(7,13)VCE,EYEC
13 FORMAT(F12.6,F12.6)
2 VCE-VCT*VCEINC
STOP
END

```

APPENDIX 4.2 CONSTANTS FOR COMPUTATION

Unless otherwise indicated on graphs or in the text the computation constants given in this appendix apply.

1. Collector-emitter voltage V_{CE}
 The values used for the PT018 were the two limiting operating voltages used were :
 1,8 V for the O.N. condition
 3.0 V for the Impulsing condition
2. h_{FEM} - The process gain measured on a discrete device below gain crowding at high injections with V_{CE} just above V_K .
 For the PT018 values of process gain were 60 or 180
3. Conduction threshold voltage - V_{CT} .
 A value of $V_{CT} = kT/q = (Temp + 273) \times 8.616 \times 10^{-5}$ was found to give good correlation with measured characteristics in simulations.
4. Region 1 (Cut-off voltage - V_{CO})
 The default value of $V_{CO} = 0,2$ V was found to give good results.
5. Region 2 (Quasi-saturation and collector resistance)
 Typical values for computation were as below.
 For the PT018 $R_{QS} = 120$ ohms
 $R_C = 80$ ohms
 For the PT014 $R_{QS} = 60$ ohms
 $R_C = 40$ ohms
6. Region 3 (Early Voltage - V_E)
 A default value of $V_E = 1\ 000$ V was used.
7. Base resistance of the PT018 output transistor - R_{B2}
 A default value of 6 ohms was used.

APPENDIX 4.2 CONSTANTS FOR COMPUTATION (CONTINUED)

8. The constant K in the V_{BE} equation.

A default value of 0,86 was used and was based on the measurements carried out on a number of transistors.

(Note : A further constant '1' was used as kT/lq in the V_{BE} equation and it was possible to obtain a better fit to measured values. A typical value of $l = 0,8$ was found to be suitable. In practice the default value of $l = 1$ was used as '1' only changed the performance of the simulated Darlington at very low values of V_{CE}).

9. The active areas of devices

PT018 Output stage : $0,6 \text{ mm}^2$ and driver stage : $0,1 \text{ mm}^2$

PT014 $0,45 \text{ mm}^2$

10. Constants for gain crowding at high injection levels

PT018 $J_C(\text{CRIT}) = 0,65 \text{ A/mm}^2$ and $D = -2$.

PT014 $J_C(\text{CRIT}) = 0,6 \text{ A/mm}^2$ and $D = -1.21$

11. Temperature correction of h_{FE} , R_C , R_{QS} and V_{BE2}

The temperature correction equations used for the first three parameters are given in Figure 4.15 (page 141) and the equation for V_{BE2} is given in equation 4.6a. The figures given below may be used for both the PT104 and PT018.

$h_{FE} : K_1 = 5 \times 10^{-3}/^\circ\text{C}$ $R_C : K_2 = 7 \times 10^{-3}/^\circ\text{C}$

$R_{QS} : K_3 = 5 \times 10^{-3}/^\circ\text{C}$

A default value of temperature of 25°C was used.

12. The area ratio N' of the PT018 was taken as 6 except when N' was used as a variable.

13. Other constants used were normally specific to the computer program and are listed in the text, where applicable.

APPENDIX 4.3 BASE EMITTER VOLTAGE V_{BE2} OF THE PT018 TRANSISTOR

In this section the expression for the forward base-emitter voltage of a bipolar transistor operating in the active region is derived in order that the collector-emitter voltage of the driver stage of the PT018 Darlington might be calculated. The derivation is taken in part from section 14.2.1.1 (pages 324/5) of 'The theory and practice of Microelectronics' by S K Ghandi (John Wiley and Sons, New York, 1968. SBN 471 29718 6).

Note: A list of symbols appears at the bottom of this page

1. Derivation of the expression for the base-emitter voltage

Let the base current be I_B , then

$$\begin{aligned} I_B &= I_n + I_p \text{ and from the above reference} \\ &= qA[DnB \times nB/WB + DpE \times pE/LpE]\{\exp(q \times V'_{BE}/kT) - 1\} \\ &= K'\{\exp(q \times V'_{BE}/kT) - 1\} \end{aligned}$$

Re-arranging

$$V'_{BE} = kT/q \times \ln(I_B) + K \quad \dots\dots\dots A1$$

Taking into account base series resistance the external base-emitter voltage is

$$\begin{aligned} V_{BE} &= V'_{BE} + R_B \times I_B \\ &= kT/q \times \ln(I_B) + R_B \times I_B + K \quad \dots\dots\dots A2 \end{aligned}$$

2. Guidelines for measurements to obtain K and R_B for silicon devices

1. The transistor must be active with the collector set at the transition from region 2 to region 3 of Model 2 for these measurements.
2. At a value of I_B giving $V_{BE} < 0,6$ V measure V_{BE} and I_B
3. At a value of I_B giving $V_{BE} > 0,9$ V measure V_{BE} and I_B
4. Use the results of 2. in equation A1 to find K
5. Use the results of 3. and K in equation A2 to find R_B

3. List of symbols

- A = Active area
- DnB = Diffusion constant for electrons in base
- DpE = Diffusion constant for holes in the emitter
- I_B = total base current
- I_n = Contribution of electrons to base current
- I_p = Contribution of holes to base current
- K = A constant
- K' = A constant
- k = Boltzmann's constant
- LpE = Diffusion length of holes in emitter
- nB = Equilibrium concentration of electrons in base
- pE = Equilibrium concentration of hole in emitter
- q = Electronic charge
- T = Absolute temperature in degrees Kelvin
- V_{BE} = Voltage between emitter and base terminals of transistor in forward biased condition
- V'_{BE} = Contribution to V_{BE} by carriers

```

C *****PROGRAMME TO CALCULATE THE COLLECTOR CURRENT OF AN*****
C *****INTEGRATED DARLINGTON TRANSISTOR AS A FN OF VCE*****
C *****WITH CORRECTION FOR HIGH INJECTION LEVELS AND TEMPERATURE**
C
C *****MODEL 2 PARAMETERS FOR THE DARLINGTON*****
C
VCE= .2
VE=1000.
HFEM=63.
RQS=120.
RC=80.
C
C *****OTHER DARLINGTON PARAMETERS AND CONSTANTS*****
C
RD2=.6.
EN=.6.
CAY=.86
AREAZ=.6
AREAZ1=AREAZ/EN
CJCRIT=.65
D=.2
CC=D*.416
EL=.8
C
C *****TEMPERATURE AT WHICH DEVICE PARAMETERS WERE MEASURED*****
C
TD=20
C
C *****OPERATING TEMPERATURE AND TEMPERATURE COEFFICIENTS*****
C
T=25
DHFE=5.E-03
DRC=6.9E-03
DRQS=5.E-03
C
C *****PROGRAMME CONSTANTS*****
C
VCE=0.5
EYEB1=.000125
VCEINC=1.01
VCEST=400.
T=23.
I=.0001
N=0
K1=0
K2=0
HFEM111=0.
RELAX=2
STABNO=20

```

```

C *****CORRECT HFEM, RC AND RQS FOR TEMPERATURE*****
C
VCT=(T+273)*8.616E-05
IF(T,RQ,TD)GO TO 1
DELT=T-TD
HFEM=HFEM*(1+DELT*DHFE)
RC=RC*EXP(DELT*DRC)
RQS=RQS*EXP(DELT*DRQS)
WRITE(6,*)DELT, HFEM, RC, RQS, VCT
C
C *****SET ITERATIONS*****
C
DO 2 WHILE(VCE.LT.VCEST)
C
C *****SET TRIAL VBE2*****
C
JL=0
M=N+1
IF(M.LT.2)VBE2=0.45
VCE1=VCE-VBE2
C
C *****CALL FUNCTION TO CALCULATE IC1 AT ESTIMATED VCE1*****
C
EYEC1=DRI(AREAZ,CC,D,CJCRIT,VCE,VCT,RC,RQS,EN,HFEM,VE,VCE1,
1 EYEB1,HFEM111,K1)
IF(EYEC1)2,2,4
EYEB2=EYEC1+EYEB1
VBE2CALC=(8.3E-5*(T+273)/EL)*LOG(EYEB2)+EYEB2*RD2+CAY
C
C *****TAKE MEAN OF NEW VBE2 AND PREVIOUS AND CHECK FOR STABILITY*****
C
VBE2CALC=(VBE2CALC+VBE2*(RELAX-1))/RELAX
JL=JL+1
IF(JL.GT.STABNO)THEN
RELAX=RELAX*2
JL=0
WRITE(6,*)'RELAXING VBE2 CONVERGENCE'
END IF
C
C *****CHECK CHANGE IN VBE IS < I *V*****
C
IF(SQRT((VBE2CALC-VBE2)**2).GT.X)THEN
VBE2=VBE2CALC
GO TO 3
END IF
VBE2=VBE2CALC

```

```

C *****CALCULATE COLLECTOR CURRENT OF OUTPUT DEVICE*****
C
1 EYEC=OUT(AREAS,CC,D,CJCRIT,VCO,VCT,RC,RQS,HFEM,VE,VCE,EYEB2,
  HFEM2,K2)
  BZ=EYEC/EYEB2
  EYECB=EYEC+EYEB1
  GAIN=EYECB/EYEB1
  WRITE(6,5)VCE,EYECB,GAIN
  WRITE(7,5)VCE,EYECB,GAIN
  FORMAT(F14.3,F14.6,F14.6)
  VCE=VCE*VCEINC
  STOP
  END
C
C *****FUNCTION TO CALCULATE COLLECTOR CURRENT OF*****
C *****DRIVER TRANSISTOR*****
C
1 FUNCTION DRI(AREA1,CC,D,CJCRIT,VCO,VCT,RC,RQS,EN,HFEM,VE,
  VCE1,EYEB1,HFEM11,K1)
C
C *****CALCULATE RC AND RQS OF THE DRIVER*****
C
  IF(HFEM11.GT.0)GO TO 112
  RC=EN*RC
  RQS1=EN*RQS
  HFEMPR1=HFEM
  HFEM1=HFEM
  HFEM11=HFEM
  ED=0
C
C *****CHECK IF TRANSISTOR IS IN ACTIVE REGION*****
C
  IF(VCE1.LT.VCT)GO TO 109
C
C *****CALCULATE IC MAX*****
C
100 EYECM1=HFEMPR1*EYEB1
  CJM1=EYECM1/AREA1
C
C *****CHECK IF CJM1 > CJCRIT*****
C
  IF(ED.GT.1)GO TO 107
  IF(CJM1.LT.CJCRIT)GO TO 108
C
C *****CALCULATE GAIN ABOVE JCRIT*****
C
107 CJ1=CJM1
  ED=ED+1
  HFEM11=HFEM1*EXP(D*LOG(CJ1)+CC)

```

4/.....

```

  HFEM11=(HFEM11+5*HFEMPR1)/10.
  IF(HFEM11.GT.HFEM1)GO TO 109
  IF(SQRT((HFEMPR1-HFEM11)**2)-.01)110,110,111
109 HFEM11=HFEM1
111 HFEMPR1=HFEM11
  GO TO 100
110 K1=K1+1
  IF(K1.LT.2)WRITE(6,*)'DRIVER IN GAIN SHOOP'
  HFEMPR1=HFEM11
  EYECM1=HFEMPR1*EYEB1
  EYECM1VE=(EYECM1*RC1+VE)*EYECM1/VE
  HFEM111=HFEM11
C
C *****CHECK IF IN QUASI-SATURATION*****
C
112 IF(VCE1-(EYECM1VE*RC1))101,103,104
C
C *****CHECK IF IN CUT-OFF REGION*****
C
101 IF(VCE1.LT.VCO)GO TO 102
C
C *****CALCULATE IC IN QUASI-SATURATION*****
C
  EYEC1=EYECM1VE-(((EYECM1VE*RC1)-VCE1)/RQS1)
  GO TO 106
C
C *****CALCULATE VALUE OF IC IN CUT-OFF REGION*****
C
102 EYEC01=EYECM1VE-(((EYECM1VE*RC1)-VCO)/RQS1)
  EYEC1=(VCE1-VCT)/(VCO-VCT)*EYEC01
  GO TO 106
C
C *****SET IC = TO ICHAF AT CHANGE TO NORMAL OPERATING REGION*****
C
103 EYEC1=EYECM1VE
  GO TO 106
C
C *****CALCULATE IC IN NORMAL REGION USING EARLY VOLTAGE*****
C
104 EYEC1=(VCE1+VE-EYECM1VE*RC1)*EYECM1VE/VE
  GO TO 106
C
C *****SET IC1 = 0 BELOW CUT-OFF*****
C
105 DRI=0.0
  RETURN
C
C *****NEW VALUE OF IC1*****
C
106 DRI=EYEC1
  RETURN
  END

```

5/.....

APPENDIX 4.4 FORTRAN LISTING FOR DARLINGTON (CONTINUED)

```

C *****FUNCTION TO CALCULATE COLLECTOR CURRENT*****
C *****OF OUTPUT TRANSISTOR*****
C
FUNCTION OUT(AREAZ,CC,D,CJCRIT,VCC,VCT,RC,RQS,HPFM,VE,VCE,ETERNZ,
1 HPFM2,K2)
HPFM2=HPFM
HPFM0=HPFM
HPFM2=HPFM
KO=0
C
C *****CHECK IF TRANSISTOR IS IN ACTIVE REGION*****
C
IF(VCE.LT.VCT)GO TO 206
C
C *****CALCULATE IC MAX*****
C
208 EYECM=HPFM2*EYEC
CJM=CJCRIT/AREAZ
C
C *****CHECK IF CJM > CJCRIT*****
C
IF(KO.GT.1)GO TO 208
IF(CJM.LT.CJCRIT)GO TO 209
C
C *****CALCULATE GAIN ABOVE JOCRIT*****
C
208 CJ2=CJM2
KO=KO+1
HPFM2=HPFM*EXP(D*LOG(CJ2)+CC)
HPFM2=(HPFM2+9*HPFM2)/10.
IF(HPFM2.GT.HPFM)GO TO 203
IF(SQRT((HPFM2-HPFM)**2)-.01)201,201,202
202 HPFM2=HPFM2
GO TO 208
203 HPFM2=HPFM
201 K2=K2+1
IF(K2.LT.2)WRITE(6,*)'OUTPUT IN GAIN DROOP'
209 HPFM2=HPFM2
EYECM=HPFM2*EYEC
EYECVE=(EYECM*RC+VE)*EYECM/VE
C
C *****CHECK IF IN QUASI-SATURATION*****
C
IF(VCE-(EYECM*RC))204,205,207
C
C *****CHECK IF IN CUT-OFF REGION*****
C
204 IF(VCE.LT.VCC)GO TO 210

```

APPENDIX 4.4 FORTRAN LISTING FOR DARLINGTON (CONTINUED)

```

C *****CALCULATE IC IN QUASI-SATURATION*****
C
202 EYEC=EYECM-((EYECM*RC)-VCE)/RQS
GO TO 211
C
C *****CALCULATE VALUE OF IC IN CUT-OFF REGION*****
C
210 EYEC0=EYECM*VE-((EYECM*RC)-VCC)/RQS
EYEC=(VCE-VCT)/(VCC-VCT)*EYEC0
GO TO 211
C
C *****SET IC = TO ICNEX AT CHANGE TO NORMAL OPERATING REGION*****
C
205 EYEC=EYECM
GO TO 211
C
C *****CALCULATE IC IN NORMAL REGION USING EARLY VOLTAGE*****
C
207 EYEC=(VCC-VE-EYECM*RC)*EYECM/VE
GO TO 211
C
C *****SET IC2 = 0 BELOW CUT-OFF*****
C
206 OUT=0.0
RETURN
C
C *****END VALUE OF IC1*****
C
211 OUT=EYEC
RETURN
END

```

APPENDIX 4.4 FORTRAN LISTING FOR DARLINGTON TRANSISTOR (CONTINUED)

A METHOD FOR DESIGNING THE COLLECTOR REGION OF MEDIUM-POWER TRANSISTORS

