REAL-TIME SIMULATOR STUDIES AND MODEL DEVELOPMENT FOR TIME-DOMAIN VOLTAGE STABILITY ANALYSIS

By

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I hereby declare that all the material incorporated into this thesis is my own original unaided work except where specific reference is made by name or in the form of a numbered reference. The work contained herein has not been submitted for a degree at any other university.

Signed:_____

J K Makasa

This thesis is dedicated to my family, notably Buyi, Blandina, Annie, Lwamba, Chikwe, Bwalya, Mutale and Mulenga and to the memory of Shephard and Henry.

ABSTRACT

Problems of voltage stability and voltage collapse have become a major concern in power system planning and operation in recent years, often as a result of power systems being operated under much more stressed conditions than was usual in the past. Factors that are responsible for this trend include: environmental pressures on transmission expansion; increased electricity consumption in concentrated heavy loads where installation of new generation is not feasible; new system loading patterns. Voltage stability problems are characterised by either slow or sudden voltage drops, sometimes escalating further to a collapse in voltage, leading, in some cases, to system wide blackouts. The power engineering community has devoted significant effort to developing new analysis tools and methods to control this type of instability. The main methods that have been developed and used for analysis of voltage stability are steady-state methods (power flow: analysis via P-V and Q-V curves); dynamic analysis (time-domain simulations); modal analysis of system jacobian matrices and optimization (special optimal power flow).

This thesis investigates the use of a particular tool, real time simulation, as a method for voltage stability analysis and testing of voltage control strategies. The particular simulator used is the Real-Time Digital Simulator (RTDS) from RTDS Technologies. The real-time simulator software environment provides generalized models of generation, transmission, distribution plant and loads that can be used to develop accurate models of power systems for analysis in real-time. The broad objectives of this thesis are to assess the suitability of the RTDS as a tool for time domain voltage stability analysis and to develop additional real-time models of particular power system controllers that are known to play a key role in voltage stability phenomena. In particular the thesis considers development of custom real-time models of a transformer on-load tap changer (OLTC) controller, detailed generator excitation controls (automatic voltage regulators), a static var compensator (SVC) controller and a synchronous condenser reactive output controller.

The thesis then describes the development of real-time models of two benchmark systems for the voltage stability studies: a well known 11-bus voltage stability benchmark system and a smaller (4-bus) benchmark system. These two benchmark systems are used to establish the validity and correctness of the custom real-time models and to investigate

simple compensation and control strategies for voltage stabilization. In particular the thesis considers the following stabilizing techniques on the 11-bus system: switched shunt capacitor compensation, voltage control using a synchronous condenser and finally the use of an SVC.

Finally, the thesis demonstrates the ability of RTDS to investigate the performance of actual hardware controllers on the plant in the real-time model of the 11 bus system in a full closed loop arrangement. The custom-developed real-time software model of the OLTC controller in the 11-bus benchmark system is replaced with an actual external hardware controllers connected in closed loop with the real-time simulation.

This thesis has successfully confirmed the known characteristics of individual power system plant using the models provided in the RTDS environment and developed additional customized software models of controllers for voltage stability studies on the RTDS. The results of the RTDS simulations of voltage stability benchmark systems have been found to agree with documented results of these systems. The thesis has shown that the RTDS provides a suitable platform on which time-domain voltage stability studies can be conducted. The thesis has also shown that real-time digital simulation is a practicable technique for the analysis and investigation of control strategies for voltage stability, particularly when interactions between real hardware controllers and their impact on system stability are of concern.

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TABLE OF CONTENTS

Abstract.....i

Acknowledgements.....iii

List of Symbols.....vii

CHAPTER ONE INTRODUCTION

1.1 General.....1.1

1.2 Thesis Background and Objectives.....1.5

1.3 Thesis Layout.....1.7

1.4 Main Findings and Achievements of the Thesis.....1.8

1.5 Research Publications.....1.9

CHAPTER TWO REVIEW OF REAL-TIME SIMULATION AND THE VOLTAGE STABILITY PROBLEM

2.1 Introduction.....2.1

2.2 Real-Time Simulation.....2.2

2.3 Fundamental Concepts Related To Voltage Stability.....2.5

2.3.1 Time scales.....2.5
2.3.2 Transmission system characteristics.....2.6
2.3.3 Load characteristics.....2.9
2.3.4 Effect of transformer on-load tap changers.....2.12
2.3.5 Reactive power transfer.....2.12
2.3.6 Effect of reactive power compensation.....2.13
2.3.7 Generator characteristics.....2.15

2.4 A Review Of Methods Of Voltage Stability Analysis.....2.16

2.5 Countermeasures Against Voltage Instability.....2.17

2.6 Conclusion.....2.18

CHAPTER THREE REAL-TIME MODELING FOR VOLTAGE STABILITY ANALYSIS

3.1 Introduction.....3.1

3.2 Transmission Line Model.....3.1

3.3 Load Models.....3.6

3.3.1 Polynomial load model.....3.6
3.3.2 Exponential load model.....3.8

3.4 Transformer On-Load Tap Changer.....3.10

3.5 Generator Excitation Control System Modelling 3.12
3.5.1 AVR modelling 3.13
3.5.2 Overexcitation limiter 3.13
3.5.3 Synchronous condenser model 3.15
3.6 Static Var Compensator 3.18
3.6.1 SVC Parameters and specifications 3.22
3.6.2 SVC control 3.23
3.6.3 Real-time model of SVC 3.24
3.7 Conclusion 3.26

CHAPTER FOUR REAL-TIME VOLTAGE STABILITY BENCHMARK SYSTEM STUDIES

4.1 Introduction 4.1
4.2 Small Benchmark System 4.1
4.2.1 System description 4.2
4.2.2 Small Benchmark system modeling 4.2
4.2.3 Simulation results 4.6
4.3 Study of an 11-Bus Benchmark System 4.7
4.3.1 System Description 4.7
4.3.2 System Modeling 4.8
4.3.3 11-Bus Benchmark System Data 4.9
4.3.4 Simulation results 4.12
4.4 Conclusion 4.17

CHAPTER FIVE COUNTERMEASURES AGAINST VOLTAGE INSTABILITY

5.1 Introduction 5.1
5.2 Voltage control by switched shunt capacitor compensation 5.1
5.3 Synchronous condenser compensation 5.15
5.4 Static var compensator 5.26
5.5 Conclusion 5.33

CHAPTER SIX CLOSED LOOP TESTING OF A PHYSICAL CONTROL DEVICE FOR VOLTAGE STABILITY ANALYSIS

6.1 Introduction 6.1
6.2 RTDS Input and Output 6.2
6.2.1 Analogue output 6.2
6.2.2 Digital input 6.2
6.3 The REG-DA Voltage Regulator 6.3

6.4 RTDS Hardware-in-loop Testing of the REG-DA Voltage Regulator 6.5

6.5 RTDS Simulation Results 6.9

6.5.1 Results of the all-software 11-bus voltage stability benchmark system 6.11
6.5.2 Results of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator 6.16

6.6 Conclusion 6.20

CHAPTER SEVEN CONCLUSION 7.1

APPENDIX A SMALL BENCHMARK SYSTEM RSCAD/DRAFT DATA A.1

APPENDIX B 11-BUS BENCHMARK SYSTEM RSCAD/DRAFT DATA B.1

REFERENCES R.1

LIST OF SYMBOLS

The commonly used symbols and notations adopted in this thesis are listed below. Other symbols used in the text are explained where they first occur.

Acronyms

AC	alternating current
AVR	Automatic Voltage Regulator
DC	direct current
DSP	Digital Signal Processor
EMTP	Electromagnetic Transients Program
FACTS	Flexible AC Transmission System
FC	Fixed Capacitor
HV	High voltage
HVDC	High Voltage Direct Current
LV	Low voltage
OLTC	on-load tap changer
PSS\E	Power System Simulator for Engineering
RSCAD	Real-time Simulation Computer Aided Design
RTDS™	Real-Time Digital Simulator
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
TCR	Thyristor Controlled Reactor
TSC	Thyristor Switched Capacitor

Symbols related to generator excitation control

V_{fd}	Field voltage
V_t	generator terminal voltage
V_{REF}	AVR reference voltage
$V_{R\,MAX}$	maximum field voltage
I_{fd}	field current

$I_{fd\ max}$	maximum field current
$I_{fd\ max\ 1}$	maximum field current low set
$I_{fd\ max\ 2}$	maximum field current high set
V_{oxl}	overexcitation limiter output voltage

Symbols related to reactive power control equipment

X_C	reactance of compensating equipment
Q_C	reactive power supplied by compensating equipment
α	thyristor firing angle
σ	conduction angle
X_L	TCR reactance at fundamental frequency
B_L	TCR susceptance at fundamental frequency

General

pu.	per unit
x_o	signifies the nominal value of variable x
$\mathbf{x}$	signifies a vector of variables x
$\dot{x}$	signifies the first derivative of x with respect to time
x_{set}, x_{ref}	signifies the set value or the reference value of an input variable x

CHAPTER ONE

INTRODUCTION

1.1 General

The first stability problems encountered in power systems were primarily those concerned with transient angle stability. However with the changing characteristics of power systems, other stability problems, particularly voltage stability have emerged as a great source of concern in maintaining system stability [1]. Factors that have lead to problems of voltage stability include increased system loadings following the increase in demand for electricity, restrictions on building new infrastructure, desire to maximise power transfer through existing transmission systems and new system loading patterns due to deregulation of the electricity market [1]. As a result of these and other factors power system utilities have been faced with new stability limitations in transmitting electricity. Many mature power systems around the world have experienced a number of voltage instability and voltage collapse incidents. These voltage stability problems have been responsible for several major blackouts in these power systems. The following are some examples [2,3,4]:

- Japanese system disturbance, July 23 1987, August 22, 1970;
- French system disturbances of January 12, 1987, December 19, 1978 November 10, 1976, December 9, 1965;
- Western Tennessee, USA disturbance of August 22, 1987;
- Florida system disturbances, USA, September 2, November 26, December 28, December 30, 1982;
- Belgian system disturbance of August 4, 1982;
- New York power pool disturbances of September 22, 1970;
- Winnipeg, Canada Nelson River HVDC link April 13, 1986;
- SE Brazil, Paraguay Itaipu HVDC link November 30, 1986;
- Western USA, July 02, 1996.

The disturbances on the Japanese system on July 23, 1987 were caused by unfavourable loading conditions. The weather was very hot and loads were abnormally high. After the noon hour, loads increased at 400MW/minute. Despite connection of all available shunt capacitors, the voltage decayed, with voltage on the 500kV system at 370kV at 13:19 hrs. Characteristics of air conditioning loads were thought to be part of the problem [3].

The French system disturbances of January 12, 1987 resulted from loss of four generating units over a period of 50 minutes. After the generating units were lost, voltages decayed and nine other generating units were lost over the next nine minutes; eight due to field current limiting. The total power deficiency was about 9000MW. Voltages then stabilized at very low levels (0.5 – 0.8pu). After six minutes the 400/225 kV transformers were tripped to shed about 1500MW of load, and the voltages recovered thereafter [3].

As a result of these and other voltage stability problems, voltage instability and voltage collapse have become important to consider in system planning and operation.

Before proceeding to a discussion on the main objectives of this thesis, some definitions and classification of voltage instability in the context of the power system stability problem in general are presented. The general problem of power system stability is concerned with the ability of the power system to maintain a state of equilibrium during normal operation or regaining an acceptable equilibrium following a disturbance. The first power system stability problems encountered were those concerned with rotor angle stability: such problems are driven by generator dynamics and occur as either monotonic rotor accelerations or undamped electromechanical oscillations. The former phenomenon is due to a lack of synchronizing torque while the latter is as a result of a lack of sufficient damping torque [1,2].

Frequency problems, resulting mainly from imbalances in power transfer between generation and loads, also present further challenges to the stability of power systems. Frequency problems encountered after major disturbances have resulted in islanding [1].

Voltage stability problems on the other hand are driven by load dynamics. Following a disturbance or a change in the system operating conditions, the dynamics of certain load types are such that they generally attempt to restore power consumption to the pre-

disturbance values. As a result, demand for power, particularly reactive power, may increase beyond the capability of the generation and transmission system. The inability of the power system to meet demand for reactive power is the main factor that leads to voltage instability. Problems of reactive power transfer cause drops in the system voltages. Drops in system voltages may sometimes escalate into a progressive and uncontrollable decline in voltage affecting a significant portion of the system. This phenomenon is known as voltage collapse [2].

Many definitions for voltage stability have been put forward by various authors and IEEE and CIGRE working groups [1,3,5]. Reference [2] provides the following definition:

"Voltage stability is the ability of a power system to maintain acceptable voltages at all buses in the system under normal operating conditions and after being subjected to a disturbance."

Voltage stability problems can be classified into two subclasses depending on the disturbance leading to instability:

(1.) Large-disturbance voltage stability is initiated by large system disturbances such as system faults, loss of generation or transmission circuit contingencies. This problem is also known as transient voltage instability.

(2.) Small-disturbance voltage stability is the ability of the system to maintain a stable operating equilibrium close to its pre-disturbance equilibrium following small changes in the system's operating conditions such as small changes in load demand.

The criterion for large-disturbance voltage stability is that the voltages at all buses in the system reach acceptable steady-state values following a disturbance and after all system control actions have settled. The criterion for small-disturbance voltage stability on the other hand is that for a particular operating point, the voltage magnitude at every bus in the system increases as the reactive power injection at the same bus is increased [2]. Reference [1] makes another classification based on the time frame in which the incident occurs as follows: short-term voltage stability, which refers to voltage instability involving dynamic

loads that have a tendency to restore power consumption in the time frame of a second, including components such as induction motors and electronically controlled loads and HVDC interconnections; long-term voltage stability, which involves slower dynamic processes such as transformer tap changers and generator excitation limiters where relevant transients last typically for several minutes [1].

The analysis of voltage stability for a given system involves the examination of two aspects [5]:

(1.) The proximity to instability; which is a measure of the distance to instability of the system in terms of physical quantities such as load level (in relation to system loadability limits) active power flow through a critical interface, and reactive power reserves.

(2.) The mechanism of voltage instability; which concerns the events and interactions that lead to instability and the sequence in which they happen. Factors that contribute to instability in the system, as well as the actions of equipment and controllers that exacerbate instability are identified. The voltage-weak areas in the system are also important to consider.

When conducting such analyses, a range of different methods can be employed to gain insight into the key phenomena and reasons for instability. As with the classification of voltage stability phenomena, so too the methods used to analyse voltage stability can be categorised. For purposes of this discussion, two very broad categories of voltage stability analysis are described, static analysis and dynamic analysis. Static methods examine the viability of the equilibrium point of the power system represented by a specified operating condition of the system [6]. The general structure of the system model for voltage stability can be expressed as a set of first order-differential equations taking the form of equation (1.1), and algebraic equations (1.2) [2].

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{V}) \tag{1.1}$$

$$\mathbf{I}(\mathbf{x}, \mathbf{V}) = \mathbf{Y}\mathbf{V} \tag{1.2}$$

Where,

$\mathbf{x}$ is the state vector of the system

$\mathbf{V}$ is a vector of bus voltages

$\mathbf{I}$ is a current injection vector

$\mathbf{Y}$ is the network node admittance matrix

and initial conditions $(\mathbf{x}_0, \mathbf{V}_0)$ are known.

The static approach considers a particular steady state equilibrium point of the system and analyses the stability of the equilibrium point following small changes. Conditions at various time frames along the time-domain trajectory are considered. At each of these time frames, time derivatives of system state variables are assumed to be zero, reducing the overall system equations to purely algebraic form, equation (1.2). Examples of static methods are modal analysis of the system jacobian matrix, special optimal power flow and P-V and Q-V curves.

Time-domain simulations on the other hand, with appropriate modelling, capture the particular events and their chronology that lead to instability. Dynamic simulation is a useful method for analysis of specific voltage collapse situations, coordination of protection controls, and testing of countermeasures. Dynamic simulations also determine whether and how the steady-state equilibrium point will be reached. The main drawback of off-line computer simulation is that it is time consuming, particularly for large systems, and does not readily provide sensitivity information or a measure of the margin of stability [2]. Closed-loop testing of control equipment cannot be performed with traditional off-line computer simulations unless the control equipment itself is represented in detail as part of the simulation model. However, often such equipment is complex and the models used in simulation consequently lack full details. It is thus not possible to make a complete assessment of the effect of physical control devices using an off-line time domain simulation tool.

1.2 Thesis Background and Objectives

The power system transient simulation problem can be considered as one of solving a set of differential equations and algebraic equations given in equations (1.1) and (1.2) respectively. As pointed out in [7], the solution used in many power system transient

computer programs is based on the algorithm proposed by H.W Dommel. In this algorithm, the differential equations are discretized using trapezoidal rule and are combined with the algebraic equations to yield a matrix equation which is solved iteratively in each time step. Reference [8] describes the application of the Dommel algorithm to a fully digital real-time electromagnetic transient simulator. Real-time digital simulators are based on special purpose Digital Signal Processors (DSP) and parallel computing technology to achieve high enough speeds for real time solution of the mathematical models describing a power system [9]. Real-time simulation has a number of advantages over non real time simulation [10,11]: using a non real time tool, for any given event happening, a longer time duration is needed to calculate and return the results than the time taken for the actual event to happen, whereas with a real-time tool calculations are done and results returned in the same time that the event happens in the actual system. The capability for real-time solution of the power system model equations makes closed loop testing of physical power system protection and control devices possible with a real-time simulator. Furthermore, since a real-time simulator continues to return results as long as the simulation is left running, it is able to provide long term system dynamic and stability information that may not be obtained using non real-time simulation tools [11].

This thesis investigates the use of a Real-Time Digital Simulator (RTDS^{TM}) as a tool for power system voltage stability analysis. The two broad objectives of this thesis can be summarised as follows.

(1.) The thesis assesses the suitability of the RTDS as a tool for time domain voltage stability analysis. The investigations use both the generalized power system models provided in the RTDS as well as developing customized real-time models of particular power system controllers for real-time voltage stability analysis. In particular, power system controllers that have been developed are: a transformer on-load tap changer and voltage regulator; generator excitation control systems with field current limiters; reactive power compensating equipment; including a Static Var Compensator and a synchronous condenser. In addition, real-time simulator models have been developed of two benchmark study systems: an 11-bus benchmark system and a smaller benchmark system have been used to examine the suitability of the real-time simulator for time-domain voltage stability studies.

(2.) The thesis also considers the ability of the RTDS to perform full closed loop testing of actual power system control hardware for voltage stability studies using the 11-bus benchmark model. The real-time model of the transformer tap changer controller in the benchmark system model is replaced with an actual hardware controller connected in closed loop with the simulation on the real-time simulator.

1.3 Thesis Layout

This thesis consists of seven chapters and appendices. In order to present the analyses of the thesis, the development of various system models, the results and main findings of the thesis, the material has been arranged as follows.

Chapter one provides an introduction and general background to the voltage stability problem and states the main objectives of the thesis.

Chapter two presents a review of real-time power system simulation and the literature and theory of the voltage stability problem. The chapter then deals with the fundamental concepts of voltage stability phenomena and the modelling requirements for its analysis. The chapter also reviews methods of voltage stability analysis, modelling tools, important concepts and interventions against voltage instability.

Chapter three presents real-time models of particular components that are important for voltage stability studies. In particular, transmission line loading and the concept of surge impedance loading are reviewed as well as the voltage dependency of loads. The chapter then presents the development of an on-load transformer tap changer controller, two generator excitation control systems with overexcitation limiter functions and reactive power controllers for a synchronous condenser and a static var compensator.

Chapter four describes the development of real-time models of two benchmark study systems on the RTDS. Results from analysis of these benchmark systems using the RTDS are presented to establish their validity. The results show that these real-time models are in very close agreement with the documented studies in the literature. This establishes that RTDS analyses of voltage stability phenomena are accurate.

In chapter five three different countermeasures against voltage instability are investigated and compared using the real-time model of the 11-bus system, namely shunt compensation, synchronous condenser compensation and static var compensation. The effectiveness of these three countermeasures under three loading conditions is studied and the results are shown to agree with the known characteristics of each compensating device.

Chapter six presents the results of hardware-in-loop testing of actual power system controllers using the real-time simulation model of the 11-bus system. The software model of the on-load tap changer controller developed in chapter three is replaced with an actual hardware controller. Results of the simulation studies with actual hardware controllers are compared with those obtained using all-software representation of these controllers. The tests show a high level of agreement between the all-software simulation and the simulation interfaced with an actual hardware controller.

Finally chapter seven concludes the findings of the thesis and gives recommendations and suggestions for future work.

1.4 Main Findings and Achievements of the Thesis

This section lists the main findings and achievements of this thesis. The thesis has

(1.) developed custom real-time models of power system controllers that are necessary for the study of voltage instability mechanisms, and which are not provided as existing models in the RTDS environment;

(2.) developed and verified real-time models of two classical benchmark systems for voltage stability analysis, using both the existing component models provided by RTDS, as well as the custom models developed in (1.);

(3.) investigated the use of the RTDS for conducting detailed time-domain voltage stability studies over relatively long time frames;

(4.) investigated the use of the RTDS for assessing different methods of voltage stability enhancement.

(5.) demonstrated the capability of the RTDS to carry out full closed loop testing of actual power system controller hardware in voltage stability studies.

1.5 Research Publications

Some of the findings of this thesis have been presented at two national conferences and at one international conference [12,13,14].

CHAPTER TWO

REVIEW OF REAL-TIME SIMULATION AND THE VOLTAGE STABILITY PROBLEM

2.1 Introduction

The previous chapter presented a discussion of factors that have been responsible for problems of voltage stability and voltage collapse in many developed power systems around the world. The discussions of that chapter showed that problems of voltage stability have become a great source of concern both for power system planning and operation, and hence the need for developing analytical tools and techniques for counteracting voltage instability.

That chapter pointed out a number of methods of analysis and tools that have been used for voltage stability analysis. The main methods are steady state methods (powerflow: P-V and Q-V curves); dynamic analysis (time domain simulations); modal analysis of the jacobian; and optimization (special optimal powerflow). Appropriate and complementary use of these methods can provide detailed insight into a variety of aspects of voltage instability phenomena. In particular, time domain simulations can be used to understand the mechanism of instability as well as the events, and their chronology leading to instability [2]. However, long term system dynamic and stability information might not be obtained with a non real-time simulation tool as non-real time simulation tools usually do not have capability for continuous operation. A real-time simulator on the other hand can provide continuous results for as long as the simulation is left running [11]. Hence this chapter reviews the literature regarding the application of real-time simulation to power system analysis in general and further considers the advantages and disadvantages of the application of real-time simulation to voltage stability studies. The chapter then reviews the theory and basic concepts of voltage stability. Modelling requirements of key types of power system plant that are important for voltage stability are reviewed. The chapter also reviews system factors that influence voltage stability and those characteristics of power

system equipment that must be modelled in order to correctly predict what happens under voltage stressed conditions.

Finally, this chapter considers techniques that are used for alleviating the problem of voltage stability, and discusses the merits and demerits of some methods of voltage control.

2.2 Real-Time Simulation

The electromagnetic transients program (EMTP) began to replace, in the mid 1970s, the very expensive and bulky analogue simulators for most power system transient simulations. This followed the development of the Dommel algorithm by H. W. Dommel for digital computer power system transient simulations [8]. Today most electromagnetic transient programs for digital computer solution of power system transients are based on the Dommel Algorithm [10]. Power systems generally comprise a number of complex individual elements whose solutions need to be determined in order to find the solution of the overall network. In a digital computer simulation for power system transient solution, the state of the power system is computed and results returned at discrete instants in time. The time period between two consecutive instants is called the simulation time-step. Typical electromagnetic transient studies require simulation time-steps in the range of 50 - 100 microseconds [10]. The number of equations that need to be solved and the amount of computations involved in one time step are thus considerable. In traditional off line simulation tools, the time it takes to complete computations and return results for any given event is longer in the simulation than the event takes to happen in the actual power system. The operation of normal transient simulations is thus non real-time. In order to operate in real-time, computation of events within one time-step needs to be completed and results returned in less than the chosen time-step [15].

The non real-time nature of traditional transient simulations precluded their use for testing of actual power system devices. Hence testing of physical devices was done either using analogue simulators, which operate in real-time, or using special devices that could play back, in real-time, the stored results of an off-line digital computer simulation. The main drawbacks of the analogue network simulators are high capital and operating costs and they are generally bulky [10]. In addition, simulations of power systems using an analogue

simulator may take a long time to prepare for studies involving complex networks [8]. Apart from these considerations, digital computers are capable of simulating very sophisticated and accurate power system models. A fully digital computer capable of real-time operation, therefore, has advantages in that it incorporates the best features of the computer based digital simulation tools and the analogue simulators [8].

Reference [8] describes development of a fully digital real-time simulator. The impetus for development of the Real-Time Digital Simulator was the need to test sensitive power system equipment that would not be easy to model under the same conditions the equipment would encounter in the power system. Reference [8] also describes application of the real-time digital simulator to testing of a joint var controller (JVC): a controller that ensures that reactive power output of synchronous machines of different ratings is shared equally among the different machines. The purpose of the JVC in this particular case was to regulate steady state voltages in the system. A real-time simulation model of the power system in which the JVC was to be used was developed and the JVC hardware tested in closed loop with the simulated power system. Input quantities produced by the simulator where fed to the JVC that monitored these quantities and in turn provided set points used by exciter models in the simulation. Reference [16] gives a description of the method and performance of a real-time simulator for relay testing. This paper provides details of how physical devices (power system controllers and protective devices) can be interfaced with a real-time simulation; appropriate signals from the simulation are provided as input to the physical device, and outputs from the physical device are fed back to the simulation. Real-time digital simulator modelling and testing of HVDC systems and their controls are also described in reference [15].

From the point of view of voltage stability analysis, a real-time simulator has a number of benefits. The capability to simulate very detailed models of power system components, coupled with the ability to test actual physical control and protective devices with a real-time simulator is a great attraction for voltage stability analysis and testing of control strategies. The capability for real-time simulation also makes it possible to carry out multiple contingency studies of complex systems in relatively short time frames [11].

This thesis focuses on assessing the suitability of a particular digital computer based real-time simulator as a tool for voltage stability analysis. The simulator is known as the Real-

Time Digital Simulator (RTDS^{TM}) from RTDS Technologies. The RTDS was initially designed for simulating electromagnetic transients in real-time [8]. Power system models can be represented on the RTDS in great mathematical detail and simulations are carried out in real-time. Multiple processors that operate in parallel solve the system state at fast enough speed for real-time simulation [8]. The hardware and software of the RTDS are custom built with the multiple processor cards housed on specially designed frames known as racks. Simulations are carried out on the processor cards in the racks, while the pre-simulation work required to build the mathematical model of the system, compile the model and carry out load flow studies is done on a host personal computer (PC) connected to the simulator through Ethernet cables. Racks also provide specialized analogue and digital input and output cards for interfacing power system hardware equipment to the real-time simulation in closed loop. RTDS racks are designed in a modular manner so that several racks and host PCs can be present in one RTDS system [17]. Fig. 2.1 shows a schematic diagram of a single-rack RTDS system interfaced with a power system controller through its digital input and output ports and a specialized analogue output card.

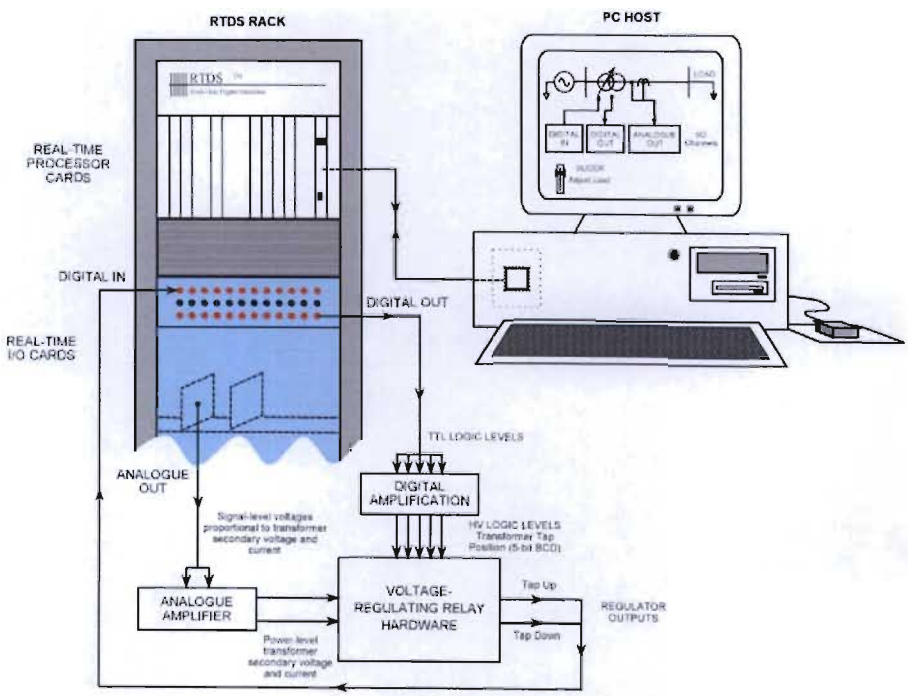

Fig. 2.1 Schematic diagram showing the Real-Time Digital Simulator and hardware-in-loop testing of a voltage regulating relay [18].

Different types of power system control hardware can be interfaced with simulations on the RTDS. Examples of these controllers include excitation controls and excitation

limiters; transformer tap changer voltage controllers; and actively controlled var compensator controllers (SVCs, STATCOMS etc). The advantages of using the real-time simulator for voltage stability analysis are that detailed models of power system components that play a key role in voltage instability mechanisms can be modelled using the RTDS software suite while certain other control equipment that cannot be modelled easily can be interfaced with the software simulation. Simulations are done in a relatively short period of time which allows testing of multiple contingencies. Detailed time-domain simulations can thus be performed on the simulator. The ability to test actual power system control hardware is also very useful for testing the physical control hardware during voltage stressed conditions. Disadvantages of using the real time simulator for voltage stability analysis are that the simulator does not calculate eigenvalues and P-V and Q-V curves cannot be readily obtained using the simulator. Thus the simulator does not readily lend itself to steady state methods of voltage stability analysis such as P-V and Q-V curves or modal analysis.

2.3 Fundamental Concepts Related To Voltage Stability

Problems of voltage stability and voltage collapse typically occur in power systems which are heavily loaded, faulted and/or have reactive power shortage [19]. Voltage collapse is a system-wide instability that involves many power system components and their variables for any one given incident. Voltage collapse may be initiated by a variety of causes but the underlying problem is an inherent weakness in the power system. Reference [5] lists the main findings of the causes of voltage collapse for a number of incidents around the world. The initial cause may be due to small gradual changes in the system such as natural increases in load or large sudden disturbances such as loss of a generating unit or a heavily loaded line. The strength of the transmission network, generator reactive power or voltage control limits, load characteristics, characteristics of reactive power compensating devices, and the action of voltage control devices such as transformer on-load tap changers are principal factors that contribute to voltage collapse.

2.3.1 Time scales

Voltage collapse takes place on time scales ranging from seconds to several minutes depending on the devices involved. The time scales are as follows [1]:

(1.) The time frame of electromechanical transients typically lasting a few seconds is referred to as transient or short term scale; this includes electromechanical transients, automatic voltage regulators, excitation systems and turbine and governor regulators that act in this time frame.

(2.) Long term scale involves longer term dynamics and the action of devices that take up to several minutes to respond to changes. These devices include discrete switching devices such as transformer tap changers, and excitation limiters acting at intervals of tens of seconds.

Voltage collapses can be classified as short term or long term according to the time frames in which they occur [1]. Sometimes a single voltage collapse incident may include the dynamics of devices acting in the long term and short term time frames. Reference [1] describes such voltage collapse incidents.

2.3.2 Transmission system characteristics

The characteristics of the transmission system that are important for voltage stability can be explained by using a simple radial network consisting of a large system supplying a load through a transmission system reactance shown in Fig. 2.2.

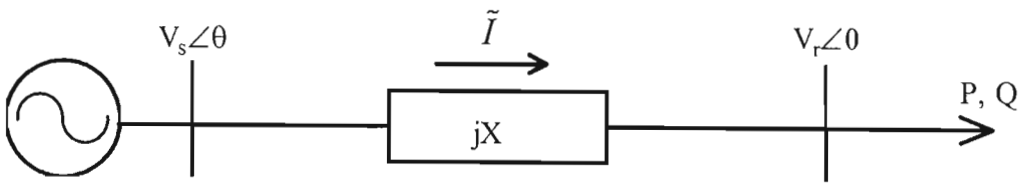

Fig. 2.2 Transmission system characteristics affecting voltage stability [3].

The real power P, and the reactive power Q, transferred to the load through the transmission system can be expressed in terms of the sending end voltage $V_s\angle\theta$, receiving end voltage $V_r\angle 0$ and transmission line reactance X as follows [1,2]:

$$P = \frac{V_s V_r}{X}\sin\theta \qquad (2.1)$$

And

$$Q = \frac{V_s V_r \cos\theta - V_r^2}{X} \tag{2.2}$$

Where, θ is the angle between the sending end and receiving end voltage phasors.

Equations (2.1) and (2.2) show that the steady state power transfer by the ac network is influenced by the magnitudes of the sending end and receiving end voltages, the transmission line reactance and the angle between the sending end and receiving end voltage phasors. Real power transfer depends more on the angle between the sending end voltage and the receiving end voltage while reactive power transfer is more dependent on the difference between the magnitudes of the sending end and receiving end voltages. Relationships between power and voltage are obtained if equations (2.1) and (2.2) are solved with respect to V and θ. If the system of Fig. 2.2 is subjected to various real power loadings at a given power factor, a family of curves of load voltage as a function of active power at the receiving end can be obtained, with one curve per load power factor. These curves are called P-V curves or nose curves. A P-V curve for the system of Fig. 2.2 at a load power factor of 0.95 for normalised real power and load voltage is shown in Fig. 2.3 [1,2].

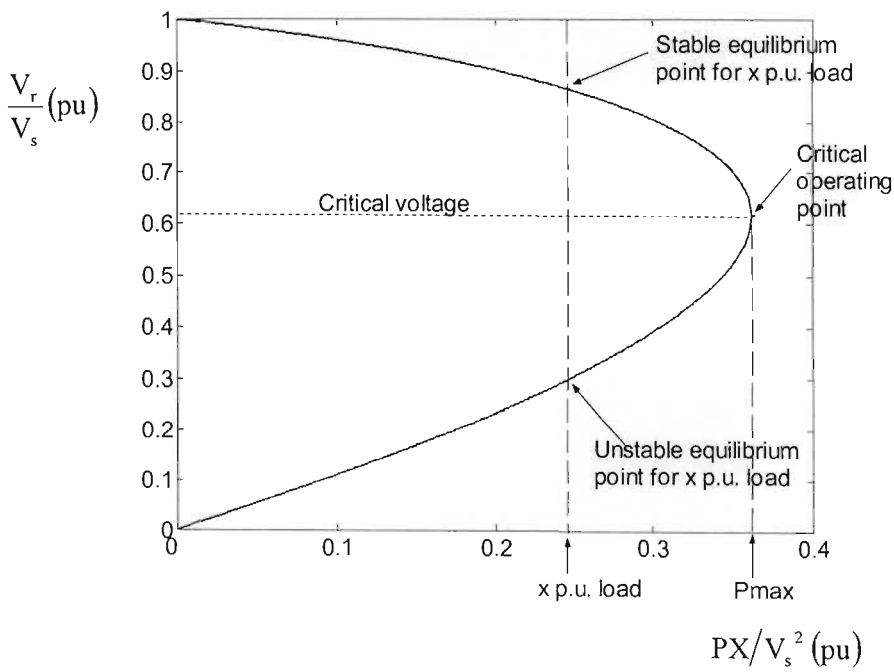

Fig. 2.3 Real power versus voltage characteristics of the system of Fig. 2.2 at a load power factor of 0.95 [2].

Fig 2.3 shows that there is a maximum value of real power that can be transferred to the load at given power factor. This maximum transferable power is shown as Pmax in the diagram. The critical operating point represents the limit of satisfactory operation.

For any given load power demand below the maximum transferable power such as x p.u. shown in the diagram, there are two possible equilibrium operating points: one at a higher voltage corresponding to the upper region of the curve and the second point with low voltage corresponding to the lower part of the curve. The higher voltage point is a stable equilibrium point. In this region of the curve increasing real power results in a reduction in voltage and increase in current. The lower portion of the curve is an unstable operating region where reduction in load voltage results in reduced real power transfer.

For load demand higher than the maximum transferable power, there is no equilibrium operating point. If load demand exceeds the maximum transferable power Pmax, or a change in the system configuration results in a particular load demand being higher than the maximum transferable power, the system becomes unstable through loss of a stable equilibrium point [1].

The power versus voltage characteristics of the system are greatly influenced by the load-power factor. A more compensated system has a higher maximum transferable power Pmax. This is because reactive power compensation reduces both reactive and active power losses in the transmission system with the result that voltage drops are lower in a compensated system. The maximum power that can be transferred is therefore higher as this is a function of the voltage magnitudes at the sending end and receiving end of the transmission system [equation (2.1)].

The reactive power Q at the receiving end, in terms of real power and power factor angle ϕ is given by $Q = P\tan\phi$. Plots of reactive power at the receiving end as a function of receiving end voltage referred to as V-Q curves can thus also be produced following a similar procedure to that used for P-V curves. Fig. 2.4 shows the corresponding V-Q curve of the system shown in Fig. 2.2 at a load-power factor 0.95 [1,2].

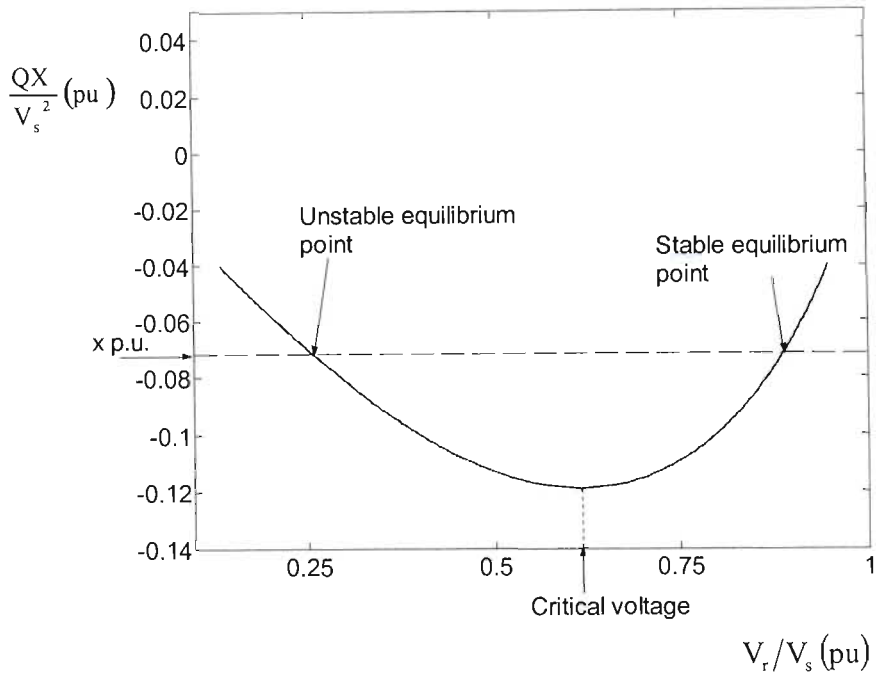

Fig. 2.4 Voltage versus reactive power characteristics of the system of Fig. 2.2 at a load power factor of 0.95 [2].

Fig. 2.4 shows that for a given reactive power at the receiving end Q, there are two possible operating equilibrium points. A stable equilibrium and an unstable equilibrium point as shown in the figure. The point on the right side is a stable equilibrium point: at points along the curve on the right hand side of the critical voltage, indicated on the graph, the slope of the V-Q curve is positive, indicating that increase in reactive power transfer results in increase of the voltage at the receiving end. The equilibrium point on the left hand side of the critical voltage on the other hand is an unstable equilibrium point: at all points on the curve to the left of the critical voltage the slope of the V-Q curve is negative.

2.3.3 Load characteristics

Loads whose characteristics vary with voltage interact with the transmission system characteristics and hence change the power flow through the system. This causes the system voltage to settle at an operating point determined by composite characteristics of the transmission system and load [3]. The load voltage characteristics are expressions of the active or reactive power consumed by the load as a function of voltage. There are two load models widely used to represent the voltage dependency of loads:

(1.) The exponential load model has the general form [1]:

$$P = P_0\left(\frac{V}{V_0}\right)^{K_{pv}} \tag{2.5}$$

$$Q = Q_0\left(\frac{V}{V_0}\right)^{K_{qv}} \tag{2.6}$$

where V_0 is the nominal voltage, and P_0 and Q_0 are the active and reactive powers consumed at nominal voltage, and the exponents K_{pv} and K_{qv} depend on the types of load. If the load is a purely constant impedance load then $K_{pv}= K_{qv}= 2$. For a constant current load $K_{pv} = K_{qv} = 1$, while both K_{pv} and K_{qv} are equal to 0 when the load is constant power. Fractional values of K_{pv} and K_{qv} represent loads that have components of the three load types depending on the amount of the load that is of each specific type [2,3].

(2.) The second model used to represent load voltage characteristics is called the polynomial load model. This model sums up the load components which are constant impedance, constant current and constant power. It is referred to as the ZIP load model for the three components of the load: constant impedance (Z) constant current (I) and constant power (P). The real and reactive characteristics of this model are given by the following quadratic expressions [2,3]:

$$P = P_0\left[ZP\left(\frac{V}{V_0}\right)^2 + IP\frac{V}{V_0} + PP\right] \tag{2.7}$$

$$Q = Q_0\left[ZQ\left(\frac{V}{V_0}\right)^2 + IQ\frac{V}{V_0} + PQ\right] \tag{2.8}$$

where ZP (ZQ), IP (IQ) and PP (PQ) are those fractions of the total real (reactive) power of the load, that are constant impedance, constant current and constant power in nature respectively.

Fig. 2.5 shows the active and reactive load characteristics for a ZIP load model with voltage varying from 0.4pu to 1.1pu. For the load characteristics shown, the active power component of the load comprises 50% constant power, 30% constant impedance and 20% constant current, while the reactive power component consists of 20% constant power, 60% constant impedance and 20% constant current. The initial load is 120MW at 0.8 p.f. lagging and 1 p.u bus voltage. The base MVA used is 100MVA.

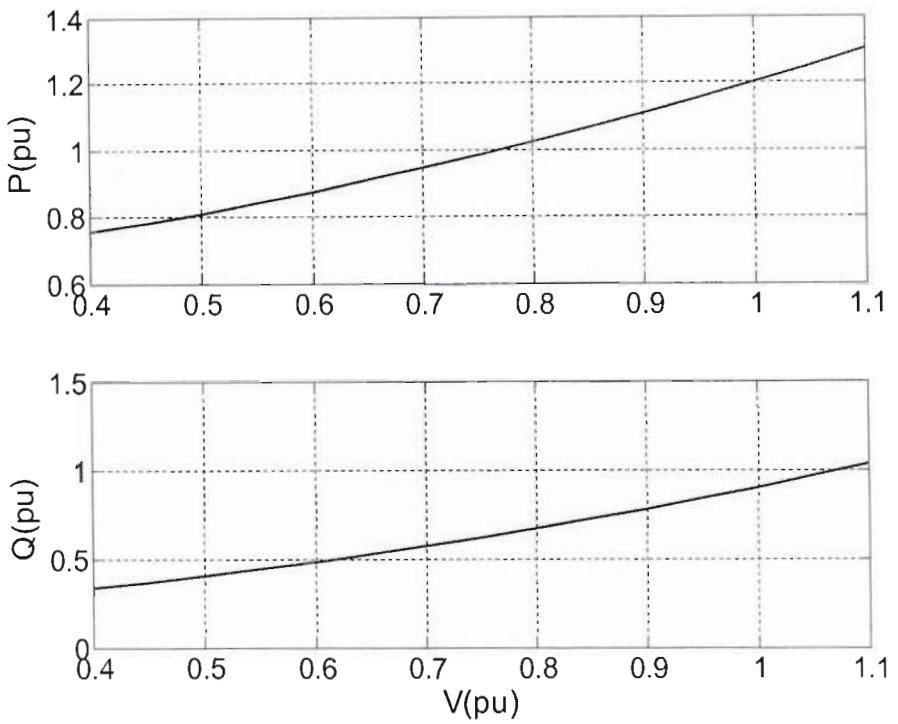

Fig. 2.5 P-V and Q-V characteristics of a ZIP load.

Voltage instability mechanisms depend on the system P-V and V-Q characteristics, Fig. 2.3 and Fig. 2.4 respectively, and load characteristics, Fig. 2.5. The intersection between the system characteristics and the load characteristics determine the operating point. In a voltage instability event, the equilibrium can change from stable equilibrium to an unstable equilibrium through various mechanisms such as gradual increase in load demand, or change in system characteristics due to a large disturbance such as the loss of a transmission line.

2.3.4 Effect of transformer on-load tap changers

The purpose of a transformer on-load tap changer (OLTC) is to regulate secondary voltage by adjusting the turns ratio of the transformer. In most cases, the variable tap is on the high voltage (HV) side of the transformer because current is lower on the HV side (thus commutation is easier) and, because the HV side has more turns, it allows for more precise regulation of voltage. OLTCs are slow acting, discrete devices changing the tap setting by one position at a time, with a time delay between tap changes, until the voltage is brought within an error band or until the tap limits are reached. Two modes of OLTC operation are distinguished [1]: sequential mode of operation and non-sequential mode. In the sequential mode the initial time delay is longer than subsequent delays and can be either inversely proportional to the magnitude of the voltage error or constant, while all subsequent tap movements have constant time intervals. The non-sequential mode, on the other hand, makes no distinction between the first tap movement and subsequent movements. Each tap up action of the OLTC results in an increase in transmission line voltage drop due to increased line current on the primary side of the transformer. Tap changing transformers maintain the voltage at the secondary side of the transformer independent of primary side voltage within a deadband of the voltage setpoint provided the tap limit has not been reached. Loads connected at this bus are thus supplied at constant voltage within the regulative range of the on-load tap changing transformer; the effect of this is to cause voltage dependent loads to maintain their power consumption even when system voltages in the transmission system are low.

2.3.5 Reactive power transfer

Problems of voltage stability typically occur in heavily loaded systems where reactive power demand cannot be met by the system. Reactive power transfer in the electrical network is closely coupled with voltage gradient. This can be seen by considering equation 2.2: for small values of load angle θ, $\cos\theta \approx 1$, such that equation 2.2 reduces to

$$Q \approx \frac{V_r(V_s - V_r)}{X} \tag{2.9}$$

Thus reactive power transfer depends mainly on the difference between sending end voltage and receiving end voltage. However, reactive power cannot be easily transmitted

over long transmission lines due to high reactive losses along the transmission line. This is attributed to the predominantly inductive nature of transmission lines. Real power transfer on the other hand depends more on the phasor angle difference between the sending end voltage and the receiving end voltage phasors, as is shown in equation 2.1.

2.3.6 Reactive power compensation

The purpose of reactive power compensation is to improve power system performance by, specifically, keeping voltages close to nominal values, reducing line currents and hence network losses, and to contribute to stability enhancement [1]. Most often compensation is provided by capacitors which counteract the predominantly inductive nature of power system networks. It may also consist of inductors where reactive power absorption is required.

Series capacitor compensation

Series compensation reduces the net transmission line inductive reactance by inserting a capacitor in series with the transmission line. It is primarily used for improving stability in long transmission lines. The reactive generation of a series capacitor increases with the square of line current, thus under heavy loads when voltage stability is of concern, its reactive generation is higher. Series capacitor compensation improves the maximum power transfer of a transmission system by reducing the net line reactance. With series capacitor compensation, the net line reactance is given by:

$$X_{net} = X - X_c \tag{2.10}$$

Substituting X with X_{net} in equations 2.1 and 2.2 gives:

$$P = \frac{V_s V_r}{X - X_c} \sin\theta \tag{2.11}$$

and,

$$Q = \frac{V_s V_r \cos\theta - V_r^2}{X - X_c} \tag{2.12}$$

Equations 2.12 and 2.13 show that the power transfer is increased for the same receiving end voltage and load angle.

Shunt capacitor compensation

Shunt capacitors are used to supply reactive power and boost voltages within load areas. In addition to voltage control, shunt capacitors contribute to load stabilization. The main advantages of shunt capacitors is that they have a relatively low cost compared with other methods of reactive power compensation, and are relatively easy to install and operate [2]. The reactive power supplied by a shunt capacitor is given by:

$$Q_C = \frac{V^2}{X_C} \tag{2.13}$$

Where,

X_C is the shunt capacitor reactance and

V is the bus voltage.

Equation (2.14) shows that the reactive power output of the capacitor varies as the square of the voltage. During low system voltages, therefore, the reactive power output of a shunt capacitor is greatly reduced. This reduction in reactive power further compounds the problem of voltage stability.

Static var compensators

A static var compensator (SVC) is a voltage controlled shunt compensation device. It provides fast and precise voltage control by providing continuously variable susceptance. Variable susceptance is obtained either by thyristor switched capacitors (TSC) or thyristor controlled reactors (TCR). An SVC may consist of a TSC in parallel with a TCR, or a TCR with a fixed capacitor. In addition harmonic filters that are capacitive at the fundamental frequency are included. Under steady state conditions the SVC controls voltage with a droop characteristic within its control range. When the SVC reaches its capacitive limit, its characteristics become the same as that of a simple capacitor [2,3].

2.3.7 Generator characteristics

Synchronous generators are the primary source of reactive power and provide the most important means of control of the voltage profile of the system. During normal operating conditions, the terminal voltage of generators is kept constant by their automatic voltage regulators (AVRs) [2]. Under stressed conditions, demand for reactive power increases. Generators increase the output of reactive power by increasing their internal generated voltages. This is achieved by increasing the field voltage and hence field current. When the field current reaches its maximum limit, voltage control at generator terminals is lost. The point of constant voltage is now behind the synchronous reactance of the generator. The effect of this is equivalent to increasing the transmission system reactance [2]. From the discussion of section 2.3.2 the system characteristics are then significantly altered and the transferable power is reduced. The reactive power capability of synchronous generators is limited by either field winding heating or armature winding heating. These limits can be represented by two curves on the real power/ reactive power characteristic of the generator known as generator capability curves. Fig 2.6 shows the generator capability curves of a synchronous machine [2]. The intersection point of the two curves represents the rated operating point of the machine.

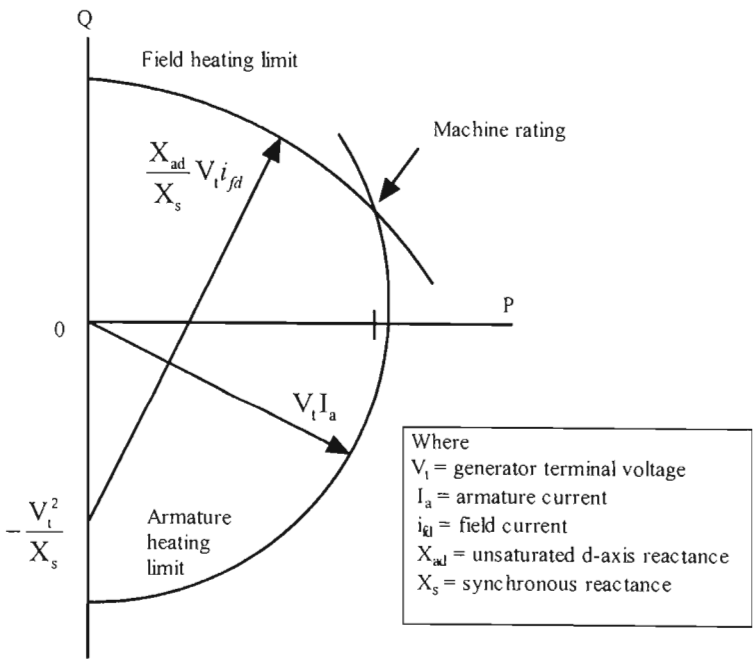

Fig. 2.6 Capability curve for a synchronous generator [3].

2.4 A Review Of Methods Of Voltage Stability Analysis

Methods of voltage stability analysis can be classified into two main approaches: static analysis methods and time domain methods. The former methods assume that the problem of voltage stability can be treated as a static phenomenon; such methods have been used in identifying voltage-weak areas and to measure proximity to instability [2,6]. On the other hand, time domain simulations, in which appropriate modelling is included, capture the actual events and their chronology that lead to instability. Reference [4] reviews the main methods that are used for voltage stability analysis. The paper also describes the use of PV and QV curves plotted from load flows by varying a parameter for demand and solving the load flow equations for values of P, Q and V. Such P-V and Q-V curves can provide insight into the distance from the stability limit for a given operating point. Some drawbacks of using P-V and Q-V curves for voltage stability analysis are that the method generally requires executing a large number of load flows, which is thus time consuming, and P-V and Q-V curves do not readily provide information useful in gaining insight into causes of stability problems. In addition, the procedure focuses on stressing individual buses independently, which may result in unrealistically distorting the stability information of the system.

Reference [6] discusses voltage stability analysis of power systems using static and dynamic methods, and points out the benefits and limitations of time domain simulations for voltage stability analysis. Time consumption, computational and engineering requirements and unavailability of sensitivity information are seen as some of the main limitations of using time domain simulations. This thesis considers use of a real-time simulator for time-domain voltage stability analysis. Real-time simulation provides the advantages of simulating in relatively short time frames and the ability to interface actual controller hardware under investigation with the simulation, both of which go some way to counteracting some of the disadvantages cited in [6]. Reference [20] uses time-domain simulation (with the PSS/E package) to determine the optimum location for a voltage instability correction device, known as a powerformer, that incorporates a generator and transformer in one device. The reference illustrates successful use of time domain simulation to determine the best location for a compensating device. Reference [21] also presents time domain simulations using the PSS/E to illustrate voltage stability analysis of a large scale power system. This thesis similarly uses real-time simulation to investigate

the effect of placing power system voltage control devices at different locations in a simple power system, and thereby aims to assess the use of real-time simulation for optimum placement of voltage control equipment.

2.5 Countermeasures Against Voltage Instability

Reference [19] illustrates voltage stability analysis of a simple two-node system using P-V curves and time domain simulations. The reference analyses the system by application of a fault for different time durations first without shunt compensation and then with compensation: the system is shown to recover if the fault is removed before a certain critical time. With shunt compensation, the critical time before instability is increased, showing that shunt compensation has a positive effect on system voltage stability. However the problem is to determine how much shunt compensation is needed and how fast should compensation be switched in. Although this thesis does not consider the effect of switching *time* of shunt compensating devices on system stability, it does however, consider the use of switched shunt capacitor compensation to control voltage stability and compares its effectiveness with other methods of control, namely using a synchronous condenser and using an SVC. To form a baseline for comparison, in the case of each method of voltage control studied in the thesis the same benchmark power system is used, namely the 11-bus benchmark system described in references [2,3,6]. The real-time model of this 11-bus benchmark system is presented and verified in chapter four.

Synchronous condensers are used in power systems for providing reactive power and maintaining system voltages. During low system voltages synchronous condensers increase their reactive power output almost instantaneously to support the system voltages. The overload capability of synchronous condensers also enables them to provide higher than normal amounts of reactive power for short periods which can be critical in maintaining system stability. In this thesis, modelling of a synchronous condenser-based reactive power output controller has been implemented on the RTDS. Simulations have shown that the reactive power output of the synchronous condenser can be controlled independent of the system bus voltage at which the synchronous condenser is connected. The effectiveness of the synchronous condenser to control voltages at three different locations in the 11-bus benchmark system is investigated.

The use of a static var compensator (SVC) to improve voltage stability in the 11-bus benchmark system has also been investigated. The SVC is used for regulating bus voltage within certain limitations [22]. In this thesis reactive power control of the SVC has been implemented on the RTDS to provide a means of comparing the effectiveness of the SVC for controlling voltage stability with other control techniques.

2.6 Conclusion

This chapter has presented a review of real-time simulation as tool for power system transient simulations. Advantages of real-time simulators for simulating power systems in general have been discussed and the application of real-time simulation to voltage stability analysis has also been discussed.

The chapter has also presented a literature review covering the fundamental concepts related to voltage stability. The chapter has discussed characteristics of the system that play an important role in voltage stability incidents. The important characteristics of the transmission system, loads, reactive power compensating devices and generators have all been discussed.

The chapter has also discussed different methods used for voltage stability analysis. The methods are broadly classified into two main approaches as static analysis methods and time domain methods.

Countermeasures against instability have also been discussed. The chapter has described the different types of equipment and techniques that are used to alleviate the problem of voltage stability.

The next chapter presents real-time model development of particular power system plant components that are important for voltage stability analysis. These models are used later in the thesis in developing real-time simulator models of two benchmark study systems.

CHAPTER THREE

REAL-TIME MODELING FOR VOLTAGE STABILITY ANALYSIS

3.1 Introduction

Chapter two presented a literature review regarding real-time simulation and issues related to power system voltage stability analysis. That chapter discussed the application of real-time simulation to power system analysis in general and further considered the advantages and disadvantages of the application of real-time simulation to voltage stability studies. That chapter also provided a review of basic concepts related to voltage stability analysis. Factors influencing voltage stability and characteristics of power system equipment that need to be modelled in order to correctly predict what happens under voltage stressed conditions were discussed. The chapter also presented a discussion of some methods that can be used for voltage stability control.

This chapter considers in detail, power system component modelling for voltage stability studies on the Real-Time Digital Simulator. In particular, real-time models of some power system controllers have been developed for use on the RTDS as part of the work of this thesis. These controllers include: transformer on-load tap changer; generator excitation control system with field current limiter; synchronous condenser reactive power control; and static var compensator reactive power control.

3.2 Transmission Line Model

The electrical parameters of transmission lines that are important for power system analysis are: line series resistance (R); line series inductance (L); shunt capacitance (C) and shunt conductance (G). When these parameters are expressed in terms of their respective units per unit length of the transmission line, they are referred to as distributed parameters. Assuming the line is transposed the analysis of the line can be done on a per phase basis. The series impedance and the shunt admittance of the transmission line per unit length per phase are expressed as $z = R + j\omega L$ and $y = G + j\omega C$ respectively. The relationship

between voltage and current at a distance x form the receiving end of the transmission line in terms of the distributed parameters of the transmission line can be expressed as [2]:

$$\bar{V} = \frac{\bar{V}_R + Z_C \bar{I}_R}{2} e^{\gamma x} + \frac{\bar{V}_R - Z_C \bar{I}_R}{2} e^{-\gamma x} \tag{3.1}$$

$$\bar{I} = \frac{\bar{V}_R / Z_C + \bar{I}_R}{2} e^{\gamma x} + \frac{\bar{V}_R / Z_C - \bar{I}_R}{2} e^{-\gamma x} \tag{3.2}$$

where,

$Z_C = \sqrt{z/y}$ is the characteristic impedance

$\gamma = \sqrt{yz} = \alpha + j\beta$ is the propagation constant; with α the attenuation constant and β the phase constant

x is the distance from the receiving end of the transmission line

$\bar{V}_R$ is the voltage at the receiving end of the transmission line and

$\bar{I}_R$ is the current at the receiving end of the transmission line.

If line losses are neglected, the characteristic impedance of the transmission line Z_C is a pure resistance equal to $\sqrt{L/C}$ and is called the *surge impedance*. The power delivered by the transmission line if it is terminated in an impedance equal to its surge impedance is known as the *surge impedance loading* (SIL), where

$$SIL = \frac{V_0^2}{Z_C} \tag{3.3}$$

and V_0 is the nominal line-line voltage

and Z_C is the characteristic impedance per phase given in equations (3.1) and (3.2).

In the travelling wave transmission line equations (3.1) and (3.2) the first term increases in magnitude and advances in phase with increasing distance from the receiving end x and is called the incident wave. The second term decreases in magnitude and phase. This term is referred to as the reflected wave. Reference [23] provides a detailed derivation of the travelling wave transmission line model equations in the time domain used in the RTDS. A special case of this line model known as the Bergeron transmission line model can be used with or without frequency dependence of the characteristic impedance and is given by the equations

$$I_S(t) = \frac{1}{Z} V_S(t) - \frac{1}{Z} V_R(t-\tau) - I_R(t-\tau) \tag{3.4}$$

$$I_R(t) = \frac{1}{Z} V_R(t) - \frac{1}{Z} V_S(t-\tau) - I_S(t-\tau) \tag{3.5}$$

where,

τ is the delay of travel time

I_S is the sending end current

I_R is the receiving end current

V_S is the sending end voltage

Z is an equivalent impedance whose frequency response is the same as that of the characteristic impedance Z_C of the transmission line.

The Bergeron transmission line model of the RTDS was used to study the characteristics of a 400kV, 361 km transmission line. Figs. 3.1 to 3.3 show the voltage and current characteristics of this transmission line for three loading conditions: line loaded at surge impedance load; line loaded above surge impedance load; and line with receiving end open.

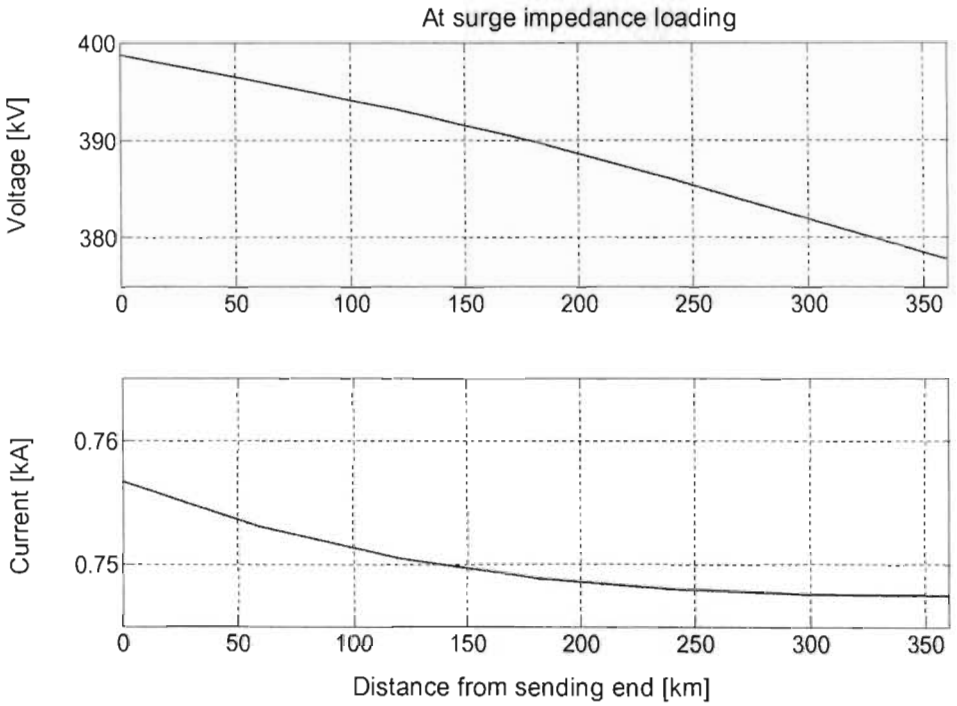

Fig. 3.1 Voltage and Current profiles along a 400kV transmission line at Surge Impedance Loading.

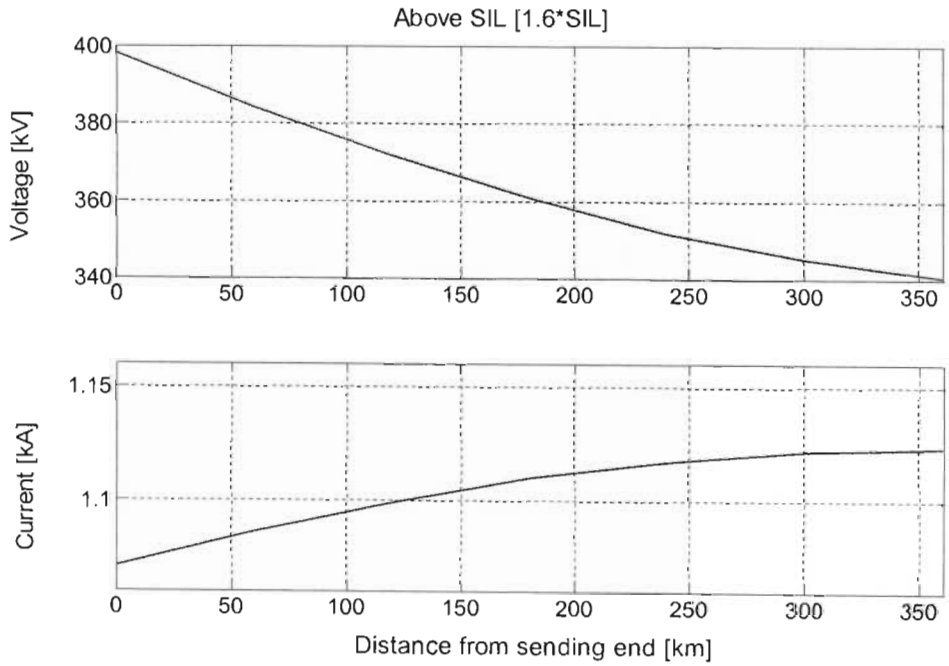

Fig. 3.2 Voltage and Current profiles along a 400kV transmission line at loading higher than Surge Impedance Loading.

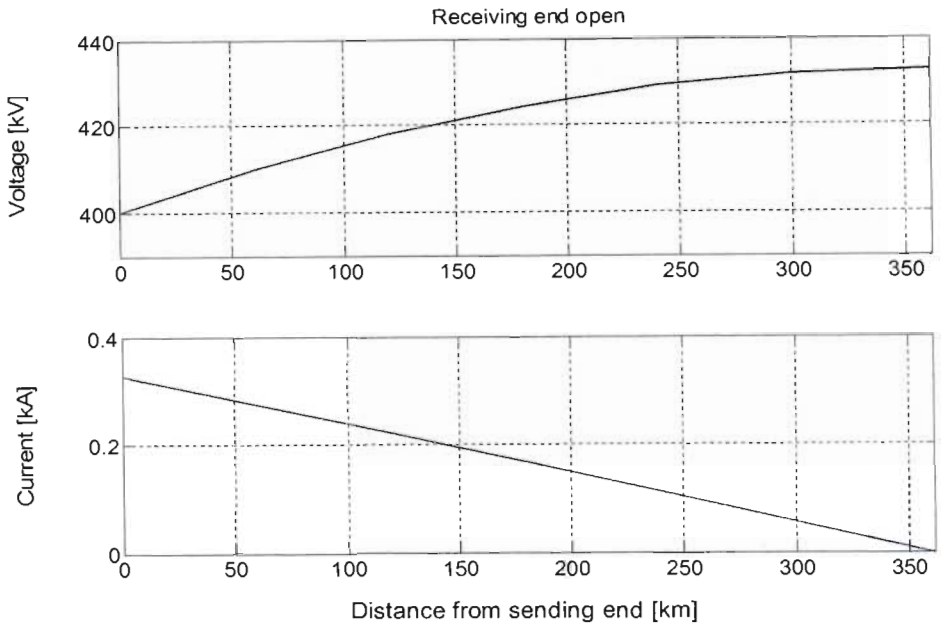

Fig. 3.3 Voltage and Current profiles along a 400kV transmission line with receiving end open.

Fig. 3.1 shows that when the transmission line is loaded at surge impedance loading the voltage has a fairly flat profile along the line (4.6% difference in voltage between sending and receiving ends). If line losses are neglected the transmission line characteristics show a flat voltage profile. The flat voltage profile is explained from the fact that at *SIL* the capacitive generation of the transmission line is equal to the reactive consumption due to the line inductive reactance. At above *surge impedance loading,* say 1.6**SIL* as shown in Fig. 3.2, there is a large voltage drop along the transmission line (15.0% difference in voltage between sending and receiving ends). This is due to the transmission line reactive consumption being higher than the transmission line reactive generation. With the receiving end open, as shown in Fig. 3.3, the shunt capacitance of the transmission line causes voltage rise along the transmission line, the voltage at the receiving end is 8.7% higher than that at the sending end. The rise in voltage is due to capacitive line charging current flowing through inductive reactance. This voltage rise is also associated with lightly loaded transmission lines and is known as the *Ferranti* effect [2].

3.3 Load Models

The RTDS provides pre-defined models of PQ loads whose active (P) and reactive (Q) set points can be controlled manually, or via other controlled blocks to implement voltage dependent load models. A phase locked loop is used to determine the instantaneous phase of the bus voltage. The phase angle of the bus voltage is used together with real and reactive power magnitude control signals to generate 3 phase sine wave currents. These 3 phase generated currents are the currents drawn by the load in each phase; they consist of a component in phase with the bus voltage and a component 90 degrees out of phase with the bus voltage. The magnitude of each current component is determined by the real and reactive power regulators respectively. A power measurement block uses the bus voltage magnitude and the current drawn by the load to compute the power flow from the bus. A P-I regulator uses this measured power of the load and the active and reactive power set points to determine the magnitudes of the real and reactive components of the current in order to regulate the active and reactive power of the load.

3.3.1 Polynomial load model

A voltage dependent PQ load is implemented on the RTDS by using a ZIP (polynomial) load control component to calculate the P and Q set point values to a PQ load component. RTDS's polynomial load model is implemented using the control circuit diagram shown in Fig. 3.4. In the RTDS algorithm of Fig. 3.4, the fractions of the active power component of the load that are constant power, constant impendence, and constant current are represented by the constants PP, ZP and IP respectively. These constants are entered by the user as required according to the type of load to be modelled. A three phase rms meter (block 1) measures the voltage (in per-unit) at the point where the load model is attached. The measured voltage is filtered using a first order lag filter (block 2) with a gain of 1.0 and time constant 0.01s. The output voltage of the filter V_0 pu is squared to obtain V_{02}. The desired real power at nominal voltage (Pord) is entered by setting the value on a slider (block 3). The part of the real power component of the load that is constant power (PCMVA) is obtained by multiplying this set point Pord by the fraction of the load that is constant power PP. The part of the real power component that is constant impedance (PCZ) is obtained by multiplying Pord by the fraction of the load that is constant impedance PZ and the value of the voltage squared V_{02}.

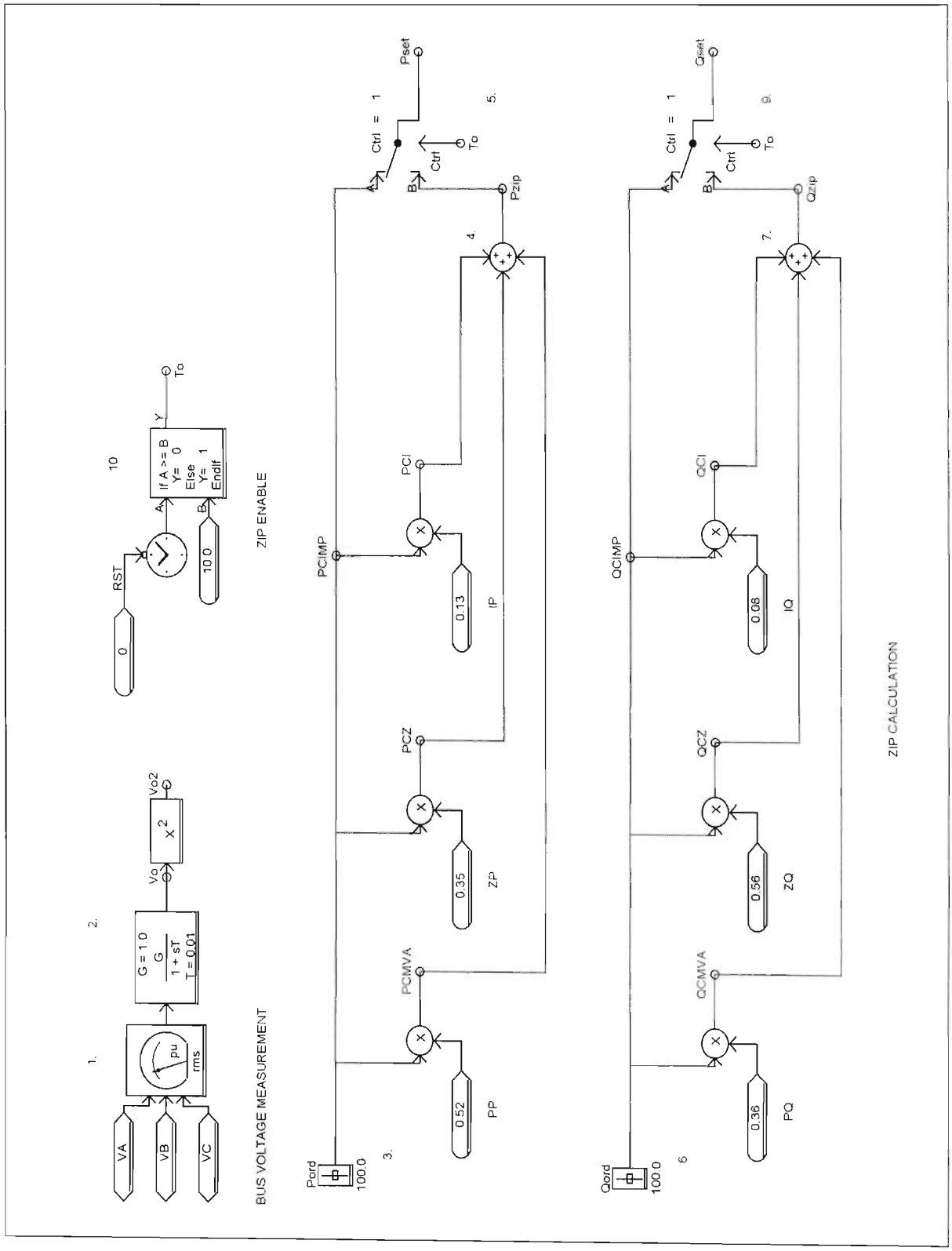

Fig. 3.4 RTDS ZIP (polynomial) load model calculation block [24].

The part of the real power component that is constant current (PCI) is obtained by multiplying Pord by the fraction of the load that is constant current IP and the voltage V_0. The sum of the three components of the real power that are constant impedance, constant current, and constant power (block 4) gives the calculated real power set point (Pzip). The calculations for the reactive power set point Qset of the dynamic load described in section 3.3 is done using a similar procedure to that used to calculate Pset described above. The desired value of reactive power at nominal voltage Qord is set by a slider (block 6). The fractions of the reactive power component of the load that are constant power; constant impedence, and constant current are represented by the constants PQ, ZQ and IQ respectively shown in the figure. The measured value of the bus voltage and the square of the voltage are used in a similar manner to that described for the real power component to obtain the calculated reactive power set point Qzip of the dynamic load model.

At the beginning of a real-time simulation, it is necessary to allow the system variables to reach a steady state before activating the ZIP calculation component. This is achieved by using selector switch components (5 and 9) for the real and reactive power component set points respectively. When the input T_0 to each of the selector switches is logic 1, the switches are in position A, and the real power set point equals Pord, while the reactive power set point equals Qord. When the input T_0 equals 0, the switches are in position B, and the real power and reactive power set points are the dynamically calculated values with ZIP characteristics Pzip and Qzip respectively. The value of T_0 is determined by a timer function (block 10) and a parameter set by the user in the ZIP block.

3.3.2 Exponential load model

The RTDS's exponential load model is implemented with the control block of Fig. 3.5. The control block implements the voltage dependence of loads by using the exponential load model given in equations (2.5) and (2.6). A three phase rms meter (block 1) measures the voltage (in per-unit) at the point where the load model is attached. The measured voltage is filtered using a first order lag filter (block 2) with a gain of 1.0 and time constant 0.01s. The output of the filter is the measured bus voltage VPU. The measured bus voltage is raised to the power of K_{pv} (block 4) and the answer is multiplied by the value of the real power desired at nominal voltage Pord to determine the calculated real power set point of the dynamic load Pecl.

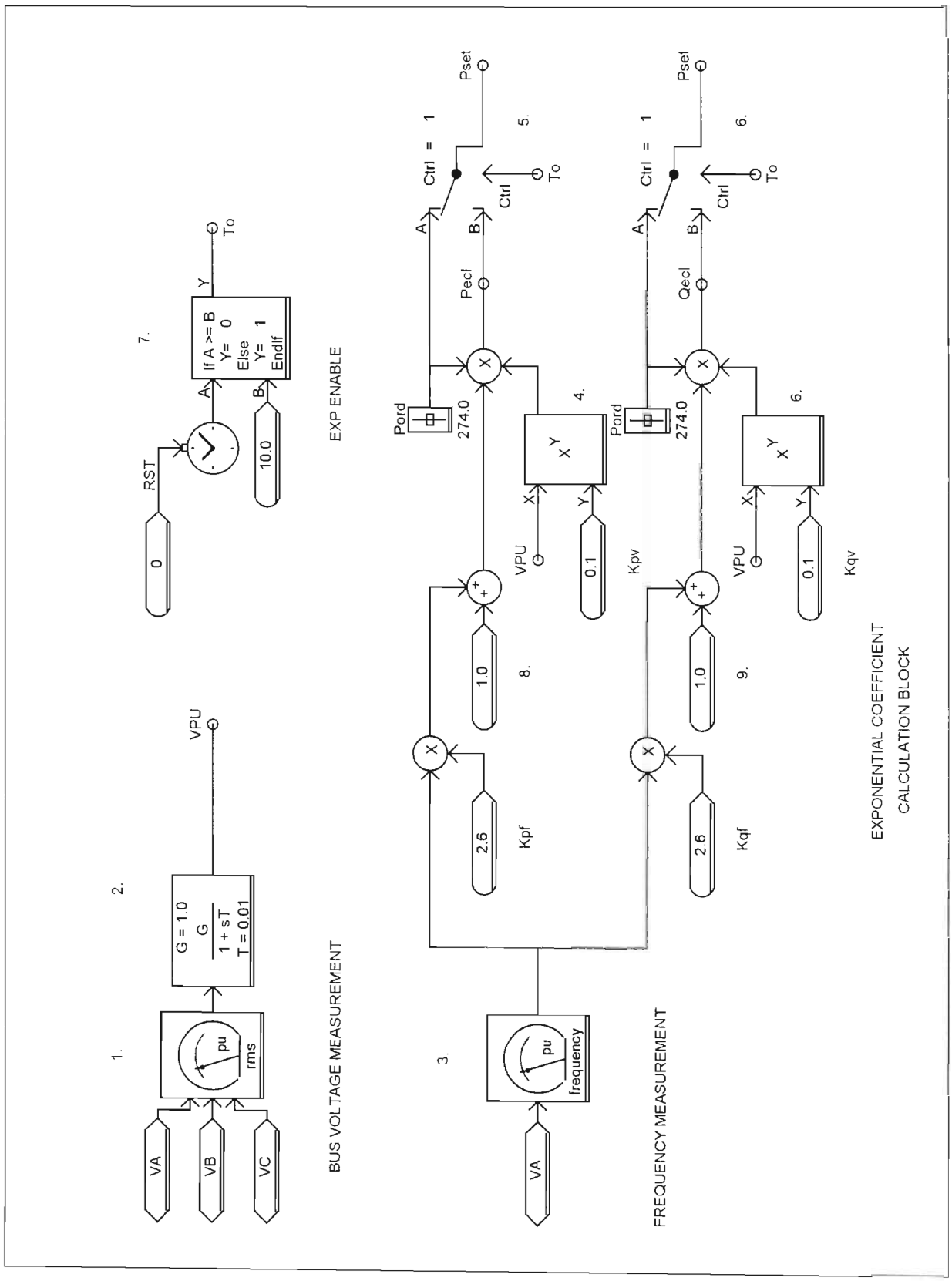

Fig. 3.5 RTDS Exponential load model calculation block [24].

The reactive power set point of the dynamic load model (Qecl) is calculated by raising the measured bus voltage VPU to the power of K_{qv} (block 6).The values of the exponents K_{pv} and K_{qv} depend on the type of the load. The exponential coefficient calculation model incorporates factors K_{pf} and K_{qf} and constant values 1.0 (block 8 and 9) together with a measured value of frequency in per-unit (block 3) to represent the effects of change in frequency (block 3) on load. If frequency dependency of the load is neglected, as is normally the case in voltage stability analysis [1], the factors K_{pf} and K_{qf} in Fig. 3.5 are both set to zero. Selector switches (5 and 6) are used to set the values of the real power set point Pset and the reactive power set point Qset equal to Pord and Qord respectively during start up to allow the simulation to attain steady state. After a time delay determined by the time delay function (block 7) the value of the real power set point Pset and reactive power set point Qset are switched to Pecl and Qecl respectively which are the dynamically calculated set points.

It is also possible to include dynamic load models such as induction motors and thermostatically controlled loads in the real-time simulator studies. However these are outside the scope of this thesis.

3.4 Transformer On-Load Tap Changer

Fig. 3.6 shows a real-time model of an on-load tap changer (OLTC) transformer controller that has been developed for use on the RTDS as part of the work of this thesis. The model is developed using control function components of the RSCAD software suite. The OLTC controller regulates the magnitude of the voltage at the controlled bus to within a deadband of the voltage set point. A three-phase rms meter (block 1) is used to measure the magnitude of the voltage (in per-unit) at the controlled bus. This measured voltage is subtracted from a user-defined voltage set point (block 2) using a summing function (block 3) to obtain the voltage error signal (Verr). Two comparators (blocks 4 and 5) are used to compare this voltage error signal to a user-settable deadband (block 6) to produce logic signals that indicate when tap up or tap down movement of the transformer tap position is required. If the voltage error signal is positive and its magnitude is greater than the deadband, a tap up signal (logic 1) is output from the comparator block 4, while if the voltage error signal is negative and its magnitude is greater than the deadband, a tap down signal (logic 1) is output from the comparator block 5. Otherwise both comparators'

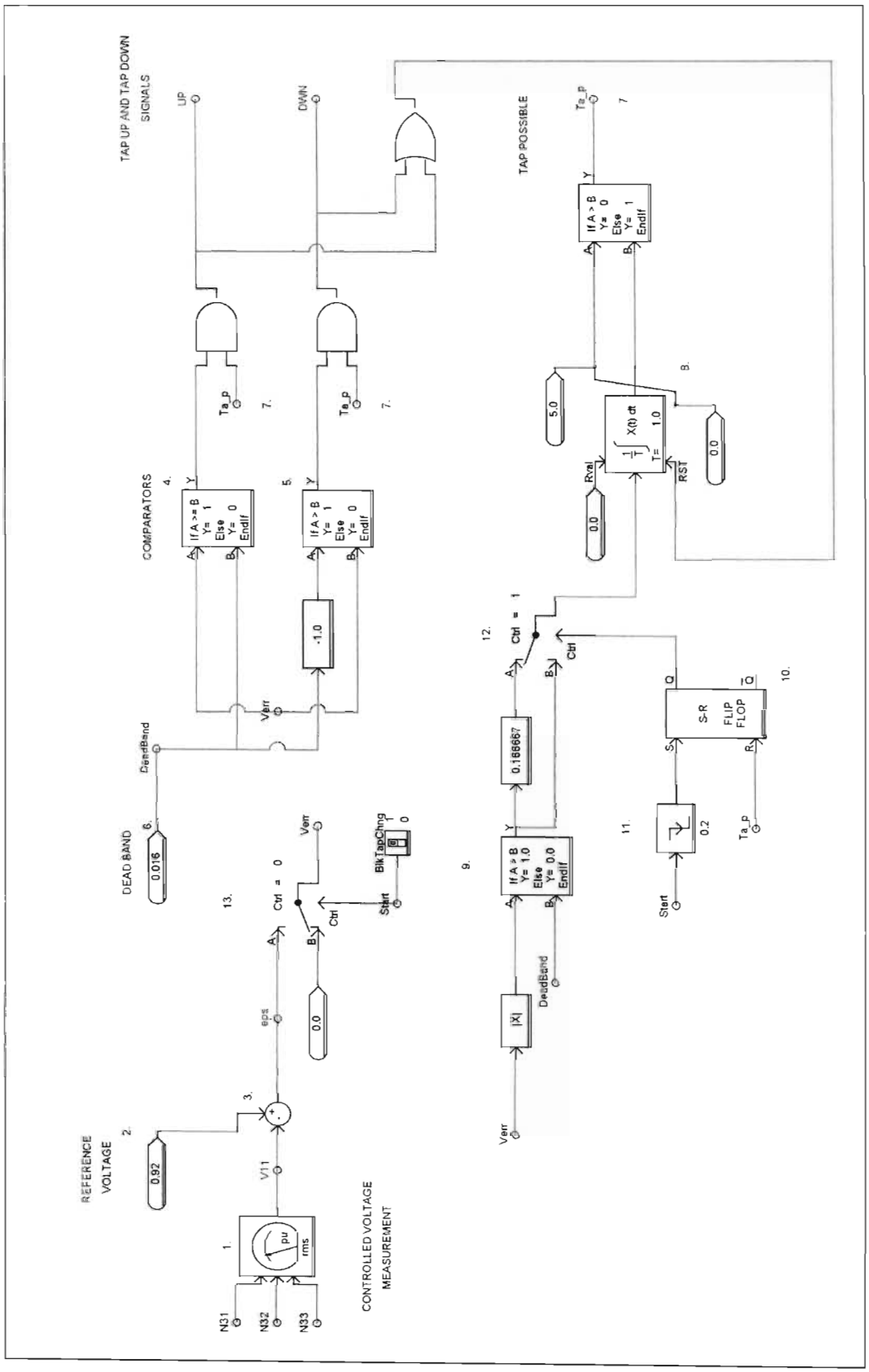

Fig. 3.6 Real-time model of an on-load tap changer transformer controller developed for use on the RTDS.

outputs are zero, indicating that the voltage at the controlled bus is within the deadband of the voltage reference and no tap up or tap down movements of the transformer are required. The logic signals at the outputs of these comparators are logically ANDed with another logic signal *tap-possible* (block 7) to produce the actual logic control signals *tap-up* and *tap-down* (UP and DWN respectively) that are connected as inputs to the transformer's tap changer. The *tap-possible* signal controls the tap changing mechanism by allowing tap movements only at discrete time intervals. In practice time delays between successive tap movements are required to ensure that the mechanical tap changer has completed its tap movement before the next tap movement command is issued. The time delay for the first tap movement is typically longer than that for subsequent tap movements to avoid the tap changer acting during temporary voltage deviations [2]. An integrator function (block 8) and comparator (block 9) provide the required time delays for the *tap-possible* signal by providing output logic 1 when the integrator output reaches its upper limit. An S-R flip flop (block 10) and a pulse generator function (block 11) provide additional logic outputs needed to set a selector function (block 12) to distinguish between the first tap movement and subsequent tap movements. The logic output of the flip flop for the first tap movement is 1, while the logic output for subsequent taps is 0. Both the integrator and flip flop are reset whenever the voltage error magnitude falls back within the deadband.

3.5 Generator Excitation Control System Modelling

The primary function of an excitation system is to provide dc current to the field winding of the synchronous machine. In addition, the excitation system performs control and protective functions. Control functions include voltage control, reactive power flow and system stabilizing controls [2]. Control of synchronous machine terminal voltage provides the most important means of controlling the voltage profile in power systems [2]. The excitation system automatically adjusts the field current of the synchronous machine to maintain the terminal voltage as output power of the machine varies. Protective functions are necessary to prevent the synchronous machine operating outside its capability limits thereby protecting both the armature winding and field winding.

3.5.1 AVR modelling

Fig. 3.7 shows a block diagram of a simple automatic voltage regulator (AVR) considered in this thesis for use on the RTDS. The AVR incorporates an input signal from a field current limiter described in section 3.5.2 below. The inputs to the main summing junction are the generator terminal voltage Vt, voltage reference Vref, and a control signal from the overexcitation limiter Voxl.

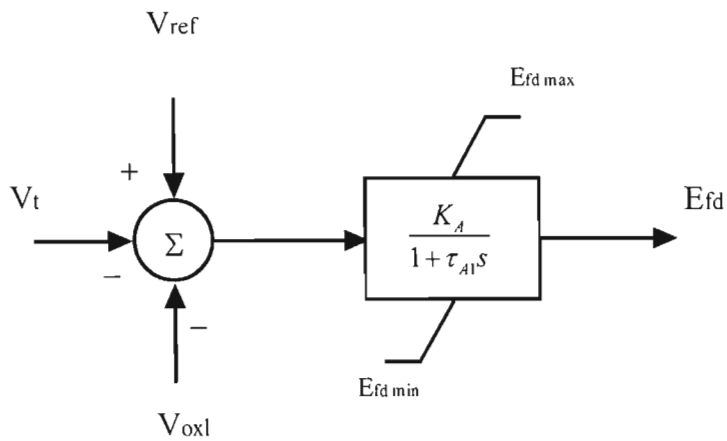

Fig. 3.7 A simple AVR [1].

3.5.2 Overexcitation limiter

There are two main categories of overexcitation limiters: the "summed" type overexcitation limiter and the "take-over" type overexcitation limiter [1,20]. The output signal of the summed type overexctation limiter is added at the AVR main summing junction with a negative sign, which has the same effect as reducing voltage reference value Vref of the AVR. In the "take-over" type overexcitation limiter on the other hand, the main excitation control loop is replaced with either the output from the main summing junction of the AVR or the output from the overexcitation limiter depending on which has the minimum or most negative value. Reference [20] presents the development of overexcitation limiter models of both these types for use in the PTI PSS/E power system simulation program. In this thesis real-time models have been developed for two overexcitation limiters of the summed type, as required by the particular benchmark systems being considered for study; one which acts with an inverse time delay in limiting

the field current, and another type that has two maximum set limits: a high set limit that imposes an instantaneous limit on the field current and a low set limit that acts with an inverse time characteristic to limit the field current. Fig. 3.8 shows an overexcitation limiter of the former type. This overexcitation limiter allows the field current to exceed the field current limit for a variable time, depending on the magnitude of the overcurrent. After the necessary time delay the overexcitation limiter forces the field current back down to the maximum limit. The inputs to the overexcitation limiter are the field current i_{fd} and field current limit $i_{fd\,max}$ as shown in the diagram. The difference between i_{fd} and $i_{fd\,max}$ x_1 goes through a two-slope gain (block 1 in the figure) obeying: $x_2 = s_1 x_1$ if $x_1 \geq 0$ or $x_2 = s_2 x_1$ if $x_1 < 0$, where s_1 and s_2 are two positive values of the slope and x_2 is the output of the two-slope gain block. The output of the two-slope gain x_2 is fed to a non-windup integrator (block 2) with upper and lower limits K_2 and $-K_1$ respectively. The integrator is initially at its negative lower bound $-K_1$. The output from the integrator x_t goes to a selector switch (block 3) which is initially in the lower position since $x_t < 0$. If the field current becomes larger than the field current limit the integrator output x_t begins to increase. As soon as x_t becomes positive, the selector switch (block 3) switches to the upper position as shown in the figure.

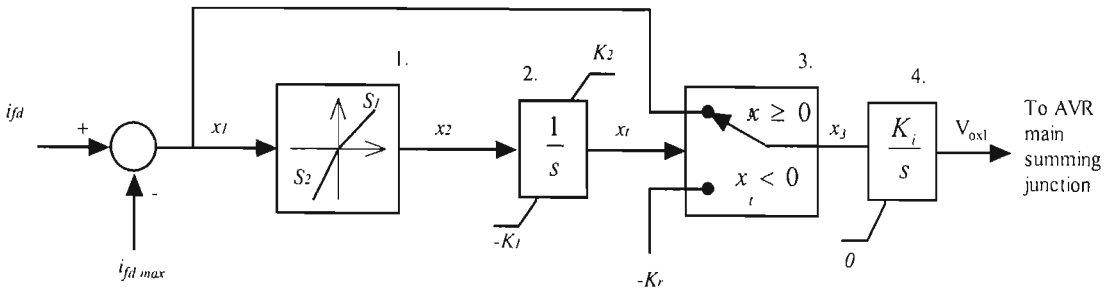

Fig. 3.8 Block diagram of an overexcitation limiter with inverse time field current limiting [1].

The output x_3 is fed to a limited integrator (block 4) which is initially set to its zero lower limit. As x_3 increases, the output of this integrator V_{oxl} increases. The output of the limited integrator V_{oxl} is fed to the main summing junction of the AVR shown in Fig. 3.7 with a minus sign for field current limiting. This signal reduces the reference voltage Vref of the

AVR. A second type of overexcitation limiter developed for use on the RTDS in this thesis is shown in Fig. 3.9. The overexcitation limiter has two maximum field current settings: the low set limit $i_{fd\,max\,1}$ and high set limit $i_{fd\,max\,2}$. The low set limit is a continuous field current limit, representing the maximum field current that is allowed continuously or permanently. The high set limit is the field current at which the overexcitation limiter is designed to limit the field current instantaneously. If the field current increases above the low set limit, the overexcitation limiter acts to limit the field current following an inverse time curve. However if the field current goes above the high set limit, the field current is limited instantaneously.

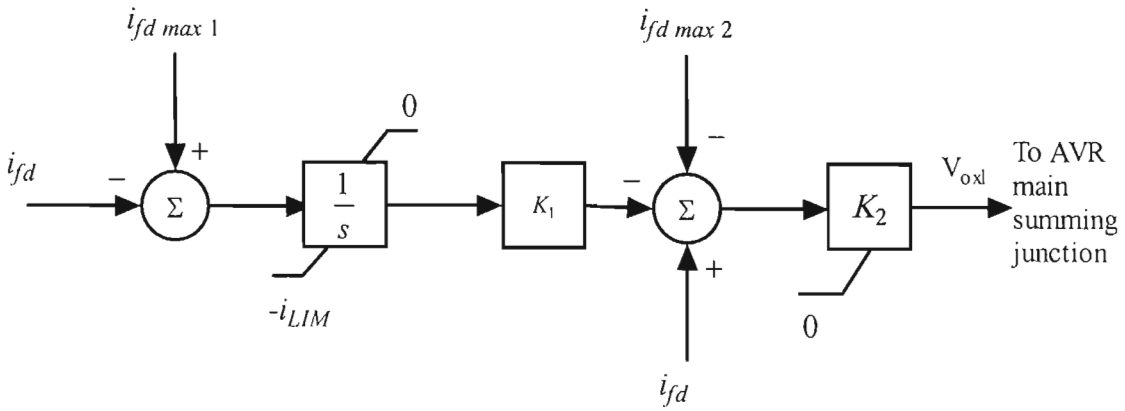

Fig. 3.9 Block diagram representation of an overexcitation limiter with inverse time and instantaneous field current limiting [6].

Fig. 3.10 shows the diagram of a real-time model of the AVR described in section 3.5.1 and the overexcitation limiter shown in Fig. 3.8 described above. Fig. 3.11 also shows a real-time model of a simple AVR together with the type of the overexcitation limiter shown in Fig. 3.9.

3.5.3 Synchronous condenser model

Fig. 3.12 shows the real-time simulator model of a synchronous condenser that has been implemented for use in the studies of this thesis. Block 1 shows the pre-configured RTDS model of a synchronous generator. Fig. 3.12 also shows a controller for the reactive power output of the synchronous condenser that has been developed in this thesis.

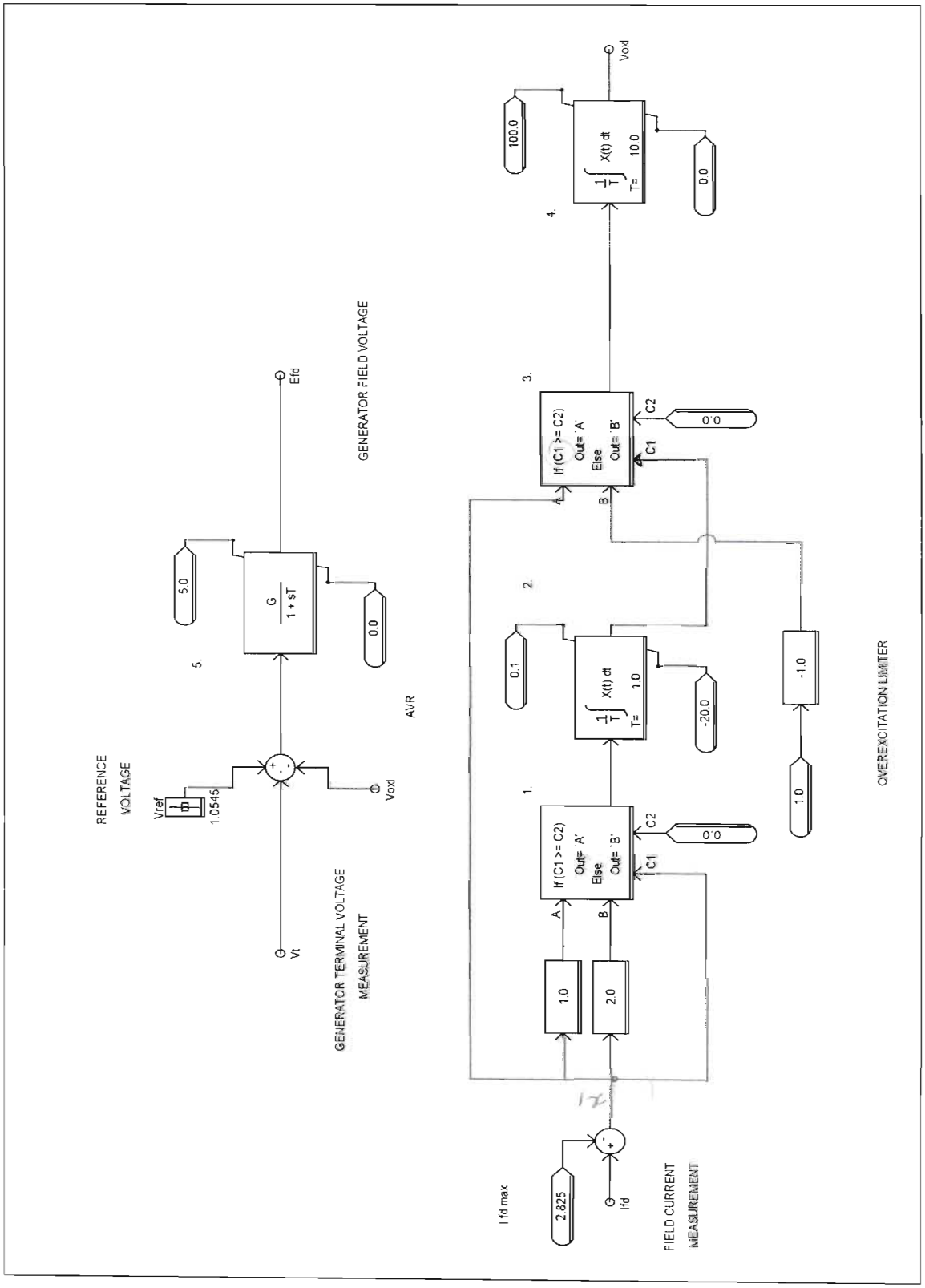

Fig. 3.10 Real-time model of a generator excitation control system as used in the small benchmark system.

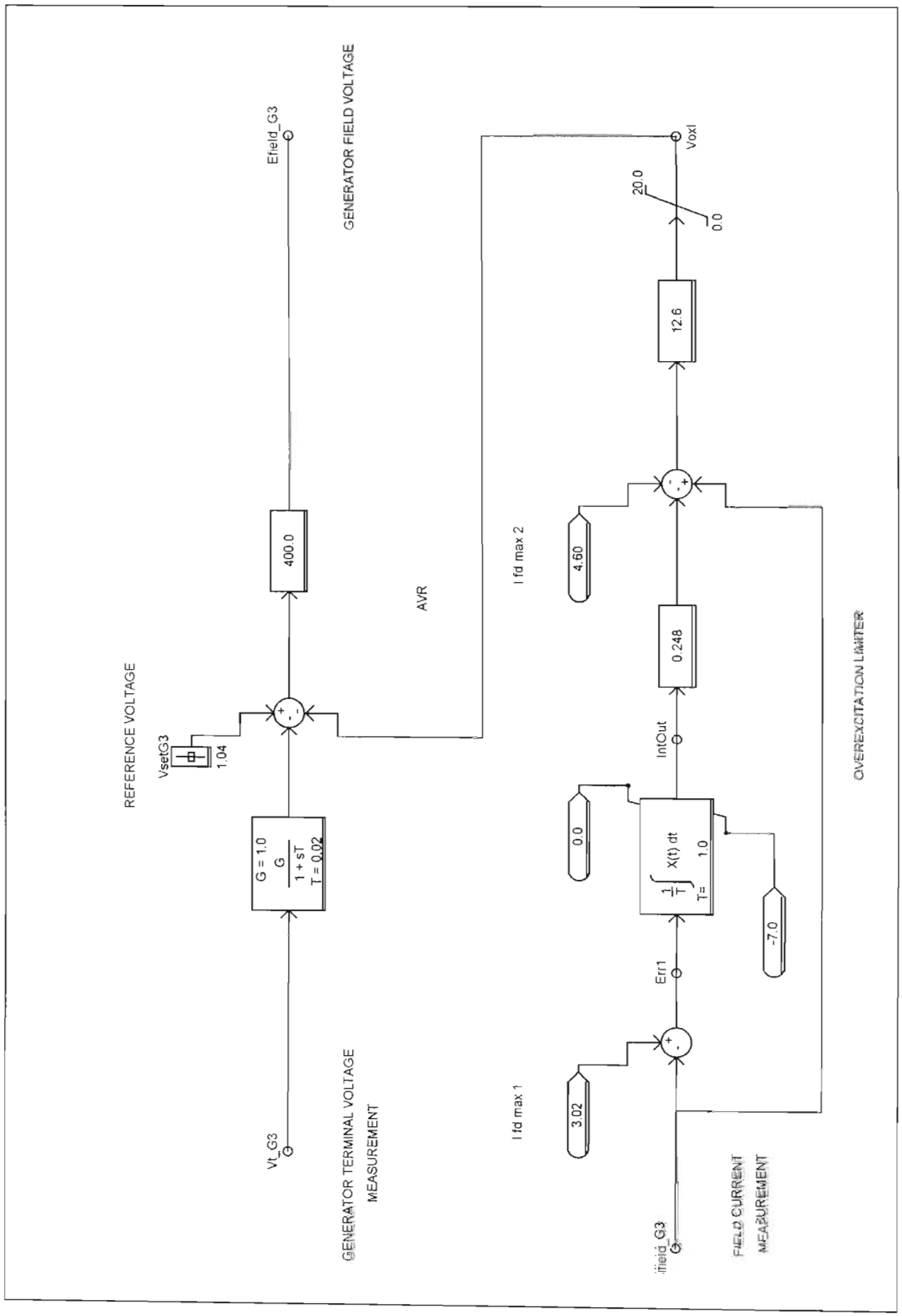

Fig. 3.11 A real-time model of a generator excitation control system with field current limiting function as used in the 11-bus benchmark system.

The controller uses a measurement of the reactive power output of the synchronous condenser and a user-settable reactive power reference in order to regulate the field current of the synchronous condenser. The inputs at the main summing junction of the controller are the measured reactive power output of the synchronous machine (number 2) in p.u. and the reactive power reference value of the synchronous machine (number 3). The summing junction (block 4) calculates the error in the reactive power output (Qerr) by subtracting the measured reactive power output of the synchronous condenser from the reactive power reference value of the synchronous condenser. This error signal Qerr is then input to a P-I (proportional and integral) controller (block 5) that regulates the field voltage, EfMAC2, (number 6) of the synchronous condenser. A limiter function (block 7) ensures that the field voltage of the synchronous condenser is kept within limits of 0.0 and 5.0 p.u. The reactive power set point of the synchronous condenser (number 3) is set to be either 0.0 p.u. or 1.0 through a selector switch. A voltage measurement from the power system or a dummy value (block 10) is used to determine the reactive power set point. A hysteresis block (block 9) prevents repeated changing of the set point on transition. When the reactive power output set point of the synchronous condenser is 0.0 the synchronous condenser floats on the system and does not supply or consume any reactive power, whereas when the set point is 1.0 p.u. the synchronous condenser supplies rated reactive power output to the system.

3.6 Static Var Compensator (SVC)

A static var compensator (SVC) is a shunt connected device that can provide rapid voltage control by continuously varying its susceptance. In practice there are many different methods of continuously varying the susceptance of an SVC. However, the most common means are by use of the thyristor controlled reactor (TCR) in parallel with a thyristor switched capacitor (TSC) and a fixed capacitor (FC) [25]. In this thesis, a pre-configured real-time model of an SVC was used for voltage stability control of the 11-bus voltage stability benchmark system. A control loop for regulating the reactive power output of the SVC was developed around the pre-configured real-time model of the SVC. Fig. 3.13 shows a schematic diagram of the SVC configuration considered in this thesis. The SVC consists of a TCR, a TSC, and a harmonic filter arranged as shown in the diagram of Fig. 3.13. The TCR is rated 450MVAr lagging, while the TSC is rated at 350MVAr leading.

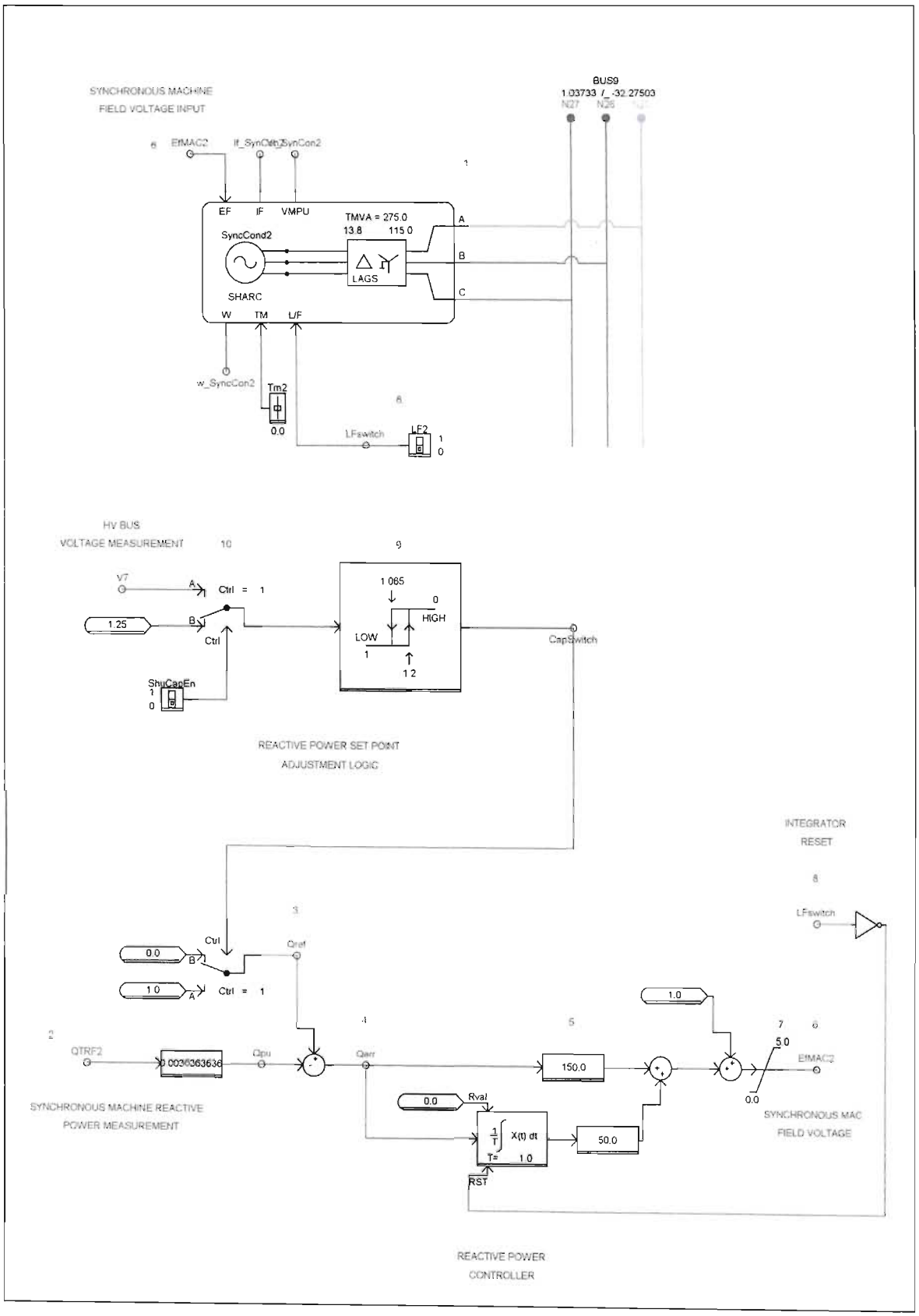

Fig. 3.12 Real-time simulator modelling of a synchronous condenser with reactive power control.

The harmonic filter is tuned to the 5th harmonic and has a leading reactive power output of 50MVAr at the fundamental frequency.

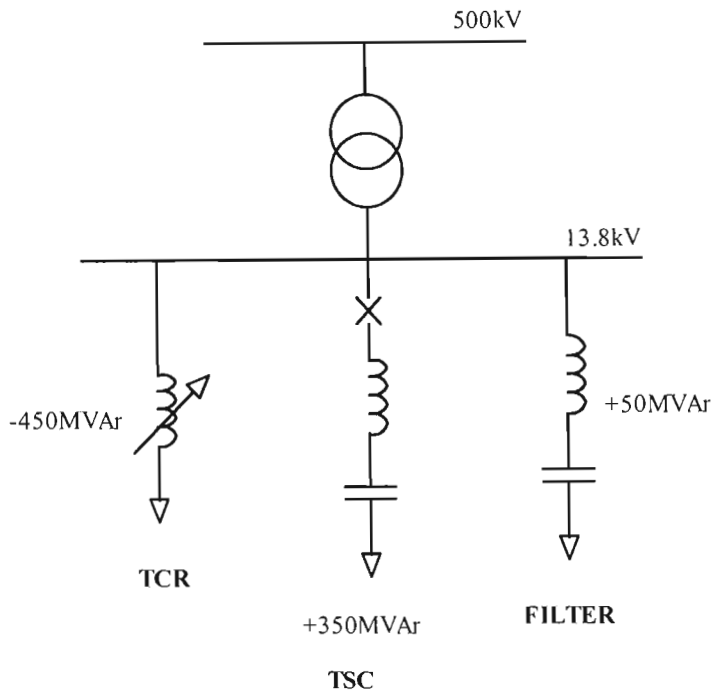

Fig. 3.13 Schematic representation of a static var system [25].

TCR operating principle

The principle of operation of the TCR can be explained using the diagram shown in Fig. 3.14. A reactor L, is connected in series with two thyristors that can conduct on alternate half cycles of the supply voltage as shown. The current through the reactor depends upon the thyristor firing angle.

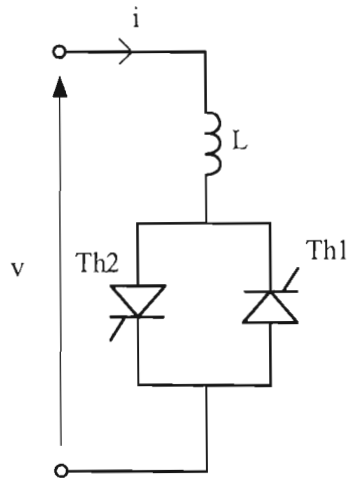

Fig. 3.14 Diagram of one phase of the thyristor controlled reactor [25].

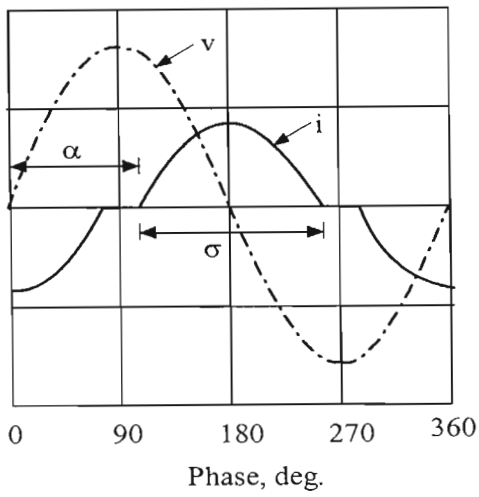

Fig. 3.15 Voltage and current waveforms of a TCR [25].

With the positive zero crossing of the supply voltage as reference, a firing angle of 90 degrees causes full conduction in the reactor. A firing angle of 180 degrees results in no current conduction in the reactor. The firing angle can be varied continuously between 90 degrees and 180 degrees in order to vary the current in the reactor from full conduction to zero conduction. Fig. 3.15 shows the waveform of the reactor current for an arbitrary firing angle α between 90 and 180 degrees. The fundamental component of this current waveform can be obtained using Fourier analysis as [25]:

$$I_1 = \frac{2(\pi - \alpha) + \sin 2\alpha}{\pi X_L} V \tag{3.7}$$

Where

α is the firing angle

V is the rms voltage and

X_L is the reactance of the reactor at fundamental frequency in ohms.

Thus from equation (3.7) the susceptance of the TCR as a function of firing angle at fundamental frequency is given by the equation:

$$B_L(\alpha) = \frac{2(\pi - \alpha) + \sin 2\alpha}{\pi X_L} \tag{3.8}$$

Fig. 3.16 shows the graph of B_L as a function of the firing angle α, where B_L is in per-unit.

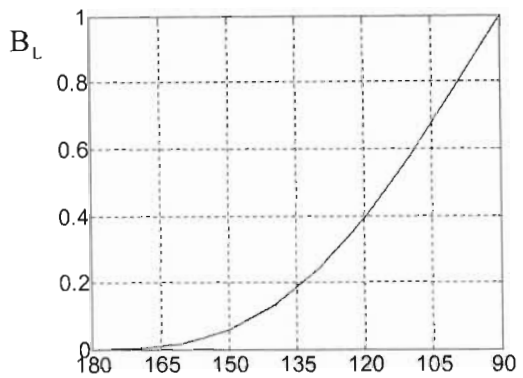

Fig. 3.16 Graph of B_L as a function of the thyristor firing angle , α [25].

3.6.1 SVC Parameters and specifications

The specifications of the SVC considered in this thesis are as follows:

Transformer: star-star connected, 500/13.8 kV, 400MVA, R=0.002 pu, X=0.1 pu.

TSC

The TSC is tuned to the 7th harmonic, +350MVAr at 60Hz and is star connected.

$X = 0.544114\Omega$ $C = 4775.6\,\mu F$ $L = 3.007 * 10^{-5}\,H$

TCR

TCR rated -450MVar at 60Hz, delta connected.

$X_L = 1.27\Omega$ $L = 0.00337H$

Filter

The filter is rated +50MVar at nominal frequency (60Hz) and tuned to the 5^{th} harmonic. The filter is connected in delta.

$X = 11.43\Omega$ $C = 222.86\mu F$ $L = 0.0013H$

3.6.2 SVC control

The main blocks of the SVC control system are shown in Fig. 3.17. The voltage or reactive power measuring device measures the controlled voltage or reactive power at the high voltage (HV) side of the step down transformer. The measured value of voltage or reactive power is compared with the voltage reference value or the reactive power reference value respectively. The error signal is fed to a regulator that determines the input to the firing angle calculator block. The firing angle calculator uses the output from the regulator to calculate the TCR thyristor firing angle required to regulate the voltage or reactive power of the SVC. The firing angle together with a synchronising signal from the phase locked loop are the inputs to the firing pulse generator that provides the thyristor firing pulses for the TCR. The pulse generator also generates firing pulses for the TSC thyristors that switch the TSC in or out as required.

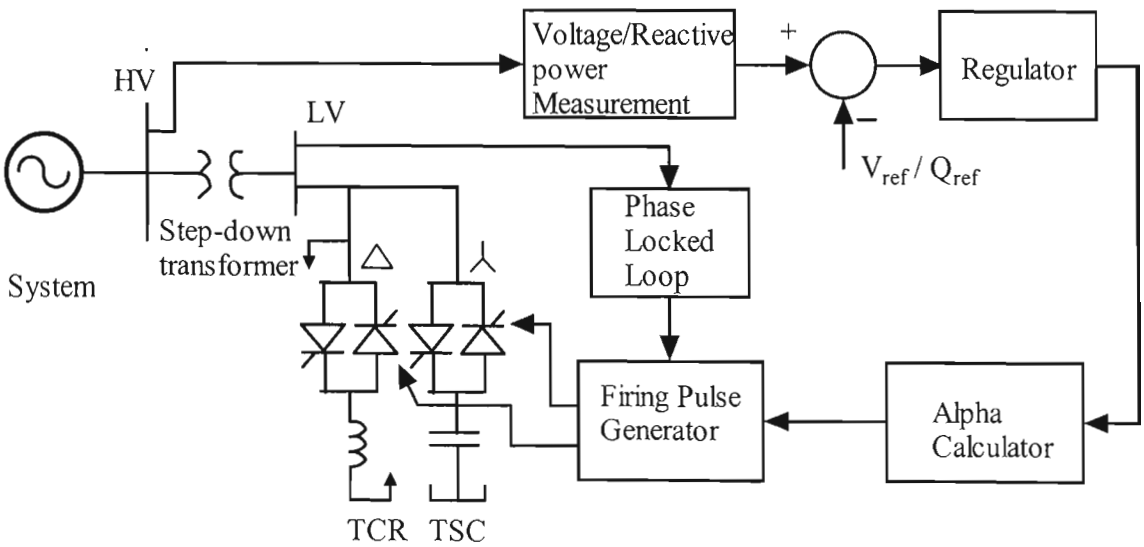

Fig. 3.17 SVC Control Block Diagram [26].

3.6.3 Real-time model of SVC

The real-time block diagram representation of a static var compensator used on the RTDS is shown in Fig. 3.18, together with the controller for the reactive power output of the static var compensator that has been developed for this thesis. The inputs at the main summing junction of the controller are the measured reactive power output of the static var compensator (number 2) in p.u. and the reactive power reference value of the static var compensator (number 3). The summing junction (block 4) calculates the reactive power error (Qerr) by subtracting the measured reactive power output of the static var compensator from the reference value of reactive power. The error signal Qerr is the input to a regulator (block 5) consisting of a first order transfer function that regulates the susceptance Bstar of the TCR (number 6). The output from the regulator together with the value of the TCR inductor's reactance (X_L) is used to determine the value of the TCR susceptance (B_L). A non-linear function (block 7) that contains the relationship between B_L and α for the TCR [as given by equation (3.8)] is used to calculate the required value of the firing angle α in degrees. A phase locked loop (block 11) whose output represents the phase angle of the A phase of the supply voltage together with the calculated angle alpha are supplied to a firing pulse generator (block 12). The function of the firing pulse generator is to provide firing signals for TCR thyristors at the appropriate firing angle alpha so as achieve the required TCR susceptance. The pulse generator also generates firing pulses that switch the TSC in and out as required. The reactive power set point of the static var compensator Qref is set to be either 0.0 p.u. or 1.0 through a selector switch (block 3). A voltage measurement from the power system or a dummy value (block 10) is used to determine the reactive power set point. A hysteresis block (block 9) prevents repeated changing of the set point on transition. When the reactive power set point of the static var compensator is 0.0 the static var compensator floats on the system and does not exchange reactive power with the system, whereas when the set point is 1.0 p.u. the SVC supplies rated reactive power to the system.

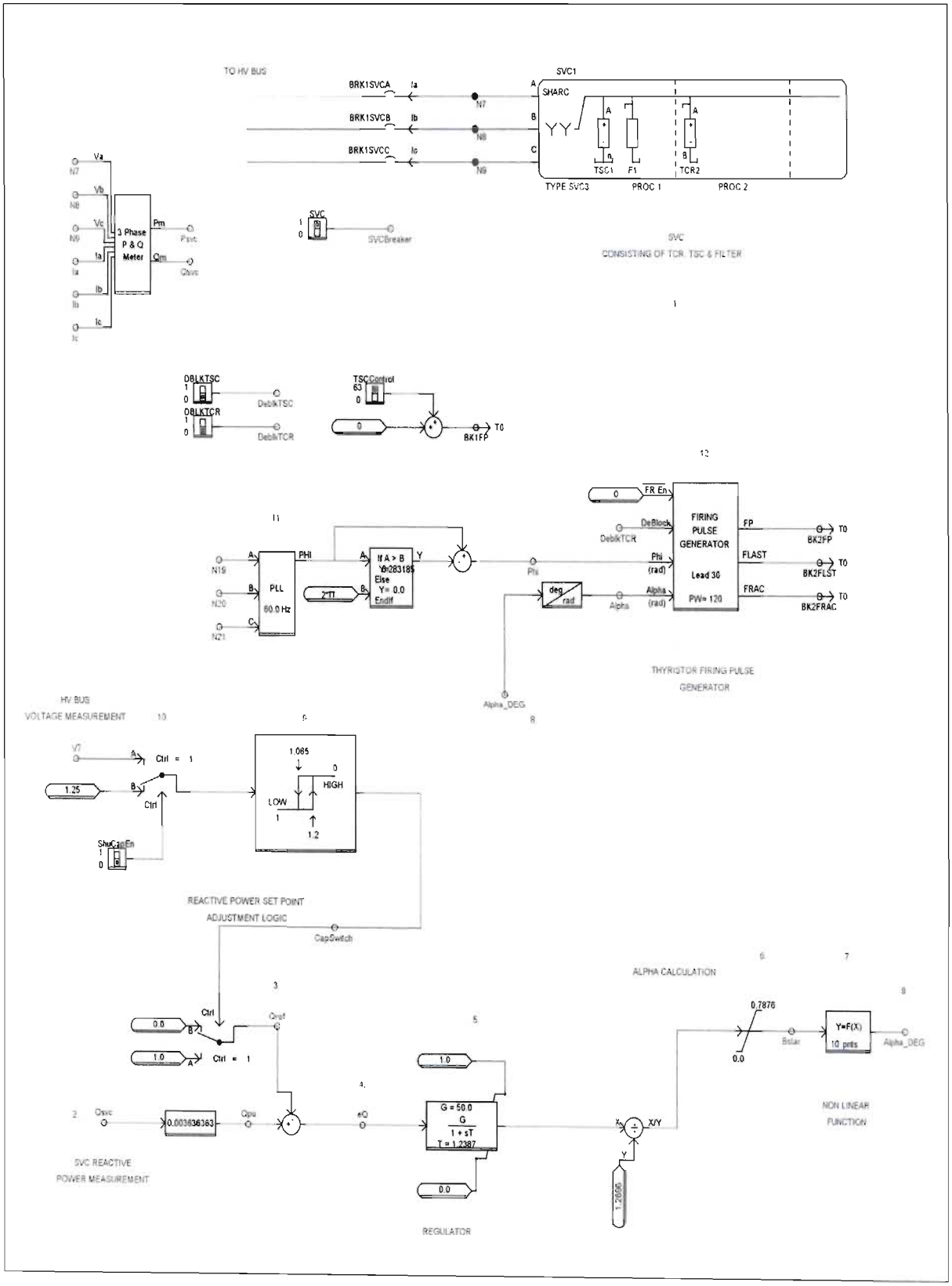

Fig. 3.18 Real-time simulator modelling of a static var compensator for reactive power control mode.

3.7 Conclusion

This chapter has presented a discussion of the performance and modelling of some power system components that are important for voltage stability studies. The chapter has presented a discussion of transmission line characteristics and described RTDS's real-time travelling wave transmission line model. Concepts of surge impedance loading and voltage profile along a transmission line at various load levels have been discussed, and some results have been presented to illustrate transmission line characteristics under different loading conditions using a real-time model. The chapter has also presented a discussion of real-time models of dynamic loads that are used on the RTDS. Two dynamic load models have been considered namely, the polynomial load model and exponential load model. The chapter has also presented real-time model development of some power system controllers that are known to be important in voltage stability incidents. The chapter has presented development of a custom real-time model of an OLTC controller for use on the RTDS. The development of generator excitation control system models including overexcitation limiters for voltage stability studies on the RTDS has been presented. A controller for regulating synchronous condenser reactive power output has been developed and its real-time simulator model presented in this chapter. Finally, the chapter has described the RTDS model of an SVC and its control loop to regulate the reactive power output that has been developed in this thesis.

The next chapter presents the development of real-time models of two benchmark systems for voltage stability studies using the custom models of power system components presented in this chapter as well as some generalised component models available in the components library of the RSCAD software suite.

CHAPTER FOUR

REAL-TIME VOLTAGE STABILITY BENCHMARK SYSTEM STUDIES

4.1 Introduction

The previous chapter presented the development of real-time models of power system components that are important for voltage stability studies. That chapter presented a discussion of the characteristics and real-time modelling of the transmission lines and dynamic load components that influence voltage stability. In that chapter the development of custom real-time models of power system components for use on the RTDS was also presented, in particular: a transformer tap changer controller; a generator excitation control system with overexcitation limiter function; synchronous condenser and static var compensator reactive power controllers.

This chapter presents the development of real-time models of two benchmark systems for voltage stability studies on the RTDS. The benchmark systems are developed using the power system components developed in chapter three together with the generalised models of power system components provided in the RSCAD software suite. The validity of the power system components developed in the last chapter is proved using a small benchmark system. Real-time simulation of the small benchmark system under specific conditions is conducted on the RTDS. The simulation results of the small benchmark system obtained with the RTDS are in very close agreement with the simulation results of the system documented in reference [1]. The chapter then presents real-time model development of an 11-bus benchmark system. Real-time simulation results of the 11-bus benchmark system obtained using the RTDS are also in very close agreement with the simulation results obtained using the Extended Transient/Midterm Stability Program [6].

4.2 Small Benchmark System

The real-time models of power system components developed in chapter three together with components in the RSCAD software suite were used to develop a real-time model of a

small benchmark test system. The small benchmark system developed was used to prove the validity of the models of power system components developed in chapter three. Fig. 4.1 shows the one-line diagram of the small benchmark system.

4.2.1 System description

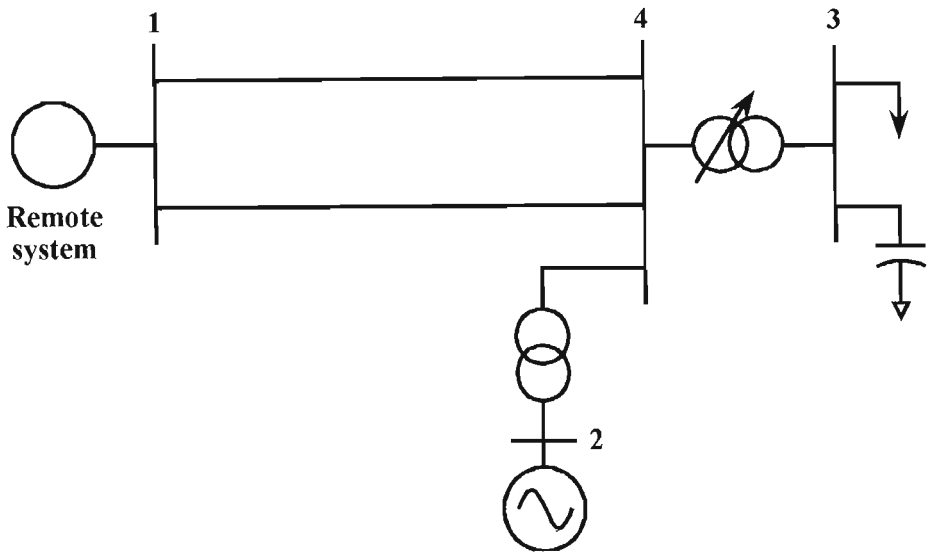

Fig. 4.1 One-line diagram of the small benchmark system [1].

The system consists of an infinite bus, bus 1, supplying a load at bus 3 through two long, parallel transmission lines. The load at bus 3 is fed through an on-load tap changing transformer. A local generator at bus 2 provides additional power to the load through a step up transformer with a fixed tap ratio. The disturbance considered is the loss of one transmission line between bus 1 and bus 4.

4.2.2 Small Benchmark system modeling

Bus 1 in Fig. 4.1 is an infinite bus, and is modeled as a constant magnitude and frequency voltage source. The transmission lines between bus 1 and bus 4 are represented by their series reactances, with the series resistance, shunt capacitance and shunt conductance of the lines neglected for simplicity. The step-up transformer between bus 2 and bus 4 has a fixed turns ratio while the load transformer between bus 4 and bus 3 is equipped with an on-load tap changer, aimed at keeping voltage at bus 3 within a deadband of a reference value. The real-time model of the on-load tap changer for the transformer between bus 3

and bus 4 is described in section 3.4. The generator at bus 2 is represented by the pre-configured synchronous machine model in the RSCAD library.

Excitation system modeling

The AVR is modeled by a simple first order transfer function with internal limits on the field voltage. The overexcitation limiter model included in the small benchmark system is of the *summed* type described in section 3.5.2. The real-time model of the AVR with the overexcitation limiter used in the small benchmark system is shown in Fig. 3.10.

Load modeling

The load at bus 3 is represented as exponential load model using the real-time model shown in Fig. 3.5. The shunt compensation at bus 3 is represented using a star-connected three phase shunt capacitor bank.

4.2.1 Small Benchmark System Data

Transmission lines (R, X and B in pu on 100MVA Base):

	R	X	B
1-4	0.0000	0.0277	0.0000

Transformers (R, X and B in pu on 100MVA Base):

	R	X	B
2-4	0.0000	0.0160	0.0000
3-4	0.0000	0.0040	0.0000

Transformer between bus 2 and bus 4: off-nominal turns ratio, $n = 1.04$ pu.

Machine parameters (reactances in pu on 500MVA Base):

$X_d = 2.1$ $X_q = 2.1$ $X'_d = 0.4$ $T'_{do} = 8\,s$

$H = 3.5\,s$ $D = 3.5\,pu$

In order to represent the model of the synchronous generator at bus 2 in Fig. 4.1 using the pre-configured synchronous generator model in the RSCAD library, approximate values of

the following additional parameters were used based on typical synchronous machine parameter values presented in reference [2]:

$R_a = 0.004$ $X_a = 0.2$ $X'_q = 0.228$ $X''_d = 0.25$

$X''_q = 0.25$ $T'_{qo} = 0.85$ $T''_{do} = 0.045$ $T''_{qo} = 0.045$

AVR

The AVR for the generator at bus 2 is modeled as shown in Fig. 3.7. The parameters of the model are as follows:

$K_A = 50$ $\tau_{A1} = 0.1$ $E_{fd\,min} = 0.0$ pu. $E_{fd\,max} = 5.0$ pu.

Overexcitation limiter

The model of the overexcitation limiter for the generator at bus 2 is shown in Fig. 3.8, and has the following parameters:

$I_{fd\,max} = 2.825$ pu. $S_1 = 1$ $S_2 = 2$ $K_1 = 20$

$K_2 = 0.1$ $K_r = 1$ $K_i = 1$

OLTC for the transformer between bus 4 and bus 3:

Time delay for the first tap movement: 20 s

Time delay for subsequent tap movements: 10 s

Dead band: ± 0.01 pu

Tap range: ± 15 steps

Step size: 0.01 pu

Load parameters:

$P_o = 1480$ MW $Q_o = 721$ MVAr

$K_{pv} = 1.5$ $K_{qv} = 2.5$

Shunt capacitor susceptance at bus 3 (in per-unit on 100MVA Base) = 6.0 pu.

Fig. 4.2 shows the real-time model of the small benchmark system that has been developed for this thesis. Appendix A shows the load flow data for the small benchmark system.

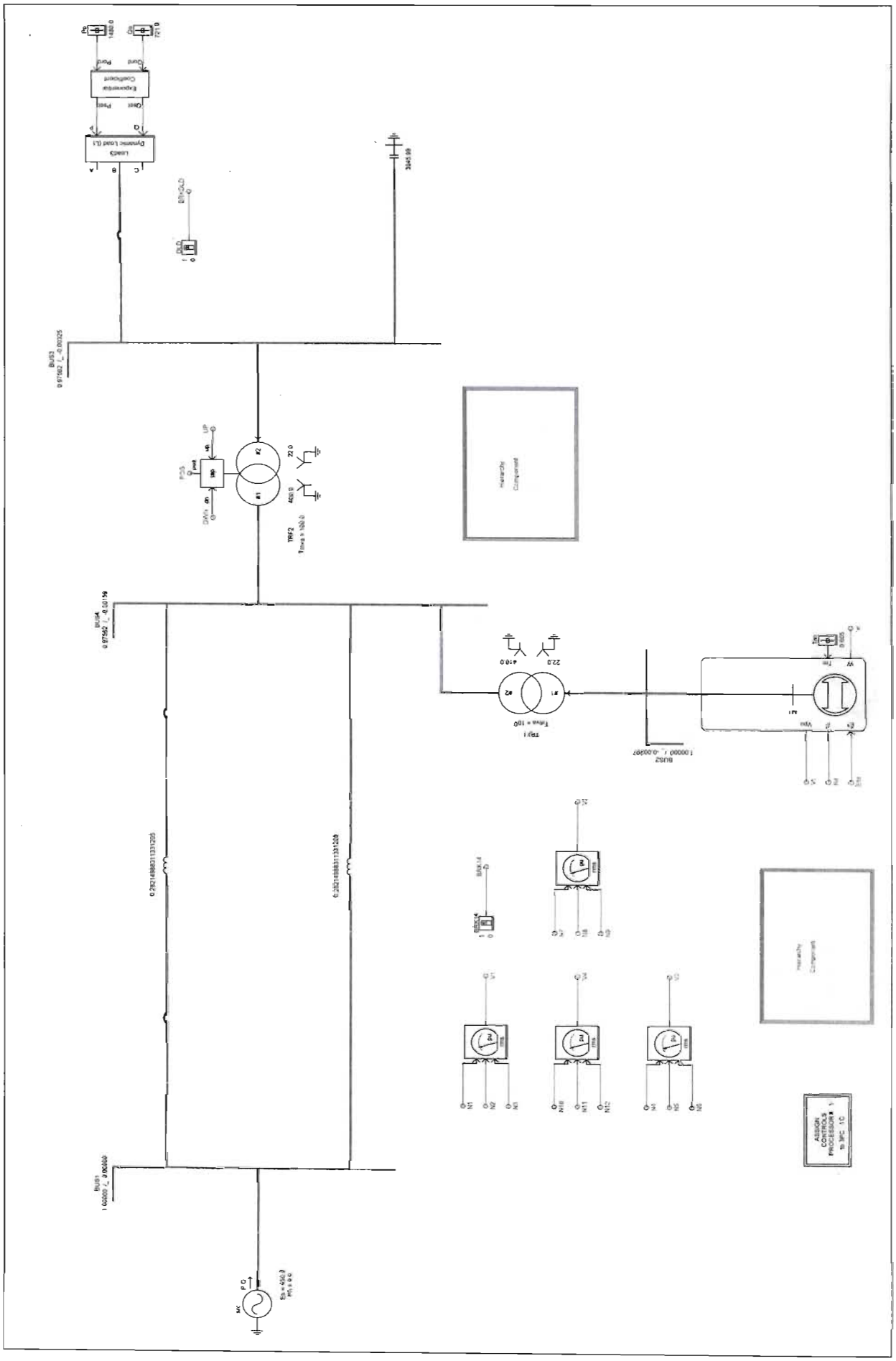

Fig. 4.2 Real-time model of the small voltage stability benchmark system.

4.2.3 Simulation results

Fig. 4.3 shows time domain simulation results for the small benchmark system using the real-time digital simulator (RTDS). Responses of load voltage (bus 3), transmission side voltage (bus 4), generator field current and transformer tap position are shown following the loss of one transmission line between bus 1 and bus 4.

The real-time simulation results for the small benchmark system in Fig. 4.3 show that immediately after the loss of the transmission line at t = 3s the load voltage drops from 1.01 pu. to 0.93 pu. and the transmission side voltage drops from 1.02 pu. to 0.97 pu. The voltage at the load bus is now outside the deadband of the voltage reference of the OLTC.

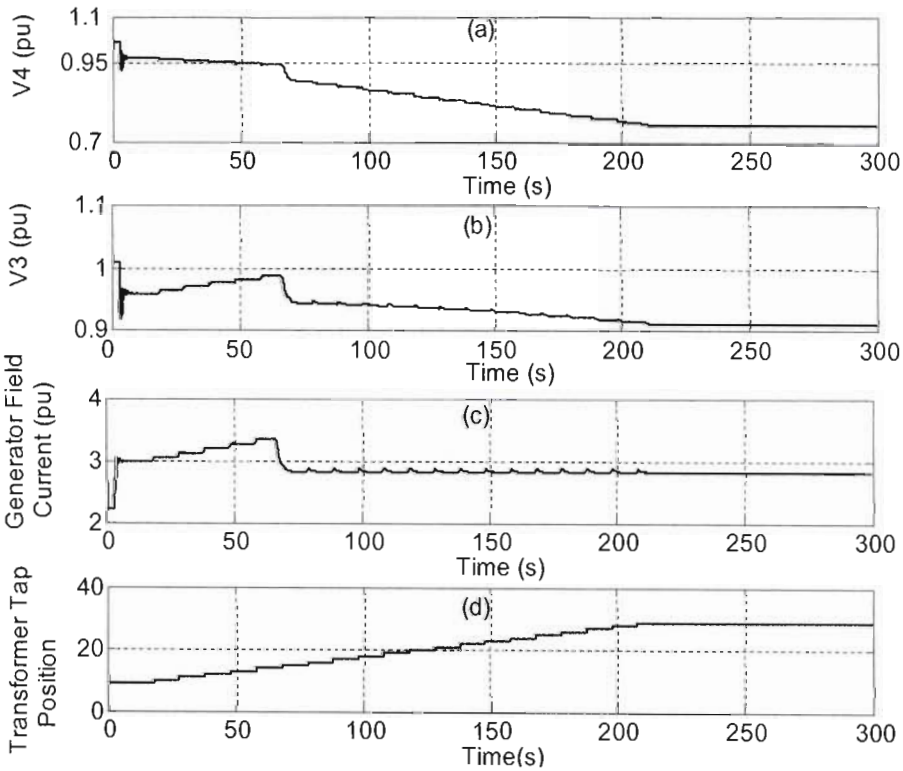

Fig. 4.3 Graphs of (a) Transmission side voltage (b) Load voltage (c) Generator field current and (d) Transformer tap position of the small benchmark system following loss of a line.

The field current of the local generator also increases from its initial value of 2.2 pu to 2.98 pu immediately after the loss of the transmission line, and is now above the field current limit setting of 2.825 pu of the overexcitation limiter. The field current limiter does not act

immediately because of its inverse time characteristic. The increase in the generator field current can be explained by the increase in the reactive power losses in the transmission line after one line is lost. Twenty seconds after the initial disturbance, the OLTC begins to operate by tapping up to restore the load voltage and continues thereafter to tap up at 10 second intervals. The action of the OLTC to restore load voltage causes further increase in reactive power demand, and thus the reactive power output and field current of the generator at bus 2 increase with each tap up movement. The overexcitation limiter of the generator at bus 2 limits the field current after about 67 seconds. The effect of the generator field current limiting is a drop in the terminal voltage of the local generator at bus 2, and hence voltages in both the transmission system and distribution system are reduced. Further attempts by the OLTC to restore load voltage do not result in the load voltage increasing but instead the load voltage decreases with each OLTC tap movement, indicating that the system is now voltage unstable. The load voltage drops progressively until the OLTC reaches its upper limit at about 210 seconds. After the OLTC has reached its upper limit, system voltages at all buses settle at values lower than their pre-disturbance values.

The real-time simulation results of the small benchmark system presented in Fig. 4.3, and described above, agree closely with results of similar studies of the same system presented in reference [1].

4.3 Study of an 11-Bus Benchmark System

4.3.1 System Description

Fig. 4.4 shows the one line diagram of an 11-bus voltage stability benchmark system modeled in this thesis. The 11-bus voltage stability benchmark system has been used for voltage stability studies in references [2,3,6]. The system consists of two generators supplying the load through five long parallel transmission lines, and a local generator in the load area for reactive power support. Generator G1 represents a large remote system and is modeled as an infinite bus, while generator G2 includes an excitation system modeled with no overexcitation limiter. Generator G3 on the other hand, has an excitation system that includes an overexcitation limiter. The load at bus 8 is supplied through a

distribution transformer T4 that has fixed taps, while the load at bus 11 is supplied through the transformer T6 with on load tap changing facility.

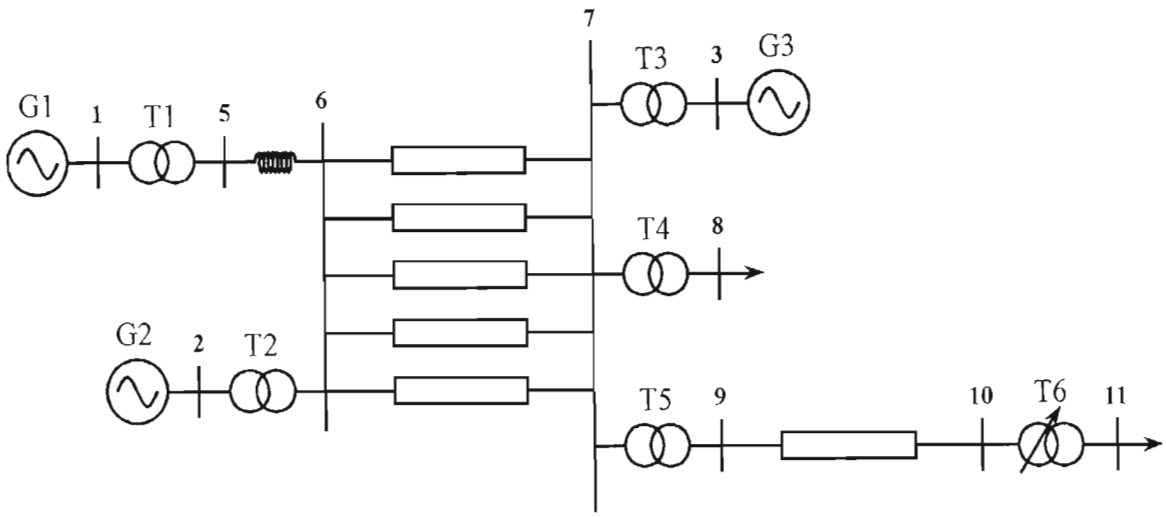

Fig. 4.4 The 11-Bus Voltage Stability Benchmark System [2].

4.3.2 System Modeling

The disturbance considered is the loss of one of the transmission lines between bus 6 and bus 7. Time domain simulations using the real-time digital simulator were conducted to determine the system response following the loss of the transmission line.

Transmission line modeling

The transmission lines between bus 6 and bus 7 are modeled using the traveling wave transmission line model described in section 3.2. The mathematical representation of the real-time traveling wave transmission line model used in this thesis known as the Bergeron transmission line model is given by equations (3.3) and (3.4). The short transmission line between bus 5 and bus 6 is modeled by a series reactance in each phase. The transmission line between bus 9 and bus 10 is modeled by a reactance and resistance in series in each phase.

Load modeling

The load at bus 11 is modeled as a ZIP load with 50% constant impedance and 50% constant current for both the active power and reactive power components, while the load at bus 8, is modeled as a constant MVA load for both the active power and reactive power components.

Transformer OLTC

The OLTC transformer T6 is modeled with a time delay of 30 seconds for the first tap movement and 5 seconds for subsequent tap movements. The deadband is assumed to be ± 0.01 p.u. of nominal voltage. The step size is 0.625% with a tap range of ± 16 steps. The real-time model of the OLTC used in this thesis is shown in Fig. 3.6.

Generator and excitation system

The generators at buses 2 and 3 were represented by the pre-configured synchronous machine model from the RSCAD library. The AVRs of generator G2 and generator G3 are modeled with a gain of 400 and a sensing circuit time constant of 0.02 second. The overexcitation limiter model of generator G3 is shown in Fig. 3.9 and has the following parameters:

$I_{fd\,max\,1} = 3.02\,pu$ $I_{fd\,max\,2} = 4.60\,pu$ $I_{LIM} = 7.0\,pu$

$K_1 = 0.248$ $K_2 = 12.6$

The real-time model of the AVR and overexcitation limiter for generator G3 is shown in Fig. 3.11.

4.3.3 11-Bus Benchmark System Data

The parameters used for the 11-bus benchmark system studies in this thesis the particular values cited in reference [2].

Transformers (R, X and B in pu on 100MVA Base):

	R	X	Ratio	
1-5	0.0000	0.0020	0.8857	
2-6	0.0000	0.0040	0.8857	
3-7	0.0000	0.0125	0.9024	
7-8	0.0000	0.0030	1.0664	
7-9	0.0000	0.0026	1.0800	
10-11	0.0000	0.0010	0.9750	(Load Level 1)
			0.9938	(Load Level 2)
			1.0000	(Load Level 3)

Transmission Lines (R, X and B in pu on 100MVA Base):

	R	X	B
5-6	0.0000	0.0040	0.0000
6-7	0.0015	0.0288	1.1730
9-10	0.0010	0.0030	0.0000

Shunt Capacitors:

Bus	MVAR
7	763
8	600
9	1710

Generator Parameters

Generator G1: Infinite bus

Generator G2: H = 2.09 , MVA Base = 2200 MVA

Generator G3: H = 2.33 , MVA Base = 1400 MVA

Stator and rotor parameters in per-unit for generator G2 and G3 on the machine MVA base are as follows:

$R_a = 0.0046$ $X_a = 0.155$ $X_d = 2.07$ $X_q = 1.99$

$X'_d = 0.28$ $X'_q = 0.49$ $X''_d = 0.215$ $X''_q = 0.215$

$T'_{do} = 4.10$ $T'_{qo} = 0.56$ $T''_{do} = 0.033$ $T''_{qo} = 0.062$

OLTC for Transformer T6:

Time delay for the first tap movement: 30 s

Time delay for subsequent tap movements: 5 s

Dead band: ± 0.01 pu

Tap range: ± 16 steps

Step size: 0.00625 pu

Fig. 4.5 shows the real-time model of the 11-bus benchmark system that has been developed for this thesis, while the load flow data for the system is presented in Appendix B.

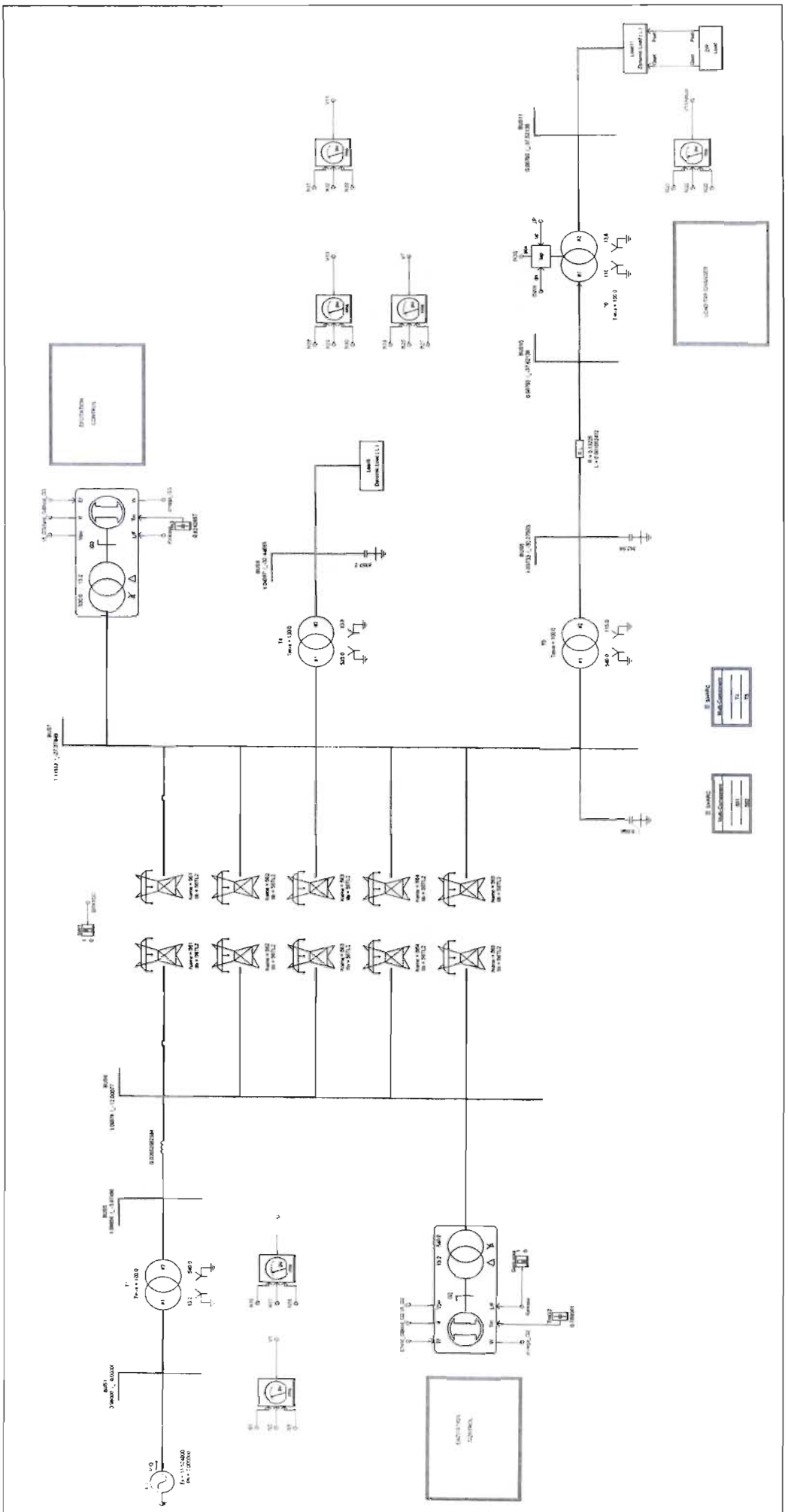

Fig. 4.5 Real-time model of the 11-bus voltage stability benchmark system.

4.3.4 Simulation results

Three cases with different pre-disturbance system load levels are considered: Load level 1; Load level 2; and Load level 3. Table 1 shows the pre-disturbance load at bus 8 and bus 11 for each of the three load levels.

	P[MW]	Q[MVAr]	
Bus 8	3271	1015	Load level 1
	3320	1030	Load level 2
	3345	1038	Load level 3
Bus 11	3376	965	Load level 1
	3378	969	Load level 2
	3449	991	Load level 3

Table 1: System load for each load level [2].

Figs. 4.6 to 4.8 show the response of the transmission system voltage (bus 7), sub-transmission system voltage (bus 10), distribution system voltage (bus 11), and the field current of generator G3 (IfieldG3) for each of the three load levels following the loss of one transmission line between bus 6 and bus 7. The figures also show graphs of the active power output of generator G3 (PGen3), the reactive power output of generator G3 (QGen3) and the reactive power supplied at bus 7 from generator G3 (QBus7) (i.e. the reactive power after the step-up transformer T3). The simulation results of the 11-bus benchmark system obtained using the RTDS in this thesis are in agreement with the results obtained using the Extended Transient/Midterm Stability Program (ETMSP), presented in [2,6].

At load level 1, the initial disturbance causes the voltages in the transmission, sub-transmission and distribution systems to drop, while the field current of generator G3 increases.

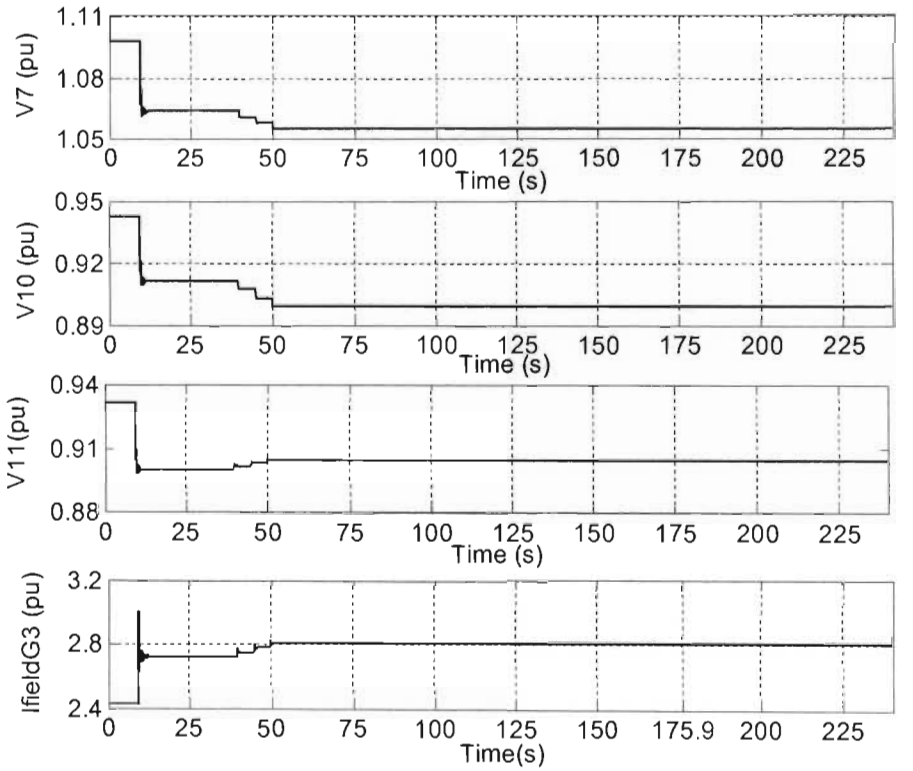

Fig. 4.6(a) Load level 1: Bus voltage magnitudes and field current of generator G3.

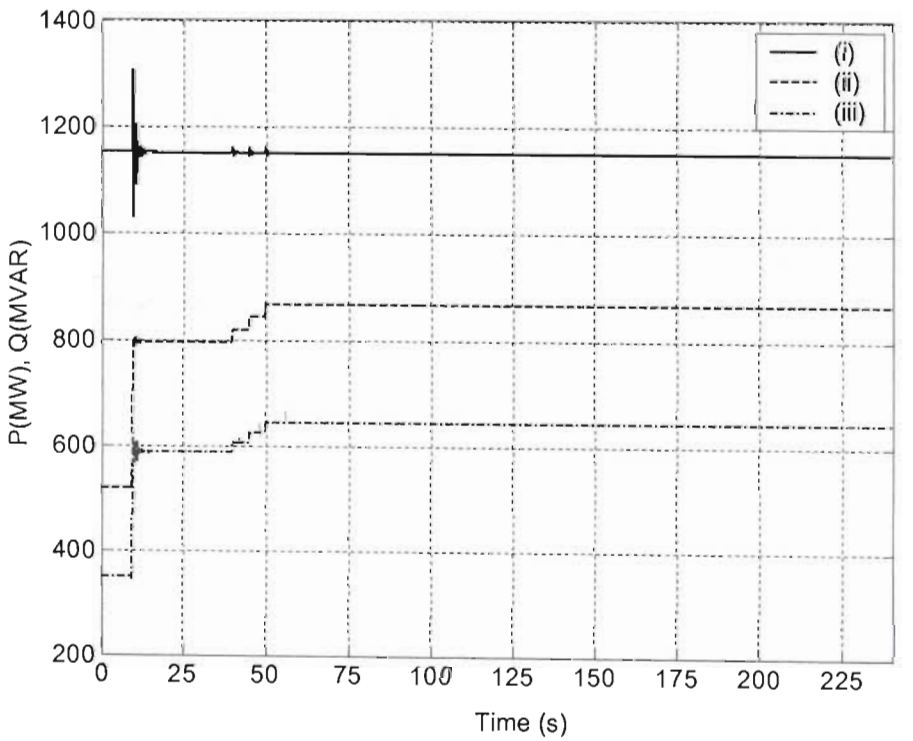

Fig. 4.6(b) Load level 1: (i) PGen3 (ii) QGen3 and (iii) QBus7.

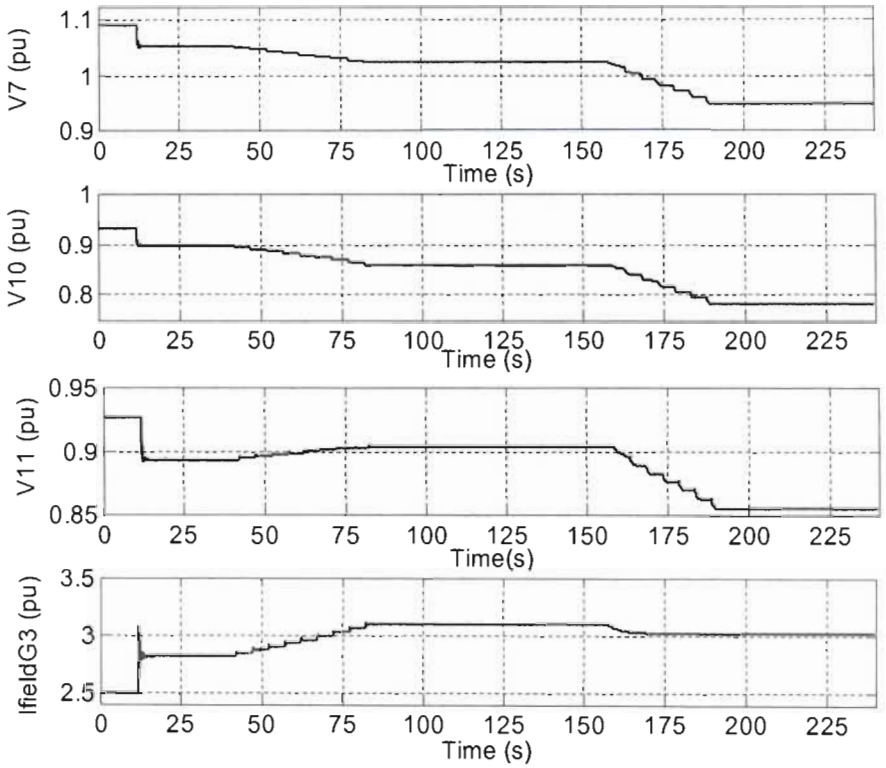

Fig. 4.7(a) Load level 2: Bus voltage magnitudes and field current of generator G3.

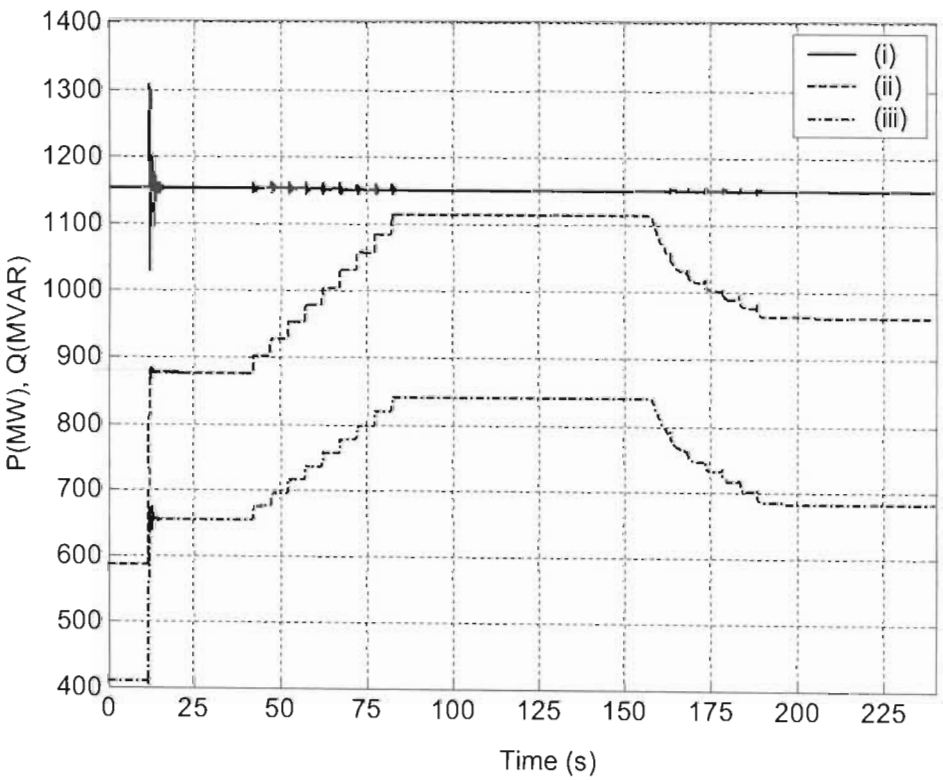

Fig. 4.7(b) Load level 1: (i) PGen3 (ii) QGen3 and (iii) QBus7.

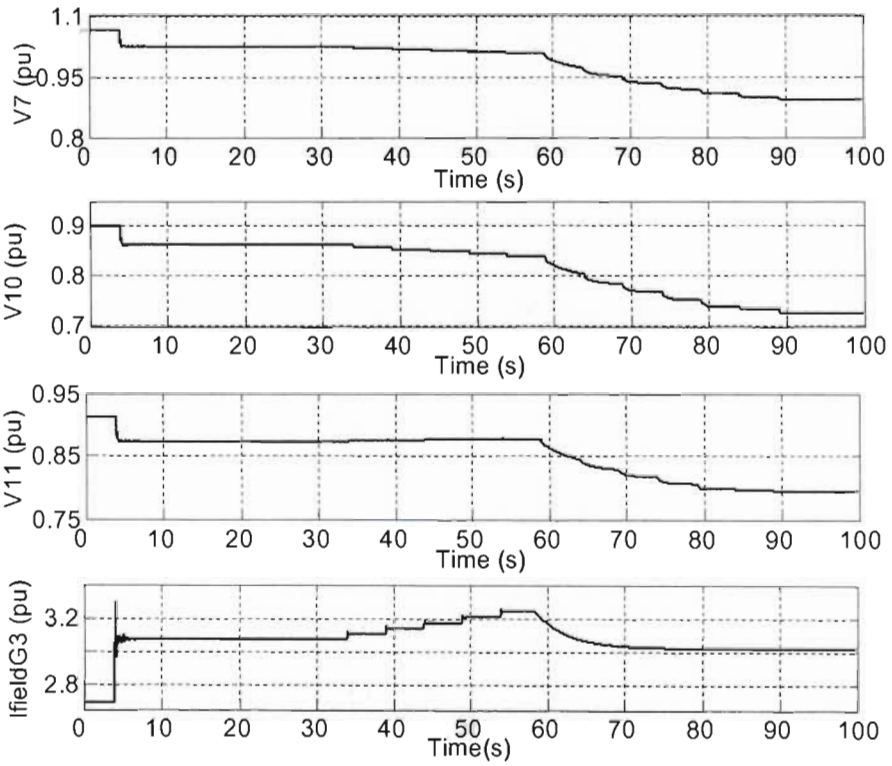

Fig. 4.8(a) Load level 3: Bus voltage magnitudes and field current of generator G3.

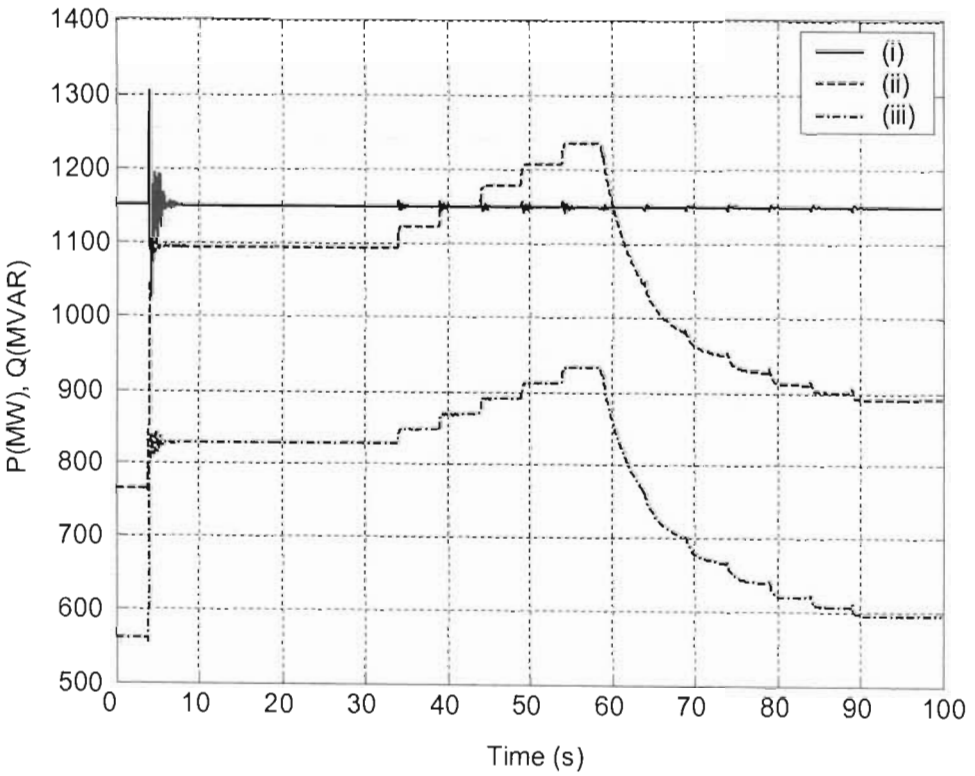

Fig. 4.8(b) Load level 3: (i) PGen3 (ii) QGen3 and (iii) QBus7.

The loss of the line also causes the reactive power output of generator G3 to increase while its active power output stays almost constant. The increase in the reactive power output of generator G3 is due to the increased reactive power demand of the transmission system after losing one branch between bus 6 and bus 7. The system voltages remain stable at values lower than the pre-disturbance values until the OLTC begins to operate. The OLTC starts to operate by tapping up after 30 seconds, and continues to tap up thereafter at 5 second intervals. Once the OLTC starts to operate, voltage at bus 11 is raised up to close to its reference value, and load power increases with each tap up movement of the OLTC. The restoration of load voltage and power increases reactive power demand on the generators, and leads to further increase of the field current of generator G3. The field current of generator G3, however, does not exceed the field current limit setting on the overexcitation limiter. The OLTC restores voltage at bus 11 to close to its reference value at about time t = 50 seconds, and thereafter no tap movements of the OLTC happen.

For the case of load level 2, the initial disturbance causes the system voltages to drop and the field current of generator G3 to increase. The initial increase in the field current of generator G3 at load level 2 is higher than in the case of load level 1 due to the heavier loading at load level 2. Once again the OLTC operates to restore load voltage after an initial delay of 30 seconds and continues to tap up thereafter at 5 second intervals. Initially tap up action of the OLTC results in the load voltage increasing toward the reference value, indicating that the system is voltage stable. The restoration of load voltage and power increases the reactive demand on the generators, and leads to further increase of the field current of generator G3. The load voltage is brought to close to its reference value after about 83 seconds. However, the field current of generator G3 is now above the low set limit but below the high set limit of the overexcitation limiter. The overexcitation limiter begins to limit the field current of generator G3 at about time t = 160 seconds. The limiting action of the overexcitation limiter results in the terminal voltage of generator G3 reducing, and therefore system voltages in the transmission, sub-transmission and distribution systems also reduce. The OLTC again attempts to restore the load voltage through tap up movements. Tap up movements of the OLTC result in decrease rather than increase of the load voltage, indicating that the system is now voltage unstable. The load voltage drops progressively until the OLTC reaches its limit at about time t = 190 seconds. Thereafter,

the system voltages are stable but are at unacceptably low values compared to their pre-disturbance values.

For the case of load level 3, the initial disturbance immediately causes the field current of generator G3 to increase above the field current limit, and system voltages drop as in the case of the previous load levels, but now the voltages are lower than for the cases of load level 1 and load level 2. The OLTC responds to restore load voltage after about 30 seconds from the time of the disturbance and continues tapping up every five seconds thereafter. Initially tap up movements of the OLTC result in the load voltage increasing toward its reference value, and the system is voltage stable. However, the overexcitation limiter starts to limit the field current of generator G3 after 58 seconds. The field current limiting takes place earlier for the case of load level 3 because of higher system loading than in the case of the previous load levels. At load level 3 the reactive power demand is higher than at load level 2 and load level 1, and hence the field current of generator G3 is higher, resulting in the field current limiter acting after a shorter time because of its inverse time characteristic. Limiting of the field current of generator G3 causes a reduction of the generator G3 terminal voltage, and consequently, voltages in the transmission, sub-transmission and distribution systems are reduced. The attempts of the OLTC to restore voltage at bus 11 result in further decrease rather than increase of the voltage at that bus, indicating that the system is now voltage unstable. The voltage at bus 11 drops progressively until the OLTC reaches its maximum limit at about time t = 90 seconds.

4.4 Conclusion

This chapter has presented the development of real-time models of two benchmark systems for voltage stability analysis. Custom real-time models of power system components developed for use on the RTDS as part of the work of this thesis and generalized components from the RSCAD software suite have been used to develop the benchmark systems. The chapter has presented the development of a real-time model of a small benchmark system for voltage stability studies on the RTDS. The simulation results of this system presented in this chapter are in agreement with the documented results of this system presented in reference [1]. The chapter has also presented the development of an 11-bus benchmark system for voltage stability studies on the RTDS. Simulation results for

the 11-bus benchmark system obtained on the RTDS are in close agreement with the simulation results for this benchmark system obtained with the Extended Transient/Midterm Stability Program (ETMSP), as presented in [2,6]. The simulations demonstrate the ability of the real-time digital simulator to conduct time domain voltage stability studies over the time frame that voltage stability problems and voltage collapse take place.

Part of the objectives of the work presented in this thesis is to assess the use of the real time digital simulator for testing methods of voltage stability control. The next chapter therefore, considers the application of three methods of voltage stability control for the 11-bus benchmark system developed in this chapter.

CHAPTER FIVE

COUNTERMEASURES AGAINST VOLTAGE INSTABILITY

5.1 Introduction

The previous chapter presented the development of real-time models for two benchmark systems for voltage stability studies on the RTDS. In that chapter, the known characteristics of the benchmark systems were verified using the real-time models developed for the RTDS. The real-time simulation results of the benchmark systems were seen to be in close agreement with the documented results of the two systems previously obtained by others using other simulation programs.

In this chapter three simple methods of voltage stability enhancement are investigated. Each of the three methods under investigation are applied to the 11-bus benchmark system described in chapter four. The three methods of voltage stability enhancement that are considered in this chapter are use of switched shunt capacitor compensation, synchronous condenser compensation and static var compensation. The investigations compare the effectiveness of each of the three methods in preventing voltage instability in the 11-bus benchmark system at various load levels.

5.2 Voltage control by switched shunt capacitor compensation

The behaviour of the 11-bus benchmark system following loss of a transmission line at three load levels was simulated and results presented in chapter four. The known characteristics of this system at each of the three load levels were successfully obtained with the real-time simulator. At load level 1, which is the lowest load level, the system voltages were stable after the disturbance, although two tap movements of the OLTC transformer were required to bring the voltage at bus 11 close to the voltage reference value. For the case of load level 2, the system was initially voltage stable and tap up movements of the OLTC transformer at bus 11 brought the voltage at that bus close to the voltage reference value. However, restoration of voltage at bus 11 caused an increase in

reactive power demand, and hence an increase in the field current of generator G3. When the overexcitation limiter of generator G3 operated to limit the field current after about 160 seconds, the system became unstable, with subsequent tap up movements of the OLTC at bus 11 resulting in a progressive decrease rather than increase of the voltage at that bus. For the case of load level 3, voltage instability and voltage collapse occurred much earlier than in the case of load level 2 as the field current limiter of generator G3 operated after only 58 seconds owing to the higher initial level of the generator field current at load level 3.

In the unstable cases of the benchmark system the voltage instability was caused by an inability of generator G3 to supply the additional reactive power demand following the loss of the transmission line. Therefore, in order to determine the amount of additional reactive power support required in the system to prevent voltage collapse, a study was carried out to determine the amount of additional reactive power needed in order to maintain the reactive power output of generator G3 close to its pre-disturbance value at each of the three different load levels considered in chapter four. The procedure involved calculating the increase in the reactive power output of generator G3 after the loss of the line but before any operation of the OLTC. The amount of additional reactive power support needed was found to be 275MVAr for load level 1; 292MVAr for load level 2 and; 330MVAr for load level 3.

Switched shunt capacitor banks rated to provide 275MVAr, 292MVAr and 330MVAr at nominal voltage were included in the 11-bus benchmark system model for the case of load level 1, load level 2 and load level 3 respectively. A simple control circuit was implemented to switch in the capacitor bank when the voltage at bus 7 dropped below a minimum threshold. Three different locations for the shunt capacitor were investigated at each load level: bus 6, bus 7 and bus 9. Figs. 5.1 to 5.3 show real-time simulation results of the 11-bus benchmark system with a 275MVAr switched shunt capacitor placed first at bus 6, then at bus 7 and finally at bus 9 for the case of load level 1. Similarly, the results after placing a 292MVAr shunt capacitor at bus 6, bus 7 and bus 9 for the case of load level 2 are shown in Figs. 5.4 to 5.6, while the results after placing a shunt capacitor rated 330MVAr at bus 6, bus 7 and bus 9 for the case of load level 3 are shown in Figs. 5.7 to 5.9. The effect of using a 292MVAr shunt capacitor at load level 3 was also investigated and the results are shown in Fig. 5.10. Each figure shows time responses of the

transmission system voltage (bus 7), sub-transmission system voltage (bus 10), distribution system voltage (bus 11), and the field current of generator G3 (IfieldG3). The figures also show graphs of the active power output of generator G3 (PGen3), the reactive power output of generator G3 (QGen3) and the reactive power supplied at bus 7 from generator G3 (QBus7) (i.e. the reactive power after the step-up transformer T3).

At load level 1, the initial disturbance causes system voltages to drop. The voltage at bus 7 drops below the threshold value of 1.065 pu, and the shunt capacitor is switched in. The reactive power output of generator G3 increases but is still close to its pre-disturbance value, and as such the field current of generator G3 is below the low set limit of the overexcitation limiter, and the voltage at bus 11 is within the deadband of the OLTC voltage reference and no tap movements occur for all the three different locations of the switched shunt capacitor.

For the case of load level 2, the system response immediately after the loss of the line is similar to that at load level 1: the switched shunt capacitor rated 292MVAr stabilizes the system voltages when placed at the three different locations.

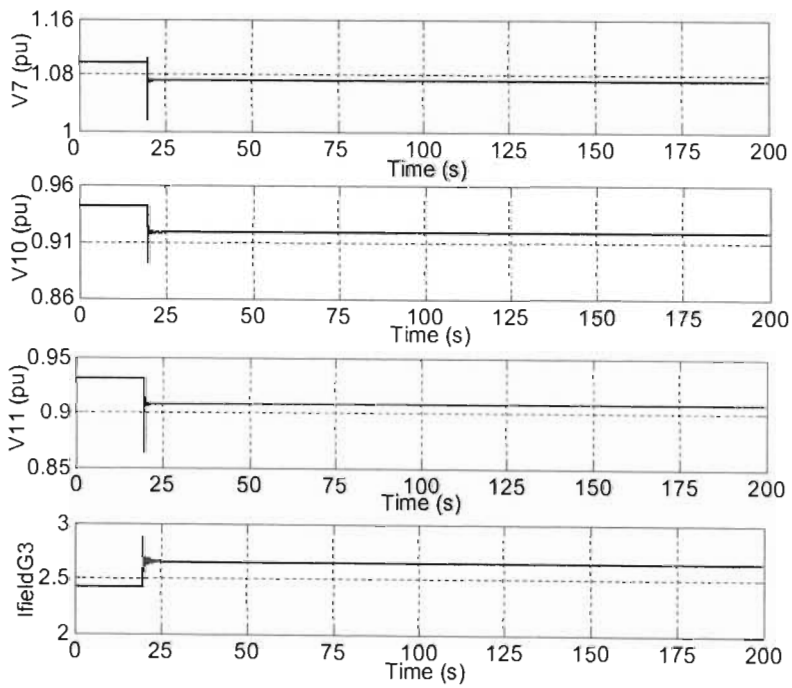

Fig. 5.1(a) Load level 1 with a switched shunt capacitor of 275MVAr at bus 6: Bus voltage magnitudes and field current of generator G3.

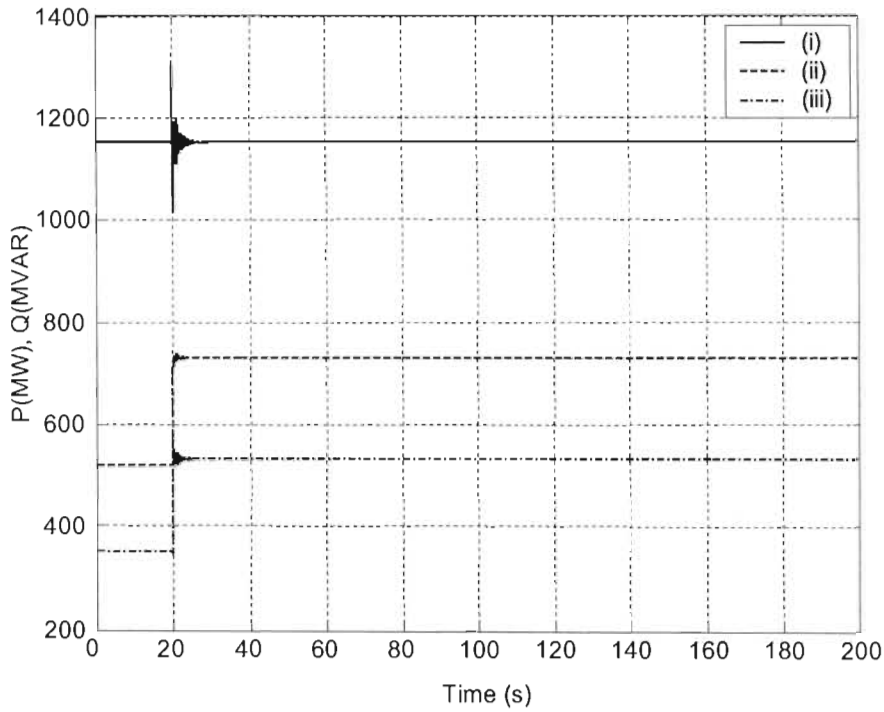

Fig. 5.1(b) Load level 1 with a switched shunt capacitor of 275MVAr at bus 6: (i) PGen3 (ii) QGen3 (iii) QBus7.

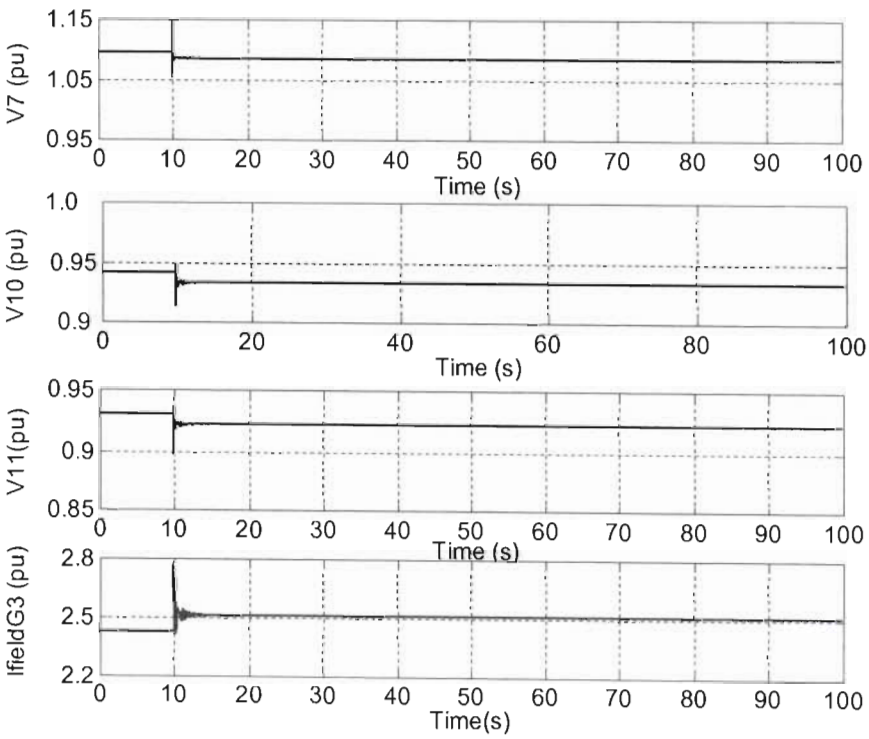

Fig. 5.2(a) Load level 1 with a switched shunt capacitor of 275MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

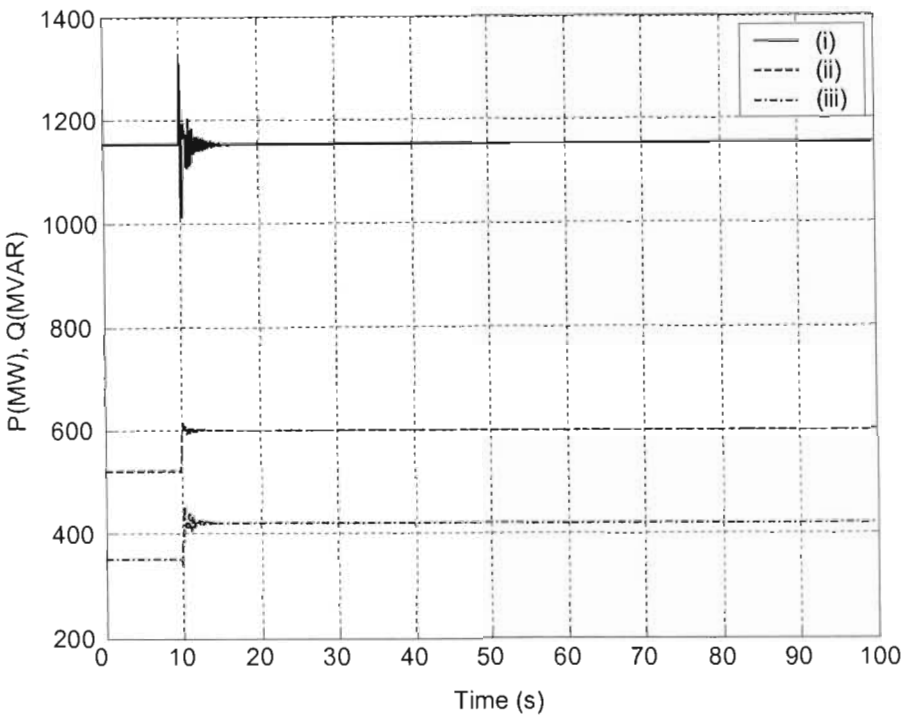

Fig. 5.2(b) Load level 1 with a switched shunt capacitor of 275MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7.

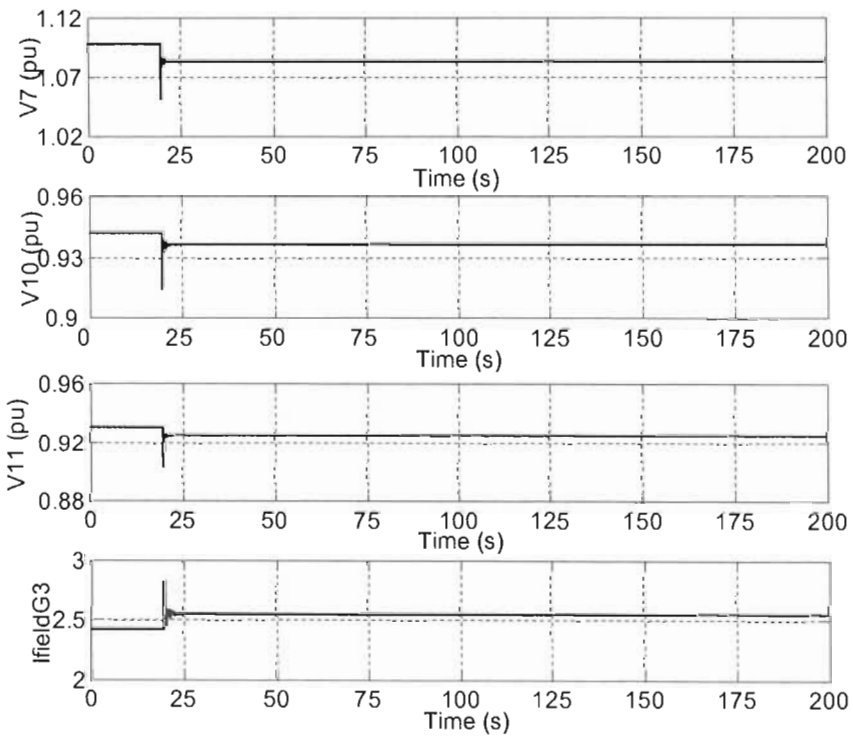

Fig. 5.3(a) Load level 1 with a switched shunt capacitor of 275MVAr at bus 9: Bus voltage magnitudes and field current of generator G3.

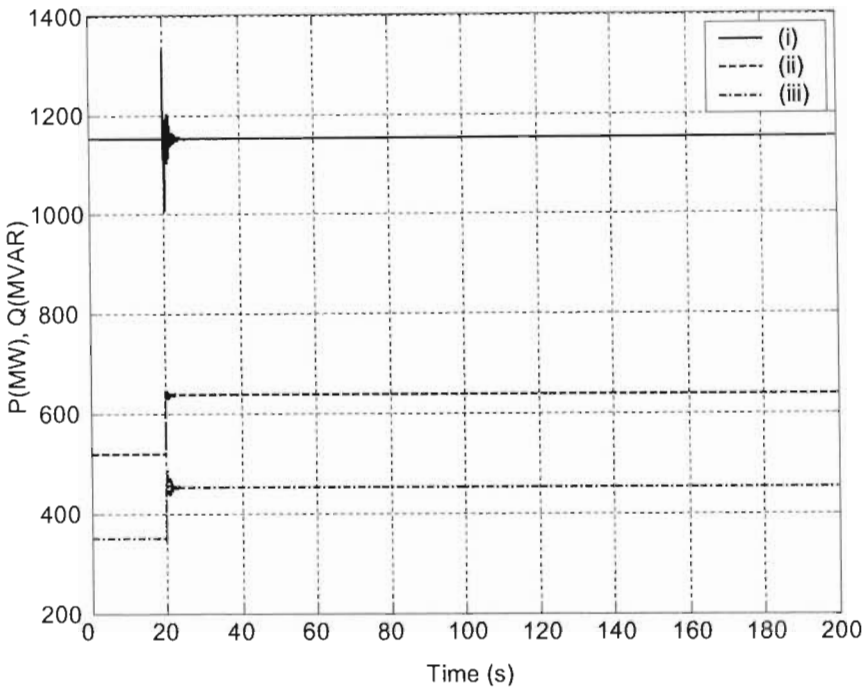

Fig. 5.3(b) Load level 1 with a switched shunt capacitor of 275MVAr at bus 9: (i) PGen3 (ii) QGen3 (iii) QBus7.

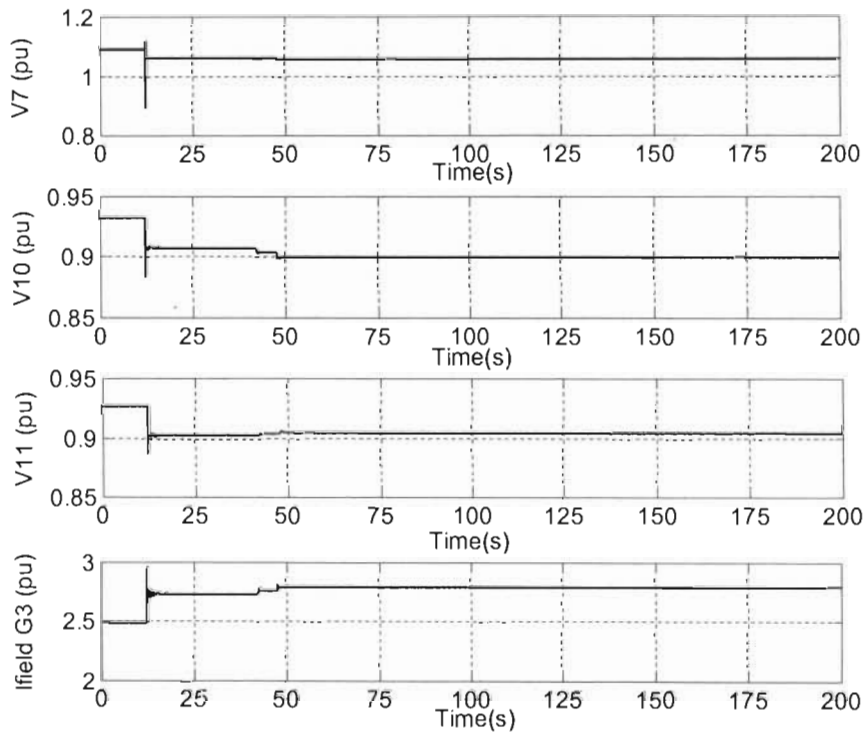

Fig. 5.4(a) Load level 2 with a switched shunt capacitor of 292MVAr at bus 6: Bus voltage magnitudes and field current of generator G3.

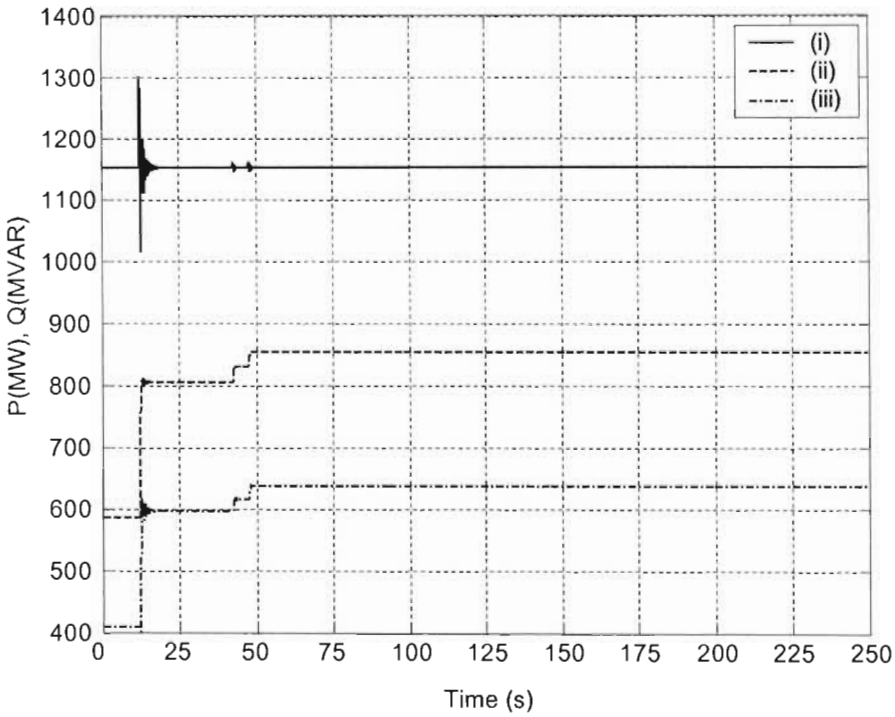

Fig. 5.4(b) Load level 2 with a switched shunt capacitor of 292MVAr at bus 6: (i) PGen3 (ii) QGen3 (iii) QBus7.

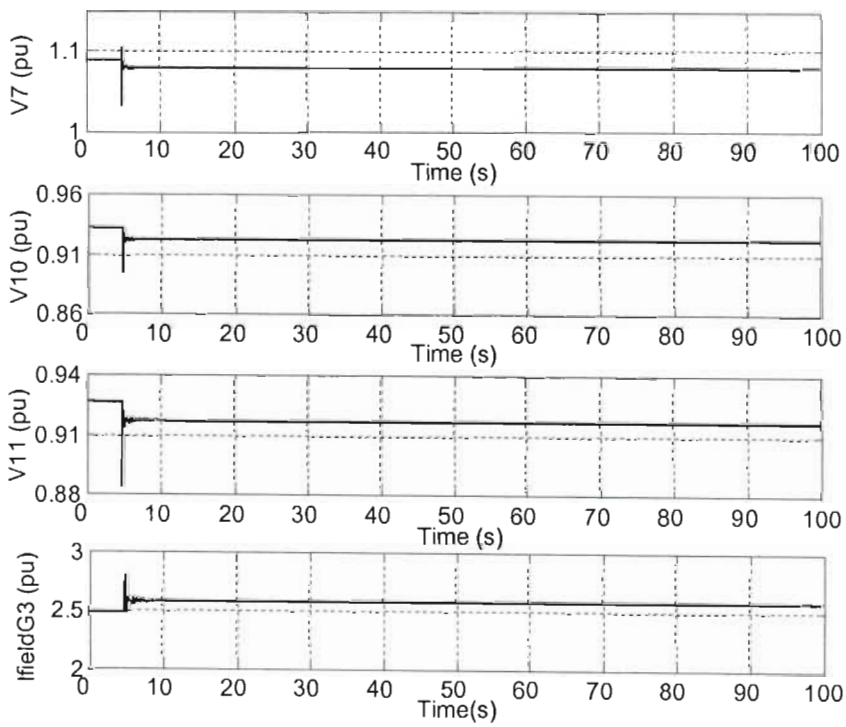

Fig. 5.5(a) Load level 2 with a switched shunt capacitor of 292MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

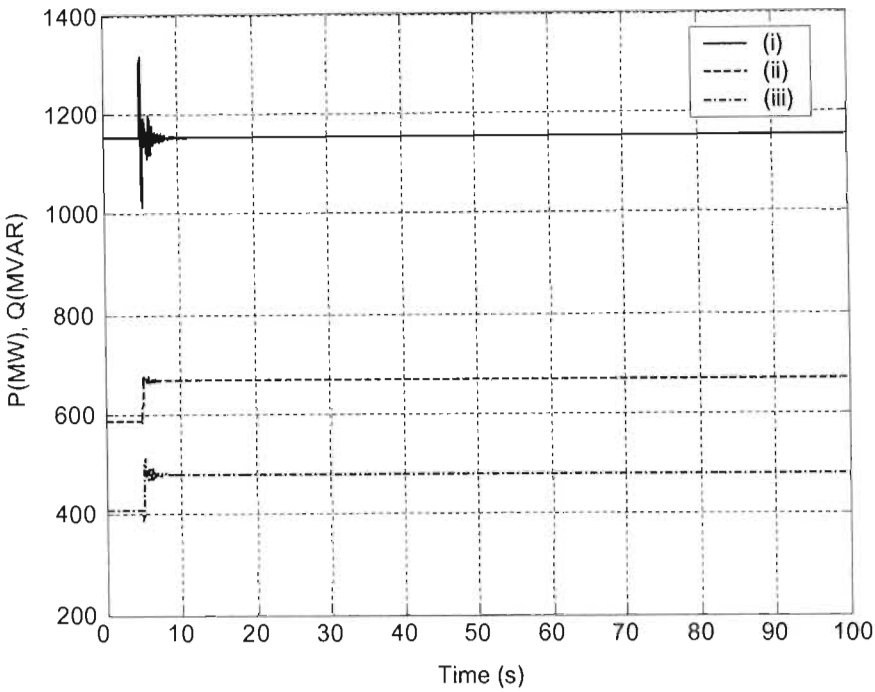

Fig. 5.5(b) Load level 2 with a switched shunt capacitor of 292MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7.

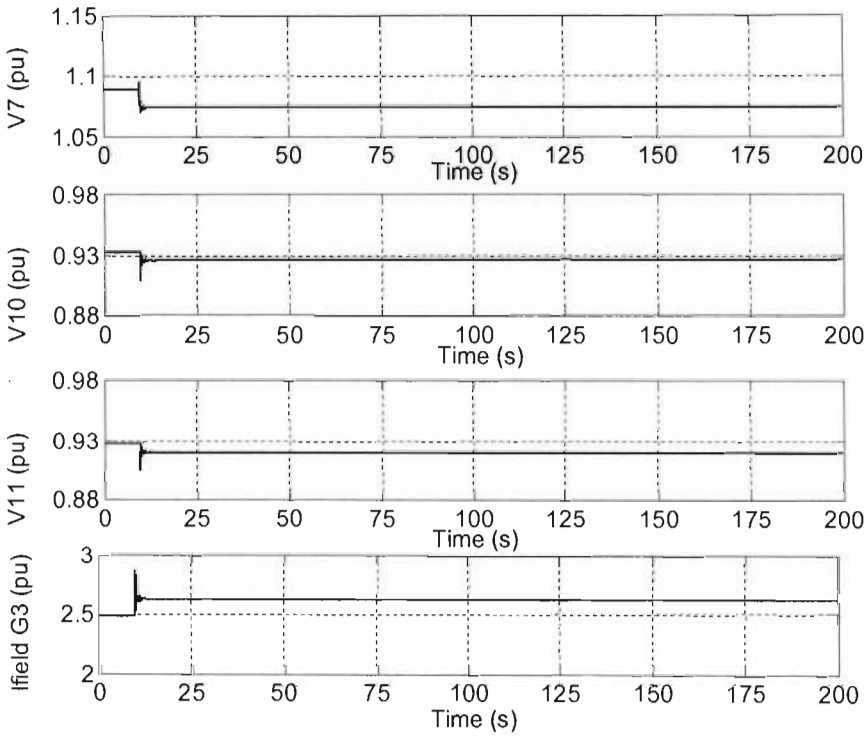

Fig. 5.6(a) Load level 2 with a switched shunt capacitor of 292MVAr at bus 9: Bus voltage magnitudes and field current of generator G3.

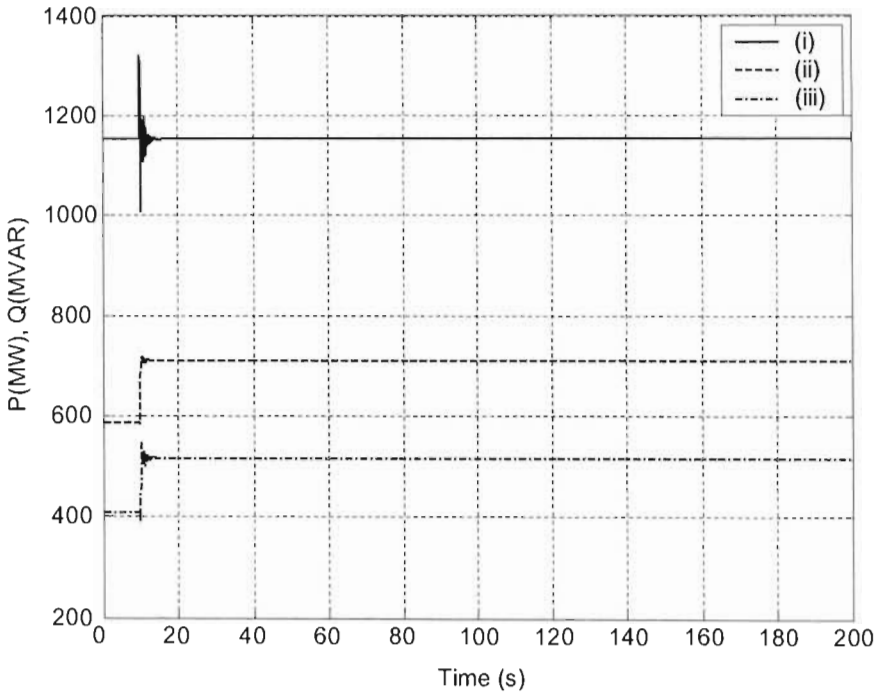

Fig. 5.6(b) Load level 2 with a switched shunt capacitor of 292MVAr at bus 9: (i) PGen3 (ii) QGen3 (iii) QBus7.

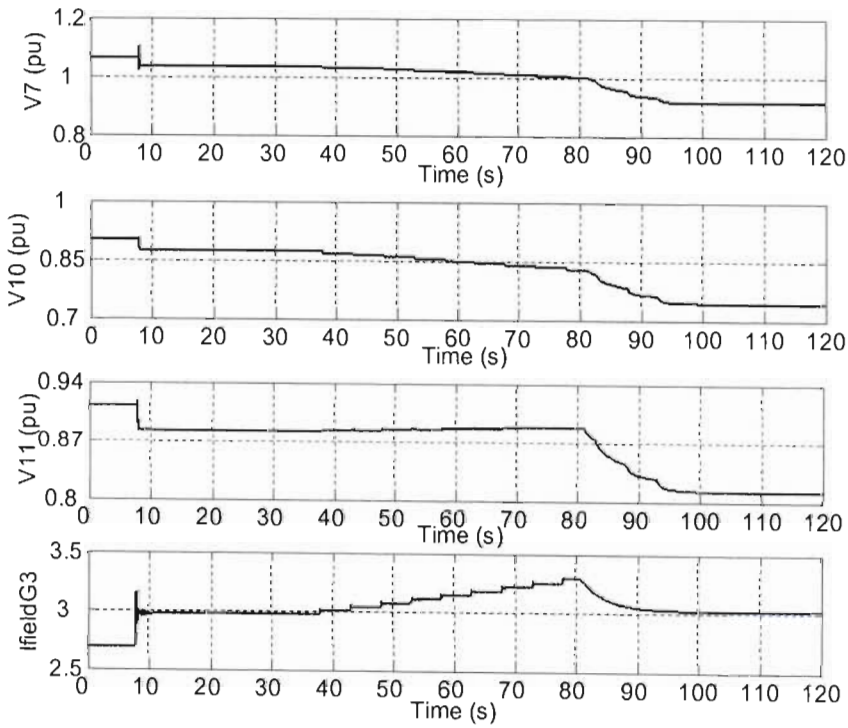

Fig. 5.7(a) Load level 3 with a switched shunt capacitor of 330MVAr at bus 6: Bus voltage magnitudes and field current of generator G3.

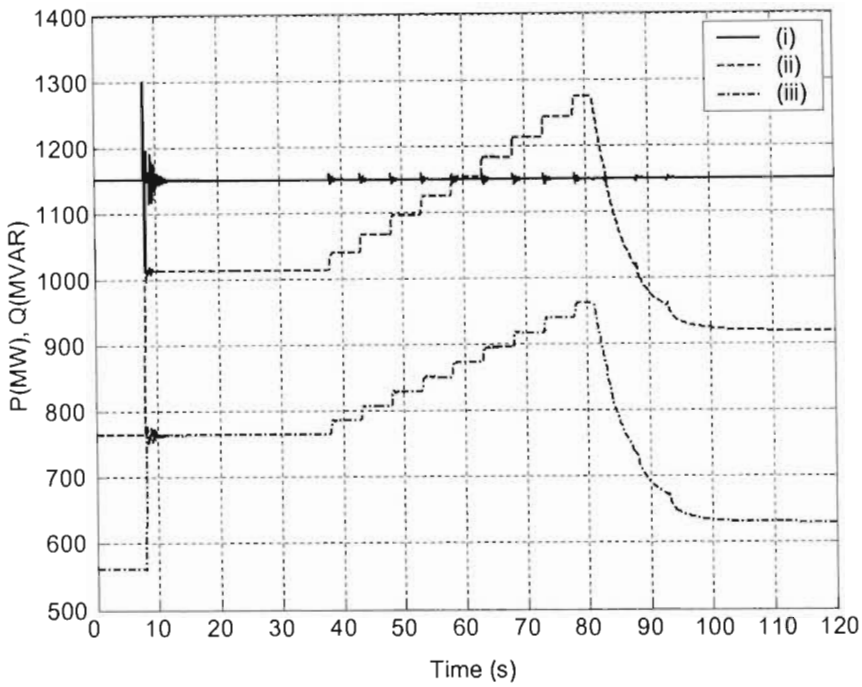

Fig. 5.7(b) Load level 3 with a switched shunt capacitor of 330MVAr at bus 6: (i) PGen3 (ii) QGen3 (iii) QBus7.

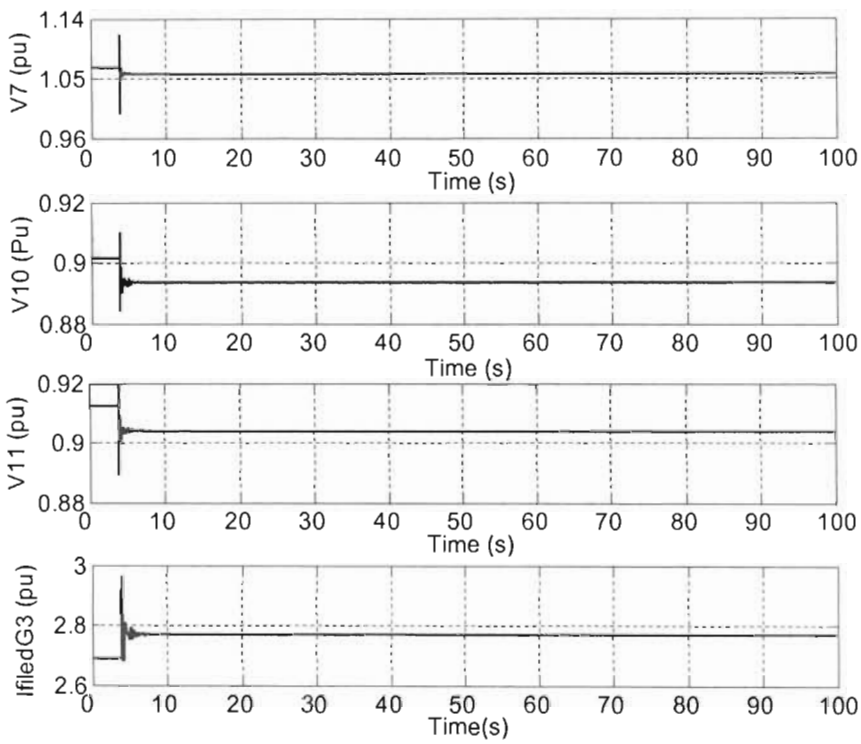

Fig. 5.8(a) Load level 3 with a switched shunt capacitor of 330MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

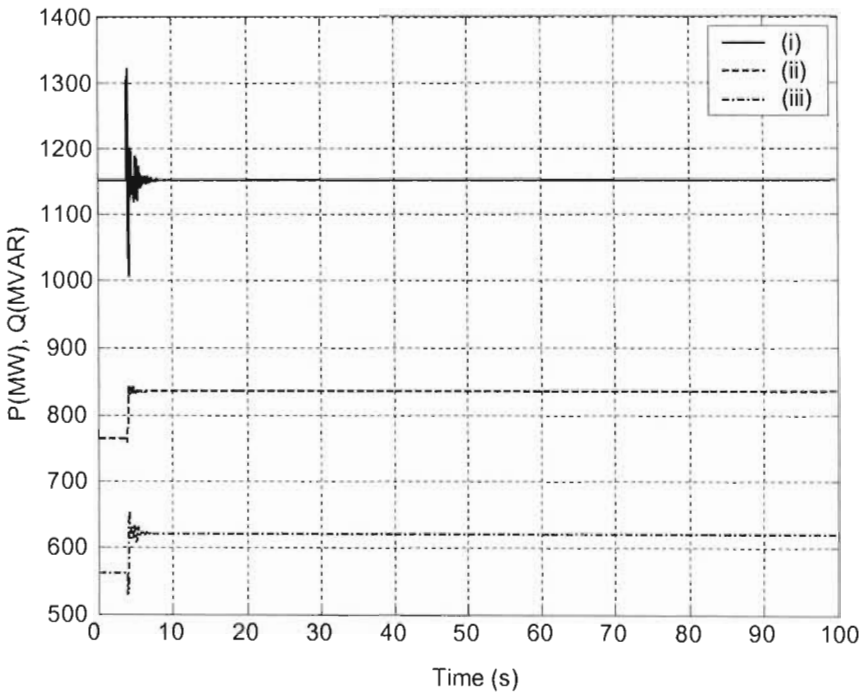

Fig. 5.8(b) Load level 3 with a switched shunt capacitor of 330MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7.

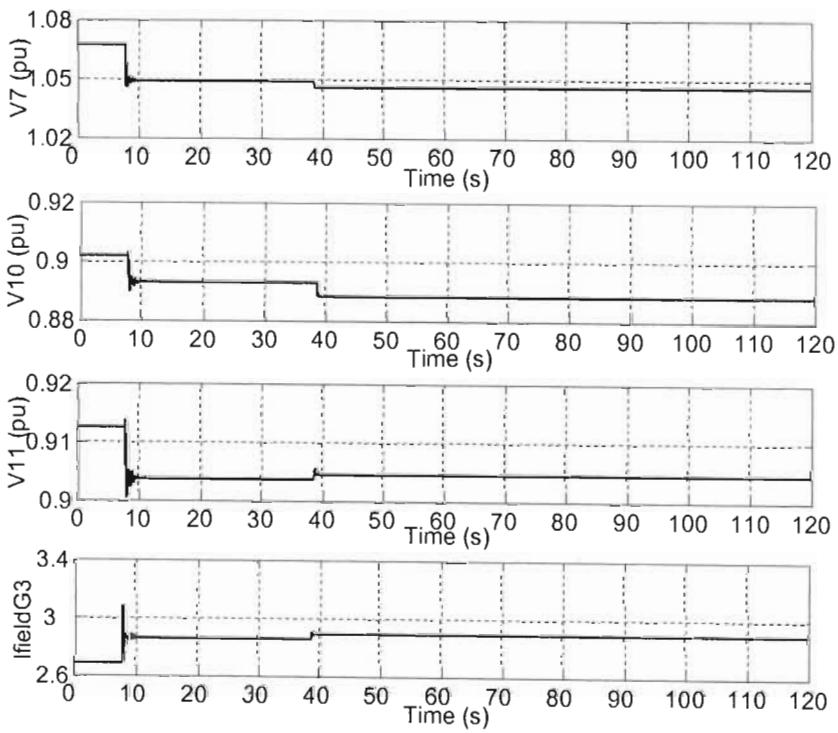

Fig. 5.9(a) Load level 3 with a switched shunt capacitor of 330MVAr at bus 9: Bus voltage magnitudes and field current of generator G3.

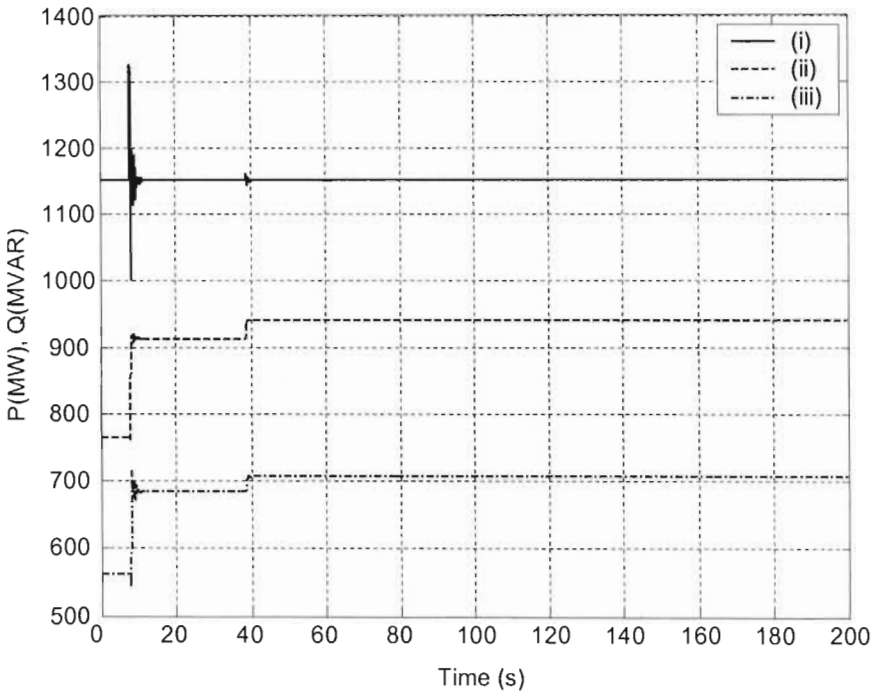

Fig. 5.9(b) Load level 3 with a switched shunt capacitor of 330MVAr at bus 9: (i) PGen3 (ii) QGen3 (iii) QBus7.

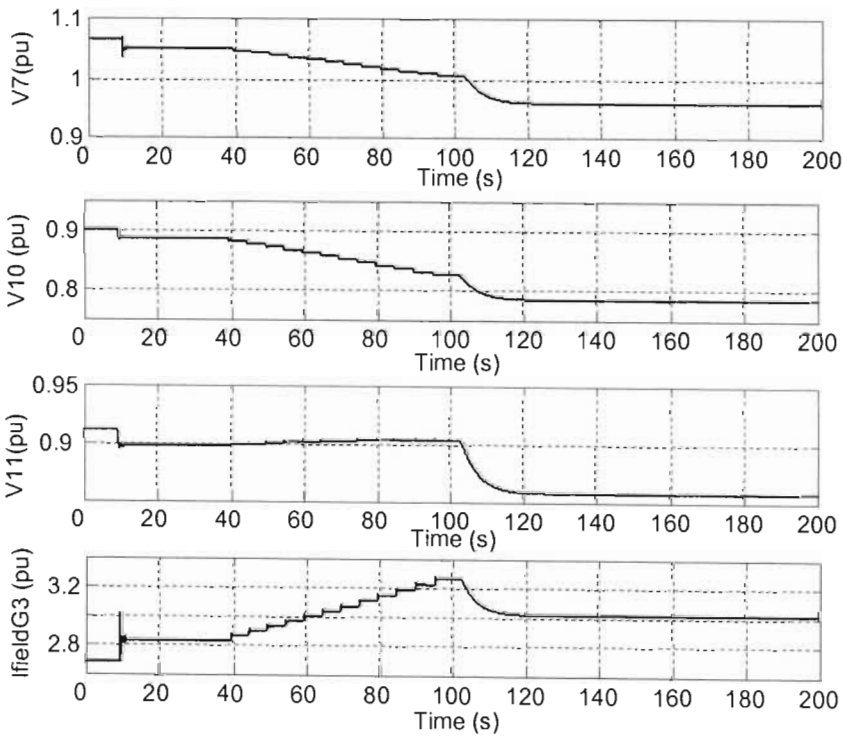

Fig. 5.10(a) Load level 3 with a switched shunt capacitor of 292MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

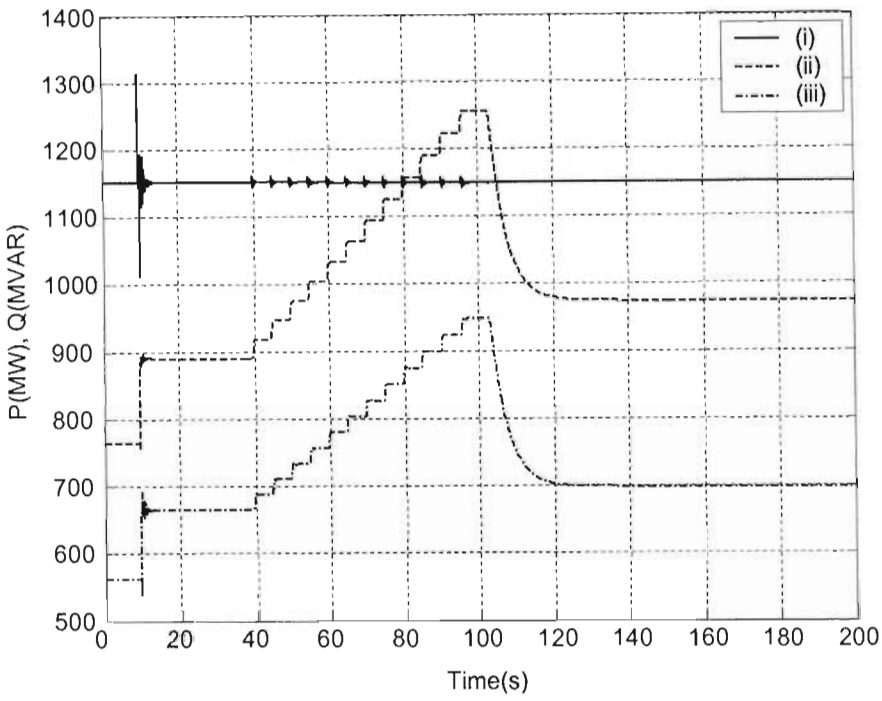

Fig. 5.10(b) Load level 3 with a switched shunt capacitor of 292MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7.

However, when the shunt capacitor is placed at bus 6, two tap up movements of the OLTC are required to bring the voltage at bus 11 within the deadband of its reference value. The differences in the effectiveness of the switched shunt capacitor in enhancing the voltage stability of the system when placed at the three different locations arise from the difficulty of transferring reactive power over long transmission lines. Reactive power cannot be easily transmitted over long transmission lines due to high reactive power losses resulting from the predominantly inductive nature of transmission lines. Bus 6 is further from the load where reactive power is needed than are bus 7 and bus 9 and thus, the reactive power support provided to the load by the switched shunt capacitor when it is placed at bus 6 is less than that when the switched shunt capacitor is placed at bus 7 or bus 9.

At load level 3, when the switched shunt capacitor of 330MVAr is placed at bus 6, system voltages are not stable after the loss of the transmission line. The system load is higher for the case of load level 3 than for the case of load level 1 and load level 2. The higher system loading coupled with the difficulty to transfer reactive power over long transmission lines, result in the reactive power support of the switched shunt capacitor not being able to meet

the additional reactive power demand after the disturbance. Hence, the reactive power output and field current of generator G3 are higher than at the two previous load levels, and the bus 11 voltage is outside of the deadband of the voltage reference of the OLTC. The OLTC operation to restore voltage at bus 11 toward its reference value results in further increase in reactive power demand and drives the field current of generator G3 above the low set limit of the overexcitation limiter. Voltage collapse ensues after about 80 seconds when the overexcitation limiter limits the field current of generator G3. The voltage at bus 11 declines with every tap up movement of the OLTC until the OLTC reaches its limit at time t = 100 seconds. By contrast when the same shunt capacitor is placed at bus 7, voltage stability is maintained after the disturbance. The voltage at bus 11 is within the deadband of the reference value, and the field current of generator G3 is below the low set limit of the overexcitation limiter. Similarly the system voltage stability is maintained when the 330 MVAr switched shunt capacitor is placed at bus 9. The switched shunt capacitor is more effective in providing reactive support when placed near to the load at bus 7 or bus 9 (where reactive power demand is)than when it is placed at bus 6.

Fig. 3.10 shows the effect of using the switched shunt capacitor rated 292MVAr to enhance the voltage stability of the 11-bus system for the case of load level 3. The figure shows that immediately after the loss of the line, voltages in the transmission, sub-transmission and distribution systems drop and, the reactive power output and field current of generator G3 increase. Immediately after the disturbance, the field current of generator G3 is below the low set limit of the overexcitation limiter. About 30 seconds after the disturbance the OLTC begins to tap up in order to restore the voltage at bus 11, and continues to tap up at 5 second intervals thereafter. The tapping up operation of the OLTC results in the increase in reactive power demand, and the field current of generator G3 increases with each tap up movement of the OLTC. Initially the tap up movements of the OLTC result in the voltage at bus 11 increasing, until after about 103 seconds when the overexcitation limiter limits the field current of generator G3. After the overexcitation limiter limits the field current of generator G3, further tap up movements of the OLTC result in the voltage at bus 11 decreasing with each tap up movement of the OLTC. These results show that the switched shunt capacitor rated to provide 292MVAr does not effectively enhance the voltage stability of the 11-bus benchmark system at load level 3.

5.3 Synchronous condenser compensation

Some of the advantages of using synchronous condensers to enhance voltage stability are that they can provide continuously adjustable reactive power that enables close control of system voltages, and that they can provide both leading and lagging reactive power to accomplish voltage support [25]. The effect of using a synchronous condenser to enhance voltage stability in the 11-bus benchmark system was investigated at the three load levels considered in chapter four. For the case of load level 1 a synchronous condenser rated 275MVAr was used, while for the case of load level 2 the synchronous condenser used was rated 292MVAr and for the case of load level 3 the synchronous condenser used was rated 330MVAr. The synchronous condenser controller used in this thesis is shown in Fig. 3.12. The controller is modelled to control the reactive power output of the synchronous condenser. The intention is to provide no reactive power to the system before the disturbance, and only after the disturbance is the reference value of the synchronous condenser reactive power output set to 1.0 pu. In the case of each of the three load levels, the synchronous condenser was placed at three different locations: bus 6, bus 7 and bus 9. Figs. 5.11 to 5.13 show real-time simulation results of the 11-bus benchmark system with a 275 MVAr synchronous condenser at bus 6, bus 7 and bus 9 for the case of load level 1. The simulation results after placing a 292MVAr synchronous condenser at bus 6, bus 7 and bus 9 for the case of load level 2 are shown in Figs. 5.14 to 5.16, while the results after placing a synchronous condenser rated 330MVAr at bus 6, bus 7 and bus 9 for the case of load level 3 are shown in Figs. 5.17 to 5.19. The figures show time responses of the transmission system voltage (bus 7), sub-transmission system voltage (bus 10), distribution system voltage (bus 11), and the field current of generator G3 (IfieldG3). The figures also show graphs of the active power output of generator G3 (PGen3), the reactive power output of generator G3 (QGen3) and the reactive power supplied at bus 7 from generator G3 (QBus7) (i.e. the reactive power after the step-up transformer T3) and the reactive power output of the synchronous condenser (QSyncCond).

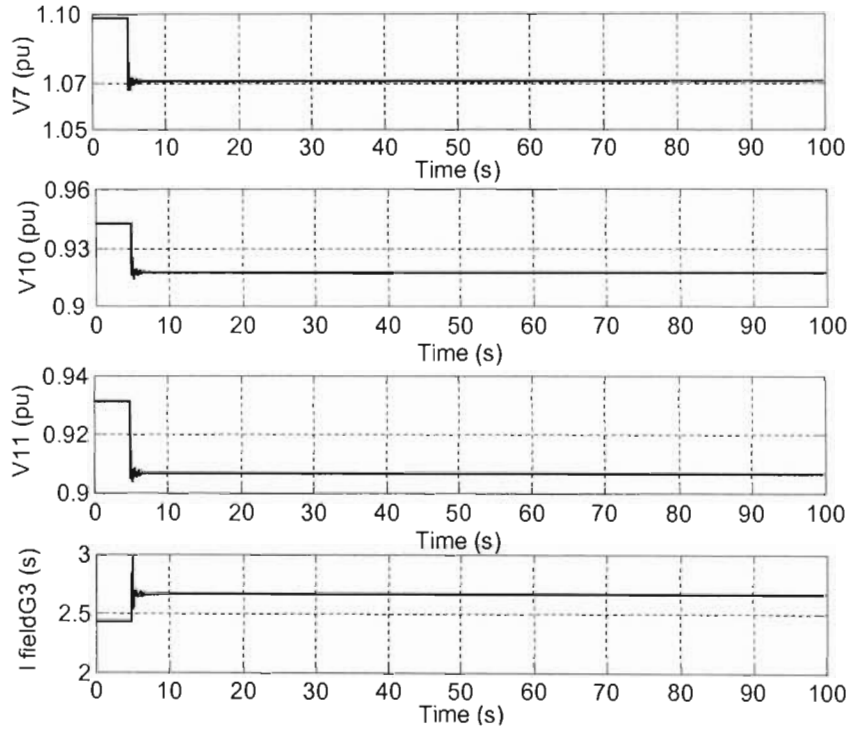

Fig. 5.11(a) Load level 1 with a synchronous condenser rated 275MVAr at bus 6: Bus voltage magnitudes and field current of generator G3.

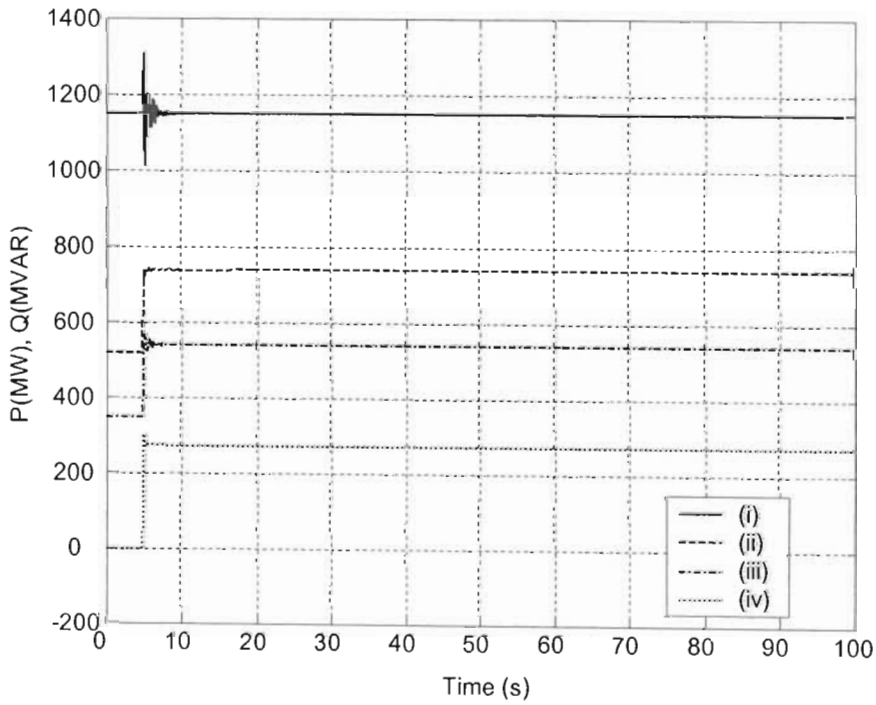

Fig. 5.11(b) Load level 1 with a synchronous condenser rated 275MVAr at bus 6: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

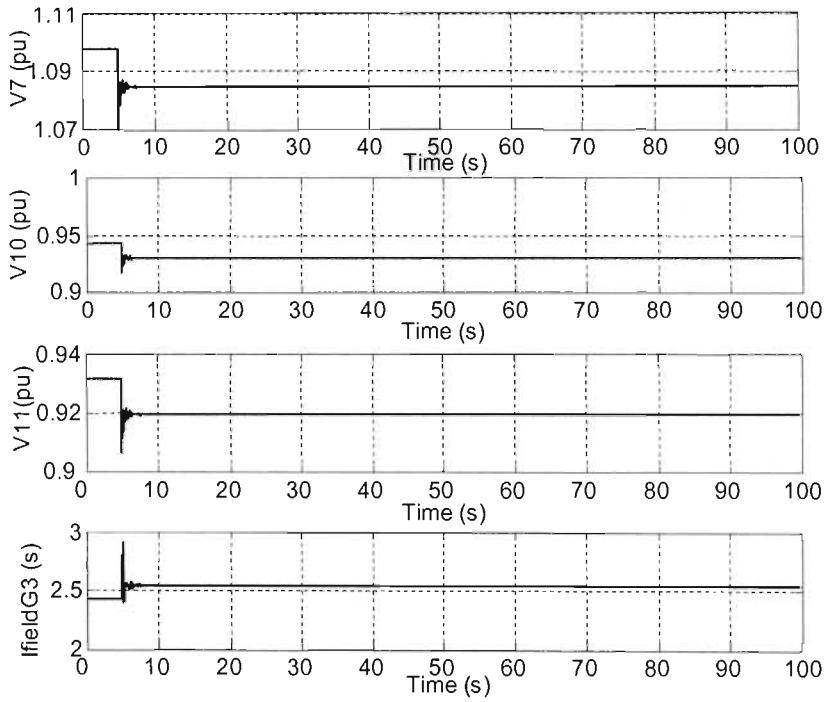

Fig. 5.12(a) Load level 1 with a synchronous condenser rated 275MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

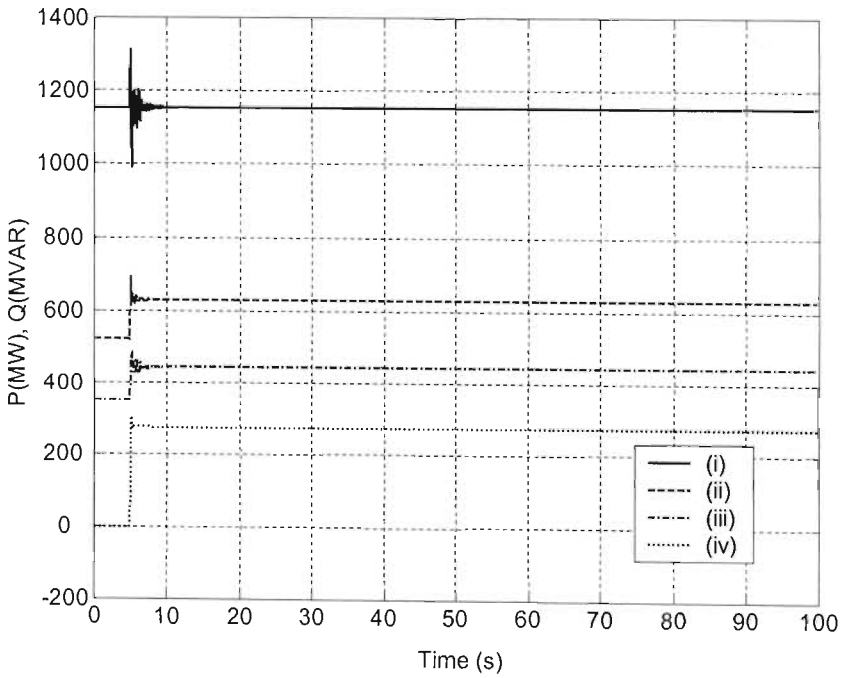

Fig. 5.12(b) Load level 1 with a synchronous condenser rated 275MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

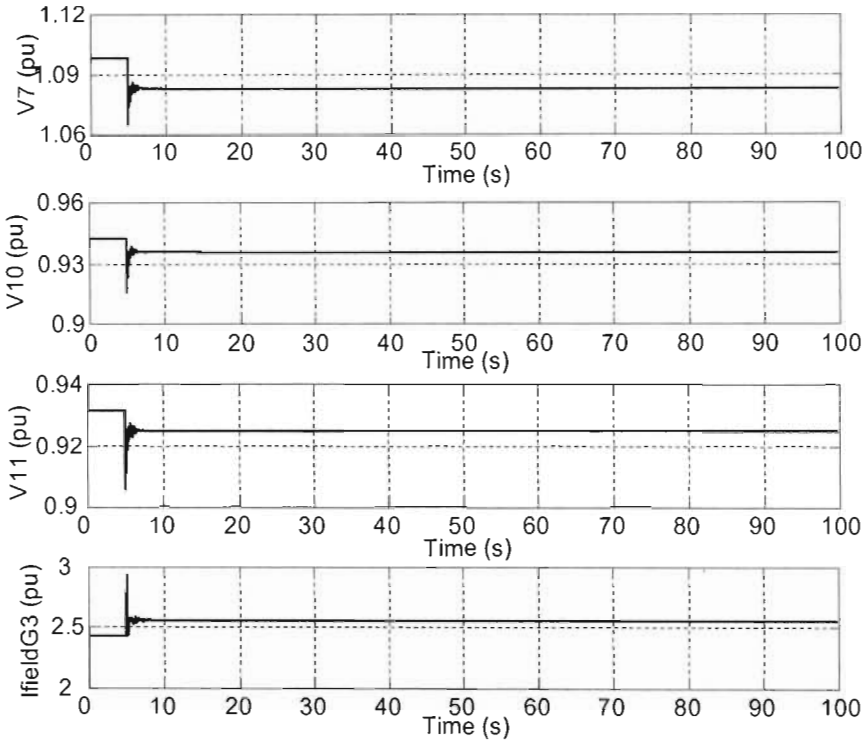

Fig. 5.13(a) Load level 1 with a synchronous condenser rated 275MVAr at bus 9: Bus voltage magnitudes and field current of generator G3.

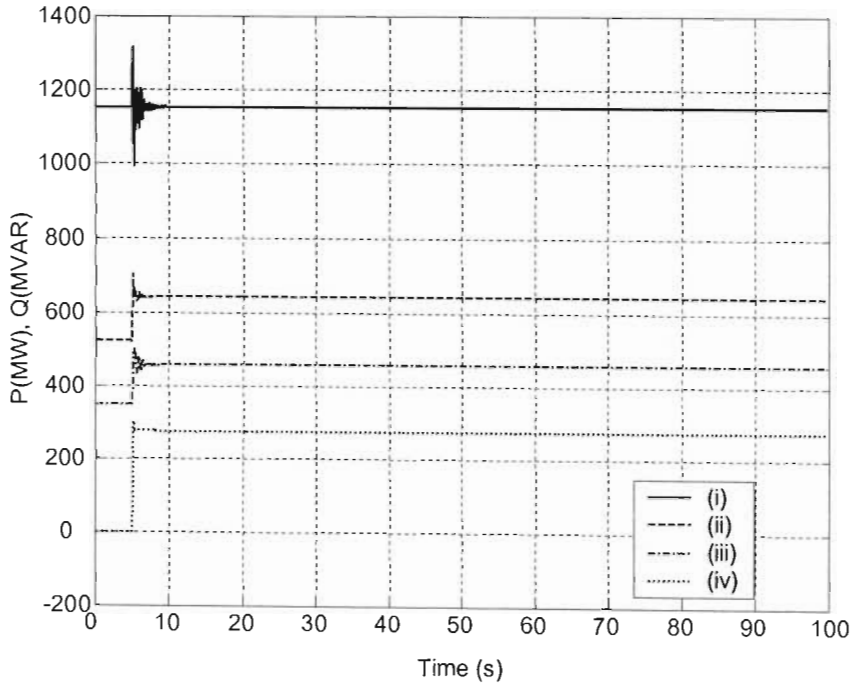

Fig. 5.13(b) Load level 1 with a synchronous condenser rated 275MVAr at bus 9: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

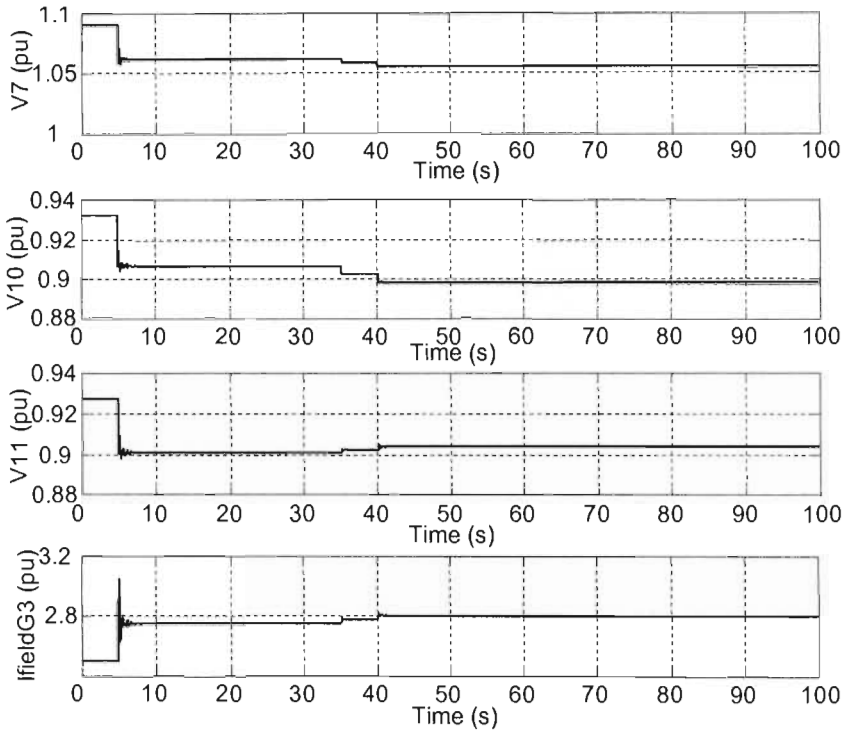

Fig. 5.14(a) Load level 2 with a synchronous condenser rated 292MVAr at bus 6: Bus voltage magnitudes and field current of generator G3.

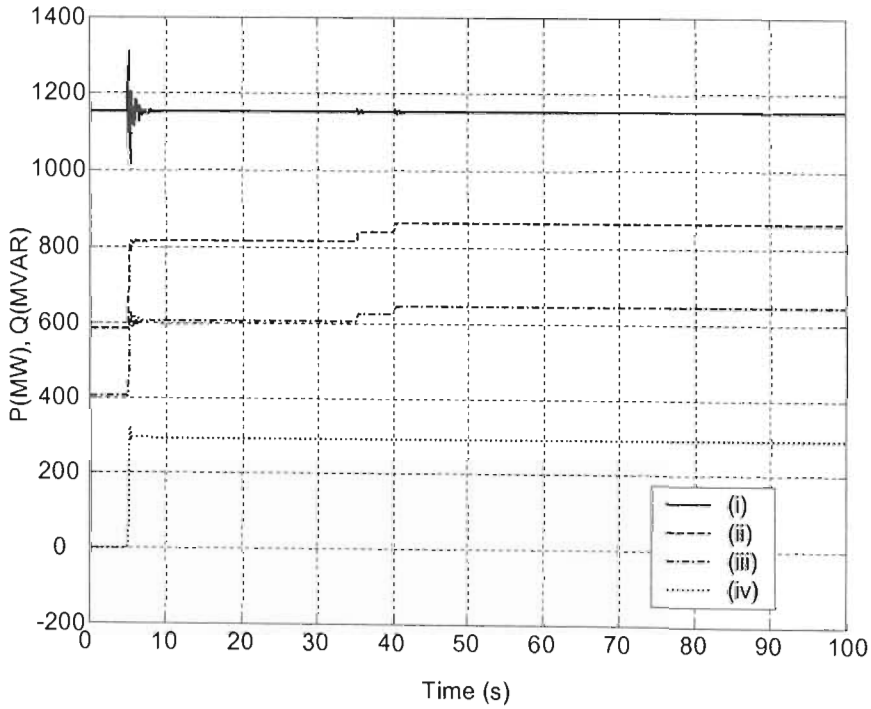

Fig. 5.14(b) Load level 2 with a synchronous condenser rated 292MVAr at bus 6: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

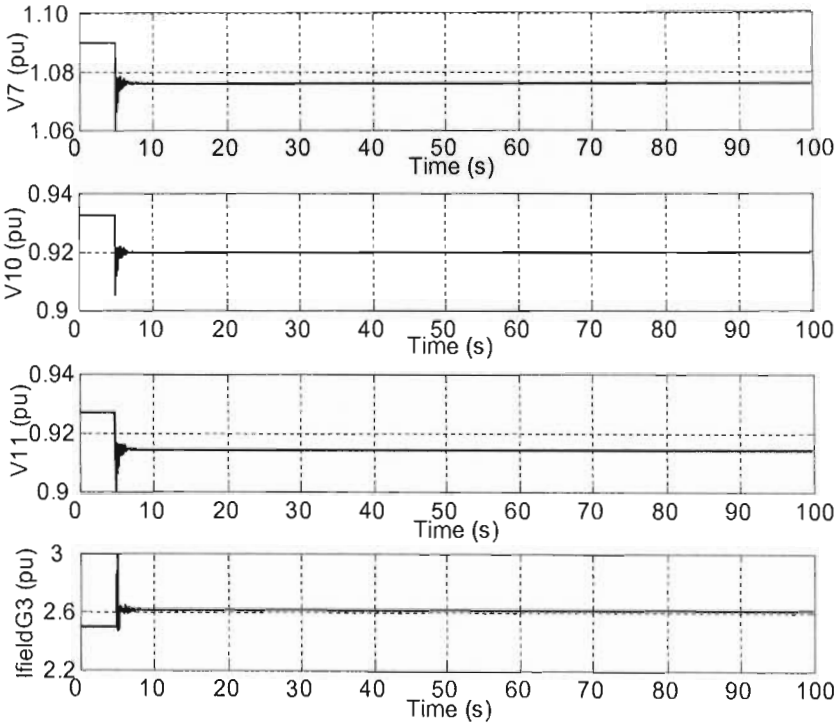

Fig. 5.15(a) Load level 2 with a synchronous condenser rated 292MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

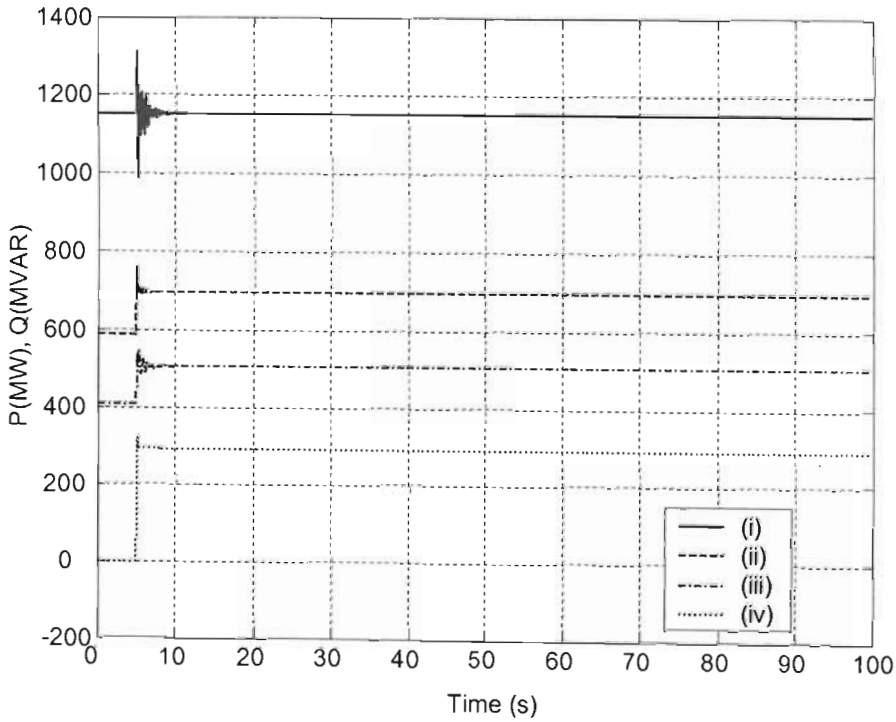

Fig. 5.15(b) Load level 2 with a synchronous condenser rated 292MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

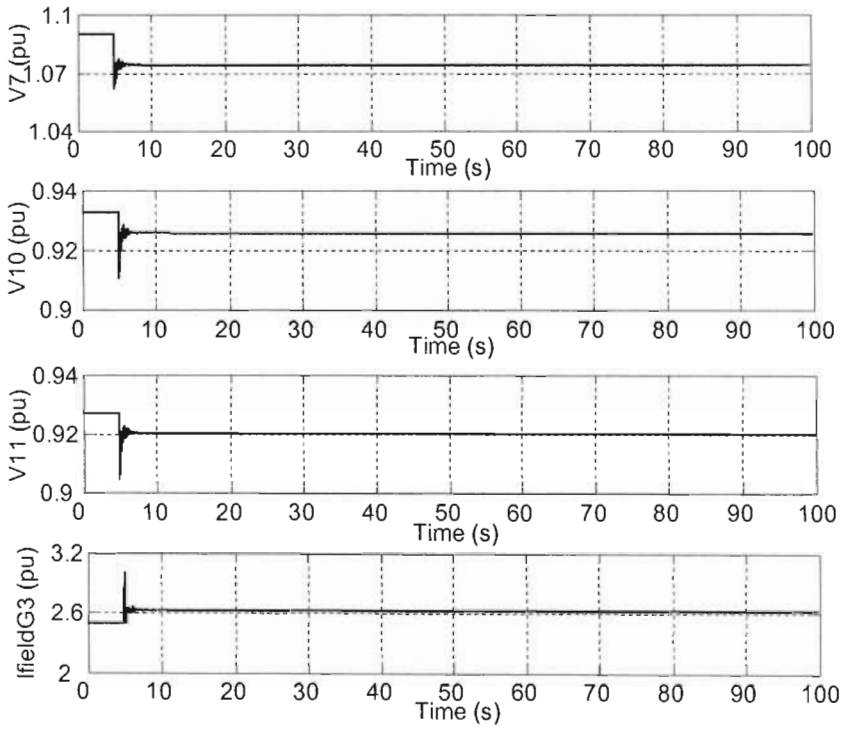

Fig. 5.16(a) Load level 2 with asynchronous condenser rated 292MVAr at bus 9: Bus voltage magnitudes and field current of generator G3.

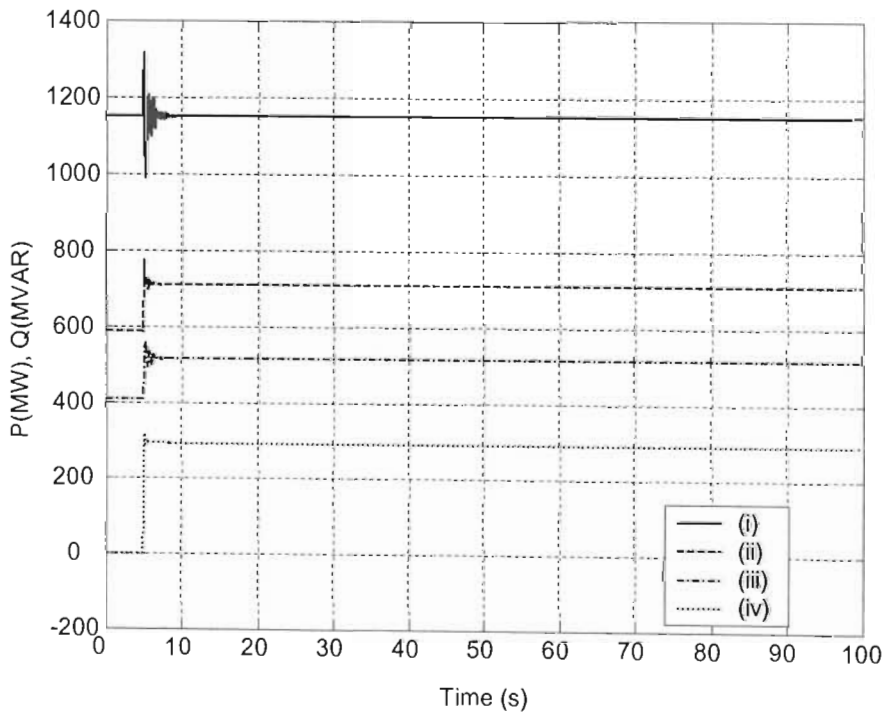

Fig. 5.16(b) Load level 2 with a synchronous condenser rated 292MVAr at bus 9: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

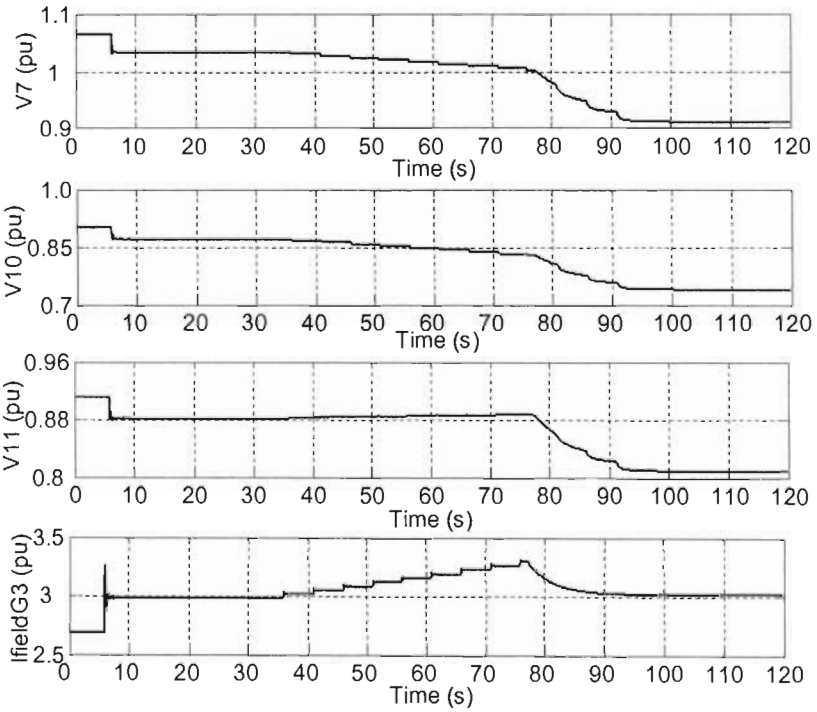

Fig. 5.17(a) Load level 3 with a synchronous condenser rated 330MVAr at bus 6: Bus voltage magnitudes and field current of generator G3.

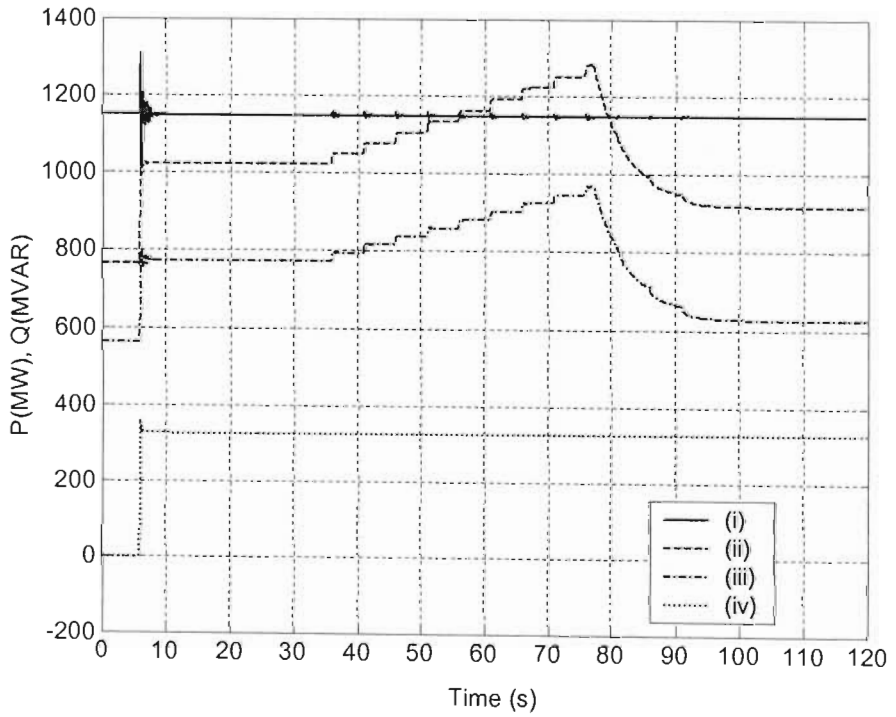

Fig. 5.17(b) Load level 3 with a synchronous condenser rated 330MVAr at bus 6: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

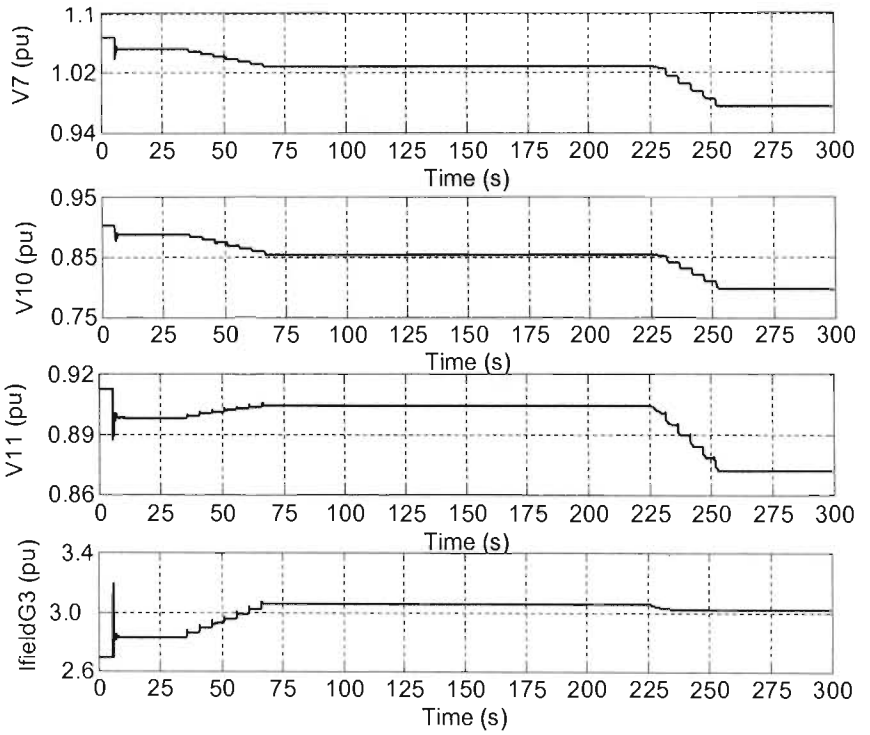

Fig. 5.18(a) Load level 3 with a synchronous condenser rated 330MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

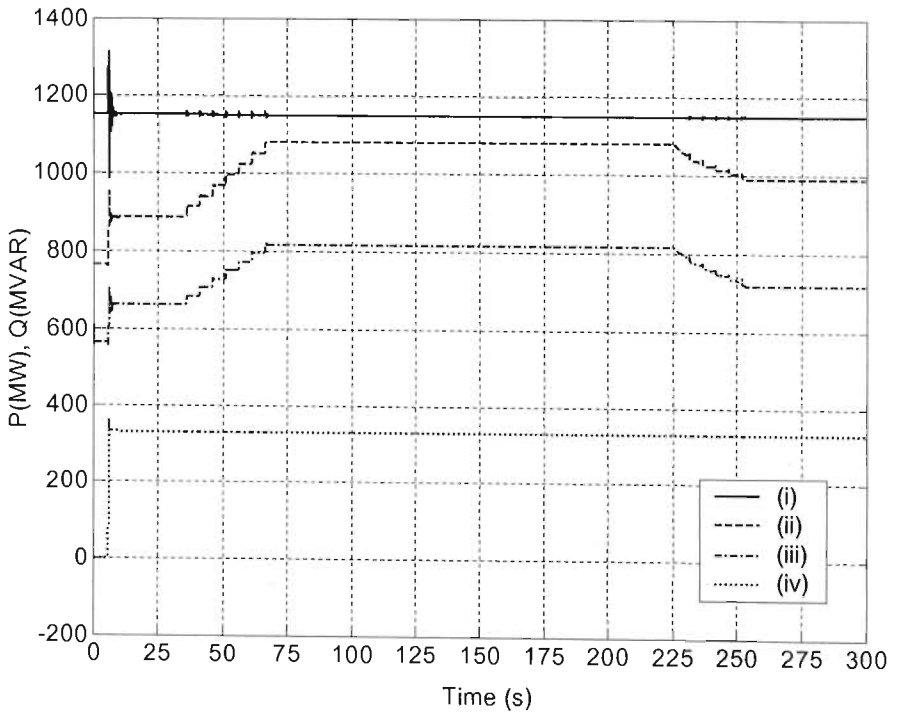

Fig. 5.18(b) Load level 3 with a synchronous condenser rated 330MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

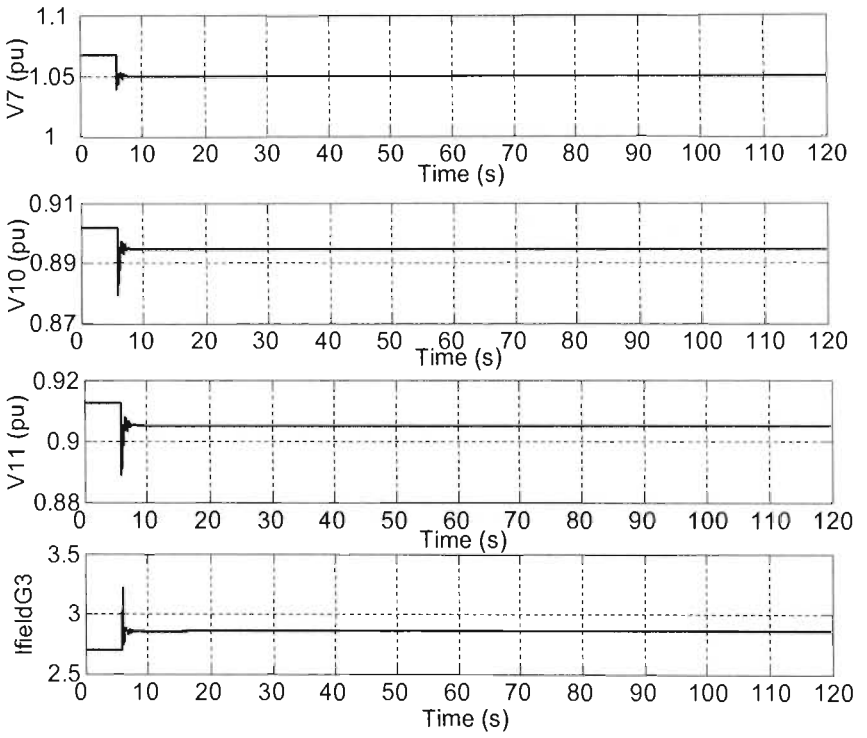

Fig. 5.19(a) Load level 3 with a synchronous condenser rated 330MVAr at bus 9: Bus voltage magnitudes and field current of generator G3.

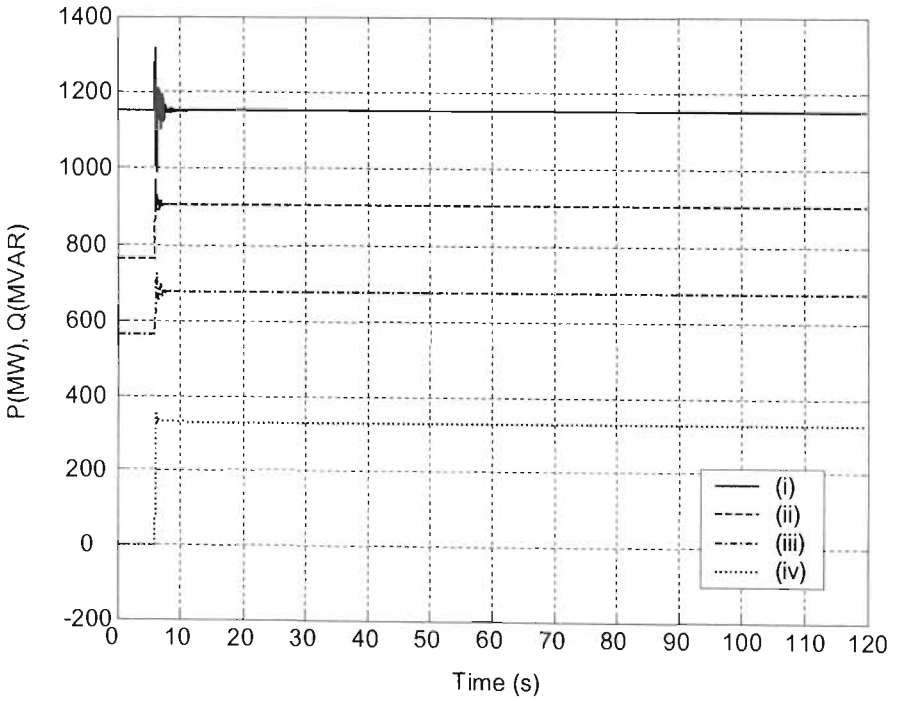

Fig. 5.19(b) Load level 3 with a synchronous condenser rated 330MVAr at bus 9: (i) PGen3 (ii) QGen3 (iii) QBus7 and (iv) QSyncCond.

At load level 1, the synchronous condenser enhances the response of the system voltages such that no OLTC tap up movements are required after the disturbance when it is placed at bus 7 and bus 9. However, two tap up movements of the OLTC are required to bring the voltage at bus 11 within the deadband of the voltage reference value when the synchronous condenser is placed at bus 6. The differences in the effectiveness of the synchronous condenser to enhance the voltage stability of the system when placed at the three different locations arise from the difficulty to transmit reactive power over long distances as discussed in section 5.2. Thus although the reactive power output of the synchronous condenser is constant irrespective of the bus at which it is connected, as can be seen from the results, its reactive power support to the load is less effective when it is placed at bus 6 than when it is placed at bus 7 or bus 9.

For the case of load level 2, two tap up movements of the OLTC transformer are required to bring the voltage at bus 11 within the deadband of its reference value when the synchronous condenser is placed at bus 6. When the synchronous condenser is placed at bus 7 or bus 9 at this load level, the system voltages remain within the required deadband without the necessity of the OLTC tapping up. The differences in the effectiveness of the synchronous condenser to enhance voltage stability when it is placed at the three different locations arise from the difficulty to transfer reactive power over long transmission lines discussed earlier in the case of load level 1. Therefore, when the synchronous condenser is placed at bus 6 the reactive power delivered to the load area is not adequate to effectively enhance the voltage stability of the system.

For the case of load level 3, voltage stability is maintained when the synchronous condenser is placed at bus 9, but is not maintained when the synchronous condenser is placed at bus 6 or bus 7. In each case of the three different locations of the synchronous condenser, the loss of the transmission line results in the voltages at the transmission, sub-transmission and distribution systems dropping, and the reactive power output and field current of generator G3 increasing. With the synchronous condenser placed at bus 6 the OLTC begins to operate about 30 seconds after the disturbance by tapping up in order to restore the voltage at bus 11 and continues to tap up thereafter at 5 second intervals. The OLTC tap up movements result in an increase of the reactive power demand and subsequently increase in the field current of generator G3. The overexcitation limiter limits

the field current of generator G3 at about time t = 78 seconds. Thereafter OLTC tap up movements result in the voltage at bus 11 decreasing instead of increasing, indicating that the system is now voltage unstable. When the synchronous condenser is placed at bus 7 the OLTC begins to operate about 30 seconds after the disturbance by tapping up in order to restore the voltage at bus 11 and continues to tap up thereafter at 5 second intervals. Initially, the tap up movements of the OLTC result in the voltage at bus 11 increasing and, about 70 seconds after the disturbance, the voltage at bus 11 is brought within the deadband of its reference value. However, the field current of generator G3 is now above the low set limit of the overexcitation limiter. The overexcitation limiter begins to limit the field current of generator G3 at about time t = 226 seconds. The limiting of the field current of generator G3 results in the terminal voltage of generator G3 reducing, and therefore system voltages in the transmission, sub-transmission and distribution systems also reduce. The OLTC again attempts to restore the load voltage through tap up movements. Each tap up movement of the OLTC results in decrease rather than increase of the load voltage, indicating that the system is now voltage unstable. The load voltage drops progressively until the OLTC reaches its limit at about time t = 165 seconds. When the synchronous condenser is placed at bus 9 its reactive power support to the load keeps the voltage at bus 11 within the deadband of the reference value, and the field current of generator G3 below the low set limit. Thus the system voltage stability is maintained when the synchronous condenser is placed at bus 9. Once again the reasons for the differences in the effectiveness of the synchronous condenser to enhance voltage stability when the synchronous condenser is placed at the three different locations arise from the difficulty in reactive power transfer over long transmission lines as discussed in the case of load levels 1 and 2.

5.4 Static var compensator

Finally the effect of using a static var compensator to enhance voltage stability in the 11-bus benchmark system was investigated. An SVC was included in the 11-bus benchmark system for each of the three load levels considered in chapter four. For the case of load level 1 a static var compensator rated 275MVAr was used, while for the case of load level 2 the static var compensator used was rated 292MVAr and for the case of load level 3 the static var compensator used was rated 330MVAr. The SVC controller used in this thesis is

shown in Fig. 3.18. The controller is modelled to control the reactive power output of the SVC. The intention is to provide no reactive power to the system before the disturbance, and only after the disturbance is the reference value of the SVC reactive power output set to 1.0 pu. Figs. 5.20(a) to 5.20(c) show the system response for the case of load level 1. The response of the system at load level 2 is shown in Figs. 5.21(a) to 5.21(c). The system response for the case of load level 3 is shown in Figs. 5.22(a) to 5.22(c). The figures show the phase A low side voltage (VLOWA) of the SVC in kV, the reactive power reference value (Qref) in pu., the calculated firing angle (alpha) in degrees, current in leg 1 (ileg1, A phase to B phase) of the TCR in kA, and the reactive power output of the SVC (Qsvc). The figures also show the time responses of the transmission system voltage (bus 7), sub-transmission system voltage (bus 10), distribution system voltage (bus 11), and the field current of generator G3 (IfieldG3). The figures also show graphs of the active power output of generator G3 (PGen3), the reactive power output of generator G3 (QGen3) and the reactive power supplied at bus 7 from generator G3 (QBus7) (i.e. the reactive power after the step-up transformer T3) and the reactive power output of the static var compensator (Qsvc).

The graphs show that in each case the reactive power output of the SVC is initially at 0.0 p.u. Immediately after the loss of the transmission line at about time t = 4 seconds, the sensing circuit measuring the voltage at bus 7 causes the set-point of the SVC's reactive power controller to be set to 1.0 p.u. The SVC's firing angle, current and reactive power output are adjusted accordingly as shown in Figs. 5.20 to Fig. 5.22.

For the case of load level 1 the extra reactive power supplied by the SVC at bus 7 is sufficient to keep the system voltages close to their pre-disturbance values. The voltage at bus 11 is within the deadband of its reference value after the disturbance, and no OLTC tap up movements are required.

For the case of load level 2, the system response is similar to that at load level 1. The voltage at bus 11 remains within the deadband of its reference value after the disturbance, and no tap up movements of the OLTC happen. The field current of generator G3 remains below the low set limit after the disturbance and the system voltage stability is maintained.

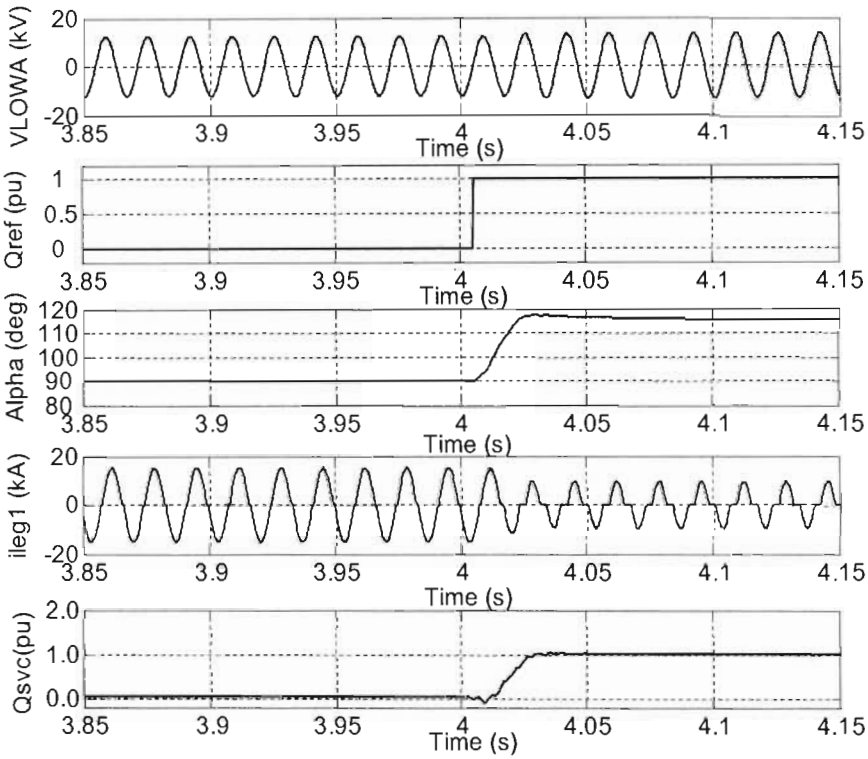

Fig. 5.20 (a) Load level 1 with an SVC of 275MVAr at bus7: Low side phase A voltage (VLOWA); reactive power reference value (Qref); firing angle (Alpha); current in leg 1 (ileg1); and reactive output power of SVC (Qsvc).

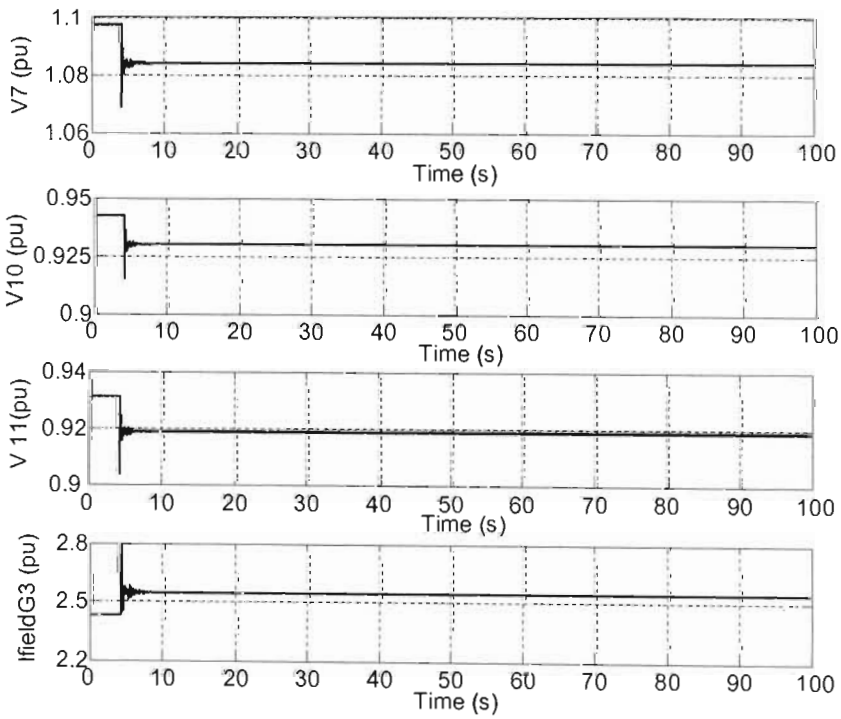

Fig. 5.20(b) Load level 1 with an SVC of 275MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

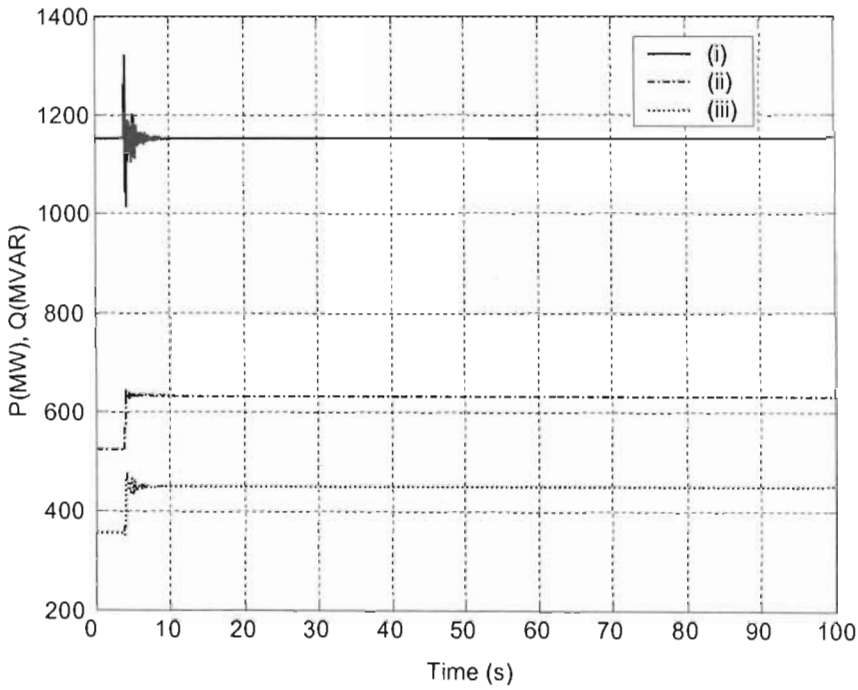

Fig. 5.20(c) Load level 1 with an SVC of 275MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7.

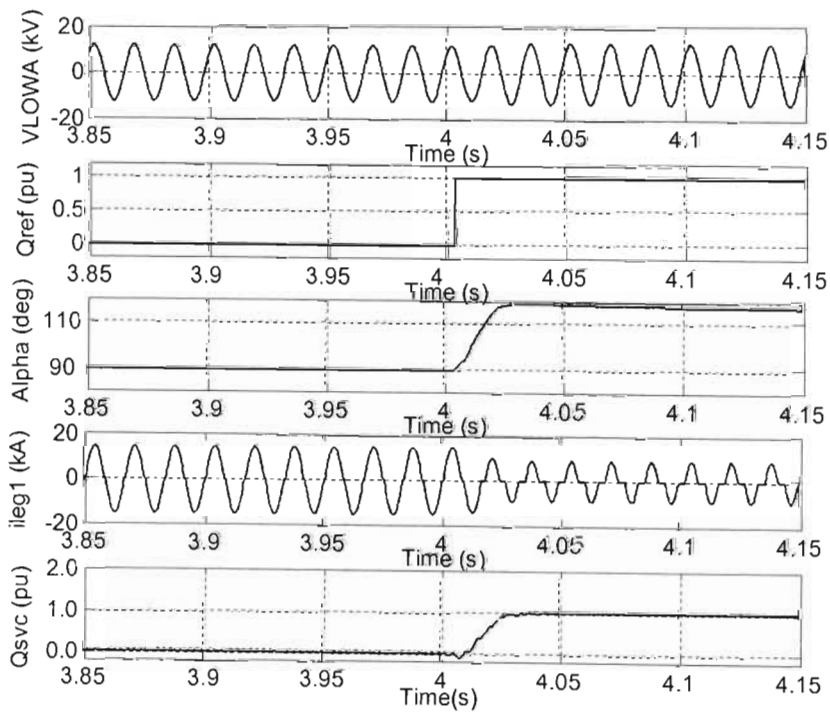

Fig. 5.21(a) Load level 2 with an SVC of 292MVAr at bus7: Low side phase A voltage (VLOWA); reactive power reference value (Qref); firing angle (Alpha); current in leg 1 (ileg1); and reactive output power of SVC (Qsvc).

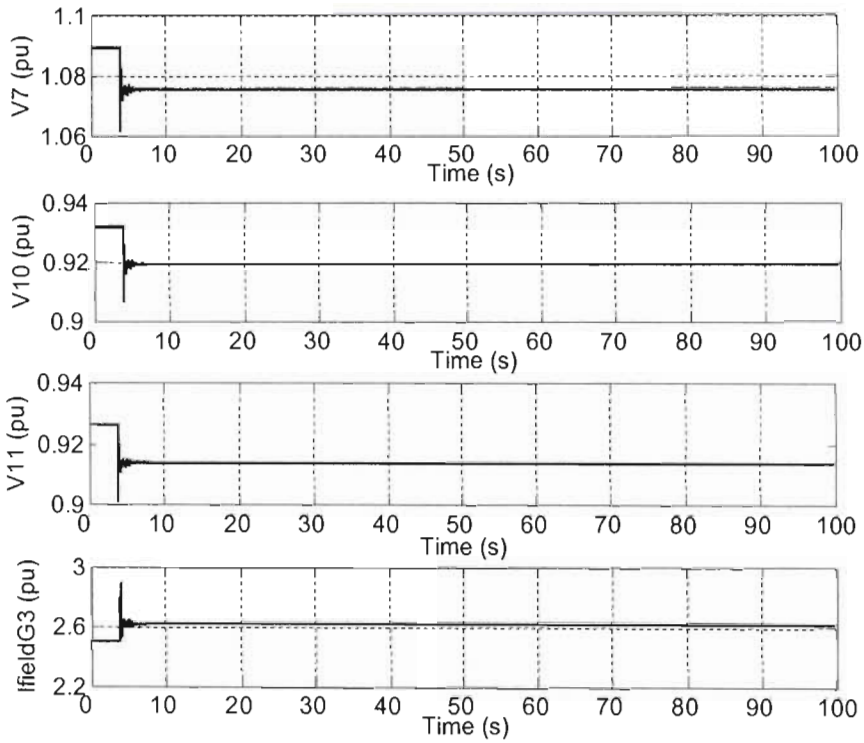

Fig. 5.21(b) Load level 2 with an SVC of 292MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

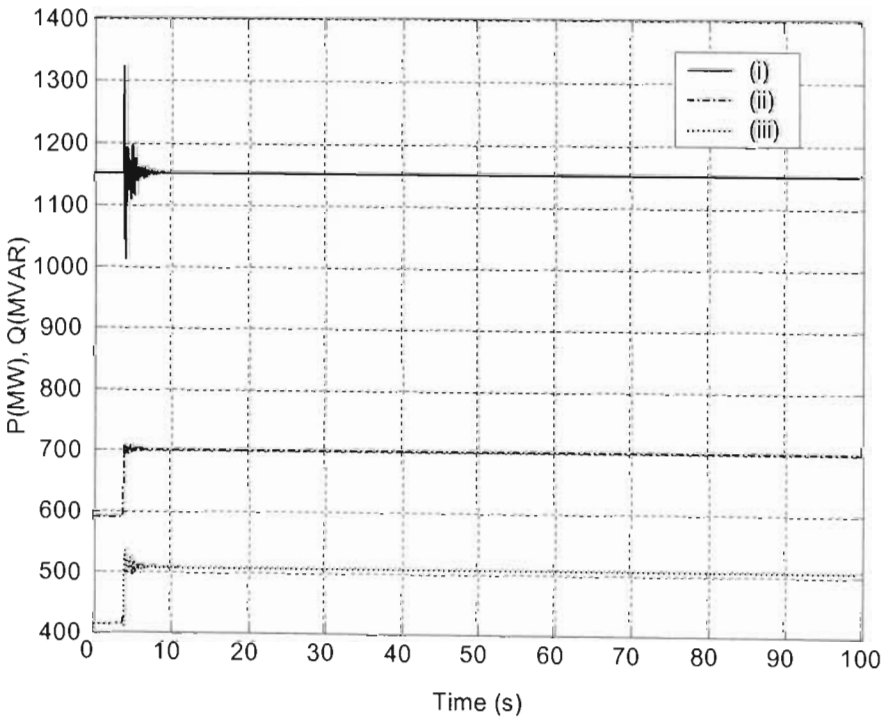

Fig. 5.21(c) Load level 2 with an SVC of 292MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7.

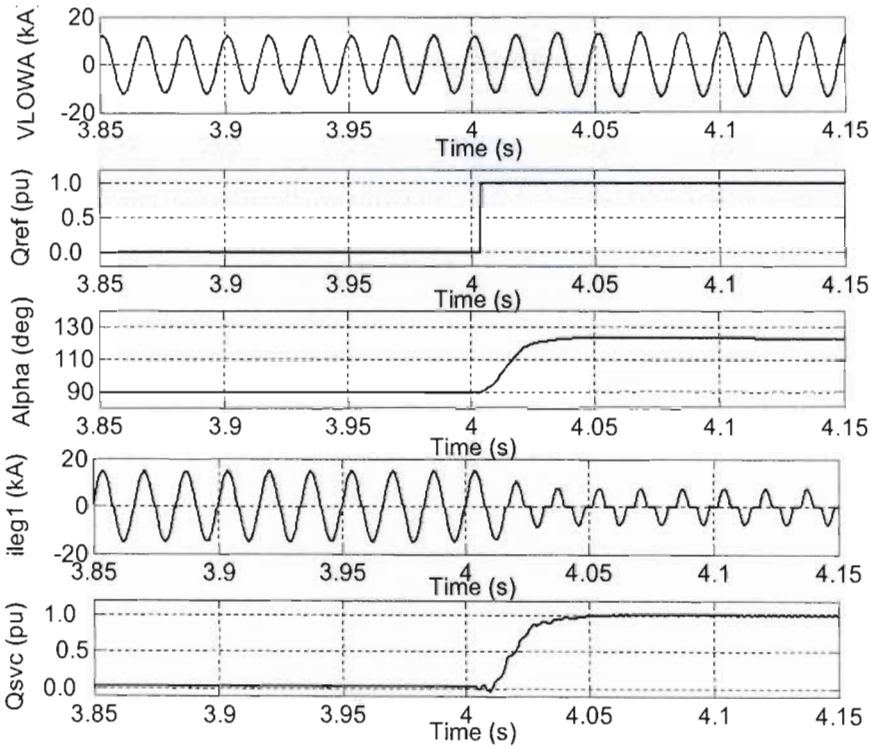

Fig. 5.22(a) Load level 3 with an SVC of 330MVAr at bus7: Low side phase A voltage (VLOWA), reactive power reference value (Qref), firing angle (Alpha), current in leg 1 (ileg1), and reactive output power of SVC (Qsvc).

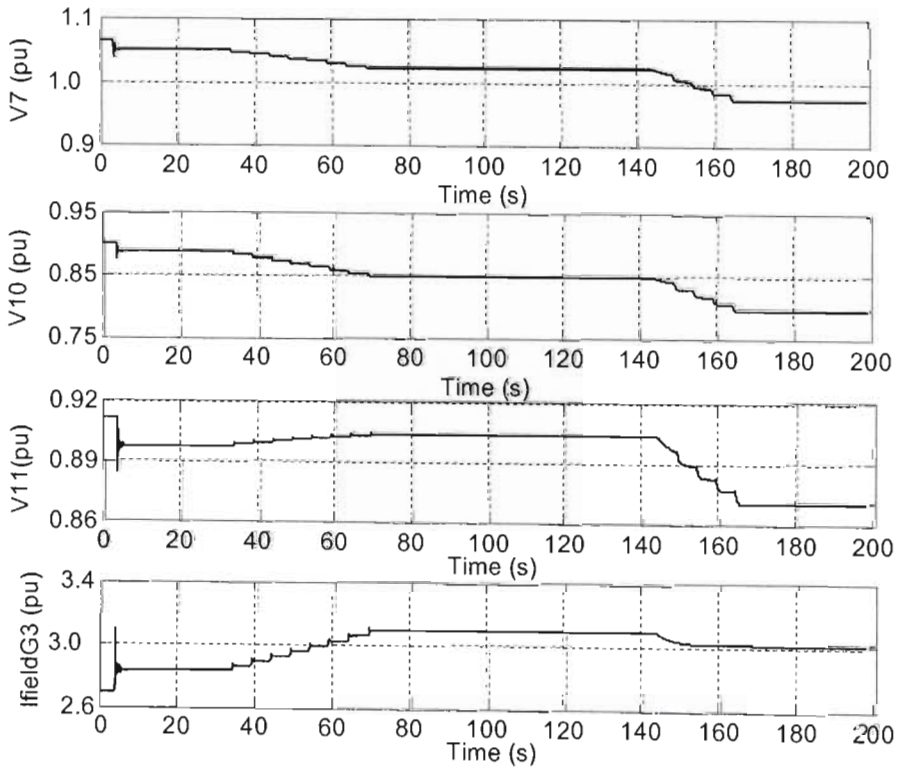

Fig. 5.22(b) Load level 3 with an SVC of 330MVAr at bus 7: Bus voltage magnitudes and field current of generator G3.

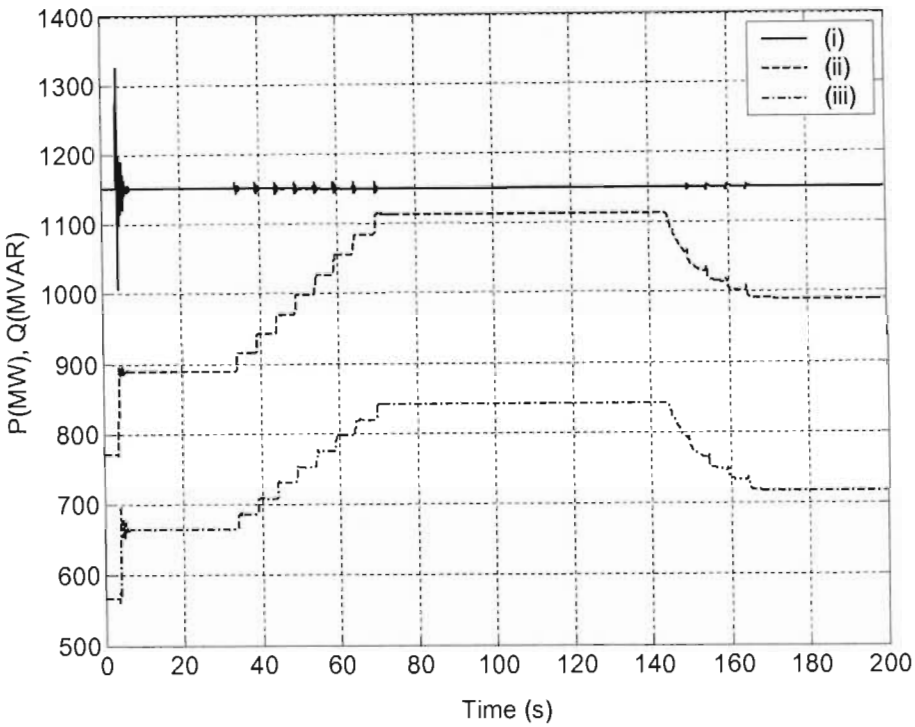

Fig. 5.22(c) Load level 3 with an SVC of 330MVAr at bus 7: (i) PGen3 (ii) QGen3 (iii) QBus7.

At load level 3, the initial disturbance causes the voltage at bus 11 to drop, and be outside the deadband of the reference value. After about 30 seconds from the initial disturbance, the OLTC begins to tap up to bring the voltage at bus 11 within the deadband of the reference value and continues to tap up thereafter at 5 second intervals. The tap up movement of the OLTC results in the increase of the reactive power demand and subsequently the increase in generator G3 reactive power output and field current. After about 70 seconds, the voltage at bus 11 is brought within the deadband of its reference value. However, the field current of generator G3 is now above the low set limit of the overexcitation limiter. The overexcitation limiter begins to limit the field current of generator G3 at about time t = 155 seconds. The limiting of the field current of generator G3 results in the terminal voltage of generator G3 reducing, and therefore system voltages in the transmission, sub-transmission and distribution systems also reduce. The OLTC again attempts to restore the load voltage through tap up movements. Tap up movements of the OLTC result in decrease rather than increase of the load voltage, indicating that the system is now voltage unstable. The voltage at bus 11 drops progressively until the OLTC reaches its limit at about time t = 163 seconds.

5.5 Conclusion

Voltage stability enhancement of the 11-bus benchmark system using three different methods has been investigated on the RTDS. The investigations have verified some of the characteristics of the different methods that can be used for enhancing voltage stability. The investigations have shown that the effectiveness of a switched shunt capacitor to enhance voltage stability relies not only on the size of the shunt capacitor used but also on its location in the power system. The investigations have also shown that the reactive power supplied by a synchronous condenser in the reactive power control mode is independent of the bus voltage at which it is located. This was seen by the constant reactive power supplied by the synchronous condenser when placed at the three different locations in the 11-bus benchmark system. Thus during low system voltages the synchronous condenser is more effective in supplying reactive power and controlling voltage than is a shunt capacitor. The SVC also provides reactive power independent of the bus voltage within its voltage control range when operated in the reactive power control mode. The studies have showed the ability of the RTDS to be used to investigate methods of voltage stability enhancement and the optimum placement of control equipment.

The effectiveness of the three methods of voltage stability enhancement to provide reactive power support varies depending on the system conditions and / or the mode of operation of the equipment used. The shunt capacitor provides reactive power that is proportional to the square of voltage (Equation 2.13). Thus when the shunt capacitor is placed at bus 7 where both the pre-disturbance voltage and post-disturbance voltage is greater than 1 p.u. (Fig. 5.8(a)) its output reactive power is higher than the rated value (1.06^2 or 1.12 times the rated output of 330MVA at load level 3). The reactive power supplied by the synchronous condenser when operated in the reactive power control mode as described in section 5.3 is kept constant at the reference value. In the studies in this thesis, the reference value of the reactive power of the synchronous condenser was 1.0 pu on the base of 330MVA at load level 3. Similarly, the reactive power output of the SVC operated in the reactive power output control mode (section 5.4) is kept constant at the reference value. The reference value of reactive power for the SVC in this thesis was 1.0 pu on the base of 330MVA at load level 3. Figs. 5.8(a) and (b), 5.18(a) and (b) and 5.22 (b) show the responses of the system at load level 3 when each of the three methods of voltage enhancement considered in this thesis are used, with the equipment placed at bus 7. The results show that the

switched shunt capacitor maintains system voltages after the disturbance, such that the voltage at bus 11 remains within the deadband of the OLTC. When the synchronous condenser is used on the other hand, the voltage at bus 11 immediately after the disturbance is outside the deadband of the OLTC and tapping up is necessary to bring the voltage at bus 11 within the deadband. Field current limiting of generator G3 takes place after about 225 seconds. In the case of the SVC, the voltage at bus 11 after the disturbance is also outside the deadband and tap up movements of the OLTC are necessary to bring the voltage at bus 11 to within the deadband. The field current limiting of generator G3 takes place after about 145 seconds.

Investigations of voltage stability enhancement in this chapter have been done using real-time software models of power system controllers. However, certain control equipment may not be easy to model accurately. In order to conduct thorough testing of the equipment, it may be necessary to test the actual hardware equipment in closed loop with a simulation of a power system. The next chapter demonstrates the use of the real-time digital simulator for carrying out hardware-in-loop testing of control equipment for voltage stability studies.

CHAPTER SIX

CLOSED LOOP TESTING OF A PHYSICAL CONTROL DEVICE FOR VOLTAGE STABILITY STUDIES

6.1 Introduction

The previous three chapters presented the development of software models of power system components and two benchmark systems for voltage stability studies on the RTDS. In chapter three the development of real-time models of power system components that are known to play an important role in voltage stability incidents was presented, while in chapter four development of two benchmark systems for real-time simulator studies for voltage stability was presented. Simulation results from the benchmark systems were used to establish the validity of the real-time models developed and demonstrated that the RTDS can be used for conducting detailed time-domain voltage stability studies over relatively long time frames. In chapter five the use of the RTDS for assessing three different methods of enhancing voltage stability in the 11-bus benchmark system was presented. The simulation studies presented in the previous chapters employed real-time software models of all the power system components and controllers.

However, in some cases, in order to carry out thorough testing of the performance of some power system control devices that may not be easy to model, it is necessary to test the actual control devices in closed loop with a simulation of the power system. This chapter demonstrates the use of the Real-Time Digital Simulator for testing the performance of a physical control device in closed loop with a simulated power system. The control device tested is a voltage regulating device known as the REG-DA voltage regulator™. The software model of the OLTC controller in the 11-bus voltage stability benchmark system presented in chapter four is substituted with the actual REG-DA voltage regulator for voltage control. Real-time simulations of the benchmark system involving all-software models of power system components are compared with the simulations involving the REG-DA voltage regulator hardware in closed loop with the simulation.

6.2 RTDS Input and Output

The RTDS provides specialized input and output ports for hardware-in-loop testing of power system control and protective devices with simulations. Variables from the simulation are taken as output from the simulator and used as input to the external control or protective device and, the output from the external device is fed back to the simulation. The input and output signals are in the form of analogue signals or digital signals depending on the particular input requirements of the control or protective device being tested and the nature of its output signals. Thus the RTDS is equipped with a number of specialised output and input ports offering a range of specifications.

6.2.1 Analogue output

There are a number of digital-analogue output cards that can be found on the RTDS. The FDAC (Fibre Digital-Analogue Converter) card is a six channel card that can produce analogue signals that require a dynamic range. The FDAC card has the following specifications [17]:

- Provides optically isolated analogue output
- Six analogue output channels
- Output voltage range: +/- 10 volts peak
- Output current: 5 mA maximum
- Resolution: 305 μV
- Signal selection and scaling in RSCAD/Draft.

6.2.2 Digital input

Input of digital signals from external equipment to the RTDS can be done via a 16-bit digital input port available on the RTDS's processor cards known as 3PC cards. The A and B processors of 3PC cards each have a 34-pin connector that provides access to a 16-bit digital input port and 16-bit digital output port. The digital inputs on the 3PC cards are TTL logic (i.e. 0-5 volts) and are pulled up to +5 volts via a 4.7kΩ resistor. Thus, when there is no connection to a digital input, the software accessing the input interprets the reading as logic "1" [27].

In this thesis, analogue signals of bus voltages are taken as output signals from the simulation of the 11-bus voltage stability benchmark system on the RTDS to an external voltage regulating relay know as REG-DA voltage regulator ™ for voltage control. The output card used to take voltage signals from the RTDS to the REG-DA voltage regulator is the FDAC card. Output contacts representing tap up and tap down commands for an on-load tap changing transformer are taken from the REG-DA voltage regulator to the simulation on the RTDS through a digital input port on a 3PC card.

6.3 The REG-DA Voltage Regulator

The REG-DA voltage regulator is a digital power system control device that can control voltage at a bus through an on-load tap changer transformer. Scaled down voltage and current signals from the controlled bus in the power system are supplied as inputs to the REG-DA. In an actual power system voltage and current are scaled down using voltage transformers (VTs) and current transformers (CTs) respectively, while in a simulation the scaling down from power levels of voltage and current can be achieved through software models of VTs and CTs and/or through special output cards such as the FDAC card used in this thesis. The REG-DA processes the input signals and provides tap up or tap down signals to the OLTC transformer depending on the user settable reference value for voltage and the deadband. The REG-DA has five operating modes that run in parallel and perform tasks according to the parameters entered for each mode [28].

The *regulator mode* controls the magnitude of the voltage at the controlled bus by comparing it with a set-point value. If the difference between the actual voltage value and the set-point value, known as the regulative deviation, is within the deadband of the voltage reference value, no tap up or tap down commands are sent to the OLTC transformer. However, if the regulative deviation is outside the deadband of the voltage reference value, a tap up or tap down command is sent to the OLTC transformer depending on whether the actual voltage of the controlled bus is lower or higher than the voltage reference value respectively.

The *transducer mode* displays various important measurement quantities at the controlled bus of the power system. Some measurements that are displayed are voltage magnitude,

current magnitude, real power, reactive power, apparent power, power factor and frequency.

The *recorder mode* records measured values of line voltage and transformer tap position. A measurement value that is the arithmetic average of the bus voltage magnitude is stored in the memory each second.

In the *statistics mode,* tap changes under load and tap changes when idling are differentiated and recorded. Tap changes under load are classified as those tap changes that occur when the measured current is more than 5% of the nominal line current, while tap changes when idling are those tap changes that occur when the line current is less than 5% above the nominal line current [28].

Lastly the *paragramer mode* is used to automatically prepare parallel connections of transformers and one-line visualisation of the status of switches.

The results presented in this thesis are based on the regulator mode of the REG-DA voltage regulator. The regulator mode of the REG-DA voltage regulator offers several time programs for delay time between tap movements of the OLTC transformer. The integral time program uses the algorithm dU * t = constant, where dU is the regulative deviation of voltage (the difference between the actual voltage measurement and the voltage set-point), and t is the delay time of the regulator. After the integral of the voltage deviation dU with respect to time reaches a specified value, a tap-change operation is carried out and the integrator is reset to zero. If the voltage is still outside the deadband after the regulation procedure, the regulator waits for the time specified in the algorithm before it initiates another command for tap movement. This ensures that small regulative deviations may be present for a long time before a tap-change is triggered, whereas large deviations are rectified more quickly. In the linear time program the delay time of the regulator is linearly proportional to the regulative deviation of the voltage. The third time program on the REG-DA voltage regulator works with fixed delay times. This time program is referred to as the *const* time program. In the *const* time program, regulative deviations that lie outside the deadband and are smaller than two times the deadband are rectified after a delay time T1. Larger regulative deviations are rectified after delay time T2. The delay time T1 is greater than T2 ensuring that large deviations are rectified faster than smaller regulative

deviations. The time settings used for the REG-DA voltage regulator in the study in this thesis were T1 = 10 seconds and T2 = 5 seconds.

The *const* time program of the REG-DA voltage regulator works with two different fixed delay times but does not offer a longer delay time for the initial tap movement as in the OLTC controller of the 11-bus voltage stability benchmark system described in section 3.4. In order to demonstrate the use of the RTDS for testing the physical REG-DA voltage regulator, the real-time model of the OLTC controller in the 11-bus voltage stability benchmark system was adjusted to have a time response similar to that of the *const* time program of the REG-DA voltage regulator. Real-time simulation results of the all-software model of the 11-bus voltage stability benchmark system were compared with simulation results involving hardware-in-loop testing of the REG-DA voltage regulator.

Fig. 6.1 shows the adjusted real-time model of the OLTC controller with the time program similar to the *const* time program of the REG-DA voltage regulator. The adjusted OLTC model shown in Fig. 6.1 is similar to OLTC model described in section 3.4 with the exception that this model uses two different delay times between tap movements. A switch (block 12) determines the delay time used. The position of the switch (block 12) depends on whether the voltage error magnitude Verr is greater than two times the deadband or the voltage error magnitude is less than two times the deadband. If the voltage error is greater than two times the deadband the delay time between tap movements is 5 seconds, while if the voltage error is less than two times the deadband but greater than the deadband, the delay time is 10 seconds. Otherwise, no tap movements are initiated.

6.4 RTDS Hardware-in-loop Testing of the REG-DA Voltage Regulator

Fig. 6.2 shows hardware-in-loop interconnections of the REG-DA voltage regulator with the RTDS. A voltage signal V_{ca} representing the voltage at the controlled bus of the simulated power system is sent as output from the RTDS through the FDAC output card. The output voltage signal from the FDAC card is amplified using an Omicron amplifier™.

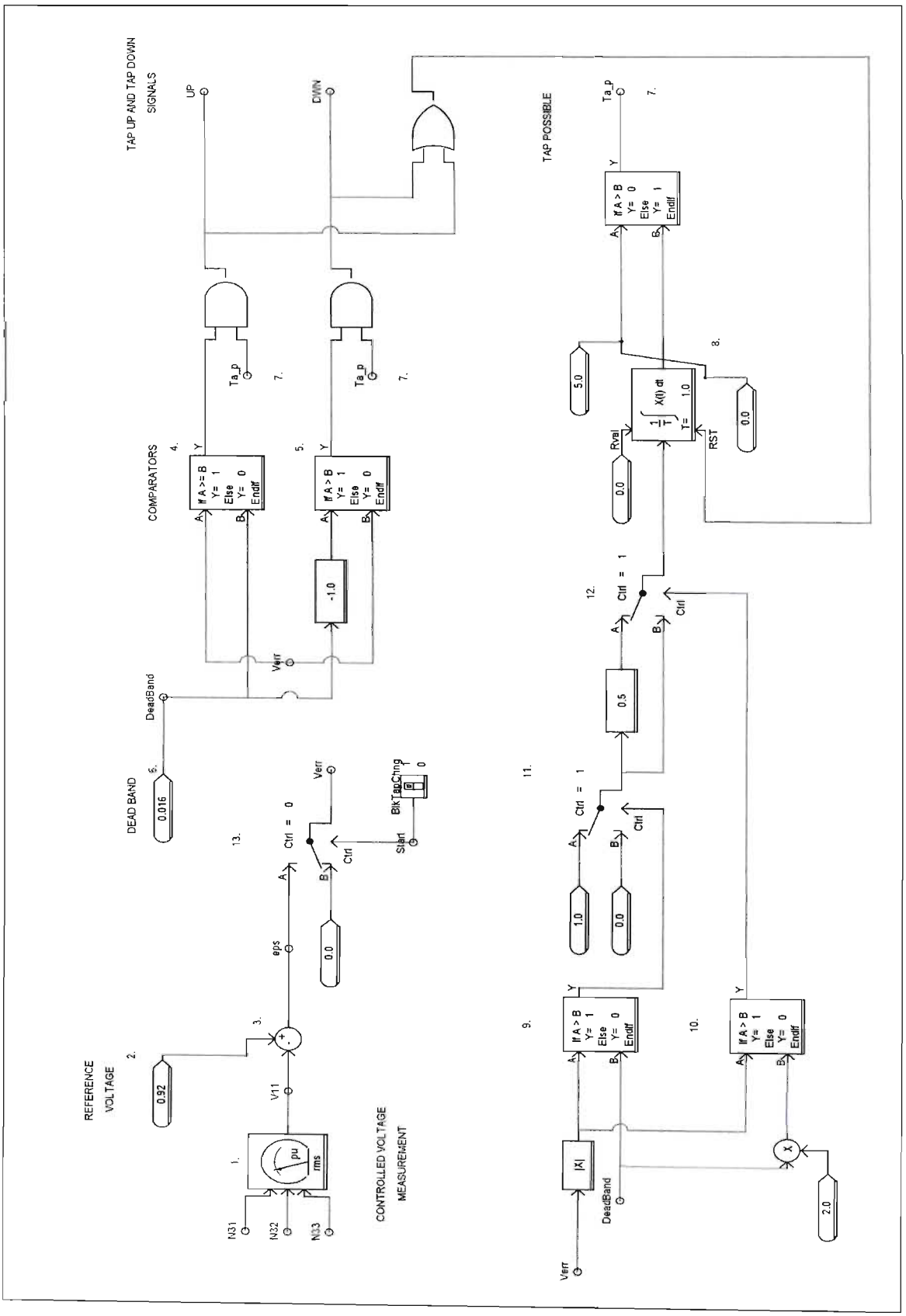

Fig. 6.1 Adjusted real-time model of an on-load tap changer transformer controller with the const time program.

The output from the Omicron amplifier is fed as input to the REG-DA voltage regulator. The REG-DA in turn sends control signals back to the RTDS for controlling the voltage at the controlled bus of the simulated power system.

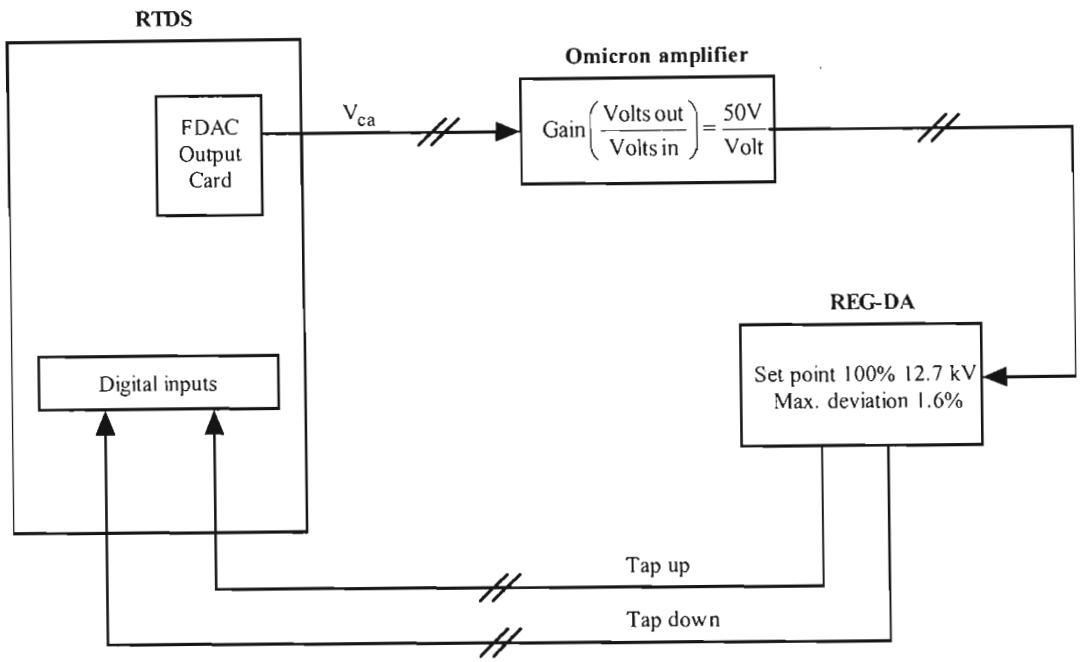

Fig. 6.2 Diagram showing interconnections for hardware-in-loop testing of a REG-DA voltage regulator with the simulation on the RTDS [27].

The nominal voltage of the controlled bus in the simulation is 13.8 kV. The output voltage signal from the FDAC card is a scaled down signal representing the voltage at the controlled bus in the simulation. The output voltage signal from the FDAC is in the range of +/-10 volts. The REG-DA voltage regulator operates with an input voltage range of 0-140 volts with 110 volts representing the nominal voltage value at the controlled bus.

Fig. 6.3 shows the overall gain of the FDAC card and the Omicron amplifier, where V_{in} is the measured bus voltage, V_{out} is the output voltage of the Omicron amplifier and S_x is the scale factor setting of the FDAC card.

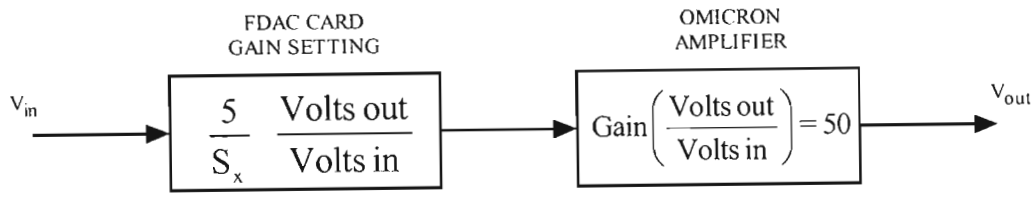

Fig. 6.3 Block diagram showing the overall gain of the FDAC card and the Omicron amplifier [27].

The measurement of the controlled bus voltage is done by the bus component in draft in kilovolts, thus the value of the reading is scaled down by a factor of 1000. In this case the nominal voltage at the controlled bus in 11-bus benchmark system is 13000 volts; this is read by the RMS meter as 13.8 since it is in kilovolts. The scale factor setting of the FDAC card can be calculated from the block diagram of Fig. 6.3 as follows:

$$V_{in} * \frac{5}{S_x} * 50 = V_{out}$$

$$13.8 * \frac{5}{S_x} * 50 = 110$$

$$S_x = 31.364$$

The REG-DA uses the voltage output from the amplifier V_{out} as the input value representing the controlled bus voltage in the simulated power system. The REG-DA regulates the system voltage at the controlled bus according to user settable parameters entered in its parameter fields. The control signals from the REG-DA are tap up and tap down commands for the OLTC transformer at the controlled bus of the power system. The tap up and tap down outputs from the REG-DA are normally-open contacts. These are fed into the digital inputs on the RTDS so that the real-time simulator can interpret the state of the contacts (i.e. open/closed) as a logical 1 or 0.

The contacts representing tap up and tap down commands are connected from the REG-DA to the RTDS as illustrated in Fig. 6.4 below. When the normally open contact in Fig.

6.4 inside the REG-DA is in the open position, the digital input to the RTDS is at logic '1' since it is pulled up to 5 volts through a 4.7Ω resistor. However when the normally open contact inside the REG-DA is closed, the digital input to the RTDS is forced to ground, and is at logic '0'.

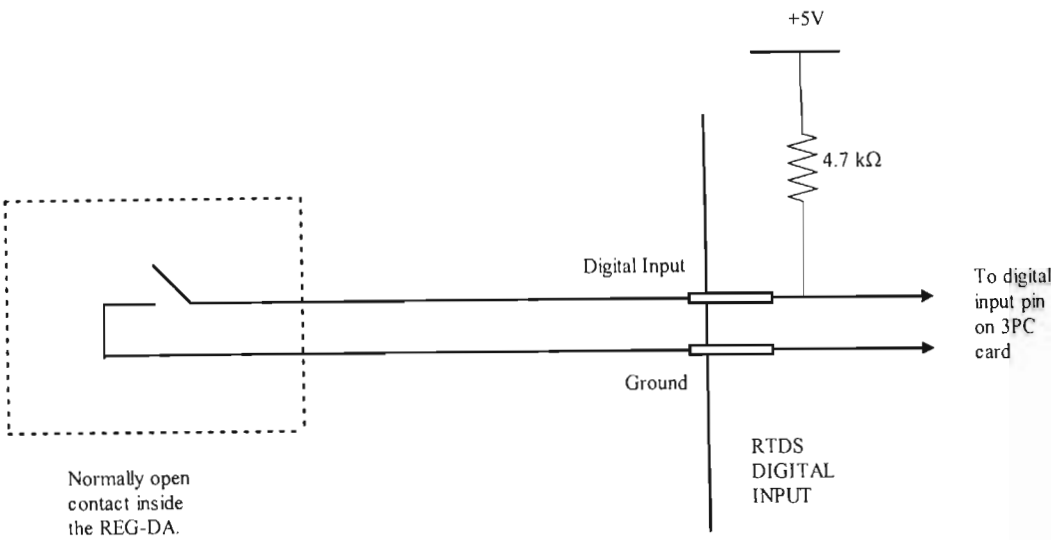

Fig. 6.4 Diagram illustrating interfacing of tap-up and tap-down contacts from the REG-DA to digital inputs on the RTDS [29].

Fig. 6.5 shows photographs of the actual interconnections between the RTDS and the REG-DA voltage regulator in the laboratory.

6.5 RTDS Simulation Results

Real-time simulator studies of the 11-bus voltage stability benchmark system were conducted first using an all-software simulation of the benchmark system, and then substituting the software model of the OLTC controller with the actual REG-DA voltage regulator hardware connected in closed loop with the simulation. In both cases the behaviour of the 11-bus voltage stability benchmark system was studied for three different load levels used in the studies in chapter four. The contingency investigated was the loss of one transmission line between bus 6 and bus 7 of the 11-bus voltage stability benchmark system.

Fig. 6.5 Photographs showing the interconnections between the RTDS and REG-DA voltage regulator in the laboratory.

6.5.1 Results of the all-software 11-bus voltage stability benchmark system

Figs. 6.6 to 6.8 show the response of the transmission system voltage (bus 7), sub-transmission system voltage (bus 10), distribution system voltage (bus 11), and the field current of generator G3 (IfieldG3) for each of the three load levels following the loss of one transmission line between bus 6 and bus 7 for the all-software simulation of the 11-bus benchmark system. The figures also show graphs of the active power output of generator G3 (PGen3) and reactive power output of generator G3 (QGen3) and the reactive power supplied at bus 7 from generator G3 (QBus7) (i.e. the reactive power after the step-up transformer T3). As can be expected, the time response of the system voltages is now influenced by the adjusted OLTC shown in Fig. 6.1. This OLTC is a software version of the REG-DA voltage regulator with its time program set to the *const* time program. The const time program does not offer a longer delay time for the initial tap movement of the OLTC transformer. Instead, the const time program uses one of two fixed time delays for tap movements, T1 and T2 depending on the magnitude of the regulative deviation.

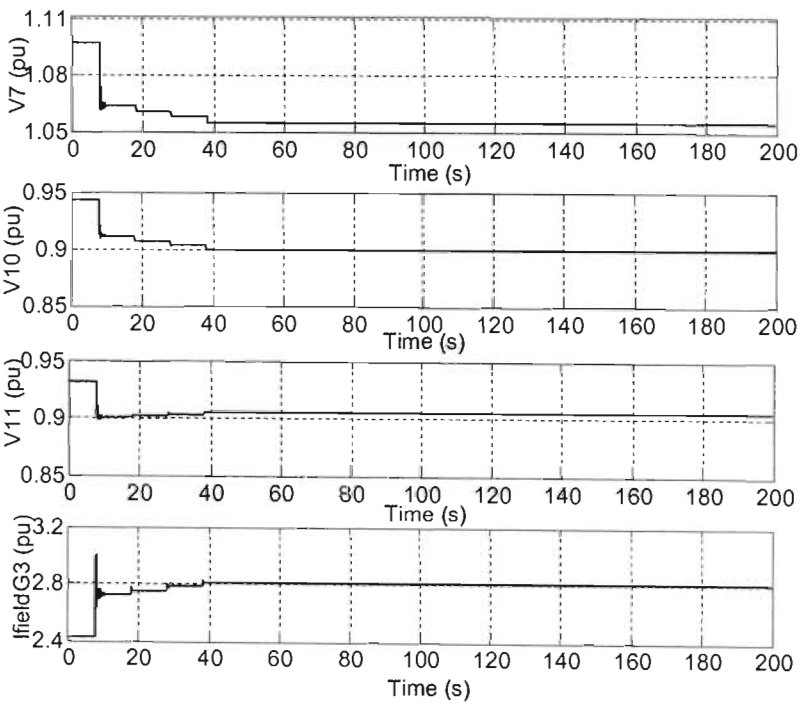

Fig. 6.6(a) Load level 1: Bus voltage magnitudes and field current of generator G3 of the all-software simulation of the 11-bus voltage stability benchmark system.

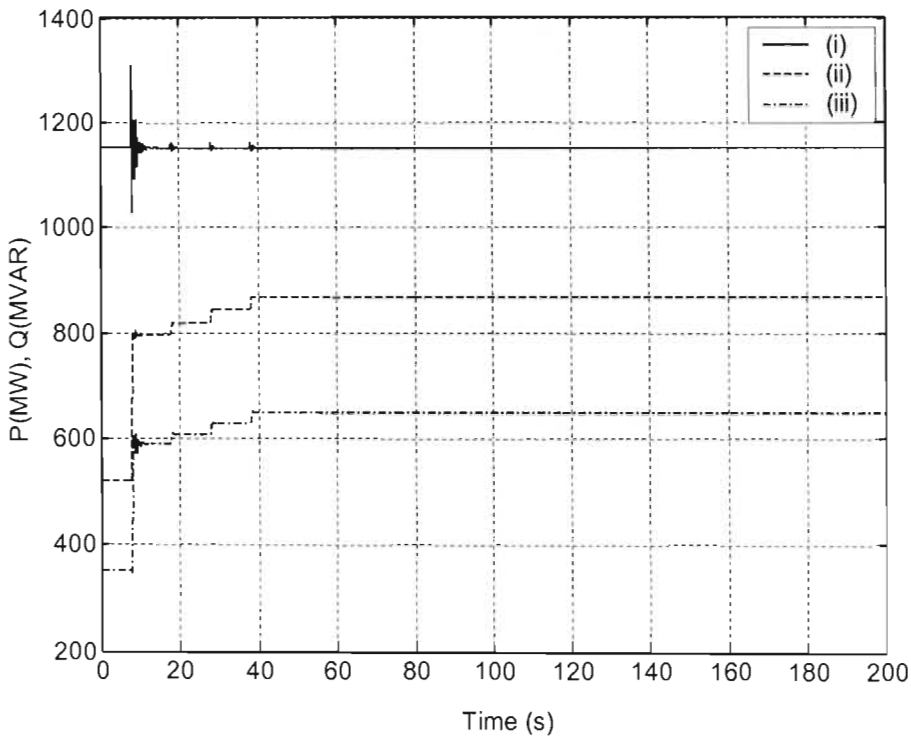

Fig. 6.6(b) Load level 1: (i) PGen3 (ii) QGen3 and (iii) QBus7 of the all-software simulation of the 11-bus voltage stability benchmark system.

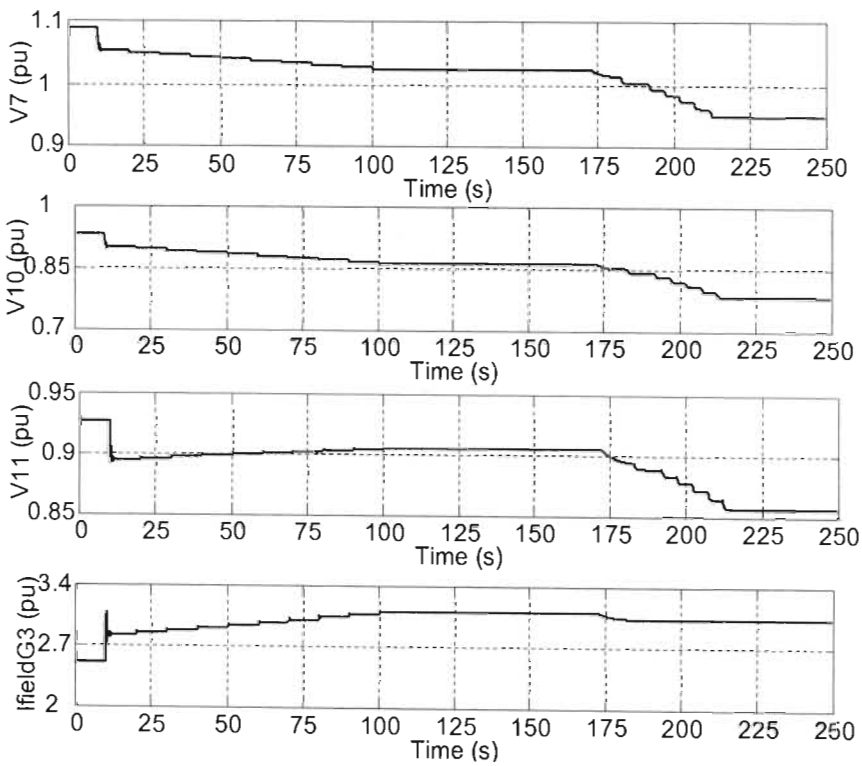

Fig. 6.7(a) Load level 2: Bus voltage magnitudes and field current of generator G3 of the all-software simulation of the 11-bus voltage stability benchmark system.

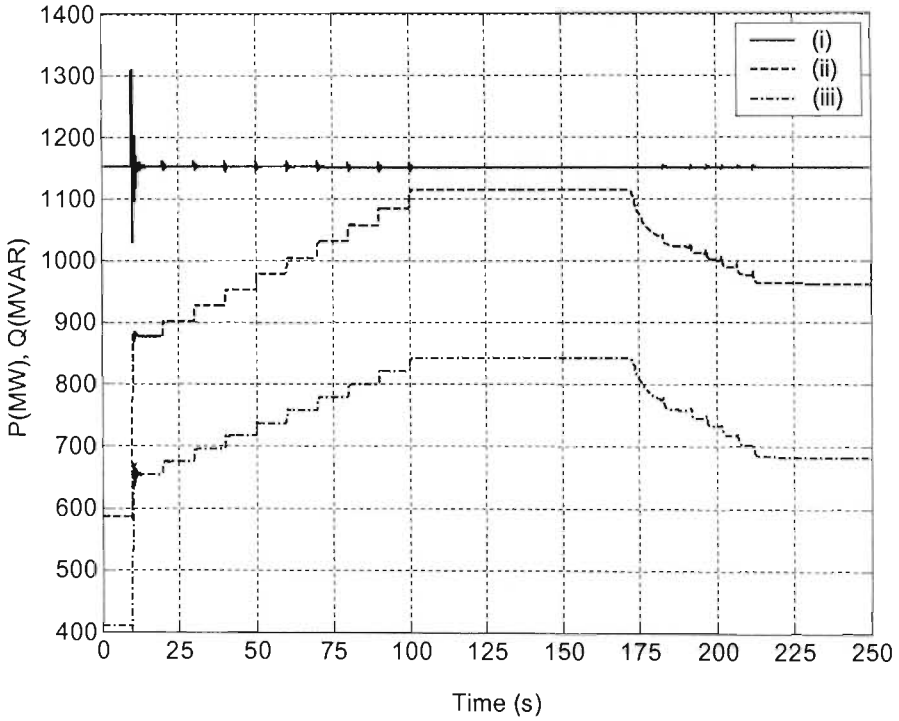

Fig. 6.7(b) Load level 2: (i) PGen3 (ii) QGen3 and (iii) QBus7 of the all-software simulation of the 11-bus voltage stability benchmark system.

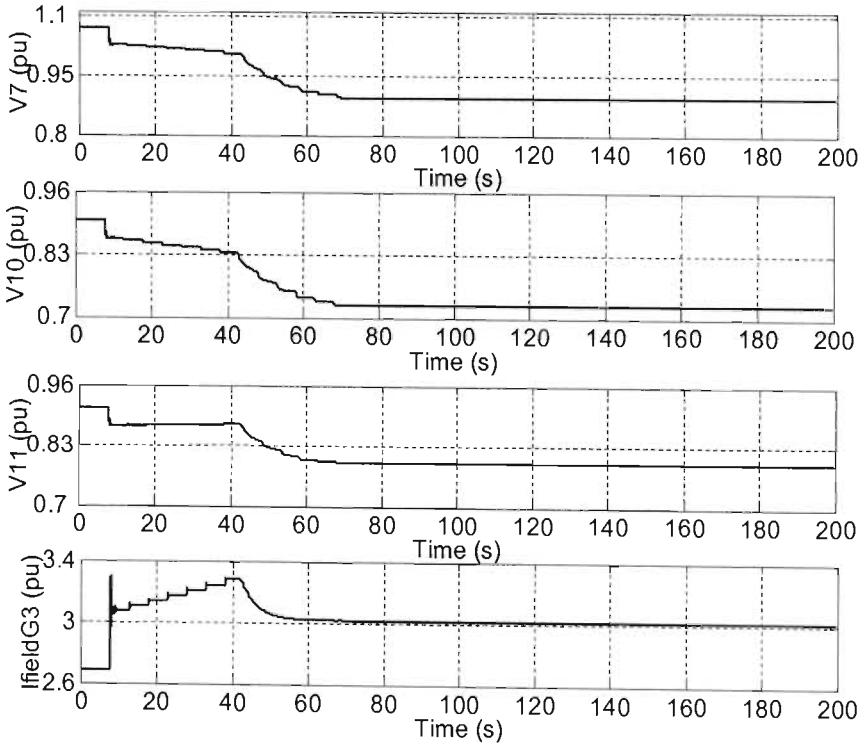

Fig. 6.8(a) Load level 3: Bus voltage magnitudes and field current of generator G3 of the all-software simulation of the 11-bus voltage stability benchmark system.

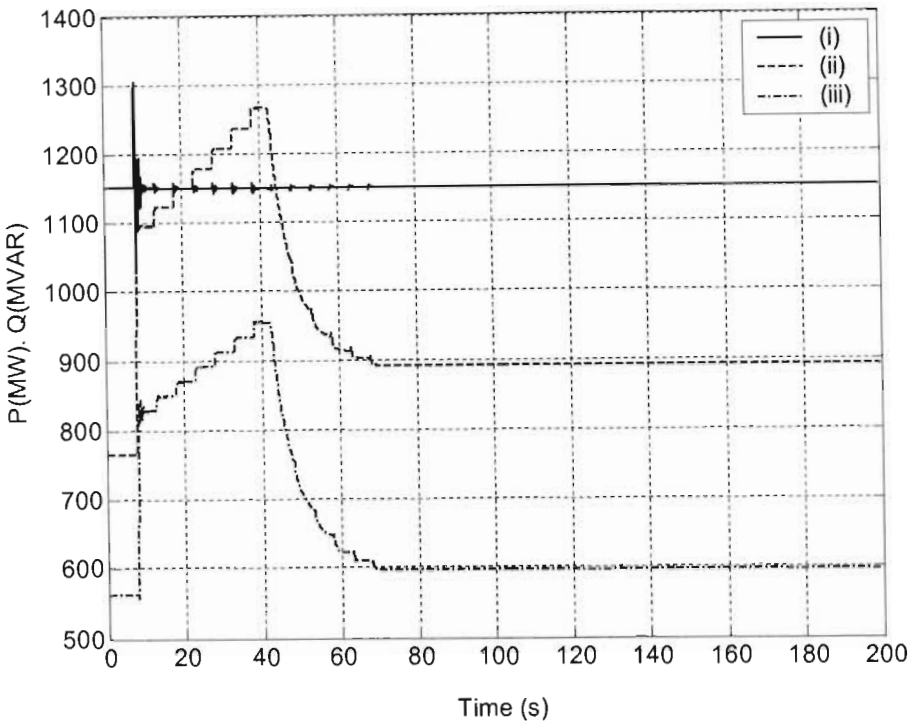

Fig. 6.8(b) Load level 3: (i) PGen3 (ii) QGen3 and (iii) QBus7 of the all-software simulation of the 11-bus voltage stability benchmark system.

At load level 1, the initial disturbance causes voltages in transmission, sub-transmission and distribution systems to drop, while the field current of generator G3 increases. The loss of the line also causes the reactive power output of generator G3 to increase while its active power output stays almost constant. The increase in the reactive power output of generator G3 is due to the increased reactive power demand of the transmission system after losing one of the lines between bus 6 and bus 7.

The system voltages remain stable at values lower than the pre-disturbance values until the OLTC begins to operate. The OLTC starts to operate by tapping up 10 seconds after the disturbance, and continues thereafter at 10 second intervals. Once the OLTC starts to operate, the voltage at bus 11 is raised up to close to its reference value, and load power increases with each tap up movement of the OLTC. The restoration of load voltage and power increases the reactive power demand on the generators, and leads to further increase of the field current of generator G3. The field current of generator G3, however, does not

exceed the field current limit setting on the overexcitation limiter. The OLTC restores voltage at bus 11 to close to its reference value at about 38 seconds, and the system voltage stability is maintained.

For the case of load level 2, the initial disturbance causes the system voltages to drop and the field current of generator G3 increases. The increase of the field current of generator G3 is higher than that for the case of load level 1 due to the heavier loading at load level 2. The system voltages at this load level are also lower than at load level 1 for the same reason of the system load being higher. Once again the OLTC operates to restore load voltage 10 seconds after the disturbance and continues at 10 second intervals for subsequent tap movements. Initially, tap up action of the OLTC results in the load voltage increasing toward the reference value, indicating that the system is voltage stable. The restoration of load voltage and power increases the reactive demand on the generators, and leads to further increase of the field current of generator G3. The load voltage is brought to close to its reference value after about 100 seconds. However, the field current of generator G3 is now above the low set limit but below the high set limit of the overexcitation limiter. The overexcitation limiter begins to limit the field current of generator G3 at about 172 seconds. The limiting action of the overexcitation limiter results in the terminal voltage of generator G3 reducing, and therefore system voltages in the transmission, sub-transmission and distribution systems also reduce. The OLTC again attempts to restore the load voltage through tap up movements. However, the tap up movements of the OLTC now result in decrease rather than increase of the load voltage, indicating that the system is now voltage unstable. The load voltage drops progressively until the OLTC reaches its limit at about 212 seconds. Thereafter, the system voltages are stable but are at low values compared to their pre-disturbance values.

For the case of load level 3, the initial disturbance immediately causes the field current of generator G3 to increase above the field current limit, and system voltages drop as in the case of the previous load levels, but now the voltages are lower than for the cases of load level 1 and load level 2. The OLTC responds to restore load voltage after about 5 seconds from the time of the disturbance and continues tapping up every five seconds thereafter. Initially tap up movements of the OLTC result in the load voltage increasing toward its

reference value, and the system is voltage stable. However, the overexcitation limiter starts to limit the field current of generator G3 after about 42 seconds. The field current limiting takes place earlier for the case of load level 3 because of higher system loading than in the case of the previous load levels. At load level 3 the reactive power demand is higher than at load level 2 and load level 1, and hence the field current of generator G3 is higher, resulting in the field current limiter acting after a shorter time because of its inverse time characteristic. Limiting of the field current of generator G3 causes a reduction of the generator G3 terminal voltage, and consequently, voltages in the transmission, sub-transmission and distribution systems are reduced. The attempts of the OLTC to restore voltage at bus 11 result in further decrease rather than increase of the voltage at that bus, indicating that the system is now voltage unstable. The voltage at bus 11 drops progressively until the OLTC reaches its maximum limit at about 68 seconds.

6.5.2 Results of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator

The simulation results of the 11-bus voltage stability benchmark system involving hardware-in-loop testing of the REG-DA voltage regulator are shown in Figs. 6.9 to 6.11. The figures show graphs of the transmission system voltage (bus 7), sub-transmission system voltage (bus 10), distribution system voltage (bus 11), and the field current of generator G3 (IfieldG3) for each of the three load levels following the loss of one transmission line between bus 6 and bus 7 of the 11-bus benchmark system. The figures also show graphs of the active power output of generator G3 (PGen3) and reactive power output of generator G3 (QGen3) and the reactive power supplied at bus 7 from generator G3 (QBus7) (i.e. the reactive power after the step-up transformer T3).

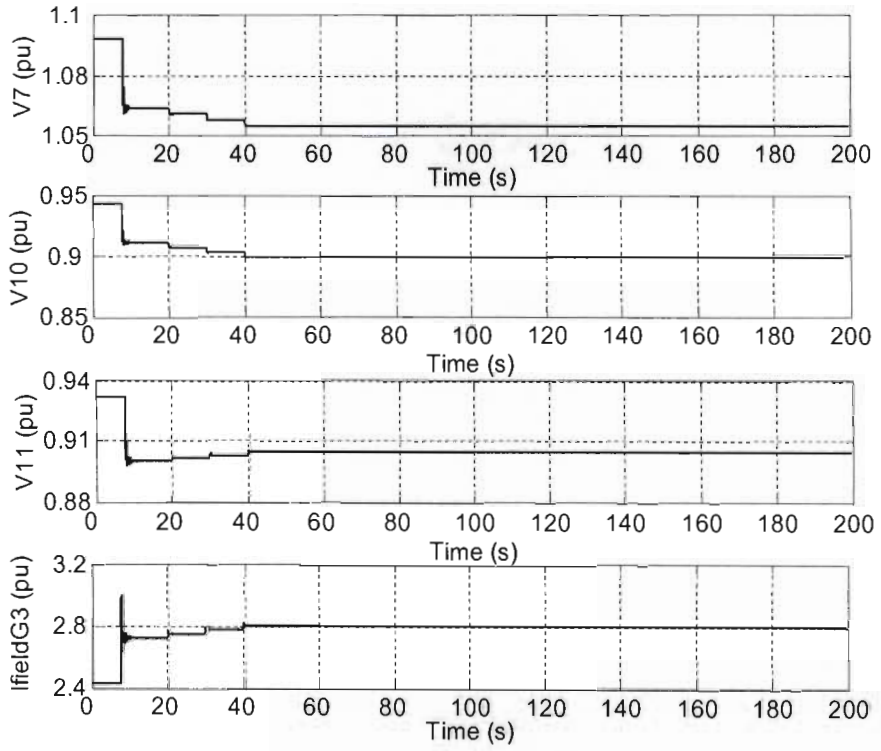

Fig. 6.9(a) Load level 1: Bus voltage magnitudes and field current of generator G3 of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator.

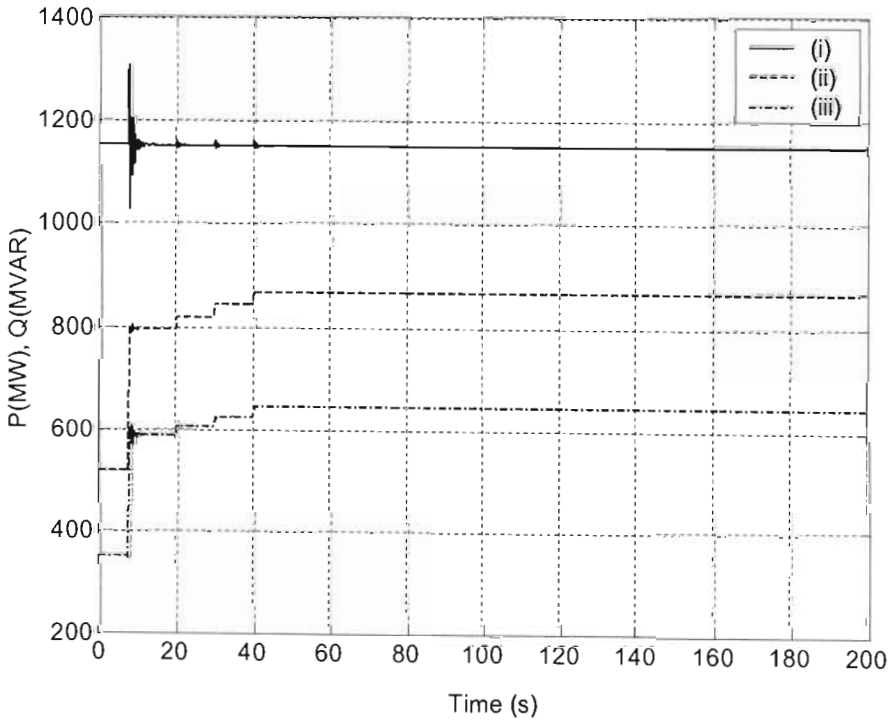

Fig. 6.9(b) Load level 1: (i) PGen3 (ii) QGen3 and (iii) QBus7 of the of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator.

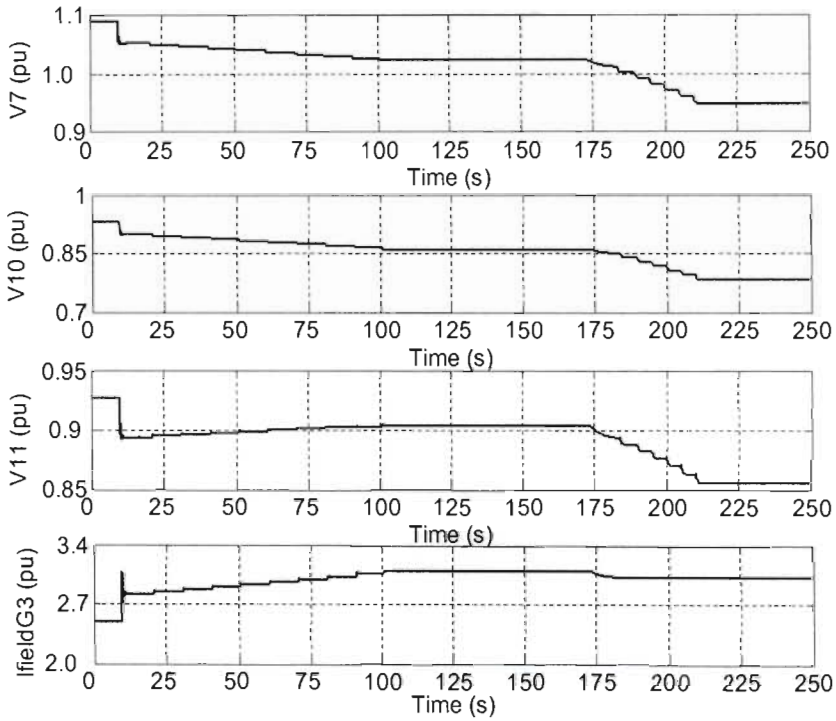

Fig. 6.10(a) Load level 2: Bus voltage magnitudes and field current of generator G3 of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator.

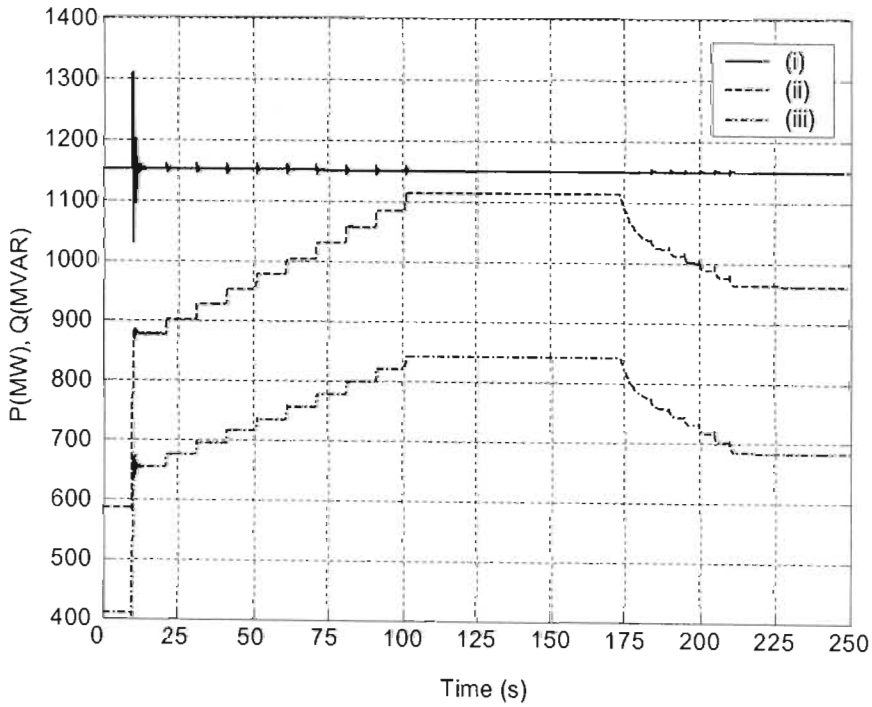

Fig. 6.10(b) Load level 2: (i) PGen3 (ii) QGen3 and (iii) QBus7 of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator.

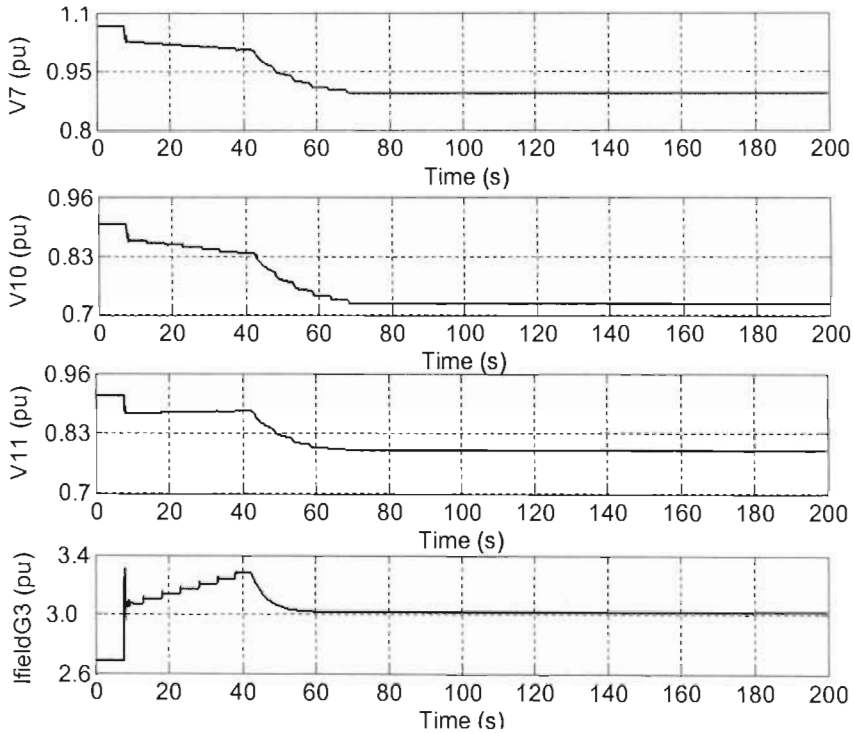

Fig. 6.11(a) Load level 3: Bus voltage magnitudes and field current of generator G3 of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator

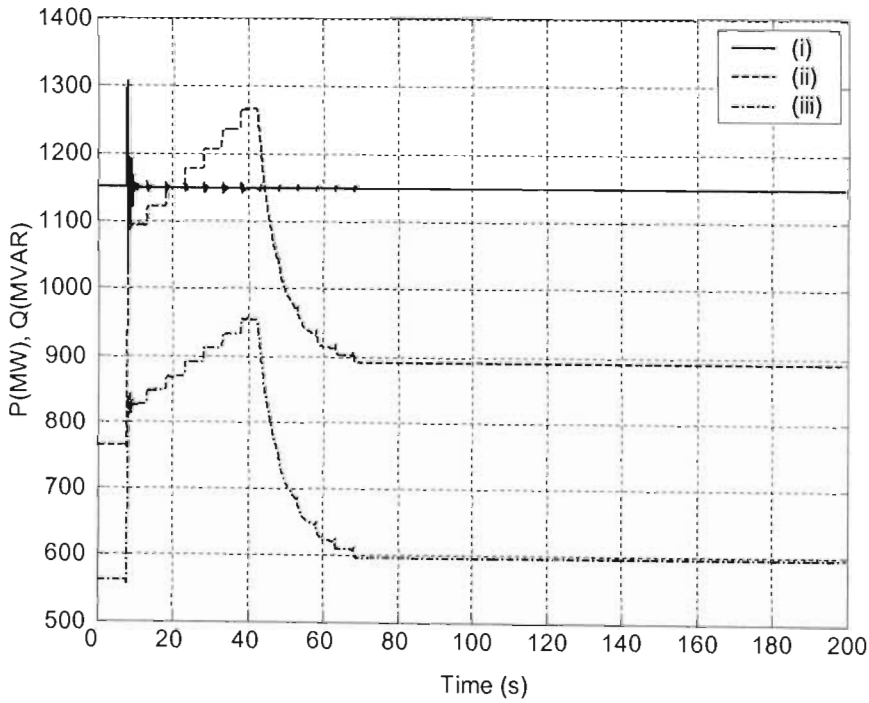

Fig. 6.11(b) Load level 3: (i) PGen3 (ii) QGen3 and (iii) QBus7 of the 11-bus voltage stability benchmark system with hardware-in-loop testing of the REG-DA voltage regulator.

The simulation results of the 11-bus voltage stability benchmark system with the REG-DA voltage regulator connected in closed loop are the same as the results of the all-software simulation of the system shown in Figs. 6.7 to 6.9. These results have shown that the software model of the REG-DA voltage regulator and the actual REG-DA voltage regulator tested in closed loop with the simulation have the same performance in controlling the system voltage of the simulated power system. Thus the real-time simulator has been successfully used to test an actual control device in closed loop with the simulation for voltage stability studies. This study has also provided confidence in the real-time models of power system components developed in this thesis for time-domain voltage stability studies.

6.6 Conclusion

This chapter has successfully demonstrated the use of the RTDS for conducting closed loop testing of a physical power system control device for voltage stability analysis. Results of the 11-bus voltage stability benchmark system using an all-software simulation have been compared with the simulation results of the benchmark system with the REG-DA in closed loop. The study has shown that the RTDS can be accurately used for testing hardware devices in closed loop with the simulation. This chapter has verified the performance of the real-time models of power system components that have been developed as part of the work of this thesis with an actual control physical device.

CHAPTER SEVEN

CONCLUSION

This thesis has considered the application of real-time power system simulation to time-domain voltage stability analysis. The advantages of using real-time simulation for voltage stability studies include among others the capability to simulate very accurate models of power system components and the ability to test actual physical control and protective devices with the software simulations. Multiple contingency studies of complex systems can be done in relatively short time frames using a real-time simulation tool. The real-time simulator used in the studies in this thesis is the Real-Time Digital Simulator from RTDS Technologies in Manitoba, Canada. The RTDS was initially designed for simulating electromagnetic transients in real-time.

The application of real-time simulation to the power system transient solution in general was presented in chapter two. That chapter also considered the advantages and disadvantages of using real-time simulation for time-domain voltage stability analysis. Fundamental concepts related to voltage stability and power system components that play an important role in voltage stability incidents were discussed. The modelling requirements of power system components important for voltage stability studies were also presented. Chapter Two also presented a review of some of the methods that have been used for voltage stability analysis. These methods were seen to be broadly classified into static and dynamic approaches. The advantages and disadvantages of each of these methods of analysis were also discussed. Finally, Chapter Two presented a discussion of the countermeasures against voltage instability. Particular emphasis was placed on the use of switched shunt capacitor compensation, synchronous condenser compensation and static var compensation. Some advantages and disadvantages of each of these methods of voltage stability enhancement were also discussed.

Chapter Three presented RTDS models of the travelling wave transmission line and static load components that have been used in this thesis for voltage stability studies. The chapter also presented the development of real-time models of some of the power system components that are known to play an important role in voltage stability incidents. The

real-time models of power system components developed are a transformer on-load tap changer controller, generator excitation control system with field current limiting function, synchronous condenser and static var compensator reactive power controllers.

In Chapter Four, the development of two real-time models of voltage stability benchmark systems was presented. The development of a small benchmark system and a larger 11-bus benchmark system were presented. The benchmark systems were developed using the custom real-time models of power system components developed in Chapter Three together with generalised power system components provided in the RSCAD software suite. The results of the real-time simulations of the benchmark systems in this thesis have been seen to be in agreement with similar studies done by others on the two systems using other simulation packages.

This thesis then presented an investigation of the use of the real time simulator for assessing methods of voltage stability enhancement. Three methods of voltage stability enhancement were investigated namely, the used of switched shunt capacitor compensation, synchronous condenser compensation and use of a static var compensator. The three different methods of voltage stability enhancement were applied to the 11-bus voltage stability benchmark system at various load levels. Some of the known characteristics of each of the methods of voltage stability control were verified using the real-time digital simulator. The advantages and disadvantages of each of the methods of voltage stability control were also verified on the real-time simulator. The effect of the location of equipment in the power system was also investigated. The investigations showed that the real-time simulator can be used for testing methods of voltage stability control, as well as optimally placing equipment for voltage stability control.

In Chapter Six the use of the real-time simulator for testing a physical control device in closed loop with a simulation for voltage stability studies was presented. A voltage regulating relay known as the REG-DA voltage regulator was tested in closed loop with the 11-bus voltage stability benchmark system simulation on the RTDS. Simulation results of the 11-bus voltage stability benchmark system using an all-software representation of the system were compared with the simulation results involving the REG-DA voltage regulator in closed loop with the simulation. The results of the all-software simulation of the 11-bus voltage stability benchmark system and those of the REG-DA voltage regulator

were seen to be in very close agreement. These results showed that the real-time simulator can be used to test a physical control device in closed loop with the simulation for voltage stability studies.

Suggestions for future work

This thesis has presented real-time voltage stability studies using two benchmark study systems. In both systems, the representation of load characteristics was done using static load models provided in the RSCAD software suite. These static load models provided in RSCAD are capable of representing constant power loads as well as the voltage dependence of loads through the ZIP and the Exponential load components. The thesis did not consider effects of specific dynamic load models such as induction motors and thermostatically controlled loads on voltage stability. The author therefore recommends that further work to model and study the effects of these load types be carried out on the RTDS.

This thesis has in part dealt with testing methods of voltage stability enhancement on the RTDS. The methods that have been investigated in the thesis are use of switched shunt capacitor compensation, synchronous condenser compensation and static var compensation. The thesis has not investigated the effect of other FACTS devices for voltage stability enhancement. It is therefore the author's recommendation that the effect of using other FACTS devices for enhancing voltage stability also be investigated on the RTDS using the benchmark systems developed in this thesis.

Finally, it is also noted that the RSCAD software suite provides a model of HVDC valves. HVDC links have been known to play an important role on power system voltage stability [1]. It is also recommended that an investigation to study the effects of an HVDC link on voltage stability be conducted on the RTDS.

APPENDIX A

SMALL BENCHMARK SYSTEM RSCAD/DRAFT DATA

The following are RSCAD/Draft components and data used for the small voltage stability benchmark system in this thesis.

Component: lf_rtds_sharc_sld_SRC (Infinite bus)

CONFIGURATION

Source Name (Name) = src

Source Impedance Type: (Type) = L

Voltage Input Time Constant (Tc) = 0.05

Zero Sequence Included (ZSeq) = No

Impedance Data Format: (Imp) = RRL Values

Source Wave Type: (WvType) = AC

Souce Control: (Sctrl) = RunTime

Preprocessor Source Impedance ? (PPVar) = No

Requested 3PC Processor (auto = blank) (ReqP) =

POSITIVE SEQUENCE RRL

Resistance (series) (R1s) = 1.0

Resistance (parallel) (R1p) = 1.0

Inductance (parallel) (L1p) = 0.0509

AC SOURCE INITIAL VALUES

Initial Source Mag (L-L, RMS) (Es) = 400.0

Initial Frequency (F0) = 60.0

Initial Phase (Ph) = 0.0

AC SOURCE INITIAL POWER OUTPUT

Load Flow Result: Real power (+ve= out) (P) = 0.231671

Load Flow Result: Reactive power (+ve= out) (Q) = -337.663600

Specified Initial Real power (+ve= out) (Pt) = 100.0

Specified Initial Reactive power (+ve= out) (Qt) = 50.0

Component: lf_rtds_sharc_sld_MACV3 (Bus 2 generator)

GENERAL MODEL CONFIGURATION

Machine name: (Name) = M1

Format of Machine electrical data input: (cnfg) = Generator

Number of Q-axis rotor windings: (cfgr) = One

Is D-axis transfer admittance known ? (trfa) = No

Rated MVA of the Machine: (mmva) = 500.0

Rated RMS Line-to-Line Voltage: (Vbsll) = 22.0

Base Angular Frequency: (HTZ) = 50.0

Specification of Mach Saturation Curve (satur) = Linear

Get Delta Speed Order (r/s) from CC ? (MM) = No

Initial Speed in the first time steps is: (spdin) = Rated

Send Elect Torque in PU, TE to CC ? (tecc) = No

Send Mach Bus V in PU, VMPU to CC ? (vtcc) = Yes

Include Optional Y-D Transformer ? (trfmr) = No

Include Optional Machine Load No. 1 ? (ldmh1) = No

Include Optional Machine Load No. 2 ? (ldmh2) = No

Assignment of Model to 3PC Card (ReqP) = Automatic

-- if Manual: Place on 3PC Card (ShrC) = 1

-- if Manual: Place on 3PC Processor (ShrP) = A

Force FP Output to CC to be IEEE: (ieeeo) = No

If float input type undefined, receive as: (defpi) = BP_MODE

MECHANICAL DATA AND CONFIGURATION

Inertia Constant (H) = 3.5

Synchronous Mechanical Damping (D) = 4.0

Location of Lock/Free Mode Switch: (MSW) = RunTime

-- Initial Mode of Lock/Free Switch (spdmd) = Lock

CC input for External H: EX_H (inh) = No

CC in for Extern Damp: EX_D EX_W (ind) = No

- If (ind=Yes), upper limit on EX_W = (upexw) = 1.15

- If (ind=Yes), lower limit on EX_W = (loexw) = 0.85

MACHINE INITIAL LOAD FLOW DATA

Load Flow: Voltage Magn. at t=0- (Vmagn) = 1.000000

Load Flow: Voltage Phase A sine at t=0- (Vangl) = -0.003758

Load Flow: Real P at t=0- (+ is Out) (P0) = 0.000000

Load Flow: React. P at t=0- (+ is Out) (Q0) = -347.973172

Start Up as Ramped Current Sources: (rmpc) = No

--- Time Constant for Ramping Up: (rmptc) = 0.05

Force initial stator currents to zero ? (iszro) = No

Force all initial currents to zero ? (izro) = No

Specified P at Component Terminal (Pt) = 0.0

Specified Q at Component Terminal (Qt) = 0.0

MACHINE ELECT DATA: GENERATOR FORMAT

Stator Leakage Reactance (Xa) = 0.2

D-axis: Unsaturated Reactance (Xd) = 2.1

D: Unsaturated Transient Reactance (Xd') = 0.4

D: Unsaturated Sub-Trans. Reactance (Xd'') = 0.25

D: Real Component of Transfer Admit. (Gfld) = 100.0

D: Imag Component of Transfer Admit. (Bfld) = 100.0

Q-axis Unsaturated Reactance (Xq) = 2.1

Q: Unsaturated Transient Reactance (Xq') = 0.228

Q: Unsaturated Sub-Trans. Reactance (Xq'') = 0.25

Stator Resistance (Ra) = 0.004

D: Unsat. Transient Open T Const. (Tdo') = 8.0

D: Unsat. Sub-Trans. Open T Const. (Tdo'') = 0.045

Q: Unsat. Transient Open T Const. (Tqo') = 0.85

Q: Unsat. Sub-Trans. Open T Const. (Tqo'') = 0.045

MACHINE ZERO SEQUENCE IMPEDANCES

Machine Zero Sequence Resistance: (Mrzro) = 0.002

Machine Zero Sequence Reactance: (Mxzro) = 0.130

Neutral Series Resistance: (Rneut) = 1.0E5

Neutral Series Reactance: (Xneut) = 0.0

Component: lf_rtds_sharc_sld_TRF3P2W (Transformer between bus 2 and bus 4)

CONFIGURATION

Transformer Name (Trf) = TRF1

Winding #1 Connection (YD1) = Y

Winding #2 Connection (YD2) = Y

Delta lags or leads Y (Lead) = Leads

Transformer Model Type (type) = Linear

Tap Changer (type cannot be Linear) (tapCh) = No

Tap Trigger on (edge) = Rising Edge

Tap Changer Inputs (inps) = RunTime

Transformer rating (3 Phase) (Tmva) = 100

Base Frequency (f) = 50.0

Leakage inductance of Tx (xl) = 0.016

No load losses (NLL) = 0.001

No load loss branch type (NLLtp) = Winding

WINDING #1

Base primary voltage (L-L RMS) (VL1) = 22.0

Magnetizing Current (Im1) = 1.0

WINDING #2

Base secondary voltage (L-L RMS) (VL2) = 416.0

Magnetizing Current (Im2) = 1.0

Component: lf_rtds_sharc_sld_TRF3P2W (Transformer between bus 3 and bus 4)

CONFIGURATION

Transformer Name (Trf) = TRF2

Winding #1 Connection (YD1) = Y

Winding #2 Connection (YD2) = Y

Delta lags or leads Y (Lead) = Leads

Transformer Model Type (type) = Ideal

Tap Changer (type cannot be Linear) (tapCh) = Step/Limit

Tap Trigger on (edge) = Rising Edge

Tap Changer Inputs (inps) = CC

Transformer rating (3 Phase) (Tmva) = 100.0

Base Frequency (f) = 50.0

Leakage inductance of Tx (xl) = 0.004

No load losses (NLL) = 0.001

No load loss branch type (NLLtp) = Winding

WINDING #1

Base primary voltage (L-L RMS) (VL1) = 400.0

Magnetizing Current (Im1) = 1.0

WINDING #2

Base secondary voltage (L-L RMS) (VL2) = 22.0

Magnetizing Current (Im2) = 1.0

TAP CHANGER B

Step size (step) = 0.011363636

Starting Tap Position (TR2) = 1.0

Upper limit (limH) = 1.2273

Lower limit (limL) = 0.909090901

Component: lf_rtds_sharc_sld_SERIESIND (Transmission line between bus 1 and bus 4)

CONFIGURATION

Series Inductance per phase (L) = 0.282

Component: lf_rtds_sharc_sld_SERIESIND (Transmission line between bus 1 and bus 4)

CONFIGURATION

Series Inductance per phase (L) = 0.282

Component: rtds_sharc_ctl_ECL (Dynamic load at bus 4)

PARAMETERS:

Name of Dynamic Load Model (Name) = Load3

Rated Bus Voltage (Vb) = 22.0

Base Frequency (Fb) = 50.0

Bus Voltage Measurement time constant (Tf) = 0.01

Startup Time (TS) = 10.0

Exponential coefficient Kpv (Kpv) = 1.5

Exponential coefficient Kqv (Kqv) = 2.5

Exponential coefficient Kpf (Kpf) = 1.0

Exponential coefficient Kqf (Kqf) = 1.0

Solve Model on card type: (prtyp) = 3PC

Assigned Controls Processor (Proc) = 1

Priority Level (Pri) = 3

Component: rtds_sharcu_RLDload (Exponential load calculator at bus 4)

PARAMETERS:

Component Name (name) = Load3

P & Q Controlled by (cc) = CC

Rated Line to Line Bus Voltage (Vbus) = 22.0

Minimum Bus Voltage(L-L) (Vmin) = 0.5

Base Frequency (freq) = 50

Initial Real Power (Pinit) = 1.0

Minimum Real Power (Pmin) = 0.001

Maximum Real Power (Pmax) = 5000.0

Initial Reactive Power (Qinit) = 1.0

Minimum Reactive Power (Qmin) = 0.001

Maximum Reactive Power (Qmax) = 3000

Time Constant for P & Q (T) = 0.001

Component: lf_rtds_sharc_sld_SHUNTCAP (Shunt compensation at bus 4)

CONFIGURATION

Shunt Capacitance per phase (CuF) = 3945.99

Connection type (type) = Y

Include Neutral Connection Point? (NR) = No

Component: rtds_sharc_sld_BUSLABEL (Bus 1)

Parameters

BUS Name (BName) = BUS1

A Phase Node Name (NA) = N1

B Phase Node Name (NB) = N2

C Phase Node Name (NC) = N3

Rated Line-Line Bus Voltage (VRate) = 400.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = SLACK

Voltage Result (from loadflow) (Vd) = 1.00000

Angle Result (from loadflow) (Ad) = 0.00000

Component: rtds_sharc_sld_BUSLABEL (bus 2)

Parameters

BUS Name (BName) = BUS2

A Phase Node Name (NA) = N4

B Phase Node Name (NB) = N5

C Phase Node Name (NC) = N6

Rated Line-Line Bus Voltage (VRate) = 22.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PV BUS

Voltage Result (from loadflow) (Vd) = 1.00000

Angle Result (from loadflow) (Ad) = -0.00376

Component: rtds_sharc_sld_BUSLABEL (Bus 3)

Parameters

BUS Name (BName) = BUS3

A Phase Node Name (NA) = N7

B Phase Node Name (NB) = N8

C Phase Node Name (NC) = N9

Rated Line-Line Bus Voltage (VRate) = 22.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 1.12042

Angle Result (from loadflow) (Ad) = -0.00348

Component: rtds_sharc_sld_BUSLABEL (Bus 4)

Parameters

BUS Name (BName) = BUS4

A Phase Node Name (NA) = N10

B Phase Node Name (NB) = N11

C Phase Node Name (NC) = N12

Rated Line-Line Bus Voltage (VRate) = 400.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 1.09353

Angle Result (from loadflow) (Ad) = -0.00336

Display bus type in icon? (Dis1) = No

APPENDIX B

ELEVEN-BUS BENCHMARK SYSTEM RSCAD/DRAFT DATA

The following are RSCAD/Draft components and data used for the 11-bus voltage stability benchmark system in this thesis.

B.1 System Data

Component: lf_rtds_sharc_sld_SRC (Infinite bus)

CONFIGURATION

Source Name (Name) = src

Source Impedance Type: (Type) = R

Voltage Input Time Constant (Tc) = 0.05

Zero Sequence Included (ZSeq) = No

Impedance Data Format: (Imp) = RRL Values

Source Wave Type: (WvType) = AC

Souce Control: (Sctrl) = RunTime

POSITIVE SEQUENCE RRL

Resistance (series) (R1s) = 1e-6

Resistance (parallel) (R1p) = 0.00001

Inductance (parallel) (L1p) = 0.000001

AC SOURCE INITIAL VALUES

Initial Source Mag (L-L, RMS) (Es) = 13.8

Initial Frequency (F0) = 60.0

Initial Phase (Ph) = 0.0

AC SOURCE INITIAL POWER OUTPUT

Load Flow Result: Real power (+ve= out) (P) = 4213.181364

Load Flow Result: Reactive power (+ve= out) (Q) = 585.788395

Specified Initial Real power (+ve= out) (Pt) = 100.0

Specified Initial Reactive power (+ve= out) (Qt) = 50.0

Component: lf_rtds_sharc_sld_MACV31 (Generator G2)

GENERAL MODEL CONFIGURATION

Machine name: (Name) = G2

Format of Machine electrical data input: (cnfg) = Generator

Number of Q-axis rotor windings: (cfgr) = Two

Is D-axis transfer admittance known ? (trfa) = No

Rated MVA of the Machine: (mmva) = 2200.0

Rated RMS Line-to-Line Voltage: (Vbsll) = 13.8

Base Angular Frequency: (HTZ) = 60.0

Specification of Mach Saturation Curve (satur) = Linear

Get Delta Speed Order (r/s) from CC ? (MM) = No

Initial Speed in the first time steps is: (spdin) = Rated

Send Elect Torque in PU, TE to CC ? (tecc) = No

Send Mach Bus V in PU, VMPU to CC ? (vtcc) = Yes

Include Optional Y-D Transformer ? (trfmr) = Yes

Include Optional Machine Load No. 1 ? (ldmh1) = No

Include Optional Machine Load No. 2 ? (ldmh2) = No

Solve Model on card type: (prtyp) = GPC

RPC-GPC CONFIGURATION

Request Exclusive Use of a Processor (exclu) = No

Assignment of Model to RPC-GPC Card (AorM) = Automatic

- If Manual: Request RPC-GPC Card (CARD) = 1

- If Manual: Request Processor (Rprc) = A

MECHANICAL DATA AND CONFIGURATION

Inertia Constant (H) = 2.09

Synchronous Mechanical Damping (D) = 0.0

Location of Lock/Free Mode Switch: (MSW) = CC

-- Initial Mode of Lock/Free Switch (spdmd) = Lock

CC input for External H: EX_H (inh) = No

CC in for Extern Damp: EX_D EX_W (ind) = No

- If (ind=Yes), upper limit on EX_W = (upexw) = 1.15

- If (ind=Yes), lower limit on EX_W = (loexw) = 0.85

MACHINE INITIAL LOAD FLOW DATA

Load Flow: Voltage Magn. at t=0- (Vmagn) = 0.964600

Load Flow: Voltage Phase A sine at t=0- (Vangl) = -38.225869

Load Flow: Real P at t=0- (+ is Out) (P0) = 1500.000000

Load Flow: React. P at t=0- (+ is Out) (Q0) = -150.374899

Start Up as Ramped Current Sources: (rmpc) = No

--- Time Constant for Ramping Up: (rmptc) = 0.05

Force initial stator currents to zero ? (iszro) = No

Force all initial currents to zero ? (izro) = No

Specified P at Component Terminal (Pt) = 1736.0

Specified Q at Component Terminal (Qt) = 0.0

MACHINE ELECT DATA: GENERATOR FORMAT

Stator Leakage Reactance (Xa) = 0.155

D-axis: Unsaturated Reactance (Xd) = 2.07

D: Unsaturated Transient Reactance (Xd') = 0.28

D: Unsaturated Sub-Trans. Reactance (Xd'') = 0.215

D: Real Component of Transfer Admit. (Gfld) = 100.0

D: Imag Component of Transfer Admit. (Bfld) = 100.0

Q-axis Unsaturated Reactance (Xq) = 1.99

Q: Unsaturated Transient Reactance (Xq') = 0.49

Q: Unsaturated Sub-Trans. Reactance (Xq'') = 0.215

Stator Resistance (Ra) = 0.0046

D: Unsat. Transient Open T Const. (Tdo') = 4.10

D: Unsat. Sub-Trans. Open T Const. (Tdo'') = 0.033

Q: Unsat. Transient Open T Const. (Tqo') = 0.56

Q: Unsat. Sub-Trans. Open T Const. (Tqo'') = 0.062

MACHINE ZERO SEQUENCE IMPEDANCES

Machine Zero Sequence Resistance: (Mrzro) = 0.002

Machine Zero Sequence Reactance: (Mxzro) = 0.130

Neutral Series Resistance: (Rneut) = 1.0E5

Neutral Series Reactance: (Xneut) = 0.0

TRANSFORMER PARAMETERS

Transformer Primary L-L RMS kV (vtpri) = 540.0

Transformer Secondary L-L RMS kV (vtsec) = 13.2

Delta Leads or Lags Primary 30 Deg. (dlagp) = Lags

Transformer MVA rating (TMVA) = 100.0

Positive Sequence Resistance: (trpos) = 0.0

Positive Sequence Reactance: (txpos) = 0.0045

Is there a TRF zero sequence path ? (itzro) = Yes

-- Zero Sequence Resistance: (trzro) = 0.0

-- Zero Sequence Reactance: (txzro) = 0.0045

Shunt Conductance at TRF Primary: (tloss) = 0.0

OUTPUT OPTIONS

Time Constant of Filter for Powers: (tconp) = 0.02

Time Const of Filter for Max Ph Crt: (tconc) = 0.0

Time Const of Filt for PU Terminal V: (tconv) = 0.0

One Step lead on Machine Currents ? (ledim) = Yes

One Step lead on Machine Bus Voltages ? (ledvm) = Yes

One Step lead on Neutral V and I ? (lednt) = Yes

One Step lead on Transformer Currents ? (ledit) = Yes

INTERNAL BUS PARAMETERS

Rated Voltage (VRate) = 13.8

Initial Bus Voltage (Vi) = 0.9646

Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PV BUS

Voltage Result (from loadflow) (Vd) = 1.0

Angle Result (from loadflow) (Ad) = 1.0

Component: lf_rtds_sharc_sld_MACV31

GENERAL MODEL CONFIGURATION

Machine name: (Name) = G3

Format of Machine electrical data input: (cnfg) = Generator

Number of Q-axis rotor windings: (cfgr) = Two

Is D-axis transfer admittance known ? (trfa) = No

Rated MVA of the Machine: (mmva) = 1400.0

Rated RMS Line-to-Line Voltage: (Vbsll) = 13.8

Base Angular Frequency: (HTZ) = 60.0

Specification of Mach Saturation Curve (satur) = Linear

Get Delta Speed Order (r/s) from CC ? (MM) = No

Initial Speed in the first time steps is: (spdin) = Rated

Send Elect Torque in PU, TE to CC ? (tecc) = No

Send Mach Bus V in PU, VMPU to CC ? (vtcc) = Yes

Include Optional Y-D Transformer ? (trfmr) = Yes

Include Optional Machine Load No. 1 ? (ldmh1) = No

Include Optional Machine Load No. 2 ? (ldmh2) = No

Solve Model on card type: (prtyp) = GPC

RPC-GPC CONFIGURATION

Request Exclusive Use of a Processor (exclu) = No

Assignment of Model to RPC-GPC Card (AorM) = Automatic

- If Manual: Request RPC-GPC Card (CARD) = 1

- If Manual: Request Processor (Rprc) = A

MECHANICAL DATA AND CONFIGURATION

Inertia Constant (H) = 2.33

Synchronous Mechanical Damping (D) = 0.0

Location of Lock/Free Mode Switch: (MSW) = CC

-- Initial Mode of Lock/Free Switch (spdmd) = Lock

CC input for External H: EX_H (inh) = No

CC in for Extern Damp: EX_D EX_W (ind) = No

- If (ind=Yes), upper limit on EX_W = (upexw) = 1.15

- If (ind=Yes), lower limit on EX_W = (loexw) = 0.85

MACHINE INITIAL LOAD FLOW DATA

Load Flow: Voltage Magn. at t=0- (Vmagn) = 0.902500

Load Flow: Voltage Phase A sine at t=0- (Vangl) = -29.999996

Load Flow: Real P at t=0- (+ is Out) (P0) = 0.000000

Load Flow: React. P at t=0- (+ is Out) (Q0) = 1.885788

Start Up as Ramped Current Sources: (rmpc) = No

--- Time Constant for Ramping Up: (rmptc) = 0.05

Force initial stator currents to zero ? (iszro) = No

Force all initial currents to zero ? (izro) = No

Specified P at Component Terminal (Pt) = 1154.0

Specified Q at Component Terminal (Qt) = 0.0

MACHINE ELECT DATA: GENERATOR FORMAT

Stator Leakage Reactance (Xa) = 0.155

D-axis: Unsaturated Reactance (Xd) = 2.07

D: Unsaturated Transient Reactance (Xd') = 0.28

D: Unsaturated Sub-Trans. Reactance (Xd'') = 0.215

D: Real Component of Transfer Admit. (Gfld) = 100.0

D: Imag Component of Transfer Admit. (Bfld) = 100.0

Q-axis Unsaturated Reactance (Xq) = 1.99

Q: Unsaturated Transient Reactance (Xq') = 0.49

Q: Unsaturated Sub-Trans. Reactance (Xq'') = 0.215

Stator Resistance (Ra) = 0.0046

D: Unsat. Transient Open T Const. (Tdo') = 4.10

D: Unsat. Sub-Trans. Open T Const. (Tdo'') = 0.033

Q: Unsat. Transient Open T Const. (Tqo') = 0.56

Q: Unsat. Sub-Trans. Open T Const. (Tqo'') = 0.062

MACHINE ZERO SEQUENCE IMPEDANCES

Machine Zero Sequence Resistance: (Mrzro) = 0.002

Machine Zero Sequence Reactance: (Mxzro) = 0.130

Neutral Series Resistance: (Rneut) = 1.0E5

Neutral Series Reactance: (Xneut) = 0.0

TRANSFORMER PARAMETERS

Transformer Primary L-L RMS kV (vtpri) = 530.0

Transformer Secondary L-L RMS kV (vtsec) = 13.2

Delta Leads or Lags Primary 30 Deg. (dlagp) = Lags

Transformer MVA rating (TMVA) = 100.0

Positive Sequence Resistance: (trpos) = 0.0

Positive Sequence Reactance: (txpos) = 0.0125

Is there a TRF zero sequence path ? (itzro) = Yes

-- Zero Sequence Resistance: (trzro) = 0.0

-- Zero Sequence Reactance: (txzro) = 0.0125

Shunt Conductance at TRF Primary: (tloss) = 0.0

INTERNAL BUS PARAMETERS

Rated Voltage (VRate) = 13.8

Initial Bus Voltage (Vi) = 0.9025

Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PV BUS

Voltage Result (from loadflow) (Vd) = 1.0

Angle Result (from loadflow) (Ad) = 1.0

Component: lf_rtds_sharc_sld_TRF3P2W (Transformer T1)

CONFIGURATION

Transformer Name (Trf) = T1

Winding #1 Connection (YD1) = Y

Winding #2 Connection (YD2) = Y

Delta lags or leads Y (Lead) = Leads

Transformer Model Type (type) = Ideal

Tap Changer (type cannot be Linear) (tapCh) = No

Tap Trigger on (edge) = Rising Edge

Tap Changer Inputs (inps) = RunTime

Transformer rating (3 Phase) (Tmva) = 100.0

Base Frequency (f) = 60.0

Leakage inductance of Tx (xl) = 0.002

No load losses (NLL) = 0.00

No load loss branch type (NLLtp) = Winding

WINDING #1

Base primary voltage (L-L RMS) (VL1) = 13.2

Magnetizing Current (Im1) = 1.0

WINDING #2

Base secondary voltage (L-L RMS) (VL2) = 540.0

Magnetizing Current (Im2) = 1.0

Component: lf_rtds_sharc_sld_TRF3P2W (Transformer T4)

CONFIGURATION

Transformer Name (Trf) = T4

Winding #1 Connection (YD1) = Y

Winding #2 Connection (YD2) = Y

Delta lags or leads Y (Lead) = Leads

Transformer Model Type (type) = Ideal

Tap Changer (type cannot be Linear) (tapCh) = No

Tap Trigger on (edge) = Rising Edge

Tap Changer Inputs (inps) = CC

Transformer rating (3 Phase) (Tmva) = 100.0

Base Frequency (f) = 60.0

Leakage inductance of Tx (xl) = 0.003

No load losses (NLL) = 0.001

No load loss branch type (NLLtp) = Winding

WINDING #1

Base primary voltage (L-L RMS) (VL1) = 533.0

Magnetizing Current (Im1) = 1.0

WINDING #2

Base secondary voltage (L-L RMS) (VL2) = 13.8

Magnetizing Current (Im2) = 1.0

Component: lf_rtds_sharc_sld_TRF3P2W (Transformer T5)

CONFIGURATION

Transformer Name (Trf) = T5

Winding #1 Connection (YD1) = Y

Winding #2 Connection (YD2) = Y

Delta lags or leads Y (Lead) = Leads

Transformer Model Type (type) = Ideal

Tap Changer (type cannot be Linear) (tapCh) = No

Tap Trigger on (edge) = Rising Edge

Tap Changer Inputs (inps) = RunTime

Transformer rating (3 Phase) (Tmva) = 100.0

Base Frequency (f) = 60.0

Leakage inductance of Tx (xl) = 0.0026

No load losses (NLL) = 0.00

No load loss branch type (NLLtp) = Winding

WINDING #1

Base primary voltage (L-L RMS) (VL1) = 540.0

Magnetizing Current (Im1) = 1.0

WINDING #2

Base secondary voltage (L-L RMS) (VL2) = 115.0

Magnetizing Current (Im2) = 1.0

Component: lf_rtds_sharc_sld_TRF3P2W (Transformer T6)

CONFIGURATION

Transformer Name (Trf) = T6

Winding #1 Connection (YD1) = Y

Winding #2 Connection (YD2) = Y

Delta lags or leads Y (Lead) = Leads

Transformer Model Type (type) = Ideal

Tap Changer (type cannot be Linear) (tapCh) = Pos Table

Tap Trigger on (edge) = Rising Edge

Tap Changer Inputs (inps) = CC

Transformer rating (3 Phase) (Tmva) = 100.0

Base Frequency (f) = 60.0

Leakage inductance of Tx (xl) = 0.0010

No load losses (NLL) = 0.00

No load loss branch type (NLLtp) = Winding

WINDING #1

Base primary voltage (L-L RMS) (VL1) = 115

Magnetizing Current (Im1) = 1.0

WINDING #2

Base secondary voltage (L-L RMS) (VL2) = 13.8

Magnetizing Current (Im2) = 1.0

TAP CHANGER A

Number of TAP positions (max=50) (NoTaps) = 33

Starting Tap Position (TR1) = 18

TAP SETTINGS (1-10)

Tap Setting for Position #1 (P1) = 0.909091

Tap Setting for Position #2 (P2) = 0.914286

Tap Setting for Position #3 (P3) = 0.919540

Tap Setting for Position #4 (P4) = 0.924855

Tap Setting for Position #5 (P5) = 0.930233

Tap Setting for Position #6 (P6) = 0.935673

Tap Setting for Position #7 (P7) = 0.941176

Tap Setting for Position #8 (P8) = 0.946746

Tap Setting for Position #9 (P9) = 0.952381

Tap Setting for Position #10 (P10) = 0.958084

TAP SETTINGS (11-20)

Tap Setting for Position #11 (P11) = 0.963855

Tap Setting for Position #12 (P12) = 0.969697

Tap Setting for Position #13 (P13) = 0.975610

Tap Setting for Position #14 (P14) = 0.981595

Tap Setting for Position #15 (P15) = 0.987654

Tap Setting for Position #16 (P16) = 0.993789

Tap Setting for Position #17 (P17) = 1.000000

Tap Setting for Position #18 (P18) = 1.006289

Tap Setting for Position #19 (P19) = 1.012658

Tap Setting for Position #20 (P20) = 1.019108

TAP SETTINGS (21-30)

Tap Setting for Position #21 (P21) = 1.025641

Tap Setting for Position #22 (P22) = 1.032258

Tap Setting for Position #23 (P23) = 1.038961

Tap Setting for Position #24 (P24) = 1.045752

Tap Setting for Position #25 (P25) = 1.052632

Tap Setting for Position #26 (P26) = 1.059603

Tap Setting for Position #27 (P27) = 1.066667

Tap Setting for Position #28 (P28) = 1.073826

Tap Setting for Position #29 (P29) = 1.081081

Tap Setting for Position #30 (P30) = 1.088435

TAP SETTINGS (31-40)

Tap Setting for Position #31 (P31) = 1.095890

Tap Setting for Position #32 (P32) = 1.103448

Tap Setting for Position #33 (P33) = 1.111111

Component: lf_rtds_sharc_sld_TLINE3 (Transmission line between bus 6 and bus 7)

CONFIGURATION

T-Line Name (Name) = 565

T-Line data file Name (tlb) = 56TL2

Monitor I, P or Q (mon) = NO

Component: lf_rtds_sharc_sld_TLINE3 (Transmission line between bus 6 and bus 7)

CONFIGURATION

T-Line Name (Name) = 564

T-Line data file Name (tlb) = 56TL2

Component: lf_rtds_sharc_sld_TLINE3 (Transmission line between bus 6 and bus 7)

CONFIGURATION

T-Line Name (Name) = 563

T-Line data file Name (tlb) = 56TL2

Component: lf_rtds_sharc_sld_TLINE3 (Transmission line between bus 6 and bus 7)

CONFIGURATION

T-Line Name (Name) = 562

T-Line data file Name (tlb) = 56TL2

Component: lf_rtds_sharc_sld_TLINE3 (Transmission line between bus 6 and bus 7)

CONFIGURATION

T-Line Name (Name) = 561

T-Line data file Name (tlb) = 56TL2

T-Line 56TL2 data:

Positive sequence series resistance / km (ohms): 0.18547

Positive sequence series inductive reactance / km (ohms): 0.37661

Positive sequence shunt capacitive reactance (Mohms)*km: 0.2279

Zero sequence series resistance / km (ohms): 0.3618376

Zero sequence series inductive reactance / km (ohms): 1.227747

Zero sequence shunt capacitive reactance (Mohms)*km: 0.34514

Line length (km): 200

Component: lf_rtds_sharc_sld_SERIESRLC (Transmission line between bus 9 and bus 10)

CONFIGURATION

Series Resistance per phase (R) = 0.13225

Series Inductance per phase (L) = 0.001052412

Series Capacitance per phase (CuF) = 0.0

Component: lf_rtds_sharc_sld_SERIESIND (Transmission line between bus 5 and bus 6)

CONFIGURATION

Series Inductance per phase (L) = 0.02652582384

Component: rtds_sharc_sld_BUSLABEL (Bus 1)

Parameters

BUS Name (BName) = BUS1

A Phase Node Name (NA) = N1

B Phase Node Name (NB) = N2

C Phase Node Name (NC) = N3

Rated Line-Line Bus Voltage (VRate) = 13.8

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 0.98

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = SLACK

Voltage Result (from loadflow) (Vd) = 0.98000

Angle Result (from loadflow) (Ad) = 0.00000

Display bus type in icon? (Dis1) = No

Component: rtds_sharc_sld_BUSLABEL (Bus 5)

Parameters

BUS Name (BName) = BUS5

A Phase Node Name (NA) = N13

B Phase Node Name (NB) = N14

C Phase Node Name (NC) = N15

Rated Line-Line Bus Voltage (VRate) = 500.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 1.09856

Angle Result (from loadflow) (Ad) = -3.97496

Component: rtds_sharc_sld_BUSLABEL (Bus 6)

Parameters

BUS Name (BName) = BUS6

A Phase Node Name (NA) = N16

B Phase Node Name (NB) = N17

C Phase Node Name (NC) = N18

Rated Line-Line Bus Voltage (VRate) = 500.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 1.09876

Angle Result (from loadflow) (Ad) = -12.00077

Display bus type in icon? (Dis1) = No

Component: rtds_sharc_sld_BUSLABEL (Bus 7)

Parameters

BUS Name (BName) = BUS7

A Phase Node Name (NA) = N19

B Phase Node Name (NB) = N20

C Phase Node Name (NC) = N21

Rated Line-Line Bus Voltage (VRate) = 500.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 1.11513

Angle Result (from loadflow) (Ad) = -27.37849

Component: rtds_sharc_sld_BUSLABEL (Bus 8)

Parameters

BUS Name (BName) = BUS8

A Phase Node Name (NA) = N22

B Phase Node Name (NB) = N23

C Phase Node Name (NC) = N24

Rated Line-Line Bus Voltage (VRate) = 13.8

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.01

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 1.04597

Angle Result (from loadflow) (Ad) = -32.44655

Display bus type in icon? (Dis1) = No

Component: rtds_sharc_sld_BUSLABEL (Bus 9)

Parameters

BUS Name (BName) = BUS9

A Phase Node Name (NA) = N25

B Phase Node Name (NB) = N26

C Phase Node Name (NC) = N27

Rated Line-Line Bus Voltage (VRate) = 115.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 1.03733

Angle Result (from loadflow) (Ad) = -32.27503

Component: rtds_sharc_sld_BUSLABEL (Bus 10)

Parameters

BUS Name (BName) = BUS10

A Phase Node Name (NA) = N28

B Phase Node Name (NB) = N29

C Phase Node Name (NC) = N30

Rated Line-Line Bus Voltage (VRate) = 115.0

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 0.96793

Angle Result (from loadflow) (Ad) = -37.52138

Component: rtds_sharc_sld_BUSLABEL (Bus 11)

Parameters

BUS Name (BName) = BUS11

A Phase Node Name (NA) = N31

B Phase Node Name (NB) = N32

C Phase Node Name (NC) = N33

Rated Line-Line Bus Voltage (VRate) = 13.8

Send Voltage(s) to D/A? (3PC Net only) (daout) = No

Bus Color (sld mode) (COL) = RED

Bus Line Width (sld mode) (LW) = 3

LOAD FLOW DATA

Variable name or Number for Initial Bus Voltage (Vi) = 1.0

Variable name or Number for Initial Bus Angle (Ai) = 0.0

Bus Type (Type) = PQ BUS

Voltage Result (from loadflow) (Vd) = 0.96793

Angle Result (from loadflow) (Ad) = -37.52138

B.2 Load Data

Load level 1

Bus 8

Component: rtds_udc_DYLOAD

PARAMETERS

Component Name (name) = Load8

Type of Load (type) = RL

P & Q Controlled by (cc) = Slider

Rated Line to Line Bus Voltage (Vbus) = 13.8

Minimum Bus Voltage(L-L) (Vmin) = 0.5

Base Frequency (freq) = 60

Initial Real Power (Pinit) = 3271.0

Minimum Real Power (Pmin) = 0.1

Maximum Real Power (Pmax) = 10000

Initial Reactive Power (Qinit) = 1015.0

Minimum Reactive Power (Qmin) = 0.1

Maximum Reactive Power (Qmax) = 10000

Bus 11

Component: rtds_sharc_ctl_ZIP

PARAMETERS:

Name of Dynamic Load Model (Name) = Load11

P,Q Input source (SorC) = Constant

Rated Bus Voltage (Vb) = 13.8

Bus Voltage Measurement time constant (Tf) = 0.01

Startup Time (TS) = 30.0

Total Real Power Order (Po) = 3751.0

Total Reactive Power Order (Qo) = 1072.0

Constant Real Impedance fraction (ZP) = 50.0

Constant Real Current fraction (IP) = 50.0

Constant Real MVA fraction (PP) = 0.0

Constant Reactive Impedance fraction (ZQ) = 50.0

Constant Reactive Current fraction (IQ) = 50.0

Constant Reactive MVA fraction (PQ) = 0.0

Solve Model on card type: (prtyp) = 3PC

Assigned Controls Processor (Proc) = 1

Priority Level (Pri) = 1

Component: rtds_udc_DYLOAD

PARAMETERS

Component Name (name) = Load11

Type of Load (type) = RL

P & Q Controlled by (cc) = CC

Rated Line to Line Bus Voltage (Vbus) = 13.8

Minimum Bus Voltage(L-L) (Vmin) = 0.8

Base Frequency (freq) = 60

Initial Real Power (Pinit) = 3384

Minimum Real Power (Pmin) = 0.1

Maximum Real Power (Pmax) = 10000

Initial Reactive Power (Qinit) = 971

Minimum Reactive Power (Qmin) = 0.1

Maximum Reactive Power (Qmax) = 10000

MONITORING

Monitor measured real power? (pPmon) = Yes

Name for measured real power (nPmon) = Pmon11

Monitor measured reactive power? (pQmon) = Yes

Name for measured reactive power (nQmon) = Qmon11

Time Constant for P & Q meas. (T) = 0.01

Load level 2

Bus 8

Component: rtds_udc_DYLOAD

PARAMETERS

Component Name (name) = Load8

Type of Load (type) = RL

P & Q Controlled by (cc) = Slider

Rated Line to Line Bus Voltage (Vbus) = 13.8

Minimum Bus Voltage(L-L) (Vmin) = 0.5

Base Frequency (freq) = 60

Initial Real Power (Pinit) = 3320.0

Minimum Real Power (Pmin) = 0.1

Maximum Real Power (Pmax) = 10000

Initial Reactive Power (Qinit) = 1030.0

Minimum Reactive Power (Qmin) = 0.1

Maximum Reactive Power (Qmax) = 10000

Bus 11

Component: rtds_sharc_ctl_ZIP

PARAMETERS:

Name of Dynamic Load Model (Name) = Load11

P,Q Input source (SorC) = Constant

Rated Bus Voltage (Vb) = 13.8

Bus Voltage Measurement time constant (Tf) = 0.01

Startup Time (TS) = 30.0

Total Real Power Order (Po) = 3779.5

Total Reactive Power Order (Qo) = 1083.9

Constant Real Impedance fraction (ZP) = 50.0

Constant Real Current fraction (IP) = 50.0

Constant Real MVA fraction (PP) = 0.0

Constant Reactive Impedance fraction (ZQ) = 50.0

Constant Reactive Current fraction (IQ) = 50.0

Constant Reactive MVA fraction (PQ) = 0.0

Solve Model on card type: (prtyp) = 3PC

Assigned Controls Processor (Proc) = 1

Priority Level (Pri) = 1

Component: rtds_udc_DYLOAD

PARAMETERS

Component Name (name) = Load11

Type of Load (type) = RL

P & Q Controlled by (cc) = CC

Rated Line to Line Bus Voltage (Vbus) = 13.8

Minimum Bus Voltage(L-L) (Vmin) = 0.8

Base Frequency (freq) = 60

Initial Real Power (Pinit) = 3435.0

Minimum Real Power (Pmin) = 0.1

Maximum Real Power (Pmax) = 10000

Initial Reactive Power (Qinit) = 985.0

Minimum Reactive Power (Qmin) = 0.1

Maximum Reactive Power (Qmax) = 10000

Load level 3

Bus 8

Component: rtds_udc_DYLOAD

PARAMETERS

Component Name (name) = Load8

Type of Load (type) = RL

P & Q Controlled by (cc) = Slider

Rated Line to Line Bus Voltage (Vbus) = 13.8

Minimum Bus Voltage(L-L) (Vmin) = 0.5

Base Frequency (freq) = 60

Initial Real Power (Pinit) = 3345.0

Minimum Real Power (Pmin) = 0.1

Maximum Real Power (Pmax) = 10000

Initial Reactive Power (Qinit) = 1038

Minimum Reactive Power (Qmin) = 0.1

Maximum Reactive Power (Qmax) = 10000

Bus 11

Component: rtds_sharc_ctl_ZIP

PARAMETERS:

Name of Dynamic Load Model (Name) = Load11

P,Q Input source (SorC) = Constant

Rated Bus Voltage (Vb) = 13.8

Bus Voltage Measurement time constant (Tf) = 0.01

Startup Time (TS) = 30.0

Total Real Power Order (Po) = 3952

Total Reactive Power Order (Qo) = 1135.785

Constant Real Impedance fraction (ZP) = 50.0

Constant Real Current fraction (IP) = 50.0

Constant Real MVA fraction (PP) = 0.0

Constant Reactive Impedance fraction (ZQ) = 50.0

Constant Reactive Current fraction (IQ) = 50.0

Constant Reactive MVA fraction (PQ) = 0.0

Solve Model on card type: (prtyp) = 3PC

Assigned Controls Processor (Proc) = 1

Priority Level (Pri) = 1

Component: rtds_udc_DYLOAD

PARAMETERS

Component Name (name) = Load11

Type of Load (type) = RL

P & Q Controlled by (cc) = CC

Rated Line to Line Bus Voltage (Vbus) = 13.8

Minimum Bus Voltage(L-L) (Vmin) = 0.8

Base Frequency (freq) = 60

Initial Real Power (Pinit) = 3460

Minimum Real Power (Pmin) = 0.1

Maximum Real Power (Pmax) = 10000

Initial Reactive Power (Qinit) = 993

Minimum Reactive Power (Qmin) = 0.1

Maximum Reactive Power (Qmax) = 10000

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