# DESIGN AND ANALYSIS OF CYLINDRICAL SURROUNDING DOUBLE GATE MOSFET USING GATE STACKED TRIPLE MATERIAL

*Thesis submitted for the fulfillment of requirements for the degree of:*

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in

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by

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# Declaration

## DESIGN AND ANALYSIS OF CYLINDRICAL SURROUNDING DOUBLE GATE MOSFET USING GATE STACKED TRIPLE MATERIAL

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*This thesis submitted in fulfillment of the requirements for the degree of Doctor of Philosophy: Electronic Engineering in Howard College of Agriculture, Engineering Science University of KwaZulu-Natal, Durban South Africa.*

As the candidate's supervisor, I have approved this thesis for submission.

Signed [redacted]

Date: 28 Aug. 2024

Prof. (Dr.) Viranjay M. Srivastava

# Declaration - Plagarism

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# Publications

An outline of the CONTRIBUTIONS MADE TO PUBLICATIONS that are integral to, or encompass, the research presented in this thesis is provided below. The research presented here has resulted in the publication of the following journal papers.

**Journal Publication**

1. **Uchechukwu Anthony Maduagwu** and Srivastava Viranjay M. "Channel length scaling pattern for cylindrical surrounding double-gate (CSDG) MOSFET." IEEE Access. vol. 8, no 4, pp. 121204-121210, July 2020 (included in chapter 3).

2. **Uchechukwu Anthony Maduagwu** and Srivastava, Viranjay .M. "Assessment of quantum scaling length model for cylindrical surrounding double-gate (CSDG) MOSFET." Micro and Nanosystems, vol 13, no. 4, pp.467-472, July 2021 (included in chapter 4).

3. **Uchechukwu Anthony Maduagwu** and Srivastava, Viranjay .M.,"Sensitivity of Lightly and Heavily Dopped Cylindrical Surrounding Double-Gate (CSDG) MOSFET to Process Variation." IEEE Access, vol 9, no 4, pp.142541-142550, October 2021 (included in chapter 5).

4. **Uchechukwu Anthony Maduagwu** and Srivastava, Viranjay .M.," Design and Analytical model of STacked triple-material gate CSDG MOSFET." IEEE Access (To be submitted) (included in Chapter 6).

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# *Abstract*

The advancement of Very Large-Scale Integration (VLSI) and nanotechnology systems has been significantly driven by the miniaturization of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) devices. Moore's Law substantiates this trend, affirming that "the quantity of transistors integrated into a semiconductor device or chip approximately doubles every two years." The principal objectives of transistor scaling are to enhance functionality, packing density, switching speed, and operational power of integrated circuits (ICs). With the technological advancement below the 100 nm regime, conventional MOSFETs appear to be of little use for scaling because of Short Channel Effects(SCEs). These SCEs encompass threshold roll-off, Drain-Induced Barrier Lowering (DIBL), surface scattering, velocity saturation, mobility degradation, and the hot carrier effect. Other effects include oxide gate tunneling and process variation. These effects contribute to the deterioration of device performance. Consequently, unconventional devices are essential to meet the goals of the International Technology Roadmap for Semiconductors (ITRS). These non-conventional devices, such as Silicon-On-Insulator (SOI) substrate gates, double gates, triple gates, surrounding gates, and double surrounding gates, uphold Moore's law. Among these unconventional MOSFETs, the double surrounding gates' solution has a promising future.

The only MOSFET category under the double surrounding gate is known as the Cylindrical Surrounding Double Gate (CSDG) MOSFETs, which was proposed a few years ago. The CSDG is a MOSFET device structure with a hollow cylindrical structure. In relation to the source, drain, gate, and channel, it exhibits similarities with both traditional MOSFETs and non-conventional Cylindrical Surrounding Gate (CSG) MOSFETs. However, the channel, on the other hand, is controlled by both the internal and external gates. The primary function of the two gates is to provide electrical shielding against the lateral electric field generated by the charges in the drain and source regions. Furthermore, numerous research studies have been undertaken utilizing this device architecture.

The natural length varies from different MOSFET structures to the other, and It aids in characterizing the potential distribution within the Silicon substrate. In this thesis, the authors proposed a natural length scaling pattern for measuring the degree of SCEs of CSDG MOSFETs, which will guide the device design. This was done by solving the Poisson equation of the cylindrical structure using the Parabolic Potential Approximation (PPA) model at the radial part of the device structure. The natural length was

derived and compared with other device geometrical structures and validated with numerical structure. Moreover, the determined intrinsic length was employed to anticipate the threshold voltage response of the device configuration.

In addition, a quantum scaling length for CSDG MOSFET was developed within the Silicon body thickness to investigate the degree of fluctuation of the device structure and to provide design guidelines for the device structure. The authors conducted the analysis using a unified quantum model that considered the lowest electron energy level as the reference point. The relationship between the quantum scaling length and natural scaling length of CSDG MOSFET was proposed. Also, the space confinement known as the quantum scaling factor was analyzed based on the variation in threshold voltage. The results obtained are in good agreement with numerical simulation.

Furthermore, the solution to the Poisson equation is investigated, and the Silicon-oxide is replaced with high-k dielectric to analyze the CSDG MOSFET's sensitivity to process variation for both lightly and heavily doped device structure. The device's immunity to channel variation was analyzed. Also, Random Dopant Fluctuations (RDFs), which severely affect non-conventional devices, was investigated. The model is juxtaposed with CSG structure, and the assessment of the threshold voltage's susceptibility to parameter variations is further scrutinized with a focus on RDFs. The results obtained demonstrated excellent consistency with numerical simulations.

Ultimately, the analytical approach employed for deducing the natural length of CSDG MOSFET is extended to apply to the surface potential, allowing for the modeling of a triple-gate material variant of CSDG MOSFET with hetero-dielectric oxide. In this model, the concepts of metal gate engineering and oxide engineering have been integrated with CSDG MOSFET to suppress SCEs further. The newly proposed Stacked Triple Material Gate (STMG) CSDG MOSFET adjusts the performance matrices of the CSDG MOSFET to provide better performance at the deep sub-22 nm technology node. A 2-D analytical model for STMG CSDG MOSFET has been formulated and introduced. This model is established by solving the 2-D Poisson equation with the utilization of the PPA approach. The developed surface potential is utilized in the development of the threshold voltage model for STMG CSDG MOSFETs and the derivation of DIBL. The model was then used to estimate the subthreshold drain current and further enhance the subthreshold swing. The results show that STMG CSDG MOSFET improves the SCEs characteristics. The numerical simulation is in accordance with the analytical model.

## *Dedication*

*This thesis is dedicated to the Supreme Creator and my deceased parents.*

*I want to thank God Almighty for this study project. God has always been trustworthy to me. Throughout this journey, His love, compassion, and favour have been immeasurable to me. Without his leadership and protection, the whole initiative would have failed.*

*Furthermore, it is impossible to convey the depth of my affection for my late parents. I yearn for more time with you before your departure. May your spirits find eternal peace. I am grateful to you for giving me life. Farewell, Mom. Farewell, Dad, who departed while I was pursuing my PhD.*

# *Acknowledgements*

I express my gratitude to the Divine for His blessings and the precious gift of life.

I extend my heartfelt appreciation to Professor (Dr.) Viranjay M. Srivastava, my supervisor, for his invaluable guidance, mentorship, unwavering support, and remarkable patience during both my MSc and PhD studies. His profound wisdom, unwavering professionalism, vast expertise, and exceptional kindness have been of immeasurable value to me.

I want to specially thank Peace Ohonsi and Ifi families for their unwavering support and encouragement.

I would also like to express my gratitude to the dedicated faculty members and research peers at Howard College, University of KwaZulu-Natal, Durban, South Africa. Their valuable contributions to my research, in the form of guidance, motivation, and support, have been instrumental.

This research project would not have been achievable without the unwavering support of those who surrounded me. I am deeply appreciative of all my academic mentors, friends, and colleagues, including Oyedeji Okikioluwa, Dr. Kolawole Bamidele, and numerous others.

# Contents

# List of Figures

# List of Tables

# Abbreviations

| | |
|---|---|
| **1-D** | **O**ne **D**imension |
| **2-D** | **T**wo **D**imension |
| **3-D** | **T**hree **D**imension |
| **CPU** | **C**entral **P**rocessing **U**nit |
| **PDE** | **P**atial **D**ifferential **E**quation |
| **DG** | **D**ouble **G**ate |
| **BJT** | **B**ipolar **J**unction **T**ransistor |
| **BOX** | **B**uried **O**xide |
| **CFS** | **C**onstant **F**ield **S**caling |
| **CMOS** | **C**omplementary **M**etal **O**xide **S**emiconductor |
| **CSDG** | **C**ylindrical **S**urrounding **D**ouble **G**ate |
| **CSG** | **C**ylindrical **S**urrounding **G**ate |
| **CVS** | **C**onstant **V**oltage **S**caling |
| **DIBL** | **D**rain **I**nduced **B**arrier **L**owering |
| **DMG** | **D**ouble **M**aterial **G**ate |
| **EMA** | **E**vanescent **M**ode **A**nalysis |
| **ENIAC** | **E**lectronic **N**umerical **I**ntegrator and **C**omputer |
| **FDSOI** | **F**ully **D**epleted **S**ilicon **O**n **I**nsulator |
| **GAA** | **G**ate **A**ll **A**round |
| **GSF** | **G**eneralized **S**calling **F**actor |
| **HCEs** | **H**OT **C**arrier - **E**ffects |
| **IC** | **I**ntegrated **C**ircuit |
| **IOT** | **I**nternet **O**f **T**hings |
| **IT** | **I**nformation **T**echnology |
| **ITRS** | **I**nternational **T**echnology **R**oadmap for **S**emiconductors |

| | |
|---|---|
| **LCD** | **L**iquid **C**rystal **D**isplay |
| **MOS** | **M**etal **O**xide **S**emiconductor |
| **MOSFET** | **M**etal - **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistors |
| **PPA** | **P**arabolic **P**otential **A**pproximation |
| **PCs** | **P**ersonal **C**omputers |
| **QMEs** | **Q**uantum **M**echanical **E**ffects |
| **RDFs** | **R**andom **D**opant **F**luctuations |
| **SCEs** | **S**hort **C**hannel **E**ffects |
| **SDMG** | **S**tacked **D**ouble **M**aterial **G**ate |
| **SG** | **S**urrounding **G**ate |
| **SOD** | **S**econd **O**rder **D**ifferentiation |
| **SOI** | **S**ilicon **O**n **I**nsulator |
| **SMSG** | **S**ingle **M**aterial **S**urrounding **G**ate |
| **STMG** | **S**tacked **T**ripple **M**aterial **G**ate |
| **TMG** | **T**riple **M**aterial **G**ate |
| **VLSI** | **V**ery **L**arge **S**cale **I**ntegration |

# Chapter 1

# Introduction

## 1.1 Semiconductor Technological Trend

The invention of Transistors (semiconductor devices) by William Shockley, Walter Brattain, and John Barden at Bells Laboratory in the late 1940s and the creation of the first Integrated Circuits (ICs) by Jack Kilby in 1958 at Texas Instruments brought humanity to the era of solid-state electronics. The emergence of this new technology ignited the evolution of Information Technology (IT), which led to the creation of the first microprocessor in a computer called the Electronic Numerical Integrator and Computer (ENIAC) as shown in Figure 1.1. Besides the invention of semiconductor devices, no

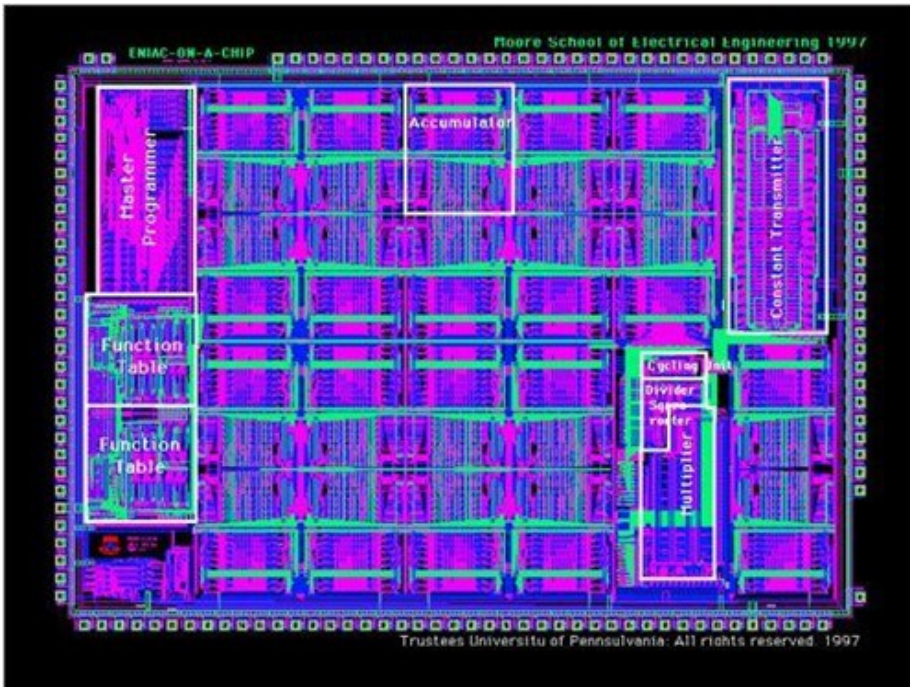


FIGURE 1.1: Intel Duo Core Process of ENIAC [1].

other invention has drastically changed human life since the invention of electricity. The semiconductor invention encompasses all fields of science and technology. Semiconductor device technology has developed at a fantastic speed. Consumers' consistent demand for better, faster, and cheaper electronics has been the driving force for such a tremendous change.

The semiconductor industries and researchers have played an exponential role in the constant development of semiconductor devices through IC designs. The Complementary Metal-Oxide Semiconductor (CMOS) technology used in transistors to manufacture the IC depends solely on a unipolar transistor called MOSFET. The process used in producing these ICs is known as the Very Large Scale Integration (VLSI) technology, in which billions of transistors are integrated into a single chip.

Over the past 20th century, the core element of the VLSI design, the MOSFET transistor, was downsized to the submicron level and eventually to the nanometer scale. The main reason for the scaling of the device size is to increase the number of transistors integrated into a single chip, increase speed, and decrease the operating voltage.

## 1.2 MOSFETs

Unlike Bipolar Junction Transistors (BJT) that show delay switching characteristics, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) remain the workhorse in modern electronics because of their perfect isolation between their terminals [2]. It

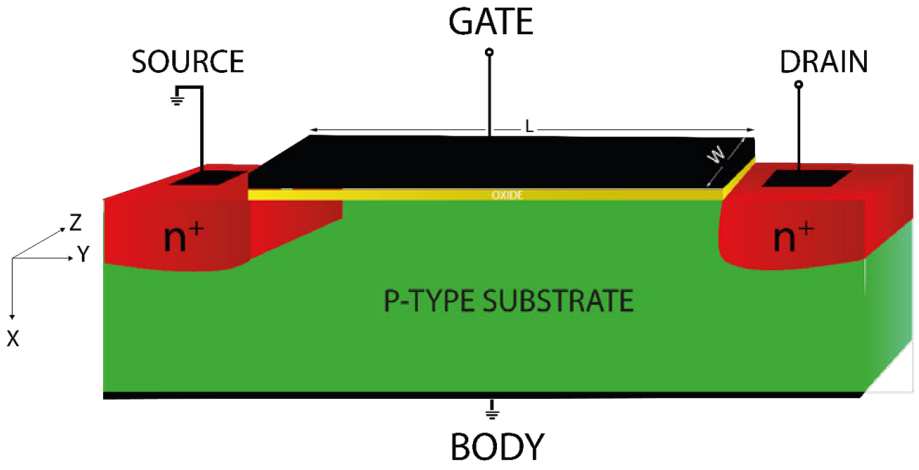


FIGURE 1.2: Conventional MOSFET Structure.

is also an underlying technology for digital logic and LCDs. MOSFETs are generally voltage-controlled electronic devices with high input resistance. These devices feature four terminals, specifically the body, source (S), gate (G), and drain (D), as illustrated

in Figure 1.2. The Silicon body (substrate) is assumed to have the same potential as the source, which made the conventional MOSFETs have three operational terminals [3].

The metal gate (G), which was later replaced with a polysilicon electrode, is separated from the semiconductor body, either N-type or P-type substrate, by a dielectric polysilicon material called Silicon dioxide (SiO2), the yellow colour in Figure 1.2. The heavily doped n-type regions consist of the source (S) and drain (D).

## 1.3 The Physics of MOS Structure – Long Channel Approximation

The MOS (Metal Oxide Semiconductor) capacitor is an excellent introduction to MOSFETs because it simplifies the analysis of the effects of the gate (G) electrode on the substrate without complicating current flow or the electric field effect. Even with DC bias applied, the MOS capacitor is always in thermal equilibrium.

Consider a P-type substrate, in which the majority of the carriers are holes, and the Fermi level of Silicon ($E_f$) is in the lower half of the energy bandgap [4]. Figure 1.3 shows the distinct situations that take place in MOS devices before the formation of a channel when a bias voltage is applied to the Gate. The silicon bands are flat, right up to the silicon-dioxide interface, because of zero net charges. Silicon remains electrically neutral, as the presence of holes (+) perfectly counterbalances the acceptor dopant ions (—). The biasing applied voltage ($V_G$) at which the zero net charges occur is called the flatband voltage ($V_{FB}$). As the biasing positive voltage exceeds the flatband voltage, the positive holes are repelled from the silicon substrate's surface, and the holes density keeps decreasing down the silicon as the biasing voltage increases. The surface becomes completely depleted of charges at a specific gate voltage (threshold voltage, $V_{TH}$). The energy band bends down because of the uncovered negative charges, as shown in the energy diagram in Figure 1.3c. Increasing the gate voltage beyond the threshold voltage triggers the formation of an inversion layer. This layer comprises electrons sourced from the source (or drain) and establishes a conductive path, commonly referred to as a "channel," connecting the source and drain, red as shown in Figure 1.3d. As a result, the energy band bends further downward due to more uncovered negative charges at the surface. When the gate-source voltage surpasses $V_{TH}$ by a margin of several thermal voltages ($kT/q$), the device is considered to be in a state of strong inversion [5].

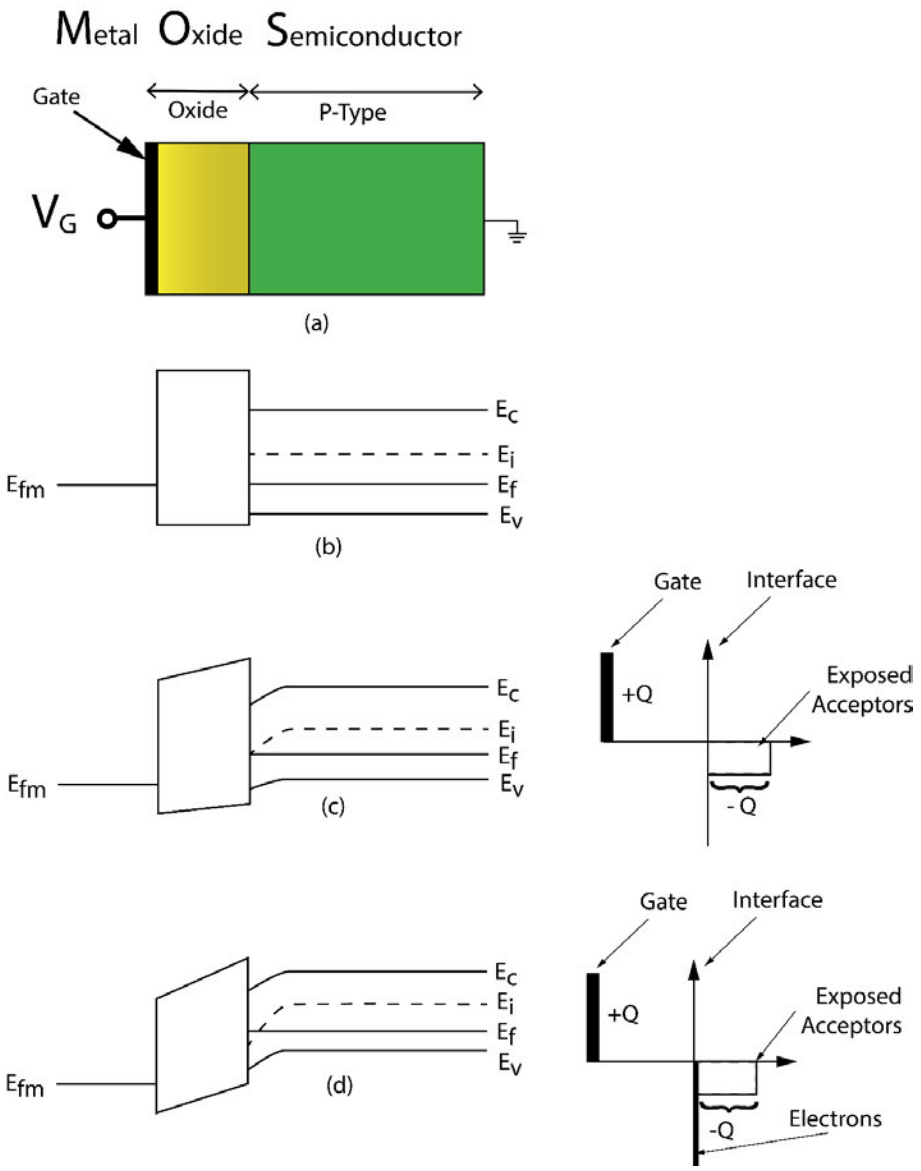


FIGURE 1.3: Energy Band bending in MOS for various biases: (a) MOS Structure (b) Flatbands c) Depletion and its Charge Distribution (d) Inversion and its Charge Distribution. $E_c$ = conduction band, $E_v$ = valence band, $E_i$ = Intrinsic level, $E_f$= Femi level of silicon, and $E_{fm}$ = Female level of Gate [6].

## 1.4 Scaling

The desire for higher performance, which is expected either exclusively for scientific purposes, medical applications, or commercial applications such as smartwatches, calculators, PCs, play machines, mobile phones, and laptops, is driving the advancement of the IC architecture. The higher performance should be able to adapt to three distinct requirements:

1. Cost Reduction.

2. Size Reduction, and

3. Reduction in Energy usage

All three are interdependent on each other. As a result of the economic constraints, Silicon won out over germanium as the primary material for basic transistors. Meanwhile, the basic principle of downscaling the ICs is to reduce its size (increase circuit speed and packing density) and energy usage (decrease the power dissipation). Therefore, MOSFET scaling becomes crucial for the present and future technological nodes.

### 1.4.1 MOSFET Scaling

During the 1960s, Gordon Moore observed that the number of transistors on a chip doubled approximately every 18 months [7]. That discovery, known as "Moore's Law," describes the consistent periodic increase in miniaturization. A new technological generation or node is introduced each time the minimum line width is decreased. Dennard et al. [8] introduced a scaling theory aimed at downsizing the conventional MOSFET to uphold Moore's law. Figure 1.4 illustrates the basic idea of MOSFETs scaling.

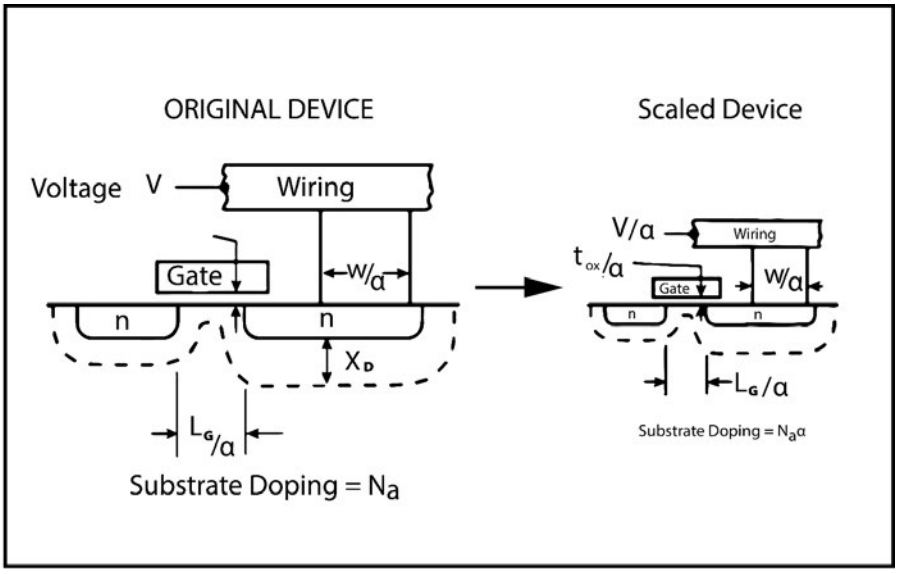


FIGURE 1.4: Basic Idea of MOSFET Scaling [9].

The work of [10] became the industry standard in the semiconductor industry. In the early stages of integrated circuits, it provided guidance for MOSFET design, circuit design, and chip design. Figure 1.5 illustrates the most recent update to Moore's law, which encompasses the introduction of the world's first CPU featuring 2 billion transistors.

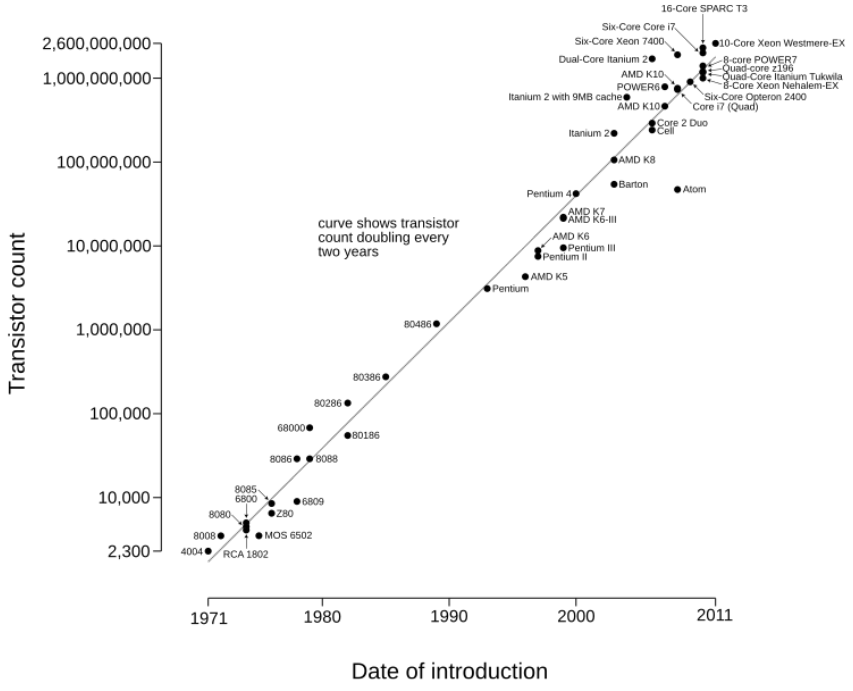


FIGURE 1.5: Transistors Integration according to Moor's Law [11].

### 1.4.2 MOSFET Scaling Mechanism

As a result, the process of scaling has consistently been guided by a limited set of methodologies with specific application objectives. These methodologies rely on the assumptions of (i) reducing the device's dimensions through improvements in lithography and (ii) preserving the fundamental structure of the MOS transistor.

The size of a MOSFET is scaled through the utilization of the scaling parameter $\alpha$ ($\alpha > 1$). There are three types of scaling mechanisms, namely, constant voltage scaling (CVS), constant field scaling (CFS), and generalized scaling factor (GSF), as shown in Table 1.1. In the latter, $\alpha$ is a dimensionless scaling factor, and it has a value that is larger than one ($\alpha > 1$). In CVS, the dimensions are reduced by a factor of $\alpha$, the drain current and power densities are increased by $\alpha$, and the electric field magnitude increases by $\alpha$. So, the constant voltage scaling mechanism decreases the MOSFET dimension by a scale factor of $\alpha$ except for the supply power and terminal voltage. However, the major shortcoming lies with the increased electric field as the MOSFET is downscaled. CFS, known as the full scaling mechanism, is a method of scaling in which the electric field magnitude is unaffected while all the power supply and terminal voltages are reduced with all other dimensions. However, the reduction in voltages may not be feasible in many cases. The peripheral and interface circuits may demand a specific voltage level for

all output and input voltages. This requirement will necessitate multiple power supply voltages and intricate level–shifter arrangements.

Table 1.1: MOSFET scaling mechanism with its parameter [12]

| Parameter | Symbol | Constant Voltage Scaling (CVS) | Constant Field Scaling (CFS) | Generalized Scaling Factor (GSF) |
|---|---|---|---|---|
| Gate Length | $L_G$ | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ |
| Current | $I$ | $\alpha$ | $1/\alpha$ | $\alpha$ |
| Gate Capacitance | $C_G$ | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ |
| Electric Field | $E$ | $\alpha$ | 1 | $\epsilon$ |
| Oxide Capacitance | $C_{ox}$ | $\alpha$ | $\alpha$ | $\alpha$ |
| Transit Frequency | $t_\tau$ | $\alpha^2$ | $\alpha$ | $\epsilon\alpha^2$ |
| Transit Time | $f_\tau$ | $1/\alpha^2$ | $1/\alpha^2$ | $1/\alpha^2$ |
| Gate Width | $W$ | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ |
| Voltage | $V$ | 1 | $1/\alpha$ | 1 |
| Power | $P$ | $\alpha$ | $1/\alpha^2$ | $\epsilon^2\alpha^2$ |
| Oxide Thickness | $t_{ox}$ | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ |
| Power Delay | $P\Delta t$ | $1/\alpha$ | $1/\alpha^3$ | $1/\alpha^3$ |
| Substrate Doping | $Na$ | $\alpha^2$ | $\alpha^2$ | $\epsilon\alpha^2$ |

GSF shows that the scaling factor for geometrical feature sizes and potentials need not be identical. By designating $\alpha$ as the scaling factor for the dimensions and the scaling factor for the potential, the trade-off between circuit downsizing and performance may be optimized.

far as ICs are concerned, the adage, "small is beautiful," holds true. Scaling is anticipated to persist. However, what obstacles might hinder further scaling? Is it possible for scaling to continue indefinitely?

## 1.5 Scaling Challenges

The remarkable advancement in microelectronics has been made possible by the consistent reduction in the size of MOSFETs. Nonetheless, challenges arise with each successive transistor generation node. These challenges are detailed as follows.

### 1.5.1 Short Channel Effects (SCEs)

This is the lateral side effect of MOSFET scaling. The deduction of the overall lateral diffusions of the source and drain from the MOSFET gate length ($L_g$) yields the actual channel length. As the channel length is scaled down approximately to the size of the depletion layer width, the short channel effects become obvious. The exact point where the effects become more obvious is determined through the natural scaling length ($\lambda$). Several short-channel effects are discussed in subsequent sections.

### 1.5.2 Drain-Induced Barrier Lowering (DIBL)

As the length of the channel diminishes, the drain junction approaches the source junction. Consequently, the electric potential within the source-channel region is influenced by both the gate voltage and the drain voltage. The drain voltage, in particular, reduces the barrier near the source end of the channel, allowing for the flow of current at a reduced gate voltage. This occurrence is commonly referred to as Drain-Induced Barrier Lowering (DIBL)[13–15].

- **Effect on threshold voltage**: An apparent decrease in the threshold voltage is one of the side effects that might result from DIBL. From a physical standpoint, the presence of DIBL makes it possible for a lower gate bias to lower the barrier to the point where current may flow. The threshold voltage continues to drop with rising $V_{DS}$. In other words, $V_{TH}$ is now a function of $V_{DS}$ and $V_{GS}$ instead of $V_{GS}$, as in the case of long-channel MOSFETs.
- **Effect on Subthreshold Behaviour**: The DIBL also causes unusual behaviour at the subthreshold of short channel MOSFETs. As the potential barrier diminishes, electrons persist in moving between the source and drain, even when the gate-to-source voltage ($V_{GS}$) falls below the threshold voltage ($V_{TH}$). At this point, the channel current flowing under this condition ($V_{GS} < V_{TH}$) is the so-called subthreshold current leakage.

### 1.5.3 Velocity Saturation

The horizontal and vertical electric field inside the MOS device becomes much more significant when the device's dimensions are reduced. The vertical electric field attracts several consequences, one of which is known as Velocity Saturation which decreases the transconductance in the saturation mode. Also, the drain current becomes limited. In long-channel MOSFETs, the electric field is notably low, and the velocity of electron drift in the channel is directly proportional to the intensity of the electric field. However, as the channel length reduces, the electric field becomes much more significant, and the drift velocity response becomes minimal, which eventually approaches the saturation value [16, 17].

### 1.5.4 Mobility Degradation

At high electric fields in the direction of carrier motion, a drop in mobility is caused by velocity saturation, which is comparable to a reduction in mobility. In addition, there is also a mobility reduction owing to transverse electric fields (the field originating from the gate). This effect becomes more pronounced as the oxide thickness and channel length decrease. The transverse fields impact lateral current flow for the following physical reasons: MOSFET carriers move in the thin inversion layer close to the silicon's surface. They experience numerous scattering events with the surface and extra Coulomb scattering owing to interface states and charges in the insulator at the interface. These processes combine to produce a lesser so-called "inversion layer" or surface mobility of semiconductors that is smaller than the bulk mobility of semiconductors. As the device is shrunk, the higher vertical fields exert a stronger pull on the carriers toward the surface [18, 19].

### 1.5.5 The Influence of Hot Carriers and Impact Ionization

With the reduction in channel lengths, the lateral electric field experiences an increase when the applied voltages remain constant. Consequently, carriers traversing the channel gain energy and reach elevated temperatures, becoming "hot" carriers. These hot carriers have the potential to induce impact ionization, resulting in the creation of additional electron-hole pairs. This leads to an additional drain current and a substrate current composed of holes generated through ionization, which flow toward the substrate, typically the most negatively charged region within the transistor. Furthermore, hot carriers may accumulate enough energy to overcome the potential barrier at the silicon-insulator interface and penetrate into the insulator [20].

## 1.6 Oxide Gate Tunnelling

This phenomenon emanates from the scaling of MOSFETs and manifests as a vertical side effect. In cases where the gate insulator of a MOSFET is considerably thinner than the channel length, the gate is able to assert control over the channel potential. The thickness of the gate oxide introduces two limitations. Firstly, the thin oxide layer leads to increased leakage current that is primarily influenced by the tunneling effect. This occurs when the oxide thickness is reduced. Although the tunneling current caused by the wide oxide layer may seem insignificant compared to the chip's current in the "ON state," it has a notable impact during standby mode. Furthermore, the thickness of the oxide layer plays a role in the reduction of inversion charge and transconductance. This is attributable to the impact of the polysilicon gate depletion effect and the quantization effect within the inversion layer.[21].

## 1.7 Process Variation

As MOSFETs shrink in size, the reduced number of atoms in the silicon significantly impacts the transistor's properties. Consequently, controlling the precise number and arrangement of dopants becomes more challenging. In the production of chips, random process variations affect various dimensions of MOSFETs, including length, width, junction depth, oxide thickness, and more. These random variations become more pronounced as MOSFETs become smaller. Consequently, the characteristic properties of MOSFETs become unpredictable due to these random process variations [22].

## 1.8 MOSFET Technological Boost

As indicated in the preceding section, the scaling issues of MOSFET technologies need the development of new technologies and materials. These innovative technology boosters result in what is known as "equivalent scaling," in which the ongoing enhancement of performance and the aggressive reduction in pitch sustain the performance trends that have been established. Meanwhile, the actual scaling of particular dimensions or electrical parameters has reached a standstill. Figure 1.6 depicts the history of transistor gate length during the previous few decades, as well as the International Technology Roadmap for Semiconductors (ITRS) estimates for the next 15 years.

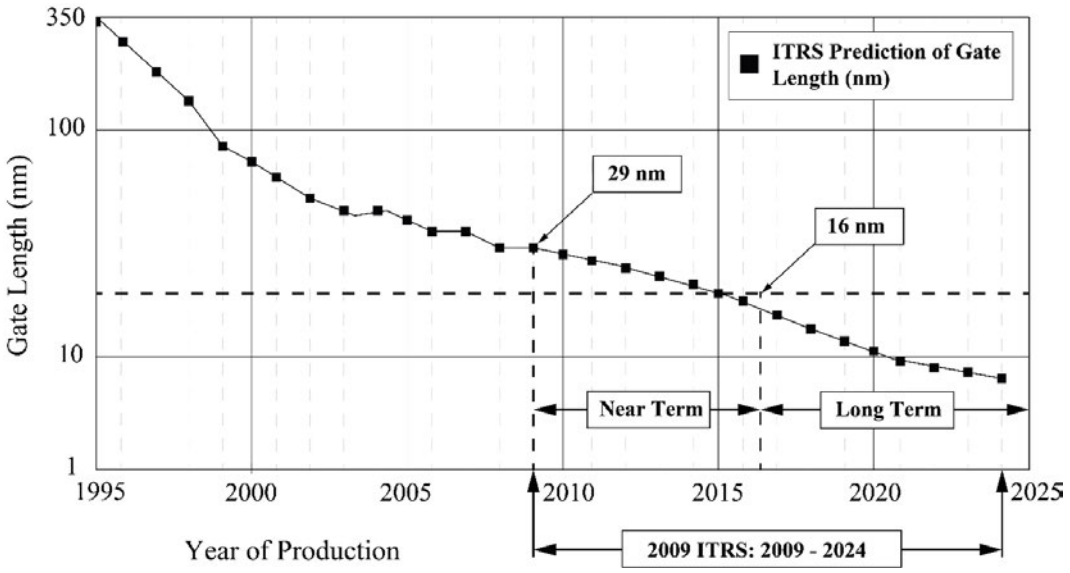


FIGURE 1.6: 2009 ITRS Prediction for next 15 years[23].

### 1.8.1 High Permittivity Gate Dielectric

The use of high gate dielectric is one of the most promising technologies to control scaling challenges in the nearest future. A variety of material restrictions and process integration criteria must be met when replacing SiO2 with a high-k dielectric stack. A stringent selection cuts out many options based on their permittivity, even though there are numerous viable high-k materials. [24].

TABLE 1.2: High- K Gate dielectric material parameter

| Material | Energy gap (eV) | Permittivity | Differences in conduction band energies (eV) | Leakage Current Reduction (SiO2 ref) | Temperature Resistance, Tmax($^oC$) |
|---|---|---|---|---|---|
| $Al_2O_2$ | 8.8 | $9.5-12$ | 2.8 | $10^2-10^3$ | $\sim 1000$ |
| $SiO_2$ | 9 | 3.9 | 3.15 | | |
| $HfO_2$ | $4.5-6$ | $16-30$ | 1.5 | $10^4-10^5$ | $\sim 430-600$ |
| $ZrO_2$ | $5.7-5.8$ | $12-16$ | $1.4-1.5$ | $10^4-10^5$ | $\sim 900$ |

To begin with, a proper conduction band offset is required to create a sufficient barrier in terms of gate leakage. Tantalum pentoxide (Ta2O5), for example, has a sufficiently high permittivity of about 25, but the conduction band barrier of 0.36 $eV$ is insufficient

to give any overall benefit over SiO2. The advantage of the high dielectric constant is negated by the smaller band gap of high-k materials. Consequently, a fundamental prerequisite for high-k dielectric candidates is to establish an appropriate balance between the permittivity and the difference in the conduction band. Some high-k dielectrics display potential as substitutes for silicon oxide, and a selection of their fundamental characteristics is presented in Table 1.2 , in comparison to $SiO_2$ [24].

### 1.8.2 Advanced Multi-gate MOSFETs

The usage of multi-gate MOSFETs is yet another potential technology that has continued to evolve despite not being a new concept. The requirement to suppress SCEs to achieve equivalent scaling technology has pushed multi-gate MOSFETs to the forefront in recent years. Multi-gate MOSFETs provide electrostatics shielding over the lateral and perpendicular electric fields that originate from the drain and gates. Also, the transverse electric field becomes minimal as the channel mobility increases. Multiple gate coupling improves channel control, resulting in a steeper subthreshold slope and lower DIBL effects. Finally, two or more inversion volumes are formed, which results in increased current flow inside the channel.

Manufacturers will unquestionably have to embrace multi-gate devices if they intend to decrease the channel length to less than 30 nm and align with the objectives of the ITRS [23]. Figure 1.7 depicts the evolution of several cross-sectional views of multi-gate MOSFET types on their BOX wafer. Given that transistor technology has always been the sole technology employed by manufacturers, along with their extensive expertise in this area, it is safe to expect that multi-gate devices will eventually replace the planar MOSFETs and be used for broad manufacturing in the nearest future. Among the Multi-gates' structures, SOI MOSFETs, Double-Gates (DG) MOSFETs, and triple-gate MOSFETs, the surrounding-gate MOSFETs have attained great popularity due to their greater gate coupling of the channel because of their gate structure. The Cylindrical Surrounding Gate (CSG) MOSFETs and Cylindrical Surrounding Double-Gate (CSDG) MOSFETs are the most promising devices in the nearest future due to their superior scalability.

## 1.9 Double Surrounding Gate - CSDG MOSFET

The CSDG MOSFET is a multi-gate MOSFET with a concentric cylindrical design. It is similar to both non-conventional CSG MOSFETs and conventional MOSFETs in terms of source, drain, gate, and channel. In contrast, the channel is regulated by both

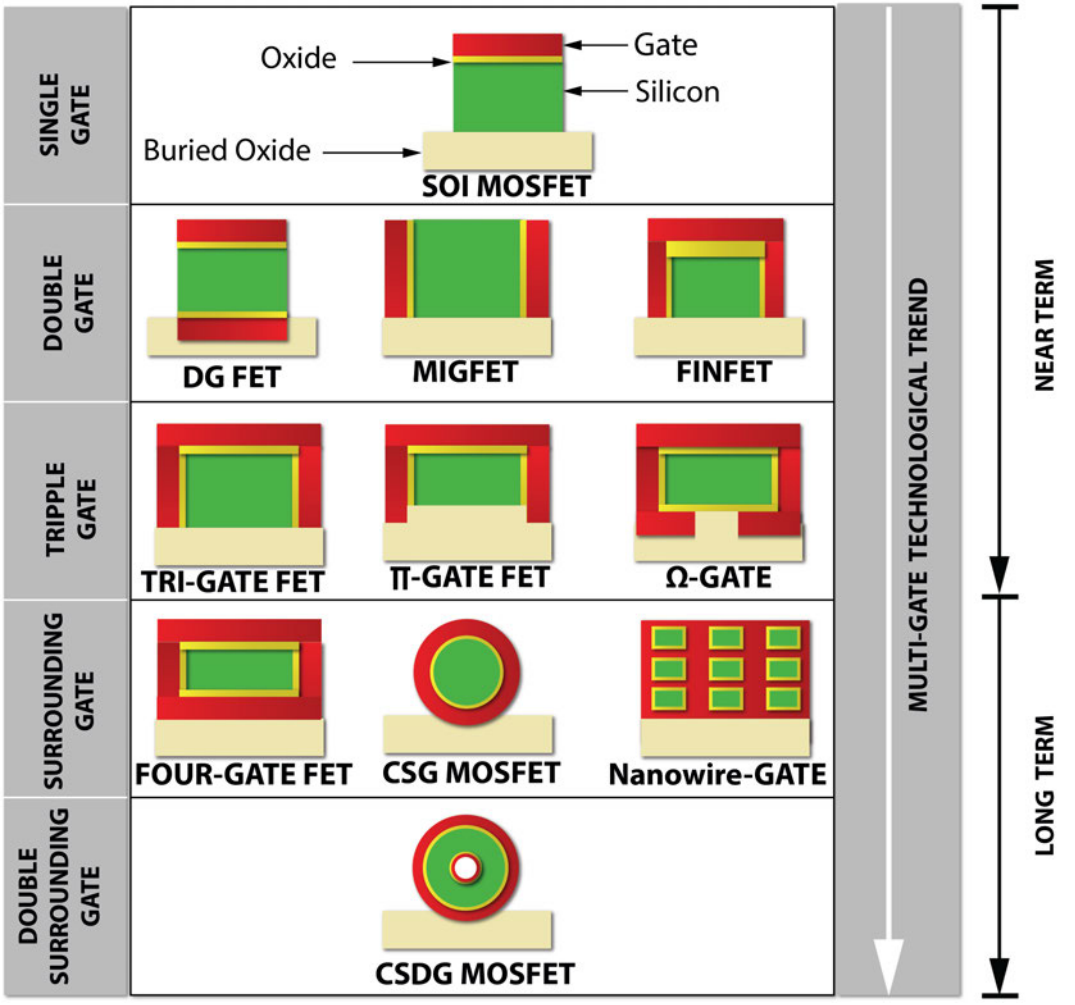


FIGURE 1.7: Cross-sectional depiction of the progression of multi-gate MOSFETs along with their SOI wafer

an internal and an exterior gate. The DG MOSFETs are folded to form the CSDG structure, as shown in Figure 1.8. Srivastava et al.[25] suggested CSDG MOSFETs with the goal of regulating the Silicon channel extremely effectively and suppressing SCEs. CSDG MOSFETs have been shown to have higher drive currents and stronger control of the gate.

The following are the benefits of CSDG MOSFETs.

1. **Better Scalability** - The internal and external cylindrical surrounding gates provide electrical shielding against the lateral electric field generated by charges in the drain and source regions. Because of its greater scalability, CSDG MOSFETs are a viable technology for the 20-nm technological node.

2. **Better Channel Control** - The CSDG MOSFET affords comprehensive gate control over the channels, primarily through the use of the internal cylindrical gate.

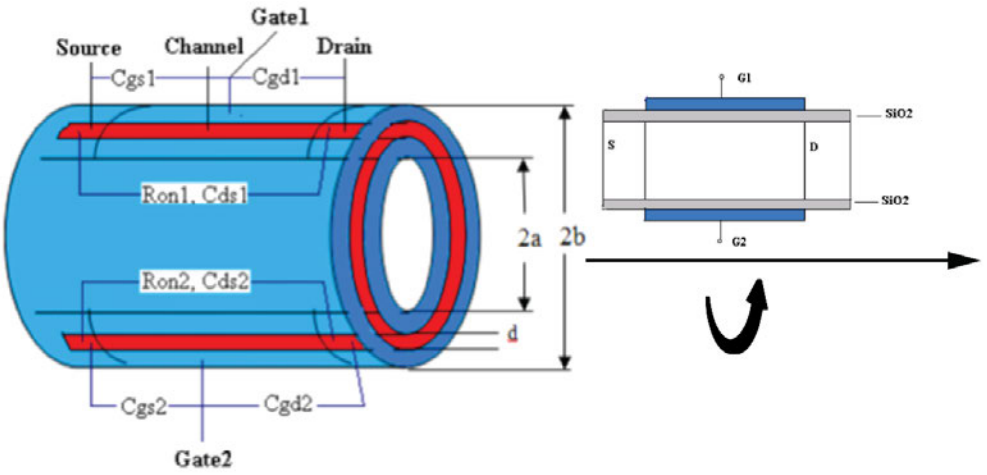


FIGURE 1.8: Structure of CSDG MOSFET [25]

In comparison to other Multi-gate MOSFETs, the combination of the internal gate and the external gate offers superior channel control and more effective mitigation of Short Channel Effects (SCEs).

3. **Increased Driving Current**– CSDG MOSFETs may function in two modes: separate inversion and volume inversion. The former leads to the establishment of two conduction channels, one at the interface between the external gate oxide and the silicon substrate and the other at the junction of the internal gate oxide and the silicon substrate. Unlike the DG MOSFET, which has volume inversion just at the top and bottom. In CSDG MOSFET, the complete current from the channel runs all the way around the cylindrical structure. As a result, the volume inversion may be much more than other multi-gate MOSFET.

4. **Overcoming Issues with Gate Misalignment in DG MOSFETs** - The main disadvantage of DG MOSFET is the misalignment of the two gates in DG MOSFETs, which is alleviated by CSDG MOSFET. In a lengthy and round component, the CSDG MOSFET gates may readily connect the circular source and drain, minimizing gate misalignment issues

5. **Higher Transconductance** - When compared to other multi-gates MOSFETs, CSDG MOSFETs have a greater transconductance. Because RF CMOS switches demand greater transconductance for faster switching and speed. As a result, the structure is a strong contender for RF applications.

6. **High Switching Frequency**- This device is well-suited for integrated circuits due to its superior On-to-OFF current ratio compared to other multi-gate devices. This dissertation analyses the modeling of the unique CSDG MOSFET structure

in terms of the technical boost for higher scalability based on the benefits. In addition, a compact model for predicting the device properties has been presented.

## 1.10 Device Analytical Modelling

One approach to understanding the behavior of multi-gate MOSFETs and analyzing short-channel effects is to determine the potential distribution within the transistor's channel by solving Poisson's equation. This information can then be utilized to derive the remaining device parameters and output characteristics. However, modeling these multi-gate devices faces additional difficulties as device complexity rises. The present numerical simulators are under pressure due to the smaller channels of the complex structure. No semiconductor company can afford to spend a lot of money on simulation gear or hundreds of hours on numerical software simulations in today's market. This is where the semiconductor's analytical and compact modeling comes into play. Its key benefit is that since it is based on the physical properties of the MOSFETs devices, it significantly cuts down on calculation times and assures a remarkable level of compatibility with numerical simulators. These models are also ideal for use in circuit simulators, giving circuit designers limitless options for brand-new device topologies.

A physics-based device model is a description of device behaviour using algebraic and analytical equations. Additionally, if device models are defined in terms of analytical and explicit expressions, they may be said to be compact. This research project is designed to comprehensively address these facets. The models presented in this work are primarily physical models, featuring a minimal number of adjustable parameters that can typically be substituted with values obtained from experimental measurements. These models leverage approximate expressions that are fine-tuned to provide an excellent match with numerical simulations. The closed-form expressions obtained provide high computation speed by reducing simulation time, thereby increasing productivity. Another significant advantage is that these models can be easily integrated into circuit simulators, enabling designers to harness the full capabilities of the design software to create new devices and applications.

## 1.11 Research Objectives

The fundamental aim of this thesis is to contribute to the development of general accurate compact models of CSDG MOSFETs that can be incorporated into design tools,

enabling circuit designers to make projections beyond the currently available scaled dimensions and achieve co-optimization of devices and circuits. The goals of this thesis can be outlined as follows:

1. To develop analytical formulae for the potential distribution of CSDG MOSFET using the parabolic approximation technique, appropriate boundary conditions, and a modelling approach of the Second-order differential solution to derive the Poisson equation's solution for the device architectures.

2. To analyze the degree of short channel effects on CSDG MOSFET through the derivation of natural length since many crucial metrics, including OFF-current, roll-off threshold voltage, and drain induced barrier lowering, rely on it. The authors of this study, for the first time, have reported a scaling theory pattern for CSDG MOSFETs, since the natural length helps quantify the severity of the short channel effects.

3. To perform assessment of quantum scaling length model for CSDG MOSFETs based on the confinement of the lowest electron energy inside a silicon thickness in a quantum well.

4. To analyse the sensitivity of CSDG MOSFET to parameter variation and random dopant fluctuations. And compare the results to CSG MOSFET since they are the only factor that determines how sensitive the threshold voltage is to parameter changes.

5. To Design, analyse, and model the triple material gate stacked CSDG MOSFETs with high-K dielectric for better enhancement of the potential profile to further suppress SCEs.

## 1.12 Thesis Organization

In this thesis, an evaluation of the performance of CSDG MOSFET has been conducted with the aim of further reducing the trade-off between performance and power conservation.

Chapter 1 serves as an introductory section, commencing with an overview of the MOSFET and offering a concise background. It delves into the challenges related to scaling, provides an understanding of short-channel effects, traces the developmental benefits of the CSDG MOSFET structure, and articulates the objectives, collectively laying the cornerstone for the research endeavors explored within this thesis.

Chapter 2 is dedicated to the literature review, encompassing an exploration of the research advancements in analytical model development, the evolution of CSDG MOSFET research, its sensitivity, the concept of gate material engineering, and the motivating factors underpinning the research work conducted within this thesis.

Chapter 3 delves into a comprehensive exploration of the derivation process for a closed-form expression for the natural length of CSDG MOSFET. This investigation entails an extensive analysis, not only examining the derivation itself, but also delving into a comparative assessment against various other multi-gate devices. The chapter scrutinizes the unique characteristics and properties of CSDG MOSFET in the context of natural length, shedding light on its advantages and distinctions in relation to other devices.

Chapter 4 provides a thorough examination of quantum mechanical effects as they relate to quantum well confinements within the context of CSDG MOSFET. The chapter undertakes an in-depth investigation into the interplay between quantum scaling length and classical scaling length, ultimately leading to a comprehensive analysis of the observed effects. These effects are scrutinized in comparison to their counterparts in other multi-gate devices, shedding light on the distinctive behavior of CSDG MOSFET in the quantum realm. This exploration not only expands our understanding of quantum phenomena in semiconductor devices but also highlights the unique attributes of CSDG MOSFET in this quantum context.

Chapter 5 is a comprehensive analytical exploration of CSDG MOSFET's sensitivity to process variation, offering an in-depth analysis of the impact of threshold voltage variation. The chapter builds upon the model introduced in Chapter 3, providing a detailed extension that covers the entire length of the device structure. This extension takes into account a wide array of parameters, meticulously addressing the influence of random dopant fluctuations and their impact on the threshold voltage. The chapter also delves into an investigation of other critical parameters, such as threshold voltage, while making an assumption about the distribution of dopants adhering to a Poisson distribution. This multifaceted analysis not only advances our understanding of CSDG MOSFET, but also elucidates its behavior in the face of process variations, shedding light on its strengths and vulnerabilities in this context.

Chapter 6 serves as an essential introduction to the realms of gate material engineering and oxide engineering, emphasizing the incorporation of high-k dielectrics as a strategic measure to enhance the mitigation of short-channel effects. This chapter propounds a novel analytical model founded upon the groundwork laid in Chapter 5, offering a meticulously detailed analysis that encompasses the three distinct regions within the device structure, each characterized by varying work functions.

This structural configuration goes beyond the mere reduction of the hot carrier effect; it serves to provide an innovative two-step potential rise along the channel. This innovation, in turn, effectively minimizes the traditional trade-off between performance and power consumption, marking a significant advancement in device engineering. The chapter not only elucidates the principles underpinning these engineering strategies but also underscores their implications in reshaping the landscape of semiconductor technology.

Finally, in Chapter 7, we draw the curtains on the extensive research journey embarked upon throughout this thesis. This chapter serves as a reflective summary and provides valuable insights into the research's implications and avenues for future exploration. Figure 1.9 illustrates the comprehensive flow of the entire thesis, as depicted in the thesis flowchart.

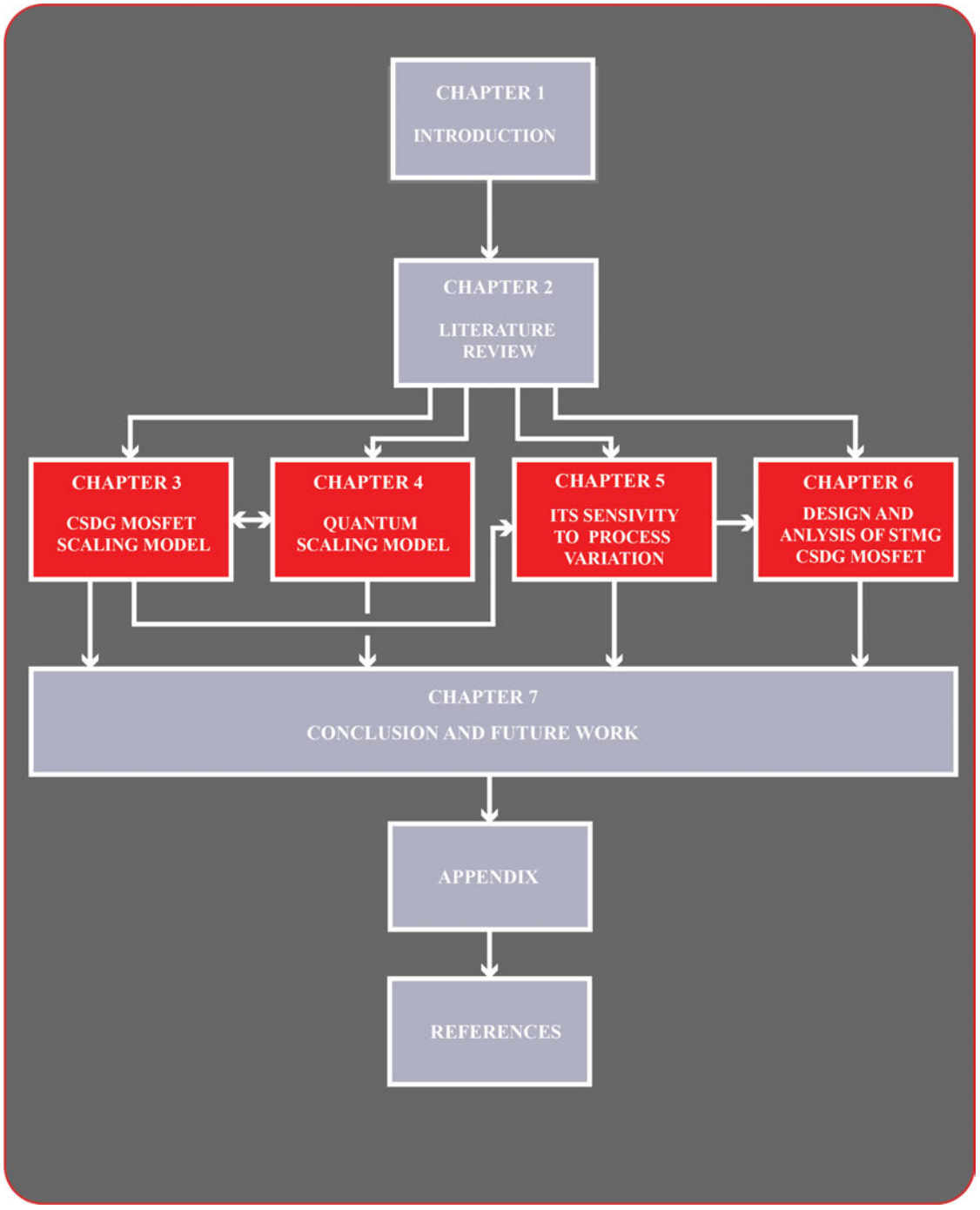


FIGURE 1.9: Thesis Flowchart

# Chapter 2

# Review of Literature

The development of analytical and compact models for various MOSFET structures is covered in detail in this chapter. Several models used to analyze MOSFET structure have been reviewed from 1974 to date. Also, the subsections of this chapter describe the comprehended literature study that was arranged to illustrate the historical progression in the realm of CSDG MOSFET technology.

## 2.1 The Analytical Models of Short-channel MOSFETS

The analytical model approach employed in solving CSDG MOSFET has developed from a 1-D structural model of conventional MOSFET to more advanced structures. The following MOSFET models are discussed.

### 2.1.1 Charge Sharing Model

*Yau* introduced the charge-sharing model in 1974 [26]. The author obtained a simple equation for the threshold voltage of MOSFET from a charge conservation concept that takes two-dimensional edge effects into account geometrically. The equation is applicable for both short and long channel lengths, and it is obtained for zero drain voltage. The channel length, source and drain depth, oxide thickness, and the maximum depletion depth under the gate were taken into consideration. The bulk depletion charge obtained for long-channel MOSFET was extended to obtain the short-channel MOSFET by considering a trapezium region under the gate. At the same time, the source and drain. Based on that assumption, a short-channel threshold voltage was obtained. The charge-sharing model's most significant contribution was highlighting the need for maximum depletion depth beneath the gate in SCEs [27–33].

### 2.1.2 Empirical Expression Model

During the 1980s, a constrained minimum channel length for short-channel devices was defined by Brews et al. [34]. This length depended on factors such as the depth of the drain and source junctions, oxide thickness, and the widths of the source and drain depletion regions. This model was based on 2-D simulation results and experimental data. The provided expression lacks an analytical foundation. Also, an improvement was made to account for non-zero channel length as the oxide thickness and depletion layer approached zero, and the short channel was left as an input variable [35].

### 2.1.3 Polynomial Potential Model

In this type of SCEs model, a cubic polynomial of the vertical variable with coefficient functions of the lateral variable is assumed to be the exact shape of that the 2-D potential function. This modelling approach was proposed by Toyabe and Asai [36]. Analytical models and 2-D numerical analysis are introduced by this model. Also, the model proposed the concept of boundary condition and the derivation of the threshold voltage using the surface potential model. Each MOSFET structure is associated with a distinct set of boundary conditions tailored to its specific model. Using this approach, an analytical solution for the 2-D Poisson's equation was put forth. Moreover, they were the pioneers in depicting the drain and source field effects within a channel through an exponential representation.

### 2.1.4 Two-Dimensional Poisson's Equation Model

The appropriate mathematical approach for addressing short-channel effects involves solving the 2-D Poisson's equation as a boundary value problem tailored to the particular geometry of a short-channel device.[37–41]. Based on this approach, an analytical solution for the electric potential can be obtained. This model has two approaches to solving the complex device geometry as explained in the next section.

### 2.1.5 Parabolic Potential Approximation (PPA) Model with General Solution to Second Order Differential (SOD) concept

Young [42] conducted foundational research work on multi-gate SOI MOSFETs by employing a simplified PPA model to solve the 2D Poisson equation. Similar to the work of Toyabe and Asai, Young described the potential distribution in the vertical direction.

However, Young approached the analysis of Poisson's equation by using a quadratic equation approach. This model served as the basis for analyzing multi-gate devices. Subsequently, the concept of natural length derivation was introduced in [43]. The natural length of a device structure represents the length of the channel area controlled by the drain, and it varies across different multi-gate structures. The natural length plays a crucial role in mitigating SCEs, and it is used to define the central potential channel of the device structure. The model was extended to encompass all multi-gate structures, and the natural length was derived for various device structures, including SOI MOSFETs, Double Gate MOSFETs, Cylindrical Surrounding (CSG) MOSFETs, and other multi-gate structures [44–48].

### 2.1.6 Superimposition Model with Separation of Variable Concept

The superimposition model, incorporating the concept of separation of variables, is a mathematical technique frequently employed for solving partial differential equations (PDEs). This concept was originally proposed by Frank et al. [49]. The superimposition principle states that the solution to a linear differential equation can be expressed as a linear combination of simpler solutions. On the other hand, the separation of variables concept is a method used to solve PDEs by assuming that the solution can be represented as a product of functions that depend on different variables, as reported in [50–52]. For instance, when dealing with a three-dimensional system described by a PDE, we can assume that the solution can be expressed as a product of functions that solely rely on the variables x, y, and z. By combining the superimposition principle with the separation of variables concept, complex PDEs can often be deconstructed into simpler ones that are more manageable to solve.

## 2.2 The Progression in Channel Engineeering

The author in [53] reported on the SOI MOSFET, where the semiconductor layer was positioned on top of the buried oxide (BOX) dielectric layer. Two types of SOI devices were proposed, namely, partially depleted SOI (PDSOI) and fully depleted SOI (FDSOI) MOSFETs. Also, It was mentioned that, for a given access speed, SOI devices consumed only half to one-third of the power compared to bulk Silicon devices. Additionally, they exhibited a speed improvement of around 20% to 25% for a given power consumption, as reported by [54]. It is worth noting that this speed enhancement roughly corresponded to the performance gain achieved by leaping ahead of one

technology generation. Furthermore, it was noted that FDSOI MOSFETs are most attractive for sub-100nm CMOS applications due to their low body effect coefficient and subthreshold slope [55]. However, this technique gives rise to body effect and junction capacitance [56, 57].

The concept of multigate structures can be designed on SOI or Bulk substrate. The DG MOSFET concept was introduced by [58]. The second gate is positioned beneath the silicon layer, with nominal overlap to the source and drain regions, and serves as the bottom conductor, forming a double gate. This concept ensured that no part of the conducting channel was separated from the gate electrodes, allowing for greater channel control [59]. The device can be operated such that both channels can conduct or either of the channels can be in weak or strong inversion [60].

The term "FINFET" was introduced to describe a double-gate configuration fabricated on an SOI substrate, where the conducting channel layer is positioned vertically to the wafer surface, allowing current to flow within the same plane as the wafer[61]. The authors of [62] employed a narrow channel area (to reduce subsurface leakage) along with a double gate configuration (to enhance capacitive coupling between the gate and channel) for mitigating variations caused by random dopant fluctuations (when the channel doping level is low) and short-channel effects.

The tri-gate technology offered a progressive pathway for further miniaturization and necessitated a low aspect ratio for the channel, enabling a reduced retrograde channel doping gradient, as reported by [63, 64]. The authors of [65] reported the random-dopant fluctuation effects on tri-gate MOSFETs, which showed that tri-gate had less threshold voltage lowering and variations. According to [66–68], the tri-gate MOSFET utilized three gates, with a single gate stacked on top of two vertical gates, creating a square or rectangular cross-section. This design increased the area available for electron travel by three times, and the gate width was equal to the sum of all three sides of the semiconductor body. Jan et al.[69] reported that tri-gate transistors minimized leakage and consumed less power than current transistors. The authors reported that the tri-gate architecture was fabricated simultaneously with high-speed logic transistors in a single SoC chip, resulting in industry-leading drive currents at exceptionally low leakage levels.

The corner effect poses a significant challenge for these devices, arising from trapped charges present at the corner edges. Consequently, the device experiences elevated temperatures, leading to reliability concerns, increased leakage current, and aggravated SCEs. The most effective approach to mitigate leakage current and alleviate the corner effect is by rounding the corners as reported by [70].

The concept of Π-Gate MOSFET and Ω-Gate MOSFET was investigated by [71, 72]. These devices typically have three to four gates, with each gate positioned around the silicon body in accordance with its appropriate Greek name. Increasing the "effective number of gates" improves the gate's electrostatic control over the channel, hence decreasing short-channel effects. A virtual back gate is generated by extending the sidewalls of the gate material into the buried oxide, providing an effective boost to the current drive and protecting the rear of the channel region from electric field lines emanating from the drain [73, 74].

The surrounding-gate MOSFET, in theory, provides optimal control over the channel region by the gate, resulting in superior electrostatic integrity. The initial surrounding-gate MOSFETs were created by encircling a gate electrode around a vertical silicon pillar during the fabrication process [75–77]. The surrounding-Gate MOSFET configuration significantly enhances performance by suppressing DIBL, establishing efficient capacitive coupling between the gate and channel, and improving subthreshold slope [78, 79].

Poisson's equation can be used to calculate the "natural length." This term refers to the length of a device's channel region that is determined by the drain [43, 44]. The electrostatic integrity is directly related to the natural length. To eliminate short-channel effects, the effective gate length of a MOS device should be at least 5 to 10 times larger than the natural length. Besides CSDG MOSFET, all the SOI MOSFETs, double-Gate MOSFESTs, tri-gate MOSFETs, and surrounding gate MOSFTETs have their respective natural length [80–82].

The concept of CSDG MOSFET was introduced by Srivastava et al.[25] as the next promising technology. A key concept behind CSDG MOSFETs is to achieve highly efficient control over the Silicon channel. This is achieved by reducing the channel width and applying gate contacts to both sides of the channel. By implementing this approach, the CSDG MOSFET effectively suppresses short-channel effects and enables higher currents when compared with other surrounding gate MOSFETs.

## 2.3 The progression in Material Engineeering

Dual-material gate and tri-material gate engineering techniques involve the use of two or three materials in the gate region. A gate material with a greater work function is used near the source end (control gate), whereas a gate material with a lower work function is used near the drain end. This arrangement effectively avoids any changes in the drain bias (screening gate) while the device is operating. Gate engineering techniques use this approach to optimize the performance and stability of the transistor.

### 2.3.1 Double-material Gate Engineering

In 1999, Long et al. [83] proposed a novel gate structure known as the double material gate MOSFET has been proposed. In contrast to asymmetric structures that use doping engineering to achieve a continuous channel field distribution, the DMG-MOSFET uses gate-material engineering with different work functions. This method introduces a field of discontinuity along the channel, which effectively improves transport while suppressing short-channel effects [84].

In 2004, the authors of [85] reported the potential advantages of utilizing a double-material gate in mitigating short-channel effects in SOI MOSFETs through a two-dimensional (2-D) analytical channel modeling approach. Suppression of short-channel effects and improved device reliability were achieved by abruptly changing the channel potential profile at the dual gate material interface. This modification significantly reduces the peak electric field at the drain side. A double-material structure was proposed to overcome SCEs by combining the benefits of gate material engineering and double-gate features within the same architecture.

Based on the analytical approach using Poisson's equation, a double material gate structure below 100 $nm$ was reported by Reddy et al.(2005). Their outcome showed reduced SCEs and simultaneous achievement of higher transconductance and reduced drain conductance compared to DG SOI MOSFET [86].

In 2010, Li Jin et al.[87] investigated the reduction of the hot carrier effect (HCE) in a DMG strained-Si on insulator MOSFET by decreasing the ratio between the control gate (M2) and screen gate (M1).

Also, James et al.[88] carried out both fabrication and simulation of DG MOSFETs in their study. In order to achieve specific device characteristics, they used different metal gate work functions. The simulations used Poisson equations and 2D quantum transport. The authors reported a reduced DIBL, decreased subthreshold leakage current, and increased $I_{on}/I_{off}$ current in the order of $10^4$, and linear increased threshold voltage. Their analysis showed that the threshold voltage of atomic-layer-doped DG MOSFET can be adjusted by varying the metal gate work function from ranges of 4.2 $eV$ to 4.5 $eV$.

In 2014, Pal et al. [89] reported the incorporation of a double material gate in cylindrical surrounding gate MOSFETs. Their goal was to mitigate the short-channel effect by introducing the concepts of a control gate and a screening gate. Furthermore, they compared the performance of this approach to that of a single material surrounding gate MOSFET (SMSG).

In 2016, Jena et al. [90] investigated the effects of varying the gate length of the double material gate and thoroughly investigated the resulting performance changes on a dual material GAA MOSFET, using gate material work-function of 4.6 $eV$ and 4.2 $eV$

In 2019, Himeli et al. [91] introduced the consideration of temperature effects and interface charge density effects in their analysis of a double material gate double-gate MOSFET. They also took into account the impact of a high dielectric constant material such as $Hf0_2$. The findings demonstrated that the incorporation of $Hf0_2$ substantially reduced the leakage current by increasing the oxide thickness while leaving the surface potential and drain current unaffected. By changing the substrate doping concentration, temperature, and gate-source voltage, the authors were able to enhance the surface potential of the minimized oxide thickness.

In 2020, The authors of [92] studied the impact of a laterally graded channel doping profile and the incorporation of a low-doped buried layer along the center of the channel of Junctionless double-material gate DG MOSFET. Their outcomes showed that the proposed device exhibits a significant increase in the potential step at the interface of the two gates, which effectively suppressed short-channel effects and reduced the OFF current.

In 2021, Monika et al. [93] reported that the optimization of the work function of the double material gate in DG junctionless MOSFETs increased the biosensor sensitivity by 90% compared to a single material gate configuration. Also, the study revealed that when the work function of the source-side gate metal (M1) was varied while keeping the work function of the drain-side gate metal (M2) constant, there was a significant enhancement in the sensitivity of the device. Conversely, when the work function of the drain-side gate metal (M2) was changed while keeping the work function of the source-side gate metal (M1) fixed, the sensitivity improvement was not as profound.

In 2022, the authors of [94] presented a subthreshold drain current model for a center channel-based junctionless channel-modulated double-material DG MOSFET. Additionally, the authors derived the subthreshold current by considering the minimum center channel potential. The results demonstrated that the optimization of the threshold voltage could be achieved through modifications in the work function and doping variations in the channel region.

In 2022, the authors conducted an investigation into the impact of a negative bottom gate voltage on the analog and RF performance of a junctionless double-material DG MOSFET [95]. The findings revealed that the utilization of a low value of the work function at the bottom gate terminal led to improvements in both analog and RF performance.

In 2023, Arighna et al. [96] reported the use of an underlap asymmetrical double material gate structure in junctionless DG MOSFETs to enhance manufacturing and logical processes. The analytical model employed demonstrated that this device structure increased the threshold voltage, rendering it suitable for future-generation circuits. Additionally, the device structure improved hot carrier reliability.

### 2.3.2 Triple-material gate engineering

In 2008, Razavi et al.[97] proposed triple-material DG MOSFET to obtain further efficacy against SCEs and search for more carrier transport efficiency using gate material work-function of 4.8 $eV$ , 4.6 $eV$ and 4.4 $eV$. By adjusting the length ratio of the gate materials and optimizing their properties, the authors reported a significant improvement in reducing short channel effects and enhancing device reliability. Suveetha et al.[98] further extended the analysis and performed an investigation of the electrical characteristics, including surface potential, electric field, and threshold voltage.

In 2010, Tiwari et al.[99] reported that triple material MOSFET have better performance than double material MOSFET using analytical approach. The authors solved the 2D Poisson equation with suitable boundary conditions by applying the parabolic potential approximation. And a lightly doped channel was considered to minimize dopant fluctuation.

In 2012, H.K.Wang et al.[100] reported an analytical model of the 2-D potential distribution using the concept of superimposition techniques. The results obtained showed that triple material of the surrounding gate MOSFETs have better performance than double material surrounding gate MOSFET and triple material DG MOSFFET.

In 2013, Dubey et al.[101] extended the investigation to explore the use of a triple material gate. The authors developed an analytical threshold voltage model based on the concept of center potential. The center potential concept was employed to formulate the threshold voltage, and also subthreshold swing and DIBL were extracted. Furthermore, the authors conducted a comprehensive investigation to examine the impact of variations in channel thickness, oxide thickness, and gate length on device performance.

In 2015, Biswajit et al.[102] developed a model for triple material DG MOSFT using a rectangular Gaussian box in the channel depletion region to predict the surface potential and threshold of the device structure. Also, they discussed the quantum mechanical effects (QMEs), and a quantum confinement-induced correction term for threshold voltage was developed. Their work paved the way for future research on gate-engineered multiple-gate MOSFET.

In 2019, the authors of [103] reported the analytical modeling of junctionless triple material gate DG MOSFET was proposed using parabolic approximation techniques. The authors reported observed an improvement in ON current while achieving an OFF current of $10^{-11}A$, making it suitable for low-power applications.

In 2020, the authors of [104] presented a triple material Double-Gate (DG) MOSFET, incorporating a high-k dielectric in addition to $Si0_2$. This design resulted in a significant reduction in leakage current, achieving a remarkable OFF current reduction of $10^{-14}A$.

In 2021, Arvind et al. [105] presented an analytical 2-D model for a stacked triple material gate all around MOSFET with an asymmetric gate configuration. The researchers enhanced the high channel effects (HCEs) by incorporating a high-k dielectric material ($Hf0_2$) along with $Si0_2$,resulting in reduced leakage currents. Additionally, the findings demonstrated that the asymmetric gate stack structure increased carrier velocity, improved carrier transport efficiency, mitigated DIBL, hot-carrier effects, and other SCEs, consequently leading to decreased power dissipation.

In 2023, the authors of [106] investigated the study focused on evaluating the performance of a dielectric-stacked triple-material cylindrical gate-all-around MOSFET in the context of low-power applications. This assessment encompassed the examination of performance metrics, including DIBL, subthreshold swing, and threshold-voltage roll-off. The outcome performance metrics showed 8%, 36.2%, and 13.5% improvement, respectively. Furthermore, the authors reported that the halo doping profile mitigates SCEs. Also, the authors analysed the analog behaviour using transconductance.

## 2.4 The progression in CSDG MOSFET

In 2011, Srivastava et al.[25] presented an analysis of CSDG MOSFET design. They emphasized the circuit-level equivalence of the device when transitioning between the ON and OFF states within the microwave sub-system. The researchers employed lumped-circuit elements to approximate the device behavior and concluded that the observed drain current behavior supports the compatibility of the device for RF switching applications.

In 2012, Yadev et al. [107] explored the drain current model and developed a model at the subthreshold for CSDG MOSFET. The results obtained showed that CSDG MOSFET's drain current surpasses other multi-gate structures.

Srivastava et al. (2013) introduced an explicit model of CSDG MOSFET, utilizing a unified charge control model [108]. The researchers derived an expression for the

channel current, incorporating terminal charges, trans-capacitance, trans-conductance, and drain conductance, which were dependent on structural parameters and applied voltage. Additionally, the derivation of the channel potential only involved solving a one-dimensional Poisson equation.

In 2016 Srivastava et al. [109] evaluated the switching behavior of CSDG MOSFET via a circuit-level model that incorporated parasitic resistance and capacitance. Based on their analysis, the researchers concluded that CSDG MOSFET offers higher switching speeds compared to other MOSFET structures, making it a promising choice for various nanotechnology-based switching circuit applications.

In 2016, Verma et al. [110] presented the modeling of a cylindrical surrounding double-gate MOSFET with a vacuum gate dielectric instead of silicon dioxide, which resulted in a great improvement in hot-carrier reliability. The author concluded that in the near future, CSDG will replace CSG MOSFET.

In 2017, Uchechukwu et al. [111] demonstrated the potential application for low-power operation in a typical rectifier circuit by customizing the CSDG basic structure into a conventional arrangement via a bridge rectifier.

In 2017, Srivastava et al. [111] provided a comprehensive list of advantages associated with CSDG MOSFET beyond the 22-nanometer technological node. The researchers emphasized the benefits achieved through scaling of the CSDG MOSFET parameters, highlighting the potential for further optimization of these parameters.

In 2018, Oyedeji et al. [112] provided a comprehensive amplifier circuit perspective, in which they reported that the voltage gain and transconductance are higher as compared to other MOSFET structures. The authors also considered the application of CSDG MOSFET in mixer circuit application [113]. Also, the author of [114] presented a circuit perspective of CSDG by utilizing a high-pass filter. The designed filter functioned with a cutoff frequency of 0.3 $THz$ and incorporated a CSDG MOSFET to suppress lower frequencies and improve gain.

In 2019, Uchechukwu et al. [115] presented the analytical solution of the 2D Poisson equation using evanescent-mode analysis (EMA) to analyse the threshold voltage and subthreshold swing behaviour of a CSDG MOSFET. The results showed that CSDG was optimized by decreasing the oxide thickness and radii silicon film difference of the CSDG MOSFET, which increased the stability of the threshold voltage and lowered the turn-off current.

In 2021, the authors of [116] analysed CSDG MOSFET using $La_2O_3$ as a high dielectric material, which shows good improvement. In their simulation, the results showed that

the highest capacitance obtained with $La_2O_3$ based on CSDG MOSFET is in the order of 17.24 $F/cm^2$.

In 2021, Dargar et al.[117] presented the design of CSDG MOSFET with stacked double material. Their results showed that the dependence of the minimum surface potential was reduced by decreasing the metal length ratio and oxide thickness ratio. Also, the stacked double material gate showed better improvement than the single material CSDG MOSFET. Also, the authors considered quantum confinement analysis, including the capacitance correction considering the average penetration of the inversion centroid [118].

In 2022, the authors of [119] reported an analytical model using the Pao Sah's double integral to derive the current of CSDG MOSFET with $La_2O_3$ material. Also, the authors reported that fabrication of CSDG MOSFET can be cut into desired length. Also, the same authors, investigate platinum, which provided higher electronic immunity towards SCEs[120].

In 2023, Gowthaman et al.[121] introduced a fabrication perspective of CSDG MOSFET using a layer-by-layer approach. This method provided comprehensive insights into establishing the optimal conditions for the fabrication chamber, which ensured the successful construction of the device. The maximum etching rate at a 2-second interval was observed to be 5.79 $\mu m/min$ at the beginning of the etching of the cylindrical structure. Over time, the etching rate gradually decreased and approached 1.43 $\mu m/min$ at the end of the flow, which occurred at a rate of 150.08 $sccm$.

## 2.5 Research Motivation

Driven by the prospects of advancing miniaturization in MOSFET technology, a strong sense of motivation arises. This motivation stems from the anticipated benefits of enhanced speed and reduced power consumption in various electronic components, especially in this era of the Internet of Things (IoT). With a focus on nanoscale advancements, the future holds great promise for cylindrical surrounding Double gate (CSDG) MOSFET. A thorough examination reveals the trajectory of progress in MOSFET scaling, marking the transition from conventional MOSFET to multi-gate MOSFET through the innovative concept of gate engineering. Furthermore, simplified compact modeling techniques are being employed to effectively capture the device's geometrics, while material engineering is being explored to overcome challenges associated with the increasing scale of the device. This motivation propels researchers and engineers towards a future where CSDG MOSFET technology will continue to flourish.

The CSDG MOSFET showcases intriguing similarities to three other prominent MOSFET structures: gate all around (GAA) MOSFET, surrounding gate (SG) structures, and DG MOSFET. CSDG combines certain features from each of these structures, resulting in a unique and promising device. When comparing CSDG with GAA and SG structures, the defining characteristic of CSDG lies in its external surrounding gate. Furthermore, CSDG shares similarities with DG structures due to its dual surrounding gate, making it a double (internal and external) surrounding gate engineering. The amalgamation of these features from GAA, SG, and DG structures positions CSDG MOSFET as a highly promising technology. The CSDG MOSFET holds great potential for advancements in the field of MOSFET technology, facilitating further progress in speed, power consumption, and overall device performance.

The utilization of analytical models and simulation techniques holds substantial importance in the realm of early detection and prediction of device characteristics. By leveraging these tools, researchers can effectively minimize the reliance on costly and time-consuming fabrication cycles. Notably, recent endeavors have concentrated on investigating the potential of gate engineering and material engineering in the context of short-channel MOS structures. Gate engineering involves the strategic design and manipulation of the gate structure to enhance device performance, improve control over electrical characteristics, and mitigate issues associated with short-channel effects. Material engineering, on the other hand, focuses on the utilization of advanced materials and their integration into device structures to augment performance, increase efficiency, and overcome scaling challenges.

The research focuses on exploring gate engineering and material engineering in the realm of short-channel MOS structures. It is expected to uncover new opportunities for enhancing device performance and functionality. This involves establishing the scaling pattern for CSDG MOSFET and introducing a triple-material approach within CSDG MOSFET for the first time. By doing so, it is anticipated that notable improvements can be achieved in device characteristics. These improvements encompass reducing threshold voltage roll-off, mitigating hot carrier effects, and overcoming short-channel effects.

In the following chapter, the authors derive the natural length of the CSDG MOSFET and evaluate and compare its short-channel characteristics with those of other multi-gate structures like SOI, DG, and CSG.

# Chapter 3

# Channel Length Scaling Pattern for CSDG MOSFET

The natural length of MOSFETs plays a crucial role in understanding the distribution of potential in the Silicon substrate [122]. This natural length varies across various device structures, ranging from single-gate to multi-gate geometries. To accurately assess the impact of SCEs, it is essential to determine the natural length as it influences important parameters like OFF-current, roll-off threshold voltage, and drain-induced barrier lowering. This section introduces a scaling theory specifically tailored for CSDG MOSFETs, offering valuable insights for future device designs.

## 3.1 CSDG MOSFET Device Geometry

As shown in Figure 3.1, the CSDG MOSFET is a variant of the DG MOSFET where the device structure is folded along the z-axis. This folding creates an exterior and interior radius with respect to the radial coordinates $r = a$ and $r = b$. The device structure includes two gates, and the extruding part of the device structure forms the drain and source ends, similar to the DG MOSFET.

A Gaussian surface is assumed, as shown in Figure 3.2, and the boundary condition is determined. The parabolic potential approximation model is used to analyze the silicon-oxide interface only. Based on that, a closed-form expression is derived with respect to the boundary condition.

The Poisson equations, both in cartesian and cylindrical forms, are employed to describe the CSDG MOSFET structures illustrated in Figure 3.1.

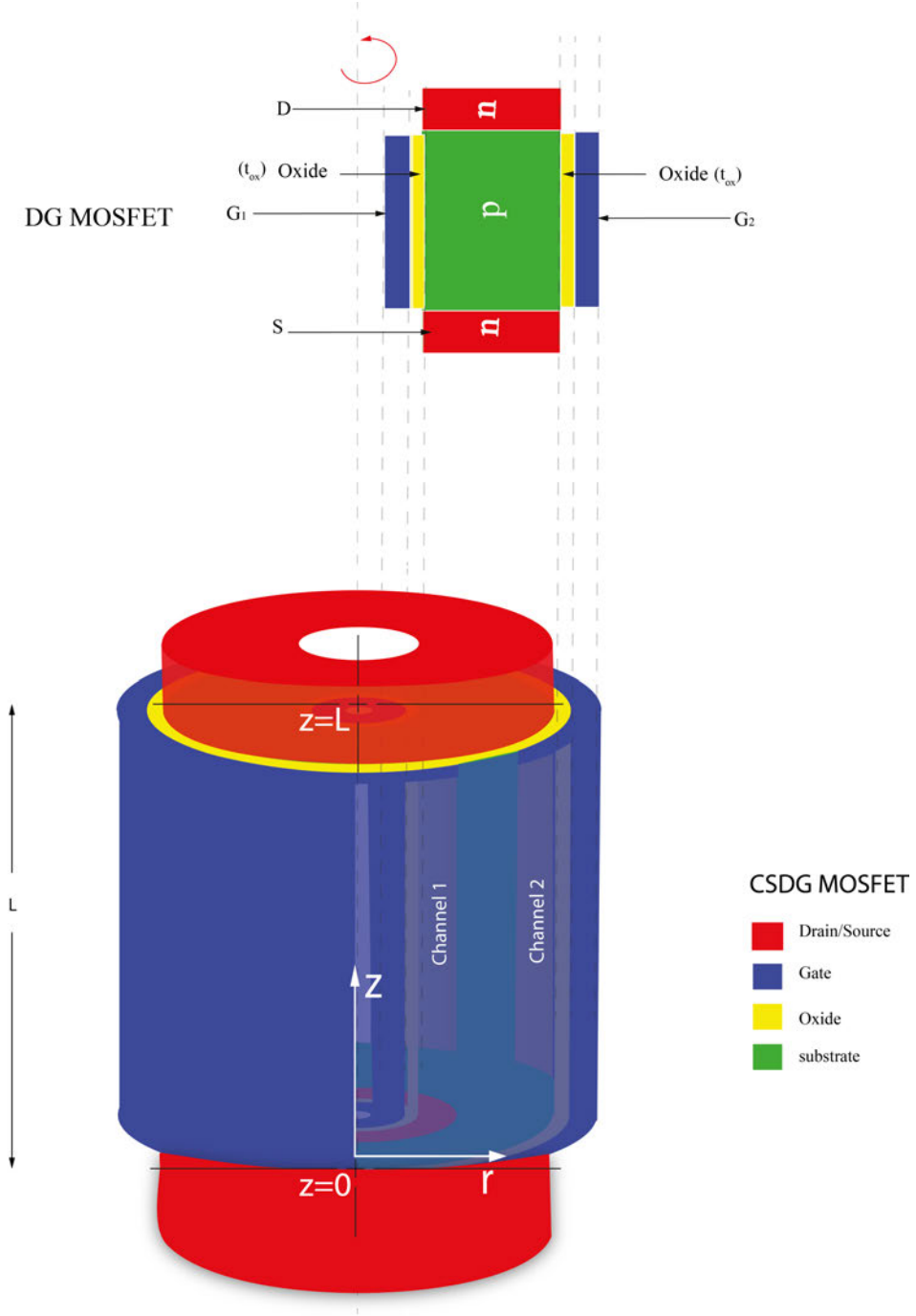


FIGURE 3.1: CSDG MOSFET in 3D view [115].

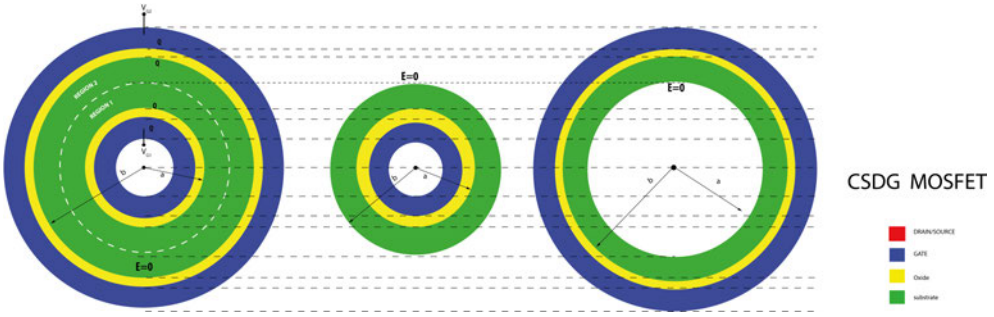


FIGURE 3.2: Circular cross-sectional depiction of the radial portion of the CSDG MOSFET structure in 2-D.

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}\psi(r,z)\right)+\frac{d^2\psi(r,z)}{d^2z}=\frac{qN_a}{\varepsilon_{si}} \tag{3.1}$$

where $Na$ represents the doping concentration, $\psi(r,z)$ stands for the potential distribution along the cylindrical form, and $q$ represents the electric charge. The permittivity of silicon is denoted as $\epsilon_{si}$ and $r$ represents the radius.

## 3.2 Centre Potential for The CDSG MOSFET Geometry

Inside the Silicon pile, at the Gaussian surface, the electric field is 0. Concerning the boundary conditions in Figure 3.2, a PPA proposed by Young uses a quadratic equation concept with the help of boundary conditions to represent Poisson's equation as a second-degree polynomial. Researchers have used a similar analytical model, known as PPA, combined with the Second-order equations to solve the recent multi-gate structures analytically. The primary distinction is in the boundary condition, as each structure differs. SOI, DG, CSG, and CSDG all have different geometry; hence, their boundary condition differs from one another). This model was used to analyze CSDG with respect to its boundary condition, as illustrated in Figure 3.2, to obtain all the variables C0, C1, and C2. Then, with the help of boundary conditions, the potential distribution was obtained using the Second-order differential equation. The Potential distribution describes the variation of charges within the channel between the MOSFET's source and drain terminals.

Using the parabolic potential approximation with respect to CSDG MOSFET geometry, Equation 3.1 can be written based on Young model as given [42]

$$\psi(r,z)=C_0(z)+C_1(z)r+C_2(z)r^2 \quad (a\le r\le b) \tag{3.2}$$

where $C_0$, $C_1$, and $C_2$ are undetermined variables, and $r$ represents the radius which ranges from $a$ to $b$ to account for the impact of both internal and external gates on the Silicon substrate. The boundary condition based on Figure 3.2 along the radial direction.

Given that the CSDG cylindrical structure has its center at radius r = 0, the following conditions are observed: the electric field (E) is zero, and the potential distribution ($\psi(r, z)$) is zero. This is because it is assumed that the electrostatic distribution of charges in the center of the device is negligible.

Furthermore, the authors determined the electric field (E) on the surface and at the center of the silicon with respect to a Gaussian surface. Based on this, the internal and external gates are considered in relation to Figure 3.2 and the corresponding boundary conditions are as follows:

### 3.2.1 Considering the internal gate at r = a

$$\left.\frac{d\psi(r,z)}{dr}\right|_{r=a} = C_1(z) + 2C_2(z)a = \frac{C_{oxa}(V_{gs} - V_{fb}) - \psi_s(a)}{\varepsilon_{si}} \tag{3.3}$$

$$\left.\frac{d\psi(r,z)}{dr}\right|_{r=\frac{t_{si}}{2}} = C_1(z) + 2C_2(z)\frac{t_{si}}{2} = -\frac{C_{oxa}(V_{gs} - V_{fb}) - \psi_s(a)}{\varepsilon_{si}} \tag{3.4}$$

### 3.2.2 Considering the internal gate at r = b

$$\left.\frac{d\psi(r,z)}{dr}\right|_{r=b} = C_1(z) + 2C_2(z)b = \frac{C_{oxb}(V_{gs} - V_{fb}) - \psi_s(b)}{\varepsilon_{si}} \tag{3.5}$$

where $C_{oxa}$, $V_{gs}$, $V_{fb}$ are the oxide capacitance per unit area, gate-source voltage, and flatband voltage, respectively.

When considering the internal gate, situated at the center of the Silicon substrate, it's important to note that the electric field is present due to the asymmetrical structure. In this context, because $(tsi/2)$ is greater than $a$, it consistently results in a positive value for $(tsi - 2a)$. Consequently, the electric field associated with the internal gate is confined within this specific region along the radial path. To determine the values of the variables $C_1$ and $C_2$, Equations (3.3) and Equation (3.4) can be simultaneously solved. Subsequently, $C_0$ can be calculated based on Equation (3.2) regarding the internal gate, as outlined below:

$$C_2 = \frac{2C_{oxa}(V_{gs} - V_{fb}) - \psi_s(a)}{(t_{si} - 2a)\varepsilon_{si}} \tag{3.6}$$

$$C_1 = \frac{(2C_{oxa}\varepsilon_{si}t_{si} + (t_{si} - 2a)C_{oxa})(V_{gs} - V_{fb}) - \psi_s(a)}{(t_{si} - 2a)\varepsilon_{si}} \tag{3.7}$$

$$C_0 = \psi_s(a) - \frac{(2C_{oxa}\varepsilon_{si}t_{si} + (t_{si} - 2a)C_{oxa})(V_{gs} - V_{fb}) - \psi_s(a)}{(t_{si} - 2a)\varepsilon_{si}} + \frac{2C_{oxa}(V_{gs} - V_{fb}) - \psi_s(a)}{(t_{si} - 2a)\varepsilon_{si}} \tag{3.8}$$

By plugging Equation (3.6), Equation (3.7), and Equation (3.8) into Equation (3.2) at $r = (tsi/2 - a)$, the relationship between the surface potential and centre potential w.r.t. the Gaussian surface at point $C$ from Figure 3.2 is obtained as:

$$\psi_s(a) = \frac{1}{1 + \frac{C_{oxa}t_{si}}{\varepsilon_{si}}}\left(\psi_c(z) + \frac{C_{oxa}t_{si}}{\varepsilon_{si}}\right) \tag{3.9}$$

where $C_{oxa}$ is the oxide capacitance per unit area with respect to the internal gate, given as:

$$C_{oxa} = \frac{2\varepsilon_{ox}}{(t_{si} - 2a)ln\left(1 + \frac{2t_{ox}}{(t_{si} - 2a)}\right)} \tag{3.10}$$

And for the external gate, the oxide capacitance is given as:

$$C_{oxb} = \frac{2\varepsilon_{ox}}{(2b - t_{si})ln\left(1 + \frac{2t_{ox}}{(2b - t_{si})}\right)} \tag{3.11}$$

By substituting Equation (3.9) and Equation (3.10) into Equation (3.1) and solving the authors obtained the radial part of the equation w.r.t. the internal gate as given:

$$\frac{8C_{oxa}(V_{gs} - V_{FB} - \psi_c(z))}{(t_{si} - 2a)\varepsilon_{si}\left(1 + \frac{C_{oxa}t_{si}}{\varepsilon_{si}}\right)} + \frac{d^2\psi(r,z)}{d^2z} = \frac{qN_a}{\varepsilon_{si}} \tag{3.12}$$

By substituting Equation (3.10) into Equation (3.12), the solution obtained is given as:

$$\frac{16\varepsilon_{ox}(V_{gs} - V_{FB} - \psi_c(z))}{(t_{si} - 2a)^2\varepsilon_{si}\ln\left(1 + \frac{2t_{ox}}{(t_{si} - 2a) + 2\varepsilon_{ox}t_{si}(t_{si} - 2a)}\right)} + \frac{d^2\psi(r,z)}{d^2z} = \frac{qN_a}{\varepsilon_{si}} \tag{3.13}$$

In the case of asymmetrical structures, there can be multiple natural lengths. This can be addressed by analysing both symmetrical and asymmetrical structures to facilitate

the analysis. For example, Tsormpatzoglou et al. [123] investigated the tri-gate MOSFET (an asymmetrical structure) by splitting it into symmetrical and asymmetrical DG MOSFETs. They derived two natural lengths and used it to obtain a closed-form expression for the threshold voltage.

Similarly, in the present research work, the device structure being asymmetrical led to the existence of two natural lengths associated with the inner and external gates. The natural length of the external gate was found to be smaller than that of the internal gate, indicating that the external gate offers better immunity against SCEs compared to the inner gate. However, as the device structure is scaled down, the two natural lengths approach each other, and its effect becomes approximately the same.

The natural scaling length ($\lambda_{CSDG}$) for CSDG MOSFET, considering the internal radius in Equation (3.13) can be described as:

$$\frac{(V_{gs} - V_{FB} - \psi_c(z))}{\lambda_{CSDG}^2} + \frac{d^2\psi(r,z)}{d^2z} = \frac{qN_a}{\varepsilon_{si}} \tag{3.14}$$

where ($\lambda_{CSDG}$), the natural scaling length, is dependent on the new parameter, a (the internal radius), Silicon film ($t_{si}$), and oxide thickness ($t_{ox}$). Also, since $(t_{si}/2) > a$, $(t_{si}-2a)$ will always be positive. Furthermore, the value of "$a$" contributes to minimizing the short channel effects (SCEs) for CSDG MOSFETs.

$$\lambda_{CSDG} = \sqrt{\frac{\varepsilon_{si}(t_{si}-2a)^2 \ln\left(1+\frac{2t_{ox}}{(t_{si}-2a)}\right) + 2\varepsilon_{ox}t_{si}(t_{si}-2a)}{16\varepsilon_{ox}}} \tag{3.15}$$

Similarly, the natural scaling length ($\lambda_{CSDG}$) w.r.t. to the external gate,"$b$", is given as:

$$\lambda_{CSDG} = \sqrt{\frac{\varepsilon_{si}(2b-t_{si})^2 \ln\left(1+\frac{2t_{ox}}{(2b-t_{si})}\right) + 2\varepsilon_{ox}t_{si}(2b-t_{si})}{16\varepsilon_{ox}}} \tag{3.16}$$

In this context, ($\lambda_{CSDG}$) relies on a novel parameter, denoted as $'b,'$ which represents the external radius. Additionally, given that $b$ is greater than $(tsi/2)$, the term $(2b-tsi)$ consistently assumes a positive value, contributing to the reduction of Short-Channel Effects (SCEs) in CSDG MOSFET.

So, proper care must be taken in choosing the values of "$b$" or ''$a$" in designing the device structure within the conventional scaling factor. In order to make a fair comparison with other multi-gate structures, we focused on the natural length of the inner gate in our

analysis. Therefore, the threshold voltage behavior was determined based on the natural length of the inner gate.

## 3.3 Short-Channel Characteristics of CSDG MOSFET

The calculated natural length is employed to forecast the occurrence of Short-Channel Effects (SCEs). The authors have derived the natural length of CSDG MOSFET, and its characteristics are compared with other multi-gate devices as shown in Table 3.1

TABLE 3.1: Natural Length of Multi-gates MOSFETS vs CSDG MOSFETs

| Multi-gate MOSFETs | Model | Varying parameters | Natural length ($\lambda$) | Scaling Factor ($\alpha$) |
|---|---|---|---|---|
| SOI MOSFET [43] | $PPA$ | Silicon and oxide | $\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}$ | $\frac{L}{2\lambda_G}$ |
| DG MOSFET [124] | $PPA$ | Silicon and oxide | $\sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{si}}{4\varepsilon_{si} t_{ox}}\right) t_{si} t_{ox}}$ | $\frac{L}{2\lambda_{DG}}$ |
| CSG MOSFET [125] | $PPA$ | Silicon and oxide | $\sqrt{2\varepsilon_{si} t_{si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) + 2\varepsilon_{ox} t_{si}^2}$ | $\frac{L}{2\lambda_{CSG}}$ |
| **CSDG MOSFET (Proposed)** | $PPA$ | Silicon and oxide | $\sqrt{\frac{\varepsilon_{si}(t_{si}-2a)^2 \ln\left(1+\frac{2t_{ox}}{(t_{si}-2a)}\right)+2\varepsilon_{ox} t_{si}(t_{si}-2a)}{16\varepsilon_{ox}}}$ | $\frac{L}{2\lambda_{CSDG}}$ |

### 3.3.1 Variation in Threshold Voltage Relative to Scaling Factor

The relationship between the natural length and gate length in multi-gate MOSFETs exhibits an exponential dependence on the variation in threshold voltage, particularly when aiming to minimize conduction in potential variation [126–128]. Hence, the correlation between the calculated natural length of the CSDG MOSFET and the threshold voltage roll-off can be expressed as follows:

$$\Delta\varphi_{min} \propto \Delta V_{th} \propto e^{\frac{L}{2\lambda_{CSDG}}} \tag{3.17}$$

Numerical simulations were conducted for the CSDG MOSFET, taking into account variations in silicon thickness and gate length as described in Equation (3.17). The natural length was calculated using Equation (3.16). To ensure the device operates within acceptable threshold voltage variations, it's crucial to carefully select the appropriate scaling factor.

### 3.3.2 The Drain Induced Barrier Lowering Characteristics of CSDG MOSFET

DIBL becomes notable when the drain voltage is increased from $0.1V$ to $1.0V$ while maintaining a constant threshold voltage, as indicated.

$$DIBL = V_{th}(V_{DS} = 0.1V) - V_{th}(V_{DS} = 1V) \tag{3.18}$$

According to ref. [125],to maintain a satisfactory DIBL value for all multi-gate MOSFETs, it is necessary to have a scaling factor greater than 2.2. Therefore, DIBL is contingent on the scaling factor value, which is tied to the natural length.

## 3.4 Results and Analysis

The authors have achieved the natural scaling of CSDG MOSFET, threshold voltage variations, and DIBL behavior. A comparison of the results has been made with different types of multi-gate MOSFETs, including SOI MOSFETs, DG MOSFETs, and CSG MOSFETs. Table 3.2 provides the list of parameters used in the analysis.

Table 3.2: Simulation Parameteric Values

| Device Parameters | Values |
|---|---|
| $a$ | 0.5 $nm$ to 3 $nm$ |
| $t_{ox}$ | 2 $nm$ |
| $t_{si}$ | 4 $nm$ to 10 $nm$ |
| $L$ | 0 $nm$ to 100 $nm$ |
| $b$ | 0.5 $nm$ to 8 $nm$ |

Figure 3.3 illustrates the relationship between the natural length of CSDG MOSFETs and variations in Silicon thickness. Also, the authors compared the Silicon thickness variation with respect to the internal and external gates. It is evident that as the Silicon thickness decreases, the natural lengths also decrease. This indicates a reduction in the influence of the drain on the channel, leading to increased controllability of the gates over the channel. Additionally, as the Silicon thickness continues to decrease, the natural lengths become nearly equal with respect to both the internal and external gates. This implies that with a thin Silicon thickness, the gates provide significant immunity over the channel while maintaining comparable electrostatic integrity.

However, as the Silicon film thickness increases, the outer gate demonstrates greater control over the channel. This implies that the internal gate is more prone to SCEs than the external gate. So, great care must be taking in selecting the minimal value for the internal radius to ensure effective immunity against SCEs.

The comparison between the natural length of the internal gate in CSDG MOSFET and those of other MOSFETs structures are presented in Figure 3.4. It is evident that device characteristics are determined by the variation in Silicon thickness concerning oxide thickness. As Silicon thickness decreases, the gates exhibit greater control over the channel. Furthermore, the natural scaling length of the internal gate in CSDG

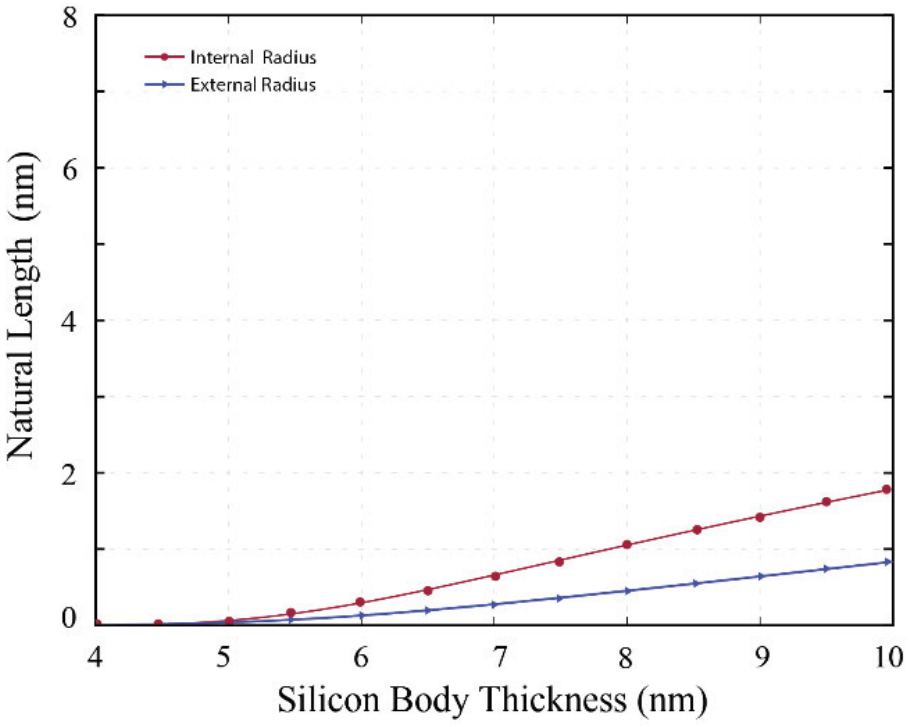


FIGURE 3.3: Relationship Between Natural Length and Silicon body thickness for the Internal and External Gates of CSDG MOSFET.

MOSFET is significantly smaller when compared to MOSFETs structures. Given that a smaller natural length is preferable for minimizing SCEs and subthreshold slope, CSDG MOSFET shows promise as a potential replacement for CSG MOSFET in the near future.

Figure 3.5 illustrates the relationship between threshold voltage variation and the scaling factor. Clearly, the CSDG MOSFET demonstrates the smallest threshold voltage roll-off, achieved at the highest extracted scaling factor ($\alpha$) of approximately 4.3. This is in comparison to other multigate MOSFETs. Consequently, the smaller natural length in CSDG MOSFET, which enables increased scaling factor, provides improved immunity against short channel effects (SCEs). Additionally, the numerical simulation aligns with the proposed analytical model, further supporting the findings.

Figure 3.6 shows a similar approach to Figure 3.5. When analyzing DIBL concerning the scaling factor ($\alpha$), it is apparent that reducing ($\alpha$) results in an increase in DIBL due to the reduction of the potential barrier in the channel resulting from the short channel. It is evident that the device structure with the lowest ($\alpha$) value is most affected, even though all devices maintain acceptable DIBL values of $< 50mV$, as illustrated in Figure 3.6. As the scaling factor value increases, $DIBL$ becomes virtually negligible.

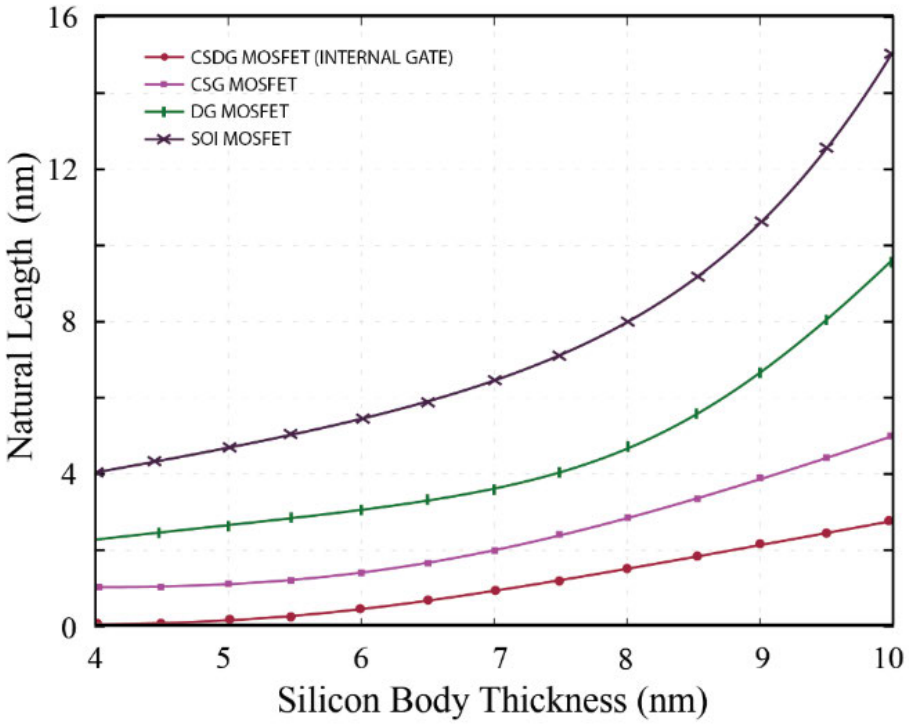


FIGURE 3.4: Natural Length of the Internal Gate in CSDG MOSFET Compared to other structures in relation to Silicon body thickness.

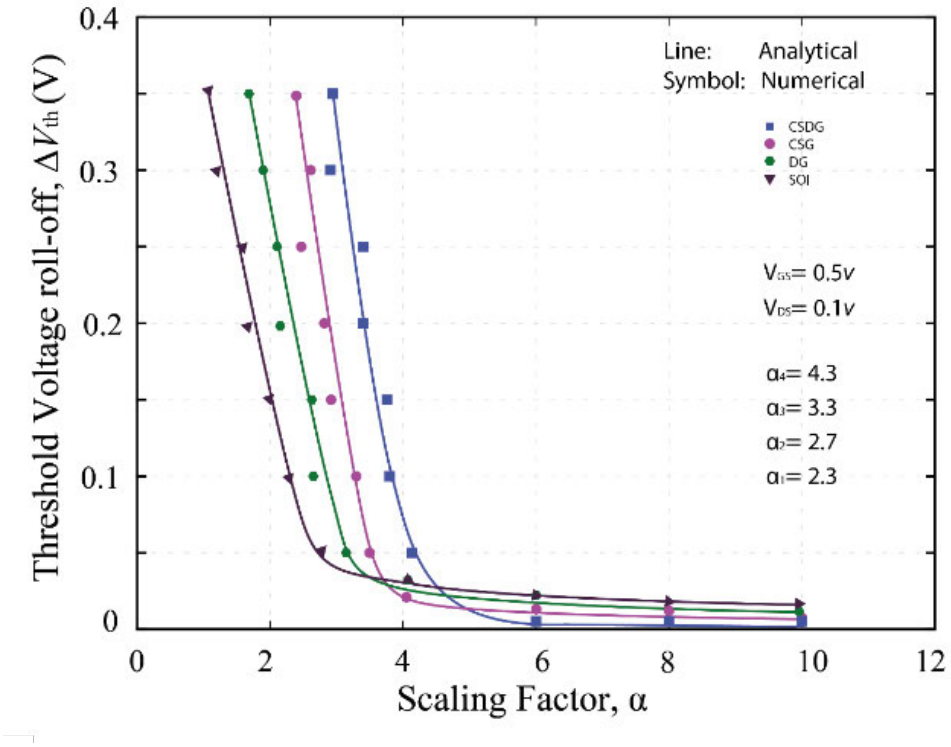


FIGURE 3.5: Threshold Voltage (Vth) roll-off and the scaling factor for various multi-gate devices, including CSDG MOSFET.

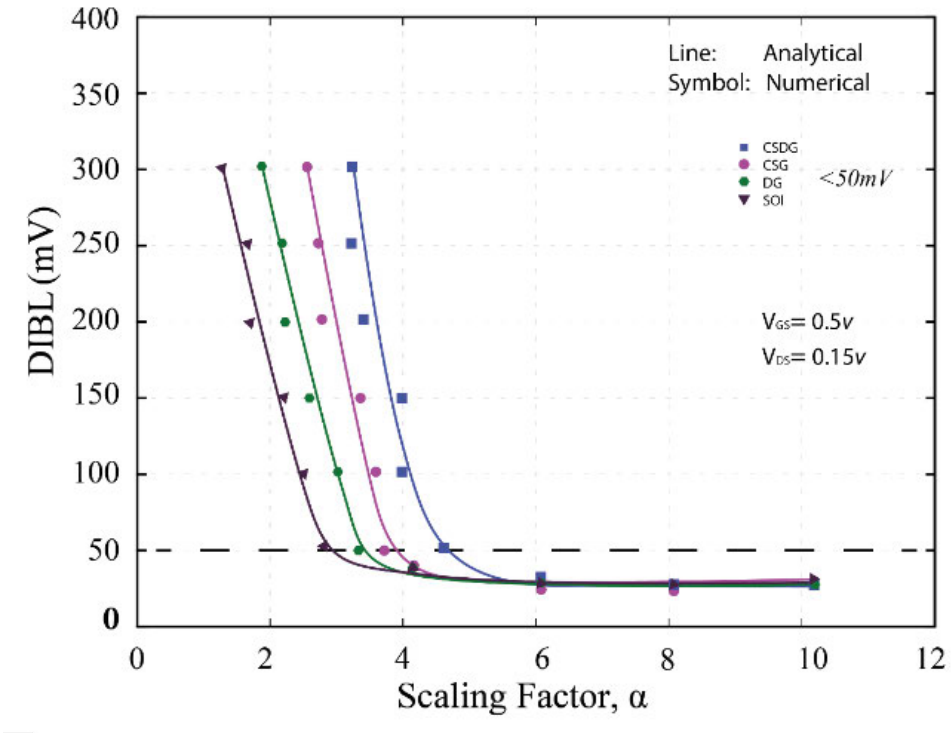


FIGURE 3.6: drain induced barrier lowering (DIBL) versus scaling factor for SOI, DG, CSG, and CSDG MOSFET.

## 3.5 Chapter Summary

In this chapter, the authors have conducted a comprehensive investigation to characterize the natural scaling length of CSDG MOSFETs, aiming to assess their potential for scaling based on internal and external gate electrostatics. The findings indicate that at higher Silicon thickness, the external gate exhibits a lower scaling factor compared to the internal gate. Consequently, the electrostatic influence of the external gate over the channel is greater than that of the internal gate. However, as the Silicon thickness decreases, both the external and internal gates demonstrate approximately equal control over the channel. Therefore, thinner Silicon thickness results in enhanced immunity against short channel effects (SCEs). Furthermore, the results highlight that CSDG MOSFETs exhibit the least scaling factor when compared to SOI, DG, and CSG MOSFETs.

In the following chapter, the quantum scaling length for CSDG MOSFET will be investigated based on quantum well confinement, and the result obtained will be compared with the classical natural length to further analyze the device behavior and obtain the minimum acceptable natural length for CSDG MOSFET.

# Chapter 4

# Quantum Scaling Length for CSDG MOSFET

At the nanoscale regime, the quantum mechanical effects (QMEs) cause a variation in the threshold voltage ($\Delta Vth$). The degree of this fluctuation depends on the multi-gate MOSFET structure. In this chapter, based on quantum well confinement with respect to the lowest electron energy level ($E_o$), a quantum scaling length has been developed for CSDG MOSFET within the Silicon body thickness.

## 4.1 Energy Level within a quantum well

The Schrödinger equation is utilized to examine the energy state within the quantum well, expressed as follows [129]:

$$E_n(K_xK_y) = \frac{\pi^2\hbar^2 n}{2m^* L_z^2} + \frac{\hbar^2}{2m^*}(K_x^2 + K_y^2) \qquad \Psi = \psi(z)e^{(iK_x x + iK_y Y)} \tag{4.1}$$

where n takes the values of 1, 2, ..., denoting the levels of confinement, $L_z$ represents the extent of confinement along the z-axis, $\Psi$indicates the potential well, $m*$ represents the effective mass, $E_n$ representes the energy level, and $e^{(iK_x x + iK_y Y)}$ describes the wave function of charges in the $x$ and $y$ directions.

By adopting a one-dimensional viewpoint and assuming a negligible potential well, Equation (4.1) can be simplified to derive the minimum energy level of electrons. This minimum energy level remains consistent across all multi-gate MOSFETs, as given [50].

$$E_0 = \frac{\pi^2 \hbar^2}{2m^* \Delta t_{si}^2} \tag{4.2}$$

At this energy level, $L_z = \Delta t_{si}$ and $n = 1$.where $E_0$ represents the lowest energy level for electrons,$L_z$ is the confinement dimension, $m*$ represent effective mass , and $\hbar$ is the reduced Planck's constant.

## 4.2 Confinement of Multi-Gate MOSFETs

The concept of quantum scaling length, derived from a one-dimensional analysis, has been universally established and characterized for all multi-gate MOSFETs as shown in Equation (4.3). This scaling length serves as a fundamental parameter in understanding and describing the quantum confinement effects that influence the behavior of these multi-gate transistor devices. The quantum confinement of multi-gate scaling length structures is given in Equation (4.3) [50]. This analysis establishes a consistent and comprehensive framework to assess and predict the quantum mechanical phenomena that arise within the structure of CSDG MOSFETs.

$$\lambda_Q = \left| \frac{K_B T}{\left(\frac{dE_0}{dt_{si}}\right)} \right| \tag{4.3}$$

where $E_0$ represents the lowest energy level for electrons, $K_B$ represents Boltzmann's constant, $T$ signifies the specific temperature measured in Kelvin, $t_{si}$ is the silicon thickness, and $\lambda_Q$ denotes the quantum scaling length of the device.

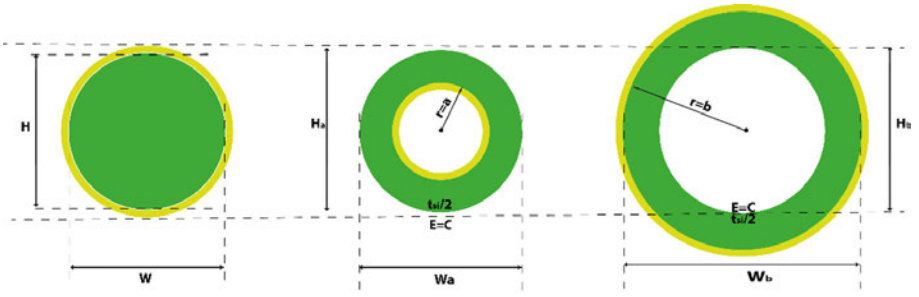


FIGURE 4.1: Cross-sectional perspectives of the CSG and CSDG MOSFETs with Gaussian Surface.

For the sake of simplicity, we have considered $H(height) = W(width) = \Delta t_{si}$ for the CSG MOSFET. Additionally, the radii of the CSDG structure are assumed as follows: for the internal radius, W$a = Ha = (tsi/2 - a)$, and for the external radius, $Wb = Hb = (b - tsi/2)$ as shown in Figure 4.1.

## 4.3 Quantum Natural Length Model for CSDG

In order to facilitate the straightforward determination of the quantum natural length associated with the CSDG MOSFET, we begin by deriving the correlation between the height and width of the CSG configuration in relation to this quantum parameter. Subsequently, by building upon this derivation, we establish a more comprehensive linkage between the structural attributes of the CSDG MOSFET and the quantum natural length. This stepwise approach not only simplifies the process of obtaining the quantum natural length for the CSDG MOSFET, but also enhances our understanding of the intricate relationship between device geometry and quantum effects.

$$\begin{aligned} \lambda_{Q_{CSG}} &= \left| \frac{K_B T}{\left(\frac{dE_0}{dH}\right)} \right| \Rightarrow \frac{dE_0}{dH} = \frac{k_B T}{\lambda_{Q_{CSG}}} \\ \lambda_{Q_{CSG}} &= \left| \frac{K_B T}{\left(\frac{dE_0}{dW}\right)} \right| \Rightarrow \frac{dE_0}{dW} = \frac{k_B T}{\lambda_{Q_{CSG}}} \end{aligned} \tag{4.4}$$

From Figure 4.1, it's obvious, $H(height) = W(width) = t_{si}$ for CSG MOSFET. Hence, Equation (4.4) can be expressed as

$$\frac{dE_0}{dH} = \frac{dE_0}{dW} = \frac{dE_0}{dt_{si}} = \frac{K_B T}{\lambda_{Q_{CSG}}} \tag{4.5}$$

By taking the derivative of Equation (4.5) and setting it equal to Equation (4.2), the quantum natural length for the CSG MOSFET can be expressed as:

$$\lambda_{Q_{CSG}} = \frac{K_B T t_{si}^3}{\pi^2 \hbar^2} \tag{4.6}$$

where $K_B$ represents Boltzmann's constant, $T$ signifies the specific temperature measured in Kelvin, $t_{si}$ is the silicon thickness, and $\lambda_{Q_{CSG}}$ denotes the quantum scaling length of the device for CSDG MOSFET.

Similarly, considering CSDG MOSFET structure from Figure 4.1, the lowest energy level of CSDG MOSFET is given as:

$$\frac{dE_0}{dt_{si}} = \underbrace{\frac{dE_0}{dH_a}\Delta H_a + \frac{dE_0}{dW_a}\Delta W_a}_{\textbf{Internal Radius}} + \underbrace{\frac{dE_0}{dH_b}\Delta H_b + \frac{dE_0}{dW_b}\Delta W_b}_{\textbf{External Radius}} \tag{4.7}$$

Equation (4.7) is further simplified with respect to the Gaussian surface, as given:

$$\frac{K_BT}{\lambda_{Q_{CSDG}}} = \underbrace{\frac{K_BT}{\lambda_{Q_{a_H}}}(\frac{t_{si}}{2} - a) + \frac{K_BT}{\lambda_{Q_{a_W}}}(b - \frac{t_{si}}{2})}_{\textbf{Internal Radius}} + \underbrace{\frac{K_BT}{\lambda_{Q_{b_H}}}(\frac{t_{si}}{2} - a) + \frac{K_BT}{\lambda_{Q_{b_W}}}(b - \frac{t_{si}}{2})}_{\textbf{Internal Radius}} \tag{4.8}$$

where $K_B$ represents Boltzmann's constant, and T is the temperature, and $\lambda_{Q_{a_H}}$, $\lambda_{Q_{a_W}}$, $\lambda_{Q_{b_H}}$, and $\lambda_{Q_{b_W}}$, are the quantum scaling length with respect to the internal and external radii's dimensions, respectively.

Upon substituting for $t_{si}$, Equation (4.9) is further simplified and equated to Equation 4.2 to derive the closed-form expression for quantum scaling length of CSDG MOSFET as given:

$$\lambda_{Q_{CSDG}} = \frac{K_BT(b-a)^3}{8\pi^2\hbar^2} \tag{4.9}$$

where $K_B$ represents Boltzmann's constant, $T$ signifies the specific temperature measured in Kelvin, $(b-a)$ is the silicon thickness, and $\hbar$ is the reduced Planck's constant.

Having successfully obtained the quantum scaling length of the CSDG device structure, a significant opportunity arises to delve into the intricacies of threshold voltage variation concerning this particular parameter. Through a comprehensive analysis, it becomes feasible to explore the nuanced interplay between the quantum scaling length and the changes in threshold voltage. This examination contributes to a deeper understanding of the complex relationship between device characteristics and quantum effects, ultimately paving the way for more informed design considerations and performance optimizations in electronic devices.

## 4.4 Scaling Factor at Quantum Level and Threshold Voltage Variation

At the quantum level, the variation in threshold voltage is intricately tied to the thermal voltage [50, 52]. This phenomenon can be explored through the given change in silicon body considerations.

$$\Delta_{V_{th}} = \frac{\Delta E_0}{q} = \frac{dE_0}{dt_{si}}.\frac{\Delta t_{si}}{q} = \frac{K_B T}{\lambda_{Q_{CSDG}}}.\frac{\Delta t_{si}}{q} = \frac{\Delta t_{si}}{\lambda_{Q_{CSDG}}}.\frac{K_B T}{q} \tag{4.10}$$

where $q$ denotes the electric charge, $K_B$ represents Boltzmann's constant, $T$ signifies the specific temperature measured in Kelvin, and $t_{si}$ is the silicon thickness.

The fluctuations in the Silicon body of CSDG MOSFET result in variations in the threshold voltage. Therefore, Equation (4.10) can be related to the change in Silicon body thickness as:

$$\Delta_{V_{th}} = \frac{K_B T}{q}.\frac{\Delta(b-a)}{\lambda_{Q_{CSDG}}} = V_T \frac{\Delta(b-a)}{\lambda_{Q_{CSDG}}} \tag{4.11}$$

where $V_T$ is the thermal voltage, and $\Delta(b-a)$ is the change in Silicon body thickness.

Equation (4.11) clearly indicates that the change in threshold voltage ($\Delta V_{th}$) is inversely linked to the CSDG MOSFET's natural length at the quantum level. A decrease in the natural length at the quantum level results in greater threshold variation due to QMEs. Furthermore, the quantum scaling factor (representing spatial confinement) of the CSDG MOSFET relies on the values of the external and internal radii, which are provided as follows:

$$\beta = \frac{\Delta(b-a)}{\lambda_{Q_{CSDG}}} \tag{4.12}$$

where $V_T$ is the thermal voltage, and $\Delta(b-a)$ is the change in Silicon body thickness, and $\lambda_{Q_{CSDG}}$ is the quantum scaling factor.

This suggests that in order to achieve the highest scaling factor within CSDG MOSFET, it's necessary to minimize the quantum natural length. By doing so, the desired outcome can be obtained while staying within the desired threshold voltage range. A shorter quantum natural length, in essence, contributes to improved scaling capabilities, allowing for optimized performance while retaining control over the threshold voltage.

## 4.5 Results and Discussions

Equation (4.12) is employed to detect the sensitivity between the quantum scaling length and the thickness of the Silicon of CSDG MOSFET. This observation pertains to analyzing the CSDG MOSFET in the nanoscale realm. Moreover, the model offers a straightforward method to guarantee the device's operation while staying within permissible threshold voltage limits.

TABLE 4.1: The device Parametric Values

| Device Parameters | Values |
|---|---|
| $t_{ox}$ | $fixed\ at\ 1\ nm$ |
| $a, b$ | 4 $nm$ to 10 $nm$ |
| $m_z^*$ | 0.98 $m_e$ |
| $N_a$ | $10^{17}\ cm^-3$ |
| $V_{DS}$ | 0.05 $V$ |
| $H = W = t_{si}$ | 4 $nm$ to 10 $nm$ |
| $V_{DS}$ | 0.05 $V$ |
| $K_B$ | $1.38X10^-23\ m^2kgs^-1k^-1$ |
| $\hbar$ | $6.626X10^-34\ m^2kgs^-1$ |
| $T$ | 300 $K$ |

Figure 4.2 displays the graphical representation illustrating the relationship between the variation in Silicon body thickness as a function of the quantum scaling and natural length. The solid lines represent the performance of the CSDG MOSFET in relation to both quantum scaling length and classical natural length as the variation in Silicon body thickness increases. In contrast, the dashed lines depict the outcomes for the CSG MOSFET. Analyzing the movement from the right to the left along the x-axis and focusing on the smaller circled region below, it becomes evident that, at any given point of thickness variation in the Silicon body, the CSDG MOSFET exhibits a smaller natural length than the CSG MOSFET. This implies that the CSDG MOSFET has superior resistance to short-channel effects compared to the CSG MOSFET. Furthermore, these findings affirm that the CSDG MOSFET offers more effective gate control in comparison to the CSG MOSFET at a quantum level.

However, when examining the upper larger circled region on the same Figure 4.2 and moving from left to right, you can observe the quantum scaling length at various points of variation in the Silicon body thickness. It's clear that CSDG MOSFETs exhibit a smaller quantum natural length compared to CSG MOSFETs. This indicates stronger quantum confinement, which, as stated in Equation (4.11), leads to greater threshold voltage variation. This suggests that CSG MOSFETs will effectively mitigate QMEs due to their weaker quantum confinement compared to CSDG MOSFETs. It's clear that both the quantum natural length and classical natural length play a significant role in determining the fundamental scaling theory necessary for designing CSDG MOSFETs at the quantum level. To achieve improved electrostatic control over the channel of CSDG MOSFETs at the quantum level, there must be a balance between the quantum natural length, classical natural length, and the Silicon body thickness of CSDG MOSFETs.

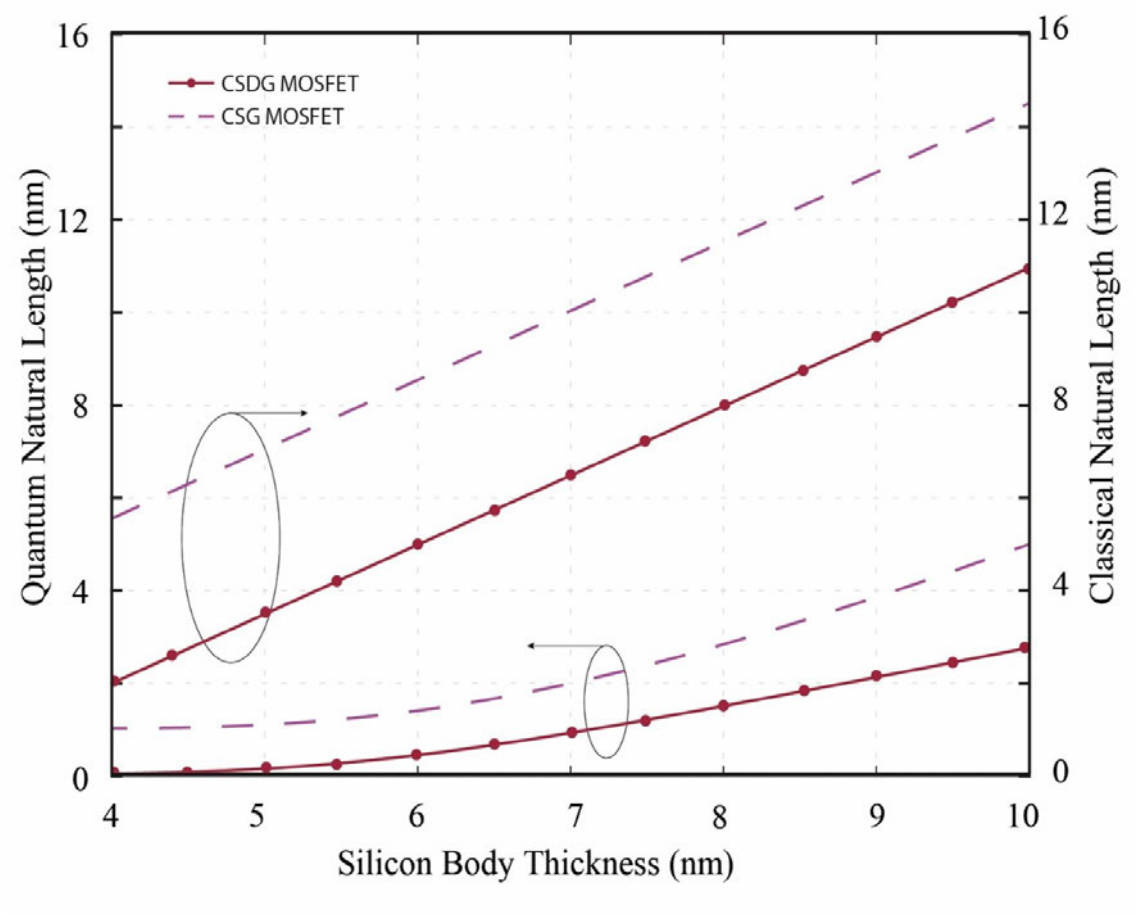


FIGURE 4.2: Variation in Silicon Body Thickness and Its Effect on Quantum and Classical Natural Lengths in CSDG and CSG MOSFETs.

In order to achieve the optimal balance for CSDG MOSFETs, Figure 4.3 presents a graph illustrating the interplay between quantum natural length and classical natural length for both CSDG MOSFETs and CSG MOSFETs. It becomes evident from this graph that both quantum and classical natural lengths serve as valuable indicators for

determining the minimal natural length required for effective device performance in CSDG MOSFETs.

Assuming that the threshold voltage ($\Delta_{V_{th}}$) variation is equal to the thermal voltage, an equivalence arises wherein the Quantum natural length ($\lambda_{Q_{CSDG}}$) must match the change in Silicon body thickness, $\Delta(b-a)$ (as detailed in Equation (4.12)). Moreover, in Figure 4.3, a pronounced exponential ascent is observed at a quantum natural scaling length of 0.5 $nm$, corresponding to $\Delta(b-a) = 0.5\ nm$ (when $(\Delta V_{th}) = V_T$). As a result, the minimum effective natural length for CSDG MOSFETs, as deduced from Figure 4.3, is $\lambda_{CSDG(min)} = 2.3\ nm$. Applying a similar methodology to the CSG MOSFET, the derived value for $\lambda_{CSDG(min)} = 2.7\ nm$.

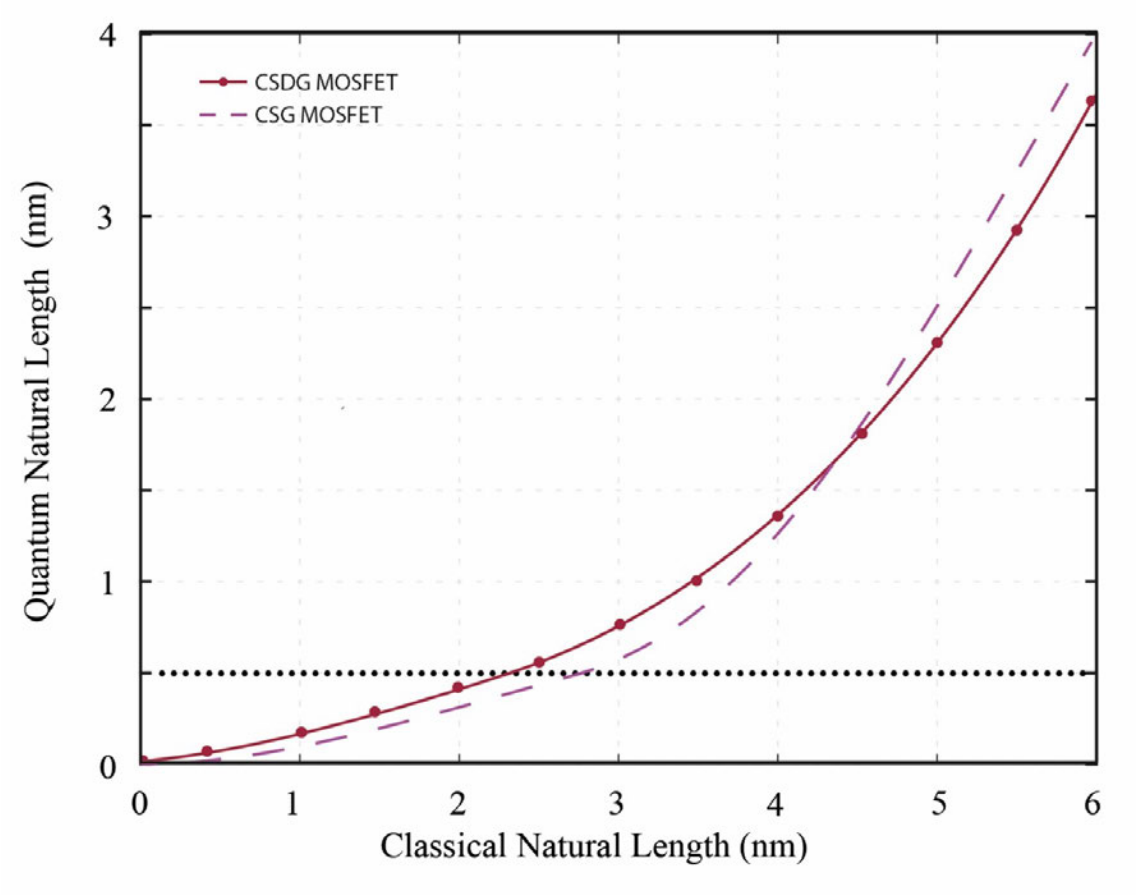


FIGURE 4.3: Comparison of Quantum Natural Length vs. Classical Natural Length in device MOSFETs structures.

Upon comparing the minimum effective natural lengths of these device structures, it becomes evident that CSDG MOSFETs have the smallest value. Consequently, CSDG MOSFETs are the preferred choice over CSG MOSFETs at the quantum level. The higher minimum value for CSG MOSFETs indicates that weak quantum confinements will diminish significantly more compared to CSDG MOSFETs, as illustrated in Figure 4.3.

Figure 4.4 illustrates the threshold voltage variation due to quantum mechanical effects as a function of the quantum scaling factor. Remarkably, CSDG MOSFETs, despite their smaller nanoscale dimensions, exhibit a similar threshold voltage variation behavior within the allowable quantum scaling factor when compared to the larger natural length of CSG MOSFET. This observation suggests that CSDG MOSFETs can effectively mitigate QMEs at the quantum level and that both the quantum scaling factor and the classical natural lengths are essential for controlling the short-channel effects and QMEs in the device structure.

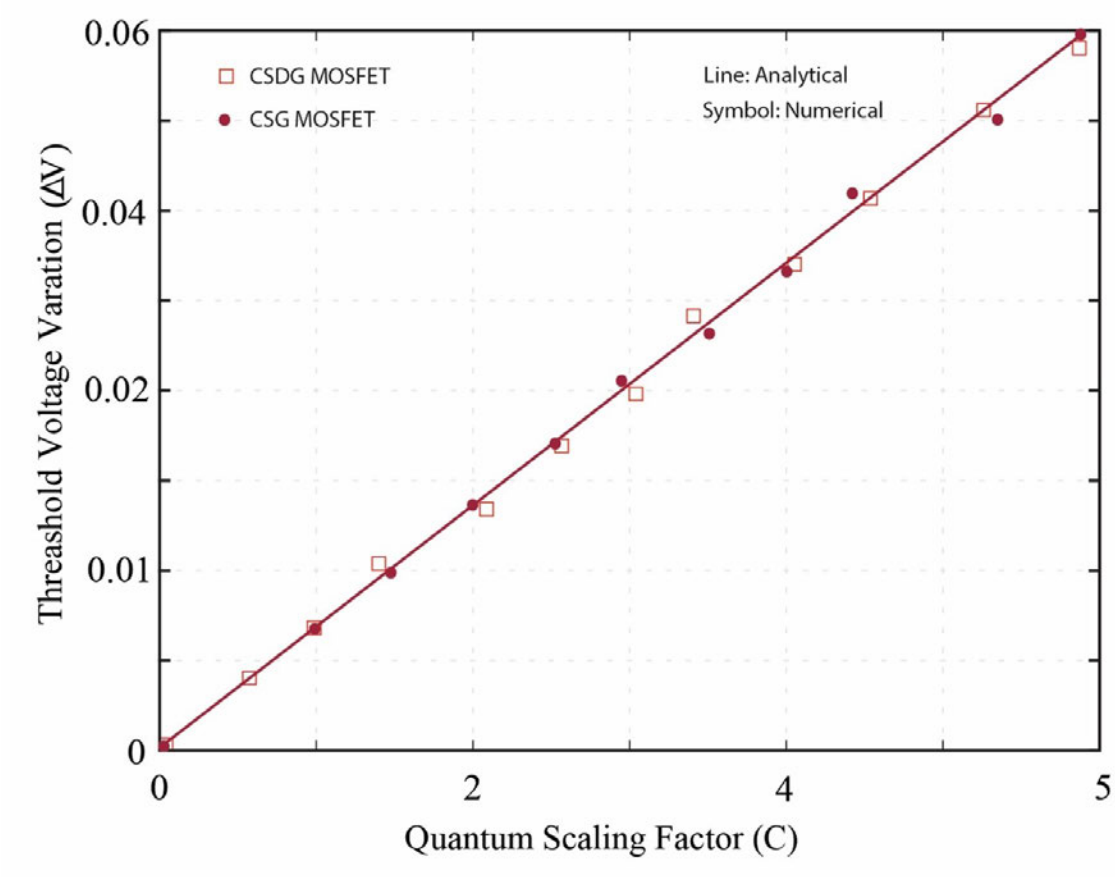


FIGURE 4.4: Threshold voltage variation due to Quantum Mechanical Effects (QMEs) for Considered MOSFET devices, as a function of the quantum scaling factor.

The minimum natural length represents the permissible channel length that is resistant to short-channel effects. Moreover, the variations in threshold voltage become more prominent due to quantum mechanical effects as the device size decreases. The analytical model is consistent with the numerical simulations.

## 4.6 Chapter Summary

In this research, we have introduced the quantum scaling length model and quantum scaling factor through a quantum confinement approach. By evaluating the performance of CSDG MOSFETs, we have determined the scaling limit for these devices by analyzing the interplay between their quantum natural length and classical natural length. Upon comparison with CSG MOSFETs, the results demonstrate that CSDG MOSFETs exhibit enhanced device characteristics at the quantum level.

With the minimum natural length and quantum scaling length established, the following chapter delves into the analytical structural modelling of CSDG MOSFET, taking into account the device geometry's radius and the source and drain along the z-axis. This approach addresses the impact of random dopant fluctuations resulting from doping to ensure a more comprehensive analysis.

# Chapter 5

# The Process Variation Sensitivity of CSDG MOSFETs

## 5.1 Introduction

This chapter comprehensively explores the sensitivity of the CSDG MOSFET to variations via analytical approach. It leverages the center potential solution derived in the preceding chapter to elucidate the potential distribution within CSDG MOSFETs. The findings were subsequently validated through rigorous numerical simulations. Furthermore, the study extends its scope by comparing these results to those of a promising multi-gate semiconductor device called CSG MOSFETs.

The investigation encompasses both lightly and heavily doped CSDG MOSFETs, subjecting them to scrutiny regarding their resilience in the face of parameter variations, such as alterations in channel length and silicon thickness, as well as the stochastic effects of Random Dopant Fluctuations (RDFs). This assessment is conducted in parallel with CSG MOSFETs, providing a comprehensive comparative analysis of the two MOSFET device types.

Applying the cylindrical coordinate system to Poisson's equation results in the calculation of the two-dimensional channel potential over the radial (r) and vertical (z) dimensions as stipulated by reference [130, 131] and illustrated in Figure 5.1, under the assumptions of uniform channel doping and the channel potential's angular independence, the complex 3D structure can effectively be treated as a simplified two-dimensional problem, mirroring the essence of Equation (3.1).

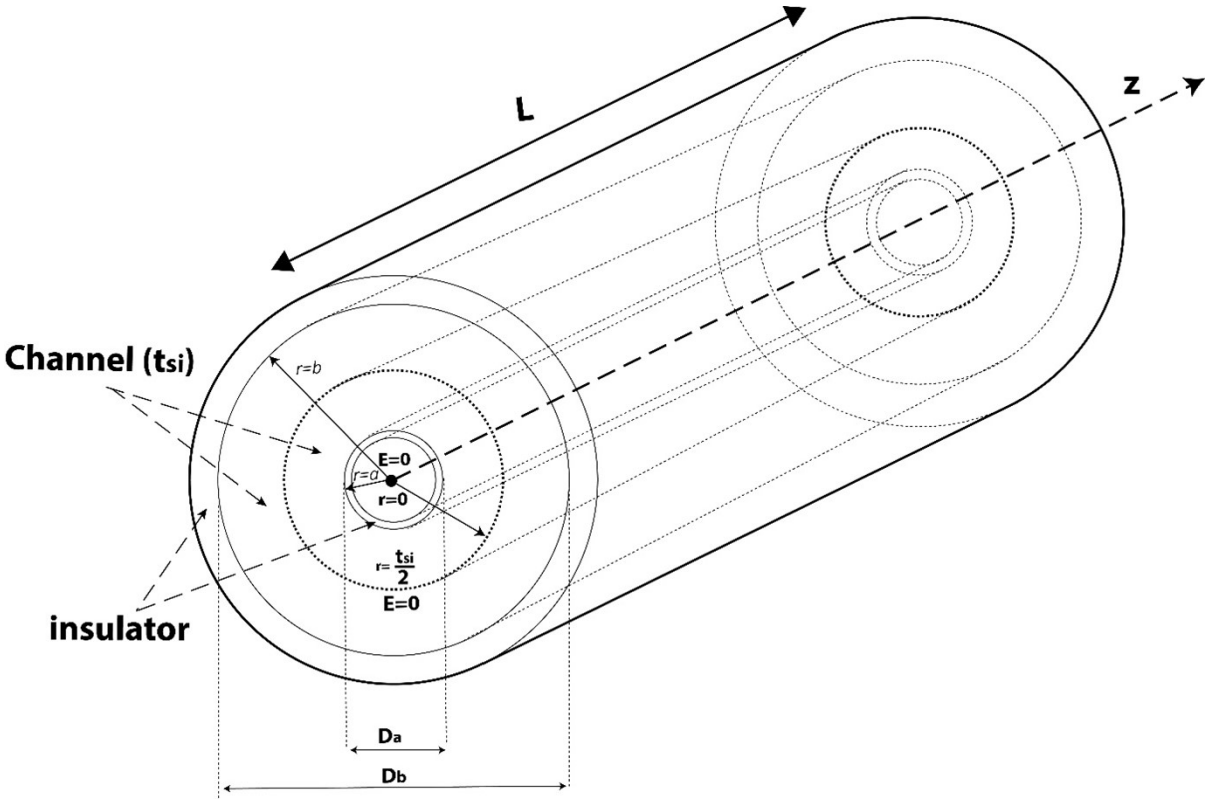


FIGURE 5.1: Illustration of the CSDG MOSFET depicting the channel thickness regarding the internal gate and external gate

Using the parabolic Equation and considering the joint effect of the two gates when biased simultaneously, The potential distribution along the z-axis demonstrates a parabolic profile. It is written as:

$$\psi_{CSDG}(r,z) = C_{0m}(z) + C_{1m}(z)r + C_{2m}(z)r^2 \quad (a \leq r \leq b) \tag{5.1}$$

In the context of the CSDG MOSFET, the designation "$m = 1$" pertains to the internal potential, characterized by arbitrary constants denoted as$(C_{01}, C_{11}, and\ C_{21})$. On the other hand,"$m = 2$" corresponds to the external potential and involves arbitrary constants represented as $(C_{02}, C_{12}, and\ C_{22})$. These arbitrary constants are determined by utilizing boundary conditions, as illustrated in Figure 5.1. The electric potential and electric field within the device's structure facilitate the analytical computation of the potential distribution.

## 5.2 Arbitrary Constants, $C_{01}$ and $C_{02}$

The derivation of $C_{01}$ and $C_{02}$ along the z-axis with respect to the Electric Potential is detailed in this section.

**Condition 1**: The built-in potential ($v_{bi} = 0$) due to a silicon pile at the device structure's origin, as depicted in Figure 5.1. Mathematically, the built-in potential can be expressed as [132]:

$$v_{bi} = \frac{K_B T}{q} \ln \frac{N_a}{n_i} \tag{5.2}$$

**Condition 2**: Taking into account the potential distribution in the vicinity of the source area around the silicon pile within the CSDG MOSFET and the drain region, the expression of the effect of the built-in potential on the CSDG structure is given as:

$$\begin{aligned} \psi_{CSDG}(r, z = 0) &= v_{bi} \\ \psi_{CSDG}(r, z = 0) &= v_{bi} + V_{DS} \end{aligned} \tag{5.3}$$

The potential at any location along the z-axis is derived from Equation (5.1) in the following manner:

$$\begin{aligned} C_{01}(z) + C_{11}(z)r + C_{21}(z)r^2 &= \frac{K_B T}{q} \ln \frac{N_a}{n_i} \\ C_{02}(z) + C_{12}(z)r + C_{22}(z)r^2 &= \frac{K_B T}{q} \ln \frac{N_a}{n_i} \end{aligned} \tag{5.4}$$

By solving Equation 5.4, It is possible to reduce the arbitrary coefficients in this way:

$$\Big[C_{01}(z) - C_{02}(z)\Big] + \Big[C_{11}(z) - C_{12}(z)\Big]r + \Big[C_{21}(z) - C_{22}(z)\Big]r^2 \tag{5.5}$$

Equation (5.5) is further simplified as given

$$\begin{bmatrix} C_{01}(z) & C_{02}(z) & 0 \\ C_{11}(z) & C_{11}(z) & 0 \\ C_{21}(z) & C_{22}(z) & 0 \end{bmatrix} \begin{bmatrix} 1 \\ r \\ r^2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{5.6}$$

The Equation (5.6) provides information about the arbitrary coefficients associated with the potential distribution in the CSDG MOSFET. The equation indicates that $C_{11}(z)$ and $C_{12}(z)$ are equal, and likewise, $C_{21}(z)$ and $C_{22}(z)$ share the same values for both

the internal and external gate regions of the device structure. However, the coefficients $C_{01}(z)$ and $C_{02}(z)$ are unique to the internal and external gates, respectively. These coefficients are influenced by the specific potential conditions at the surfaces of the internal and external gates.

To calculate $C_{01}(z)$ and $C_{02}(z)$, we applied the boundary condition at the Silicon interface. Hence, these distinct arbitrary coefficients for both the internal and external gates are given as

**Surface Potential due to internal gate**

$$\begin{aligned}\left(\psi_{CSDG}(a,z)\right)\Big|_{\left(r=\frac{t_{si}}{2}-a\right)} &= C_{01}(z)+C_{11}(z)r+C_{21}(z)r^2=\psi_a(z)\\ C_{01}(z) &= \psi_a(z)-C_{11}(z)\left(\frac{t_{tsi}-2a}{2}\right)+C_{21}(z)\left(\frac{t_{tsi}-2a}{2}\right)^2\end{aligned} \tag{5.7}$$

**Surface Potential due to external gate**

$$\begin{aligned}\left(\psi_{CSDG}(b,z)\right)\Big|_{\left(r=\frac{2b-t_{si}}{2}\right)} &= C_{02}(z)+C_{12}(z)r+C_{22}(z)r^2=\psi_b(z)\\ C_{02}(z) &= \psi_b(z)-C_{11}(z)\left(\frac{2b-t_{tsi}}{2}\right)+C_{21}(z)\left(\frac{2b-t_{tsi}}{2}\right)^2\end{aligned} \tag{5.8}$$

Equation 5.7 and Equation 5.8 shows the electric potential distribution.

## 5.3 Arbitrary Constant, $C_{11}$, $C_{12}$, $C_{21}$, and $C_{22}$

The derivation of $C_{11}$, $C_{12}$, $C_{21}$, and $C_{22}$ along the z-axis with respect to the Electric Field is detailed in this section,

To avoid repetition, through the process of differentiating the electric potential [133], it is possible to determine the electric field. Subsequently, this allows us to derive the values of the remaining arbitrary coefficients, specifically$C_{11}(z) = C_{12}(z)$ and $C_{21}(z)$= $C_{22}(z)$, as indicated below.

$$C_{21}(z) = \frac{C_{oxa}\Big(V_{GF} - \psi_a\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]} + \frac{C_{oxb}\Big(V_{GF} - \psi_b\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]}$$

$$C_{22}(z) = \frac{C_{oxa}\Big(V_{GF} - \psi_a\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]} + \frac{C_{oxb}\Big(V_{GF} - \psi_b\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]}$$

$$C_{11}(z) = \frac{\Big(2b - t_{si}\Big)\Big(t_{si} - 2a\Big)C_{oxa}\Big(V_{GF} - \psi_a\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]} + \frac{\Big(t_{si} - 2a\Big)\Big(C_{oxb} - C_{oxa}\Big)\Big(\psi_b - V_{GF}\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]}$$

$$C_{12}(z) = \frac{\Big(2b - t_{si}\Big)\Big(t_{si} - 2a\Big)C_{oxa}\Big(V_{GF} - \psi_a\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]} + \frac{\Big(t_{si} - 2a\Big)\Big(C_{oxb} - C_{oxa}\Big)\Big(\psi_b - V_{GF}\Big)}{\epsilon_{si}\Big[(t_{si} - 2a) - (2b - t_{si})\Big]} \tag{5.9}$$

where the voltage $V_{GF}$ = gate voltage ($V_G$) – Fermi Voltage ($V_F$). The gates capacitance ($C_{oxa}$ and $C_{oxb}$) has been previously defined in Chapter 3.

Equation (5.9) is integrated into Equation (5.7) and Equation (5.8) to compute the values of $C_{01}(z)$ and $C_{02}(z)$, and these coefficients are vital in establishing the interplay between the gates. The understanding of this interplay is crucial in the analysis of the potential distribution of the entire structure.

## 5.4 Derivation of Potential Distribution

The relations between the internal and external gate potential surface can be derived by substituting Equation (5.9) into Equation (5.7) and Equation (5.8). Through rigorous mathematical manipulations, the relationship between the gates is given in Equation (5.10). For a thorough understanding of the derivation process, please refer to the Appendix, which provides detailed explanations.

$$\begin{aligned} \psi_a(z) &= P_1\psi_b(z) + Q_1 V_{GF} \\ \psi_b(z) &= P_2\psi_a(z) + Q_2 V_{GF} \end{aligned} \tag{5.10}$$

The coefficients, $P_1$, $Q_1$, $P_2$, $Q_2$, are determined based on the values of the arbitrary constants. Detailed explanations of how these coefficients are derived can be found in the Appendix. The potential distribution can be obtained by substituting the values of the obtained arbitrary constants into Equation (5.1).

Since the potential distribution concerning both the internal and external gates has been determined, it can be represented in a standardized form as a second-order differential equation along the z-axis of the CSDG structure, as shown below.

$$\begin{aligned} \frac{d^2\psi_a(z)}{d^2z} - \sigma_1^2\psi_a(z) &= \alpha_1 P_1 \sigma_1^2 \\ \frac{d^2\psi_b(z)}{d^2z} - \sigma_1^2\psi_b(z) &= \alpha_1 \sigma_2^2 \end{aligned} \tag{5.11}$$

where the variables of the differential equations are obtained based on the arbitrary constants, and their expressions are given in the Appendix.

The general solution to Equation (5.11) is obtained based on [134, 135]. And it's given as

$$\begin{aligned} \psi_a(z) &= C_4 e^{\sigma_1 z} + C_5 e^{\sigma_1 z} - \alpha_1 \\ \psi_b(z) &= C_6 e^{\sigma_1 z} + C_7 e^{\sigma_1 z} - \alpha_2 \end{aligned} \tag{5.12}$$

The new arbitrary constants,$C_4$, $C_5$, $C_6$, and $C_7$, are dependent on the initial boundary conditions and constitute the linearly independent solution to the potential distribution along the r and z axis. They are obtained based on the boundary condition in Equation (5.3) and are given as

$$\begin{aligned} C_4 &= \frac{(v_{bi} + \alpha_1)(e^{-\sigma_1 L} - 1) - V_{DS}}{(e^{\sigma_1 L} - e^{-\sigma_1 L})} \\ C_5 &= \frac{(v_{bi} + \alpha_1)(e^{-\sigma_1 L} - 1) - V_{DS}}{(e^{-\sigma_1 L} - e^{\sigma_1 L})} \\ C_6 &= \frac{(v_{bi} + \alpha_2)(e^{-\sigma_2 L} - 1) - V_{DS}}{(e^{-\sigma_2 L} - e^{\sigma_1 L})} \\ C_7 &= \frac{(v_{bi} + \alpha_2)(e^{-\sigma_2 L} - 1) - V_{DS}}{(e^{\sigma_2 L} - e^{-\sigma_2 L})} \end{aligned} \tag{5.13}$$

The variables, $\sigma_1$, $\sigma_2$, $\alpha_1$, $\alpha_2$ are defined in the Appendix.

## 5.5 Current Derivation in CSDG MOSFET Struture

Now that we have determined the potential distribution of the device structures, we can calculate their subthreshold current using the established model presented by [136], as follows:

$$I_{DS} = \frac{\left[\mu W\left(KT/q\right)\left(n_i^2/N_a\right)\left(1 - e^{\left(\frac{-V_{DS}}{(\frac{KT}{q})}\right)}\right)\right]}{Z} \tag{5.14}$$

In this context, Z is contingent on the potential distribution derived from CSDG MOSFET. As a result, it can be expressed as:

$$Z = \int_0^L \frac{dz}{2\pi \int_0^{\frac{2b-t_{si}}{2}} \int_0^{\frac{2b-t_{si}}{2}} \left(re^{\left(\frac{\psi_{CSDG}(r,z)}{KT}\right)}\right) drdr} \tag{5.15}$$

The next section aims to explore how CSDG MOSFET responds to process variations to aid the CSDG manufacturing process in the nearest by employing an analytical approach. It is conducted after analyzing the potential distribution, since it plays a crucial role in the subsequent sensitivity analysis.

## 5.6 Variation in Process Parameters of CSDG MOSFET

This study represents the inaugural endeavor to investigate the susceptibility of both CSG MOSFET and CSDG MOSFET to variations in process parameters. This investigation was conducted using a well-established and practical lithography technique with a deviation of $\pm$ $3\sigma_c$, where $\sigma_c$ denotes the standard deviation. This particular technique is known to be applicable for the fabrication of MOSFET devices in real-world applications [137–139]. The deviations induced by this technique have analogous effects on the physical dimensions of CSG MOSFET and CSDG MOSFET, such as channel length and channel width, dictated by their respective geometries.

Furthermore, variations in threshold voltage are influenced by fluctuations in dopant concentrations. The assessment of threshold voltage, derived from the subthreshold current model, is instrumental in gauging the sensitivity to dopant fluctuations, presuming that the distribution of dopants adheres to the Poisson distribution. In this context, the standard deviation represents the mean value of dopant counts ($N_a$).

This thorough examination and methodology will facilitate the practical integration of CSDG MOSFETs in the near future, aligning with the recent recommendations made by the authors in [140], who have proposed a perspective for the fabrication of CSDG MOSFETs.

Figure 5.2 presents a comprehensive depiction of the three-dimensional CSDG MOSFET structures employed in device simulations. These structures were virtually fabricated utilizing a simulator designed for 45 nm technology. The modeling process utilized the principles of device physics to accurately represent these devices within the submicron technological framework, making use of the parameters outlined in Table 5.1. To assess and characterize the CSG and CSDG MOSFET devices, a device simulator was employed. These MOSFET devices were meticulously calibrated to meet the stringent low-power application requirements outlined in the ITRS, with an off-current of nearly 1 nanoampere per meter ($1nA/m$).

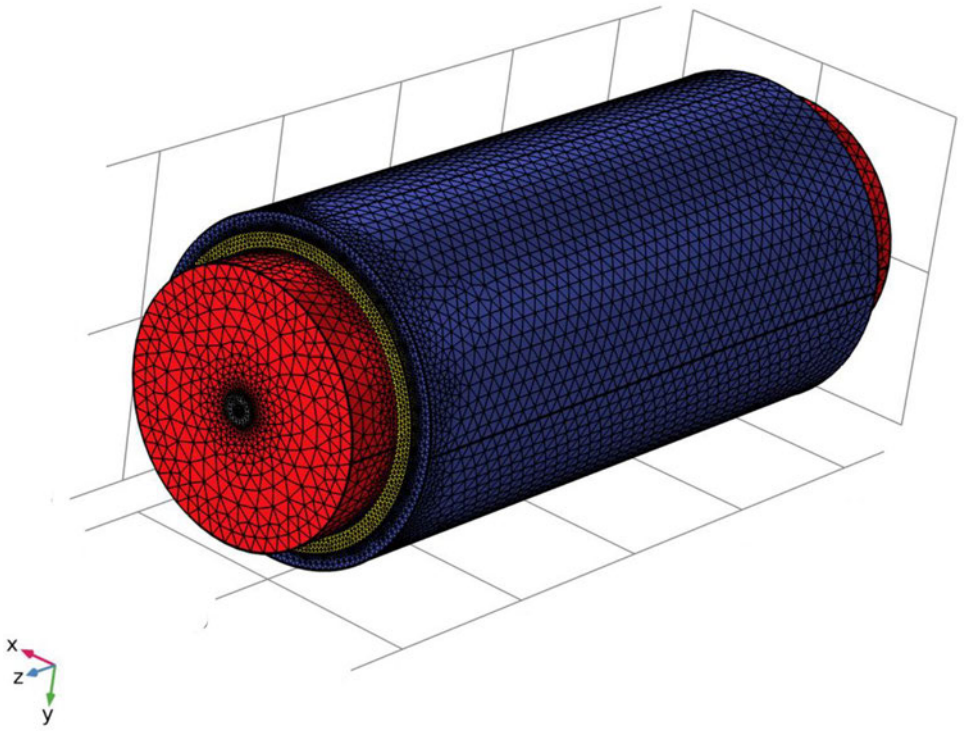


FIGURE 5.2: Mesh Diagram for Device Simulation of CSDG MOSFET.

## 5.7 Results and Discussion

To compare the process variation of CSG MOSFETs and CSDG MOSFETs, the widths (W) must be equal to make a fair comparison. The total width of CSG MOSFET is

$W_{TOTAL} = 2\pi(r)$ and that of CSDG MOSFET is $W_{TOTAL} = 2\pi(b-a)$ as shown in the Table 5.1, here a point to note is that $r = (b-a)$.

TABLE 5.1: Parameteric values Considered for TMGS CSDG MOSFET

| Symbol | Parameters | CSG MOSFET | CSDG MOSFET |
|---|---|---|---|
| $L$ | Channel Length | 20 nm | 20 nm |
| $a$ | Internal Radius | – nm | 4 nm |
| $b$ | External Radius | r=10 nm | 14 nm |
| $N_a^{++}$ | Heavy Channel Doping | $10^{18}$ $^{-}3$ | $10^{18}$ $cm^{-}3$ |
| $N_a^{+}$ | Light Channel Doping | $10^{17}$ $cm^{-}3$ | $10^{17}$ $cm^{-}3$ |
| $t_{ox}$ | Oxide Thickness | 1 nm | 1 nm |
| $HfO_2$ | Hafnium Oxide Thickness | 2 nm | 2 nm |
| $\Phi_M$ | Gate Work-Function | 4.8 $eV$ | 4.8 $eV$, |

The accuracy of the closed-form subthreshold current expression derived from Equation 5.14 has been rigorously confirmed through a comparison of the analytical model with simulation. Employing the drain current extraction technique, the authors have computed the threshold voltage by relying on the critical value of subthreshold current. This critical subthreshold current is contingent upon the device's channel width and gate length and is calculated as $I_{DS_{CRITICAL}} = 300\ nm \times (W_{TOTAL}/L)$ [141, 142].

For the assessment of threshold voltage values in both heavily and lightly doped CSG and CSDG MOSFETs, the authors have conducted drain-current extraction. Silicon oxide was taken into account as the oxide thickness for the heavily doped device structure, while Hafnium dioxide (HfO2) was considered as the dielectric constant for the lightly

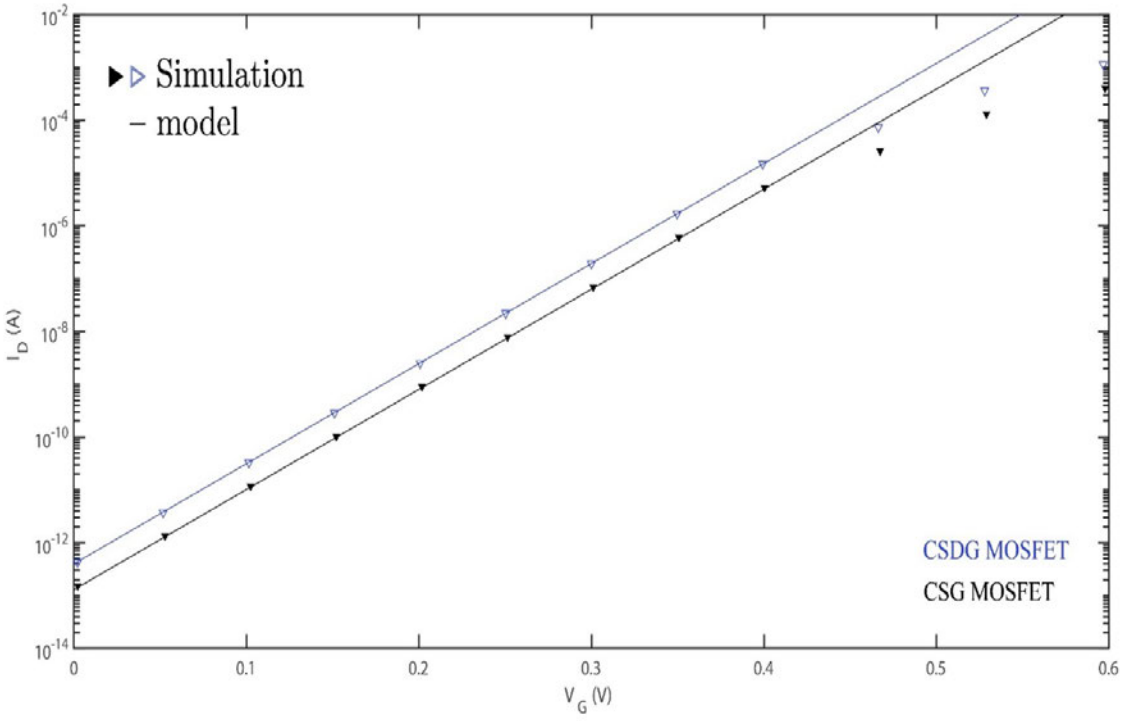


FIGURE 5.3: Subthreshold Current as a function of Gate Voltage for Lightly Doped device MOSFETs.

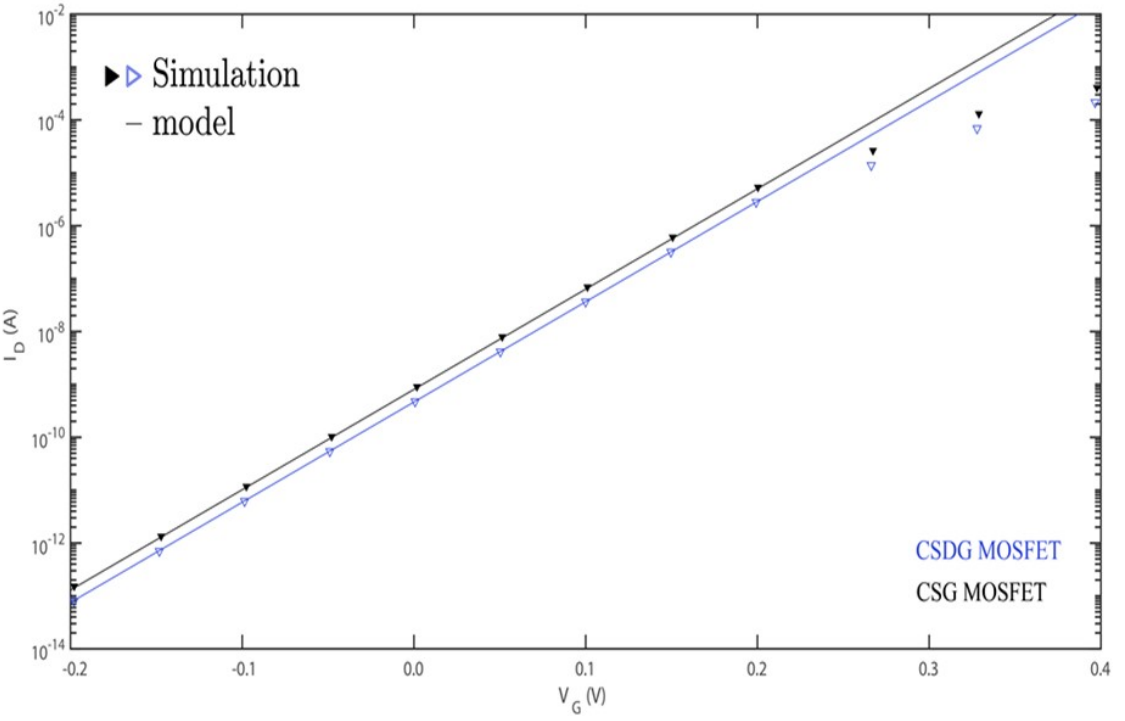


FIGURE 5.4: Subthreshold Current as a function of Gate Voltage for heavily doped device MOSFETs.

doped device structure due to its requirement of a lower equivalent oxide thickness. Hafnium dioxide has demonstrated excellent electrical performance, thermal stability, a high dielectric constant, and reduced leakage current when contrasted with silicon dioxide [143–147].

As indicated in Figure 5.3, it is evident that the threshold voltage value for both lightly doped CSG MOSFET and CSDG MOSFET is approximately 0.42 $V$. Conversely, for heavily doped CSG and CSDG MOSFETs, the threshold voltage, as illustrated in Figure 5.4, hovers around 0.22 $V$. It's important to note that the focus of this model is primarily on the subthreshold regime, ensuring accuracy for gate voltage ($V_{GS}$) below the threshold voltage ($V_{th}$). The results indicate that structures with lighter doping exhibit higher stability in terms of threshold voltage compared to heavily doped structures, showing lesser current leakage. The model's precision has been validated by comparing it with device simulations, demonstrating a high level of agreement between the two.

For the sake of meaningful comparison between the two devices, Figures 5.5, Figure 5.6, and Figure 5.7 have been employed to investigate the impact of channel length, variations in random dopant fluctuation, and channel thickness on the behavior of the threshold voltage in both CSG MOSFETs and CSDG MOSFETs. In the case of heavily doped devices, a dopant concentration of $110^{18}/cm3$ was introduced into the channel, while for the lightly doped device, a dopant concentration of 1 x 1 $\times$ $10^{17}/cm^3$ was utilized.

The results, as depicted in Figure 5.5, elucidate the fluctuation in threshold voltage stemming from random dopant variations, considering a channel width ($W_{total}$) of 65 $nm$ and a channel length of 20 $nm$. Notably, the effect of dopant fluctuation on the threshold voltage is marginally more pronounced in the case of CSDG MOSFETs in comparison to CSG MOSFETs. This discrepancy can be attributed to the larger surface area possessed by CSDG MOSFETs in relation to devices with an equivalent width. Consequently, for heavily doped CSDG MOSFET devices, the fluctuation in dopant numbers assumes a significant role that necessitates careful consideration during the fabrication process.

Figure 5.5 illustrates that heavily doped channels exhibit a more pronounced variation in threshold voltage compared to their lightly doped counterparts. These findings align closely with the numerical data. Additionally, Figure 5.6 delves into the behavior of threshold voltage in both CSG and CSDG MOSFETs concerning variations in Silicon thickness.

Notably, the results demonstrate that CSDG MOSFETs exhibit a narrower variation in threshold voltage for lightly doped channels when compared to CSG MOSFETs. This

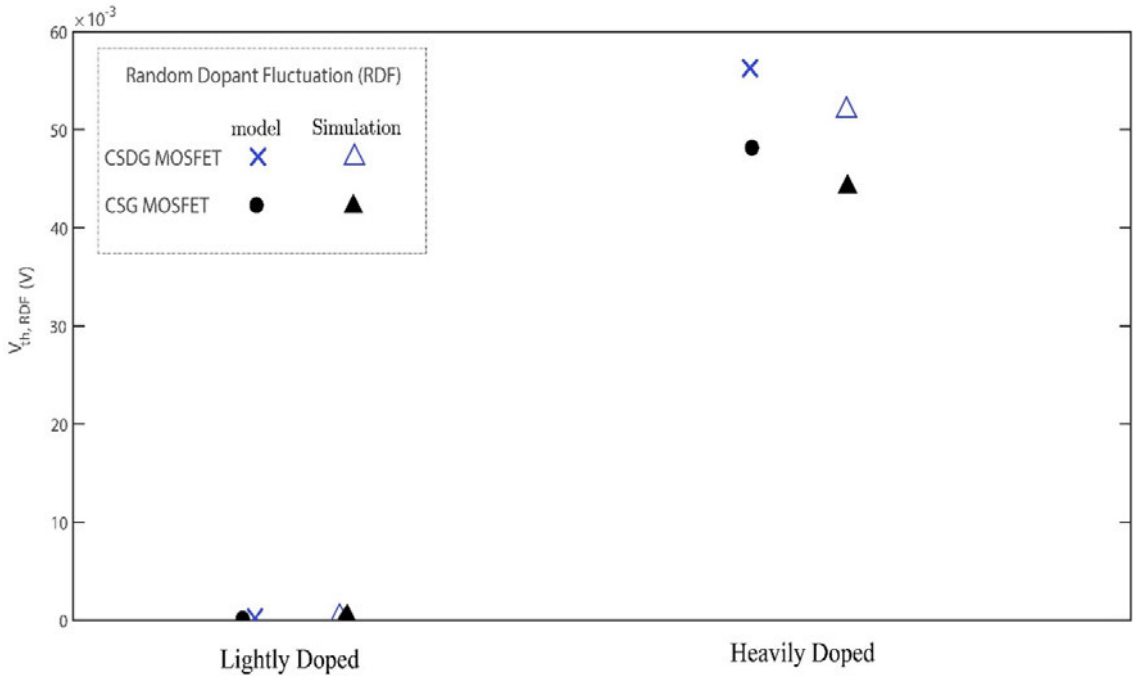


FIGURE 5.5: Influence of channel doping variation on the threshold voltage in device MOSFETs.

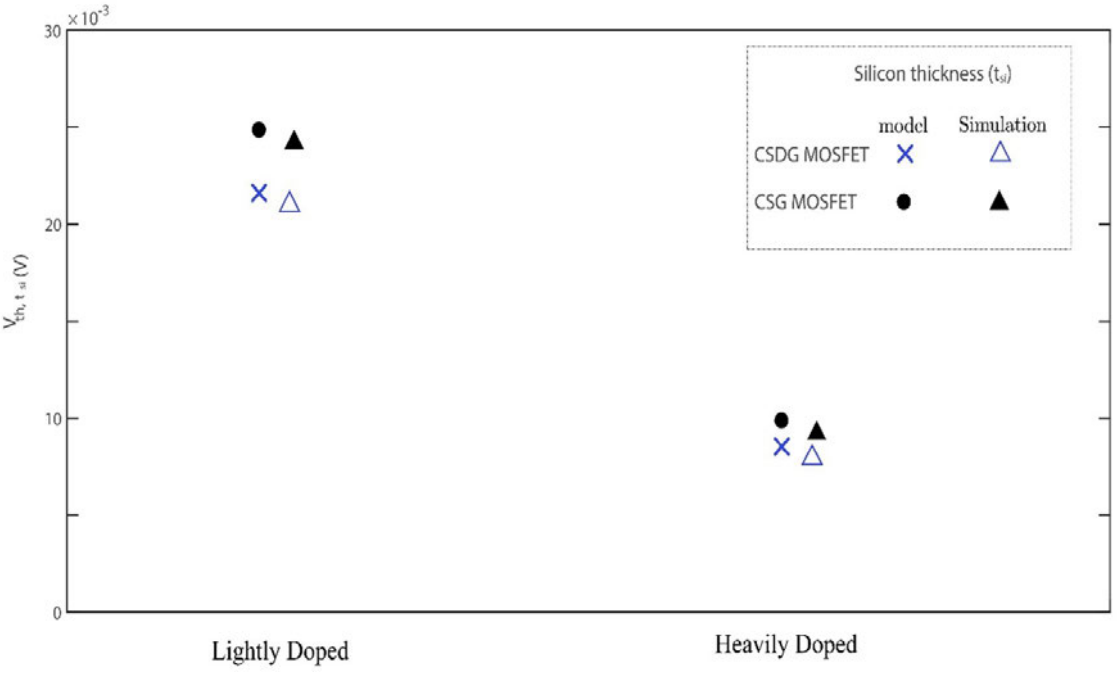


FIGURE 5.6: Influence of channel thickness variation on the threshold voltage in device MOSFETs

phenomenon can be attributed to the unique configuration of the double-gate structure, which offers enhanced electrostatic control over the channel in CSDG MOSFETs.

Conversely, for heavily doped channels, the effects of Silicon thickness variation are less pronounced.

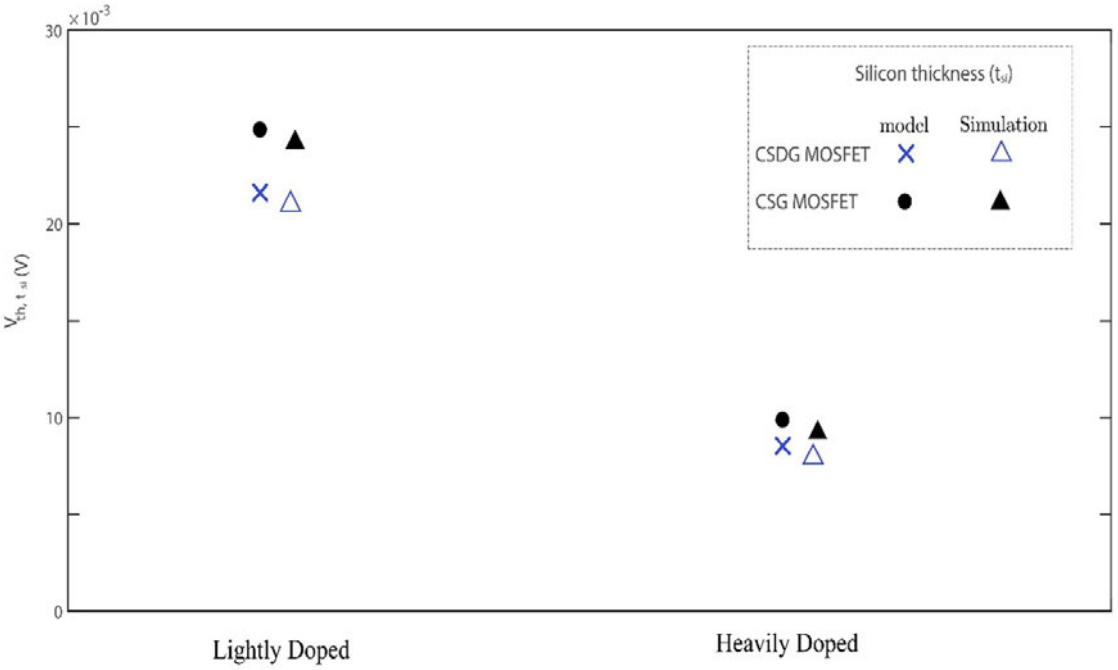


FIGURE 5.7: Influence of channel length variation on the threshold voltage in device MOSFETs.

Figure 5.7 presents an analysis of the impact of channel length variation on threshold voltage. Notably, the difference in threshold voltage between CSDG and CSG MOSFETs for heavily doped channels is minimal, to the extent that it may be considered negligible. This phenomenon can be attributed to the effect of heavy channel doping, which significantly reduces the device's dependence on gate controllability. However, in the case of lightly doped CSG MOSFET and CSDG MOSFETs, the disparity in threshold voltage is more subdued in CSDG MOSFETs as compared to CSG MOSFETs. This outcome can be attributed to the presence of the internal gate core within CSDG MOSFET, which contributes to this enhanced performance.

Figure 5.8 shows the threshold voltage roll-off characteristics of device MOSFETs structures for high doping channels. Both CSG MOSFET and CSDG MOSFET have the same roll-off characterization. This is because the heavily doped channel reduces the device's dependence on the channel's electrostatic control. In the lightly doped device structure shown in Figure 5.9. The threshold voltage roll-off for the MOSFET structures under consideration appears to be quite similar. Nevertheless, as the channel length is

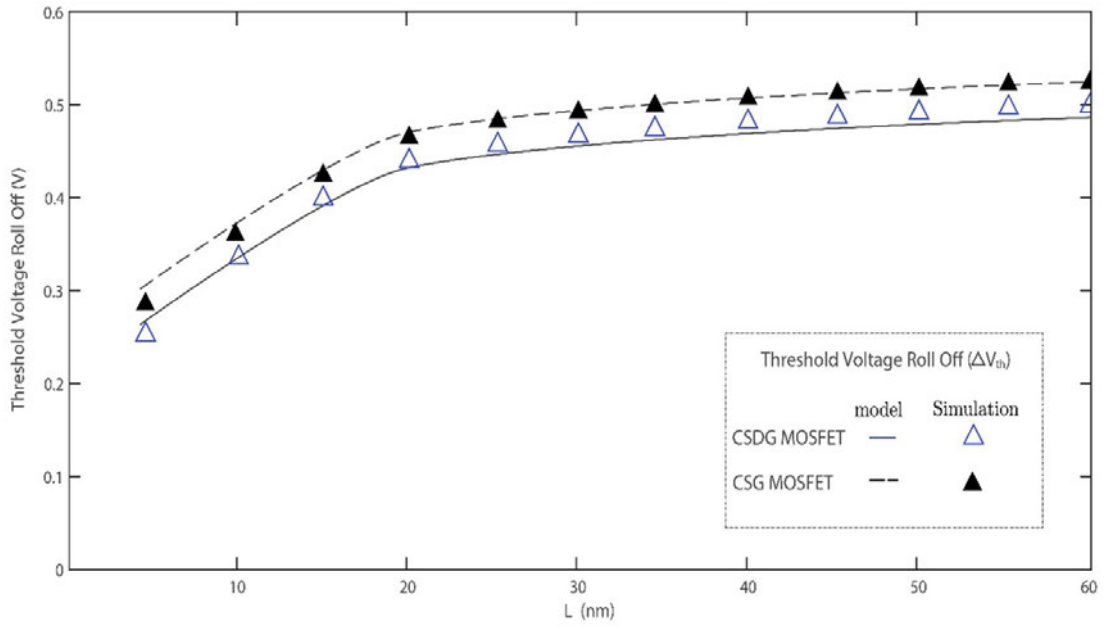


FIGURE 5.8: Threshold voltage roll-off behavior in device MOSFETs with high doping.

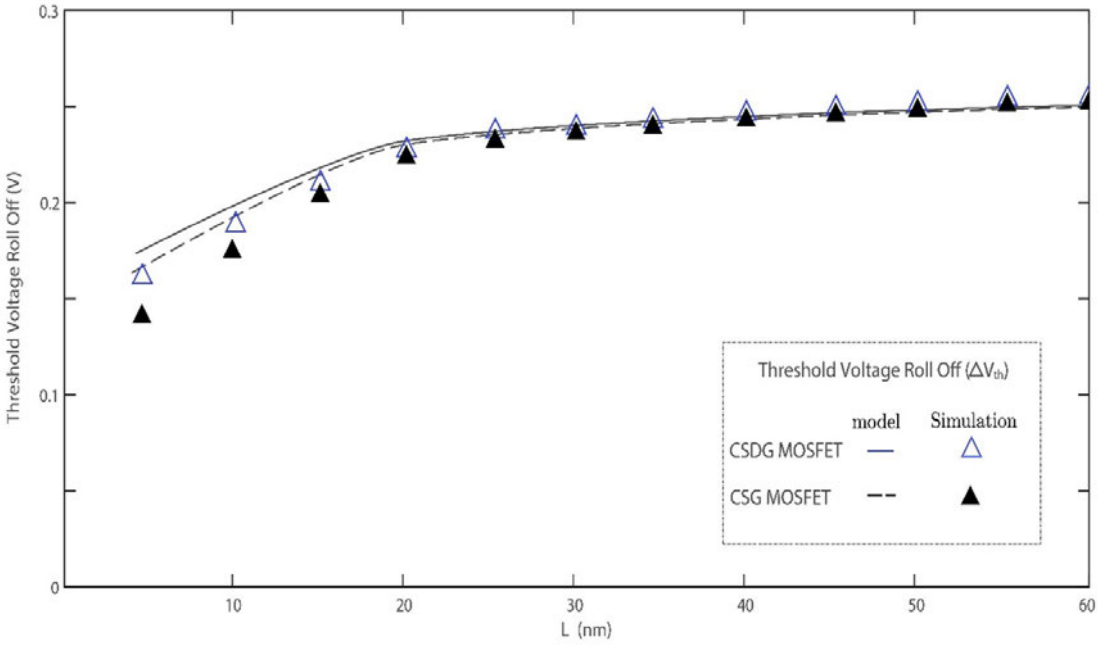


FIGURE 5.9: Threshold voltage roll-off behavior in device MOSFETs with low doping.

varied beyond a certain point, the threshold roll-off for CSG MOSFET is slightly lower 20 $nm$.

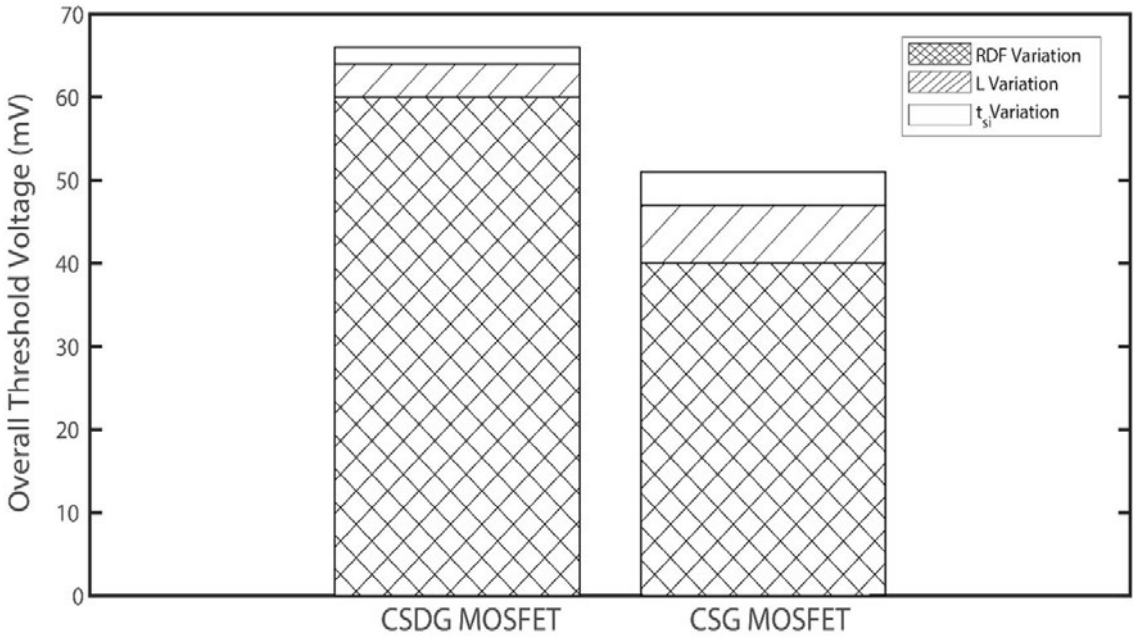


FIGURE 5.10: Comparison of total threshold voltage with other parameters for high doping

The comprehensive analysis of the overall threshold voltage variation attributed to source variations in the considered device MOSFET structures can be approached by considering that the variations in sources such as Random Dopant Fluctuation (RDF), channel length (L), and channel thickness ($t_{si}$) are mutually independent. Consequently, the cumulative effect of all these variation sources equates to the total threshold voltage variation ($V_{th}, Total$). This total threshold voltage variation serves as a key determinant of device sensitivity, and it can be represented as: $V_{th}, Total = |V_{th}, RDF| + |V_{th}, L| + |V_{th}, t_{si}|$.

Thus, in the context of heavily doped channels, the variation in threshold voltage concerning channel length and channel thickness is comparatively less influential, while the threshold voltage discrepancy primarily arises from the impact of RDF ($V_{th}, RDF$). Conversely, when examining the influence of channel length ($V_{th}, L$), the impact of $\Delta V_{th}$, $RDF$, RDF is negligible, and $V_{th}$, $t_{si}$ becomes less significant, with the overall threshold voltage dispersion being predominantly governed by $V_{th}, L$.

Furthermore, when evaluating variations due to silicon thickness ($V_{th}$, $t_{si}$), $V_{th}, RDF$ holds minimal significance, whereas $V_{th}, L$ becomes less substantial, as elucidated in Figure 5.10 and Figure 5.11.

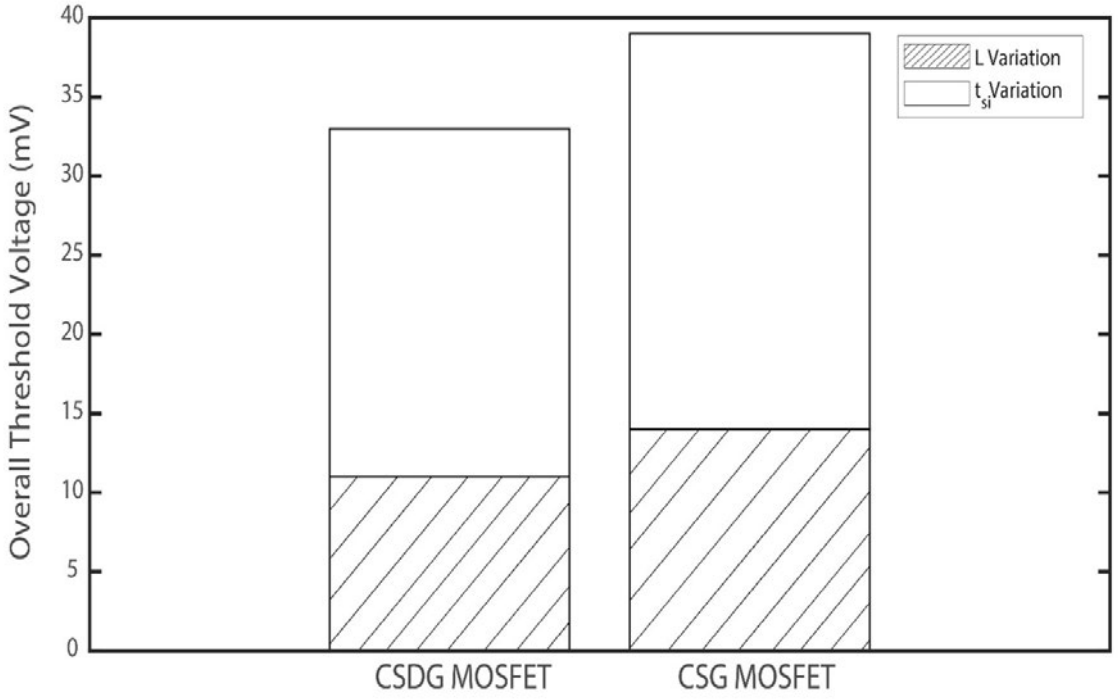


FIGURE 5.11: Comparison of total threshold voltage with other parameters for low doping

In essence, the analysis highlights that different factors contribute to the threshold voltage variation in these devices, and their relative importance varies depending on the specific source of variation under consideration.

## 5.8 Summary

This study employs the analytical solution of the 2-D Poisson equation for the considered MOSFET device structures. Verification through device simulations enables the analysis of their sensitivity to process variation. Notably, it has been observed that lightly doped CSDG MOSFET exhibits smaller threshold voltage variations than CSG MOSFET at the nanometer scale. Consequently, as MOSFET dimensions shrink, lightly doped devices exhibit increased immunity to process variation compared to heavily doped ones. Nonetheless, thanks to its lower threshold voltage value, the lightly doped CSDG MOSFET exhibits greater immunity compared to CSG MOSFET. Moreover, CSDG MOSFET demonstrates superior resistance to variations in channel thickness and channel length due to its inherent internal core and external gate controllability. As CSG MOSFET shows promise to replace FinFET and other multi-gate families, CSDG represents the next-generation semiconductor device for CMOS technology, primarily due to its remarkable features.

At long channel length, the heavy dopant effects on both CSG and CSDG MOSFETs are insignificant. However, the random dopant fluctuation (RDF) determines the overall threshold voltage variation as the channel length reduces. This is because the larger surface area of CSDG MOSFET to volume ratio contributes to its larger threshold voltage variation than CSG MOSFET. Hence, RDF is an essential factor that must be considered at nanometre range when designing heavily doped CSDG MOSFET devices. In the case of long channel lengths, the impact of heavy doping on both device MOSFETs structures is negligible. However, as the channel length decreases, the overall threshold voltage variation is primarily determined by random dopant fluctuation. This is attributed to the increased surface area-to-volume ratio of CSDG MOSFET, which results in a larger threshold voltage variation compared to CSG MOSFET. Therefore, RDF emerges as a critical factor to be taken into account when designing heavily doped CSDG MOSFET devices in the nanometer range.

Alternatively, a light dope CSDG with the concept of gate material engineering can be incorporated to achieve the best performance, as well as low consumption power, without much trade-off.

Following an in-depth analysis of the doping impact on CSDG MOSFET, the next chapter concentrates on mitigating short-channel effects of lightly doped CSDG MOSFET, particularly as the channel length decreases. This is achieved through advanced gate material and gate-oxide engineering techniques. The PPA model is further expanded to model the triple material gate CSDG MOSFET, incorporating both the radial direction and the source and drain along the z-axis of the device geometry.

# Chapter 6

# Design and Analysis of Stacked Triple Material-Gate (STMG) CSDG MOSFET

## 6.1 Introduction

In contrast to the doping engineering approach discussed in the preceding section, the current section introduces a novel technique for enhancing the device structure's potential distribution within the Stacked Triple Material-Gate (STMG) MOSFET with a high-K structure. This approach leverages gate-material engineering and gate-oxide engineering to achieve its objectives. Instead of relying solely on doping adjustments, this method strategically employs multiple gate materials with varying work functions to induce a potential step within the channel. The primary aim of this approach is to effectively mitigate short-channel effects and elevate the electric field at the source side of the transistor. A potential step that not only suppresses SCEs but also augments the efficiency of carrier transport within the channel region is introduced. As a result, the TMGS transistor with a high-K structure becomes more adept at facilitating the flow of charge carriers, leading to an overall enhancement in its performance and operational characteristics.

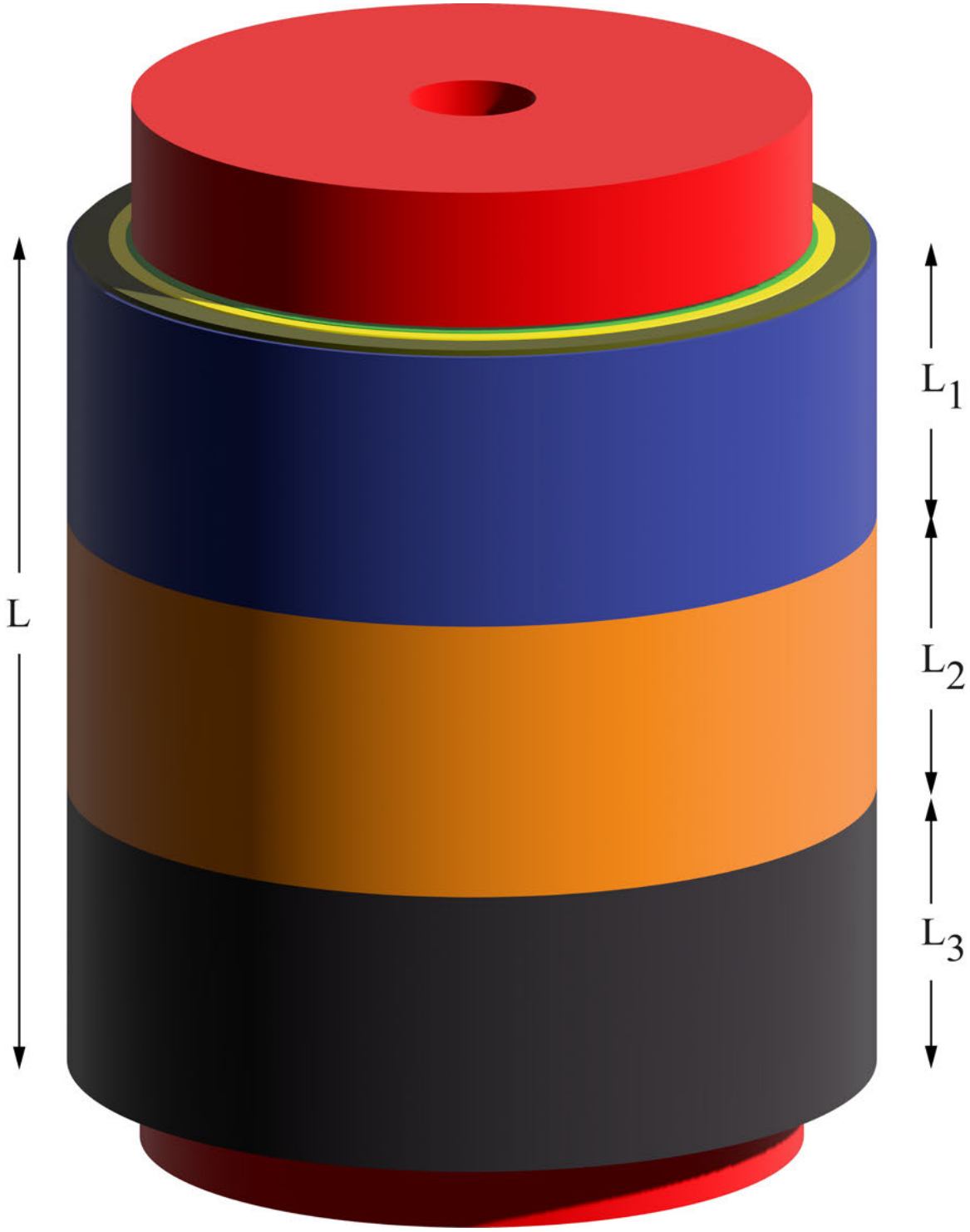


FIGURE 6.1: Proposed 3D view of Triple Material Gate Stacked (TMGS) CSDG MOSFETs.

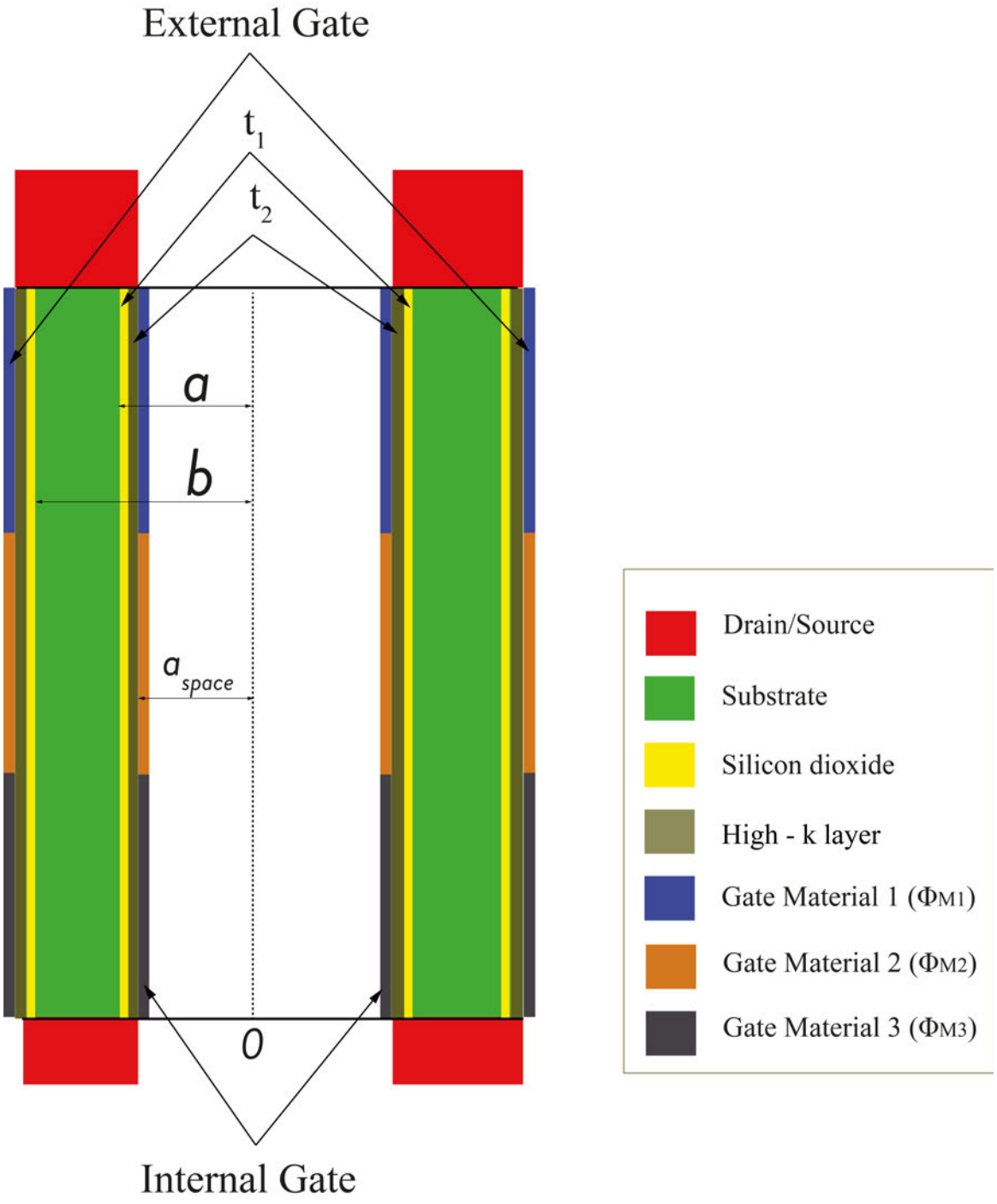


FIGURE 6.2: 2D Cross Sectional view of TMG CSDG MOSFETS.

## 6.2 STMG CSDG Device Structure Geometry - A Potential Distributor Competitor

The STMG CSDG MOSFETs, as envisioned in this proposal, feature a distinctive gate structure characterized by the integration of three materials with varying work functions. Within this innovative design, three distinct regions, namely Region 1, Region 2, and Region 3, are defined, each possessing unique lengths denoted as L1, L2, and L3. Furthermore, it is worth noting that the channel within these transistors is intentionally subjected to light doping to enhance their performance characteristics.

Central to the architecture of these STMG CSDG MOSFETs is incorporating two key oxide materials: Silicon dioxide and a high-K dielectric. This composite structure is vividly illustrated in Figure 6.1, highlighting these materials' pivotal role in the device's overall functionality and performance. Utilizing this multi-material gate configuration, in conjunction with the carefully tailored channel doping, promises to yield substantial improvements in the device performance, enabling a wide range of applications in modern electronic systems.

## 6.3 Device Model

The proposed novel STMG CSDG MOSFET contains triple metal gate electrode that are stacked together in the inner and external gate as shown in Figure 6.3. These gate electrodes have different work functions named $\Phi_{M1}$, $\Phi_{M2}$, and $\Phi_{M3}$ in such a way that the $\Phi_{M1}$ of the first gate electrode is greater than the $\Phi_{M2}$ of the second gate electrode and the $\Phi_{M2}$ of the second electrode is greater than $\Phi_{M3}$ of the third gate electrode.

In the proposed novel structure, the metal gate with the highest work function (i.e., $\Phi_{M1}$) is placed at the source end of the device structure considering the first gate Length L1 nm. This L1 nm metal gate is called the Control Gate. The gate electrode with intermediate work function (i.e., $\Phi_{M2}$), L2 nm, is placed as the second gate electrode, which is known as the First Screen Gate. And finally, the gate electrode with the lowest work function (i.e., $\Phi_{M3}$) is called the Second Screen Gate. This gate load with the lowest work function is placed at the drain end of the novel device structure. So, the total gate length is L= L1+L2+L3, and the work function is represented in ascending order as $\Phi_{M1} > \Phi_{M2} > \Phi_{M3}$, respectively. This method employed is known as gate-material engineering. This method will analytically develop a three-step surface potential to suppress SCEs.

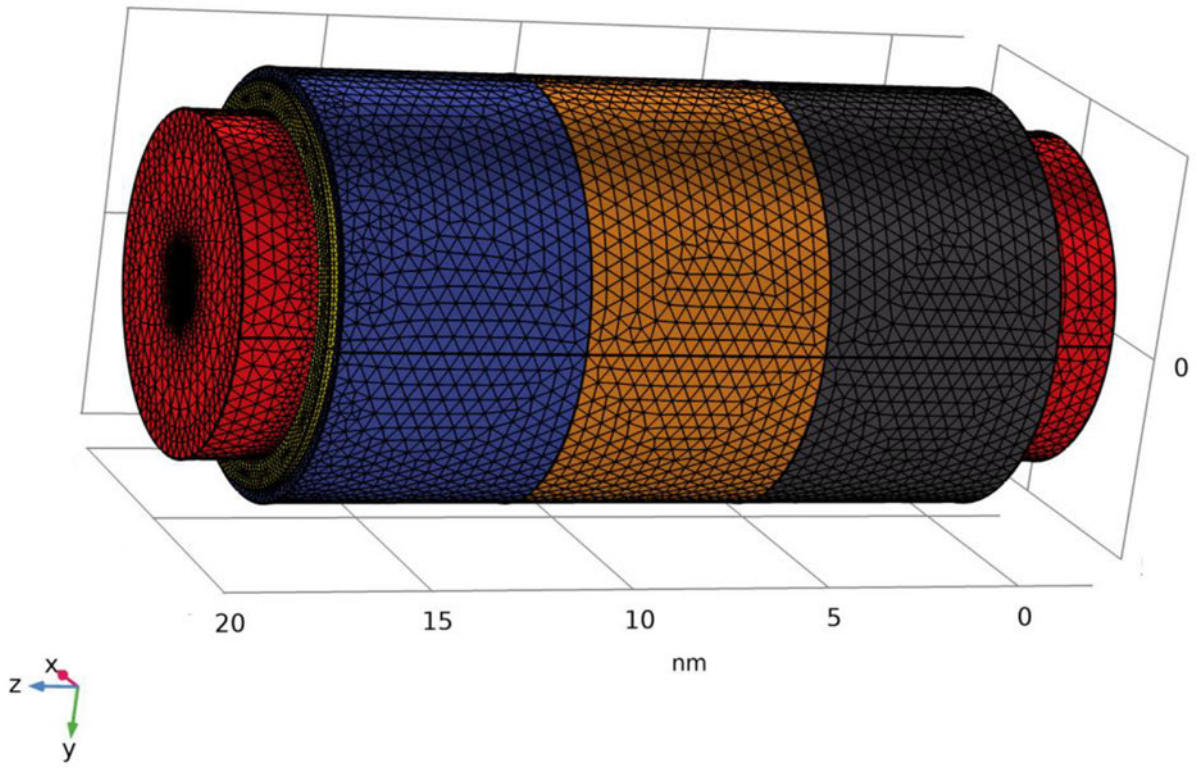


FIGURE 6.3: Simulated Mesh Analysis of TMGS CSDG MOSFET.

Also, A hetero-dielectric stacked gate oxide is implemented in the proposed device. The method involves a combination of high-k oxide (t1) and low-k oxide (t2) at the Silicon interface to separate the gate electrodes and the channel. This method is called gate-oxide engineering. The method was implemented to reduce electron scattering. The operational principle of the novel STMG MOSFET follows device physics. And the behaviour of the proposed device is analyzed under volume conduction mode. It assumed that the device operates under a subthreshold region for less complicated analyses, and the channel is fully depleted.

## 6.4 Numerical Modelling Framework.

The numerical simulator of the discrete 3D finite-element mesh structure iteratively solves the 2-D Poisson equation of the STMG CSDG MOSFET. Since STMG CSDG MOSFET is a very small device, quantum treatment was employed in the model. The finite mesh structure allows an accurate description of the complex structure with respect to the boundary conditions.

At each time step, the self-consistent solution of the Poisson equation is computed in a 3D mesh. And the potential is obtained from every node in the mesh structure. A quantum

correction method based on the solution to the Schrödinger equation is incorporated into the model. This method assumes the longitudinal and transverse electron effective masses in a Silicon with little conduction [148]. It explains the penetration of the wave function into the surrounding dielectric layer. Using distribution dependence on the gradient of electron density, the Schrödinger equation is solved on 2-D slices across the device structure using distribution dependence on the gradient of electron density. With Schrödinger's eigen-states, a 2-D quantum-mechanical electron density is obtained, which contains the Boltzmann statistics.

The 2-D quantum-mechanical electron density can be interpolated to the 3D structure to obtain the quantum correction potential. An error is calculated for each iteration, and the device simulator attempts to converge on a solution with an acceptable small error. Once the surface potential is obtained, the TMGS CSDG MOSFET's threshold voltage can be modelled, as shown in the flow chart in Figure 6.4.

## 6.5 Boundary Condition of STMG CSDG MOSFET.

This section delves into a crucial aspect of the STMG CSDG MOSFET, specifically focusing on the boundary condition employed during the analytical derivation process. This boundary condition serves as a fundamental cornerstone for obtaining a comprehensive, closed-form expression for this innovative transistor's internal and external surface potentials.

To elucidate further, understanding the boundary condition becomes essential in deriving precise and insightful expressions for the surface potentials, which play a pivotal role in characterizing the device's electrical behavior and performance. Utilizing this boundary condition enables us to unravel the intricate electrostatic interactions at the transistor's surface, shedding light on how its various regions and materials influence potential distribution.

By explicating this boundary condition and its role in the analytical derivation process, we gain valuable insights into the underlying physics of the STMG CSDG MOSFET. Unlike the Cylindrical Surrounding Gate (CSG) MOSFET, the electric field of STMG CSDG MOSFET is not zero from the Silicon pile's center (at r=0) since there is no Silicon in the center of the device structure. The center of the Silicon pile in the device structure is the Gaussian surface at $r = t_{si}/2$, where the electric field equals zero. The inner interface between the gate and the Silicon is denoted as "a" while the outer interface is denoted as "b" as shown in Figure 6.5. Also, the Silicon thickness is determined by subtracting the external interface from the internal interface as $(b - a = tsi)$.

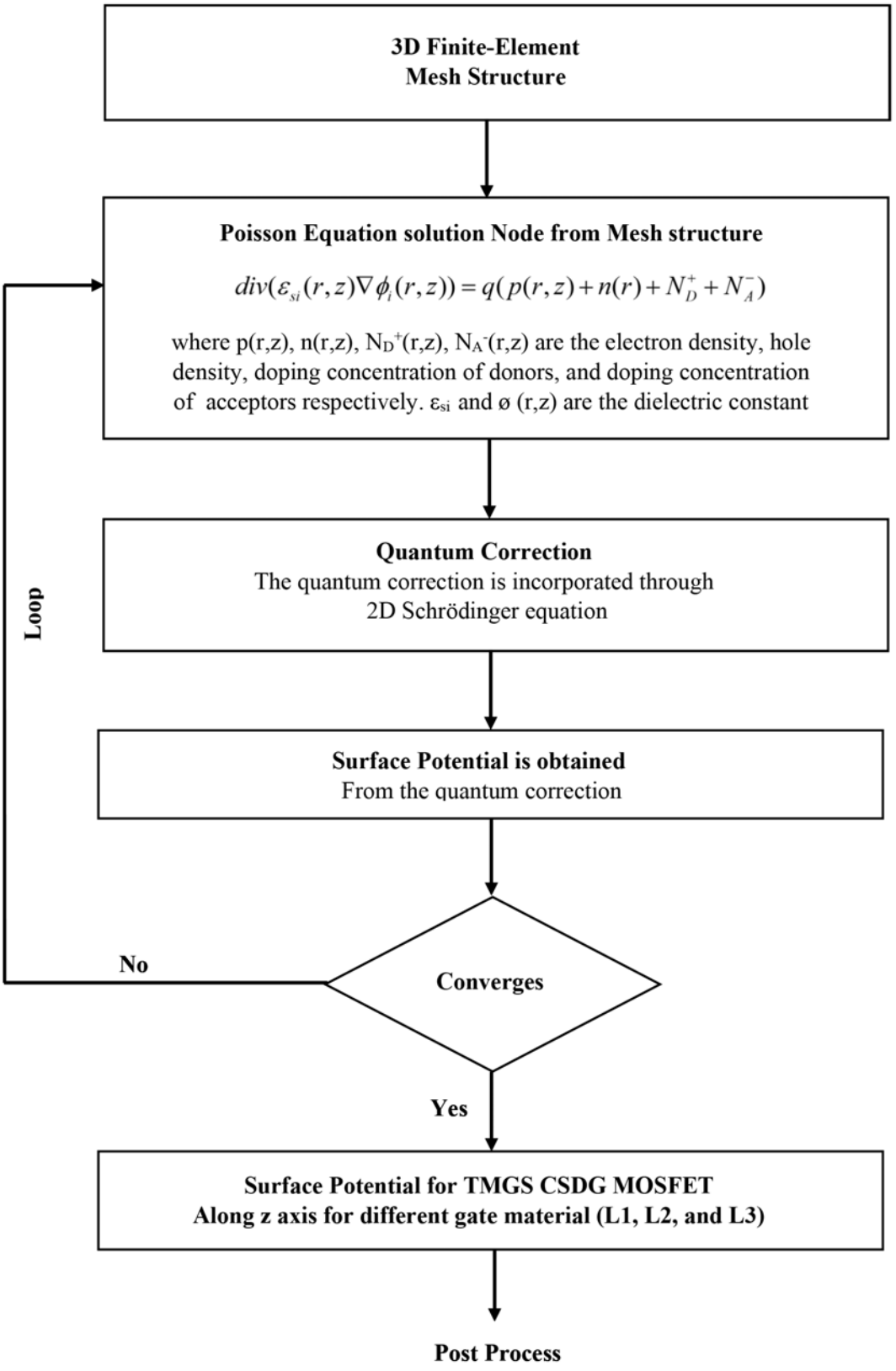


FIGURE 6.4: Simulation Framework of the Mesh structure.

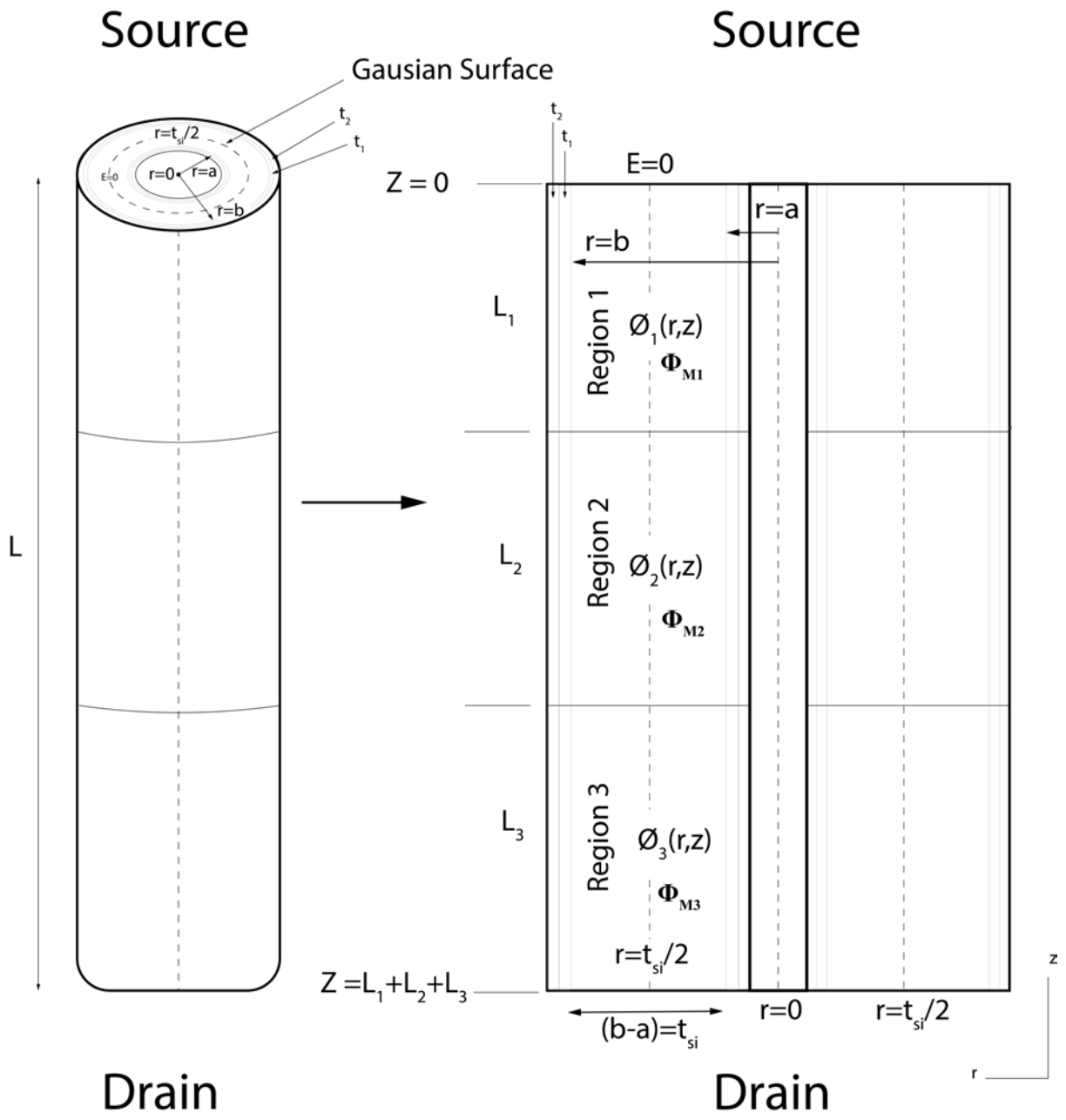


FIGURE 6.5: Boundary Condition Representation of TMG CSDG MOSFET.

## 6.6 Surface Potential Analytical Model derivation for TMGS CSDG MOSFET

To model the potential distribution of STMG CSDG MOSFET, it must be noted that the major difference between CSDG MOSFET and STMG CSDG MOSFET is the triple gate material used along the Z axis. Therefore, the surface potential distribution around the radial part (r axis) of STMG CSDG MOSFET has similar boundary conditions with CSDG MOSFET. As illustrated in Figure 6.5, the surrounding metals partition the whole channel area into three parts labelled Region 1, Region 2, and Region 3.

The surface potential distribution along the channel regions (As a consequence, the Poison equation with respect to the partition will be stated as follows:

$$\frac{d^2\psi_j(r,z)}{d^2z} + \frac{1}{r}\frac{d}{dr}\Big(r\frac{d}{dr}\psi_j(r,z)\Big) = \frac{qN_a}{\varepsilon_{si}} \tag{6.1}$$

where $j = 1, 2, 3.\psi_j(r, z)$ represent the surface potential distribution at a specific point along the channel, $Na$ represents the acceptor concentration along the channel, $Z$ represents the channel length direction, $r$ represents the direction perpendicular to the channel, $q$ represents the electronic charge, and $\epsilon_{si}$ represents the silicon permittivity.

In STMG CSDG MOSFET, the external and internal gates consist of three materials with metal work functions. Since the Flatband of STMG CSDG MOSFET depends on the work function, it is given as: For Internal gate and external Flatband voltage with respect to gate material

$$\begin{aligned} V_{FB,intj} &= \Phi_{msj} = \Phi_{mj} - \Phi_s \\ V_{FB,extj} &= \Phi_{msj} = \Phi_{mj} - \Phi_s \end{aligned} \tag{6.2}$$

where $j = 1, 2, 3$ for the three material regions within the internal and external gate, $\Phi_s$ is the silicon work function, represented as

$$\begin{aligned} \Phi_s &= \chi_s + \frac{E_s}{2q} + \Phi_f \\ \Phi_f &= V_T \ln\Big(\frac{N_a}{n_i}\Big) \end{aligned} \tag{6.3}$$

where $E_g$, $\chi$, and $\Phi_f$ are the silicon band gap, electron affinity of silicon, and Fermi potential, respectively. $n_i$ and $V_T$ are the intrinsic and carrier concentration and thermal voltage, respectively.

As with CSDG MOSFETs, the potential in all regions of the STM CSDG MOSFETs is described using the PPA model proposed by Young [42] as:

### 6.6.1 Potential Distribution Derivation

Potential Distribution due to the Internal Gate

$$\begin{aligned} \phi_j(r,z) = D_{0j}(Z) + D_{1j}(Z)r + D_{2j}(Z)r^2 \\ (a \le r)\ for\ j = 1, 2, 3 \end{aligned} \tag{6.4}$$

Potential Distribution due to the External Gate

$$\begin{aligned} \phi_i(r,z) = E_{0j}(Z) + E_{1j}(Z)r + E_{2j}(Z)r^2 \\ (b \geq r)\ for\ j = 1,2,3 \end{aligned} \tag{6.5}$$

Where $D_{0j}$, $D_{1j}$, $D_{2j}$, $E_{0j}$, $E_{1j}$, and $E2j$ are the arbitrary coefficients of approximation and are determined with the help of the structure's boundary conditions shown in Figure 6.5. The $j$ represents the number of regions within the TM CSDG structure.

We outline the essential boundary conditions that must be satisfied at the channel interface to determine the internal and external channel potentials accurately. Furthermore, it's vital to maintain the continuity of electric flux at the gate-oxide interface across different material regions for both the internal gate and the internal channel interface. The ensuing equations have been derived with meticulous consideration of these critical boundary conditions.

### 6.6.2 Potential Distribution due to Internal gate

At the gate oxide interface, the internal gate of the device structure under different materials is given as:

**1) The potential at the source end is**

$$\psi_j(r, z = 0) = V_{bi} \tag{6.6}$$

**2) The potential at the drain end**

$$\begin{aligned} \psi_j(r, z = L) = V_{bi} + V_{DS} \\ L = L_1 + L_2 + L_3 \end{aligned} \tag{6.7}$$

where are $V_{bi}$ and $V_{DS}$ are the built-in potential and drain to source voltage.

**3) Considering the boundary condition at the internal gate interface**

The potential distribution due to the internal gate under the three materials at the interface is given as

$$\begin{aligned} \psi_i(r = a, z)|_{a=a_{space}+t_1+t_1} = \psi_{aj}(z) \\ j = 1,2,3 \end{aligned} \tag{6.8}$$

**4) Also, the electric flux of the internal gate and the internal channel interface is continuous at the gate-oxide interface throughout the material regions**.

$$\left.\frac{d\psi_1(r,z)}{dr}\right|_{r=a} = \frac{C_{oxa-eff}(\psi_a(z) - V_{GF-L1})}{\epsilon_{si}} \; for\; 0 \le z \le L_1$$

$$\left.\frac{d\psi_2(r,z)}{dr}\right|_{r=a} = \frac{C_{oxa-eff}(\psi_a(z) - V_{GF-L2})}{\epsilon_{si}} \; for\; L_1 \le z \le L_1 + L_2 \tag{6.9}$$

$$\left.\frac{d\psi_3(r,z)}{dr}\right|_{r=a} = \frac{C_{oxa-eff}(\psi_a(z) - V_{GF-L3})}{\epsilon_{si}} \; for\; L_1 + L_2 \le z \le L_1 + L_2 + L_3$$

$$V_{GF-Lj} = V_{GS} - V_{FB,intj}$$

where $\psi_1(r,z)$,$\psi_2(r,z)$, and $\psi_3(r,z)$ are the potential distribution with respect to the three gate materials, $j = 1$, 2 and 3.

The oxide capacitance for the internal gate is obtained as follows:

$$C_{oxa-eff} = \frac{\epsilon_1}{(b - t_{si}) \ln\left(1 + \frac{t_{eff}}{b - t_{si}}\right)} \tag{6.10}$$

$$t_{eff} = t_1 + t_2 \frac{\epsilon_1}{\epsilon_2}$$

where $t1$, $t2$, $teff$ are the silicon dioxide layer, the high-K dielectric layer, and the effective thick of oxide

**5) At the Gaussian surface, the electric field is zero**

$$\left.\frac{d\psi_j(r,z)}{dr}\right|_{r=\frac{t_{si}}{2}} = 0 \tag{6.11}$$

**6) The electric potential and the electric field across the three regions are continuous at the internal interface of the materials**

$$\begin{aligned}
\psi_1(a, L_1) &= \psi_2(a, L_2) \\
\left(\frac{d\psi_1(a, L_1)}{dz}\right)\Big|_{z=L_1} &= \left(\frac{d\psi_2(a, L_2)}{dz}\right)\Big|_{z=L_2} \\
\psi_2(a, L_1 + L_2) &= \psi_3(a, L_1 + L_2) \\
\left(\frac{d\psi_2(a, L_1 + L_2)}{dz}\right)\Big|_{z=L_2} &= \left(\frac{d\psi_3(a, L_1 + L_2)}{dz}\right)\Big|_{z=L_3}
\end{aligned} \tag{6.12}$$

### 6.6.3 Potential Distribution due to External gate

Similarly, the potential distribution due to the external gate effects on the device structure is given as:

The potential distribution due to the external gate under the three different materials is given as

$$\begin{aligned}
\psi_j(r = a, z)|_{b=a+t_{si}} &= \psi_{bj}(z) \\
j &= 1, 2, 3
\end{aligned} \tag{6.13}$$

The electric flux of the external gate and the channel is continuous at the gate-oxide interface throughout the material regions.

$$\begin{aligned}
\frac{d\psi_1(r, z)}{dr}\Big|_{r=b} &= \frac{C_{oxb-eff}(V_{GF-L1} - \psi_b(z))}{\epsilon_{si}} \; for \; 0 \leq z \leq L_1 \\
\frac{d\psi_2(r, z)}{dr}\Big|_{r=b} &= \frac{C_{oxb-eff}(V_{GF-L2} - \psi_b(z))}{\epsilon_{si}} \; for \; L_1 \leq z \leq L_1 + L_2 \\
\frac{d\psi_3(r, z)}{dr}\Big|_{r=b} &= \frac{C_{oxb-eff}(V_{GF-L3} - \psi_b(z)-)}{\epsilon_{si}} \; for \; L_1 + L_2 \leq z \leq L_1 + L_2 + L_3 \\
V_{GF-Lj} &= V_{GS} - V_{FB,extj}
\end{aligned} \tag{6.14}$$

Also, the oxide capacitance due to the external gate is given as

$$C_{oxa-eff} = \frac{\epsilon_1}{(a+t_{si})\ln\left(1+\frac{t_{eff}}{a+t_{si}}\right)}$$
$$t_{eff} = t_1 + t_2\frac{\epsilon_1}{\epsilon_2} \tag{6.15}$$

where $t1$, $t2$, $teff$ are the silicon dioxide layer, the high-K dielectric layer, and the effective thick of oxide.

Similar to the internal gate, at the Gaussian surface, the electric field with respect to the external gate is zero. Additionally, at the materials interface, with regard to the external gate, the electric potential and the electric field are continuous throughout the three regions as

$$\psi_1(b, L_1) = \psi_2(b, L_2)$$
$$\left(\frac{d\psi_1(b, L_1)}{dz}\right)\Big|_{z=L_1} = \left(\frac{d\psi_2(b, L_2)}{dz}\right)\Big|_{z=L_2} \tag{6.16}$$
$$\psi_2(b, L_1+L_2) = \psi_3(b, L_1+L_2)$$
$$\left(\frac{d\psi_2(b, L_1+L_2)}{dz}\right)\Big|_{z=L_2} = \left(\frac{d\psi_3(b, L_1+L_2)}{dz}\right)\Big|_{z=L_3}$$

The arbitrary coefficients of the three regions (Region 1, Region 2, and Region 3) are derived by applying the boundary condition at the Gaussian surface where the electric field is equal to zero (i.e., Equation (6.11)) to Equation (6.9) and Equation (6.14), where $j = 1, 2, 3$ represents the three regions.

The arbitrary coefficients of the three regions (Region 1, Region 2, and Region 3) for the internal and external gates are derived by applying the boundary conditions derived from Equation (6.6) to Equation (6.11) and Equation (6.13) to Equation (6.15) into Equation (6.4) and Equation (6.5), respectively.

$$D_{1j} = E_{1j} = \frac{b[C_{oxa-eff}(\psi_b(z) - V_{GF-Lj})]}{\epsilon_{si}[(b-a)]} + \frac{b[C_{oxb-eff}(\psi_b(z) - V_{GF-Lj})]}{\epsilon_{si}[(b-a)]} \tag{6.17}$$

$$D_{2j} = E_{2j} = \frac{[C_{oxa-eff}(V_{GF-Lj}) - \psi_b(z)]}{\epsilon_{si}[2(b-a)]} + \frac{[C_{oxb-eff}(V_{GF-Lj} - \psi_b(z))]}{\epsilon_{si}[2(b-a)]} \tag{6.18}$$

$$\begin{aligned} D_{0j} = \psi_a(z)\left[1 - \frac{[a(2b-a)C_{oxa-eff}]}{2\epsilon_{si}[(b-a)]}\right] - \psi_b(z)\left[\frac{[a^2 C_{oxb-eff}]}{2\epsilon_{si}[(b-a)]}\right] \\ + V_{GF-Lj}\left[\frac{[a(2b-a)C_{oxa-eff} - a^2 C_{oxb-eff}]}{2\epsilon_{si}[(b-a)]}\right] \end{aligned} \tag{6.19}$$

$$\begin{aligned} E_{0j} = \psi_b(z)\left[1 - \frac{[b^2 C_{oxa-eff}]}{2\epsilon_{si}[(b-a)]}\right] - \psi_a(z)\left[\frac{[b^2 C_{oxb-eff}]}{2\epsilon_{si}[(b-a)]}\right] \\ + V_{GF-Lj}\left[\frac{[b^2(C_{oxa-eff} - C_{oxb-eff})]}{2\epsilon_{si}[(b-a)]}\right] \end{aligned} \tag{6.20}$$

Based on Equation (6.19) and Equation (6.20), and the boundary condition in Equation (6.13) and Equation (6.16) respectively, the relationship between the internal and external potential is given:

$$\psi_a(z) = \zeta_1 \psi_b(z) + \kappa_1 V_{GF-Lj} \tag{6.21}$$

$$\psi_b(z) = \zeta_2 \psi_a(z) + \kappa_2 V_{GF-Lj} \tag{6.22}$$

where the coefficients are given as follows:

$$\begin{aligned} \zeta_1 &= \left[\frac{2\epsilon_{si}t_{si} - [(a+t_{si})(a+t_{si})C_{oxb-eff}]}{(a+t_{si})^2 C_{oxa-eff}}\right] \\ \zeta_2 &= \left[\frac{2\epsilon_{si}t_{si} - [(b+t_{si})(b-t_{si})C_{oxa-eff}]}{(b-t_{si})^2 C_{oxb-eff}}\right] \\ \kappa_1 &= \left[\frac{[C_{oxb-eff} - C_{oxa-eff}]}{C_{oxa-eff}}\right] \\ \kappa_2 &= \left[\frac{[(b+t_{si})C_{oxa-eff} - (b-t_{si})C_{oxb-eff}]}{(b-t_{si})C_{oxb-eff}}\right] \end{aligned} \tag{6.23}$$

Since the surface potential and electric field at the interface of any two dissimilar metals are continuous, as shown in Equation (6.13) and Equation (6.16).Substituting the arbitrary coefficients (Equation (6.17) to Equation (6.22) into Equation (6.4) and Equation (6.5) respectively, the internal and external surface potential of TMGS CSDG MOSFET is mathematically derived as given:

**Internal Surface Potential of TMGS CSDG MOSFET**

$$\psi_j(r=a,z)=\psi_a(z)\left[\beta_{int}+\mathcal{J}_{int}a-\gamma_{int}a^2\right]+V_{GF-Lj}\left[\mathcal{R}_{int}+\mathcal{N}_{int}a-\delta_{int}a^2\right] \quad (6.24)$$

where the parameters are defined as follows:

$$\begin{aligned}
\beta_{int} &= \left[\frac{(b-t_{si})(b+t_{si})C_{oxa-eff}}{2\epsilon_{si}t_{si}}\right]+\left[\frac{2\epsilon_{si}t_{si}+(b-t_{si})(b+t_{si})C_{oxb-eff}}{2\epsilon_{si}t_{si}}\right]\\
\mathcal{J}_{int} &= \left[\frac{(a+t_{si})\epsilon_{si}t_{si}}{(b-t_{si})^2\epsilon_{si}t_{si}}+\frac{(b+t_{si})(b-t_{si})C_{oxb-eff}}{(b-t_{si})^2\epsilon_{si}t_{si}}\right]\\
\gamma_{int} &= \left[\frac{(b-t_{si})^2C_{oxa-eff}}{2(b-t_{si})^2\epsilon_{si}t_{si}}\right]+\left[\frac{2\epsilon_{si}t_{si}+(b-t_{si})(b+t_{si})C_{oxb-eff}}{2(b-t_{si})^2\epsilon_{si}t_{si}}\right]\\
\mathcal{R}_{int} &= \left[\frac{(b-t_{si})(b+t_{si})C_{oxa-eff}}{4\epsilon_{si}t_{si}}\right]+\left[\frac{(b-t_{si})^2C_{oxb-eff}}{4\epsilon_{si}t_{si}}\right]\\
\mathcal{N}_{int} &= \left[\frac{(b-t_{si})(b+t_{si})C_{oxa-eff}-(b-t_{si}C_{oxb-eff})}{(b-t_{si})\epsilon_{si}t_{si}}\right]+\left[\frac{(a+t_{si})C_{oxb-eff}}{(b-t_{si})\epsilon_{si}t_{si}}\right]\\
\delta_{int} &= \left[\frac{(b-t_{si})^2C_{oxa-eff}+(b+t_{si}C_{oxa-eff})}{2(b-t_{si})^2\epsilon_{si}t_{si}}\right]+\left[\frac{(b-t_{si})^2C_{oxb-eff}-(b-t_{si})C_{oxb-eff}}{2(b-t_{si})^2\epsilon_{si}t_{si}}\right]
\end{aligned} \quad (6.25)$$

**External Surface Potential STMG CSDG MOSFET**

$$\psi_i(r=b,z)=\psi_b(z)\left[\beta_{ext}+\mathcal{J}_{ext}b-\gamma_{ext}b^2\right]+V_{GF-Lj}\left[\mathcal{R}_{ext}+\mathcal{N}_{ext}b-\delta_{ext}b^2\right] \quad (6.26)$$

where the parameters are defined as follows:

$$\begin{aligned}
\beta_{ext} &= \left[\frac{(a+t_{si})^2 C_{oxb-eff}}{2\epsilon_{si}t_{si}}\right] + \left[\frac{2\epsilon_{si}t_{si} + (a+t_{si})^2 C_{oxb-eff}}{2\epsilon_{si}t_{si}}\right] \\
\mathcal{J}_{ext} &= \left[\frac{2\epsilon_{si}t_{si}}{(a+t_{si})\epsilon_{si}t_{si}} + \frac{(a+t_{si})^2 C_{oxb-eff}}{(a+t_{si})\epsilon_{si}t_{si}}\right] \\
\gamma_{ext} &= \left[\frac{(a+t_{si})^2 C_{oxb-eff}}{2(a+t_{si})^2\epsilon_{si}t_{si}}\right] + \left[\frac{2\epsilon_{si}t_{si} - (a+t_{si})^2 C_{oxb-eff}}{2(a+t_{si})^2\epsilon_{si}t_{si}}\right] \\
\mathcal{R}_{ext} &= \left[\frac{(a+t_{si})^2 C_{oxb-eff}}{4\epsilon_{si}t_{si}}\right] + \left[\frac{(a+t_{si})^2 C_{oxa-eff}}{4\epsilon_{si}t_{si}}\right] \\
\mathcal{N}_{ext} &= \left[\frac{(a+t_{si})C_{oxb-eff} - (a+t_{si}C_{oxa-eff})}{\epsilon_{si}t_{si}}\right] + \left[\frac{(a+t_{si})C_{oxa-eff}}{\epsilon_{si}t_{si}}\right] \\
\delta_{ext} &= \left[\frac{C_{oxa-eff}}{(2\epsilon_{si}t_{si}}\right] + \left[\frac{C_{oxb-eff}}{2\epsilon_{si}t_{si}}\right]
\end{aligned} \tag{6.27}$$

By incorporating Equation (6.24) and Equation (6.26) into Equation (6.1), it is possible to derive second-order differential equations with constant coefficients, as given.

$$\frac{d^2\psi_j(z)}{d^2z} - \lambda_a^2\psi_j(z) = \sigma_a \tag{6.28}$$

The coefficient relations are expressed as given:

$$\lambda_a^2 = \left[\frac{\mathcal{H}_{\dashv}}{\sigma_a}\right] \tag{6.29}$$

where the coefficients are given as follows:

$$\begin{aligned}
\mathcal{H}_{\dashv} &= \left[\frac{\mathcal{N}_{int})}{a} - 4\delta_{int}\right] \\
\sigma_a &= \left[\frac{qN_a}{\epsilon_{si}} - \frac{\mathcal{X}_a}{\lambda_a^2}V_{GF-Lj}\right] \\
\mathcal{X}_a &= \left[1 - \beta_{int} + (J)_{int}a - \gamma_{int}a^2\right]
\end{aligned} \tag{6.30}$$

where $\lambda_a$ is the newly derived natural length for TMGS CSDG MOSFET with respect to the internal gate. Similarly, the natural length due to the external gate can be obtained as:

$$\lambda_b^2 = \left[\frac{\mathcal{H}_{\lfloor}}{\sigma_b}\right] \tag{6.31}$$

where the coefficients are given as follows:

$$\begin{aligned} \mathcal{H}_{\lfloor} &= \left[\frac{\mathcal{N}_{ext}}{b} - 4\delta_{ext}\right] \\ \sigma_b &= \left[\frac{qN_a}{\epsilon_{si}} - \frac{\mathcal{X}_b}{\lambda_b^2} V_{GF-Lj}\right] \\ \mathcal{X}_b &= \left[1 - \beta_{ext} + (J)_{ext} a - \gamma_{ext} a^2\right] \end{aligned} \tag{6.32}$$

Having obtained the natural length, the general solution to the Second-order differential in Equation (6.29), the solution to Poisson's equations, is expressed in a close formulation with respect to the three regions under the L1, L2, and L3.

**Region 1**

$$\psi_{a1}(z) = \left[M_1 e^{\lambda_a z} + N_1 e^{\lambda_a z} - \frac{\sigma_a}{\lambda_a^2}\right] \; for \; 0 \leq z \leq L_1 \tag{6.33}$$

**Region 2**

$$\psi_{a2}(z) = \left[M_2 e^{\lambda_a (z - L_1)} + N_2 e^{\lambda_a (z - L_1)} - \frac{\sigma_a}{\lambda_a^2}\right] \; for \; L_1 \leq z \leq L_1 + L_2 \tag{6.34}$$

**Region 3**

$$\psi_{a2}(z) = \left[M_3 e^{\lambda_a (z - (L_1 + L_2))} + N_3 e^{\lambda_a (z - (L_1 + L_2))} - \frac{\sigma_a}{\lambda_a^2}\right] \; for \; L_1 + L_2 \leq z \leq L_1 + L_2 + L_3 \tag{6.35}$$

where the variables $M1$, $M2$, $M3$, $N1$, $N2$, and $N3$ are derived using the boundary conditions that describe the potential at the source end and drain end (Equation (6.6) and Equation (6.7)) and the boundary condition that describes the continuity of the electric potential along the three regions (Equation (6.12). These mathematical derivations are found in the appendix.

Similarly, for the external gate, the solution to the Poisson's equation can be expressed under the three regions:

**Region 1**

$$\psi_{b1}(z) = \left[M_4 e^{\lambda_b z} + N_4 e^{\lambda_b z} - \frac{\sigma_b}{\lambda_b^2}\right] \; for \; 0 \leq z \leq L_1 \tag{6.36}$$

**Region 2**

$$\psi_{b2}(z) = \left[ M_5 e^{\lambda_b (z - L_1)} + N_5 e^{\lambda_b (z - L_1)} - \frac{\sigma_b}{\lambda_b^2} \right] \; for \; L_1 \leq z \leq L_1 + L_2 \tag{6.37}$$

**Region 3**

$$\psi_{b2}(z) = \left[ M_6 e^{\lambda_b (z - (L_1 + L_2))} + N_6 e^{\lambda_b (z - (L_1 + L_2))} - \frac{\sigma_b}{\lambda_b^2} \right] \; for \; L_1 + L_2 \leq z \leq L_1 + L_2 + L_3 \tag{6.38}$$

where the variables $M4$, $M5$, $M6$, $N4$, $N5$, and $N6$ are derived using the boundary conditions that describe the potential at the source end and drain end (Equation (6.6) and Equation (6.7)) and the boundary condition that describes the continuity of the electric potential along the three regions (Equation (6.16). These mathematical derivations are found in the appendix.

## 6.7 Electric Field Derivation for STMG CSDG MOSFET

The electron transport velocity across the channel is proportional to the channel's electric pattern. So, by differentiating the surface potential with respect to either the internal or the external gate, the electric-field distribution along the channel length may be calculated as given.

**Internal Gate**

$$E_{int1}(z) = \frac{\psi_{a1}(z)}{dr} = \left[ \lambda_a M_1 e^{\lambda_a z} - \lambda_a N_1 e^{-\lambda_a z} \right] \; for \; 0 \leq z \leq L_1 \tag{6.39}$$

$$E_{int2}(z) = \frac{\psi_{a2}(z)}{dr} = \left[ \lambda_a M_2 e^{\lambda_a (z - L_1)} - \lambda_a N_2 e^{-\lambda_a (z - L_1)} \right] \; for \; L_1 \leq z \leq L_1 + L_2 \tag{6.40}$$

$$E_{int3}(z) = \frac{\psi_{a3}(z)}{dr} = \left[ \lambda_a M_3 e^{\lambda_a (z - (L_1 + L_2))} + \lambda_a N_3 e^{-\lambda_a (z - (L_1 + L_2))} - \frac{\sigma_a}{\lambda_a^2} \right] \quad L_1 + L_2 \leq z \leq L_1 + L_2 + L_3 \tag{6.41}$$

**External Gate**

$$E_{ext1}(z) = \frac{\psi_{b1}(z)}{dr} = \left[ \lambda_b M_4 e^{\lambda_b z} - \lambda_b N_4 e^{-\lambda_b z} \right] \; for \; 0 \leq z \leq L_1 \tag{6.42}$$

$$E_{ext2}(z) = \frac{\psi_{b2}(z)}{dr} = \left[\lambda_b M_5 e^{\lambda_b(z-L_1)} - \lambda_b N_5 e^{-\lambda_b(z-L_1)}\right] \; for \; L_1 \leq z \leq L_1 + L_2 \quad (6.43)$$

$$E_{ext3}(z) = \frac{\psi_{b3}(z)}{dr} = \left[\lambda_b M_6 e^{\lambda_b(z-(L_1+L_2))} + \lambda_b N_6 e^{-\lambda_b(z-(L_1+L_2))} - \frac{\sigma_b}{\lambda_b^2}\right] \quad (6.44)$$
$$for \; L_1 + L_2 \leq z \leq L_1 + L_2 + L_3$$

The derived electric field distribution equations are used to determine how the proposed TMGS CSDG MOSFET structure modifies the drain-side electric field effect under Region 1. This is implemented in the next section

## 6.8 Minimum Surface Potential and Threshold Voltage Model for STMG CSDG MOSFET

In order to evaluate SCEs parameters like subthreshold swing, subthreshold current, and threshold voltage roll-off, the minimum surface potential and its location are crucial. Due to the coexistence of three metal gates with different work functions in the TMSG CSDG MOSFET structure, the metal gate with the higher work function alone determines the minimum surface potential. Therefore, it is possible to calculate the silicon pillar's minimum surface potential beneath the gate by differentiating the surface potential in the region 1 (M1) of the internal gate and external gate and equating the resulting expression to zero as shown:

$$\left.\frac{\psi_{a1}(z)}{dz}\right|_{z=z_{min}} = 0, \left.\frac{\psi_{b1}(z)}{dz}\right|_{z=z_{min}} = 0 \quad (6.45)$$

By using Equation (6.45) and Equation (6.39), we obtained the minimum surface potential with respect to the internal gate as given:

$$Z_{min} = 2\frac{1}{2\lambda_a} ln\left(\frac{N_1}{M_1}\right) = 0$$
$$\psi_{a1(min)}(Z_{min}) = 2\sqrt{N_1 M_1} + \Lambda_a \quad (6.46)$$
$$\Lambda_a = \left(\frac{-\sigma_b}{\lambda_b}\right)$$

Similarly, the surface potential with respect to the external gate is :

$$\begin{aligned} Z_{min} &= 2\frac{1}{2\lambda_b} ln\left(\frac{N_1}{M_1}\right) = 0 \\ \psi_{b1(min)}(Z_{min}) &= 2\sqrt{N_1 M_1} + \Lambda_a \\ \Lambda_a &= \left(\frac{-\sigma_b}{\lambda_b}\right) \end{aligned} \tag{6.47}$$

The threshold voltage of TMGS CSDG MOSFET is defined as the gate voltage in Region 1 at which the minimum surface is twice the bulk potential.

$$\psi_{a1(min)}(Z_{min}) = 2\phi_F \tag{6.48}$$

where $\phi_F$ represents the distinction between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level.

So, by substituting the gate voltage with the threshold voltage and solving for the threshold voltage, the derived closed-form expression can be expressed as

$$\psi_{a1(min)}(Z_{min}) = \left(\frac{V_1 \pm \sqrt{V_1^2 - 4V_2V_3}}{2V_2}\right) = V_{tha1} \tag{6.49}$$

where the coefficients $V_1, V_2$, and $V_3$ are given in the Appendix.

## 6.9 Subthreshold Drain Current Derivation for STMG CSDG MOSFET

Through the diffusion process, subthreshold drain current travels from source to drain throughout the channel length [149]. The subthreshold drain current may be evaluated using the 3D channel potential model, where the effective channel potential mostly controls the subthreshold current. The very short-channel STMG CSDG MOSFET's subthreshold drain current has been calculated using the Pao-double Sah's integral [150–152], and is denoted by

$$I_{DS_{sub}} = \frac{\mu W V_T \left(1 - e^{\frac{V_{DS}}{V_T}}\right)}{\left(\int_0^{L_1} Q_1^{-1} dz\right) + \left(\int_{L_1}^{L_1+L_2} Q_2^{-1} dz\right) + \left(\int_{L_1}^{L_1+L_2+L_3} Q_3^{-1} dz\right)} \tag{6.50}$$

where $\mu$, $V_T = KT/q$, and $W = 2\pi(b-a)$ are the free carrier mobility, thermal voltage, and wide of the TMGS CSDG MOSFET structure, respectively. $Q_i(j = 1, 2, 3)$is the charge density, and $V_{DS}$ is the drain voltage.$K$, $T$, and $q$ are Boltzmann's constant, absolute temperature (in kelvin), and electric charge, respectively.

Since the subthreshold leakage only occurs in the minimum potential, the depletion charge is defined as given [153, 154]

$$\begin{aligned} Q_i &= \frac{qn^2}{N_a}\int_a^b \left(e^{\frac{q\psi_{ieff(min)}}{KT}}\right) dr \ for \ i = 1, 2, 3 \\ \psi_{i_eff(min)(Z_{min})} &= \frac{\psi_{ai(min)(Z_{min})} + \psi_{bi(min)(Z_{min})}}{2} \end{aligned} \tag{6.51}$$

where n is the intrinsic carrier density, and $\psi_{ai(min)(Z_{min})}$is the minimum effective channel potential of TMGS CSDG MOSFET.

This minimum effective potential, known as the virtual cathode potential, lies close to the center region of the device channel [155]. Solving Equation (6.50), and applying numerical integration of trapezoidal rule [156, 157] to Equation (6.51), the close form expression for subthreshold drain current is obtained as

$$I_{DS_{sub}} = \frac{\mu W V_T \left(1 - e^{\frac{V_{DS}}{V_T}}\right)}{\left(\frac{N_a L_1}{e^{\frac{q\psi_{1eff(min)(Z_{min})}}{KT}}}\right) + \left(\frac{N_a L_2}{e^{\frac{q\psi_{1eff(min)(Z_{min})}}{KT}}}\right) + \left(\frac{N_a L_3}{e^{\frac{q\psi_{1eff(min)(Z_{min})}}{KT}}}\right)} \tag{6.52}$$

Similar to threshold voltage analysis, the Subthreshold Current is limited by the minimum surface potential within Region 1 (M1) since other minimum potentials at Region 2 (M2) and Region 3 (M3) are larger than it [158]. Therefore, Equation (6.52) can be reduced to

$$I_{DS_{sub}} = \frac{\mu W V_T \left(1 - e^{\frac{V_{DS}}{V_T}}\right)}{\left(\frac{N_a L_1}{e^{\frac{q\psi_{1eff(min)(Z_{min})}}{KT}}}\right)} \tag{6.53}$$

Further simplification of Equation (6.53) renders the subthreshold drain current in the simplest form, as given.

$$I_{DS_{sub}} = \frac{2\pi\mu q n^2 (b-a) V_T \left(1 - e^{\frac{V_{DS}}{KT}}\right)\left(e^{\frac{q\psi_{1eff(min)(Z_{min})}}{KT}}\right)}{\left(N_a L_1\right)} \tag{6.54}$$

The obtained subthreshold drain current is used in the derivation of the subthreshold swing, [159] as given.

$$S_S = \frac{kT}{q} \ln 10 \left[\frac{\psi_{ieff(min)(Z_{min})}}{dV_{GS}}\right] = \frac{1}{\left(\frac{d}{dV_{gs}} \log(I_{DS_{sub}})\right)} \tag{6.55}$$

The subthreshold swing serves as a performance metric illustrating the relationship between the minimum on the gate-source bias voltage. This is further simplified to depict its variation concerning the subthreshold drain current.

## 6.10 Results and Discussion

The 2D analytical model was verified with numerical simulations done at room temperature (300k). The parameters used for simulation are given in Table 6.1.

To verify the 2D model of the short-channel devices, Figure 6.6 shows the variation of the surface potential with the normalized channel position for different gate materials with the ratios of $\Phi_{M1}, \Phi_{M2}, \Phi_{M3}$ as given in Table 6.2.

Good agreement between the results of our model and those of device simulator is obtained. The plot indicates that the minimum surface potential barrier between the source side and the minimum channel position can be increased for the high ratio of $\Phi_{M1}, \Phi_{M2}, \Phi_{M3}$ in $L_1 : L_2 : L_3$, which therefore enhances the immunity to the SCEs and effectively represses the DIBL for the devices.

Also, Figure 6.6 depicts a surface potential comparison of the SSMG CSDG MOSFET, SDMG CSDG, and STMG CSDG MOSFETs. The Surface potential profile of the SSMG CSDG MOSFET is noticeably steeper. In contrast, there is a step rise in the surface potential profile in SDMG CSDG MOSFET, which provides superior immunity to SCEs than SSMG CSDG MOSFET.

The proposed STMG CSDG, on the other hand, has a two-step rise, as indicated in the surface potential profile. This is owing to the different work functions of the three distinct stacked gate materials. When compared to SSMG CSDG MOSFET and SDMG CSDG

TABLE 6.1: Parametric values Considered for STMG CSDG MOSFET

| Symbol | Parameters | SSMG CSDG MOSFET | SDMG CSDG MOSFET | STMG CSDG MOSFET |
|---|---|---|---|---|
| L | Channel Length | 20 nm | 20 nm | 20 nm |
| a | Internal Radius | 4 nm | 4 nm | 4 nm |
| b | External Radius | 14 nm | 14 nm | 14 nm |
| $N_a$ | Channel Doping | $10^{17}$ $cm^{-}3$ | $10^{17}$ $cm^{-}3$ | $10^{17}$ $cm^{-}3$ |
| $t_{eff}$ | Oxide Thickness | 2 nm | 2 nm | 2 nm |
| $\Phi_{M_1,M_2,M_3}$ | Gate Work-Function | 4.8 eV | 4.8 eV, 4.6 eV | 4.8,4.6 eV,4.4 eV |

TABLE 6.2: Work Function used for modeling and simulation of Gate-engineered CSDG MOSFET

| MOSFET Structure | $\Phi_{M_1}(eV)$ $Region1$ | $\Phi_{M_2}(eV)$ $Region2$ | $\Phi_{M_2}(eV)$ $Region3$ |
|---|---|---|---|
| Stacked Single Material Gate (SSMG) CSDG MOSFET | 4.8 eV | 4.8 eV | 4.8 eV |
| Stacked Double Material Gate (SDMG) CSDG MOSFET | 4.8 eV | 4.6 eV | 4.6 eV |
| Stacked Triple Material Gate (STMG) CSDG MOSFET | 4.8 eV | 4.6 eV | 4.4 eV |

MOSFET, this steady two-step rise in surface potential guarantees greater screening of the channel area under Region 1 ($M_1$) from drain voltage changes. The SSMG structure exhibits more bending of the surface potential profile at 20 $nm$ at a low drain bias ($VDS = 0.1V$), indicating that SSMG CSDG MOSFETs are more prone to SCEs as compared to SDMG CSDG MOSFET and STMG CSDG MOSFET.

However, the proposed STMG CSDG architecture provides the best immunity to SCEs. Figure 6.7 displays the surface potential variation along the channel length position for various channel length ratios. It is evident that when the gate length in Region 1

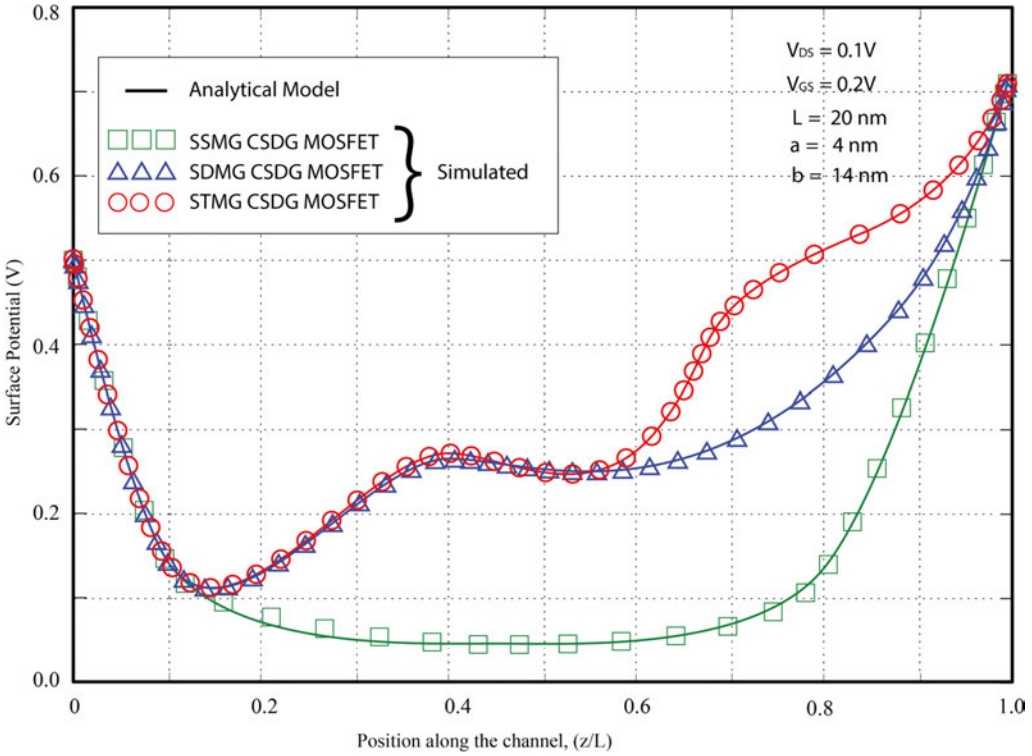


FIGURE 6.6: Surface potential variation with the normalized channel length position (Z/L) for the CSDG MOSFET, SDMG CSDG, and STMG CSDG MOSFETS with $V_{DS} = 0.1, V_{GS} = 0.2V, and\ L = 20nm$, $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

(L1) decreases, the minimum surface potential barrier between the source end and the minimum channel position lowers. And the drain impact on the channel is lessened by this alleged "Control Gate"(L1), which lowers DIBL and creates higher immunity to hot-carrier effects. Therefore, the threshold voltage of the STMG CSDG MSOFET device can be tuned by adjusting the ratio of the $L_1 : L_2 : L_3$ for digital and analog applications. Furthermore, as the lengths of the Screen-Gates (L2 and L3) increases, a drop in the peak electric field at the drain end occurs, which further increases the immunity to SCEs. Figure 6.7 shows that $L_1 : L_2 : L_3 = 1 : 2 : 3$ gives a better result. So, this configuration is used for STMG CSDG MOSFET analysis, except where stated.

The surface electric field variation versus normalized channel length position for CSDG, SDMG CSDG, and STMG CSDG MOSFET is shown in Figure 6.8. The two peaks in the electric field profile of STMG CSDG MOSFET results to a better transport efficiency compared to CSDG MOSFET and SDMG CSDG MOSFETs. The two peak causes rapid acceleration to the carriers in the channel, thus ensuring a higher transport

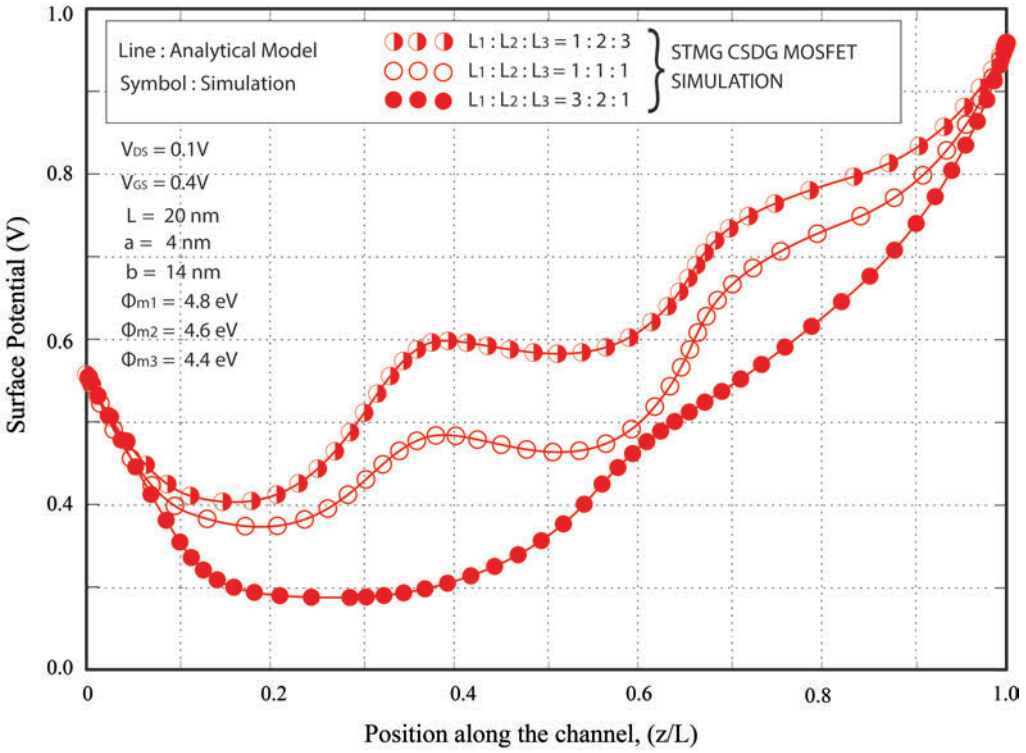


FIGURE 6.7: Surface potential variation versus normalized channel length position in STMG CSDG MOSFET for different gate material ratios: L1:L2: L3, at $V_{DS} = 0.1, and V_{GS} = 0.4V$, and $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

efficiency as more numbers of the carrier are supplied to the drain. Also, the low peak electric field at the drain end offers higher immunity to SCEs and ensures an increase in reliability. When the device is in the ON state, the electric field plays a significant role in the device performance, as more band bending is influenced by the field's distribution peak at tunneling junction. This helps to enhance the carrier's tunneling effect. The horizontal effect of the Electric field shown in Figure 6.9 shows a noticeable upsurge, which reduces gate control over the channel. The effect becomes more produced as the drain voltages increase. Figure 6.10 shows the effect of high drain voltage on the horizontal electric field. High drain voltage does not change the source field. However, it has a major impact on the drain field. This implies a shift in zero-field point towards the source. With the proposed STMG structure, such change in the potential under Region 1 (under M1) does not take effect even with a high value of drain voltage ($V_{DS}$). This makes the region under M1 be screened from the changes in the drain potential.

Hence, the region under M1 is called the control voltage, and the region under M2 and M3 is called the first and second screening gate. As a result of that, the peak electric field of STMG structure is low at the drain end. This reduction in the electric field of

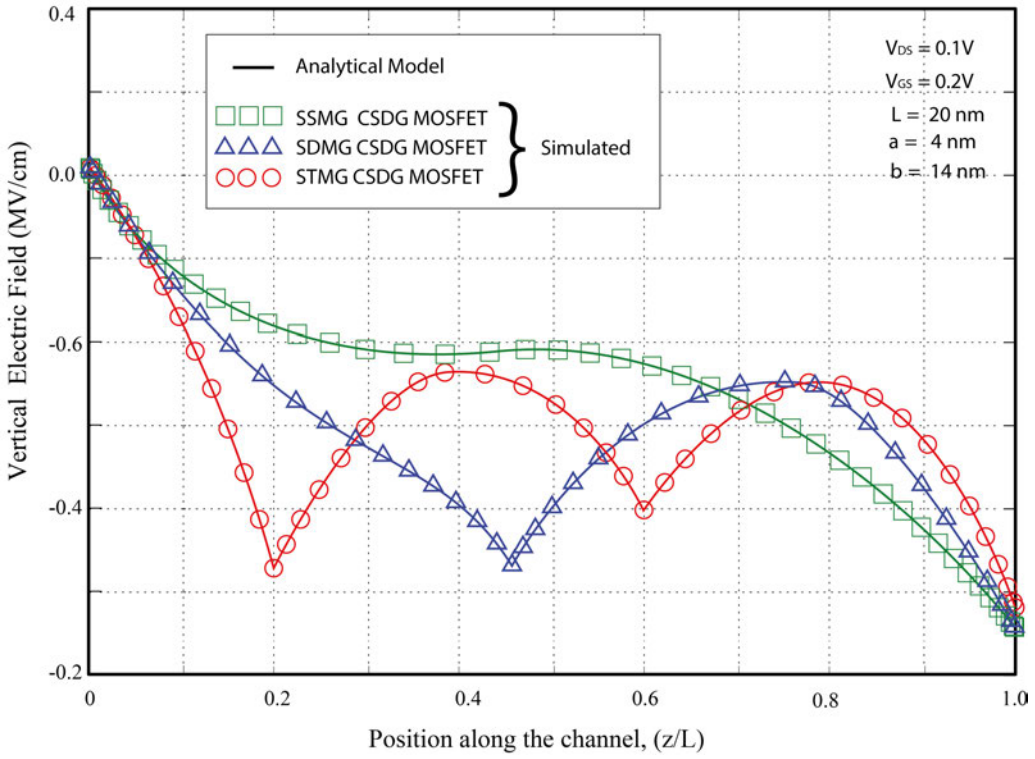


FIGURE 6.8: Vertical Electric field variation versus normalized channel length position in CSDG MOSFET, SDMG CSDG MOSFET, and STMG CSDG MOSFET at $V_{DS} = 0.1$, $V_{GS} = 0.2V$, and $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

the STMG channel leads to a reduction in the hot-carriers effect.

The observed trend indicates that an increase in the L1:L2:L3 ratio, coupled with a rise in the proportion of the larger work function gate, leads to an increase in threshold voltage. This is because a higher gate voltage is needed to activate the region under L1 compared to L2 and L3, given that L1 possesses the highest work function. Additionally, the activation of regions under L2 and L3 is contingent upon forming a channel under L1. Consequently, Region L1 contributes to an increase in threshold voltage($V_{Th}$) [160, 161]. This results to a lower threshold voltage degradation as shown in Figure 6.11. Hence, the STMG CSDG MOSFET (1:2:3) tends to have the lowest variation in the degradation of the threshold voltage compared to other analyzed multi-gate structures.

However, for the STMG CSDG MOSFET (3:2:1) and SDMG CSDG MOSFET (2:1), as the channel length decreases beyond 50 $nm$, the drain-source voltage becomes obvious. Meanwhile, as the drain voltage ($V_{Th}$) increases further to 0.4, the SDMG CSDG (2:1) and STMG CSDG MOSFET(3:2:1) suffer the effect of Drain induced barrier lowering (DIBL), which makes the threshold voltage unstable.

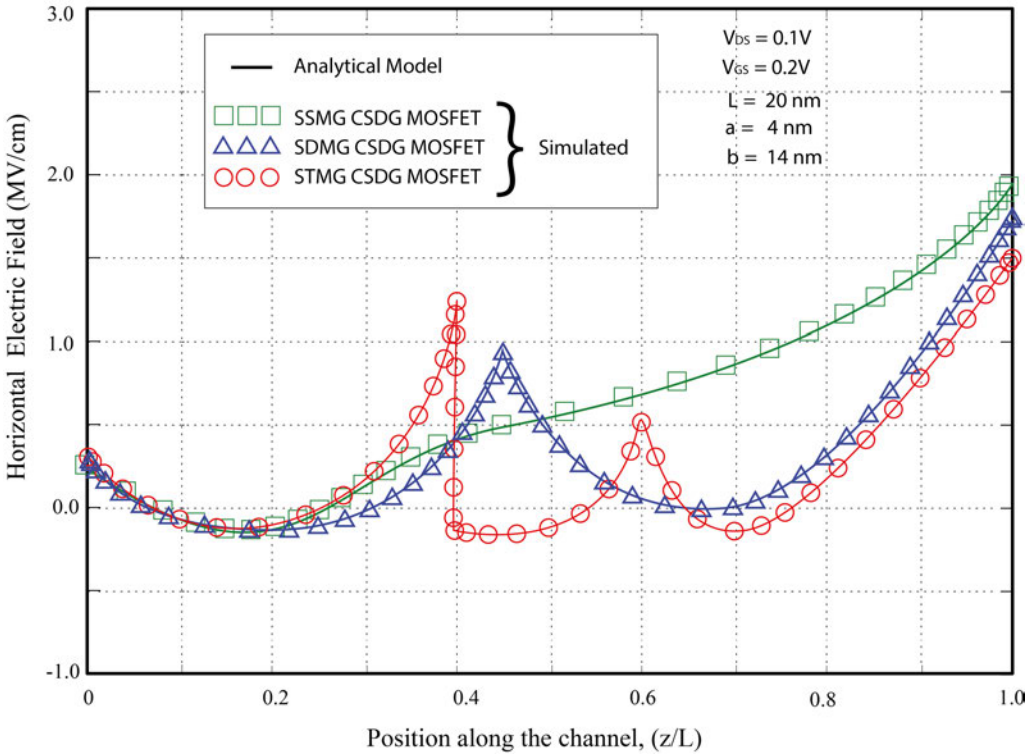


FIGURE 6.9: Horizontal Electric field variation versus normalized channel length position in CSDG MOSFET, SDMG CSDG MOSFET, and STMG CSDG MOSFET at $V_{DS} = 0.1, and V_{GS} = 0.2V.$, $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

DIBL is the disparity in threshold voltage resulting from an increase in drain voltage. The impact of DIBL on the proposed gate material CSDG MOSFET is illustrated in Figure 6.12. It is evident that gate material configurations in STMG CSDG MOSFET exhibit lower DIBL compared to those in SDMG CSDG MOSFET configurations. This discrepancy arises due to the more pronounced screening effect in STMG, in contrast to SDMG CSDG MOSFET.

Within the STMG CSDG MOSFET configurations (STMG CSDG MOSFET (1:1:1), STMG CSDG MOSFET (1:2:3), and STMG CSDG MOSFET (3:2:1)), the STMG CSDG MOSFET (1:2:3) configuration stands out for its superior DIBL performance. This superiority is attributed to its larger screening effect, particularly from L2 and L3. The enhanced screening effect ensures that the barrier height for channel carriers at the source's edge undergoes less variation with an increasing drain voltage. Therefore, as seen in the Figure 6.12, It's obvious that as the DIBL increases, its effect on the STMG CSDG MOSFET structure is far less compared with SDMG CSDG MOSFET structure as the channel length decreases.

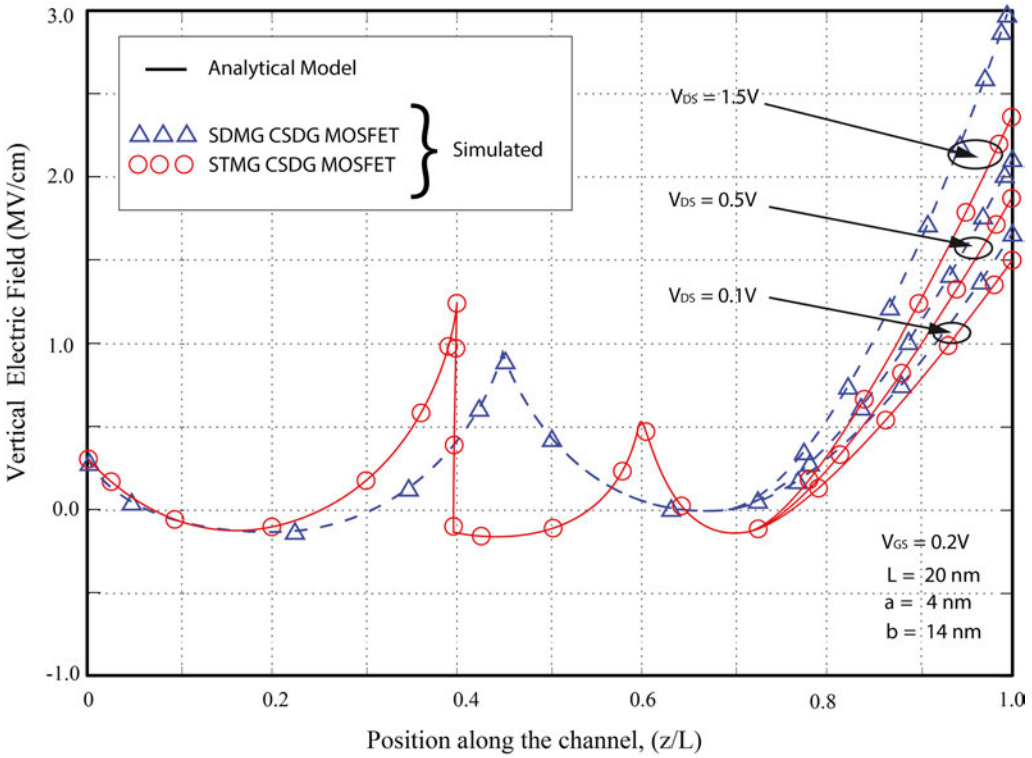


FIGURE 6.10: Electric field variation versus normalized channel length position for different drain biases. STMG structure is compared with SDMG CSDG structure at $V_{DS} = 0.1V$, $V_{DS} = 0.5V$, $V_{DS} = 1.5V$, and $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

The focal point of several research interest in the design of nanoscale integrated circuits for low-power consumption and high-speed switching performance has been the reduction of leakage current. In a MOSFET, the gate voltage controls the current flow between the source and drain terminals. However, when Short-Channel Effects come into play, it hampers the MOSFET's ability to control this current effectively. These worsen as the channel length is lowered to the nanoscale. This leads to degradation in the Subthreshold swing (SS) and an increase in the OFF-state leakage current. Hence, the SS is a performance matrix for measuring the electron response to the gate voltage signal. As illustrated in Equation (6.55), Figure 6.13 portrays the impact of an increased gate bias on the minimum potential. The slope in the graph indicates that the STMG CSDG MOSFET (1:2:3) structure exhibits the highest slope, effectively elevating the channel potential barrier to mitigate short-channel effects compared to other structures of CSDG MOSFET. Given that subthreshold swing is inversely proportional to the slope, it is evident that the STMG CSDG MOSFET (1:2:3) structure will accordingly decrease, potentially resulting in minimal leakage current. This is particularly advantageous as the CSDG MOSFET structure undergoes ultra-large scaling integration, contributing

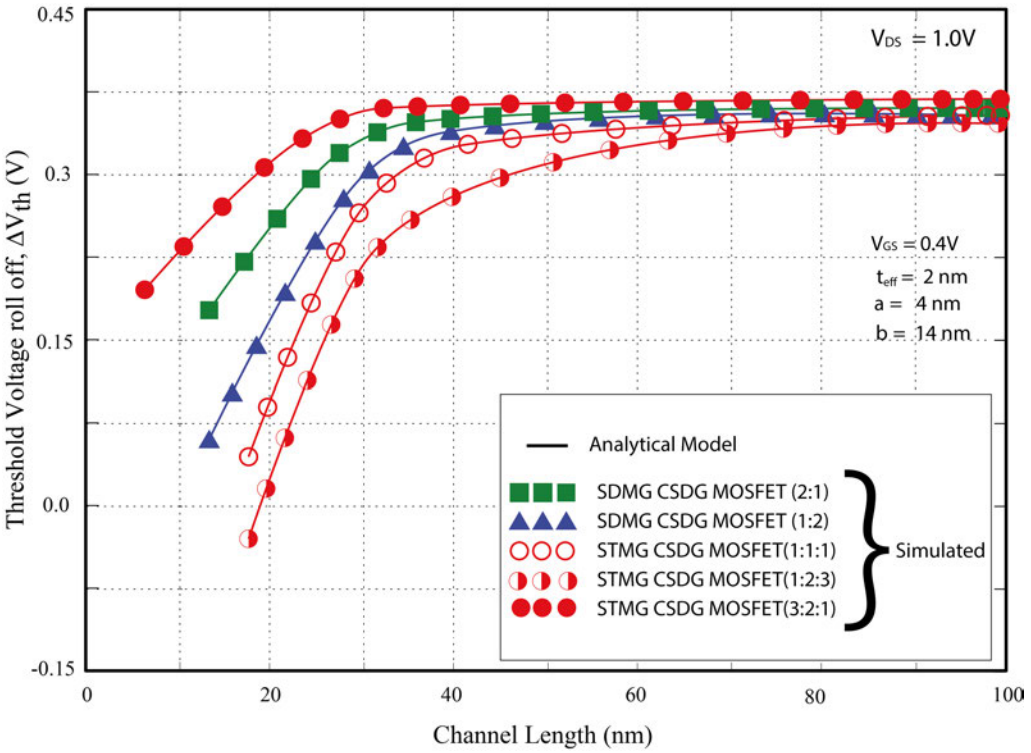


FIGURE 6.11: Threshold voltage roll-off with channel length for different CSDG MSOFET Structural gate material architecture with $V_{DS} = 1.0\ V$, and $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

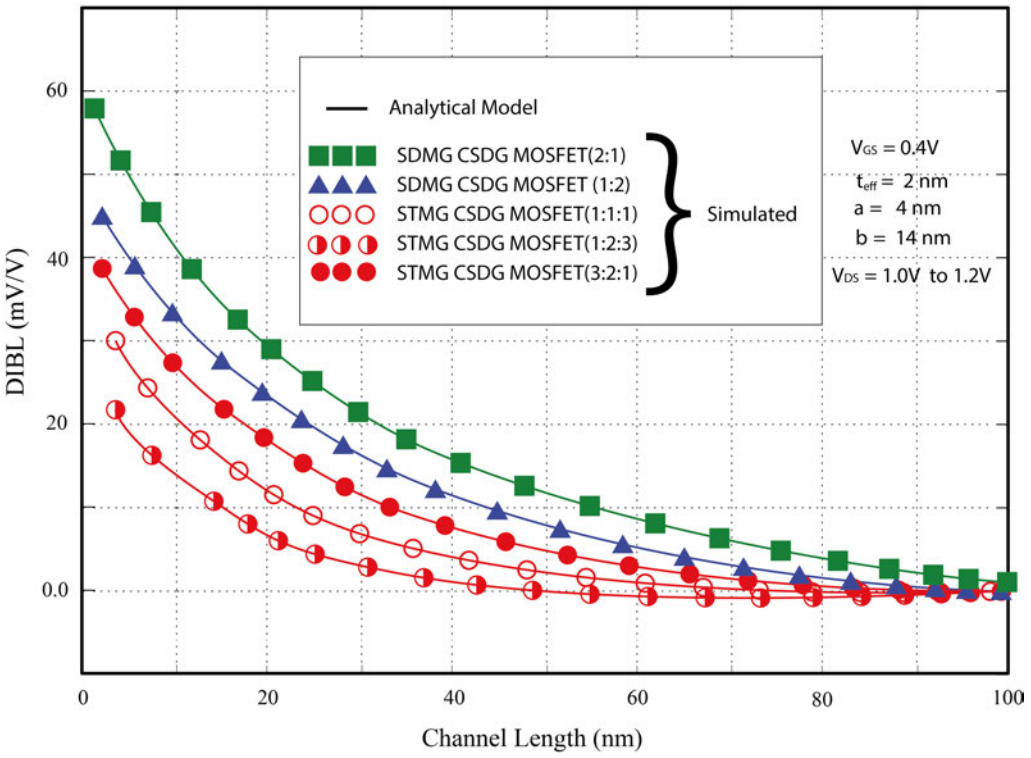


FIGURE 6.12: DIBL variation with channel length from $Vds = 1.0\ V$ to $Vds = 1.2\ V$, and $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

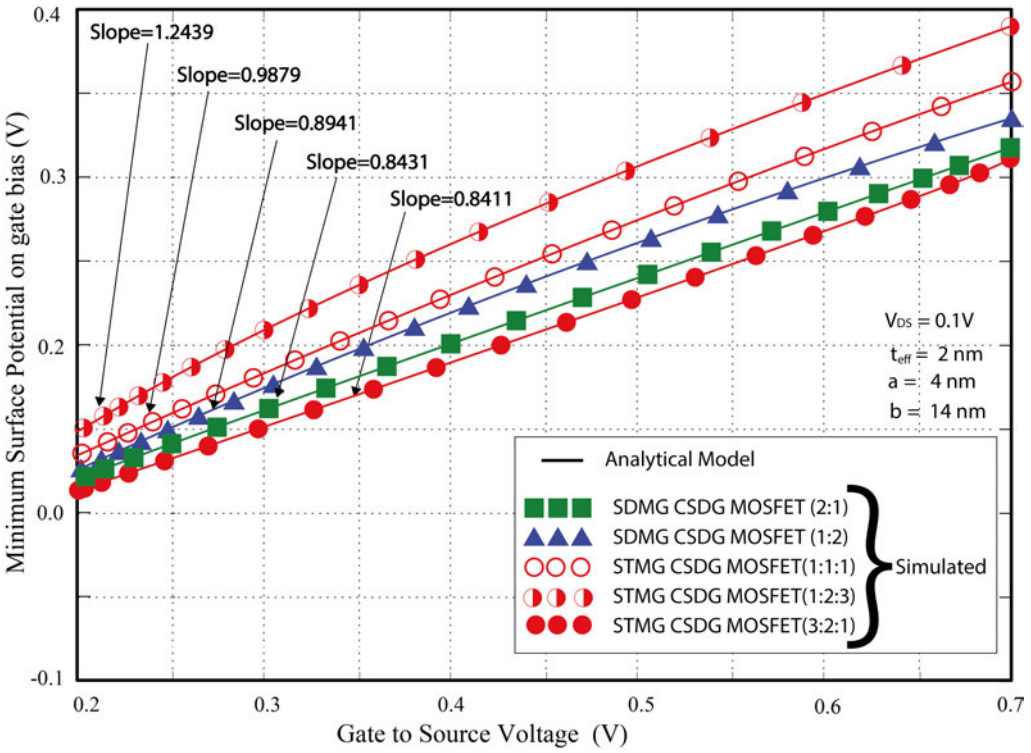


FIGURE 6.13: The variation of the minimum surface potential on gate bias,$\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

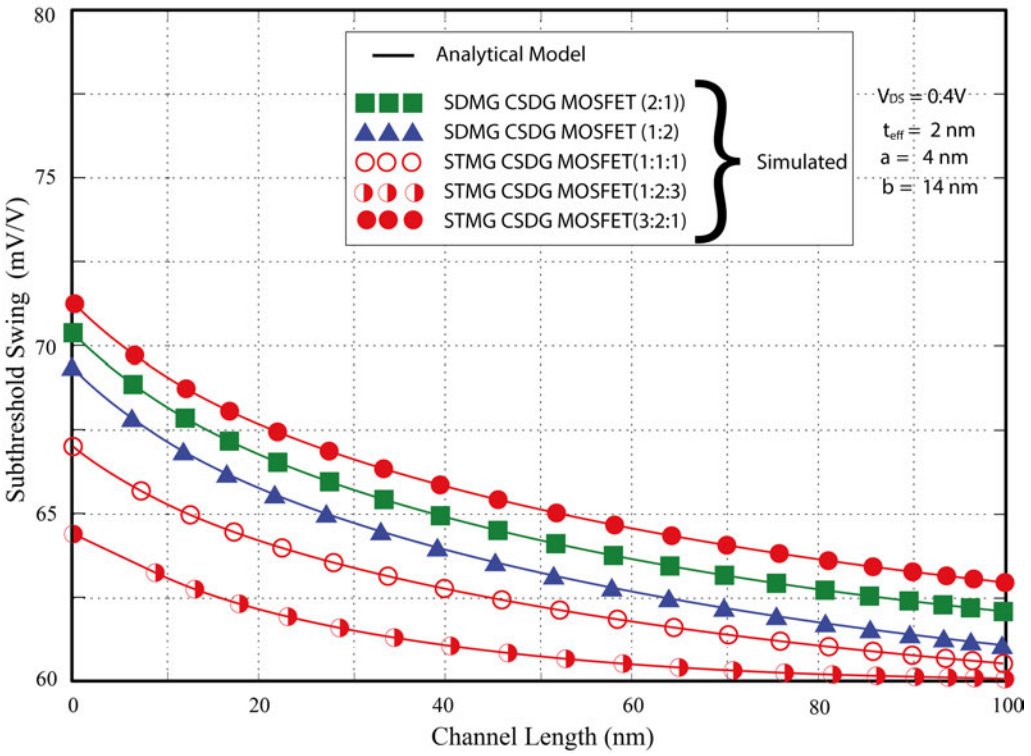


FIGURE 6.14: the variation in subthreshold swing (SS) versus the channel length across various CSDG MOSFET structures $\Phi_{M1} = 4.8\ eV, \Phi_{M2} = 4.6\ eV, \Phi_{M3} = 4.4\ eV$

to reduced power consumption.

Subthreshold Swing is a key parameter that aids in quantifying the efficiency of the turn-off process in MOSFETs. It provides valuable insights into energy consumption, leakage current, and overall device performance during the transition from the on-state to the off-state. A MOSFET with a lower subthreshold swing experiences less leakage current during turn-off, improving power efficiency. Figure 6.14 illustrates the variation in subthreshold swing versus the channel length across various CSDG MOSFET structures. It is evident that STMG CSDG MOSFET (1:2:3) structures exhibit the lowest subthreshold swing compared to other CSDG MOSFET configurations. Consequently, they present the smallest leakage current, attributed to the presence of screening gates and high-K materials.

With silicon dioxide (SiO2) as the gate dielectric, as the MOSFET scales down, the thinning SiO2 results in increased direct tunneling, leading to higher subthreshold swing and leakage current. In our model, the added high-k materials to Silicon dioxide have a higher dielectric constant than SiO2, allowing for thicker gate dielectrics without sacrificing capacitance. This helps to reduce tunneling and, consequently, improves subthreshold swing in the CSDG MOSFETs structures with STMG CSDG MOSFET (1:2:3) configuration having the best subthreshold swing as illustrated in Figure 6.14. Table 6.3 presents a comparison of the results for various CSDG MOSFET structures.

The results obtained from the simulations, as presented in Table 6.3, offer a comprehensive evaluation of the proposed structure. In conclusion, the findings indicate that the proposed structure successfully fulfills all the necessary requirements for advanced semiconductor devices. Notably, it excels in terms of drain-induced barrier lowering, providing superior control over the channel, and exhibiting significantly reduced leakage current. These advantages are particularly evident when the channel length is maintained below 10 $nm$.

TABLE 6.3: Results Comparison of Various Device Performance matrix with STMG CSDG MOSFET at 10 $nm$

| MOSFET Structure | $I_{on}(mA)$ | $I_{off}(\mu A)$ | $V_{th}(V)$ | SS (mV/dec) | DIBL (mV/V) |
|---|---|---|---|---|---|
| SDMG CSDG MOSFET (4.6 eV, 4.8 eV) (2:1) | 3.125× $10^{-4}$ | 5.3721 × $10^{-5}$ | 0.3021 | 68.4515 | 40.2351 |
| SDMG CSDG MOSFET (4.8 eV, 4.6 eV) (1:2) | 2.376× $10^{-3}$ | 5.1721× $10^{-7}$ | 0.3214 | 67.2341 | 32.4567 |
| STMG CSDG MOSFET (4.8 eV, 4.8 eV, 4.8 eV) (1:1:1) | 3.3723× $10^{-2}$ | 4.1723× $10^{-10}$ | 0.3514 | 66.7641 | 21.4578 |
| STMG CSDG MOSFET (4.8 eV, 4.6 eV 4.4 eV ) (1:2:3) | 2.2134× $10^{-1}$ | 2.3723× $10^{-14}$ | 0.3714 | 62.9814 | 15.1435 |
| STMG CSDG MOSFET (4.4 eV, 4.6 eV 4.8 eV ) (3:2:1) | 4.3863× $10^{-2}$ | 4.4723× $10^{-9}$ | 0.2198 | 69.1646 | 29.457 |

## 6.11 Chapter Summary

In this chapter, we conduct a comparative analysis among various gate-engineered MOSFET structures of identical dimensions to assess their resilience against short-channel effects. The investigation also explores the impact of different length ratios within the three channel regions associated with distinct gate materials in STMG MOSFET on SCEs characteristics parameters. The study's findings demonstrate that STMG MOSFETs and SDMG MOSFETs with a higher L1:L2:L3 ratio, exemplified by the STMG (1:2:3) configuration and SDMG (1:2) configuration, exhibit superior threshold voltage roll-off. This enhanced performance is attributed to these devices at low drain voltage. Also, as channel length decreases, the effect of the low significant voltage increases, which causes DIBL effect, is minimized. The structural arrangement with $L1 : L2 : L3$ ratio, exemplified by the STMG (1:2:3), showcases heightened carrier transport efficiency and improved DIBL performance, owing to the larger 'screen-gate.' and the presence of the high-K material further reduces the subthreshold swing, which leads to decrease in leakage current. The developed analytical model provides insights into the nuanced

interplay between gate engineering, channel region dimensions, and SCEs characteristics and proposes the best configuration to satisfy performance and power consumption. The comparative study enhances our understanding of the advantages of associating the gate-engineering concept of CSDG MOSFET structure with oxide engineering to mitigate the trade-off between performance and power consumption. This will contribute valuable information to the ongoing pursuit of optimizing transistor performance in semiconductor devices.

# Chapter 7

# Conclusion and Recommendation

In this segment, concise conclusions derived from each chapter of the thesis are presented, encapsulating the key findings. Additionally, the subsequent section delineates suggested avenues for future research endeavors.

## 7.1 Conclusions

Chapter 3 extensively investigates the natural scaling length of CSDG MOSFETs, concentrating on an in-depth analysis of their scalability. The study uncovers notable insights: with increased Silicon thickness, the external gate exhibits a diminished scaling factor in contrast to the internal gate. This differential scaling leads to a heightened electrostatic influence of the external gate on the channel. Conversely, as Silicon thickness diminishes, both gates demonstrate nearly equal control over the channel, enhancing resistance against SCEs. Notably, CSDG MOSFETs exhibit the least scaling factor compared to SOI MOSFETs, DG MOSFETs, and CSG MOSFETs.

The experimental approach employed the resolution of the Poisson Equation for the cylindrical structure, leveraging the Parabolic Potential Approximation (PPA) model in the radial section. Significantly, the authors introduce a groundbreaking contribution—the derivation of a closed-form expression formula for the natural length of CSDG MOSFET. This formula, reported for the first time, is poised to serve as a guiding principle in the design process, offering valuable insights into the behavior of CSDG MOSFETs. The results further highlight that CSDG MOSFET exhibits the highest scaling factor, reaching 4.3. This elevated scaling factor translates to CSDG MOSFET having the smallest natural length among various device structures, underscoring its potential for advanced semiconductor applications.

In Chapter 4, the authors introduce a quantum scaling length model and quantum scaling factor employing the quantum confinement approach. A comprehensive exploration into the performance of CSDG MOSFETs opens avenues for defining the scaling limits. This is achieved through a meticulous evaluation of the trade-off between the quantum natural length and the classical natural length of CSDG MOSFETs. The obtained results are systematically juxtaposed with those of CSG MOSFETs, revealing a distinct advantage of CSDG MOSFETs in terms of superior device characteristics at the quantum level.

The quantum scaling length model, a hallmark of Chapter 4, employs principles of quantum confinement to delve into the intricacies of scaling phenomena in CSDG MOSFETs. Through this approach, the research not only contributes to advancing the understanding of quantum effects on device scaling but also establishes a comparative framework with CSG MOSFETs. The findings highlight the quantum superiority of CSDG MOSFETs, offering promising insights for the development of next-generation electronic devices where quantum effects play a pivotal role in shaping device performance.

In Chapter 5, the authors delve into a comprehensive exploration of the sensitivity of multi-gate MOSFETs to process variations, employing analytical solutions derived from the 2-D Poisson's equation, which were further validated through meticulous device simulations. This investigation sheds light on the nuanced impact of process variations on the performance characteristics of multi-gate MOSFETs, with a specific focus on CSDG MOSFET and CSG MOSFET devices.

Our analysis observed that the lightly doped CSDG MOSFET exhibited the smallest threshold voltage ($V_{th}$) dispersion due to process variations and dopant number fluctuations. This implies that the choice of doping concentration, especially in lightly doped configurations, plays a pivotal role in minimizing $V_{th}$.

Interestingly, our findings also highlight a noteworthy trend in heavily doped devices. In these instances, dopant number fluctuations emerge as a critical factor, potentially overshadowing other sources of variability and becoming the dominant contributor to overall $V_{th}$ variation. This insight underscores the significance of precise control over doping levels, particularly in heavily doped multi-gate MOSFETs, to ensure consistent and reliable device performance.

Moreover, our investigation extends to the comparison between CDSG MOSFET and CSG MOSFET devices. The results suggest that the $V_{th}$ dispersion of CSDG MOSFET devices is comparatively smaller than that of CSG MOSFET. This phenomenon can be attributed to the superior immunity of CSDG MOSFET structures to dopant number fluctuations. The hollow cylindrical architecture of CSDG MOSFETs provides enhanced

control over the channel region, thereby mitigating the impact of dopant variations and contributing to more stable threshold voltage characteristics.

In essence, our study not only underscores the intricate interplay of process variations and doping strategies in CSDG MOSFETs, but also elucidates the potential advantages of CSDG MOSFET architectures in terms of mitigating $V_{th}$ dispersion. These insights are crucial for the continued advancement of semiconductor technology, guiding the optimization of fabrication processes and design considerations for enhanced performance and reliability in next-generation electronic devices.

In Chapter 6, a novel model was proposed to exploit the concept of gate-material engineering and gate-oxide engineering to eliminate the trade-off between the device performance and device power consumption at the nanoscale level. A comparison was made between different CSDG MOSFET configurations, and the results were presented in terms of an improvement in potential distribution and electric field. The analyzed novel structure consisting of the three stacked regions, each representing $L_1$, $L_2$, and $L_3$ with a lightly doped channel of $1 \times 10^{17} cm^{-}3$ increases carrier transport efficiency compared to the SSMG and SDMG structure of the CSDG device. Additionally, the gate materials have varying work functions in decreasing order from source to drain: $\Phi_{M1} = 4.8\ eV\ (e.g., Au), \Phi_{M2} = 4.6\ eV\ (e.g., Mo), \Phi_{M3} = 4.4\ eV\ (e.g., Ti)$, which optimized the STMG MOSFET structure by reducing the peak electric field at the drain end. This reduction in the electric field of the STMG channel Further leads to a reduction in the hot-carriers effect.

Also, it has been apparent that the structural arrangement of $1:2:3$ of STMG MOSFET structure offers the best carrier efficiency and improved DIBL performance than other structural arrangement of STMG MOSFET. The result obtained shows STMG MOSFET $(1:2:3)$ arrangement has the lowest OFF-current of $2.3723 \times 10^{-}14\mu A$, which shows less leakage of current compared to other structural arrangement of CSDG MOSFET. This result underscores the remarkable reduction in current leakage achieved by this specific configuration when contrasted with other structural arrangements of CSDG MOSFETs. This observation positions the STMG MOSFET (1:2:3) arrangement as a highly promising and innovative structural design, particularly well-suited for applications demanding low power consumption, exceptional efficiency, and better switching. Furthermore, the subthreshold slope closely matched the ideal value with $62.98 mV/dec$ values, indicating a favorable performance.

## 7.2 Future Recommendations

A CSDG MOSFET, renowned for its application in high-frequency scenarios, data transmission, and RF circuits due to its promising characteristics, serves as the focal point of this study. In this research endeavor, the authors present a comprehensive mathematical analysis of the CSDG MOSFET. This analysis entails the derivation of a natural scaling length model, establishing a clear linkage between the natural length and the quantum natural length. Moreover, the research delves into the sensitivity of the CSDG MOSFET to process variations via an analytical approach, shedding light on the device's resilience to manufacturing fluctuations. To further enhance device performance, the study introduces an innovative concept of stacked triple gate materials coupled with gate-oxide engineering.

Looking ahead, there is potential for the development of a generalized quantum confinement model that can be applied to a broader spectrum of multi-gate devices, extending the utility of this research. Additionally, an avenue for future exploration lies in the creation of a mathematical model that incorporates quantum corrections specifically tailored for CSDG MOSFETs featuring a Germanium channel. Furthermore, a new study can point to the feasibility of investigating other critical device parameters, such as transconductance, within the context of dopant number fluctuation.

Additionally, research into gate material engineering has demonstrated its potential to improve the device's electrical properties. Future efforts will undoubtedly be guided and informed by the revelations produced by the research design suggested in this thesis. It is possible to expand the Triple material gate design model to look at how it affects variables like velocity saturation and other short-channel effects. A small-signal model can be derived using the device physics described in this work as a foundation, and future research may examine device operation at high frequencies. The correlation between experimental device fabrication and numerical outcomes adds a useful dimension to the study. Additional investigations can extend to the exploration of alternative high-K materials, which hold the potential to enhance device performance even further, particularly as devices continue to shrink to nanometer scales. Moreover, it would be beneficial to incorporate quantum mechanical effects into the analysis of the proposed device structure to offer valuable insights into its behavior and performance characteristics at the quantum level.

# Appendix A

# Derivation of Coefficients in Chapter 5

The coefficients of Equation 5.10 are derived by substituting the arbitrary coefficient to Equation 5.1 and factorizing with respect to internal and external gates.

$$
\begin{aligned}
P_1 &= \frac{\Big(4 + 2(t_{si} - 2a)^2((t_{si} - 2a) + 1)[1 - C_{oxa}]\Big)}{\Big(4 + 2(t_{si} - 2a)(2b - t_{si})[C_{oxb}(t_{si} - 2a)(2b - t_{si}) - C_{oxa}(1 + (t_{si} - 2a))]\Big)} \\
P_2 &= \frac{\Big(4 + 2(t_{si} - 2a)(2b - t_{si})[C_{oxb}(t_{si} - 2a)(2b - t_{si}) - C_{oxa}(1 + (t_{si} - 2a))]\Big)}{\Big(4 + 2(t_{si} - 2a)^2((t_{si} - 2a) + 1)[1 - C_{oxa}]\Big)} \\
Q_1 &= \frac{\Big(4 + 2(t_{si} - 2a)^2((t_{si} - 2a) - C_{oxa})\Big)}{\Big(4 + 2(t_{si} - 2a)(2b - t_{si})[C_{oxb}(t_{si} - 2a)(2b - t_{si}) - C_{oxa}(1 + (t_{si} - 2a))]\Big)} \\
Q_2 &= \frac{\Big(4 + 2(t_{si} - 2a)^2((t_{si} - 2a) - C_{oxa})\Big)}{\Big(4 + 2(t_{si} - 2a)^2((t_{si} - 2a) + 1)[1 - C_{oxa}]\Big)}
\end{aligned}
\tag{A.1}
$$

The coefficient of differential Equation in Equation 5.11 are derived from Equation 5.1:

$$\sigma_1 = \frac{\left(E_1\right)}{\left(G_1\right)}$$

$$\alpha_1 = \frac{\left(qN_a\right)}{\left(\epsilon_{si}G_1\right)} + V_{GF}\left[\frac{F_1}{G_1}\right]$$

$$\sigma_2 = \frac{\left(E_1\right)}{\left(G_2\right)} \tag{A.2}$$

$$\alpha_2 = \frac{\left(qN_a\right)}{\left(\epsilon_{si}G_2\right)} + V_{GF}\left[\frac{F_2}{G_2}\right]$$

The constants from Equation A.2 are given as follows:

$$E_1 = \frac{\left(P_1(t_{si}-2a)\left[(C_{oxb}-C_{oxa})-(2b-t_{si})C_{oxa}\right]\right)-4C_{oxb}(1-P_2)}{\left([\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]r\right)}$$

$$E_2 = \frac{\left((t_{si}-2a)\left[(C_{oxb}-C_{oxa})-P_1(2b-t_{si})C_{oxa}\right]\right)-4C_{oxa}P_1+C_{oxb}}{\left([\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]r\right)}$$

$$F_1 = \frac{\left((t_{si}-2a)\left[(C_{oxb}-C_{oxa})(Q_1-1)\right]\right)+4(C_{oxa}+C_{oxa})(1-Q_2)}{\left([\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]r\right)}$$

$$F_2 = \frac{\left((t_{si}-2a)\left[(Q_1+1)(2b-t_{si})-(C_{oxb}-C_{oxa})\right]\right)+4C_{oxa}(1+Q_2)+C_{oxb}}{\left([\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]r\right)}$$

$$G_1 = 1+\frac{(t_{si}-2a)C_{oxa}\left[(2(2b-t_{si})+1)\right]-P_2\left[(t_{si}-2a)(C_{oxb}-C_{oxa})\right]}{\left(4[\epsilon_{si}(((t_{si}-2a)-(2b-t_{si}))]\right)}$$

$$+\left[\frac{(t_{si}-2a)\left[(C_{oxb}-C_{oxa})P_2\right]-\left[(t_{si}-2a)(C_{oxa})\right]}{\left(4[\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]\right)}\right]r+\left[\frac{\left[(1+P_2)(C_{oxb})\right]}{\left(4[\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]\right)}\right]r^2$$

$$G_2 = 1+\frac{2(t_{si}-2a)C_{oxa}\left[((2b-t_{si})-(t_{si}-2a))-2C_{oxa}(2b-t_{si})+P_2C_{oxa}(2(2b-t_{si})+1)\right]}{\left(4[\epsilon_{si}(((t_{si}-2a)-(2b-t_{si}))]\right)}$$

$$+\left[\frac{(t_{si}-2a)\left[(C_{oxb}-C_{oxa})\right]-\left[P_1(2b-t_{si})(C_{oxa})\right]}{\left(4[\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]\right)}\right]r+\left[\frac{\left[(C_{oxa}P_1)+(C_{oxb})\right]}{\left(4[\epsilon_{si}((t_{si}-2a)-(2b-t_{si}))]\right)}\right]r^2 \tag{A.3}$$

# Appendix B

# Derivation of Coefficients in Chapter 6

Considering the internal gate from Equation 6.33, and using the boundary conditions from Equation 6.6 and Equation 6.7. The coefficients are derived as given.

$$
\begin{aligned}
M_1 &= \frac{(v_{bi} + \frac{\sigma_a}{\lambda_a^2})(e^{-\lambda_a z} - 1) - V_{DS}}{(sinh(\lambda_a z))} \\
N_1 &= \frac{(v_{bi} + \frac{\sigma_a}{\lambda_a^2})(e^{\lambda_a z} - 1) - V_{DS}}{(sinh(\lambda_a z))} \\
M_2 &= \frac{(v_{bi} + \frac{\sigma_a}{\lambda_a^2})(e^{-\lambda_a (z - L_1)} - 1) - V_{DS}}{(sinh(\lambda_a (z - L_1)))} \\
N_2 &= \frac{(v_{bi} + \frac{\sigma_a}{\lambda_a^2})(e^{\lambda_a (z - L_1)} - 1) - V_{DS}}{(sinh(\lambda_a (z - L_1)))} \\
M_3 &= \frac{(v_{bi} + \frac{\sigma_a}{\lambda_a^2})(e^{-\lambda_a (z - (L_1 + L_2))} - 1) - V_{DS}}{(sinh(\lambda_a (z - (L_1 + L_2)))} \\
N_3 &= \frac{(v_{bi} + \frac{\sigma_a}{\lambda_a^2})(e^{\lambda_a (z - (L_1 + L_2))} - 1) - V_{DS}}{(sinh(\lambda_a (z - (L_1 + L_2))))}
\end{aligned}
\tag{B.1}
$$

Similarly, the external gate coefficient is obtained as follows

$$\begin{aligned}
M_4 &= \frac{(v_{bi}+\frac{\sigma_b}{\lambda_b^2})(e^{-\lambda_b z}-1)-V_{DS}}{(sinh(\lambda_b z))} \\
N_4 &= \frac{(v_{bi}+\frac{\sigma_b}{\lambda_b^2})(e^{\lambda_b z}-1)-V_{DS}}{(sinh(\lambda_b z))} \\
M_5 &= \frac{(v_{bi}+\frac{\sigma_b}{\lambda_b^2})(e^{-\lambda_b (z-L_1)}-1)-V_{DS}}{(sinh(\lambda_b (z-L_1)))} \\
N_5 &= \frac{(v_{bi}+\frac{\sigma_b}{\lambda_b^2})(e^{\lambda_b (z-L_1)}-1)-V_{DS}}{(sinh(\lambda_b (z-L_1)))} \\
M_6 &= \frac{(v_{bi}+\frac{\sigma_b}{\lambda_b^2})(e^{-\lambda_b (z-(L_1+L_2))}-1)-V_{DS}}{(sinh(\lambda_b (z-(L_1+L_2)))} \\
N_6 &= \frac{(v_{bi}+\frac{\sigma_b}{\lambda_b^2})(e^{\lambda_b (z-(L_1+L_2))}-1)-V_{DS}}{(sinh(\lambda_b (z-(L_1+L_2))))}
\end{aligned} \tag{B.2}$$

The coefficients, $V_1, V_2$, and $V_3$, from Equation 6.49, are expressed as follows.

$$\begin{aligned}
V_1 &= d_1 d_2 - d_3^2 \\
V_2 &= d_2 d_4 + d_1 d_5 - 2 d_3 d_6 \\
V_3 &= d_4 d_5 + d_6^2
\end{aligned} \tag{B.3}$$

where the variables are expressed as given.

$$\begin{aligned}
d_1 &= \frac{(e^{-\lambda_a z}-1) d_3}{(sinh(\lambda_a z))} \\
d_2 &= \frac{(e^{\lambda_a z}-1) d_3}{(sinh(\lambda_a z))} \\
d_3 &= \frac{\mathcal{H}_{\dashv}}{\mathcal{H}_{\dashv}} \\
d_4 &= \frac{(v_{bi})(e^{-\lambda_a z}-1)-(\frac{qN_a}{\epsilon_{si}\mathcal{H}_{\dashv}})(e^{-\lambda_a z}-1)+V_{DS}}{(sinh(\lambda_a z))} \\
d_5 &= \frac{(v_{bi})(e^{\lambda_a z}-1)-(\frac{qN_a}{\epsilon_{si}\mathcal{H}_{\dashv}})(e^{\lambda_a z}-1)+V_{DS}}{(sinh(\lambda_a z))} \\
d_6 &= 2\phi_f - V_{tha1} - (\frac{qN_a}{\epsilon_{si}\mathcal{H}_{\dashv}})
\end{aligned} \tag{B.4}$$

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