A DSP-BASED DIGITAL CONTROLLER FOR A THYRISTOR CONTROLLED SERIES CAPACITOR

by

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I hereby declare that all the material incorporated into this thesis is my own original and unaided work except where a specific reference is made by name or in the form of a numbered reference. The work contained herein has not been submitted for a degree at any other university.

Signed: _____

Anand Pillay

This thesis is dedicated to my parents

Abstract

The power transfer capability of long high voltage transmission lines is often limited by the inductive reactance of the transmission line. Series compensation is in some instances employed to lower the inductive reactance of the transmission line which increases the transmission line power transfer capability. Numerous methods have been employed to provide series compensation of a transmission line. One such method is to use a thyristor controlled series capacitor (TCSC).

A thyristor controlled series capacitor (TCSC) belongs to the flexible alternating current transmission systems (FACTS) family of devices. It is a variable capacitive and inductive reactance device that can be used to provide series compensation in high voltage transmission lines. One of the significant advantages that a TCSC has over other series compensation devices is that the TCSC's reactance is instantaneously and continuously variable. This means that the TCSC can be used not only to provide series compensation but can also be used to enhance the stability of the power system.

However accurate control of the TCSC is challenging due to its highly non-linear variable reactance characteristic. The TCSC consists of back to back thyristors that control the reactance of the TCSC. By changing the trigger angle of these back to back thyristors it is possible to vary the reactance of the TCSC. The reactance characteristic becomes highly non linear at higher levels of compensation; at such operating points the trigger angle of the thyristors needs to be accurately controlled to avoid small variations in the thyristor trigger angle causing significant variation in the reactance of the TCSC.

Literature has shown that there is an acceptable limit to the resolution of the thyristor trigger angle based on the parameters of the components used in the TCSC. If a controller is developed to meet this acceptable level of thyristor trigger angle resolution, then the operation of the TCSC will also be acceptable and its operation will not result in unwanted fluctuations in the transmission line variables.

This thesis details the development of such a controller for use in a laboratory-scale TCSC. The thesis then goes on to present the practical results obtained from laboratory experiments on the laboratory-scale TCSC with the TCSC triggering controller being used to control the operation of the laboratory-scale TCSC. For purposes of comparison and benchmarking, a detailed simulation model of the laboratory-scale TCSC is developed to take into account the non-ideal properties of the components used in make-up of the laboratory-scale TCSC since the theoretical model is derived assuming ideal conditions.

The detailed simulation model is also used to aid in the redesign the power circuit of the laboratory-scale TCSC in an attempt to improve the performance of the laboratory-scale TCSC by obtaining better agreement between the theoretical and practical results. The redesigned laboratory-scale TCSC is used to obtain practical results to confirm the findings of the simulation studies.

Finally, the TCSC triggering controller is tested using a real time digital simulator (RTDS). The simulation model developed on the RTDS consisted of a two area, four generator power, with the TCSC connected between the two areas. The RTDS simulation model is used to study the ability of the TCSC to damp inter-area mode oscillations and hence the RTDS simulation model incorporated a power oscillation controller. The input of TCSC triggering controller was "connected" to the power oscillation damping controller and the output of the TCSC triggering controller was "connected" to the thyristors of the TCSC.

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List of Symbols

The commonly used symbols and notations adopted in this thesis are listed below. Other symbols used in the text are explained where they first appear.

Acronyms

AC	Alternating Current
ADC	Analogue to Digital Converter
DAC	Digital to Analogue Converter
DSP	Digital Signal Processor
FACTS	Flexible Alternating Current Transmission System
PLL	Phase Locked Loop
POD	Power Oscillation Damping
PSCAD	Power System Computer Aided Design
RTDS	Real Time Digital Simulator
TCR	Thyristor Controlled Reactor
TCSC	Thyristor Controlled Series Capacitor

Symbols

α	Thyristor trigger angle
β	Thyristor conduction angle
π	Constant = 3.1416
θ	Instantaneous Angle
$^{\circ}$	Degrees (Angular)
Ω	Ohm
α_{RES}	Thyristor trigger angle at which resonance occurs
C	Capacitor
I_{LINE}	Transmission line current
K_B	Boost Factor
L	Inductor
pu	per unit
V_{CAP}	Voltage across the TCSC capacitor
X_C	Capacitive reactance
X_L	Inductive reactance
X_{TCR}	Thyristor Controlled Reactor reactance
X_{TCSC}	Thyristor Controlled Series Capacitor reactance
Z	Impedance

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Figure H.3: TCR current envelope for inter-area mode oscillations: POD input signal - Synthesised speed difference.....H.3

Figure H.4: Transmission line current response for inter-area mode oscillations: POD input signal - Direct speed difference.....H.4

Figure H.5: TCSC capacitor voltage response for inter-area mode oscillations: POD input signal - Direct speed difference.....H.4

Figure H.6: TCR current response for inter-area mode oscillations: POD input signal - Direct speed difference.....H.5

Figure H.7: Transmission line current response for inter-area mode oscillations: POD input signal – Rate of change of power flow.....H.6

Figure H.8: TCSC capacitor voltage response for inter-area mode oscillations: POD input signal – Rate of change of power flow.....H.6

Figure H.9: TCR current response for inter-area mode oscillations: POD input signal – Rate of change of power flow.....H.7

Chapter One

Introduction

1.1 General

Active power flow through a high voltage transmission line is often limited by the inductive reactance of the transmission line as well as by the stability limits of the system. This leads to the under utilisation of high voltage transmission lines. Traditional forms of fixed series capacitor compensation alleviate this problem to an extent by reducing the inductive reactance of the transmission line but are still limited by stability and fault condition considerations. Specifically during transmission line fault conditions, fixed series compensation may result in an increased amount of fault current.

An alternative is to use switched series compensation. This form of compensation relies on the use of mechanical circuit breakers to control the amount of series compensation capacitors inserted in the line, which would only be available in discrete amounts. This method of series compensation is better than the fixed type since it allows for the series compensation to be switched in or out of the transmission network depending on conditions. However the disadvantage of switched series compensation is that there are switching transients on the transmission network due to the operation of the mechanical circuit breakers and the operation of the mechanical circuit breakers is slow.

The advancement of power electronics made available devices that were capable of fast switching. This led to the advent of Flexible Alternating Current Transmission Systems (FACTS) devices. FACTS devices were designed conceptually awaiting the improvement of power electronic devices to the point were they can be used reliably in high voltage applications.

1.2 The Thyristor Controlled Series Capacitor

The Thyristor Controlled Series Capacitor (TCSC) belongs to the Flexible AC Transmission Systems (FACTS) group of power systems devices. The concept of the TCSC has been around since the mid 1980s, with the first known commercial installation being in 1992 [Christl1] in the United States of America. Essentially a TCSC is a variable reactance device that can be used to provide an adjustable series compensating reactance to a transmission line. Its advantage over other series compensating devices is that its reactance can be instantaneously and precisely controlled [IEE1]. This makes the TCSC well suited to enhance the stability of a power system [Haro1, Helbing1, Tan1, Yin1].

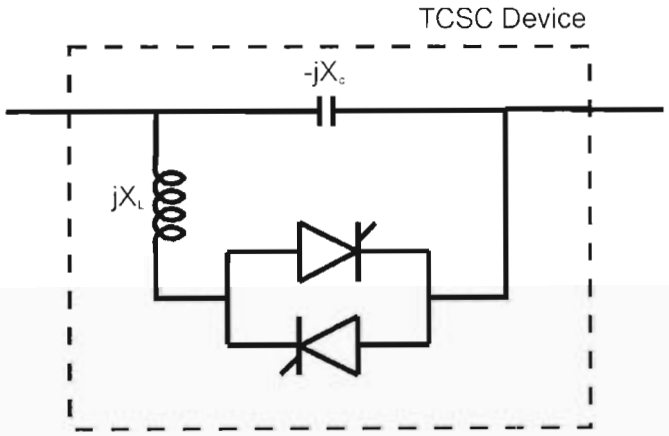

Figure 1.1: Simplified circuit diagram of a single phase TCSC

A TCSC consists of a fixed capacitor in parallel with a variable inductive reactance as shown in Figure 1.1. This variable inductive reactance is obtained by connecting back to back thyristors in series with a fixed-reactance inductor, and is known as a Thyristor Controlled Reactor or TCR. By controlling the trigger angle of the back to back thyristors, it is possible to vary the effective inductive reactance of the TCR, and hence control the reactance provided by the TCSC [IEE1].

The reactance of the TCSC can be capacitive or inductive, depending on the trigger angle of the back to back thyristors; however the area of interest in this thesis is confined to the operation of the TCSC in capacitive mode. The capacitive reactance characteristic of the TCSC is a highly non-linear function of the trigger angle of the back to back thyristors, which presents a number of technical challenges when

designing a controller for a TCSC. It will be shown that the consequence of an inadequate controller leads to unwanted fluctuations in the TCSC capacitive reactance.

As stated previously the advantage of a TCSC over other series compensating devices is that its capacitive reactance can be instantaneously and precisely controlled, but the realization of these advantages is dependant on the controller. Therefore a controller needs to be developed to fully exploit these properties of the TCSC and also overcome the technical challenges presented by the control of the TCSC's capacitive reactance. A review of the literature will show [Zheng1] that the thyristor trigger angle resolution of the controller needs to be less than 0.1° for the satisfactory control of the capacitive reactance of the TCSC.

1.3 Thesis objectives

The focus in this thesis will be on the development, implementation and testing of a high performance TCSC triggering controller to satisfactorily control the reactance of a laboratory-scale TCSC. The testing of the TCSC triggering controller necessitated the redesign and construction of a laboratory-scale TCSC in the Machines Research Laboratory at the University of KwaZulu-Natal [Pillay1, Mazibuko2]. The TCSC triggering controller and both the original, and redesigned laboratory-scale TCSC will be used to investigate the characteristics and behaviour of the laboratory-scale TCSC under static and dynamic conditions.

For purposes of an in-depth understanding of the laboratory-scale TCSC, a detailed simulation model of the laboratory-scale TCSC was also developed. The detailed simulation model of the laboratory-scale TCSC allowed for comparison of the practical results obtained from the laboratory-scale TCSC. The thesis then also considers the influence of the TCSC's own parameters on its static and dynamic performance, as well as on the requirements of the low level synchronisation and triggering controller.

1.4 Thesis layout

This thesis consists of nine chapters and has seven appendices. A brief overview of the chapters in the thesis is given below.

Chapter One provides an introduction to the TCSC series compensating device. The objectives of the thesis are stated, with the main objective of the thesis being the development and testing of a high performance TCSC triggering controller. Chapter Two provides detailed insight into the theory of operation of a TCSC. Chapter Two then goes on to focus on the variable reactance characteristic of the TCSC, providing an explanation as to why there is a need for an accurate (high resolution) triggering controller. The accuracy requirement of the controller is then defined based on a review of the literature.

Chapter Three presents the first set of practical results obtained using the original laboratory-scale TCSC [Mazibuko2] and a prototype TCSC triggering controller. The practical results are compared to results obtained from a detailed simulation model of the laboratory-scale TCSC. The detailed simulation model was developed to provide an in-depth understanding and accurate representation of the laboratory-scale TCSC. The important finding of Chapter Three is the identification of the effects of the non-ideal properties of the components used in the construction of the laboratory-scale TCSC.

Chapter Four discusses the prototype TCSC triggering controller that was used to obtain the practical results presented in Chapter Three. Although the prototype TCSC triggering controller was successfully implemented, its performance does not meet the requirement in the thyristor trigger angle resolution as proposed in literature. Chapter Four takes note of the reason for the shortcomings of the prototype TCSC triggering controller.

Chapter Five then uses the shortcomings of the prototype TCSC triggering controller as a starting point for the development of an improved hybrid TCSC triggering controller. Chapter Five discusses, in detail, a hybrid TCSC triggering controller that

is developed to meet the specification for the resolution of the thyristor triggering signals as proposed in literature. Finally, Chapter Five presents the results of tests conducted on the hybrid TCSC triggering controller.

Chapter Six presents results and findings of detailed simulation studies conducted in-order to specifically examine the impact of a TCSC's inductor parameters on the performance of a laboratory-scale TCSC. The outcome of the detailed simulation studies is the identification of two newly manufactured inductors that could result in improved performance of the laboratory-scale TCSC.

Chapter Seven presents practical results obtained using the hybrid TCSC triggering controller and the original design of the TCSC power circuit, in order to determine the performance improvement of the laboratory-scale TCSC due to the improvement in resolution of the hybrid TCSC triggering controller. The second set of practical results is obtained using the two different newly manufactured inductors together with the high-resolution hybrid TCSC triggering controller.

Chapter Eight presents further tests on the performance of the hybrid TCSC triggering controller, but using a representative high-voltage TCSC's parameters with the TCSC modeled on a real time digital simulator (RTDS). The use of the RTDS allows the performance of the hybrid TCSC triggering controller developed in this thesis to be studied without the problems of a laboratory-scale TCSC's non-ideal parameters affecting the results.

Finally Chapter Nine concludes the findings of this thesis, and makes suggestions for further work.

1.5 Contributions of this thesis

The contributions made by this thesis are the practical implementation of a controller for a laboratory-scale TCSC, which can be used for further research work. An accurate simulation model of the laboratory-scale TCSC has been developed taking into account the non-ideal characteristics of the laboratory-scale TCSC. This

simulation model can be used to predict the behaviour of the laboratory-scale TCSC. The performance of the TCSC for different inductor parameters is also documented in this thesis, in order to allow for future refinements of the laboratory-scale TCSC.

1.6 Research Publications

Some of the findings of this thesis have been presented at national and international conferences [Pillay1, Pillay2].

Chapter Two

Theory of operation of a thyristor controlled series capacitor

2.1 Introduction

Chapter One provided a brief background of how the implementation of series compensation was developed over the years. The benefit of series compensation is that it can be used to enhance the stability of a power system and increase the power transfer capability of high voltage transmission lines. A Thyristor Controlled Series Capacitor (TCSC) is a device that is capable of performing both of these functions. The manner in which the TCSC does this and an overview of its operation was given in Chapter One.

This chapter goes on to discuss the theory of operation of a TCSC in greater detail, beginning with a circuit analysis of the TCSC. Following the circuit analysis, the theory of operation of the TCSC and its capabilities are discussed. The significance of the sensitivity of the capacitive reactance of the TCSC to variations in its trigger angle is then discussed. The factors influencing the sensitivity and its effects are investigated.

The sensitivity of the reactance of the TCSC to changes in the thyristor trigger angle poses challenges when implementing a controller to control the triggering of the thyristors. A review of literature will show why this is so and the methodologies that have been proposed to ensure that the operation of the TCSC is satisfactory.

2.2 The thyristor controlled series capacitor

A TCSC is a variable inductive and capacitive reactance device. The main area of application of the TCSC will typically be for series compensation; therefore this thesis will confine the detailed analysis of the TCSC to the capacitive reactance mode of

operation, and give only a brief overview of the inductive reactance mode of operation. A TCSC consists of a fixed reactance capacitor connected in parallel with a variable inductor, and by varying the reactance of the inductive branch it is possible to change the reactance of the TCSC [IEE1, Matsuki2].

While TCSCs can be used to provide series compensation, their real benefits are realised during dynamic power system conditions. These benefits include the ability to control power flow and damp power oscillations [Christl1, Gama1]. There are at least three known commercial installations of TCSCs worldwide, one in Brazil [Gama1] and the other two in the United States of America [Christl1, Kinney1]. There are also numerous laboratory-scale TCSCs worldwide used for research purposes [Ghosh1, Haro1, Matsuki1, Mazibuko1, Rigby1, Yin1].

2.3 Circuit analysis of a TCSC

A single-phase TCSC consists of a fixed-reactance capacitor in parallel with a variable reactance inductor. This variable reactance inductor is obtained by connecting an inductor in series with back-to-back thyristors. For a three phase TCSC this arrangement is identical for all three phases. The inductor/thyristor parallel branch of the circuit is known as a thyristor controlled reactor. This branch of the circuit is the most important part of a TCSC and therefore requires further discussion.

2.3.1 Thyristor controlled reactor

A thyristor controlled reactor consists of back to back thyristors connected in series with an inductor as shown in Figure 2.1(a). The reactance characteristic of the TCR as a function of the trigger angle α of the thyristors is shown in Figure 2.1(b).

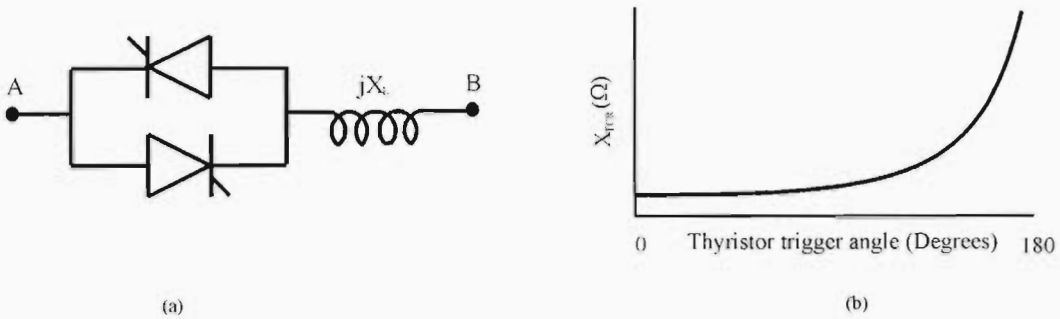

Figure 2.1: (a) Circuit diagram of a TCR; (b) Plot of TCR reactance versus thyristor trigger angle

The characteristic in Figure 2.1(b) shows that the inductive reactance of the TCR increases as the trigger angle of the back to back thyristors is increased from 0°. The equation describing the behaviour of the reactance of the TCR as a function of the thyristor trigger angle is given by [Kundur1]:

$$X_{TCR} = \frac{\pi X_L}{2(\pi - \alpha) + \sin 2\alpha} \qquad (2.1)$$

where

X_{TCR} is the net reactance of the TCR at the fundamental frequency

X_L is the reactance of the inductor at the fundamental frequency

α is the trigger angle of the thyristors

The circuit of a TCSC is obtained when a fixed reactance capacitor is added in parallel to the TCR. By understanding the operation of the TCR it is now possible to analyse the circuit diagram of a single phase TCSC and obtain insight into the operation and variable reactance characteristic of a TCSC.

2.4 Operation of a TCSC

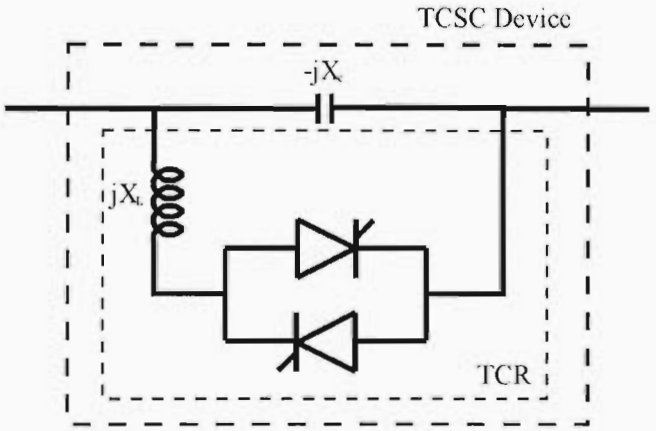

Figure 2.2: Simplified single line diagram of a TCSC

Having discussed the circuit diagram and operation of a TCR, it is now possible to analyse the circuit diagram of a TCSC to understand the operation of a TCSC in greater detail. As shown in Figure 2.2, a TCSC consists of two parallel branches one containing a fixed-reactance capacitor and the other a thyristor controlled reactor (TCR). Using this description and equation (2.1), used to describe the operation of a TCR, it is possible to arrive at the following formula used to describe the operation of a TCSC [Helbing1].

$$X_{TCSC} = jX_{TCR} // (-jX_C) \tag{2.2}$$

$$\therefore X_{TCSC} = \frac{-jX_C}{1 - \frac{X_C}{X_{TCR}}} \tag{2.3}$$

where

X_{TCSC} is the net reactance of the TCSC at the fundamental frequency

X_{TCR} is the net reactance of the TCR at the fundamental frequency

X_C is the reactance of the TCSC's internal capacitor at the fundamental frequency

Referring to equation (2.3) it can be seen that as X_{TCR} is decreased the absolute value of X_{TCSC} will be increased. To illustrate this, two extreme cases will be taken when:

$X_{TCR} = \infty$ it can be seen that $|X_{TCSC}| = |X_C|$. The thyristors are not triggered and the TCR branch is open circuit. This is the condition for minimum series compensation. $X_{TCR} \approx X_C$ it can be seen that $|X_{TCSC}| = \infty$. The thyristors are being triggered. This is the condition of maximum series compensation and is also the point at which resonance between the inductor and capacitor occurs. However, practically this condition is never realised, for reasons that are explained later on in this section. The corresponding thyristor trigger angle at which resonance occurs is defined as α_{res}.

From the previous discussion it was shown that the minimum reactance of the TCSC is equal to the reactance of the fixed capacitor, therefore the TCSC can be thought of as an 'amplifier' that can, theoretically, boost the reactance of the physical capacitor by a factor of one to infinity. This leads to the definition of a term called the boost factor, K_B, which gives an indication of the 'amplification' of the reactance of the TCSC's internal capacitor.

$$K_B = \frac{X_{TCSC}}{X_C} \tag{2.4}$$

where

K_B is the boost factor of the TCSC at the fundamental frequency

X_{TCSC} is the net reactance of the TCSC at the fundamental frequency

X_C is the reactance of the TCSC's internal capacitor at the fundamental frequency

Equation (2.3) does not accurately predict the behaviour of the TCSC but was used to gain an insight into the operation of a TCSC. To understand the reason for the limitations of equation (2.3) the internal dynamics of the TCSC need to be discussed.

2.5 TCSC loop current – circuit analysis

To gain insight into how the change in the capacitive reactance of the TCSC occurs, the current and voltage dynamics internal to the TCSC require discussion. As stated previously, a decrease in the trigger angle of the thyristors results in an increase in the capacitive reactance of the TCSC, but exactly how this comes about will now be discussed.

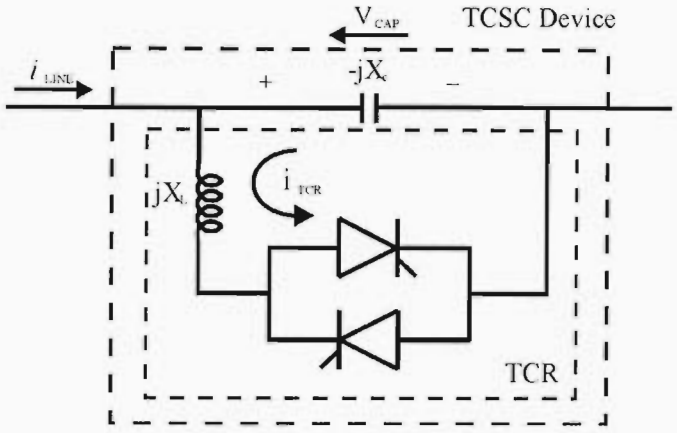

Figure 2.3: Single line diagram of a TCSC

Consider the single line diagram of a TCSC shown in Figure 2.3. If the forward biased thyristor is triggered just before the TCSC capacitor voltage is zero, then a small circulating current, I_{TCR} will flow in the TCR branch as shown in the figure. This circulating current adds to the transmission line current flowing through the capacitor, which results in an increase in the voltage, V_{CAP}, across the capacitor, and an increase in the capacitive reactance of the TCSC [Helbing1, IEE1, Matsuki2, Matsuki2, Yin1].

From the discussion above it can be seen that the voltage across the capacitor, and hence the voltage across the TCR, is not constant but is dependant on the trigger angle of the thyristors [Helbing1]. Therefore equation (2.3) does not accurately predict the behaviour of the TCSC since equation (2.1) was developed assuming that the TCR was connected across an ideal voltage source.

2.6 Mathematical model of a TCSC

Equation (2.1) was developed assuming the TCR was connected across an ideal voltage source. This is not the case with the TCSC as the TCR is now connected across a capacitor. During normal operation the TCR current adds to the transmission line current which causes an increase in the voltage of the capacitor and hence the capacitive reactance of the TCSC [Helbing1, IEE1].

The theoretical equation describing the boost factor K_B of a TCSC is shown by equation (2.5). Equation (2.5) was derived neglecting losses in the components of the TCSC and assuming that the TCSC is connected to an ideal current source [IEE1, Matsuki2].

$$K_B = 1 + \frac{2}{\pi}\frac{\lambda^2}{\lambda^2 - 1}\left[\frac{2\cos^2\beta}{\lambda^2 - 1}(\lambda \tan\lambda\beta - \tan\beta) - \beta - \frac{\sin 2\beta}{2}\right] \qquad (2.5)$$

where

$$\lambda = \sqrt{\left|\frac{X_C}{X_L}\right|}$$

X_C is the reactance of the TCSC's internal capacitor at the fundamental frequency

X_L is the reactance of the TCSC's internal inductor at the fundamental frequency

K_B is the boost factor of the TCSC at the fundamental frequency

β is the conduction angle of the thyristors in radians ($\beta = \pi - \alpha$)

α is the trigger angle of the thyristors in radians, measured from the zero crossing of the TCSC capacitor voltage, V_{CAP} shown in Figure 2.3.

The TCSC can operate in one of three modes, depending on the thyristor trigger angle, α. These modes are discussed below [IEE1]:

α = 180° - The thyristors are off and the conduction path of the current is only through the capacitor, therefore $X_{TCSC} = X_C$. The corresponding boost factor is 1. This is known as the blocking mode and is the case of minimum compensation.

α = 0° - The thyristors are continuously conducting and this allows current to flow through the inductor and through the capacitor. The capacitor and inductor are now in parallel. $X_{TCSC} = -|X_C // X_L|$. The corresponding boost factor is negative and the TCSC reactance is inductive. This mode is known as the bypass mode, and this mode of operation is used during fault conditions, when the transmission line current is high, to reduce the stress on the capacitor [IEE1].

$\alpha = [\alpha_{res}, 180°]$ - the physical reactance of the capacitor is increased. The reactance of the TCSC is capacitive and is dependent on the value of α. The boost factor, K_B, can vary in the range [∞ , 1]. This mode of operation is referred to as the capacitive boost mode. However, practically a boost factor of $K_B = \infty$ is not possible for reasons that

are explained later on in this section and this in turn limits the minimum allowable thyristor trigger angle, α to a value somewhat larger than α_{res} [Xu1].

The three modes of operation, and the full variable reactance characteristic of the TCSC is shown in Figure 2.3 which was plotted using equation (2.5). Table 2.1 shows the reactance values that were used for the TCSC's internal capacitor and TCR inductor in equation (2.5) which are the same as those used in the laboratory-scale TCSC studied later in the thesis.

Table 2.1. Reactances used in the TCSC

$X_L = j\ 0.8\ \Omega$	$X_C = -j\ 2.0\ \Omega$

2.7 Resonance

From Figure 2.4, it can be seen that the boost factor, K_B, increases to infinity in the capacitive boost region. Resonance occurs at the point when K_B is infinite and the thyristor trigger angle at which resonance occurs is defined as α_{res}. This happens because of a circulating current in the reactive elements, and is represented in equation (2.5) as the trigonometric function, tan $\lambda\beta$ [IEE1]. Solving for tan $\lambda\beta = \infty$ to obtain the trigger angle α_{res}, at which resonance occurs yields the equation (2.6).

$$\tan\lambda\beta = \infty$$

$$\Rightarrow \lambda\beta = \frac{\pi}{2} \quad \Rightarrow \beta = \frac{\pi}{2\lambda}$$

$$\text{since } \beta = \pi - \alpha \quad \text{and} \quad \lambda = \sqrt{\left|\frac{X_C}{X_L}\right|}$$

$$\pi - \alpha = \frac{\pi}{2\sqrt{\frac{X_C}{X_L}}}$$

$$\therefore \alpha_{res} = \pi - \frac{\pi}{2\sqrt{\frac{X_C}{X_L}}} \qquad (2.6)$$

where

α_{res} is the trigger angle at which resonance occurs

Equation (2.6) shows that the thyristor trigger angle at which resonance occurs is dependent on the reactance of the internal elements used in the TCSC. If the reactive components are not chosen judiciously there is a possibility that there can be more than one resonant point, which will reduce the useable capacitive reactance range of the TCSC.

Ideally the parameters of the reactive components used in the TCSC are chosen such that value of α_{res} is as small as possible so that a wider range of trigger angles is obtained [Helbing1], and also so that there is just one trigger angle at which resonance occurs [Christl1, Rigby1]. However it will be shown that the thyristor trigger angle at which resonance occurs is a secondary consideration when designing a TCSC.

For the laboratory-scale TCSC the thyristor trigger angle at which resonance occurs can be calculated using equation (2.6); substituting the values shown in Table 2.1 into equation (2.6) it was found that resonance occurs at $\alpha_{res} = 123.08°$. In theory this is the absolute minimum value of the thyristor trigger angle, α, for operation of the TCSC in the capacitive reactance region. It will be shown that the minimum value of α is limited even further due to practical considerations.

It must be noted that equation (2.5) and hence equation (2.6) were arrived at neglecting losses in the TCSC [IEE1]. In a practical implementation of a TCSC the inductor used in the TCR branch is non-ideal and will have a finite amount of resistance. It will be shown in later sections that the impact of the resistance of the TCR inductor has a significant effect on the performance of the TCSC in laboratory-scale implementations. One of the effects of the resistance of the TCR inductor is to reduce the thyristor trigger angle at which resonance occurs [Ghosh1].

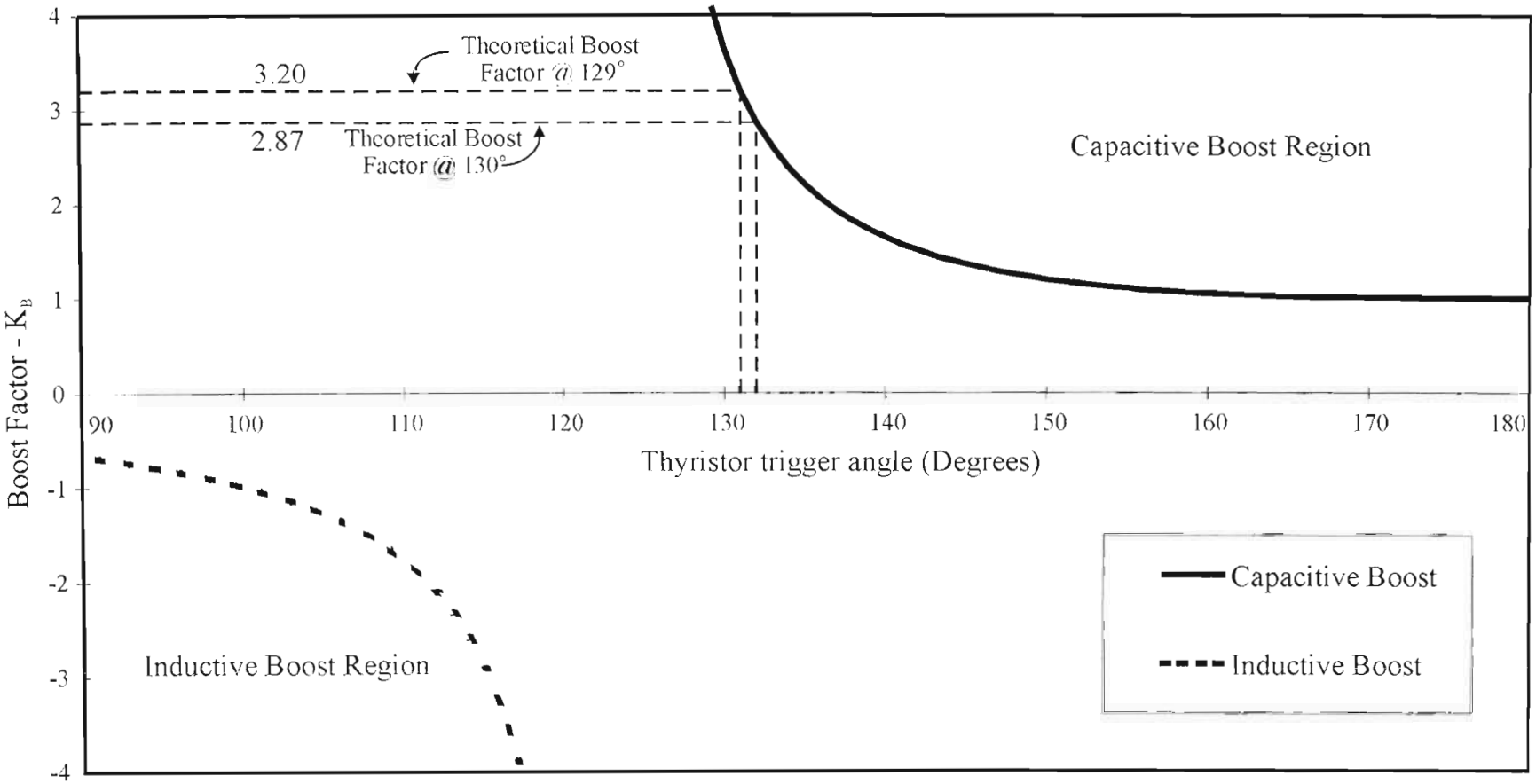

Figure 2.4:Graph showing the TCSC characteristic as a function of the trigger angle α as well as the sensitivity of the TCSC reactance to changes in the trigger angle.

2.8 Harmonics generated by the TCSC

In the capacitive boost mode of operation the thyristors in the TCSC will perform phase control, meaning that the thyristors will be partially conducting. The switching of the thyristors results in the flow of a non-sinusoidal TCR current which consists of odd harmonics of the fundamental, although only the lowest order harmonics are of interest [Larsen1, IEE1]. The third harmonic is the most dominant and increases with the decrease in thyristor trigger angle, which corresponds to higher levels of compensation [Helbing1, Matsuki2]. The effect of the harmonics results in the distortion of the voltage across the capacitor [Matsuki2, Xu1].

In practice TCSCs are typically installed in long high voltage transmission lines which have high impedance and high impedance loads connected to the ends of the transmission line. Therefore the harmonic current flow is restricted to circulate internally within the TCSC where the impedance is significantly lower than that of the transmission network [IEE1, Johnson1, Matsuki2, Xu1].

A review of the literature showed that there was no effect on the quality of the power due to the TCSC harmonics [Helbing1, Kinney1]. It was also concluded in [Matsuki2] that there is only a slight effect on the power system due to the harmonics generated by the TCSC. The effects of the harmonics can therefore be typically ignored in analysis [Xu1].

The first two known commercial implementations of a TCSC were the Western Area Power Administration TCSC, on the 230 kV Kayenta system in 1992, and the Bonneville Power Administration TCSC, on the 500kV Slatt system in 1993. For both of these TCSCs there was no need for the use of harmonic filters as the distortion was insufficient to necessitate the use of the filters [Kinney1, Larsen1].

2.9 Sensitivity of the TCSC reactance

One of the most important aspects in the implementation of a TCSC is the thyristor triggering controller. The controller must synchronise, calculate and generate the appropriate thyristor triggering signals to each of the thyristors. However the implementation of such a controller poses a number of technical challenges, foremost of which is the sensitivity of the reactance of the TCSC to changes in the thyristor trigger angle.

The sensitivity of the capacitive reactance of the TCSC is due to its highly non-linear capacitive reactance characteristic. The sensitivity of the capacitive reactance of the TCSC becomes more pronounced at lower thyristor trigger angles which correspond to higher levels of compensation. The significance of the sensitivity of the reactance of the TCSC is that the signal for the triggering of the thyristors has to be accurately and consistently generated by the controller.

If the controller does not generate the signal to trigger the thyristors accurately and consistently there will be a considerable error between the commanded level of compensation and that which is effectively being provided by the TCSC. Table 2.2 shows an example of the error that could arise due to the inaccuracy of the controller at lower values of α. Table 2.2 shows that at a nominal value of $\alpha = 130°$, a 1° change in the thyristor trigger angle, α, results in a 33% change in the boost factor, K_B, and hence of the TCSC's net capacitive reactance. The sensitivity of the TCSC's reactance to small changes in trigger angle is also illustrated graphically in Figure 2.4.

Table 2.2. Table showing sensitivity of TCSC to changes in the thyristor trigger angle

Boost factor of the TCSC (K_B) at a thyristor trigger angle (α) of 130°	2.87
Boost factor of the TCSC (K_B) at a thyristor trigger angle (α) of 129°	3.20
Percentage change in the boost factor of the TCSC ($\Delta K_B/K_B * 100$)	33%

The previous discussion dealt with the impact of any inaccuracy of the controller with regards to generating the thyristor triggering signal. This inaccuracy can be eliminated

with closed loop feedback control. The various closed loop strategies that have been proposed in literature will be discussed in the next section.

The second undesirable effect that could occur is due to inconsistencies or variations in the generation of the thyristor triggering signals. The problem with variations in the triggering signal generated to the thyristors is that the capacitive reactance of the TCSC will fluctuate from one mains cycle to the next causing the power transfer capability of the transmission line to change which could result in instability of the transmission network. A review of literature has shown that an error of less than 0.1° in the thyristor triggering signal is considered acceptable [Xu1].

An accurate and reliable controller is required to control the operation of a TCSC. This will ensure that the benefits that a TCSC is capable of providing are realised. It will be shown in later sections that the sensitivity or steepness of the TCSC reactance characteristic can be changed and is dependant on the parameters of the inductor used in the TCR.

2.10 Practical implementation and operation of a TCSC

The practical implementation and limits of operation of a TCSC differ from the theoretical operating limits. This is due to the ratings of the components used in the TCSC which are specified according to the intended application of the TCSC [Kinney1, Kosterev1, Mazibuko1]. A review of literature has shown that the boost factor of less than three is typically chosen [Kinney1, Kosterev1, Mazibuko1].

In theory the TCSC can provide an infinite amount of series compensation to a transmission line, however practically this is not possible. The maximum level of compensation that can be provided by the TCSC is limited by the voltage rating of the capacitor and the current rating of the inductor which are specified to meet the intended application of the TCSC [IEE1, Larsen1, Xu1].

A review of literature has shown that multi-module TCSCs (two or more TCSCs connected in series at the same site) provide a wider and smoother range of operation

[Larsen1] as compared to a single module TCSC. Multi-module TCSCs are much more economical and practical to operate [Larsen1], and many have been proposed and implemented [Gama1, Kinney1]. A further benefit of multi-module TCSC installations is that they can be operated in such a manner that does not produce harmonics [Larsen1].

Protection of a TCSC is achieved by using a metal-oxide varistor (MOV) which is used to prevent over-voltages across the fixed reactance capacitor. A bypass breaker is also installed across the TCSC to allow for the TCSC to be switched out of the circuit for maintenance or under fault conditions [Johnson1].

In commercial operation the TCSC can be used for any number of applications; these include: power oscillation damping, increasing the power transfer capability of a transmission line, limiting fault currents, subsynchronous resonance mitigation [Christl1, Gama1, Gama2, Helbing1, IEE1, Larsen1].

2.11 Synchronisation and Triggering Control of a TCSC

The reactance of the TCSC is controlled by back to back thyristors. The general requirement for the consistent and accurate control of a thyristor is to synchronise its triggering to the zero crossing of the sinusoidal AC voltage. The triggering resolution of these thyristors ultimately determines the accuracy with which the reactance of the TCSC can be controlled. This section discusses how the triggering of the thyristors is performed practically and discusses and the closed loop control schemes that have been proposed.

2.11.1 Method of synchronisation

The triggering of the thyristors in the TCSC needs to be referenced to the sinusoidal AC TCSC capacitor voltage. However, direct synchronisation to the TCSC capacitor voltage is unsuitable due to the harmonic distortion of the TCSC capacitor voltage under normal operating conditions [Matsuki2]. It has also been shown that such direct synchronisation is unsuitable under transient conditions [Yin1]. Instead it has been proposed [IEE1, Jalali1, Johnson1, Tan1] that the transmission line current be used for

synchronisation purposes. To accommodate for the 90° phase difference between the transmission line current and TCSC capacitor voltage, some manipulation is required.

One method of synchronisation is to perform zero crossing detection which relies on the detection of the zero crossing of the sinusoidal AC transmission line current waveform [Haro1]. However the shortcoming of this approach is that under transient conditions it becomes unreliable as the instantaneous angle of the TCSC capacitor voltage is only known at the zero crossings of the transmission line current. Furthermore any DC offset in the AC transmission line current will result in incorrect operation.

An alternative method of synchronisation is to make use of a digital phase locked loop [IEE1, Johnson1]. The phase locked loop allows for more reliable and consistent operation as it calculates the instantaneous angle of the transmission line current at every sampling interval of the controller, typically in the order of micro seconds. The theory of operation of a phase locked loop is beyond the scope of this dissertation; however a brief overview is contained in Appendix A.

2.11.2 Practical implementation of the PLL

The inputs to the phase locked loop are the instantaneous three phase transmission line currents to which synchronisation is required. In this case the Phase A and Phase C transmission line currents are used. The output of the phase locked loop is the instantaneous angle of the Phase A transmission line current. From the instantaneous angle of the Phase A transmission line current, assuming a balanced system, the instantaneous angle of the Phase B and Phase C transmission line currents can be determined. The simplified block diagram in Figure 2.5 shows the implementation of the phase locked loop. A detailed discussion of the implementation of the phase locked loop and controller appears in Chapter Four.

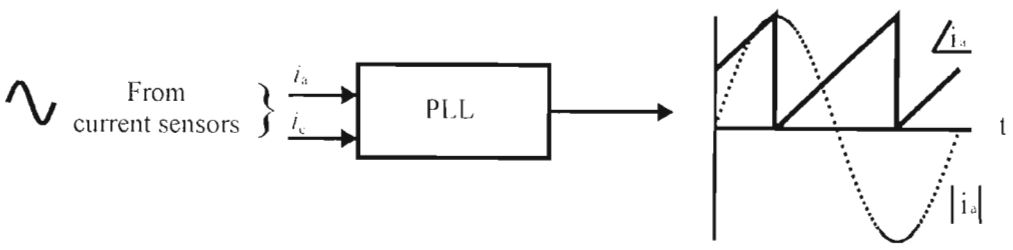

Figure 2.5: Simplified block diagram showing the inputs and output of the PLL algorithm

2.11.3 Closed loop control schemes

For open loop control of the TCSC impedance, the thyristor trigger angle is set externally and the controller generates the appropriate triggering signal to the thyristors. The trigger angle is chosen depending on the level of compensation required. Alternatively, the level of compensation is set externally and the controller determines the appropriate trigger angle from a look up table or a best fit function.

Numerous low level closed loop control strategies have been proposed to implement a triggering controller for the TCSC. One of the advantages of a closed loop control system is to speed up the slow response time of the TCSC [IEE1, Jalali1, Jalali2, Tan1]. The slow response time of the TCSC is due to the effect of the TCR branch and the capacitor [Jalali2] in the TCSC.

The closed loop control strategies that have been proposed are closed loop current control, conduction angle feedback and impedance feedback [Yin1, IEE1]. The feedback signals required for the implementation of these control strategies are the TCSC capacitor voltage and transmission line current for impedance control, and the TCR current for conduction angle feedback control. An advantage of using the TCSC capacitor voltage as a feedback signal is that possible over-voltage conditions of the TCSC can also be avoided [IEE1] by monitoring the TCSC capacitor voltage.

Further advantages of closed loop control of the TCSC include the ability to negate the effects of the non linear properties of the TCSC [IEE1], and to reduce the dependency of response on the operating point [Jalali1]. It was also proposed [Yin1] that the transmission line current of each phase be used as a feedback signal and a trigger angle be generated for each phase to minimize the effects of the dissimilar parameters of components used in the construction of the TCSC.

2.12 Conclusion

A TCSC consists of a fixed-reactance capacitor connected in parallel with a thyristor controlled reactor (TCR). The TCSC effectively boosts the capacitive reactance of its internal capacitor by a controllable amount. This is a result of a circulating current flowing in the TCR branch which boosts the voltage across the capacitor, causing a boost in the capacitive reactance of the TCSC.

It was shown that the capacitive reactance characteristic of the TCSC is a highly non-linear function of the thyristor trigger angle. Theoretically the capacitive reactance of the TCSC increases as the thyristor trigger angle is decreased up to a point where resonance occurs. However in practice this point of operation is avoided.

Under normal operating conditions there are harmonics generated within the TCSC. This is due to the switching of the thyristors which results in the flow of a non-sinusoidal TCR current. However a review of the literature has shown that the harmonics are confined to the low impedance path internal to the TCSC and do not flow into the high impedance transmission line.

It was shown that the capacitive reactance of the TCSC is sensitive to variations in the thyristor trigger angle. The consequence of this is that the controller that is generating the triggering signals to the thyristors needs to generate these signals accurately and consistently. If this is not done then there will be undesirable errors and fluctuations in the capacitive reactance provided by the TCSC.

An overview of the thyristor triggering controller that is used to control the operation of the TCSC was discussed. A review of literature showed the best manner in which to implement such a controller, and proposed a number of closed loop control schemes in an attempt to minimise the effects of the sensitivity of the TCSC.

Chapter Three presents results which were obtained from experimental measurements and a detailed simulation model of the TCSC and its triggering controls. The simulation model parameters were based on the existing laboratory-scale TCSC and

took into account the non-ideal characteristics of the actual components used in this TCSC.

Chapter Three

Detailed simulation model of the laboratory scale TCSC and its triggering controls

3.1 Introduction

Chapter Two discussed the theoretical operation of a thyristor controlled series capacitor (TCSC). The theory provided insight into the operation of the TCSC and a theoretical mathematical model was used to predict its behaviour. However much of the theoretical modelling used to predict the behaviour of the TCSC was simplified and was based on ideal conditions. In practice this is not the case as the components used in the TCSC display non-ideal characteristics.

This chapter details the development of a simulation model that is capable of modelling the non-ideal properties of the components used in the laboratory-scale TCSC. The simulation and modelling of the laboratory scale TCSC was carried out using PSCAD [Manitoba1]. The simulation model allowed for the modelling of the laboratory-scale TCSC and the thyristor triggering controller in detail. The simulation model was initially developed with ideal components and was tested against the theoretical expectation of the laboratory-scale TCSC's variable capacitive reactance characteristic.

When the ideal simulation model was proven, it was then extended to include all of the non-ideal properties of the components actually used in the laboratory-scale TCSC. As far as practicable, all aspects of the laboratory TCSC were included in the simulation model. This culminated in a simulation model that accurately predicted the true behaviour of the laboratory-scale TCSC. The simulation model was based on the parameters of the laboratory-scale TCSC which is discussed in the next section.

3.2 Laboratory-scale TCSC

A three phase laboratory-scale TCSC was constructed for research purposes in the Machines Research Laboratory at the University of KwaZulu-Natal [Pillay1]. This laboratory-scale TCSC was based on, and extended, the earlier work in [Mazibuko2]. The TCSC was designed to operate using the existing equipment in the research laboratory, specifically the artificial transmission line simulator. The operating voltage for the test circuit shown in Figure 3.1 was chosen to be 28 V_{phase} (0.22 pu). This was to ensure that the current handling capabilities, 7.87 A (1 pu), of the laboratory equipment were not exceeded. (Note that the transmission line in the Machines Research Laboratory is actually rated at 220 V_{L-L} (1 pu); in these studies, the 28 V (0.22 pu) phase voltage used represents the *difference* between the sending and receiving end voltages at either end of the transmission line.) The operating voltage was set with the aid of a variac which was connected to an infinite bus. The transmission line inductive reactance was chosen to be 10 Ω and the resistance was measured to be 1.6 Ω.

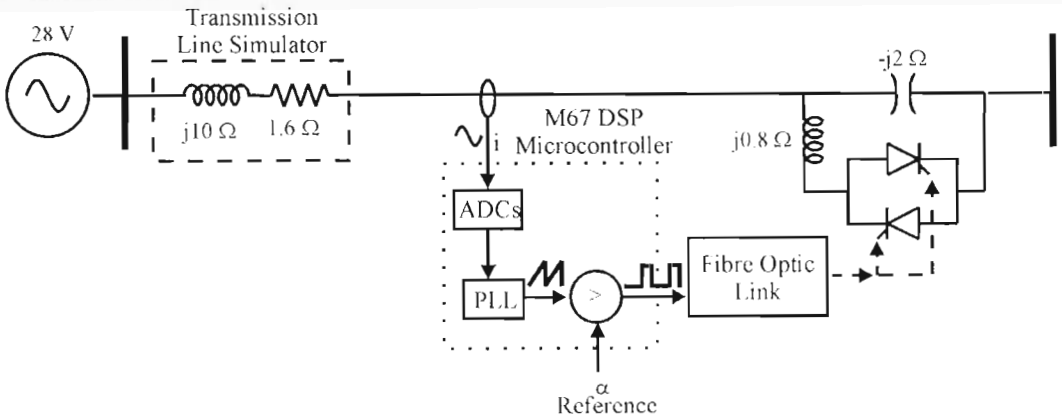

Figure 3.1: Simplified single line diagram of the laboratory-scale TCSC and its triggering controls

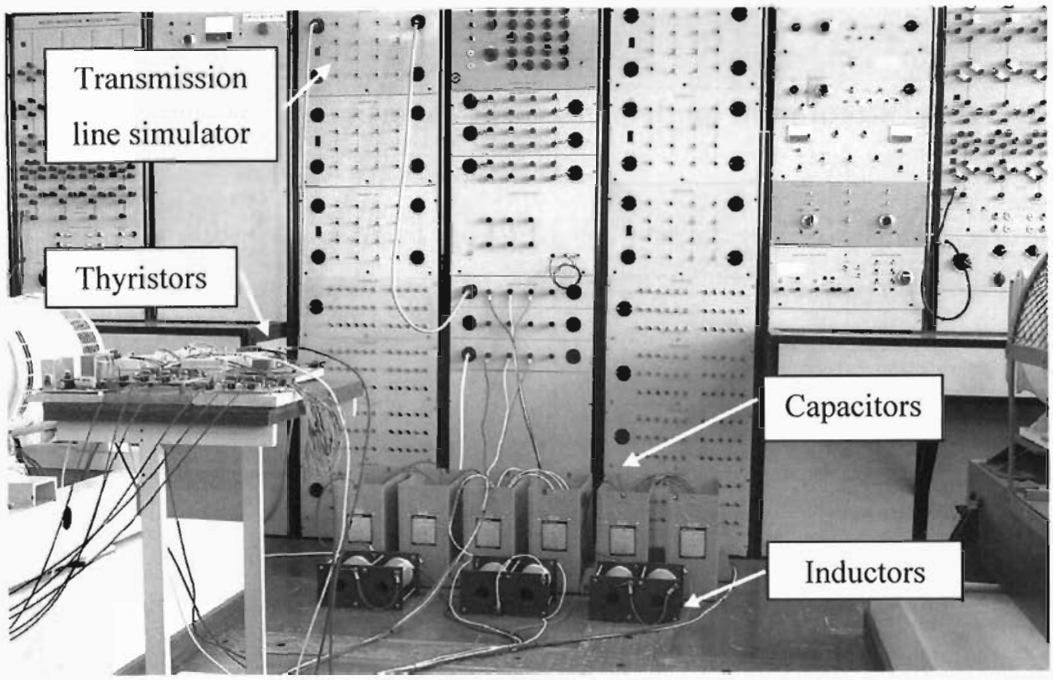

Figure 3.2: Photograph of the laboratory-scale TCSC used in the experiments

The circuit was terminated in a short circuit to ensure maximum current flow during compensated and uncompensated conditions. The phase locked loop (PLL) algorithm, used to synchronise the triggering of the thyristors, required the instantaneous values of the Phase A and Phase C transmission line currents. Hall Effect current transducers were used to provide the required isolation for the measurement of the transmission line currents used by the controller. A detailed discussion of the implementation of the controller appears in the next chapter.

The simplified laboratory-scale TCSC shown in Figure 3.1 was used to obtain practical measurements. The time domain waveforms, of transmission line current, TCSC capacitor voltage, and TCR current pulses of the laboratory-scale TCSC were captured using a data acquisition system. From the waveforms of the transmission line current and the TCSC capacitor voltage the capacitive reactance characteristic of the laboratory-scale TCSC was obtained for a range of values of trigger angle, α. A Fourier transform was used to obtain the fundamental components of the TCSC capacitor voltage and line current and from these the capacitive reactance characteristic of the laboratory-scale TCSC was calculated at each value of α. A similar FFT-based method was employed in the PSCAD simulation model to obtain

the capacitive reactance characteristic of the simulated laboratory-scale TCSC as a function of trigger angle.

3.3 Ideal simulation model versus the theoretical expectation

The first step in developing the simulation model of the laboratory-scale TCSC was to model the laboratory-scale TCSC as having ideal components. This will allow for the simulation model to be tested against the theoretical expectation of the laboratory-scale TCSC's capacitive reactance characteristic. It will also prove that the simulation model is capable of being used as a tool to predict the behaviour of the laboratory-scale TCSC.

The simulation model was developed to include the triggering controls of the laboratory-scale TCSC. A time step of 25 μs was deliberately chosen for the simulation model in order to be the same as the sampling period of the actual TCSC's controller, and this helped to model the discrete nature of the controller. The actual PLL algorithm used to synchronise the triggering of the thyristors was also included in the simulation model. A comparator was used to determine when to generate the signal to trigger the appropriate thyristor. The test circuit parameters used in the simulation model of the laboratory-scale TCSC is shown in Figure 3.1.

The simulated capacitive reactance characteristic of the ideal laboratory-scale TCSC was calculated from the fundamental components of the TCSC capacitor voltage and transmission line current, which were obtained using a Fast Fourier transform (FFT) of the waveforms. The resulting capacitive reactance characteristic of the laboratory-scale TCSC obtained from the simulation model is shown in Figure 3.3. The theoretical capacitive reactance characteristic obtained from equation (2.5) is also plotted in Figure 3.3.

It can be seen that there is close agreement between the results obtained from the PSCAD simulation model and the theoretical equation. It was noted that there was a small deviation between the simulated and theoretical capacitive reactance characteristics for the laboratory-scale TCSC at lower thyristor trigger angles. However the evaluation of the simulation model as a tool to predict the behaviour of

the laboratory-scale TCSC continued. The simulation model was then extended to include the non-ideal properties of the components used in the laboratory-scale TCSC.

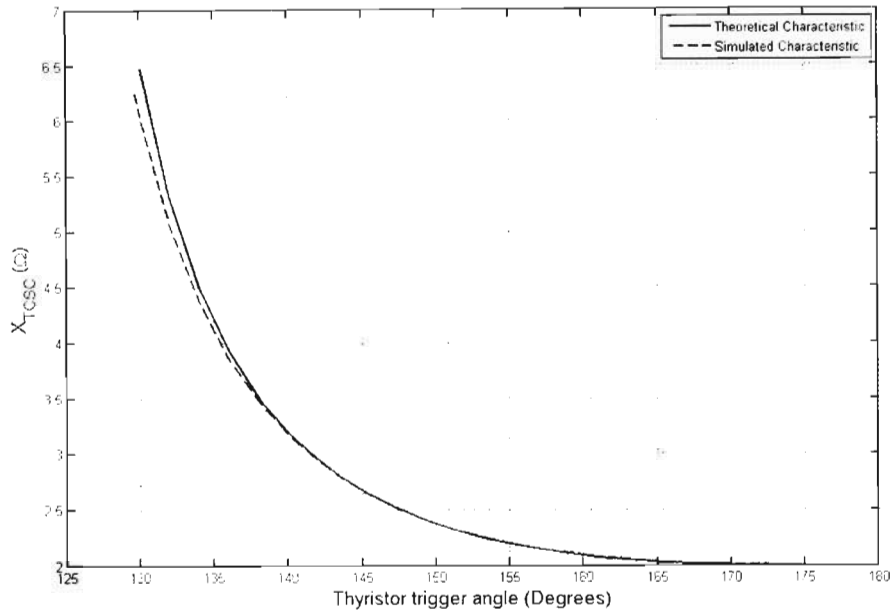

Figure 3.3: Theoretical and simulated capacitive reactance characteristic of the ideal laboratory-scale TCSC

3.4 The effects of the non–ideal components on the performance of the laboratory-scale TCSC

The theoretical equation, equation (2.5), describing the reactance characteristic of the TCSC was developed assuming ideal conditions [IEE1]. A review of literature has shown that there are deviations between the theoretical expectation of the capacitive reactance characteristic and the practical capacitive reactance characteristic of a TCSC. This is due to the resistance of the TCR inductor [Ghosh1, Haro1, Matsuki1] and the forward volt drop of the thyristors. However the forward volt drop of the thyristors is a concern in low voltage TCSCs and will not have a significant effect in high voltage applications [Pillay1].

The individual effects on the performance of the laboratory-scale TCSC, caused by the non-ideal components used, will be investigated in this section. This will be

achieved by extending the simulation model to include the non-ideal properties of the components used in the TCSC and finally analysing the combined effect of all the identified non-ideal properties of the components used in the laboratory-scale TCSC. At this point the capacitive reactance characteristic of the laboratory-scale TCSC which was calculated and obtained from experimental measurements is compared to the capacitive reactance characteristic of that obtained from the simulation model of the laboratory-scale TCSC.

3.4.1 Modelling of the TCSC triggering controller

The TCSC thyristor triggering controller was modelled in detail using PSCAD. The PSCAD simulation time step was initially chosen to be the same as the sampling period of the digital controller used in the laboratory TCSC in order to replicate the effect of the discrete nature of these hardware controls. A comparator was used to determine when to trigger the thyristors in the simulation model, based on the commanded angle and the instantaneous angle of the TCSC capacitor voltage.

The effect of the triggering controller's sampling period on the variable reactance characteristic of the TCSC was then investigated by conducting three separate simulation studies. The time step of the first simulation study was chosen to be 25 μs, which corresponded to the sampling period of the initial prototype of the digital thyristor triggering controller for the laboratory TCSC. The time step for the second simulation study was chosen to be 5 μs, which corresponded to the effective sampling period of the controller that would be required to meet the requirements for a 0.1° trigger angle resolution as proposed in the literature [Xu1].

For purposes of comparison a third simulation study was conducted. The third simulation study was used to obtain an "ideal" set of simulated results based on the laboratory-scale TCSC parameters, but with the effect of the triggering controller's sampling period on the performance of the TCSC removed. This was achieved by making use of an interpolated thyristor firing block within PSCAD. This interpolated firing block closely replicates the behaviour of an ideal analogue comparator in the TCSC's triggering controls, despite the fact that the PSCAD model is only solved at discrete time intervals [Manitoba1].

The effect of the digital controller's sampling period on the performance of the laboratory-scale TCSC was investigated by obtaining the capacitive reactance characteristic of the laboratory-scale TCSC for all three cases. Figure 3.4 shows the variable capacitive reactance characteristics obtained from the three simulation studies.

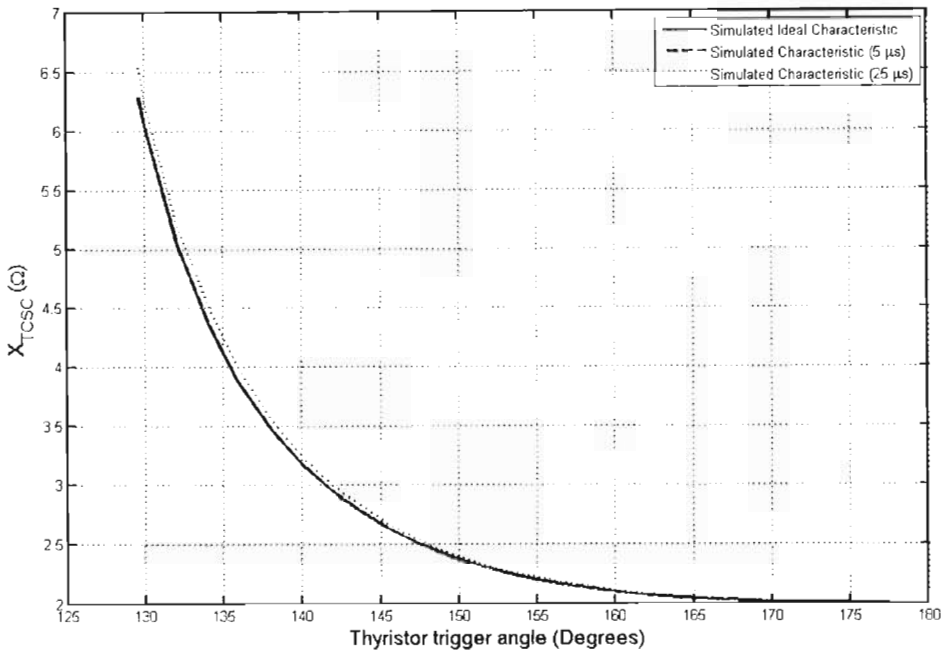

Figure 3.4: Capacitive reactance characteristic of the laboratory scale TCSC for different digital triggering controller sampling periods in the simulation model

From Figure 3.4 it can be seen that the discrete nature of the digital triggering controller has an effect on the performance of the laboratory-scale TCSC. The figure shows that for a sampling interval of 25µs, the capacitive reactance characteristic obtained deviates slightly from the capacitive reactance characteristic obtained from the ideal simulation model. The figure also shows that the performance of the laboratory-scale TCSC improves when the sampling interval is reduced to 5µs, as there is closer agreement to the capacitive reactance characteristic obtained from the ideal simulation model.

It was shown that the time step of the simulation model and hence the sampling period of the laboratory-scale TCSC triggering controller had an effect on the performance of the laboratory-scale TCSC. It was seen that the effect of the sampling period of the TCSC triggering controller on the performance of the TCSC can be minimised by

reducing the sampling period of the controller. Therefore one of the design criteria for the TCSC triggering controller will be to minimise the sampling period of the digital TCSC triggering controller as far as possible.

3.4.2 Modelling of the snubber circuit

The laboratory-scale TCSC makes use of RC snubber circuits connected across the back-to-back thyristors. The RC snubber circuits are used to limit the rate of voltage rise (dV/dt) across the thyristors that occurs when the thyristor, feeding an inductive load, switches off. Without such snubbers, an excessively high rate of voltage rise at turn off of the thyristors (higher than the thyristor's voltage rise rating of 100 V/μs [IRF1]) could incorrectly cause them to turn on. The reason for also including the snubber circuit in the simulation model was to accurately represent the laboratory-scale TCSC and to investigate the effect of the snubber circuit on the performance of the TCSC reactance characteristic.

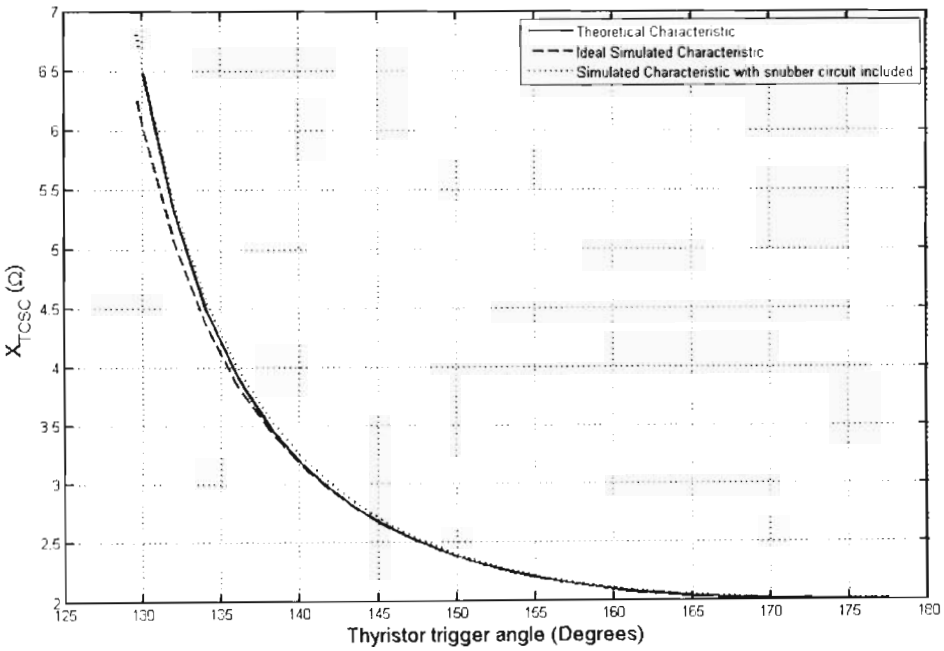

Figure 3.5: Capacitive reactance characteristic of the laboratory scale TCSC: Ideal and with the snubber circuit represented in the simulation model.

Figure 3.5 shows that effect of including the snubber circuit in the simulation model is to improve the agreement between the simulated and theoretical capacitive reactance characteristics of the laboratory-scale TCSC therefore further investigation into in the effect of the snubber circuit on the performance of the TCSC was not warranted.

3.4.3 Modelling of the thyristor forward volt drop

One of the non-ideal properties of the components used in the laboratory-scale TCSC that was identified is the forward volt drop of the thyristors. The forward volt drop of the actual thyristors used in the laboratory scale TCSC was obtained from the technical datasheet [IRF1] and was found to be 1.7 V. A forward volt drop of 1.7 V was then included in the characteristics of each thyristor in the detailed PSCAD simulation model.

The effect of the forward volt drop of the thyristors on the capacitive reactance characteristic of the laboratory scale TCSC was then analysed. Figure 3.6 shows the theoretical expectation of the capacitive reactance characteristic and the capacitive reactance characteristic of the laboratory-scale TCSC obtained with the forward thyristor volt drop represented in the simulation model.

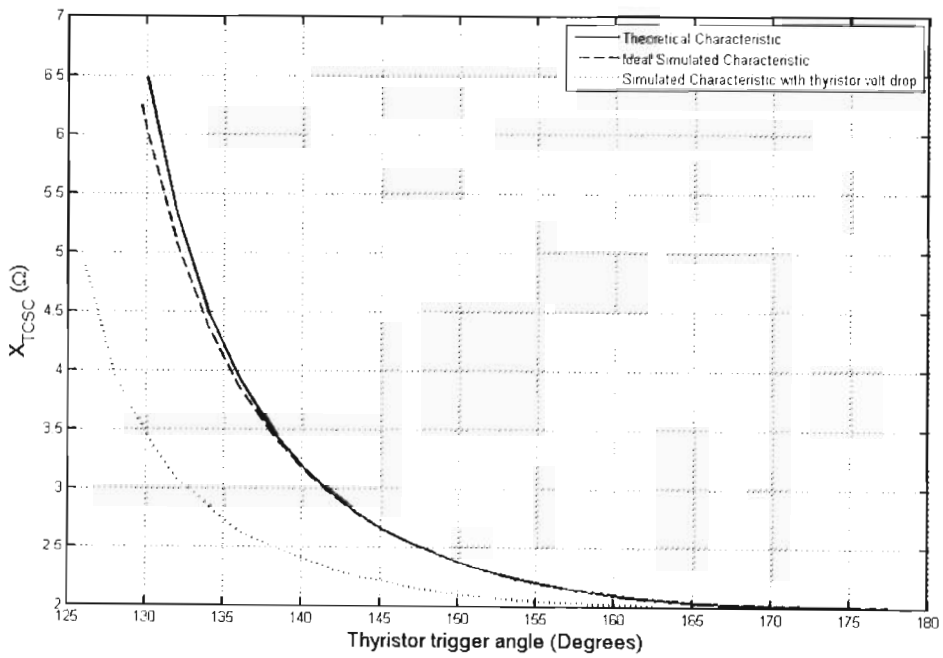

Figure 3.6: Capacitive reactance characteristic of the laboratory scale TCSC: Ideal and with forward thyristor volt drop represented in the simulation model.

Figure 3.6 shows that although the basic shape of the TCSC's reactance characteristic is preserved, the effect of the forward volt drop of the thyristors is to shift the TCSC's characteristic curve significantly to the left; in other words for a given thyristor trigger angle the capacitive reactance of the laboratory-scale TCSC is lower than the

theoretical expectation when the forward volt drop of the thyristors are taken into account. The time domain waveforms of the laboratory TCSC were analysed to investigate the reason for this deviation.

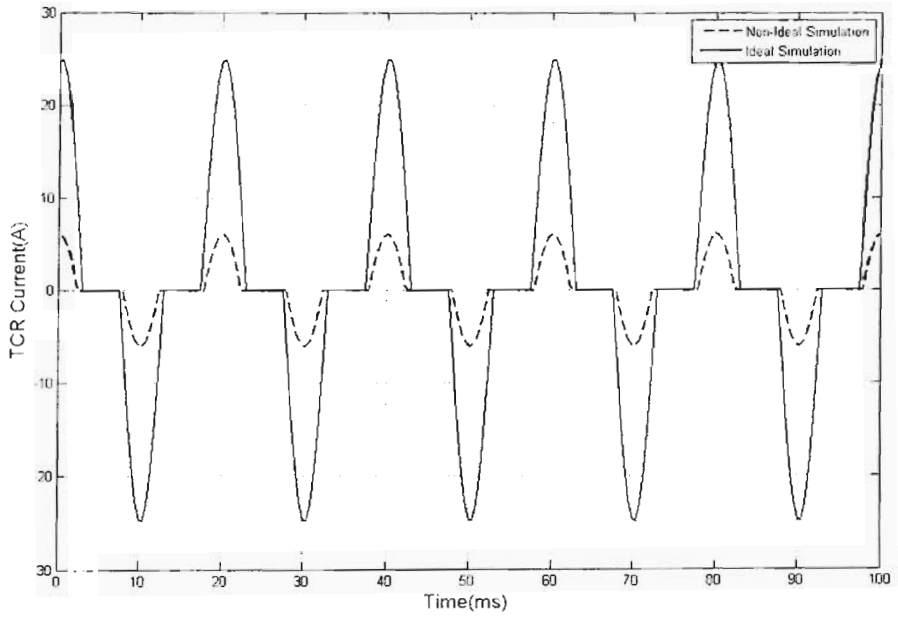

Figure 3.7:Time domain waveform of the TCR current for the laboratory-scale TCSC with the forward volt drop of the thyristors represented in the simulation model.

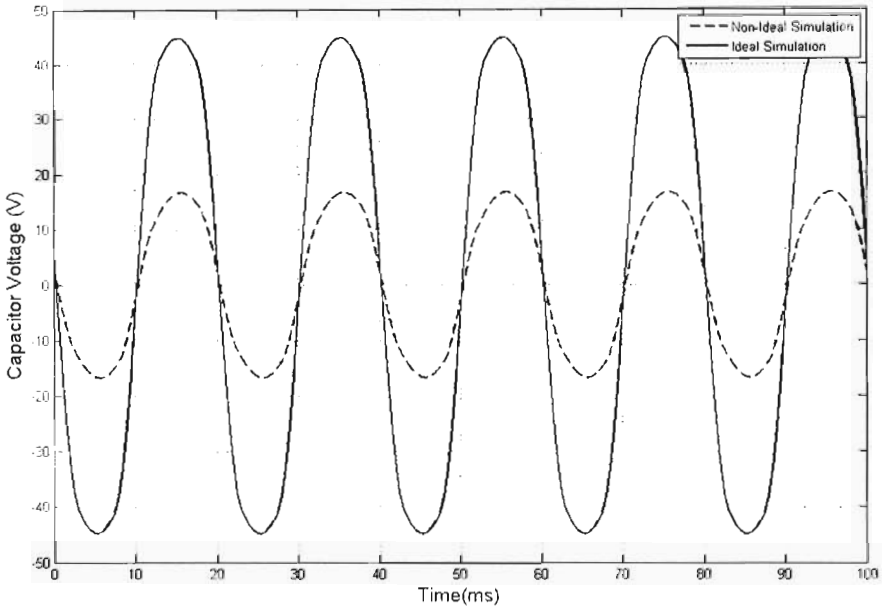

Figure 3.8: Time domain waveform of the TCSC capacitor voltage for the laboratory-scale TCSC with the forward volt drop of the thyristors represented in the simulation model.

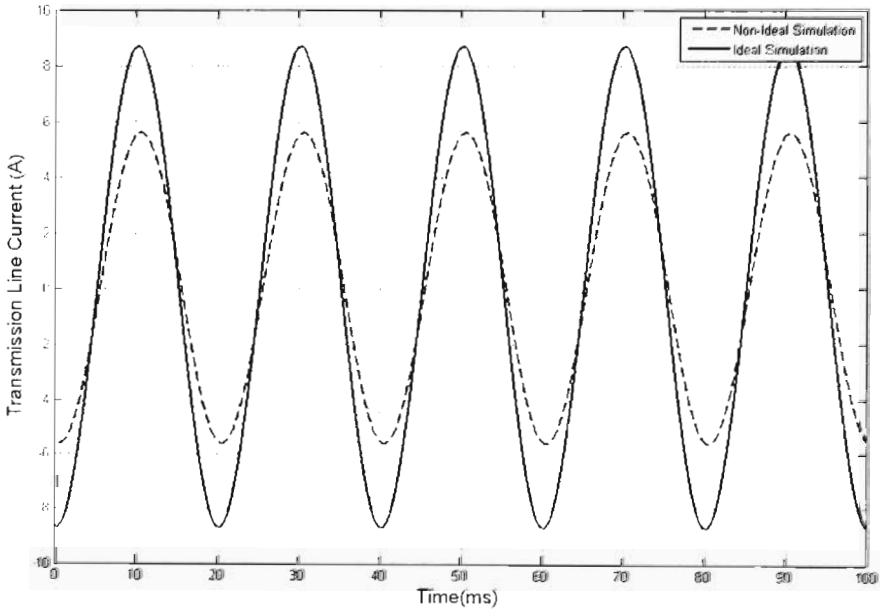

Figure 3.9: Time domain waveform of the transmission line current for the laboratory-scale TCSC with the forward volt drop of the thyristors represented in the simulation model.

Figure 3.7 shows the TCR current pulses obtained from the simulation studies of the laboratory-scale TCSC when the forward volt drop of the thyristors are taken into account in the simulation model. Figure 3.7 shows that the TCR current pulses are asymmetrical about their peaks and the magnitude of the TCR current pulses is markedly lower when the forward volt drop of the thyristors are taken into account.

The reason for this is that there is a lower effective voltage available to drive the current in the TCR branch when the volt drop across the thyristors is represented. This causes a lower "boost" voltage across the capacitor, shown in Figure 3.8, as a result of the TCR current flow, which in-turn results in a lower than expected theoretical capacitive reactance of the laboratory-scale TCSC at a given thyristor trigger angle. Finally the lower than expected capacitive reactance of the laboratory-scale TCSC results in a lesser amount of series compensation which in-turn results in a lower transmission line current flow, as shown in Figure 3.9. In the case of a low voltage laboratory-scale TCSC, the small volt drop across the thyristors is unfortunately not negligible relative to the voltage across the TCSC capacitor, as it would be in a large installation.

3.4.4 Modelling of the TCR inductor resistance

The inductors used in the TCR branch of the laboratory TCSC are of the air core type having copper windings. Measurements of the parameters of the inductors showed that there was a finite non-negligible resistance associated with the inductor. A review of the literature has shown that the impact of this resistance on the performance of the TCSC is significant and therefore needs to be taken into account [Ghosh1, Haro1, Matsuki1].

The resistance of the TCR inductors were modelled by inserting an external resistor into the TCR branch in the PSCAD simulation model. The resistance of the TCR inductors used in the laboratory-scale TCSC were measured and these values were used to parameterise the simulation model. The measured resistance of the final inductor combination, used in the PSCAD simulation, was found to be 0.29 Ω.

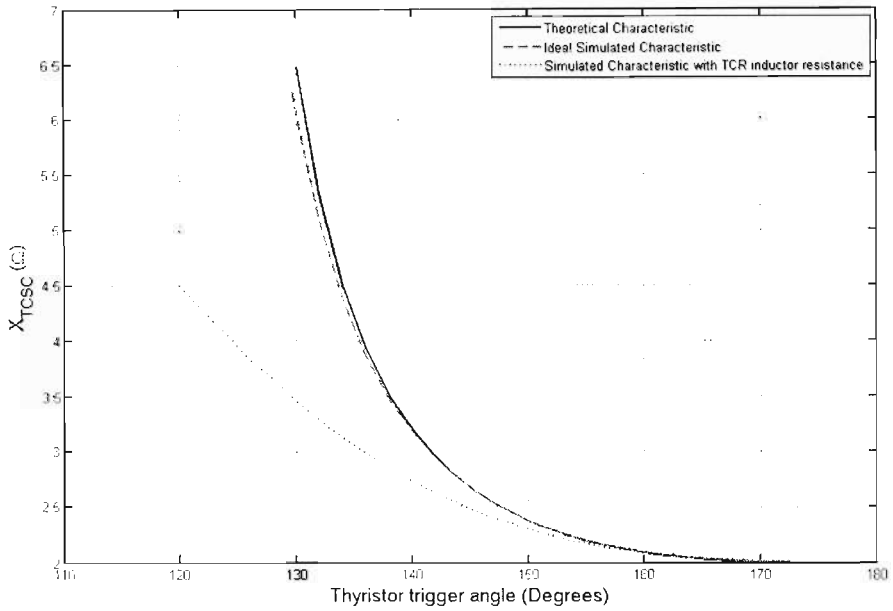

Figure 3.10: Capacitive reactance characteristic of the laboratory scale TCSC: Ideal and with TCR inductor resistance represented in the simulation model.

Figure 3.10 shows that the effect of resistance in the TCR inductor is to decrease the steepness of the laboratory-scale TCSC's reactance characteristic. This effectively means that for a given thyristor trigger angle the capacitive reactance of the laboratory-scale TCSC is lower than the theoretical expectation when the resistance of the TCR inductors are taken into account.

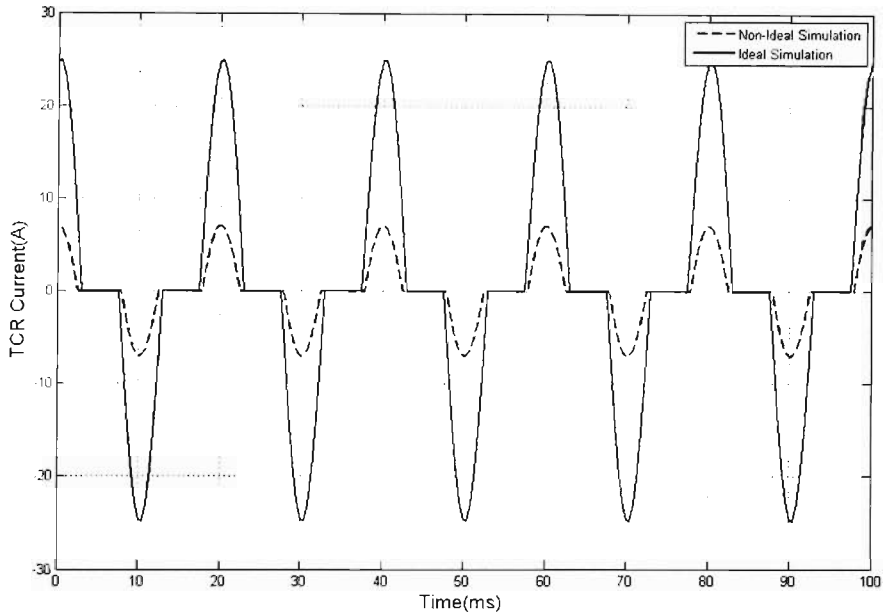

Figure 3.11: Time domain simulation waveform of the TCR current for the laboratory-scale TCSC with the TCR inductor resistance represented in the simulation model

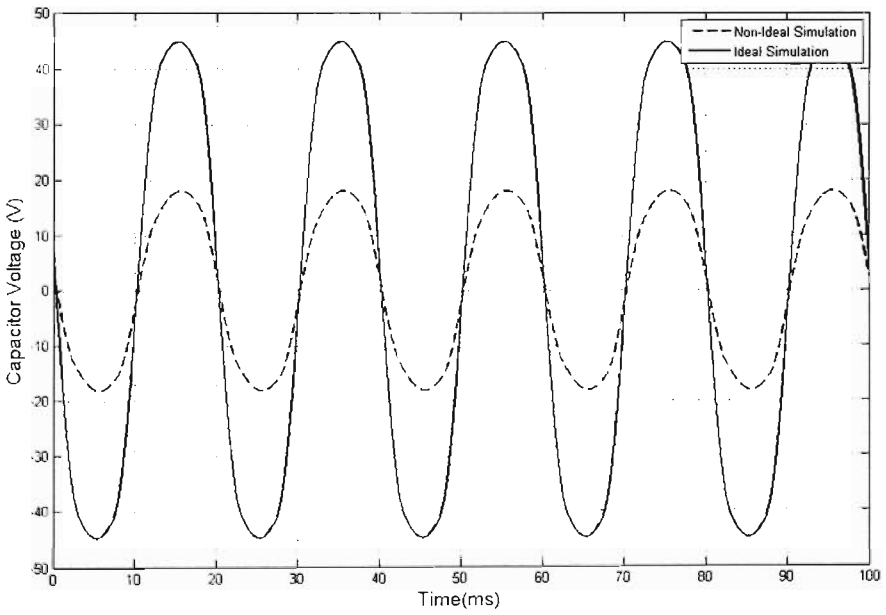

Figure 3.12: Time domain simulation waveform of the TCSC capacitor voltage for the laboratory-scale TCSC with the TCR inductor resistance represented in the simulation model

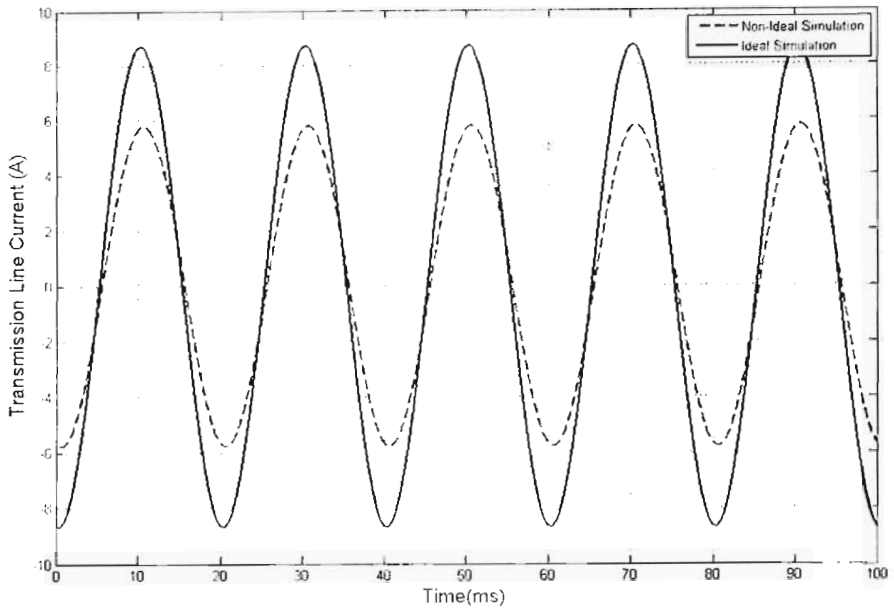

Figure 3.13: Time domain simulation waveform of the transmission line current for the laboratory-scale TCSC with the TCR inductor resistance represented in the simulation model

The time domain analysis of the TCR current pulses, shown in Figure 3.11, and TCSC capacitor voltage waveform, shown in Figure 3.12, obtained from the detailed PSCAD model revealed the reason for the capacitive reactance of the laboratory-scale TCSC being lower than the theoretical expectation at a given thyristor trigger angle. Figure 3.11 shows that the effect of the inductor resistance on the TCR current pulses is to reduce the magnitude of these pulses. From the loop current analysis in Section 2.5, it was shown that the circulating current of the TCR boosts the voltage across the capacitor which results in an increase in the capacitive reactance of the TCSC.

It can be seen from Figure 3.11 that since the effect of the inductor resistance is to reduce the magnitude of the TCR current pulse it ultimately results in the reduction of the capacitive reactance of the laboratory-scale TCSC, which in-turn results in a lower transmission line current, shown in Figure 3.13, due to the lower amount of series compensation provided by the laboratory-scale TCSC. A more detailed analysis and discussion of the effects of the TCR inductor parameters on the performance of the laboratory-scale TCSC will be presented in Chapter Six.

3.4.5 Combined effect of non-ideal TCSC parameters

Finally all the non-ideal properties of the laboratory-scale TCSC were included collectively in the simulation model, namely the sampling period of the controller, the forward volt drop of the thyristors and the resistance of the TCR inductors. The TCSC capacitive reactance characteristic obtained using this detailed simulation model was compared to that obtained from actual experimental measurements performed on the laboratory-scale TCSC (using the test circuit shown in Figure 3.1). The results of these comparisons are shown in Figure 3.14.

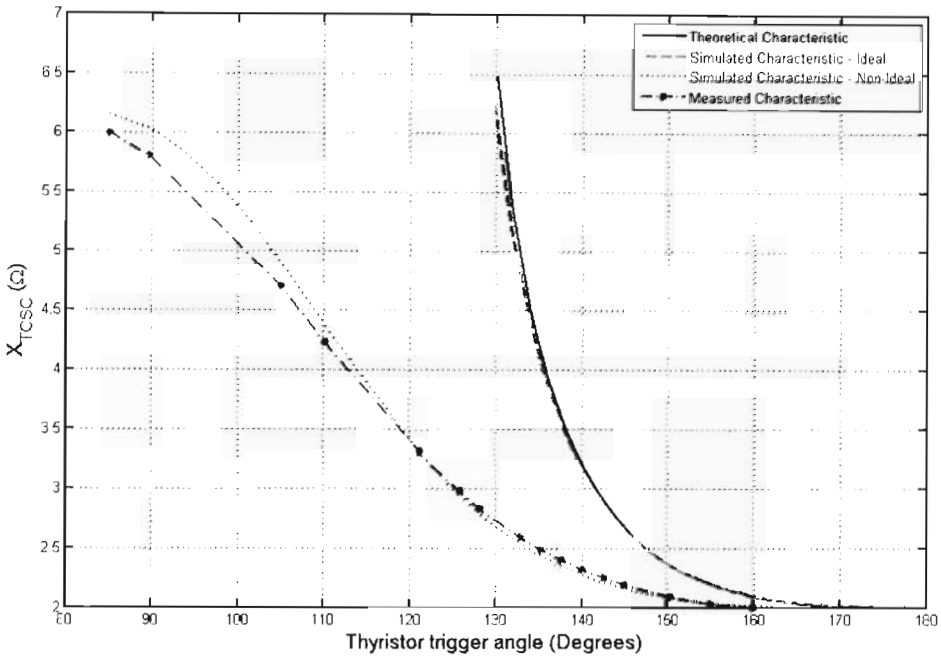

Figure 3.14: Plot of the capacitive reactance characteristic of the laboratory-scale TCSC showing the results obtained from practical measurements and simulation studies that include the TCSC's non-ideal component characteristics

The capacitive reactance characteristic obtained from the simulation model that took into account the non-ideal properties of the components used in the laboratory-scale TCSC showed close agreement with the capacitive reactance characteristic of the laboratory-scale TCSC that was obtained from practical measurements. However, both the simulated and the measured capacitive reactance characteristics of the non-ideal laboratory-scale TCSC showed significant deviation from the theoretical capacitive reactance characteristic of the laboratory-scale TCSC obtained from equation (2.5).

The results in Figure 3.14 confirm that the non-ideal properties of the components used in the laboratory-scale TCSC have a significant effect on its performance. The results also show that these non-ideal properties (the sampling period of the controller, the forward volt drop of the thyristors and the resistance of the TCR inductor) can be incorporated into a more detailed simulation model, which can be used to predict the true behaviour of a laboratory-scale TCSC. To provide further proof of the validity of the simulation model, the time domain waveforms obtained from the experimental measurements on the laboratory TCSC were compared with the time domain waveforms obtained from the simulation study with all the non-ideal effects included. Figure 3.15 shows a comparison of the measured and simulated TCR currents.

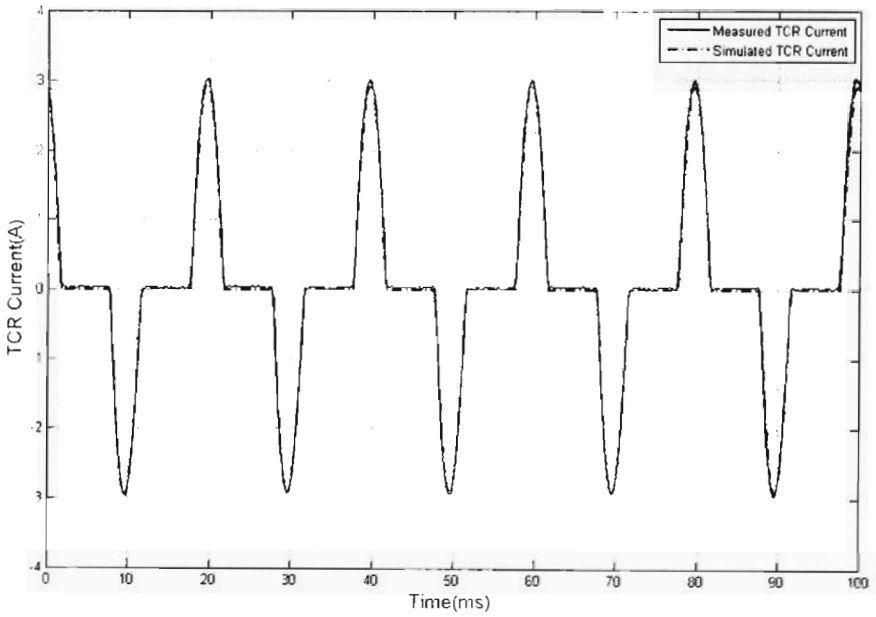

Figure 3.15: Time domain waveform of the laboratory-scale TCSC's TCR currents obtained from simulation studies and practical measurements: all non-ideal properties represented.

Any discrepancies in the TCR current will result in discrepancies in the TCSC capacitor voltage and the transmission line current. However Figure 3.15 shows that there is close agreement between the TCR current pulses obtained from simulation and experimental measurements. The magnitude and duration of the simulated and measured TCR current pulses are now almost exactly the same once the non-ideal characteristics of the TCSC's components are included in the simulation model. The

asymmetry of the TCR current pulses is now also evident in both the simulated and measured results.

The effect of the TCR current pulses is to boost the voltage across the TCSC capacitor from which the capacitive reactance of the laboratory-scale TCSC is calculated. Therefore the next time domain waveform to be analysed was the TCSC capacitor voltage.

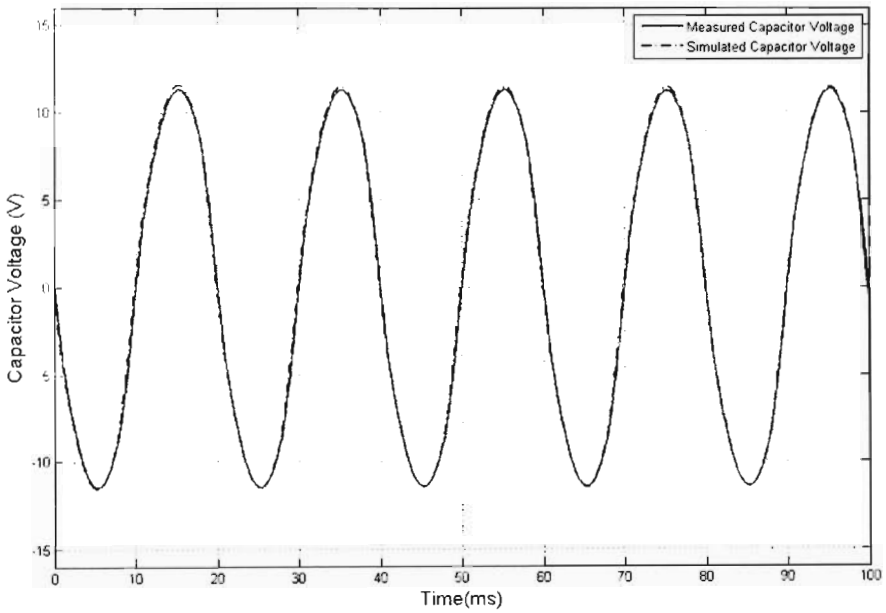

Figure 3.16: Time domain waveform of the laboratory-scale TCSC capacitor voltage obtained from simulation studies and practical measurements: all non-ideal properties represented.

Figure 3.16 compares the TCSC capacitor voltage obtained from simulation and experimental measurements. It can be seen that there is close agreement between the two waveforms. Finally the time domain waveforms of the transmission line current were analysed.

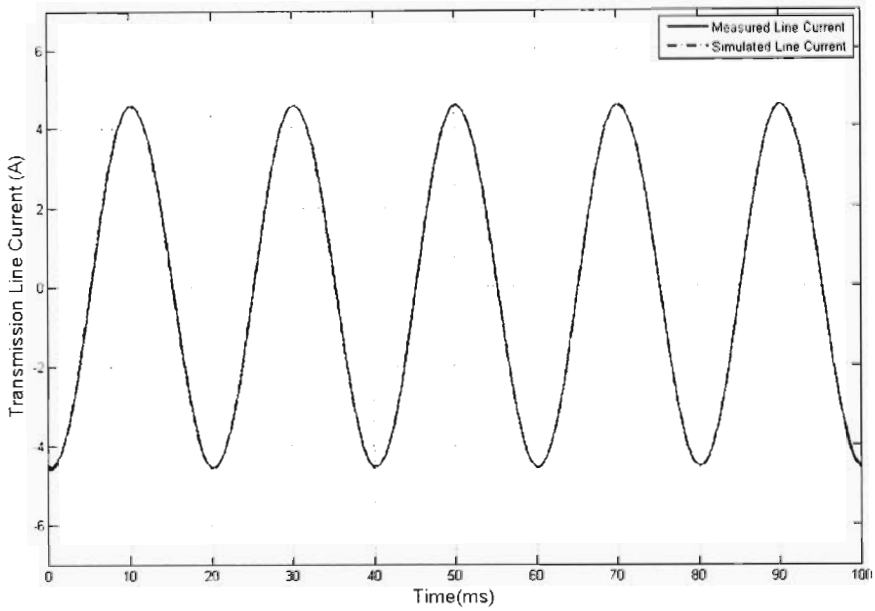

Figure 3.17: Time domain waveform of the laboratory-scale TCSC transmission line current obtained from simulation studies and practical measurements: all non-ideal properties represented.

Figure 3.17 shows the time domain waveforms of the transmission line current obtained from simulation and experimental measurements identical. Figure 3.17 also confirms that overall, the actual hardware laboratory-scale TCSC is providing the exactly the same amount of series compensation as compared to the simulated laboratory-scale TCSC at the given thyristor trigger angle due to the equal current magnitudes of the transmission line current obtained from experimental measurements and simulation.

The time domain waveforms of the three key laboratory-scale TCSC variables obtained from simulation studies and experimental measurements were analysed for a range of thyristor trigger angles and in all instances it was observed that there was close agreement between the simulated and measured time domain results. This verified the accuracy of the simulation model in predicting the behaviour of the laboratory-scale TCSC. The simulation model can therefore also be used as a tool to assist in designing a laboratory-scale TCSC with better parameters so as to obtain a variable reactance characteristic that more closely resembles high power TCSCs used in actual transmission applications.

3.5 Conclusion

The non ideal properties of the components used in a laboratory-scale TCSC have been identified and their effects on the performance of the TCSC have been investigated. It was seen that the effect of the snubber circuit did not have a significant effect on the performance of the TCSC.

The effect of the forward volt drop of the thyristors was to reduce the capacitive reactance of the laboratory-scale TCSC for a given thyristor trigger angle. The effect of inductor resistance was to reduce the steepness of the laboratory-scale TCSC's variable reactance characteristic. Both of these phenomena were explained with the aid of the time domain waveforms obtained from the detailed simulation model. It was seen that the magnitude of the TCR current pulses was lower which effectively resulted in a lower capacitive reactance of the laboratory-scale TCSC.

Finally, when the simulation model was extended to include all non-ideal effects it was tested against measured results obtained from experiments conducted on the laboratory-scale TCSC. The results showed close agreement. The time domain results from which the capacitive reactance characteristic of the TCSC are derived were also compared. There was also close agreement observed which proved that the simulation model can be used to predict the behaviour of the laboratory-scale TCSC.

Chapter Four now describes the development of an improved digital triggering control scheme for the laboratory-scale TCSC to obtain the 0.1° trigger angle resolution required in practice.

Chapter Four

M67 DSP-based prototype TCSC triggering controller

4.1 Introduction

Chapter Three discussed the performance of the prototype laboratory-scale TCSC. The most important finding was that the performance of the laboratory-scale TCSC differs significantly from the theoretical expectation. This was shown to be due to the non-ideal properties of the components used in the laboratory-scale TCSC, namely the forward volt drop of the thyristors, the resistance of the TCR inductor and the sampling period of the controller.

A simulation model was developed to include the non-ideal properties of the laboratory-scale TCSC. The simulation model was tested against experimental measurements and was found to accurately predict the behaviour of the laboratory-scale TCSC. The experimental results were obtained using a prototype digital TCSC triggering controller.

This chapter discusses this prototype digital TCSC triggering controller that was successfully developed for use in the Machines Research Laboratory at the University of KwaZulu-Natal [Pillay1]. This controller made use of a digital phase locked loop (PLL) in order to synchronise the triggering of the thyristors to the transmission line current. However the performance of this controller regarding the resolution of the thyristor trigger angle was found to be inadequate. This chapter describes the implementation of the controller and discusses its limitations.

4.2 Implementation of the laboratory-scale TCSC triggering controller

The capacitive reactance of the TCSC is a function of the thyristor trigger angle. The thyristor trigger angle is measured from the zero crossing of the TCSC capacitor voltage, therefore the first requirement of a TCSC thyristor triggering controller is that it must be capable of synchronising the triggering of the thyristors to the TCSC capacitor voltage. This effectively means that the phase locked loop (PLL) algorithm, which is used to synchronise the triggering of the thyristors to the TCSC capacitor voltage, is the most important aspect in the implementation of the laboratory-scale TCSC thyristor triggering controller.

The second requirement is that the controller must be capable of generating the appropriate signal to the thyristors based on high level inputs, examples of which can be the thyristor trigger angle or the level of compensation required from the TCSC. A simplified block diagram of the TCSC triggering controller is shown in Figure 4.1, below.

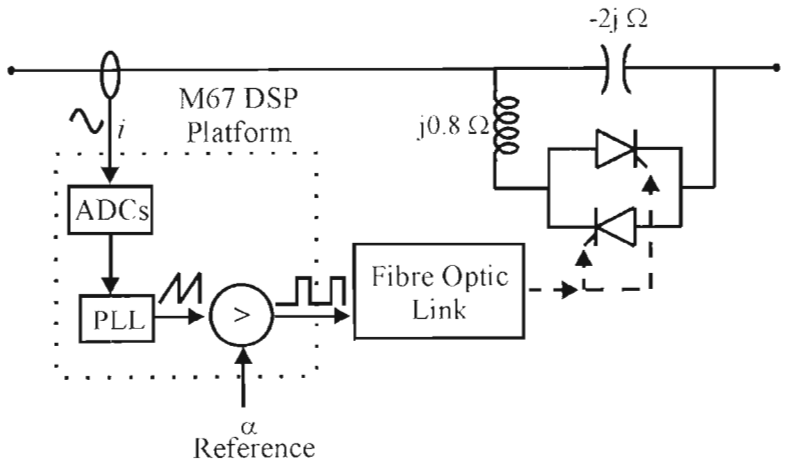

Figure 4.1: Simplified diagram of the TCSC triggering controller

The figure above shows a simplified diagram of the implementation of the TCSC triggering controller. The diagram illustrates that the entire PLL synchronisation and triggering control is carried out on an M67 digital signal processor (DSP) development board [Innovative1]. LEM current transducers are used to measure the transmission line currents, and also provide galvanic isolation between the power

circuit and the M67 DSP. The output of the current transducers are signal level voltages proportional to the transmission line currents; these voltages are sampled by analogue-to-digital converters (ADCs) onboard the M67 DSP platform.

The phase locked loop algorithm requires instantaneous magnitudes of the Phase A and Phase C transmission line currents and the output of the PLL algorithm is the instantaneous angle of the Phase A TCSC capacitor voltage. The instantaneous angles of the Phase B and Phase C TCSC capacitor voltage can be calculated from the instantaneous angle of the Phase A TCSC capacitor voltage, assuming a balanced system.

The instantaneous angles of the Phase A, B and C TCSC capacitor voltages are then compared, on board the M67 DSP platform, to the commanded TCSC trigger angle α in order to generate logic level triggering pulses for each thyristor in the TCSC. These triggering pulses are output to a fibre optic link via a digital output port on the M67 DSP board. The fibre optic link feeds an interfacing circuit used to provide the drive characteristics needed to electrically trigger each thyristor, as well as galvanic isolation.

4.3 M67 DSP Hardware

The Texas Instruments M67 DSP controller was used to implement the prototype digital TCSC controller. The M67 DSP operates at a clock frequency of 166 MHz and was programmed using the C programming language. The M67 processor is a 32 bit floating point DSP that is capable of accurately carrying out the necessary computations for the PLL algorithm. Furthermore the M67 features mono-rail ADCs that are required for the sampling of the transmission line currents. This effectively makes the M67 well suited to implement the PLL algorithm.

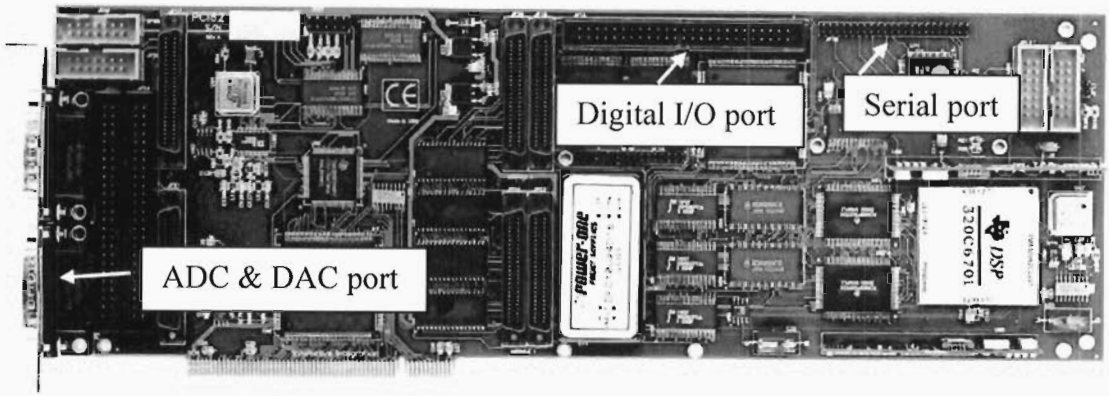

Figure 4.2: Photograph of the M67 DSP platform [Signalogic1]

The shortcoming of the M67 is that while it is flexible and computationally powerful, it is not able to operate at sufficiently high speeds required for the implementation of a high resolution triggering controller for a TCSC. Specifically, it is not possible to implement the PLL algorithm using floating point mathematics on board the M67 DSP in sufficiently short time periods to allow for the very small sampling intervals required to achieve 0.1° thyristor trigger angle resolution. The effect of a low sampling period on the performance of the laboratory-scale TCSC was investigated. It showed that a low sampling period resulted in inaccuracy in the generation of the triggering signal to the thyristors. This ultimately caused undesirable variations in the transmission line current which could lead to instability of the transmission system.

To interface with external equipment, the M67 DSP thyristor triggering controller makes use of two groups of peripherals. The analogue-to-digital converters (ADCs) are used to sample the transmission line currents and the digital input/output port is used to obtain the commanded thyristor trigger angle (input) and generate the thyristor triggering signals (outputs). In addition, an onboard timer was used to provide the accurate and consistent sampling events to clock the PLL and triggering pulse algorithm implemented on the M67 DSP.

4.3.1 Analogue-to-digital converters

The two analogue signals representing the instantaneous Phase A and C transmission line currents are sampled using two 16-bit analogue-to-digital converters (ADCs). The ADCs were triggered by an on-board timer operating at a frequency of 40 kHz. This sampling frequency was arrived at by measuring the time taken by the M67 DSP to

execute one compete iteration of the software program which included the 5μs overhead on the ADCs from the time they are triggered until the data is available. Therefore the sampling frequency was dependant on the time to execute the software and the limitations of the ADCs.

4.3.2 Digital port

The other input to the M67 DSP thyristor triggering controller is the reference signal representing the commanded thyristor trigger angle. The input was in the form of an 8-bit digital signal that is generated using eight DIP switches, although the input would come from a high-level FACTS controller in an actual application. The commanded thyristor trigger angle is calculated from this 8-bit digital value. The option of using a digital input was chosen as it requires minimal processing time. It also allows for the commanded thyristor trigger angle to be accurately set, which is beneficial when comparing simulated and measured results for a specific thyristor trigger angle.

The three output signals that are generated by the M67 DSP thyristor triggering controller are the triggering pulses to the thyristors. The three signals are split by the thyristor drive circuit to generate the pulses required to trigger the six thyristors in the laboratory-scale TCSC. The reason for using the digital port to generate the thyristor triggering signals was due to its high speed operation.

4.3.3 Timer

Finally an onboard timer was used to trigger the ADCs, which effectively controlled the sampling frequency of the thyristor triggering controller, and hence the angular resolution at which the thyristors can be triggered. The maximum obtainable sampling frequency or timer frequency was obtained by measuring the time that the M67 DSP actually takes to execute the PLL and triggering control algorithm in software. This ensured that there was no overrun or overlap of the software and no over-clocking of the ADCs.

4.4 M67 DSP Software

The M67 DSP was programmed using the C programming language. The software was used to configure and initialise the M67 DSP hardware, namely the timer, the ADCs, and the digital input/output port. The majority of the software was for the implementation of the phase locked loop (PLL) algorithm. The software program can be divided into two main components, the synchronisation stage which consists of the PLL algorithm, and the comparator stage which determines if a thyristor is to be triggered. This section discusses these stages starting with the synchronisation stage.

4.4.1 Synchronising stage: Phase Locked Loop (PLL) algorithm

A review of literature [IEE1, Jalali1, Johnson1, Matsuki2, Tan1, Yin1] has shown that the best manner in which to synchronise the triggering of the thyristors to the TCSC capacitor voltage is to make use of a PLL algorithm that uses the transmission line currents as its inputs. The reason for this is that the TCSC capacitor voltage becomes distorted due to harmonics under normal operating conditions making it unsuitable to be used for synchronisation purposes. The simplified block diagram below shows the algorithm of the PLL that was implemented.

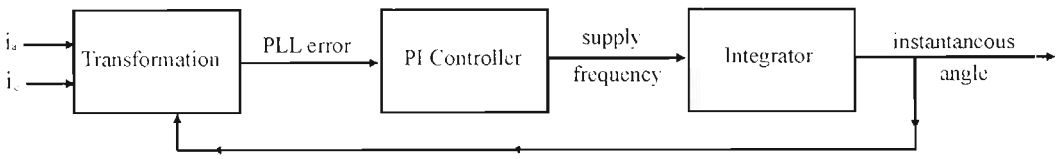

Figure 4.3: Simplified block diagram of the PLL algorithm

The output of the PLL algorithm that was implemented on the M67 DSP triggering controller is the instantaneous angle of the Phase A TCSC capacitor voltage. The PLL algorithm works by transforming the instantaneous Phase A and Phase C transmission line currents into the two-axis coordinates of a space vector. The PLL algorithm then locks the phase of a rotating coordinate frame to this space vector. The instantaneous angle of this coordinate frame, synchronised to the transmission line current space vector, is then used to determine the instantaneous angle of phase A of the TCSC capacitor voltage. A detailed explanation of the theory of the PLL appears in Appendix A along with the transformation equations used in the implementation of the PLL algorithm.

The output from the PLL algorithm was the instantaneous angle of the Phase A TCSC capacitor voltage. To obtain the instantaneous angle of the Phase B and Phase C TCSC capacitor voltages it was assumed that the system was balanced. For a balanced system the voltages are angularly spaced by 120°, therefore the instantaneous angle of the Phase B TCSC capacitor voltage was obtained by adding 120° to the instantaneous angle of the Phase A TCSC capacitor voltage and the instantaneous angle of the Phase C TCSC capacitor voltage was obtained by subtracting 120° from the instantaneous angle of the Phase A TCSC capacitor voltage.

4.4.2 Comparator stage

The output from the phase locked loop (PLL) is the instantaneous angle of the Phase A TCSC capacitor voltage from which the instantaneous angle of the Phase B and Phase C TCSC capacitor voltages are obtained. To determine if a thyristor in any phase of the TCSC needs to be triggered, a comparison is done between the instantaneous angle of the TCSC voltage in that phase and the commanded reference thyristor trigger angle. This comparison is done for all three phases in every sampling interval.

The drawback of this approach is that the thyristors can only be triggered at the end of a sampling period. This means that the sampling period determines the resolution at which the thyristors can be triggered, which is ultimately determined by the time taken to execute the software and interface with peripherals.

The comparator stage is the point in the software where a simple comparison is done between the instantaneous angles calculated and the commanded reference thyristor trigger angle. Depending on the outcome of this comparison a signal is generated via the digital port to trigger the appropriate thyristor. If the thyristor is to be triggered a digital logic high value (1) is written to the appropriate pin in the digital port. Figure 4.4 shows a block diagram of the implementation of the M67 DSP thyristor triggering controller that was developed for the laboratory-scale TCSC.

4.4.3 External control interface circuitry

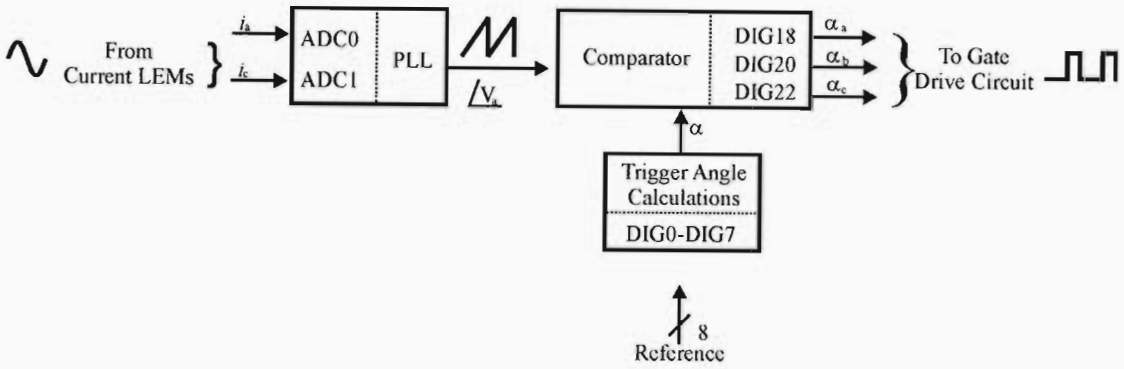

Figure 4.4: Block diagram of the M67 thyristor triggering controller

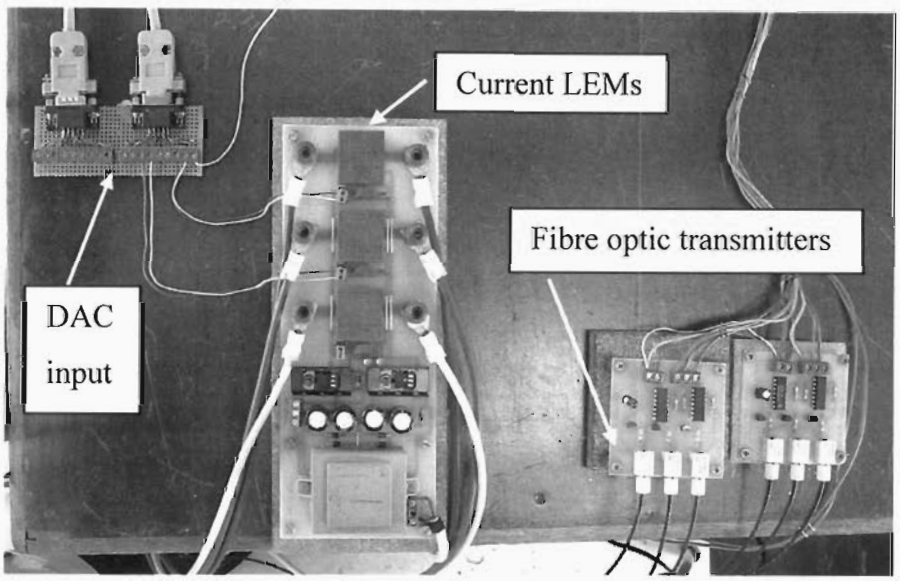

Figure 4.5:Photograph showing the input circuitry to the M67 thyristor triggering controller

Figure 4.4 shows a block diagram of the M67 thyristor triggering controller. It is a simplified flow diagram of the software and the peripherals that are used. The magnitudes of the Phase A and Phase C transmission line currents are sampled by the ADC channel 0 and ADC channel 1 respectively. The 8-bit digital reference signal is connected to pins 0 to 7 and the thyristor triggering signals for Phase A, B and C are connected to pins 18, 20 and 22 respectively. The thyristor triggering signal is connected to the thyristor gate drive circuit shown in Figure 4.6.

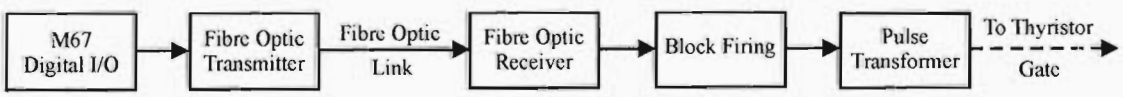

Figure 4.6: Block diagram of the thyristor drive circuit

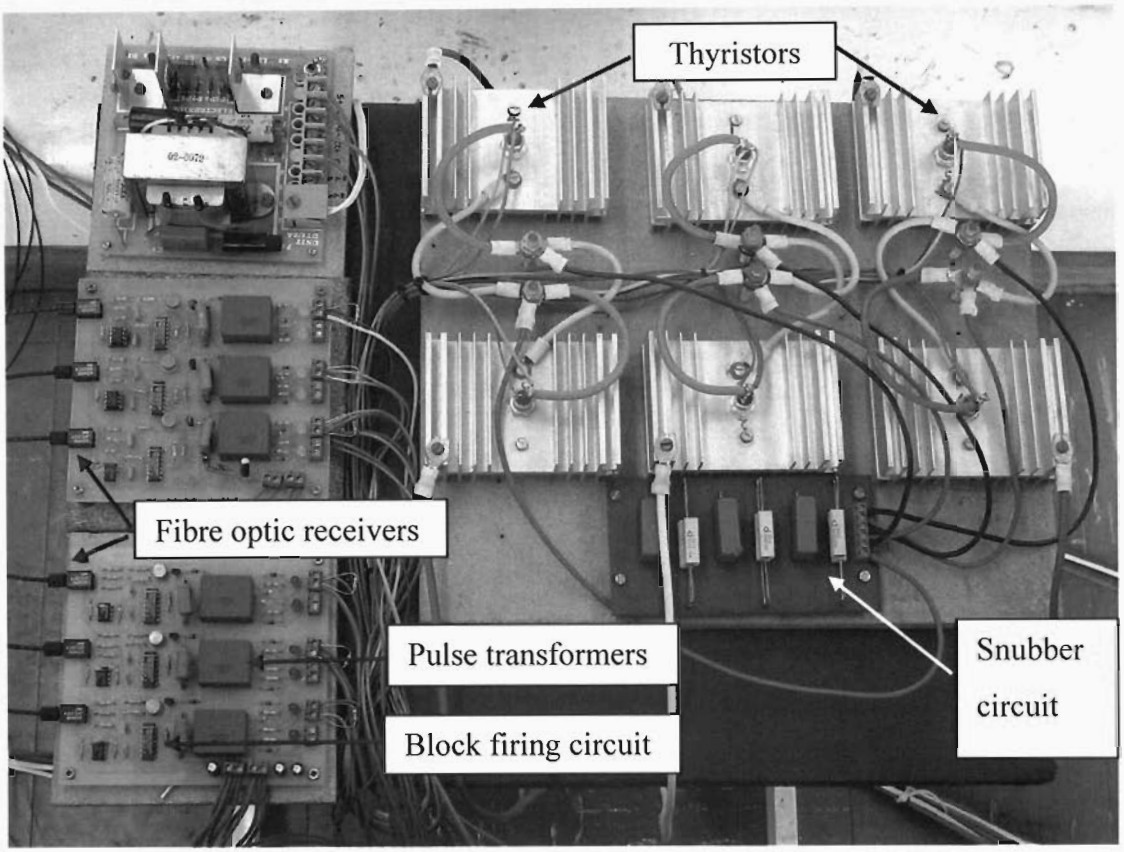

Figure 4.7: Photograph showing the external thyristor triggering circuit

Figure 4.6 shows a simplified block diagram of one channel of the thyristor drive circuit. The digital thyristor triggering signal is connected to a fibre optic transmitter which provides a means to transmit the triggering pulse to the thyristor and also minimises the signal power requirements on the M67 DSP.

The output from the fibre optic cable is connected to a receiver which converts the signal back into a digital electrical signal. A block firing stage is incorporated into the circuit to provide a high frequency digital thyristor triggering signal. The final stage is a pulse transformer which allows the transmission of the high frequency thyristor triggering signal. The pulse transformer also provides isolation between the power circuit and the thyristor drive circuit.

4.5 Performance of the M67 DSP controller

In Section 2.9 it was shown that the thyristor triggering controller has a significant effect on the performance on the TCSC. Inaccuracy of the controller can result in instability of the power system, due to the sensitivity of the TCSC to small variations in the thyristor trigger angle. It was shown that the effects of the variation in thyristor trigger angle become more pronounced at lower thyristor trigger angles where the levels of capacitive reactance compensation are higher.

The resolution at which the M67 DSP controller can control the thyristor trigger angle was found to be 0.45°. This value was obtained by measuring the variation of the instance in time of the front edge of the thyristor trigger pulse for a constant commanded triggering angle as well as by measuring the execution time of the software algorithm on the M67 DSP. It was found that the most time was taken to read the ADCs and to perform the trigonometric calculations used by the coordinate transformations in the PLL algorithm.

A review of the literature has shown that the thyristor trigger angle resolution must be less than 0.1° for satisfactory control of the TCSC, therefore it was undertaken to develop an improved controller that is capable of controlling the thyristor trigger angle at resolutions of 0.1° or better. Chapter Six presents details of the implementation of this controller.

4.6 Conclusion

A prototype digital thyristor triggering controller was developed to control the triggering of the thyristors of the laboratory-scale TCSC. The controller was developed using the Texas Instruments M67 DSP. Although the M67 DSP is capable of performing accurate calculations, it lacks sufficient processing speed to execute the complex PLL algorithm at small enough sampling intervals for high resolution thyristor triggering. The majority of the software was used to implement the PLL algorithm. The remaining software was used to configure and communicate with the

peripherals used in the implementation of the M67 DSP thyristor triggering controller. The ADCs were used to sample the transmission line currents and the digital port was used to read the reference control signal and was also used to generate the thyristor triggering signals.

The time taken to execute the algorithm determines the maximum sampling frequency of the M67 DSP thyristor triggering controller. This in turn determines the resolution at which the thyristors can be triggered since the thyristors can only be triggered at the end of a sampling interval. The resolution at which the existing M67 DSP thyristor triggering controller can trigger the thyristors is 0.45°. A review of literature has shown that the resolution at which the thyristors should be triggered must be less than 0.1° for satisfactory control of the TCSC, therefore it was undertaken to develop a controller that is capable of controlling the thyristor trigger angle at this higher resolution.

Chapter Five now details the development of this new hybrid TCSC triggering controller which was designed to meet the specification of 0.1 degree resolution in the thyristor trigger angle.

Chapter Five

M67 and eZDSP based hybrid TCSC triggering controller

5.1 Introduction

Chapter Four presented the details of the implementation of the prototype digital thyristor triggering controller. The controller was implemented using the Texas Instruments M67 digital signal processor (DSP). The M67 DSP is a floating point DSP that is capable of accurate mathematical computations. The shortcoming of the M67 is that it is not capable of generating high-resolution triggering pulses which are a requirement for a TCSC thyristor triggering controller.

The requirement for high-resolution timing of the thyristor triggering controller comes from the sensitivity of the TCSC to small variations in the thyristor triggering angle. The sensitivity of the TCSC is dependant on the TCR inductor parameters used in the TCSC. A review of literature has shown that for satisfactory control of the TCSC capacitive reactance the trigger angle resolution of the controller needs to be less than 0.1° [Xu1]. In the case of the prototype M67 digital signal processor (DSP) thyristor triggering controller, the best achievable trigger angle resolution was found to be 0.45° which necessitated an improvement in the controller.

A review of the literature has also shown that the best manner in which to implement a TCSC controller is to split the controller into a high level controller and a low level controller [Johnson1]. The high level controller will be required to perform the necessary PLL calculations and the low level controller to generate the triggering pulses to the thyristors. This chapter details the development and implementation of this improved hybrid digital controller. Two distinct Texas Instruments DSP-based controllers are used to implement this improved hybrid controller. An overview of the DSP controllers' individual capabilities is firstly given, which is followed by an in-depth discussion on the details of the implementation of the hybrid two level controller.

5.2 The DSP controllers - Overview

The two controllers that were used are Texas Instruments devices, which are highly specialised DSP-based platforms. The M67 DSP, the high level controller, is capable of performing accurate mathematical computations and the eZDSP, the low level controller, is capable of accurate timing. The two controllers in tandem are capable of satisfying the requirements for the laboratory-scale TCSC controller.

5.2.1 The M67 DSP-based controller

Chapter Four discussed the prototype digital thyristor triggering controller that was developed to control the laboratory-scale TCSC. The M67 DSP platform was successfully used to implement the prototype TCSC triggering controller; however it did not meet the performance specification of 0.1° resolution in the thyristor trigger angle as recommended in the literature [Xu1]. The maximum attainable resolution in the thyristor trigger angle was found to be 0.45°.

The prototype controller showed that the M67 DSP platform is capable of successfully implementing the PLL algorithm. The only limitation on the performance of the prototype controller stemmed from the M67 DSP platform not having an appropriate peripheral to accurately generate the thyristor triggering signals, independent of the sampling period of the controller.

Based on this it was decided to use the M67 DSP platform as the high level controller to implement the PLL algorithm and the necessary high-level calculations. The low level controller would then be required to communicate with the M67 DSP and ultimately be capable of generating the thyristor triggering pulses to meet the literature specification of 0.1° resolution in these pulses. The Texas Instruments F2812 eZDSP, discussed in the next section, was found to be most suited to these requirements.

5.2.2 The eZDSP controller

The F2812 eZDSP is a DSP based Texas Instruments device. The eZDSP is a 16 bit fixed point controller that operates at a clock frequency of 150 MHz [Texas1]. Since the eZDSP is a fixed point controller it is not ideally suited to the implementation of the trigonometric calculations required in the PLL algorithm of the TCSC controller. However, it is well suited for embedded system control, and it is capable of providing the accurate timing and signal generation required to generate high-resolution thyristor triggering signals for the TCSC.

The eZDSP is best described as a powerful event management DSP. It has numerous peripherals that are available to be used for accurate signal generation and signal timing measurement. The eZDSP has an event manager module that manages the operation of the peripherals that are dependant on both internal and external events. The most important trait of the event manager module is that it allows for background processing which frees up the main processor to perform other tasks.

The event manager module controls the operation of peripherals such as the interrupts, pulse-width modulation units and timers [Texas1]. However the discussion in this thesis will be confined to these eZDSP peripherals that are actually used in the implementation of the TCSC thyristor triggering controller, namely the four on-board timers, the digital port, the serial port and the pulse width modulation (PWM) peripheral.

The eZDSP has four individually configurable on-board timers, which have corresponding pulse-width modulation (PWM) outputs [Texas2]. The eZDSP also has three individually configurable PWM compare peripherals with corresponding outputs [Texas2]. These peripherals can be used to accurately generate the thyristor triggering signals that are required to implement a TCSC triggering controller with a resolution of less than 0.1°.

The overview of the two DSPs given shows their suitability to be used in tandem to implement the new hybrid two level controller as proposed in the literature [Johnson1]. It has been shown that the M67 is well suited for the role of the high level

controller due to its computational abilities, while the eZDSP is well suited for the role of the low level controller due to its accurate timing and hence accurate signal generation capabilities.

5.3 The improved hybrid DSP controller - Hardware

It was decided to use the M67 DSP as the high level controller due to its computational ability and the onboard monorail ADCs. This meant that the PLL algorithm and the calculation of the time-to-trigger the TCSC's thyristors are implemented on the M67 DSP. The eZDSP was chosen as the low level controller due to its accurate timing abilities and appropriate output peripherals. Consequently, the eZDSP is used to generate the high resolution thyristor triggering signals based on the time to trigger information passed to it from the high level controller. This arrangement of a high level and low level controller meant that, at a minimum, a communication link between the two DSPs is required.

Figure 5.1 shows a simplified block diagram of the high level and low level controllers, their functional roles, and the interfaces between them. Figure 5.1 shows that the inputs to the high level controller (M67 DSP) are the Phase A and Phase C transmission line currents and the commanded thyristor trigger angle, α. On board the M67 DSP, the high level algorithm employs a PLL to synchronise the TCSC triggering pulses to these power frequency variables measured from the transmission line, in the same manner as described in the prototype controller earlier in the thesis. However, in this hybrid controller, the PLL on the M67 DSP now uses an additional three-step-ahead prediction algorithm to calculate (in absolute time) the exact time left until triggering is required of the next thyristor in the TCSC, as well as which thyristor is to be triggered next.

Thus in the hybrid controller, the outputs from the high level controller (M67 DSP) are now a thyristor identification (ID) signal sent from the digital I/O port, and a second signal, sent from the serial port, that represents the exact time remaining till triggering of the identified thyristor is required. Both of outputs are sent to the low level controller.

Figure 5.1 also shows that in the hybrid controller, the ADCs on the M67 DSP are now externally triggered by a master clock signal generated on board the low level (eZDSP) controller. On board the low level controller, the eZDSP's Timer 4 is used to generate this master clock signal, and the remaining three timer ports (Timer 1, 2, and 3) and three PWM ports (PWM 1, 3, and 5) are used to generate the six high-resolution triggering pulses sent to the thyristors in the TCSC, based on the thyristor ID signal and time-to-trigger signals received from the high level controller.

The most important aspect of the new hybrid control scheme is to ensure that the two DSPs are time synchronised to each other; this is necessary because the time-to-trigger values for each thyristor are calculated relative to the time at which the M67 DSP ADCs sample the instantaneous transmission line currents. This synchronisation between the DSPs is achieved by making use of a master clock signal generated by eZDSP using timer 4. The consistent and accurate generation of this master clock signal ensures that the two DSPs are synchronised in time. The following sections of the chapter discuss the detailed implementation of each subsection of the hybrid scheme shown in Figure 5.1, starting with the master clock.

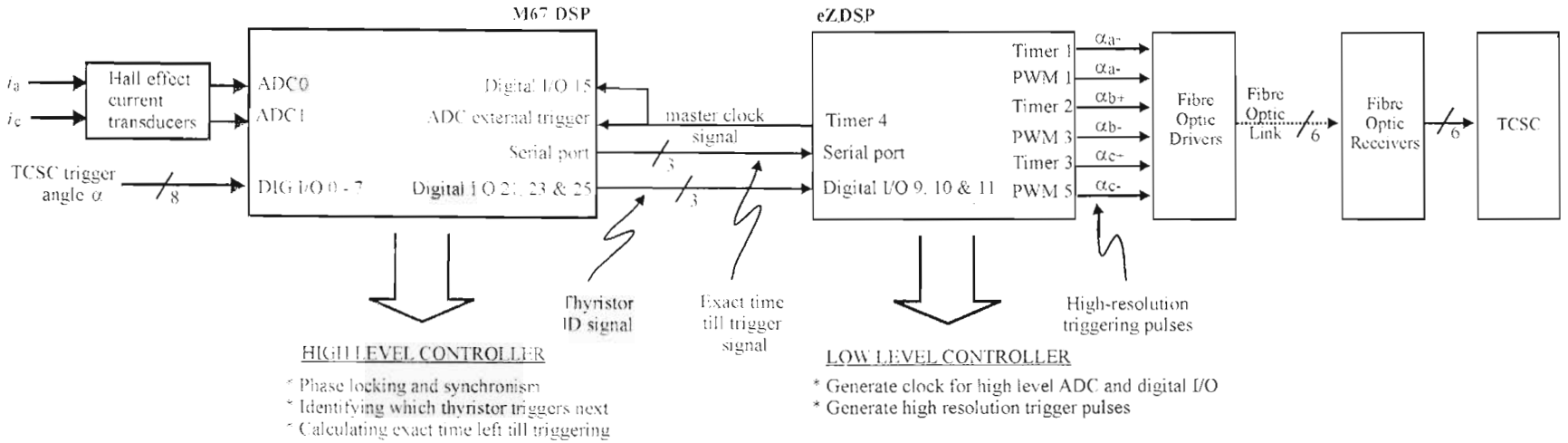

Figure 5.1: Block diagram giving an overview of the hybrid thyristor triggering controller.

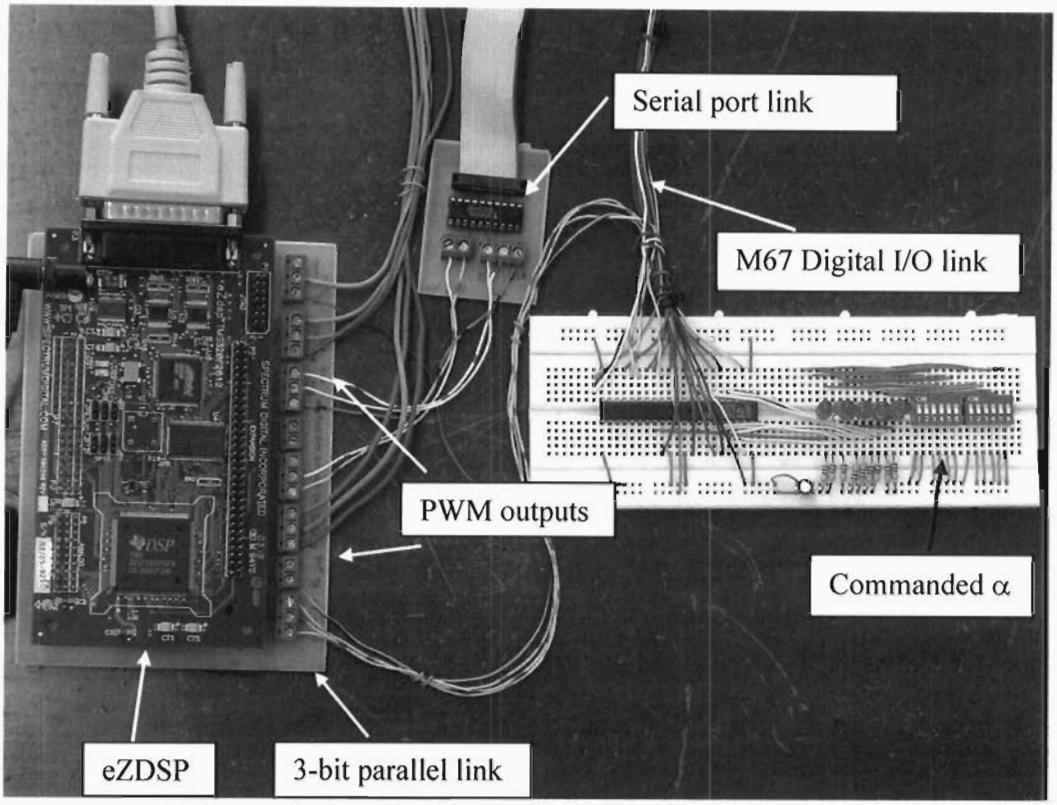

Figure 5.2: Photograph of the eZDSP (low level controller) showing the external connections

5.3.1 Master Clock – Timer 4

On board the high level controller, the time remaining until triggering of a thyristor is required is calculated relative to the sampling instants at which the high level controller (M67 DSP) itself measures the instantaneous transmission line currents. However, since the low level controller (eZDSP) is used to generate the actual triggering signals sent to the thyristors, the low level controller (eZDSP) also needs to know exactly when the high level controller's (M67 DSP's) ADCs have sampled the transmission line currents.

The approached adopted to ensure the required synchronisation in time between the two controllers is to use a master clock to drive the high level controller and its ADCs; this single clock then provides the reference both for the sampling of the ADCs on board the high level controller as well as for the triggering of the thyristors on board the low level controller. It was decided that, the low level controller would be used to provide the master clock signal, due to its accurate timing capability and

configurability of its timers. Specifically, Timer 4 on board the low level controller is used to generate the master clock so that the time at which the analogue-to-digital conversions are initiated is easily obtained by reading and storing the Timer 4 value onboard the low level controller.

The low level controller's Timer 4 has a dedicated PWM output pin which was used to make the generated clock signal available externally, to clock the high level controller in the hybrid scheme. Furthermore, the generation of the Timer 4 signal is achieved using the low level controller's event manager module, so that it is independent of the core processor: this approach ensures that the master clock signal for the two DSPs in the hybrid controller is accurately and consistently generated.

The actual configuration used to generate the master clock via Timer 4 had to take into consideration the specifications of the high level controller's ADCs since these ADCs have their own timing limitations. The specifications of the high level controller's ADCs, and hence the configuration of Timer 4, are discussed in the following section, which describes how the low level controller's Timer 4 is used to trigger the high level controller's ADCs.

5.3.2 Externally triggered ADCs

The most important event in the high level controller, that requires accurate time stamping is the initiation of an analogue-to-digital conversion onboard the high level controller. This time stamping is achieved by configuring the ADCs on the high level controller to be triggered by the rising edge of an external clock source, so that the low level controller's Timer 4 can trigger and initiate analogue-to-digital conversions onboard the high level controller. The master clock signal generated by the low level controller Timer 4, as shown in Figure 5.3, is connected to the external trigger input pin of the high level controller's ADC and to a digital I/O pin onboard the high level controller.

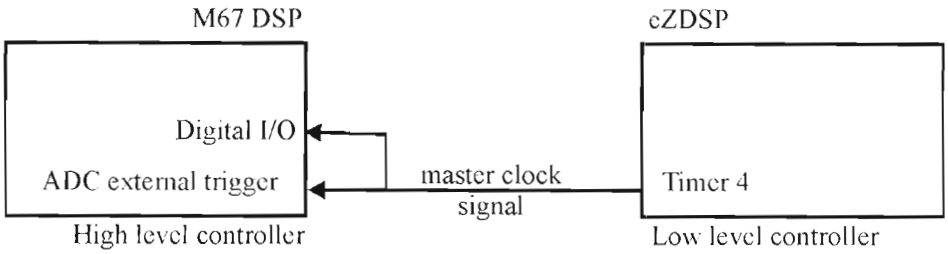

Figure 5.3: Simplified block diagram showing the master clock connection between the two DSPs

The rising edge of the low level controller's Timer 4 initiates an analogue-to-digital conversion onboard the high level controller and the falling edge signals that the ADC can be read. The falling edge of Timer 4 is detected by polling the high level controller's digital I/O pin 15, hence the reason for the connection of Timer 4 to the digital I/O pin. The alternative approach of using an external interrupt to control the analogue-to-digital conversion process was not used, as previous experience with the high level controller had shown that the latency of the interrupt service routine of the M67 DSP is relatively high; hence for this reason the software polling method described above was used to control the analogue-to-digital conversions on board the high level controller.

The high level controller's ADCs have a maximum sampling frequency of 200 kHz and a settling time of 5 μs [Innovative2], effectively meaning that the ADCs can only be read 5 μs after a conversion has been initiated. Hence, the master clock was configured in such a manner that a rising edge initiates, and signals the start of, an analogue-to-digital conversion and the falling edge signals that the ADCs can be read. To accommodate for the aforementioned specifications of the ADCs, and to allow sufficient time for the execution of the high level controller algorithm, the master clock was configured to operate at a frequency of 5 kHz and with a high time set to 6 μs.

The next set of hardware peripherals that are described are those that were used for communication of data between the high level and low level controllers, starting with the serial communication link which was used to communicate the time remaining until a thyristor should be triggered.

5.3.3 Serial communications

The high level controller and the low level controller each have a high-speed serial port interface that is suitable for communication purposes between DSP-based platforms. Figure 5.4 shows the three-wire serial communication system: a data signal, clock signal, and a read enable signal. The high level controller was configured as the master, which meant that the high level controller initiates communications and controls the clock frequency. The 16-bit data flow is unidirectional from the high level controller to the low level controller.

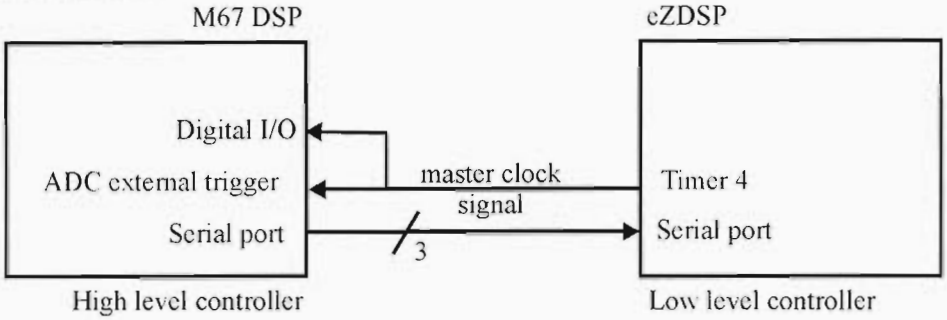

Figure 5.4: Simplified diagram showing serial communication link between the two DSPs

The data that is sent from the high level controller to the low level controller represents the time remaining until a thyristor should be triggered relative to when an analogue-to-digital conversion was initiated onboard the low level controller. This time-to-trigger value is calculated on board the high level controller as part of the high-level controller algorithm using a three-sampling-period ahead prediction algorithm which is discussed in greater detail later in the chapter. Apart from the time at which a thyristor is to be triggered, the other information that the eZDSP requires is which of the six thyristors in the TCSC should be triggered. This thyristor ID information was sent via a parallel communication link from the high level controller to the low level controller.

5.3.4 Parallel communications

Figure 5.5 shows the 3-bit parallel communication link that was designed to transmit data from the high level controller to the low level controller. The data sent using the 3-bit link allows for the unique identification of each thyristor. This thyristor ID information is required by the low level controller since the gate of each thyristor in the TCSC is driven from a dedicated compare register and associated hardware output

pin on board the eZDSP. Therefore the 3-bit data obtained by the low level controller from the parallel link specifies which compare register should be loaded with the time-to-trigger value obtained from the serial port (described in section 5.3.3) and hence ultimately which thyristor will be triggered.

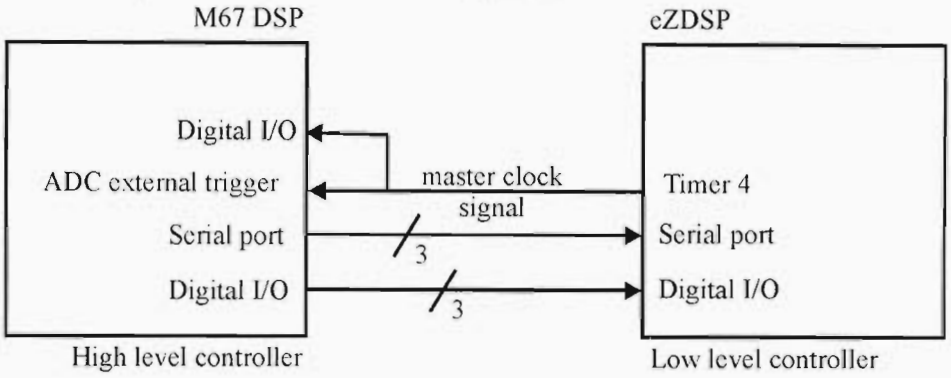

Figure 5.5: Simplified diagram showing parallel communication link between the two DSPs

The high-level algorithm developed for the high level controller determines which thyristor is to be triggered within the next three sampling periods by making use of dedicated decision structures for each of the six thyristors. In this high level algorithm, each of the six thyristors of the three-phase TCSC is allocated a unique identification number from one to six; the actual representation and identification scheme used for the six thyristors is shown in Appendix C.

5.3.5 Thyristor triggering signal generation

The final hardware peripheral group used to generate the thyristor triggering signals comprises three timer PWM ports (T1PWM, T2PWM, T3PWM) and three general purpose PWM ports (PWM1, PWM3, PWM5), all of which are on board the eZDSP. Figure 5.6 shows that the six different PWM ports on board the low level controller are used to generate individual thyristor triggering signals that are sent to the six thyristors in the TCSC. Each PWM port has a dedicated output pin and an associated compare register, and is configured so as to generate a logic high when the compare is a logic-true. In the case of the PWM compare registers the reference used is Timer 1, whereas in the case of the timer compare registers, the reference used by the compare register is its own counting register. Furthermore the three timers (Timer 1, Timer 2, and Timer 3) onboard the low level controller are configured to be free running and

were synchronised to each other. The benefits of configuring the three timers in this manner will become evident in section 5.4.4.

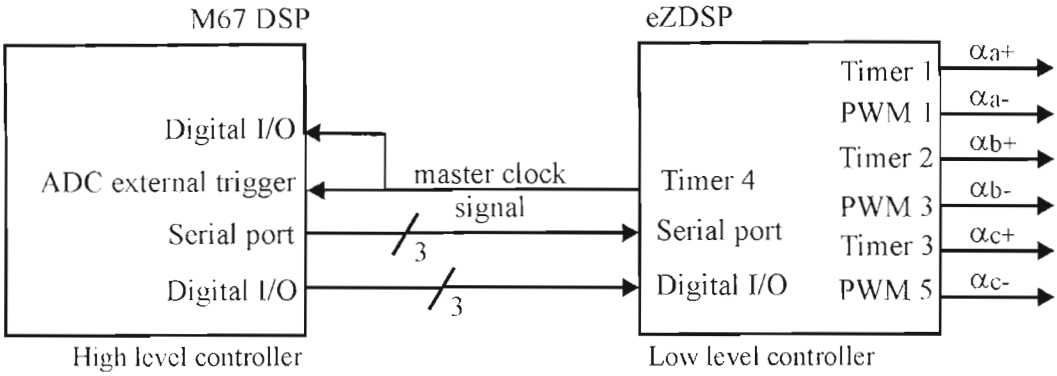

Figure 5.6: Simplified block diagram showing the connections between the two DSPs and the connections from the PWM ports.

The thyristor trigger pulses are generated by the low level controller using two pieces of information that are transmitted from the high level controller over the serial and parallel links described earlier. The data sent by the high level controller via the parallel port is the thyristor ID information which is used by the low level controller to determine which thyristor is to be triggered, and hence which particular compare register must be set up to generate the next thyristor trigger signal.

The data sent via the serial port contains the information regarding how much time remains until the identified thyristor must actually be triggered; this time-to-trigger information is sent from the high level controller in the form of an integer number of timer increments, calculated relative to the rising edge of the master clock that occurred at the beginning of the current sampling interval. In this way, the low level controller is able to load the correct compare register (as determined by the thyristor ID data) with the required number of timer increments (as determined by the time-to-trigger data) so that a logic high signal is generated at the required instant in time relative to the master clock signal. The following section discusses the software algorithm that was developed for the hybrid TCSC triggering controller.

5.4 The improved hybrid DSP controller – Software Algorithms

The previous section has described the various hardware features used on the high level and low level controllers, and their interconnections, in the hybrid TCSC triggering controller designed in this thesis. This section now discusses the software algorithms that have been developed for the hybrid TCSC controller. The high level and low level controllers were programmed using the C programming language. The hybrid TCSC triggering controller algorithm as a whole was, at all times, designed to be robust and as time efficient as possible.

The high level algorithm executing on board the high level controller was designed to execute sequentially, starting with the reading of the ADCs, followed by the PLL calculations needed to obtain the instantaneous angle of the TCSC capacitor voltage, and finally a decision structure to determine if any of the six thyristors need to be triggered. If the decision structure determines that a particular thyristor is to be triggered, the high-level algorithm calculates the time remaining until this thyristor is to be triggered and communicates this to the low-level high resolution triggering algorithm on the low level controller.

5.4.1 External event detection

Experience gained from the implementation of the prototype TCSC triggering controller described in Chapter Four, showed that the interrupt latency of the M67 DSP is excessively high. The use of interrupts in the prototype TCSC triggering controller increased the execution time of the algorithm, hence reducing the maximum achievable sampling frequency of the controller. As will be shown later in the chapter, the entire hybrid controller algorithm is event driven, this means that the algorithms are started by the occurrence of external events. In the case of the high level controller it is the occurrence of the falling edge of the master clock which starts the algorithm on the high level controller. In the case of the low level controller it is the reception of data on the parallel port, which starts the low level controller algorithm.

Therefore the occurrence of these events (the falling edge of the master clock on the high level controller and the reception of data on the parallel port of the low level

controller) requires monitoring, which necessitates the use of structures to detect these occurrences. An alternative solution to the use of interrupts is instead to use software polling in the design of the DSP software algorithm for the hybrid TCSC triggering controller. In the case of the hybrid TCSC triggering controller, the use of software polling is a reliable and much more time efficient method of event detection as opposed to the use of interrupt service routines.

As stated previously the software algorithms were developed to execute in the most time efficient manner. The reason for this was to reduce the time taken to execute the software algorithm hence minimise the error introduced into the thyristor triggering signal due to the time taken to execute the software algorithm. Figure 5.1 shows that the hybrid TCSC triggering controller has a cascaded arrangement, which will inherently introduce further time delays in the execution of the software algorithm, resulting in greater inaccuracies in the generation of the thyristor triggering signal. The next section discusses an algorithm that was designed to eliminate the time delays associated with the execution of the entire hybrid TCSC triggering controller algorithm.

5.4.2 Three step ahead prediction algorithm

One of the problems identified with the prototype TCSC triggering controller was that the resolution of thyristor trigger angle was dependant on the sampling interval of the TCSC triggering controller algorithm. This was because the thyristor triggering signal could only be generated at the end of a sampling period, as the M67 DSP is incapable of background processing. In practice, the finite time required for ADC sampling, and the execution of the PLL algorithm on board the M67 DSP meant that, when using the prototype controller approach, the sampling intervals that could be achieved with the M67 DSP were not small enough to meet the trigger angle resolution required for a TCSC.

The two-DSP hybrid approach described in this chapter was conceived to address these problems. In particular, this approach uses a modified algorithm on board the high level controller, to firstly accommodate for the finite time taken from the moment that the variables are sampled using the ADCs until the triggering controller algorithm has finished executing, and secondly to allow generation of thyristor

triggering signals independently from the M67 DSP's algorithm execution to allow for a thyristor to be triggered at the exact time instant that it needs to be. The algorithm works by determining if a thyristor is to be triggered within the next three sampling periods. This means that the thyristor trigger angle is calculated in advance, which ensures that the thyristor is triggered at the exact time that it needs to be.

The algorithm implemented on the prototype TCSC triggering controller made use of a simple comparison to determine when a thyristor should be triggered. The comparison was performed between the instantaneous angle of the TCSC capacitor voltage, θ, (output of PLL algorithm) and the commanded thyristor trigger angle, α. If the instantaneous angle of the TCSC capacitor voltage, θ, is greater than the commanded thyristor trigger angle, α, then a logic high is generated to trigger a thyristor. Figure 5.7 shows the time delays that are associated with the algorithm implemented on the prototype TCSC triggering controller.

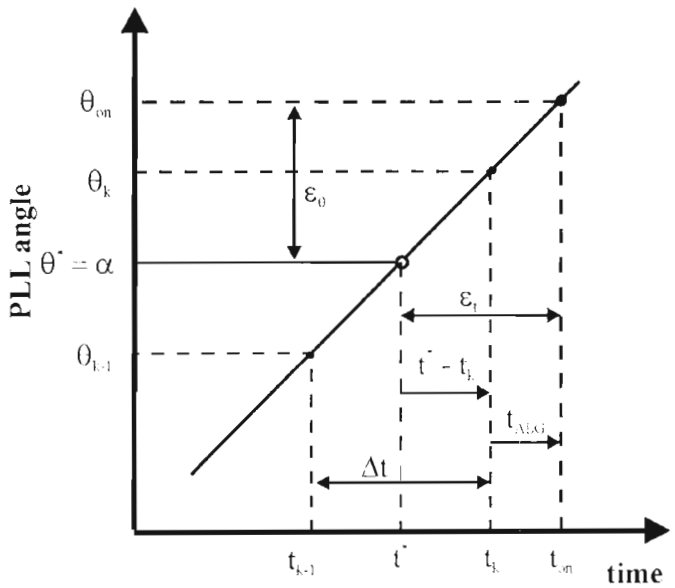

Figure 5.7: Figure showing the origins of time delays in the generation of the thyristor triggering signal for the prototype TCSC triggering controller

At any given sampling interval, k, the instantaneous angle of the TCSC capacitor voltage calculated by the PLL algorithm will be, θ_k, then the decision to trigger a thyristor is taken as follows:

If $(\theta_k \geq \theta^*)$
    trigger thyristor
end

Because of the (a) the discrete nature of the sampled-data control system, and (b) the fact that the algorithm has no step ahead prediction or background processing abilities, then the earliest the thyristor can actually turn on is at time t_k when it should turn on at t^*, as shown in Figure 5.6. (In practice, the actual turn on time will be somewhat later than t_k, because of the finite time t_{ALG} taken to read the on board ADCs and for the time taken to execute the algorithm). Thus the practical error, ε_t, in the turn on time is $(t_{on} - t^*)$, yielding a thyristor trigger angle error of $\varepsilon_\theta = (\theta_{on} - \theta^*)$. The component of the turn on time error $(t^* - t_k)$ can be anywhere between zero and one sampling interval Δt, such that the total error in the turn on time can vary between t_{ALG} and $(t_{ALG} + \Delta t)$ for this method of control.

The following discussion is on the three-step-ahead prediction algorithm that is used by the hybrid TCSC triggering controller to accurately determine when a thyristor should be triggered.

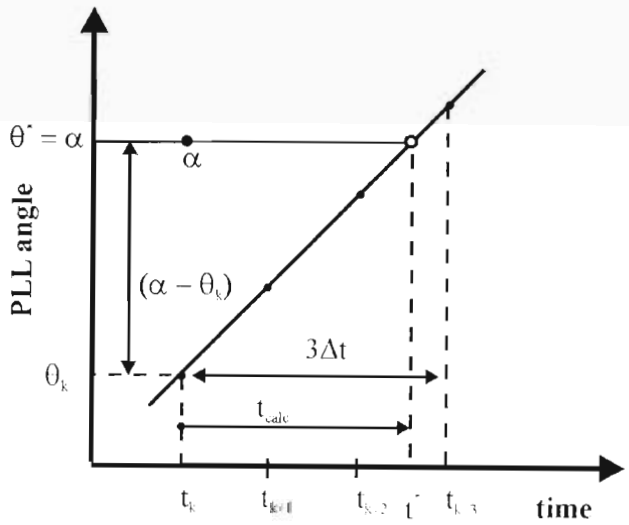

Figure 5.8: The three-step-ahead prediction algorithm

With reference to Figure 5.8, it can be seen that at a given sampling interval,

$$\dot{\theta}_k \approx \frac{\Delta\theta}{\Delta t} = \frac{(\alpha - \theta_k)}{(t^* - t_k)} \tag{5.1}$$

where $\dot{\theta}_k$ is the rate of change of θ with respect to time at time t_k. Since the variable $\dot{\theta}$ is explicitly available as part of the PLL algorithm, at any sampling interval k, as are the PLL output angle, θ, and the commanded thyristor trigger angle α, then at

each sampling interval k the exact time left till triggering of the thyristor is required is given by $t_{calc} = (t^* - t_k)$ and can be calculated directly as

$$t_{calc} = \frac{(\alpha - \theta_k)}{\dot{\theta}_k} \tag{5.2}$$

Thus, in the hybrid controller algorithm, the exact time left to trigger a thyristor, relative to the current sampling time, is calculated using equation (5.2). If this time t_{calc} is less than three sampling intervals of the master clock ($3\Delta t$), then the high level algorithm determines which thyristor is required to trigger next. This time, t_{calc} is converted into an integer number of low level controller timer counts. This timer increment value is transmitted immediately via the serial communication link and at the same time the thyristor ID is transmitted via the parallel communication link so that the required thyristor will be triggered at the correct time t^*, independently of the high level controller.

5.4.3 Decision structures

The difference between the commanded thyristor trigger angle and the calculated instantaneous angle of the TCSC capacitor voltage is used to determine if a thyristor shall be triggered. The difference in the two angles is converted to time by dividing the difference by the system frequency as shown in equation (5.2). The result of this calculation is then checked to determine if the value is less than three sampling periods, which is 600 μs. If the calculated value is less than 600 μs then the time-to-trigger the thyristor is recalculated in terms of timer increments of the timers on board the low level controller. The serial communication link is then used to transmit this calculated number of timer increments, from the high level controller to the low level controller.

The other information required to trigger a thyristor is which one of the six thyristors should be triggered. Each of the six thyristors in the laboratory-scale TCSC is assigned a unique integer value, the thyristor ID, from one to six within the high level controller algorithm. Dedicated decision structures within the hybrid TCSC triggering controller determine which one of the six thyristors should be triggered. Once the thyristor that must be triggered is identified, the thyristor's unique thyristor ID is written to the parallel port of the high level controller. The parallel communication link then transmits the thyristor ID from the high level controller to the low level

controller. The low level controller then uses the thyristor ID information to trigger the correct thyristor. The next section goes on to discuss in greater detail how the parallel port data (thyristor ID), and the serial port data (time-to-trigger), discussed earlier in this section, are used by the low level controller to ultimately generate the correct thyristor trigger signal.

5.4.4 Generation of the thyristor triggering signal

The previous section looked at how the high level controller algorithm determined when and which thyristor to trigger. The time-to-trigger information specified when the thyristor should be triggered and the thyristor ID specified which of the six thyristors should be triggered. The time-to-trigger information was sent by the high level controller to the low level controller via the serial communication link and the thyristor ID was sent by the high level controller to the low level controller via the parallel communication link.

The time-to-trigger and thyristor ID information is used by the low level controller to generate the appropriate thyristor triggering signal. However, recall that the time-to-trigger information is a calculated time delay until a thyristor should be triggered, and consequently cannot be used on its own by the low level controller algorithm to determine when a thyristor should be triggered. The low level controller algorithm also requires a reference time from which to count down the time-to-trigger information it receives from the high level controller. Then, when the time-to-trigger delay has elapsed relative to this reference time, the low level controller generates a logic high to trigger the appropriate thyristor.

Recall that the low level controller's Timer 4 is the master clock which provides the time reference for the hybrid TCSC triggering controller, and it is the rising edge of Timer 4 that initiates an analogue-to-digital conversion on board the high level controller. The absolute time at which an analogue-to-digital conversion occurs, corresponding to the rising edge of Timer 4, is of importance because the instantaneous angle of the TCSC capacitor voltage calculated in the high level controller algorithm is effectively determined at this value of time. This effectively makes the point in time at which a rising edge of Timer 4 occurs the reference for the triggering of thyristors, since the decision to trigger a thyristor is based on the

instantaneous angle of the TCSC capacitor voltage, which is calculated using variables sampled at this point in time.

Since Timer 4 is onboard the low level controller, the time at which a rising edge of Timer 4 occurs is readily available to the low level controller algorithm. The rising edge of Timer 4 is determined within the low level controller algorithm by software polling of the Timer 4 flag, since this flag changes to a logic true whenever the rising edge of Timer 4 occurs. A second timer (Timer 1 on board the low level controller) is used as a reference to record the exact time at which the Timer 4 flag changes to true, effectively meaning that the count value of Timer 1 is saved whenever a rising edge of Timer 4 occurs. As stated in section 5.3.5, Timer 1 is also the internal reference timer on board the low level controller for the generation of the thyristor triggering signal. Therefore the saved count value of Timer 1, which corresponds to the time of the last rising edge of Timer 4, is used as the time reference for the triggering of a thyristor. The final value loaded in to a particular compare register on the low level controller is then calculated by adding the saved counter value of Timer 1 to the time-to-trigger information obtained from the serial port (high level controller algorithm) to determine the absolute value of time at which a thyristor should be triggered.

The reason that it is possible to use the Timer 1 count value for calculating the thyristor turn-on-time irrespective of which thyristor is to triggered, is that the other timers used to generate thyristor triggering signals (Timer 2 and Timer 3 in Figure 5.5) are synchronised to Timer 1, which means that their count values are exactly the same at any point in time. The PWM ports' compare registers were configured to use Timer 1 as their counting reference. A detailed flow chart of the hybrid controller algorithm is contained in Appendix C.

Therefore, for the low level controller to generate the thyristor triggering signal, three sets of information are required: (a) the thyristor ID (obtained from the high level controller via the parallel communication link); (b) the time-to-trigger (obtained from the high level controller via the serial communication link); and (c) the reference time to be used to determine the absolute triggering time of a thyristor (obtained internally on board the low level controller). The next section presents the results obtained from tests conducted on the hybrid TCSC triggering controller to ensure that hybrid TCSC

triggering controller actually met the performance and design philosophy requirements outlined thus far.

5.5 Performance tests of the hybrid TCSC triggering controller

The design and performance of the hybrid controller was tested before the controller was used to control the operation of the TCSC. The hybrid controller was tested by viewing the various output waveforms with the aid of an oscilloscope.

5.5.1 Low level controller Timer 4 waveform

The most important waveform that required verification was the Timer 4 waveform generated by the low level controller (eZDSP). The Timer 4 waveform is important because it acts as the master clock reference signal for the hybrid controller, and any variation in the Timer 4 signal will be transferred through to the thyristor triggering pulses. A further consideration is that the three step ahead prediction algorithm relies on accurate and consistent generation of the triggering signal to the ADCs on board the high level controller in order to predict the instantaneous angle of the TCSC capacitor voltage.

Figure 5.9 shows a measurement carried out on the Timer 4 signal, using a digital storage oscilloscope, to determine the degree of variation in the time at which the Timer 4 waveform goes high on successive leading edges. The oscilloscope was set up to trigger on a leading edge of the Timer 4 clock waveform in continuous-capture and display mode, so that each captured waveform was displayed without erasing previous captured waveforms. By allowing the oscilloscope to run in this mode for some time it is possible to measure the variation (relative to the first leading edge of the waveform) in the time at which a large number of subsequent edges occur.

Figure 5.9 shows that the variation in the point at which successive leading edges of the Timer 4 waveform occur relative to previous leading edges is 240 ns. For a 50 Hz system, a measurement resolution in time of 240 ns corresponds to a triggering angle resolution of 0.00432°.

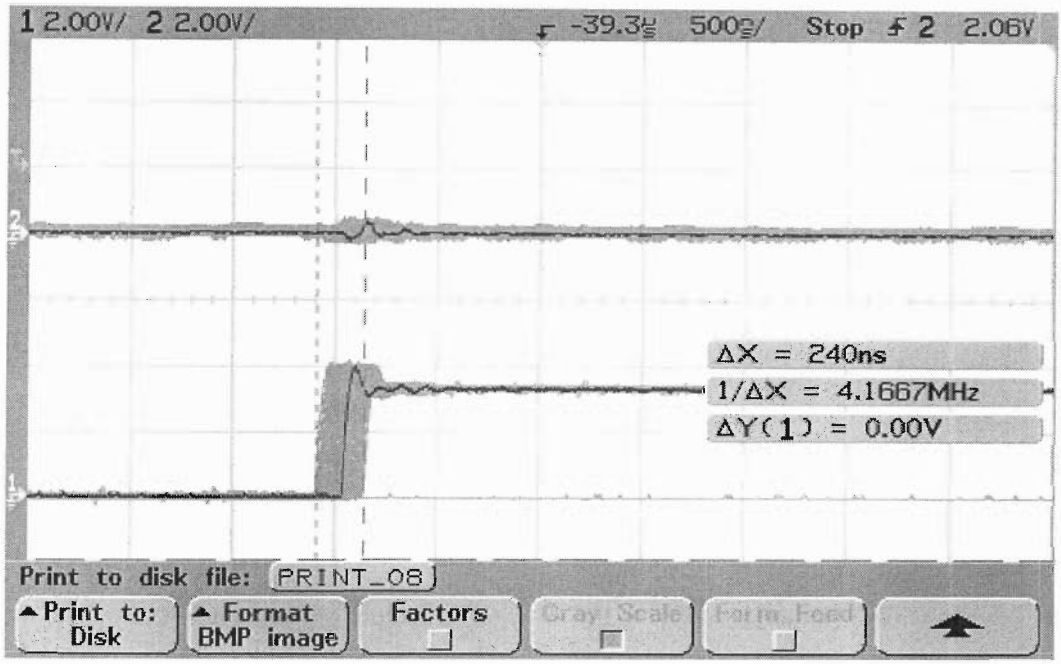

Figure 5.9: Timer 4 waveform showing the variation of the leading edge

Such resolution is well within the 0.1° requirement for TCSC triggering, and hence the results obtained from measurement shown in Figure 5.9 demonstrate that Timer 4 on board the low level controller is capable of generating the triggering signal to the ADCs on board the high level controller, consistently and to a sufficiently high degree of accuracy in time. The next section presents the results obtained from verification tests conducted on the parallel and serial communication links.

5.5.2 Communication waveforms

The serial and parallel communication links were tested by viewing their data waveforms on the oscilloscope, as well as checking the values of internal variables in the controllers. The serial and parallel communication links are unidirectional, with the high level controller being the master and the low level controller being the slave in both instances. The serial communication link was tested first.

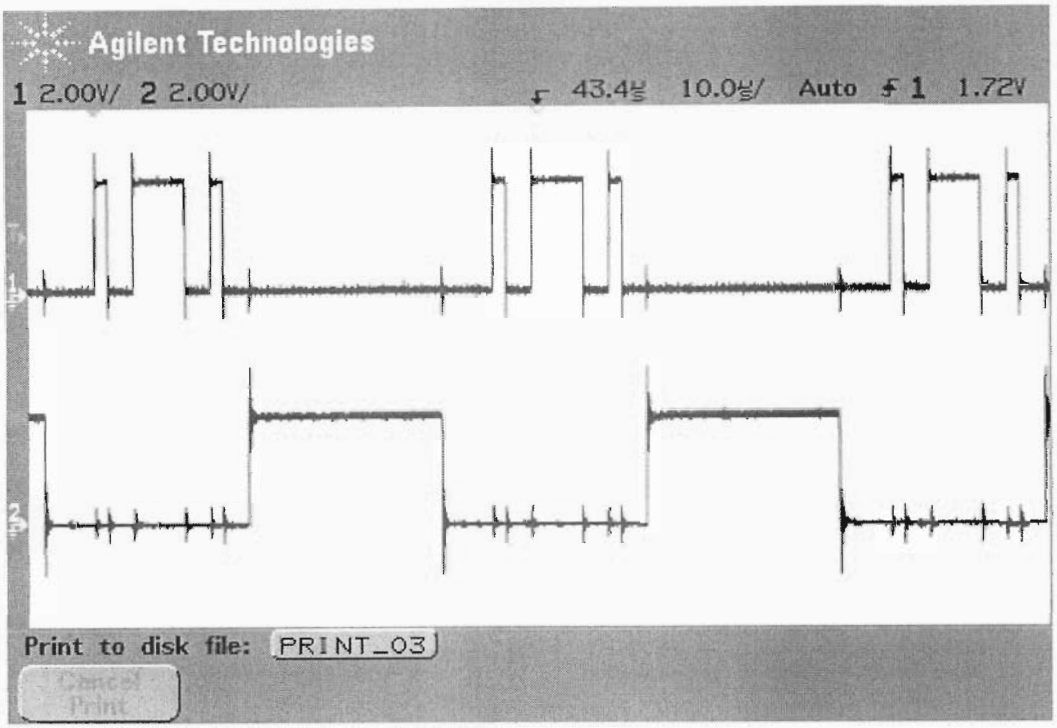

Figure 5.10: Oscilloscope screen shot showing the serial port data waveform (top) and the synchronisation pulse (bottom)

Figure 5.10 shows a screen shot of the output waveforms of the serial port of the high level controller, the top waveform being the data waveform and the bottom waveform being the synchronisation and read-enable waveform. Figure 5.10 was used to ensure that the serial communication link was configured and functioning correctly, specifically that the read enable waveform was sixteen bits long.

The clock frequency of the serial port was also verified along with the synchronisation pulse for which the measured waveforms are shown in Appendix D. Verification tests were also carried out by sending known data via the serial communication link and observing the data waveforms with the aid of the oscilloscope. In addition, the final data obtained in the appropriate destination registers was checked to ensure that the data sent by the high level controller corresponded with the data received by the low level controller.

The other important communication waveform that was of significance was the timing between the sending of parallel data and the sending of serial data by the high level controller. This is of significance since the low level algorithm on board the low level

controller is triggered by the reception of parallel data, which then allows the serial port to be read. These waveforms were captured using an oscilloscope and are shown in Figure 5.11.

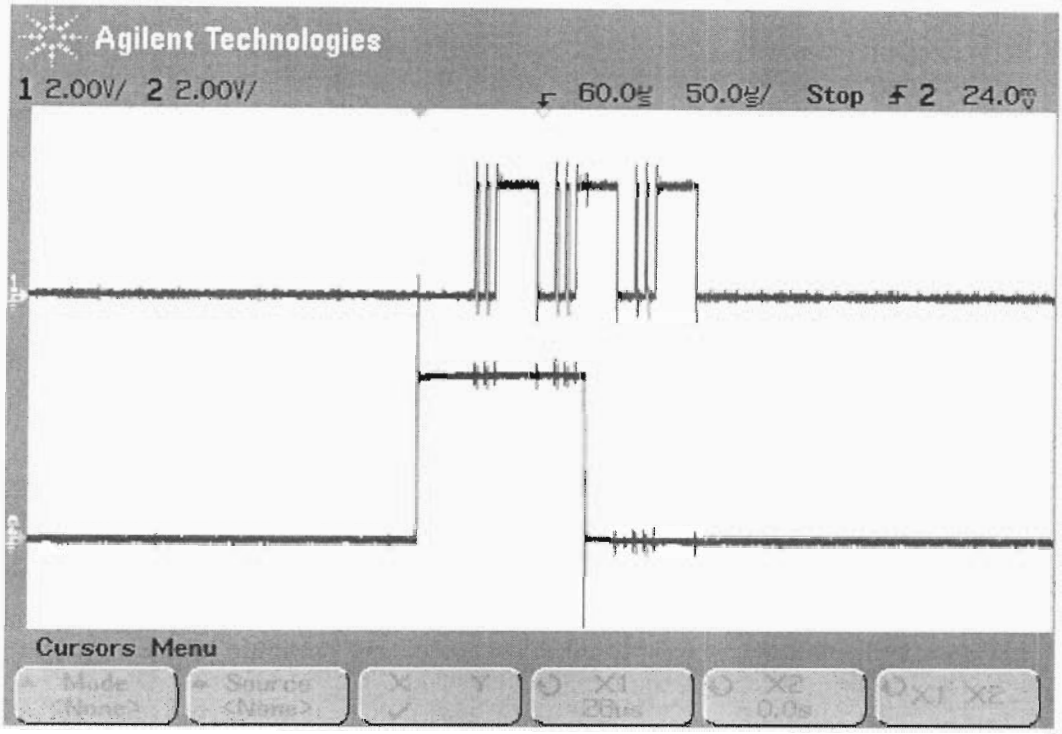

Figure 5.11: Oscilloscope screen shot showing the serial port data waveform (top) and one bit of the parallel data waveform (bottom)

Figure 5.11 shows that the parallel data waveform, shown on the bottom, is sent before the serial port waveform, shown on the top. Figure 5.11 thus confirms that the communication links are operating as designed, hence proving that the high level controller algorithm is being executed in the correct sequence. The timing between the parallel and serial data waveforms also ensures that the algorithm on the low level controller will also be executed in the correct sequence.

The reason for structuring the algorithms in this manner and hence the communication timing was to minimise the occurrence of communication errors and incorrect operation, which could lead to spurious generation and hence triggering of the thyristors. After the communication waveforms were verified to be correct, the thyristor triggering waveforms were then checked.

5.5.3 Thyristor triggering pulse waveforms

The thyristor triggering waveforms were checked by simulating ideal 50 Hz transmission line currents within the high level controller and specifying a known and constant thyristor trigger angle. In other words, during the initial testing, the high level algorithm on board the high level controller was executed using ideal, pseudo-measurements at its inputs by means of on board DSP software instead of using actual external inputs. The thyristor triggering signals from the output PWM ports were then viewed and captured, under these ideal and controlled conditions, with the aid of an oscilloscope.

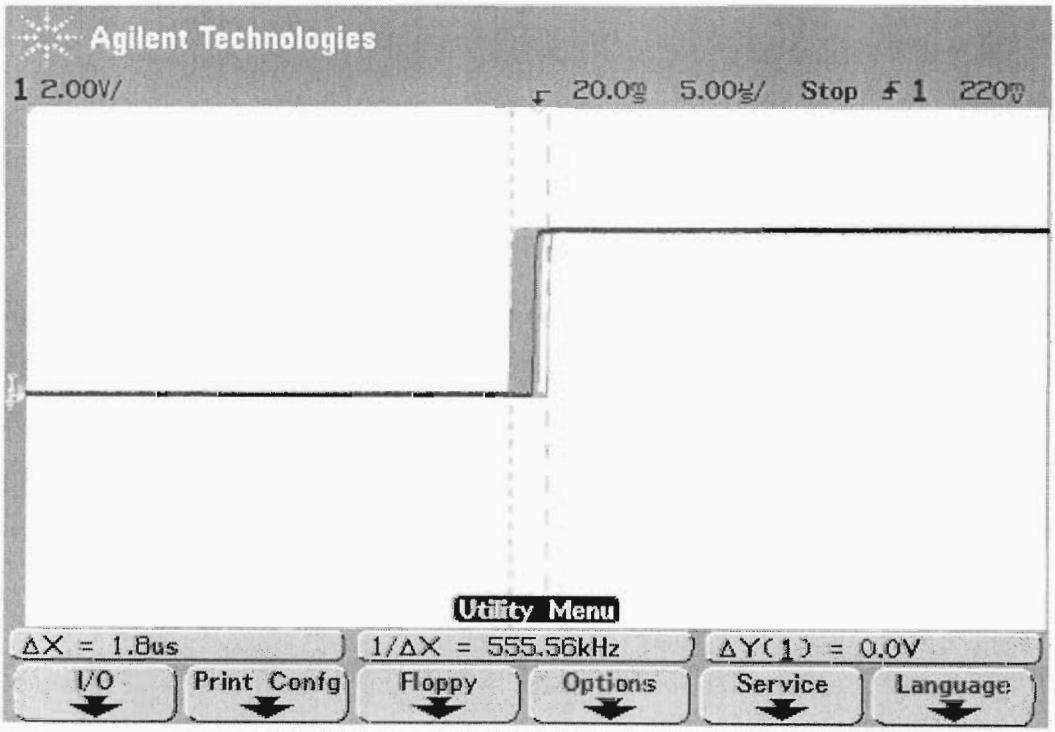

Figure 5.12: Oscilloscope screen shot showing the front edge of the thyristor triggering pulse

The most important aspect of the thyristor triggering waveform was the variation of the front edge of the thyristor triggering pulse, as shown in Figure 5.12. The specification as proposed by literature [Xu1] was a 0.1° resolution in the thyristor triggering pulse (5.55μs for a 50 Hz system or 4.63 μs for a 60 Hz system). The digital storage oscilloscope was used to view the thyristor triggering pulse waveform and was once again configured to capture and display multiple instances of the leading edge of this signal. Figure 5.12 shows the captured waveform for one of the

thyristor triggering signals and the measured variation in the timing of the front edge of the thyristor triggering signal.

The measurement of the variation in time of the front edge of the thyristor triggering signal in Figure 5.12 is 1.8 μs. The design specification is that the maximum allowable variation of the thyristor triggering pulse is 5.55μs. This means that the new hybrid controller comfortably meets the design specification. The duration (i.e. the on time) of the thyristor triggering pulses were also checked and verified, as well as the phase differences between the six pulses. Selected waveforms captured with the aid of the oscilloscope are contained in Appendix D. At this point the controller was rigorously tested to ensure that it would function as required, before being used to control the operation of the laboratory-scale TCSC.

5.6 Conclusion

Chapter Four discussed the details of the prototype TCSC thyristor triggering controller that was developed to control the operation of the laboratory-scale TCSC. The prototype controller was successfully implemented using the M67 DSP platform, but it did not meet the performance requirement of 0.1° resolution in the thyristor trigger angle as proposed in literature [Xu1]. The maximum achievable resolution was measured to be 0.45°. This necessitated an improvement in the performance of the thyristor triggering controller.

A review of literature showed that a two level or split controller scheme is best suited to implement a controller for a TCSC [Johnson1]. The experience of implementing the prototype TCSC triggering controller showed that the M67 DSP was capable of implementing the required PLL algorithm, but that its shortcoming was that it did not have an appropriate peripheral to accurately generate the thyristor triggering signals independently of its sampling period. It was decided to retain the M67 DSP platform as the high level controller and use a low level controller to generate the thyristor triggering pulses.

The F2812 eZDSP was selected to be used as the low level controller. The eZDSP possessed the required capabilities to accurately generate the thyristor triggering pulses and communicate with the high level, M67 DSP, controller. This chapter provided the details of the implementation of this improved hybrid controller. The performance of the hybrid controller was tested by viewing the relevant output waveforms with the aid of an oscilloscope. The waveforms showed that the controller was operating as designed and it also exceeded the performance specification of 0.1° in trigger angle resolution as proposed in literature. The resolution of the thyristor trigger angle for the new hybrid controller was measured to be 0.032° for a 50 Hz system.

A second area for possible improvement in the performance of the laboratory-scale TCSC that was identified in Chapter Three was to re-examine the parameters of the components used in the laboratory-scale TCSC. This possible parameter re-design was proposed to minimise the effects of the non-ideal components used in the laboratory-scale TCSC. Specifically it was noted that the resistance of the TCR inductor played a significant role in the performance of the laboratory scale TCSC, as compared to the ideal expectation. Chapter Six now goes onto discuss the redesign of the laboratory-scale TCSC parameters in order to minimise the non-ideal effects of the components used in its construction.

Chapter Six

The effect of TCR inductor parameters on the performance of the laboratory-scale TCSC

6.1 Introduction

Chapter Five discussed the implementation of the improved hybrid TCSC triggering controller. A review of literature had shown that the thyristor trigger angle resolution of the TCSC triggering controller must be less that 0.1° for the stable operation of the power system and the TCSC [Xu1]. The first prototype TCSC triggering controller was shown to have a trigger angle resolution of 0.45° whereas the improved hybrid controller has a thyristor trigger angle resolution of 0.0324°.

This improvement in the trigger angle resolution of the TCSC triggering controller also means that there should be better agreement between the practical performance of the laboratory-scale TCSC and the theoretical characteristics. One of the other areas of possible improvement that was identified was the parameters of the laboratory-scale TCSC itself. Specifically the reactance of the TCR inductor used in the original laboratory-scale TCSC power circuit design was chosen to be large [Mazibuko2]. The reason for this choice of large TCR inductor was to reduce the current ratings of the thyristors, and the inductors used in the laboratory-scale TCSC.

This chapter looks at redesigning the laboratory-scale TCSC, with the aid of a detailed PSCAD simulation model, based on a range of new inductors that had been constructed for use in the laboratory-scale TCSC since the work described in [Mazibuko2]. Thereafter, based on the findings of these simulation studies, a select few of these inductors are chosen for use in the practical laboratory-scale TCSC.

6.2 TCR inductor

The TCR branch of the laboratory-scale TCSC consists of back-to-back thyristors connected in series with an inductor. The TCR branch of the TCSC is the most important part of the TCSC power circuit as it is the part of the circuit that is used to control the operation of the TCSC. It is also the parameters and characteristics of the TCR branch that determine the net variable reactance characteristic of the TCSC as a whole, therefore the components used in the TCR branch were revisited to improve the performance of the laboratory-scale TCSC.

Chapter Three examined the effects of the non ideal properties of the inductor and thyristors on the performance of the laboratory-scale TCSC. Chapter Three showed that the effect of the forward volt drop of the thyristors is to reduce the magnitude of the TCR current pulses in the time domain and to move the capacitive reactance versus trigger angle characteristic of the laboratory-scale TCSC to the left. However, the forward volt drop of a thyristor is a characteristic of the device itself and hence cannot be minimised; moreover, it was noted that the effect of the forward volt drop of the thyristors is only apparent in a low voltage TCSC. The redesign efforts in this chapter were therefore focused on the inductor used in the TCR branch.

Chapter Three also discussed the effects of the non ideal properties of the inductor on the performance of the laboratory-scale TCSC. It was shown that the effect of the resistance of the inductor was to reduce the steepness of the TCSC's capacitive reactance versus trigger angle characteristic. It was also seen that the resistance of the inductor introduced asymmetry in the steady state time domain waveforms of the TCR current pulses. Therefore it was decided to manufacture new inductors to minimise the resistance of the inductor and hence increase the X/R ratio of the inductors.

Another TCSC design parameter that is revisited in this chapter is the parameter $\lambda = \sqrt{X_C / X_L}$ as defined in section 2.6. A review of literature [IEE1] has shown that the value of λ for a TCSC should ideally lie between 2 and 4. The reactance of the inductor used in the original laboratory-scale TCSC power circuit design was chosen

to be relatively large in order to reduce the current ratings of the inductor and the thyristors [Mazibuko2]. The calculated value of λ for the existing TCSC parameters designed in [Mazibuko2] is 1.6 which is outside the range recommended in the literature.

A set of new inductors had already been constructed for developing a second version of the laboratory-scale TCSC by the time this thesis project began. The objective in this project was therefore to study what combinations of these newly-available TCR inductors could be used to improve the performance characteristics of the laboratory-scale TCSC. The new inductors had been designed with lower values of both reactance and resistance compared to the original TCR inductors. In this thesis project, the actual reactance and resistance values of the manufactured inductors were obtained by measurement. The measurement approach used was to use a low power factor wattmeter in conjunction with an ammeter and a voltmeter. Appendix E discusses the measurement procedure and associated calculations in greater detail.

The parameters of the newly manufactured inductors are shown in Table 6.1, with Inductor A being the parameters of the original TCR inductor shown also for comparison. The TCR inductor parameters shown in Table 6.1 were used in the detailed simulation model of the laboratory-scale TCSC that was developed using PSCAD in Chapter Three. The simulation studies were undertaken to determine which of the new inductors were the most suitable for use in the laboratory-scale TCSC.

Table 6.1: Parameters of the newly manufactured TCR inductors

	R_L	X_L	X_L/R_L	λ
Inductor A	**0.29 Ω**	0.828 Ω	2.855	1.6
Inductor B	**0.145 Ω**	0.414 Ω	2.855	2.225
Inductor C	**0.070 Ω**	0.127 Ω	1.806	4.015
Inductor D	0.098 Ω	0.196 Ω	2.00	3.235
Inductor E	0.075 Ω	0.159 Ω	2.133	3.59
Inductor F	0.097 Ω	0.276 Ω	2.855	2.725

6.3 Simulation Studies

The detailed TCSC simulation model that was developed in Chapter Three was used to determine which of the new TCR inductors manufactured were the most appropriate for use in the laboratory-scale TCSC. The detailed simulation model also allowed for measurement and insight into the electrical circuit variables of the simulated laboratory-scale TCSC. Specifically, this ensured that the current magnitudes could be observed and checked to ensure that they remained within the designed operating limits of the laboratory-scale TCSC. The detailed simulation model, for the various inductors under consideration, was used to obtain the capacitive reactance characteristic of the laboratory-scale TCSC as a function of the trigger angle. These were then used to evaluate and predict the performance of the laboratory-scale TCSC.

The capacitive reactance characteristics of the laboratory-scale TCSC that were obtained from the detailed simulation model for the various TCR inductors were also compared to the ideal TCSC capacitive reactance characteristic obtained by using the theoretical equation (2.5). The simulated capacitive reactance characteristics of the laboratory-scale TCSC were firstly obtained for the case with only the TCR inductor resistance represented in the detailed simulation model: this was to explicitly show the effect that the TCR inductor resistance has on the capacitive reactance characteristic of the laboratory-scale TCSC. Thereafter the forward volt drop of the thyristors was included in the detailed simulation model to obtain the full predicted capacitive reactance characteristics of the practical laboratory-scale TCSC for each inductor type.

In order to identify meaningful trends and conclusions from the results obtained, the TCR inductors listed in Table 6.1 were broadly divided into two groups. Firstly, TCR inductors A, B and F all have the same X/R ratio of 2.855, which also happens to be the highest possible X/R ratio that can be achieved with the currently-available inductors. Secondly, TCR inductors C, D and E all have, to varying degrees, lower X/R ratios than those TCR inductors in the aforementioned group, and they also

constitute the lowest possible TCR inductances that can be achieved with the currently-available inductors.

6.3.1 High X/R ratio TCR inductors

TCR inductors A, B, and F have been grouped together as the TCR inductors having the highest available X/R ratio. An inductor with an X/R ratio that was infinite would correspond to an ideal inductor, therefore a higher X/R ratio of the TCR inductor should mean better agreement between the capacitive reactance characteristic obtained from the detailed TCSC simulation model and the ideal capacitive reactance characteristic obtained using the theoretical equation (2.5). The simulated and theoretical (ideal) capacitive reactance characteristics of the laboratory-scale TCSC for TCR inductors A, B, and F are shown in Figures 6.1, 6.2 and 6.3 respectively.

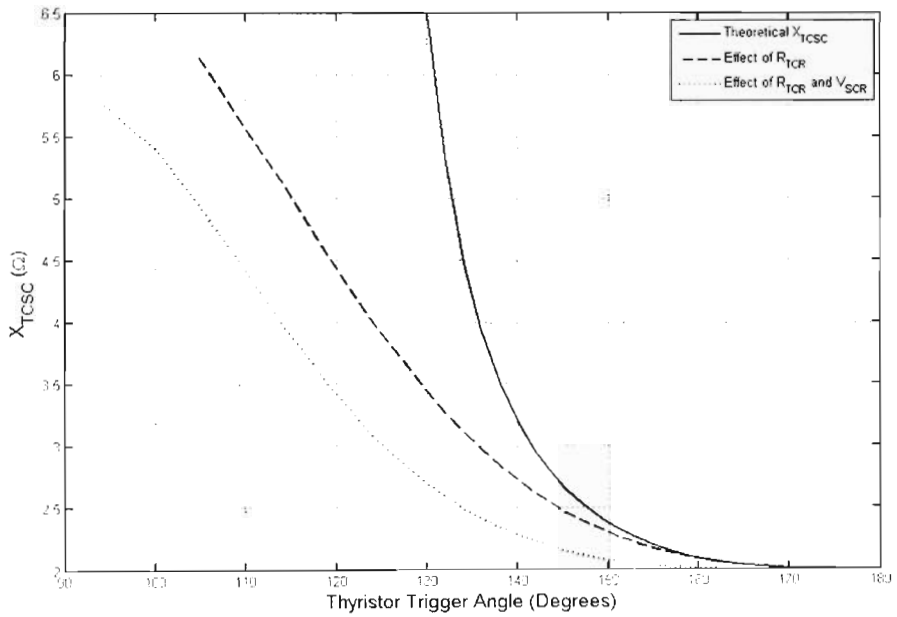

Figure 6.1: Predicted capacitive reactance characteristic of the laboratory-scale TCSC obtained for TCR inductor A.

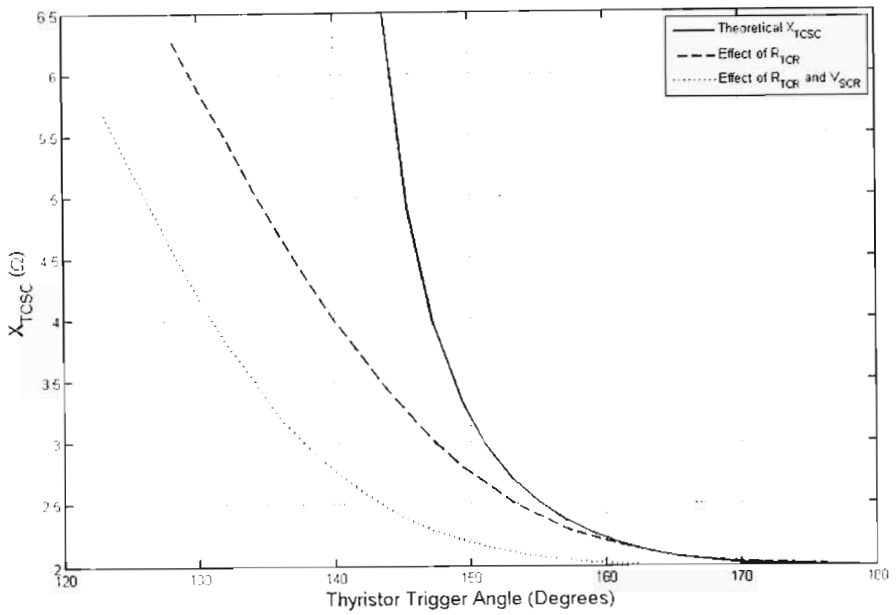

Figure 6.2: Predicted capacitive reactance characteristic of the laboratory-scale TCSC obtained for TCR inductor B.

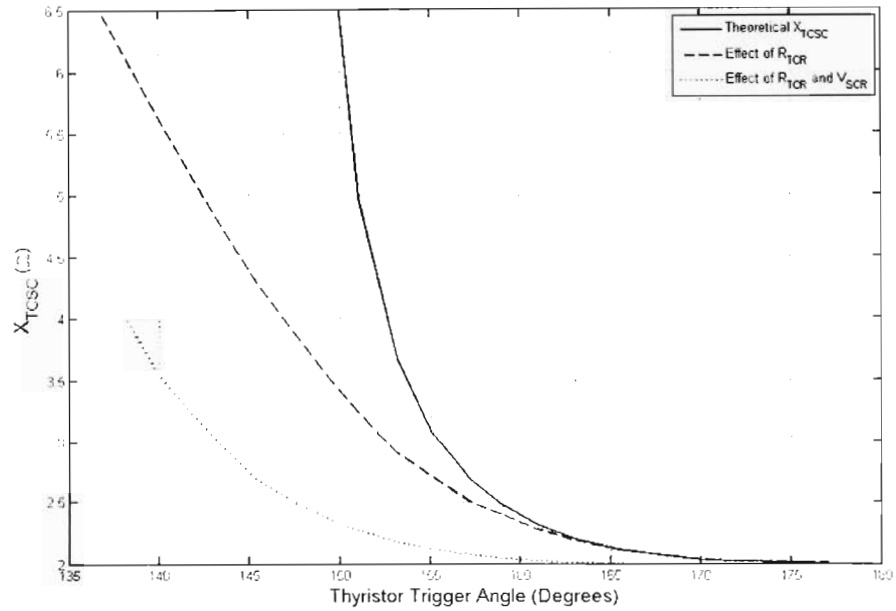

Figure 6.3: Predicted capacitive reactance characteristic of the laboratory-scale TCSC obtained for TCR inductor F.

Comparison of the results in Figures 6.1, 6.2, and 6.3 show that for a fixed X/R ratio of the TCR inductor, the steepness of the TCSC's reactance versus thyristor trigger

angle characteristic (both ideal and non-ideal) increases as the TCR inductance is reduced. However, Figures. 6.1, 6.2, and 6.3 also show that, for a fixed X/R ratio of the TCR inductor, the maximum attainable reactance from the non-ideal TCSC decreases as its TCR inductance value is reduced.

Both of these trends are consistent with findings reported in the literature by other authors [Ghosh1, Haro1, Helbing1, Matsuki1, Matsuki2, Mazibuko1]. For the laboratory TCSC, TCRs B and F constitute a moderate reduction in inductance from the value used in the initial prototype (TCR A), but without any reduction in the TCR's X/R ratio. For these cases, as the TCR inductance is decreased, the practical TCSC's variable reactance characteristic becomes steeper (and hence closer to the characteristics of a high-voltage TCSC) with a modest reduction in the practical operating range.

6.3.2 Low X/R ratio TCR inductors

The second group of TCR inductors considered were those with lower X/R ratios, meaning that this group of TCR inductors would be expected to show a more pronounced effect on the capacitive reactance characteristic of the laboratory-scale TCSC away from the ideal characteristics. The TCR inductors that have low X/R ratios are TCR inductors C, D, and E. The capacitive reactance characteristic of the laboratory-scale TCSC obtained for TCR inductors C, D, and E are shown in Figures 6.4, 6.5 and 6.6 respectively.

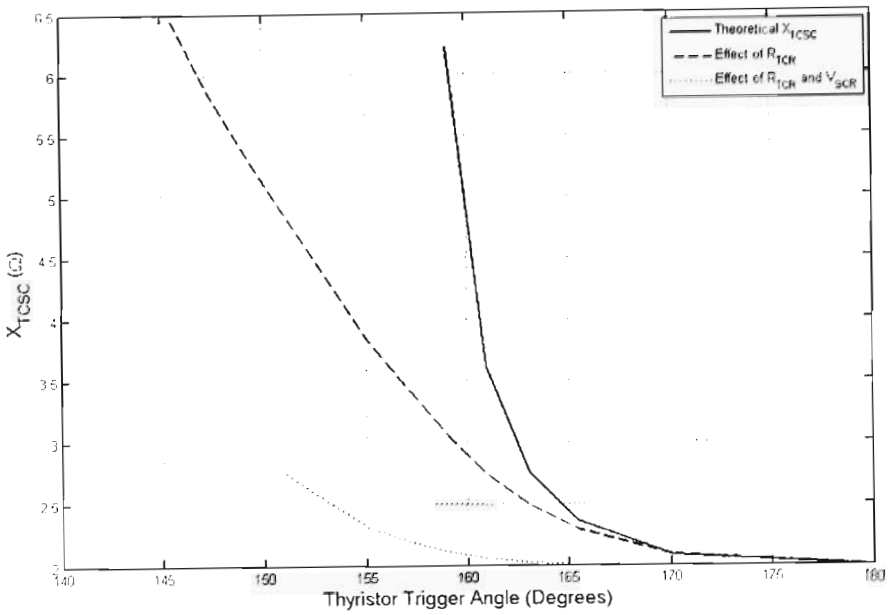

Figure 6.4: Predicted capacitive reactance characteristic of the laboratory-scale TCSC obtained for TCR inductor C.

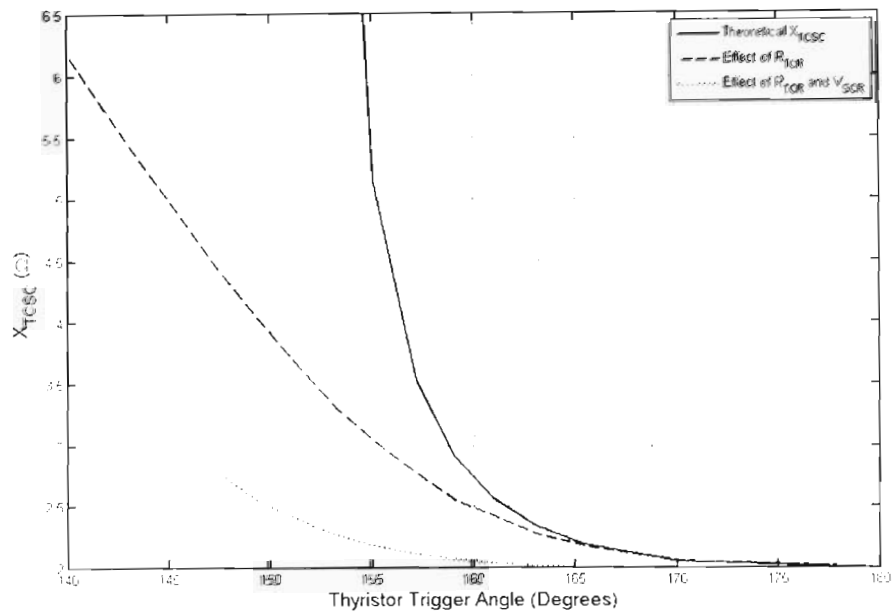

Figure 6.5: Predicted capacitive reactance characteristic of the laboratory-scale TCSC obtained for TCR inductor D.

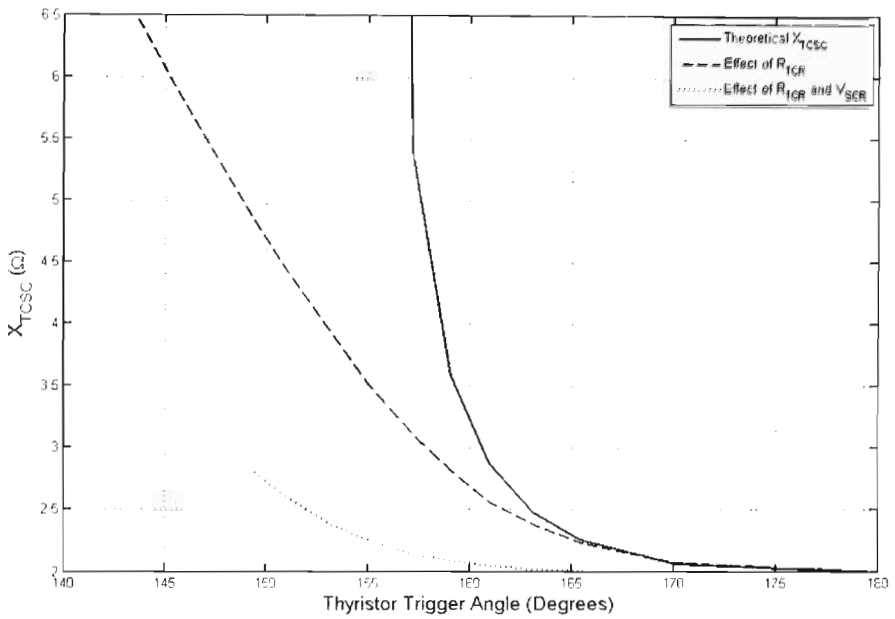

Figure 6.6: Predicted capacitive reactance characteristic of the laboratory-scale TCSC obtained for TCR inductor E.

Figures 6.4, 6.5, and 6.6 predict that with these inductors, the maximum attainable reactance from a non-ideal TCSC is severely restricted in each case; that is, the results predict that the laboratory TCSC would only be capable of increasing its reactance to 2.27 Ω before its phase locked loop triggering control loses synchronism. Although one would expect some further reduction in the practical operating range of the TCSC's variable reactance at the low values of TCR inductance in TCRs C, D and E, one would also expect the extent of this reduction to be dependent on the value of the inductance itself, as is the case in Figures 6.1, 6.2, and 6.3.

However, Figures 6.4, 6.5, and 6.6 predict that for all of these low values of TCR inductance, the upper limit of the practical TCSC's reactance range is 2.27 Ω, irrespective of the actual value of the inductance. A further interesting finding in the results is that when the volt drops of the thyristors are ignored in the analysis, but the TCR resistance is still included, the TCSC is able to operate at high values of reactance without loss of synchronism in its triggering controls for all values of TCR inductance considered.

The results therefore suggest that in a low voltage TCSC, the thyristor volt drops not only contribute to the non-ideal shape of the TCSC's reactance versus trigger angle characteristics, but can also contribute to restricting the range of TCSC reactance values that can be obtained in practice. In particular, the results show that in a low voltage TCSC, where the thyristor volt drops cannot be neglected, there is a limit to how low the value of TCR inductance can be made, as well as a limit to how low its X/R ratio can be, before the usable reactance range of the TCSC becomes severely restricted. The results also show that, conversely, if a TCSC is such that its thyristor volt drops can realistically be ignored, its usable reactance range is then significantly less sensitive to the inductance and X/R ratio of its TCR.

It should be pointed out that in all of the investigations considered here, the TCSC's phase locked loop triggering control controls in the detailed simulation model were operated at the same trigger angle resolution of 0.45°, (corresponding to the practical trigger angle resolution of the initial prototype TCSC triggering controller) and the phase locked loop gains were not re-designed for each new inductor value considered. Thus, the results can be used to predict the possible improvement in TCSC characteristics that could be obtained via power circuit parameter changes but without any improvement in triggering control resolution.

6.4 Conclusion

The initial capacitive reactance characteristics obtained for the original laboratory-scale TCSC showed that there was significant deviation between the theoretical (ideal) and practical characteristics. It was therefore undertaken to improve the performance of the laboratory-scale TCSC to obtain better agreement between the theoretical and practical capacitive reactance characteristics.

Firstly, it was noted that the performance of the prototype thyristor triggering controller was a contributing factor in the deviation between the theoretical and practical reactance characteristics of the laboratory-scale TCSC. A review of literature [Xu1] showed that for satisfactory control of a TCSC the thyristor trigger angle resolution needed to be less than 0.1°. The trigger angle resolution of the initial

prototype controller was measured to be 0.45° and therefore required improvement. The implementation of an improved hybrid TCSC triggering controller was discussed in Chapter Five.

Secondly, the reactance of the TCR inductor, for the original laboratory-scale TCSC power circuit design, was chosen to be large to minimise the required current ratings of the equipment in the research laboratory. However the literature [IEE1] shows that the ratio λ of the reactance of inductor to the reactance of the TCSC capacitor is an important quantity in the design of a TCSC and needs to be within a range of, 2 to 4. Since the value for the design parameter, λ, for the original power circuit parameters of the laboratory-scale TCSC was 1.6, it was decided to manufacture new TCR inductors to meet this specification.

Thirdly, detailed simulation studies in Chapter Three showed that the effect of the non-ideal components used in the laboratory-scale TCSC also contributed to the deviation between the theoretical and practical capacitive reactance characteristics of the laboratory-scale TCSC. Specifically the forward volt drop of the thyristors and the resistance of the TCR inductors were identified as having adverse effects on the performance of the laboratory-scale TCSC, however only the effect of the resistance of the TCR inductors could be minimised by component redesign. A set of new TCR inductors had been manufactured with these two considerations in mind. In considering which of these new inductors to use, the ratio of the reactance of the TCR inductor to the reactance of the TCSC capacitor needed to be within the limits as proposed in literature [IEE1] and the resistance of the inductors should be minimised.

The parameters of the new TCR inductors were then used in the detailed simulation model discussed in Chapter Three to determine their impact on the TCSC characteristics. The results were grouped for TCR inductors having a high X/R ratio and TCR inductors having a low X/R ratio. The results of the detailed simulation studies showed that the agreement between the theoretical and simulated capacitive reactance characteristics improved for the case of the inductors with a higher X/R ratio.

The simulation studies also showed that in the case of the TCR inductors with a low X/R ratio, the practical operating range of the laboratory-scale TCSC was drastically reduced. This finding makes TCR inductors with a low X/R ratio unattractive for use in the laboratory-scale TCSC. Finally, the results indicate that while a moderate reduction in TCR inductance value will indeed improve the practical characteristics of the laboratory TCSC, if the inductance is reduced too much, the low inductance itself, coupled with the poor X/R ratio, results in a restricted operating range of the TCSC.

Based on the investigations in Chapter Six TCR inductors B and E were chosen for use in the remainder of the laboratory-scale TCSC investigations in this thesis. Chapter Seven discusses the practical results obtained from the laboratory-scale TCSC when using TCR inductors B and E, and when simultaneously using the improved hybrid TCSC triggering controller with high thyristor trigger angle resolution.

Chapter Seven

Laboratory-scale TCSC performance tests using the hybrid controller

7.1 Introduction

Chapter Six discussed the influence of the TCR inductor parameters on the performance of the laboratory-scale TCSC. The results showed that an increase in the value of the TCR inductance resulted in a decrease in the steepness of the capacitive reactance versus trigger angle characteristic of the laboratory-scale TCSC. Hence by decreasing the value of the TCR inductance the steepness of the laboratory-scale TCSC's reactance characteristic can be increased. The reason for decreasing the value of the TCR inductance is to bring the design parameter λ for the laboratory-scale TCSC to within the range of 2 to 4 proposed in the literature [IEE1]. The calculated value of λ for the existing TCSC parameters designed in [Mazibuko2] is 1.6.

The simulation studies discussed in Chapter Six showed that if the resistance of the TCR inductor can be minimised then there will be improved agreement between the theoretical and practical variable capacitive reactance characteristics of the laboratory-scale TCSC. The outcome of the simulation studies, in Chapter Six, was the identification of which of the newly manufactured TCR inductors would result in better agreement between the theoretical and practical capacitive reactance characteristics of the laboratory-scale TCSC.

Chapter Seven presents practical results obtained from an improved laboratory-scale TCSC. The two areas of improvement are the use of TCR inductors that have parameters that are closer to an ideal inductor, and the use of the improved hybrid TCSC triggering controller as discussed in Chapter Five. Therefore the objectives of Chapter Seven are two fold: firstly to illustrate the improvement in the performance of the laboratory-scale TCSC due to the improved TCSC triggering controller; secondly,

to illustrate the improvement in the performance of the laboratory-scale TCSC due to the redesign of the TCR inductor parameters.

7.2 Measured performance of the hybrid TCSC triggering controller

The first objective was to measure the improvement in the performance of the laboratory-scale TCSC due to the improvement in the TCSC triggering controller. This was achieved firstly by using the prototype TCSC triggering controller and then, secondly the improved hybrid TCSC triggering controller to individually control the operation of the laboratory-scale TCSC with its original power circuit design parameters. This would allow for comparison of the results obtained for the two different controllers and would show any improvements in the performance of the hybrid TCSC triggering controller. However, the focus will be on the results obtained when the hybrid TCSC triggering controller was used to control the operation of the laboratory-scale TCSC.

7.2.1 Steady state measured time domain results

Firstly, the prototype TCSC triggering controller was connected to the laboratory-scale TCSC. The prototype TCSC triggering controller was then used to obtain the steady state time domain waveforms of TCSC capacitor voltage, transmission line current, and TCR current, of the laboratory-scale TCSC at a thyristor trigger angle, α, of 131°. The prototype TCSC triggering controller was then disconnected from the laboratory-scale TCSC and the hybrid TCSC triggering controller was then connected to the laboratory-scale TCSC. The hybrid TCSC triggering controller was now used to obtain the steady state time domain waveforms of TCSC capacitor voltage, transmission line current, and TCR current, of the laboratory-scale TCSC at a thyristor trigger angle, α, of 131°.

For comparison purposes, the detailed simulation model developed in Chapter Three was also used to obtain the steady state time domain waveforms of TCSC capacitor voltage, transmission line current, and TCR current of the laboratory-scale TCSC at a

thyristor trigger angle, α, of 131°. The simulation model was based on the original power circuit design parameters of the laboratory-scale TCSC and the time step for the simulation model was chosen to be 5 μs, which corresponded to the effective sampling period of the hybrid TCSC triggering controller. Figures 7.1, 7.2 and 7.3 show the steady state results obtained from the simulation model, and the practical results when the prototype TCSC triggering controller, and then the hybrid TCSC triggering controller was used to control the operation of the laboratory-scale TCSC.

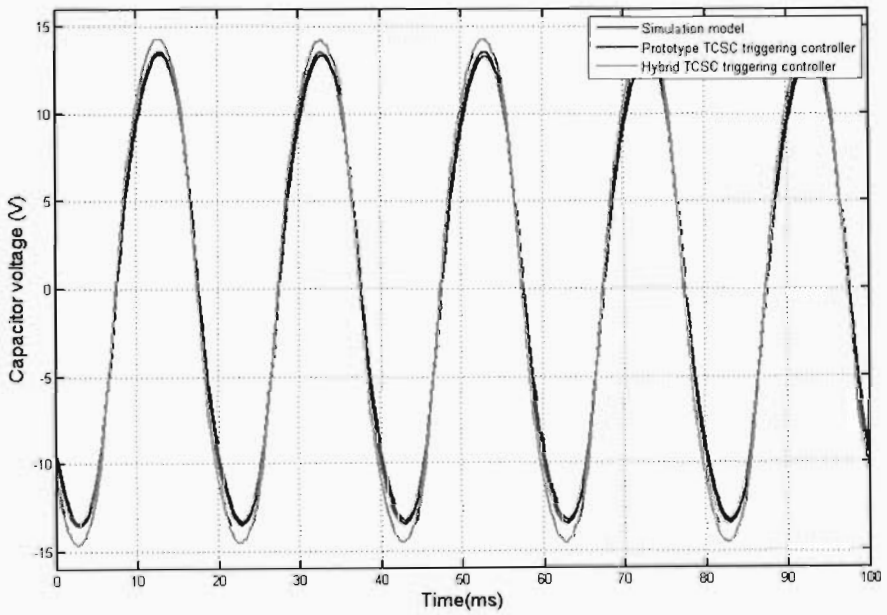

Figure 7.1: Simulated and measured time domain waveforms of the TCSC capacitor voltage at α = 131°

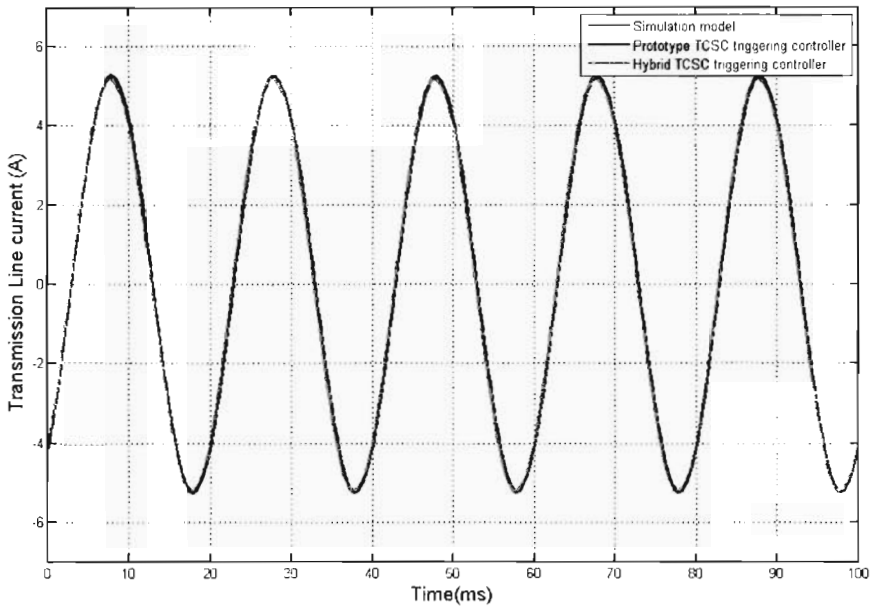

Figure 7.2: Simulated and measured time domain waveforms of the transmission line current at $\alpha = 131°$

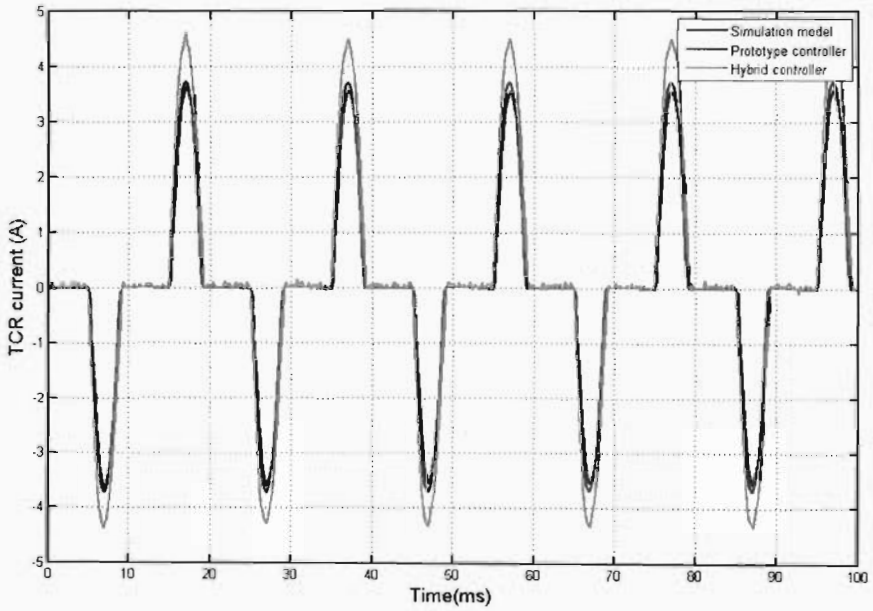

Figure 7.3: Simulated and measured time domain waveforms of the TCR current at $\alpha = 131°$

Figures 7.1, 7.2 and 7.3 show that in all three instances (simulation, prototype controller, and hybrid controller), the individual steady state time domain waveforms

(TCSC capacitor voltage, transmission line current, ad TCR current) are repetitive with respect to time. This observation demonstrates that in the three instances the laboratory-scale TCSC operates in a stable manner. But more specifically the results shown in Figures 7.1, 7.2, and 7.3 demonstrate that the hybrid TCSC triggering controller is capable of controlling the operation of the actual laboratory-scale TCSC.

Figure 7.3 shows that for the case for when the hybrid TCSC triggering controller was used, the magnitude of the TCR current is 22 % higher which resulted in a 6.5 % increase in TCSC capacitor voltage, as shown in Figure 7.1. The reason for the difference in the TCR current measurements will become evident in the following section when the capacitive reactance characteristic of the laboratory-scale TCSC is discussed.

7.2.2 Measured capacitive reactance characteristic of the original laboratory-scale TCSC

The steady state results presented in the previous section allowed for the comparison of the performance of the hybrid TCSC triggering controller and prototype TCSC triggering controller at a specific thyristor trigger angle of 131°. In order to assess the overall performance of the hybrid TCSC triggering controller, the capacitive reactance characteristic versus thyristor trigger angle of the laboratory-scale TCSC was obtained across the operating range of the laboratory-scale TCSC. The characteristics of the laboratory-scale TCSC were first tested using the prototype TCSC triggering controller and then using the hybrid TCSC triggering controller.

The capacitive reactance characteristic of the laboratory-scale TCSC was obtained by capturing the steady state time domain waveforms of the TCSC capacitor voltage and the transmission line current at several thyristor trigger angles. A Fast Fourier Transform (FFT) was performed on these individual waveforms to obtain the fundamental frequency (50 Hz) magnitudes of the TCSC capacitor voltage and transmission line current. The phase difference at the fundamental frequency (50 Hz) between the TCSC capacitor voltage and transmission line current was also calculated. The capacitive reactance of the laboratory-scale TCSC was calculated from these three quantities (TCSC capacitor voltage, transmission line current, and the phase difference).

A similar method to the one discussed above was used to obtain the capacitive reactance characteristic of the laboratory-scale TCSC using the detailed simulation model. The simulation studies were conducted for the ideal and non-ideal cases. For the non-ideal case the simulation model took into account the TCR inductor resistance, the forward volt drop of the thyristors and the effect of the sampling period of the hybrid TCSC triggering controller. Figure 7.4 shows the capacitive reactance versus thyristor trigger angle characteristic of the laboratory-scale TCSC obtained from the simulation studies (ideal and non-ideal), and from laboratory experiments using both the prototype and hybrid TCSC triggering controllers. The theoretical (ideal) capacitive reactance characteristic versus thyristor trigger angle for the laboratory-scale TCSC is also shown in Figure 7.4.

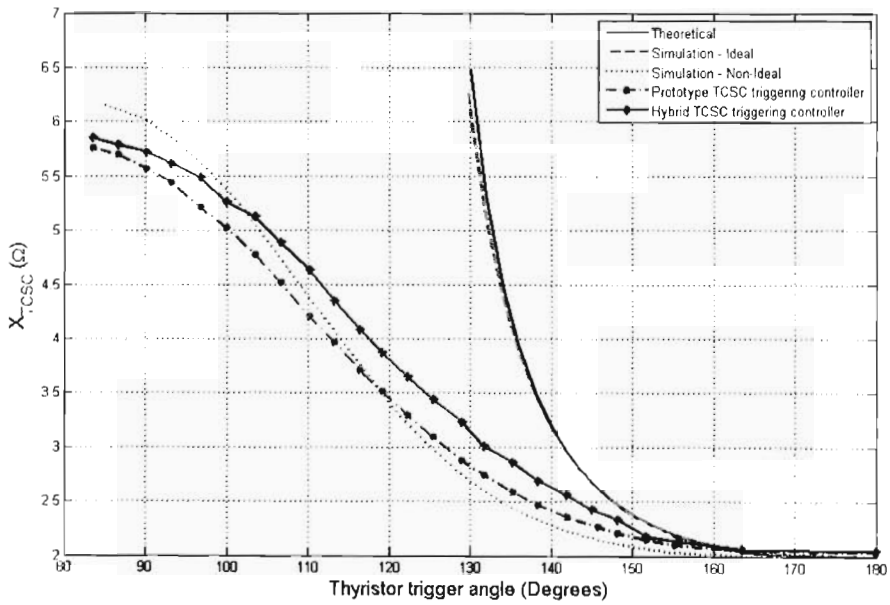

Figure 7.4: Capacitive reactance characteristic of the laboratory-scale TCSC for the prototype controller and the hybrid TCSC thyristor controller.

Figure 7.4 shows that for the case when the hybrid TCSC triggering controller was used to control the operation of the laboratory-scale TCSC, the capacitive reactance characteristic obtained lies above the capacitive reactance characteristics obtained from the non-ideal simulation studies and that obtained when the prototype TCSC triggering controller was used to control the operation of the laboratory-scale TCSC. This observation is a reflection of the higher magnitudes of the TCSC capacitor

voltage (6.5 % increase) and TCR current (22 % increase) seen in the time domain waveforms presented in the previous section.

However, the most important observation of the results shown in Figure 7.4 is that the measured capacitive reactance characteristic of the laboratory-scale TCSC is closer to the ideal theoretical prediction when the hybrid TCSC triggering controller is used to control the operation of the laboratory-scale TCSC. This improvement in the capacitive reactance characteristic reflects an improvement in the performance of the laboratory-scale TCSC, which can be solely attributed to the hybrid TCSC triggering controller.

The improved agreement between the measured capacitive reactance characteristic obtained for the laboratory-scale TCSC when the hybrid TCSC triggering controller was used and the theoretical capacitive reactance characteristic of the laboratory-scale TCSC demonstrates that the performance of the laboratory-scale TCSC has been improved by using the hybrid TCSC triggering controller. The main improvement of the hybrid TCSC triggering controller over the prototype TCSC triggering controller was to remove the dependency of the resolution of the thyristor triggering pulses on the sampling period of the controller and hence trigger the thyristors consistently and accurately at the correct thyristor trigger angle. The final step in proving the new hybrid controller was to use it to perform step changes in the commanded thyristor trigger angle using the laboratory-scale TCSC.

7.2.3 Step responses using the hybrid controller on the original laboratory-scale TCSC power circuit design

The previous two sections showed that the steady state performance of the hybrid TCSC triggering controller is superior to that of the prototype TCSC triggering controller. The final test was to check the performance of the hybrid TCSC triggering controller under dynamic conditions, which would demonstrate the hybrid TCSC triggering controller's ability to dynamically change the capacitive reactance of the laboratory-scale TCSC. The dynamic tests were performed using the original laboratory-scale TCSC power circuit design and the hybrid TCSC triggering controller. The step responses were conducted for changes in thyristor trigger angle, α, between 98° and 130°. Figures 7.5, 7.6 and 7.7 show the response of the

laboratory-scale TCSC to step changes in the thyristor trigger angle, α, from 130° to 98°; further step response waveforms are shown in Appendix F.

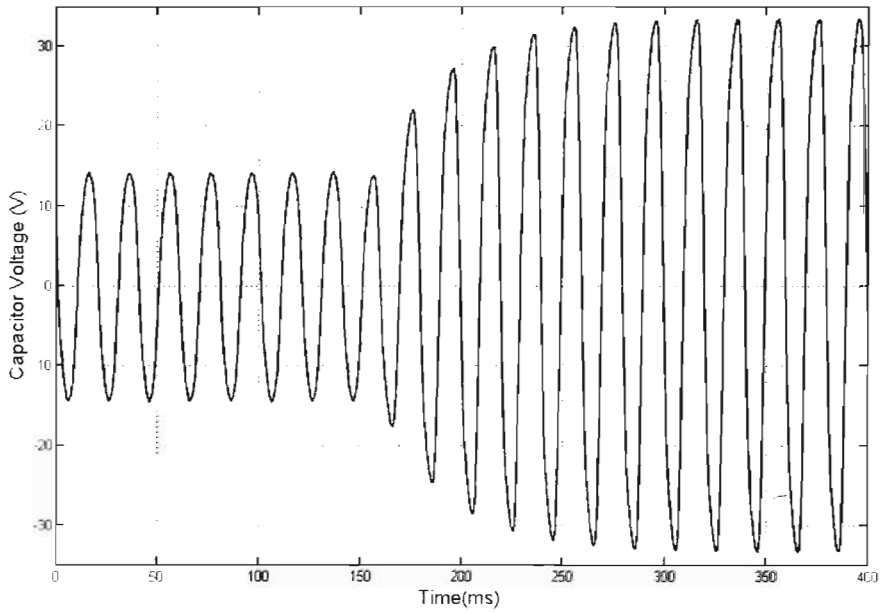

Figure 7.5: TCSC capacitor voltage waveform for a step in α from 130° to 98°

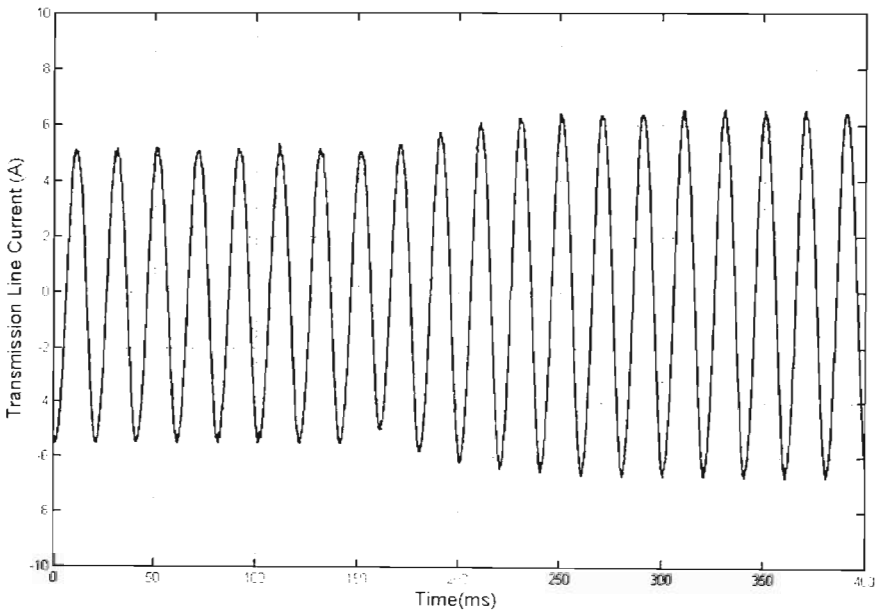

Figure 7.6: Transmission line current waveform for a step in α from 130° to 98°

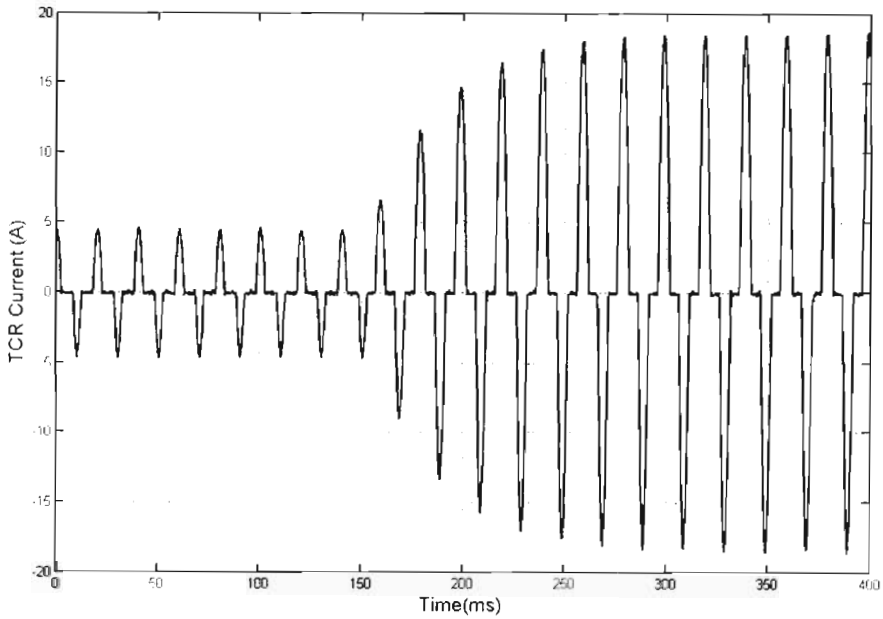

Figure 7.7: TCR current waveform for a step in α from 130° to 98°

Figures 7.5, 7.6, and 7.7 show the time domain waveforms of the TCSC capacitor voltage, transmission line current and TCR current respectively. Figure 7.7 shows the response of the TCR current to a step change in the thyristor trigger angle. Figure 7.7 shows that the magnitude and duration of the TCR current pulses increase in response to the step change in the thyristor trigger angle. The increase in the TCR current magnitude by 300 % results in an increase in the TCSC capacitor voltage by 138 %, as evident in Figure 7.5, which in turn causes an increase of 26 % in the magnitude of the transmission line current, as seen in Figure 7.6. Therefore, the waveforms shown in Figures 7.5, 7.6, and 7.7 demonstrate the ability of the hybrid TCSC triggering controller to dynamically change the capacitive reactance of the laboratory-scale TCSC.

Another important outcome of the dynamic tests conducted on the laboratory-scale TCSC using the hybrid TCSC triggering controller is that the results demonstrate that the laboratory-scale TCSC operates in a stable manner following a step change in the thyristor trigger angle. This specifically means that the PLL algorithm does not lose synchronism with the transmission line currents which could lead to spurious triggering of the thyristors.

The results presented thus far have proved that the performance of the hybrid TCSC triggering controller is superior to that of the prototype TCSC triggering controller. This is seen as an improvement in the agreement between the theoretical and measured capacitive reactance characteristics of the laboratory-scale TCSC when the hybrid TCSC triggering controller was used. The step response tests then demonstrated that the hybrid TCSC triggering controller as a whole (including software algorithms) is capable of stable operation under dynamic conditions. Hence the hybrid TCSC triggering controller succeeded the prototype TCSC triggering controller and is now used to check the improvement in the performance of the laboratory-scale TCSC due to the redesign of the laboratory-scale TCSC's TCR inductor parameters.

7.3 Laboratory-scale TCSC performance tests using new TCR inductors

Chapter Six revisited the design of the original power circuit of the laboratory-scale TCSC by examining newly manufactured TCR inductors that had lower inductance and higher X/R ratios as compared to the TCR inductor used in the original design of the power circuit of the laboratory-scale TCSC. The reasons for the redesign were firstly due to the findings of Chapter Three which showed that the TCR inductor resistance had a negative effect on the performance of the laboratory-scale TCSC. Therefore it was concluded that TCR inductors with lower resistance or higher X/R ratios would result in improved performance of the laboratory-scale TCSC.

The second reason for the redesign of the original laboratory-scale TCSC power circuit design was that the design parameter, λ, for the original laboratory-scale TCSC was 1.6. A review of literature [IEE1] has shown that the value of λ for a TCSC should ideally lie between 2 and 4. Therefore it was concluded that for the design parameter, λ, of the laboratory-scale TCSC to lie within the range of 2 and 4, the inductance of the TCR inductor had to be reduced. The simulation studies in Chapter Six then identified two newly manufactured TCR inductors that resulted in better predicted performance of the simulated laboratory-scale TCSC.

The two inductors that were identified for further investigations were TCR inductor B and TCR inductor E. The parameters of TCR inductor B and TCR inductor E are shown in Table 7.1 along with the parameters of TCR inductor A, which was used in the original power circuit design of the laboratory-scale TCSC.

Table 7.1: Parameters of the TCR inductors that will be used in further studies

	R_L	X_L	X_L/R_L	λ
Inductor A	0.29 Ω	0.828 Ω	2.855	1.6
Inductor B	0.145 Ω	0.414 Ω	2.855	2.225
Inductor E	0.075 Ω	0.159 Ω	2.133	3.59

7.3.1 Practical measurements using TCR inductor B

The laboratory-scale TCSC was, firstly, reconnected using TCR inductor B instead of TCR inductor A. Time domain waveforms of the TCSC capacitor voltage, transmission line current and TCR current were then measured at a thyristor trigger angle, $\alpha = 131°$. The detailed simulation model was also used to obtain the TCSC capacitor voltage, transmission line current and TCR current for TCR inductor B. The resulting waveforms are shown in Figures 7.8, 7.9, and 7.10.

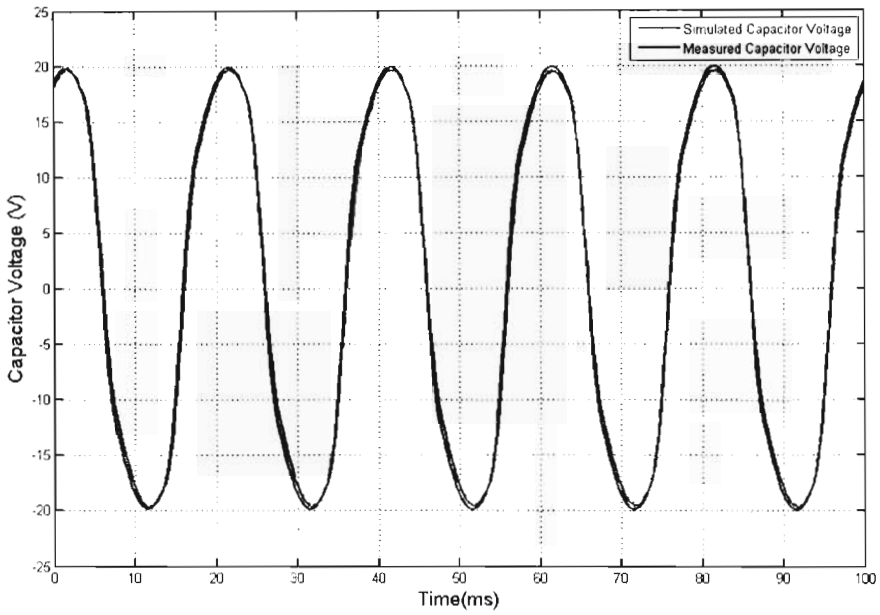

Figure 7.8: Simulated and measured time domain waveforms of the series TCSC capacitor voltage obtained when using TCR inductor B

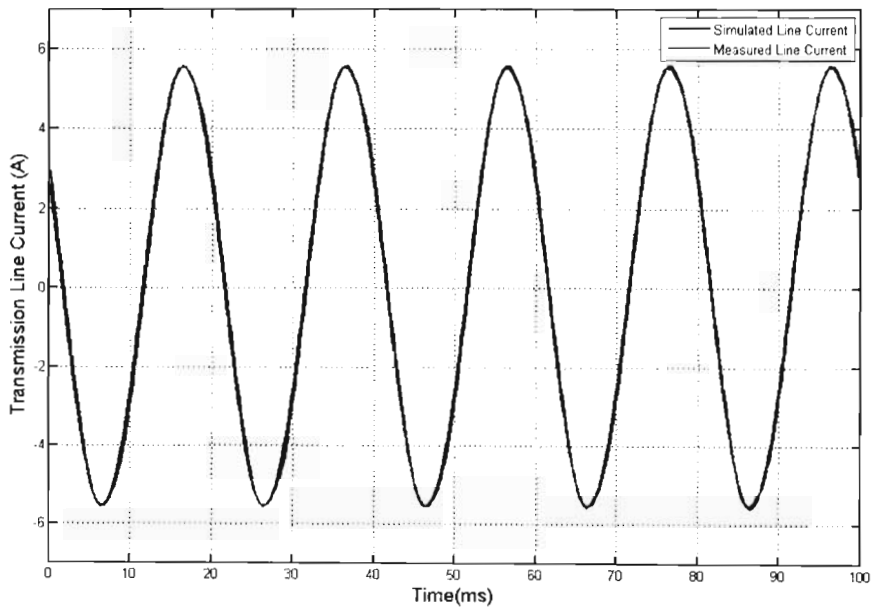

Figure 7.9: Simulated and measured time domain waveforms of the transmission line current obtained when using TCR inductor B

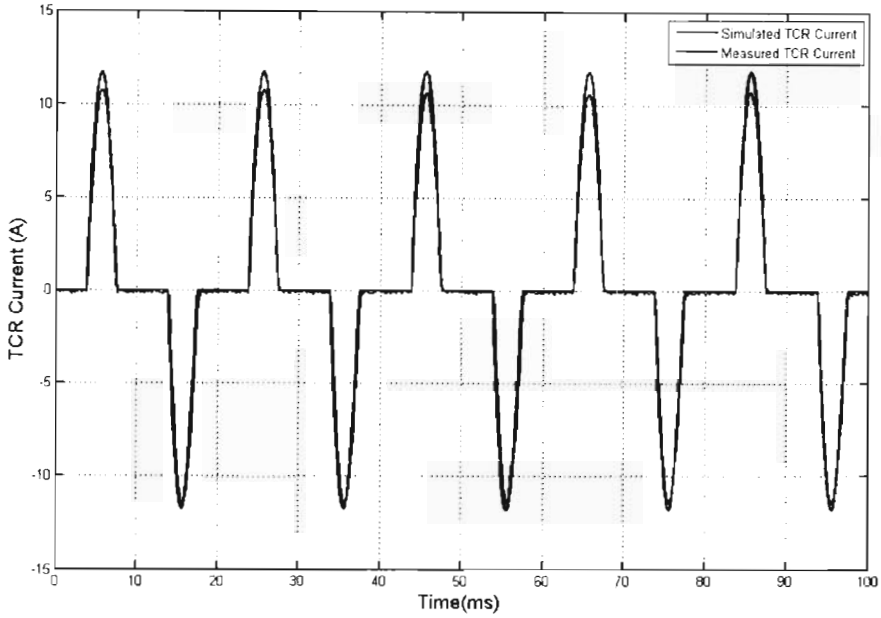

Figure 7.10: Simulated and measured time domain waveforms of the TCR current obtained when using TCR inductor B

Figures 7.8, 7.9, and 7.10 show the time domain waveforms obtained using the detailed simulation model and the measured time domain waveforms of the laboratory-scale TCSC when using TCR inductor B. The figures show excellent agreement between the time domain waveforms obtained from the detailed simulation model and practical measurements, which further proves the correct operation of the improved TCSC thyristor triggering controller and the laboratory-scale TCSC itself.

The measured capacitive reactance characteristic of the laboratory-scale TCSC with TCR inductor B was obtained once again by using the process described in section 7.2.2. The capacitive reactance characteristic of the laboratory-scale TCSC was also obtained using the same procedure on the detailed simulation model. The results are plotted in Figure 7.11.

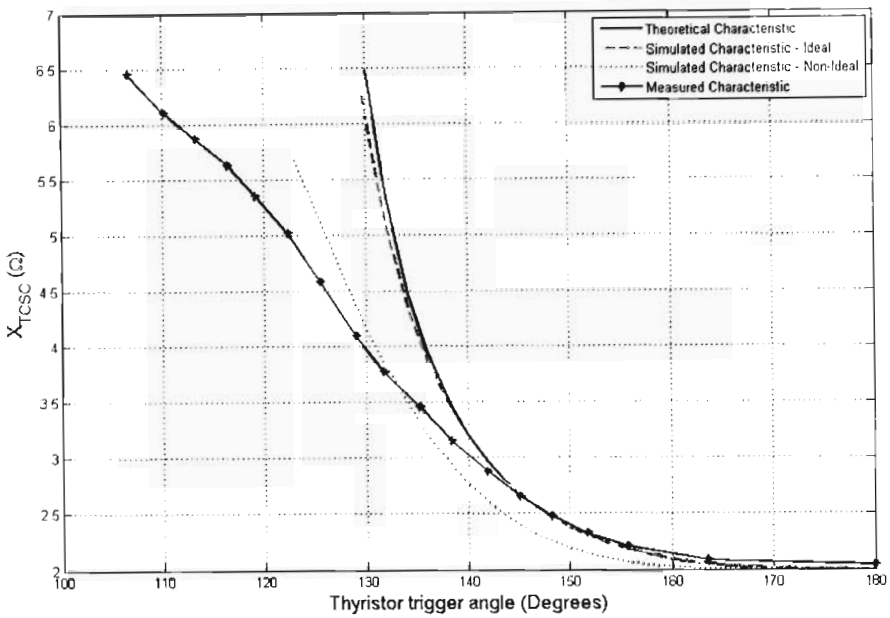

Figure 7.11: Capacitive reactance characteristic of the laboratory-scale TCSC using TCR inductor B

Figure 7.11 shows the capacitive reactance characteristic of the laboratory-scale TCSC across its operating range obtained when using TCR inductor B. The interesting and most important observation in Figure 7.11 is that it shows there is very close agreement at higher thyristor trigger angles between the theoretical and measured capacitive reactance characteristics. However, as the thyristor trigger angle is decreased the measured capacitive reactance characteristic diverges from the theoretical capacitive reactance characteristic but with both characteristics following a similar trend.

The agreement, at higher thyristor trigger angles, between the measured and theoretical capacitive reactance characteristics reflects an improvement in the performance of the laboratory-scale TCSC itself due to the use of TCR inductor B. It must be noted that both the original inductor, TCR inductor A, and TCR inductor B both have the same X/R ratio of 2.855. More interestingly when TCR inductor A, having a reactance of 0.828Ω, was used in the laboratory-scale TCSC, the value of the design parameter, λ, is 1.6 for the laboratory-scale TCSC. By contrast when the TCR inductor B, having a reactance of 0.414 Ω was used in the laboratory-scale TCSC the

design parameter, λ, had a value of 2.225, which is within the range of 2 and 4 as proposed in literature [IEE1].

Hence the results in Figure 7.11 show that for a given X/R ratio, the performance of the laboratory-scale TCSC is improved by selecting a TCR inductor with a 50 % lower inductance. However the reactance of the TCR inductor must be chosen such that the design parameter, λ, for the laboratory-scale TCSC is within 2 and 4 as proposed in literature [IEE1]. Following the tests conducted using TCR inductor B, TCR inductor E was connected to the laboratory-scale TCSC.

7.3.2 Practical measurements using TCR inductor E

The other TCR inductor identified in Chapter Six for further tests was the TCR inductor having an X/R ratio of 2.133 and a reactance of 0.159Ω. The laboratory-scale TCSC was reconnected using TCR inductor E in order to perform practical measurements. The first step was to verify the steady state operation of the laboratory-scale TCSC using TCR inductor E, by comparing the measured time domain waveforms with the time domain waveforms obtained from the detailed simulation model. The time domain waveforms of the TCSC capacitor voltage, transmission line current, and TCR current obtained from the simulation studies and the laboratory measurements are shown in Figures 7.12, 7.13 and 7.14.

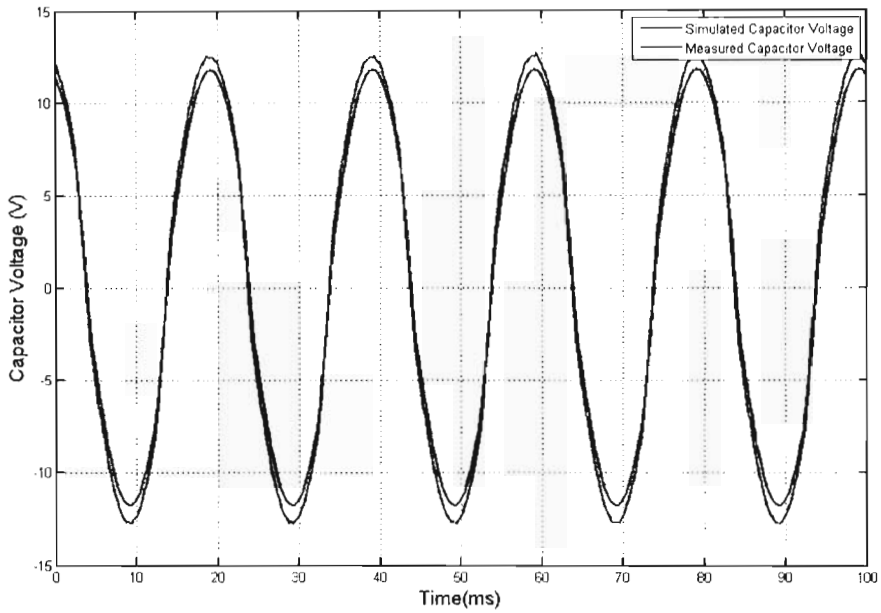

Figure 7.12: Simulated and measured time domain waveforms of the series TCSC capacitor voltage obtained when using TCR inductor E

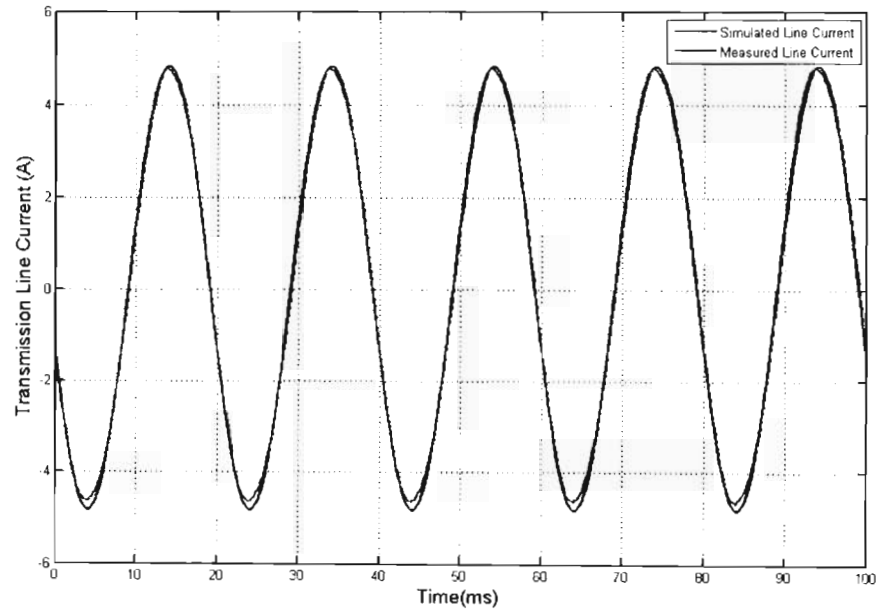

Figure 7.13: Simulated and measured time domain waveforms of the transmission line current obtained when using TCR inductor E

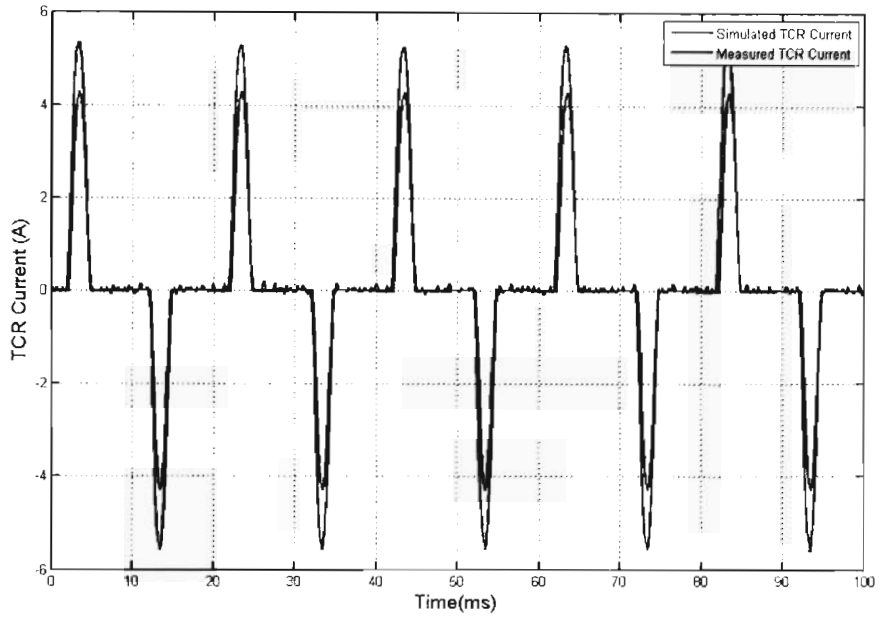

Figure 7.14: Simulated and measured time domain waveforms of the TCR current obtained when using TCR inductor E

Figure 7.14 shows that the magnitude of the TCR current pulses is larger by 25.6 % in the case of the measured results as compared to the results obtained from the simulation studies. Figure 7.12 shows that the magnitude of the TCSC capacitor voltage is also larger by 7 % in the case of the measured results which is due to the larger TCR current. The test to determine if there was an improvement in the performance of the laboratory-scale TCSC due to the use of TCR inductor E was to compare the theoretical (ideal) and measured capacitive reactance characteristic versus thyristor trigger angle of the laboratory-scale TCSC across its operating range.

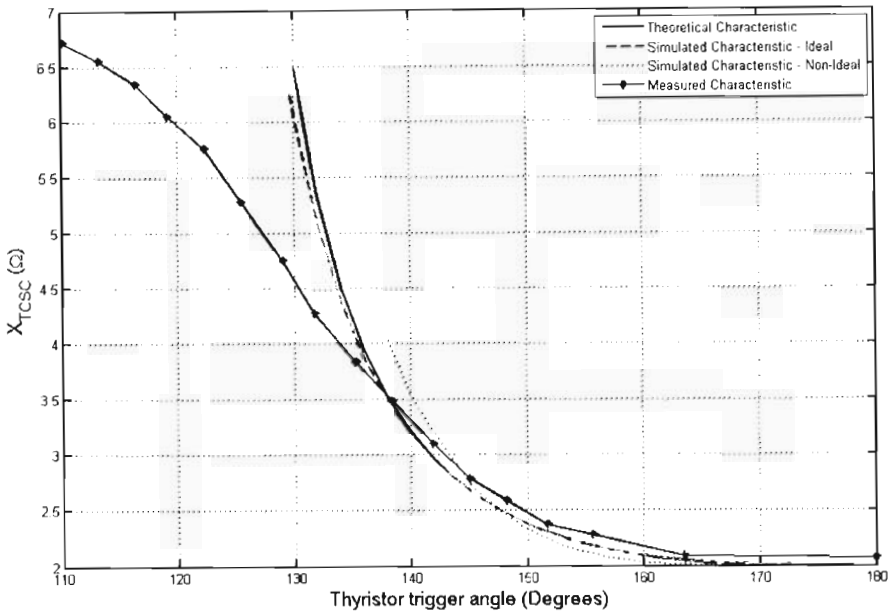

Figure 7.15: Capacitive reactance characteristic of the laboratory-scale TCSC using TCR inductor E

Figure 7.15 now shows the theoretical, simulated, and measured capacitive reactance versus thyristor trigger angle characteristic of the laboratory-scale TCSC when the TCR inductor E was used. Figure 7.15 shows that the measured capacitive reactance characteristic shows good agreement with the theoretical (ideal) and simulated capacitive reactance characteristics of the laboratory-scale TCSC at high values of thyristor trigger angle. At lower thyristor trigger angles the measured capacitive reactance characteristic of the laboratory-scale TCSC begins to diverge from the theoretical capacitive reactance characteristic, but still maintaining the same trend of increasing capacitive reactance with decreasing thyristor trigger angle.

Figure 7.11 shows that the measured capacitive reactance characteristic obtained when using TCR inductor B begins to diverge from the theoretical capacitive reactance characteristic at a TCSC capacitive reactance of approximately 2.75 Ω. Figure 7.15 shows that for TCR inductor E, the measured capacitive reactance characteristic of the laboratory-scale TCSC begins to diverge from the theoretical capacitive reactance characteristic at a TCSC capacitive reactance of approximately 3.5 Ω. For the case of the original design of the laboratory-scale TCSC power circuit

the divergence of the measured capacitive reactance characteristic from the theoretical capacitive reactance characteristic is at approximately 2.2 Ω.

The observations, regarding the divergence of the measured capacitive reactance characteristic from the theoretical capacitive reactance characteristic, show that the highest point of divergence occurred when the TCR inductor E was used. TCR inductor E was also the TCR inductor with the lowest reactance of 0.159 Ω. Therefore it can be concluded that of the three inductors (TCR inductors A, B, and E) the performance of the TCSC is the best when using TCR inductor E.

From the results obtained for the three TCR inductors it can be seen that the parameters of the TCR inductor play an important role in a low-voltage TCSC which ultimately affects the performance of the low-voltage TCSC. However the results also showed that the effects resulting from the TCR inductor can be minimised.

7.4 Conclusion

Chapters Five and Six discussed ways in which the performance of the laboratory-scale TCSC could be improved. Chapter Five discussed the implementation of a hybrid TCSC triggering controller which generates the thyristor triggering signals with a higher resolution than the prototype TCSC triggering controller. Chapter Six analysed newly manufactured TCR inductors and identified two of these inductors that would result in improved performance of the laboratory-scale TCSC. Chapter Seven has now presented the results obtained from practical tests conducted on the laboratory-scale TCSC to confirm the improvements obtained from the enhancements described in Chapters Five and Six.

Firstly, the improved performance of the hybrid controller was proved by comparing the capacitive reactance characteristics of the laboratory-scale TCSC when the prototype controller and the hybrid controller were used in-turn to control the operation of the laboratory-scale TCSC. The capacitive reactance characteristic obtained when the hybrid controller was used showed better agreement to the theoretical capacitive reactance characteristic of the laboratory-scale TCSC as

compared to when the prototype controller was used, hence proving that the performance of the hybrid controller is superior to that of the prototype controller.

Secondly the practical capacitive reactance characteristics of the laboratory-scale TCSC were obtained for the two new TCR inductors identified in Chapter Six. The first TCR inductor, TCR inductor B, has lower inductance and resistance as compared to the TCR inductor used in the original laboratory-scale TCSC power circuit design. The measured capacitive reactance characteristic of the laboratory-scale TCSC obtained when TCR inductor B is used shows better agreement with the theoretical capacitive reactance characteristic as compared to the capacitive reactance characteristic obtained for the original parameters of the laboratory-scale TCSC power circuit design.

The second TCR inductor, TCR inductor E, had the lowest reactance and resistance of the two inductors considered for further studies. The practical capacitive reactance characteristic obtained for the laboratory-scale TCSC when TCR inductor E is used shows the best agreement with the theoretical capacitive reactance characteristic.

The results obtained from the practical results matched the results obtained from simulation, which was that the non ideal effects of the TCR inductor can be minimised in a low voltage TCSC by carefully choosing the TCR inductor. Chapter Eight now looks at the case where the non ideal conditions of the low voltage laboratory-scale TCSC are eliminated by using a real time simulator to simulate a high voltage TCSC.

Chapter Eight

Real Time Digital Simulator testing

8.1 Introduction

Chapter Seven presented the practical results obtained from the laboratory-scale TCSC. Firstly the practical results proved that the hybrid controller was capable of controlling the operation of the laboratory-scale TCSC. It also proved that the performance of the laboratory-scale TCSC improved when the hybrid controller is used. Secondly the practical results obtained in Chapter Seven showed that the negative effects of the TCR inductor parameters on the performance of a low voltage laboratory-scale TCSC can be minimised by careful choice of the TCR inductor. Specifically the results contained in Chapter Seven showed that the performance of the laboratory-scale TCSC improved when the inductance of the TCR inductor was reduced, such that the design parameter, λ, for the laboratory-scale TCSC was kept within the limits proposed in literature [IEE1].

Chapter Eight now goes on to present results obtained when a real time digital simulator (RTDS) is used to simulate a high voltage TCSC, so that the non-ideal effects evident in a low voltage laboratory-scale TCSC (thyristor forward volt drop and TCR inductor resistance) become negligible. The RTDS is a simulator that is capable of real time simulation of a power system. The other important feature of the RTDS is that the RTDS has external input/output capabilities, meaning that selected internal simulation variables can be made available signals as external signals to drive external controllers, and external signals can be imported back into the RTDS simulation model. The significance of the ability of the RTDS to have external interface capability means that the hybrid TCSC triggering controller can be used to control the operation of a more realistic, high voltage TCSC, simulated in real-time.

The high voltage TCSC that was modelled on the RTDS was chosen to be the 230 kV Kayenta TCSC located in the USA [Christ11]. The capacitive reactance operating

range of the Kayenta TCSC is -15j Ω to -j45 Ω. For the purposes of the RTDS simulation studies in this thesis project the Kayenta TCSC is connected to a two area, four generator system [Kundur1] in the RTDS simulation model. This two area, four generator study system, is well known for its use in investigations of inter-area mode oscillations and a real-time simulator model of this system had already been developed for the RTDS [Rigby2] to investigate the ability of the TCSC to damp inter-area mode oscillations. The same power oscillation damping controller designs already developed in [Rigby2] were used in the work in this chapter, in conjunction with several different input control signals to use the TCSC to damp the inter-area mode oscillations of the study system. However, in the tests presented in this chapter, the triggering control of the TCSC was carried out using the hybrid TCSC triggering controller scheme of Chapter Five, connected hardware-in-loop with the RTDS simulator, whereas in the results in [Rigby2] the TCSC triggering controls were implemented as part of the real-time simulation itself.

8.2 Testing environment

The RTDS is a simulator that is capable of real time simulation of a power system. A simulation model of the study system is developed and downloaded to a multiple array of processing cards that solve the simulation model in real time. The important feature of the RTDS is that it has external input/output capabilities so that selected internal simulation variables can be made available externally as real-time analogue outputs via digital-to-analogue converters (DACs), and external signals can be imported into the simulation via digital inputs. The significance of the ability of the RTDS to have external interface capability means that the hybrid TCSC triggering controller can be used to control the operation of a high voltage TCSC, with realistic parameters, simulated in real time.

Figure 8.1 shows the connection of the hybrid TCSC triggering controller to the RTDS. The hybrid TCSC triggering controller was connected in a closed loop manner and was used to generate the thyristor triggering signals to the simulated TCSC via the high speed digital inputs of the RTDS. The DACs on the RTDS were used to

provide scaled outputs of the transmission line currents which were used by the PLL algorithm on board the hybrid TCSC triggering controller.

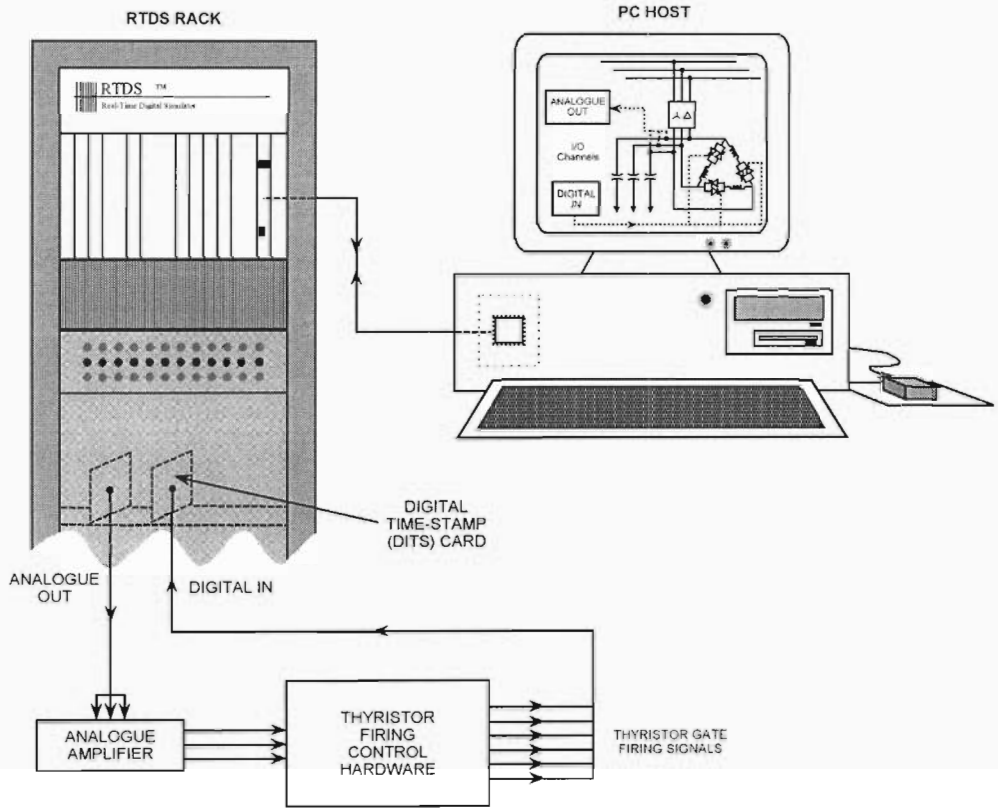

Figure 8.1: Figure showing the connections between the hybrid TCSC triggering controller and the RTDS [Rigby2]

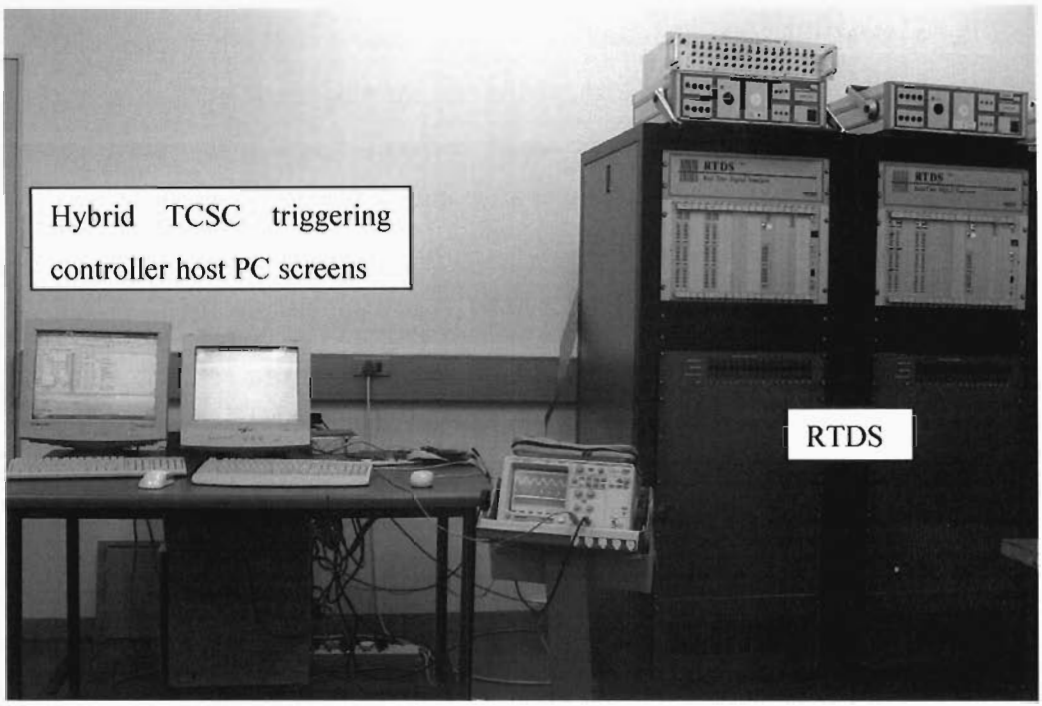

Figure 8.2: Photograph of the RTDS and the hybrid TCSC triggering controller

The real time digital simulator (RTDS) was used to simulate a high voltage TCSC connected to a two area, four generator study system. The study system, shown in Figure 8.3, is the classical two area, four generator power system used to study inter-area mode oscillations [Kundur1]; the real time model of the system was developed in [Rigby2].

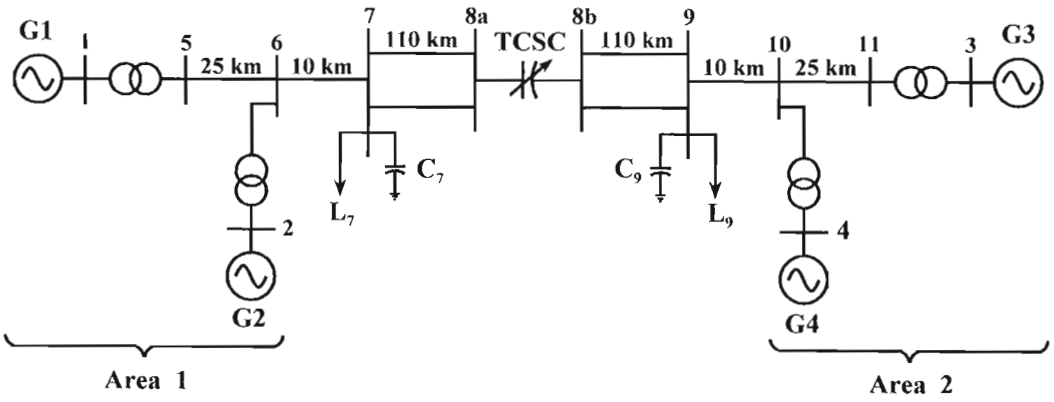

Figure 8.3: Real time digital simulator study system [Rigby2]

The study system, shown in Figure 8.3, which was modelled on the RTDS platform, consists of two identical areas. Each area consists of two 900 MVA, 20 kV generators each having an automatic voltage regulator and a selectable (on or off) power system

stabiliser. The two areas are connected together (between busses 7 and 9) by means of a weak 230 kV transmission system. Bus 8 was split into bus 8a and 8b to accommodate the TCSC. The reason for locating the TCSC between busses 8a and 8b is so that the TCSC can influence the oscillations in the active power transferred between Area 1 and Area 2 that arise due to the inter-area mode oscillation problem. The parameters used for the TCSC in the RTDS simulation model were taken from the Kayenta 230 kV TCSC installed in USA [Christl1, Jalali1].

The Kayenta TCSC consists of a 177μF capacitor and a 0.0068 henries inductor, which for a 60 Hz power system corresponds to a -j15 Ω reactance for the capacitor and j2.56 Ω reactance for the inductor. The capacitive reactance operating range of the Kayenta TCSC is -j15 Ω to -j45 Ω resulting in a thyristor trigger angle range of 180° to 143°. Interestingly, the design parameter, λ, for the Kayenta TCSC is 2.42, which lies within the range of 2 and 4 as proposed in literature [IEE1]. It is also worth noting that the system in Figure 8.3 is a 60 Hz one, and it was simulated as such on the RTDS. The hybrid TCSC triggering controller developed in this thesis is capable of operating on either a 50 Hz or 60 Hz TCSC, as will become evident in the results to be presented in the chapter.

8.3 RTDS and hybrid controller: manual control of trigger angle α

8.3.1 Time domain results

Figure 8.1 showed the connection of the hybrid controller to the RTDS platform. The hybrid controller was used to control the triggering of the thyristors in the real-time simulation model of the TCSC in a closed-loop, hardware-in-loop manner. However, for the initial tests, the commanded trigger angle input (α) to the hybrid TCSC triggering controller was operated manually in order to verify the operating characteristics of the real-time simulated TCSC as controlled by the hybrid controller hardware (ie initially with no power oscillation damping controls). In fact, these initial tests were the same as those carried out on the laboratory-scale TCSC, but this time with the TCSC being the Kayenta TCSC simulated on the RTDS.

The resulting steady state time domain waveforms of the series TCSC capacitor voltage, transmission line and the TCR current is shown in Figures 8.4, 8.5, and 8.6. For comparison purposes the time domain waveforms of the TCSC were also captured at the same thyristor trigger angles using the internal all-simulation model of the TCSC triggering controller developed for the studies in [Rigby2].

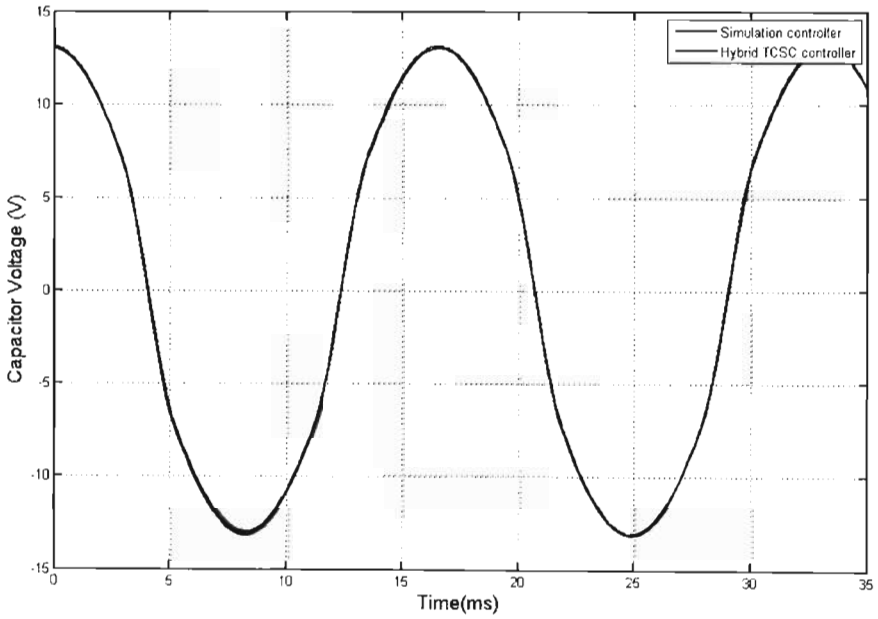

Figure 8.4: Comparison of the time domain waveforms of the TCSC capacitor voltage for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

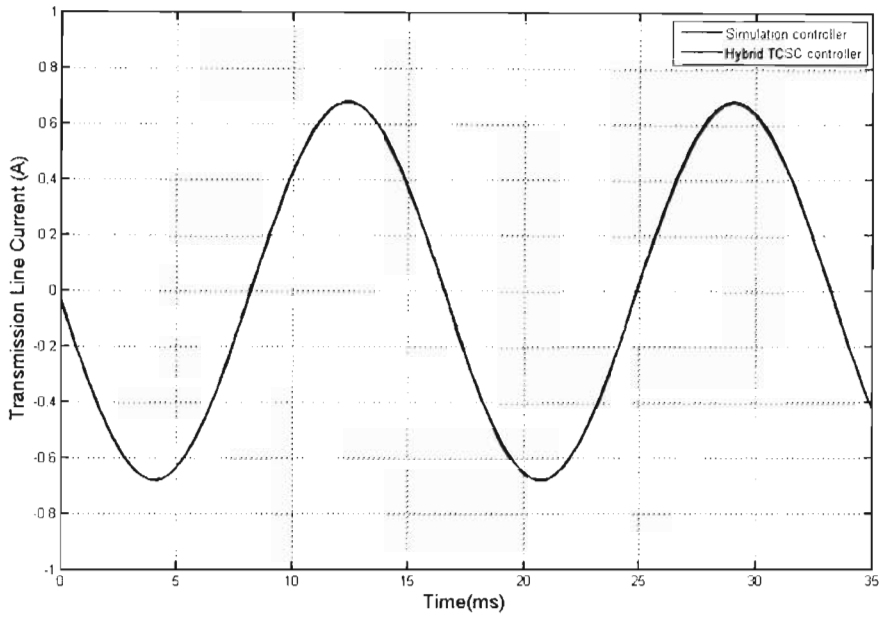

Figure 8.5: Comparison of the time domain waveforms of the transmission line current for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

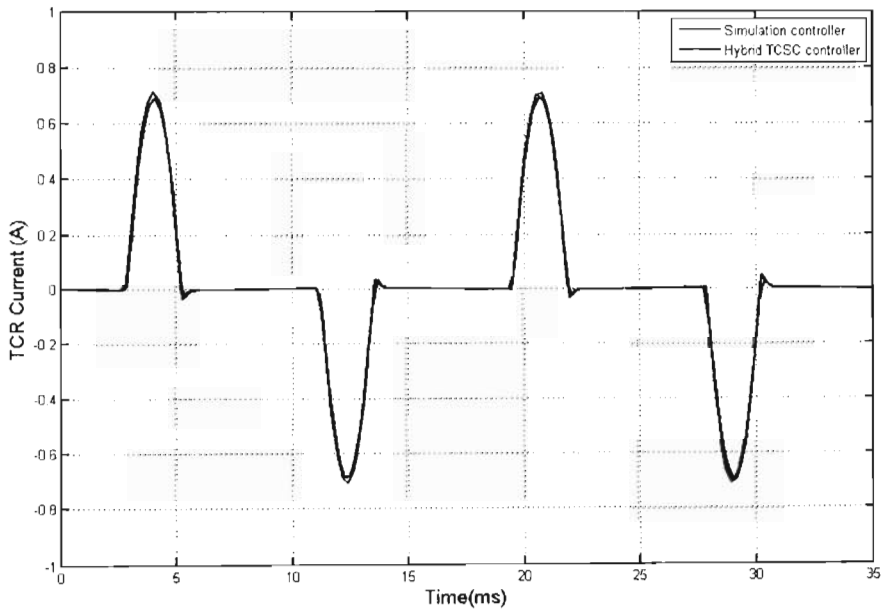

Figure 8.6: Comparison of the time domain waveforms of the TCR current for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

Figures 8.4, 8.5, and 8.6 show that the time domain waveforms obtained from the real-time model when the TCSC triggering controls are part of the real-time model itself agree closely with those obtained from the real-time model when the hybrid TCSC triggering controller connected hardware-in-loop and used to control the triggering of the TCSC in the real-time model. Similar steady state time domain waveforms were captured for several thyristor trigger angles and a select few are shown in Appendix G.

The steady state time domain waveforms obtained at other thyristor trigger angles show similar agreement to that seen in Figures 8.4, 8.5, and 8.6. The time domain waveforms prove that the external hybrid TCSC triggering controller is capable of accurately controlling the operation of the high-voltage TCSC modelled on the real time simulator. Figures 8.4, 8.5, and 8.6 also show that the behaviour of the TCSC is identical irrespective of which controller (internal simulation controller or external hybrid controller) is used. The next step was to verify the operation of the TCSC across its capacitive reactance operating range when the hybrid controller was used to control the TCSC.

8.3.2 Capacitive reactance characteristic

The capacitive reactance versus thyristor trigger angle characteristic for the Kayenta TCSC was firstly obtained using the internal all-simulation model of the TCSC and its triggering controller, and then by using the external hybrid TCSC triggering controller connected hardware-in-loop with the RTDS model of the TCSC. The capacitive reactance characteristic was obtained by calculating the capacitive reactance in the simulation model of the TCSC for several thyristor trigger angles. The resulting capacitive reactance characteristic is shown along with the theoretical prediction in Figure 8.7.

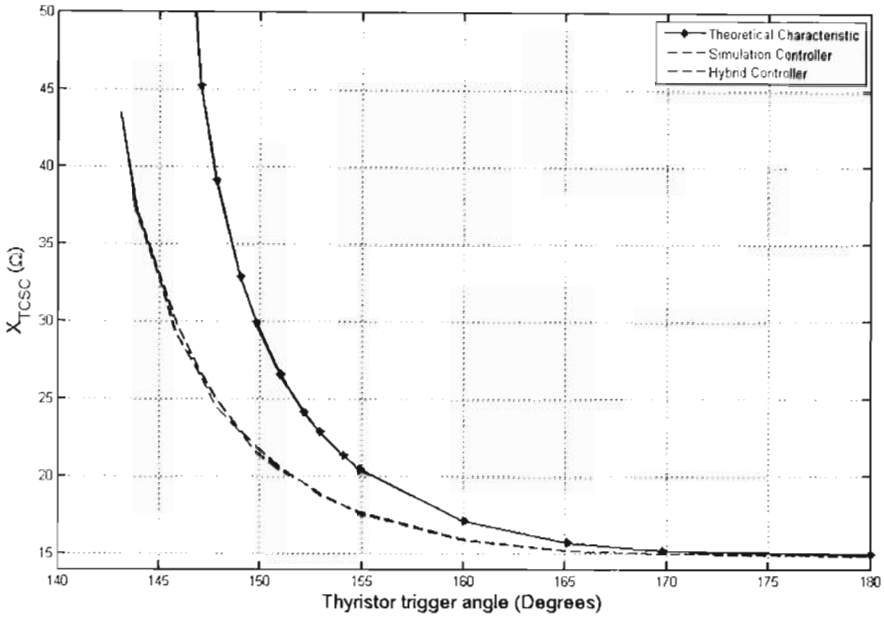

Figure 8.7: Capacitive reactance characteristics of the RTDS model of the Kayenta TCSC: theoretical characteristic, simulated triggering controls and external triggering using the hybrid controller

Figure 8.7 shows that the capacitive reactance characteristics obtained from the RTDS model of the Kayenta TCSC when the simulated triggering controls and the hybrid controller are used are nearly identical. The capacitive reactance characteristics shown in Figure 8.7 also show there is some deviation between the capacitive reactance characteristics obtained from the RTDS simulator and the theoretical capacitive reactance characteristic. However the capacitive reactance characteristics follow a similar trend in each case. The next test was to determine if the external hybrid TCSC triggering controller is capable of stable operation under dynamic conditions.

8.3.3 Step responses

The hybrid TCSC triggering controller, connected hardware-in-loop with the RTDS, was used to conduct step responses of the Kayenta TCSC by changing the commanded thyristor trigger angle from one value to another. The step responses would determine if the hybrid controller was capable of stable operation during dynamic conditions which is of importance because it would mean that the hybrid TCSC triggering controller would be capable of being driven by a higher-level controller (such as a power oscillation damper). The step responses were conducted

for various changes in the thyristor trigger angle. Figures 8.8, 8.9, and 8.10 show the time domain waveforms captured for a step change in the thyristor trigger angle from 144° to 153° when using the all-simulation model of the Kayenta TCSC, and when using the hybrid TCSC triggering controller connected hardware-in-loop.

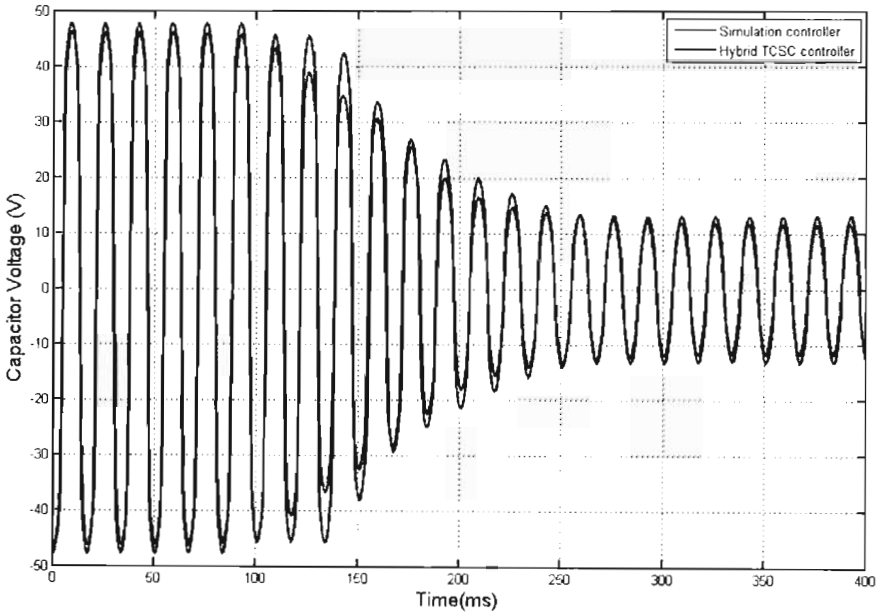

Figure 8.8: Time domain waveforms of the TCSC capacitor voltage for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls obtained for a change in α from 144° to 153°

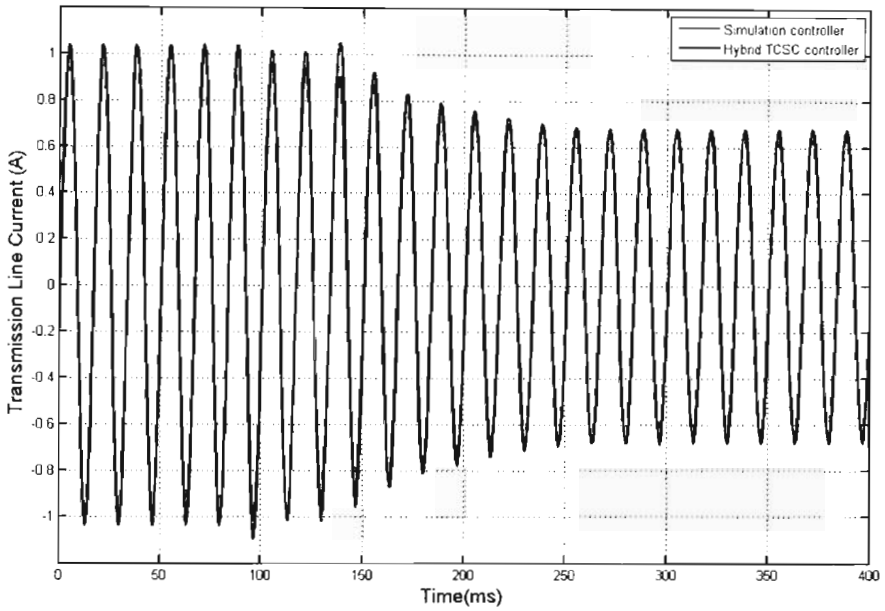

Figure 8.9: Time domain waveforms of the transmission line current for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls obtained for a change in α from 144° to 153°

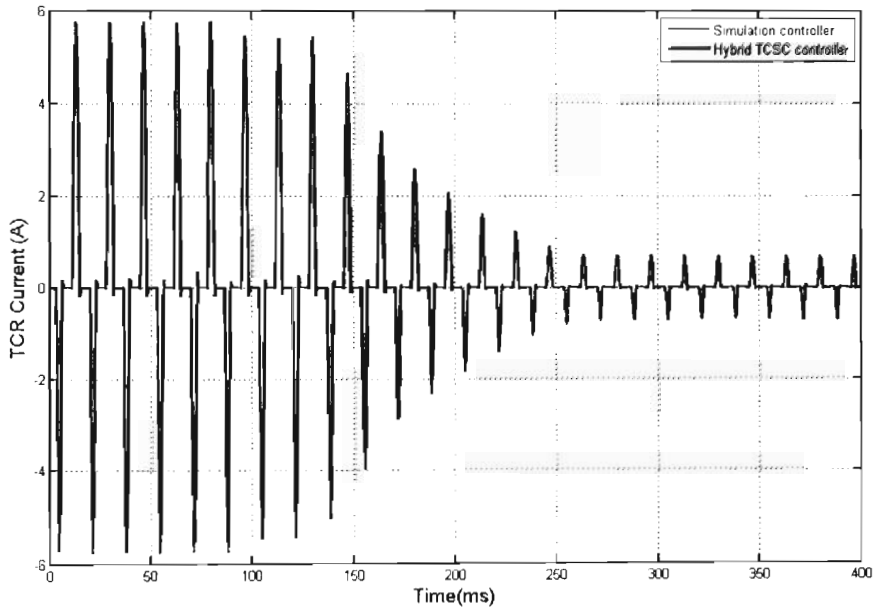

Figure 8.10: Time domain waveforms of the TCR current for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls obtained for a change in α from 144° to 153°

For purposes of comparison the time domain waveforms obtained when using the all-simulation model of the TCSC triggering controller were plotted together with the results obtained when the external hybrid TCSC triggering controller is used. Figures 8.8, 8.9, and 8.10 show that there is a difference between the all-simulation model results and the hardware-in-loop results during the transient period, however there is improved agreement between the results when the study system returns to steady state. The response during the transient period is dependant on when the step change is requested relative to the 60 Hz power system waveforms, which leads to different responses for different points on the 60 Hz waveforms. The results confirm that the performance of the external hybrid TCSC triggering controller is on par with the performance of the simulated triggering controller.

The results in Figures 8.8, 8.9, and 8.10 also showed that the hybrid TCSC triggering controller was capable of stable operation under dynamic conditions and hence could be driven by a higher-level controller. This meant that the external hybrid TCSC triggering controller could now be driven by a power oscillation damping controller to dynamically adjust the reactance of the TCSC in the study system shown in Figure 8.3.

8.4 RTDS and hybrid TCSC triggering controller for power oscillation damping controls

One area of application of a TCSC is to use it to enhance the stability of a power system by providing low frequency power oscillation damping [Gama1, Gama2, Haro1, Johnson1, Matsuki1, Tan1, Yin1]. The TCSC provides damping by changing the impedance of the transmission line by dynamically changing the amount of series compensation it provides to the transmission line. The amount of change in the TCSC compensating reactance is determined by a high-level FACTS controller developed specifically for this purpose. Such a TCSC-based damping control scheme had already been developed for use in the two area, four generator study system, shown in Figure 8.3 [Rigby2]. The TCSC-based damping controller in [Rigby2] used the TCSC to damp the inter-area mode oscillations of the study system modeled on the RTDS platform.

This section discusses the results obtained when the external hybrid TCSC triggering controller developed in this thesis is driven by a high level trigger angle command at its input that is obtained from the TCSC-based damping controller designed in the work of [Rigby2]. The ability of the TCSC and the TCSC-based damping controller to damp the inter-area mode oscillations, when using three different input signals to the TCSC-based damping controller, will be investigated. In this manner, the use of the hybrid TCSC triggering controller developed in this thesis for a realistic high-level FACTS control application will be tested. In all instances for the investigations in this thesis, the inter-area mode oscillations were provoked by applying a 5 ms three phase short circuit fault at bus 7.

8.4.1 Power Oscillation Damping Controller

A TCSC-based damping controller was developed in [Rigby2] for the RTDS simulation platform, and is used to damp inter-area mode oscillations of the two area, four generator study system shown in Figure 8.3. The structure of the TCSC-based damping controller from [Rigby2] is shown in Figure 8.11. Figure 8.11 shows that the controller consists of a signal conditioning section followed by a proportional-gain damping controller whose output ΔX_{TCSC} is the commanded output of the TCSC reactance [Rigby2]. Figure 8.11 shows that the steady state set-point, X_{TCSC0} is chosen to be –j30 Ω.

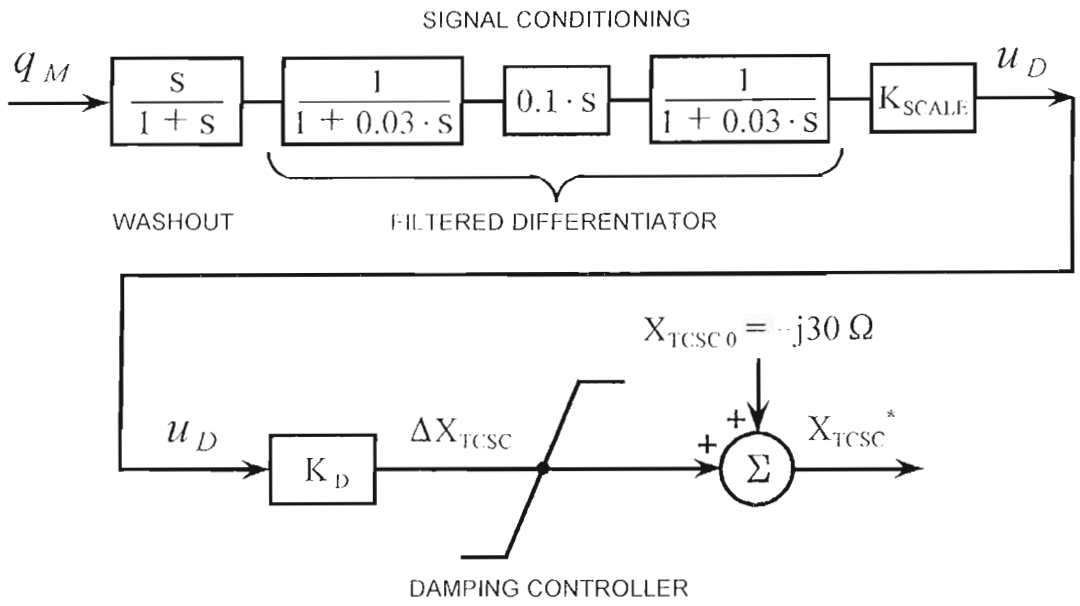

Figure 8.11: Structure of the TCSC-based damping controller [Rigby2]

Section 8.4.2 discusses the individual inter-area mode oscillation damping capabilities of the PSS and the TCSC-based damping controller, while sections 8.4.3, 8.4.4, and 8.4.5 the performance of the TCSC-based damping controller for three different input signals, q_M, considered in this thesis. The performance of the TCSC-based damping controller is determined by examining the response of the inter-area mode oscillations of the study system. The captured waveforms of the TCSC itself appear in Appendix H.

8.4.2 Inter-area mode damping

The two means of providing damping of the inter-area mode oscillations are to use the PSSs on the four generators or the TCSC-based damping controller. The first step was to show ability of the PSSs to damp the inter-area mode oscillations and then to show the ability of the TCSC-based controller to damp the inter-area mode oscillations. Figure 8.12 shows the response of the study system following a 5ms three phase short circuit fault at bus 7 without damping and then with damping of the inter-area mode oscillations. The damping in this instance is provided by switching on the PSSs on all four generators.

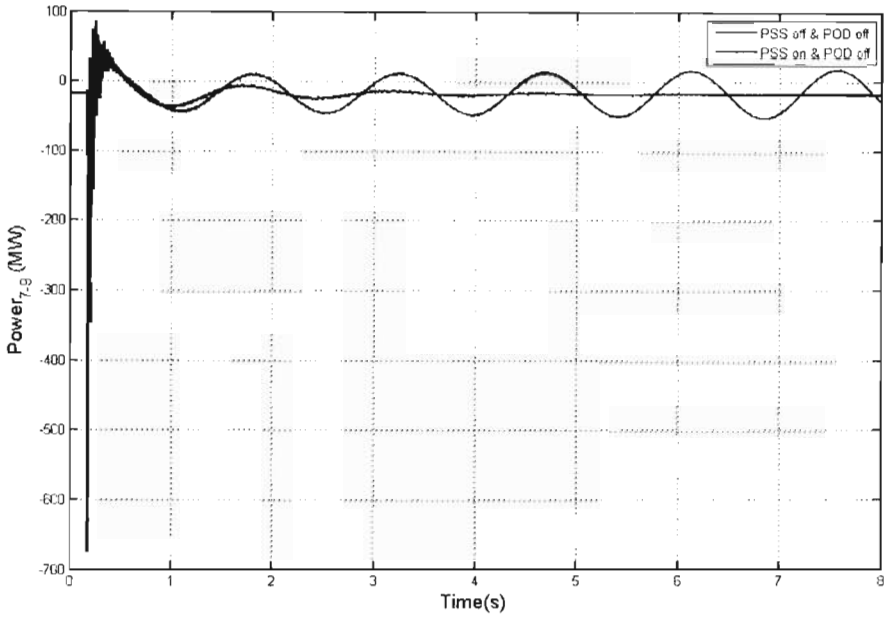

Figure 8.12: System response to a disturbance: without damping and with damping provided by the PSSs

Figure 8.12 shows active power transfer $P_{7\text{-}9}$ at the intertie in the absence of any damping is negatively damped. Figure 8.12 also shows that when the PSSs on all four generators are switched on, the inter-area mode oscillations are highly damped and the study system returns to normal steady state operation within 5 seconds. This test was repeated to measure the performance of the TCSC-based damping controller to damp the inter-area mode oscillations instead of using the PSSs on the four generators.

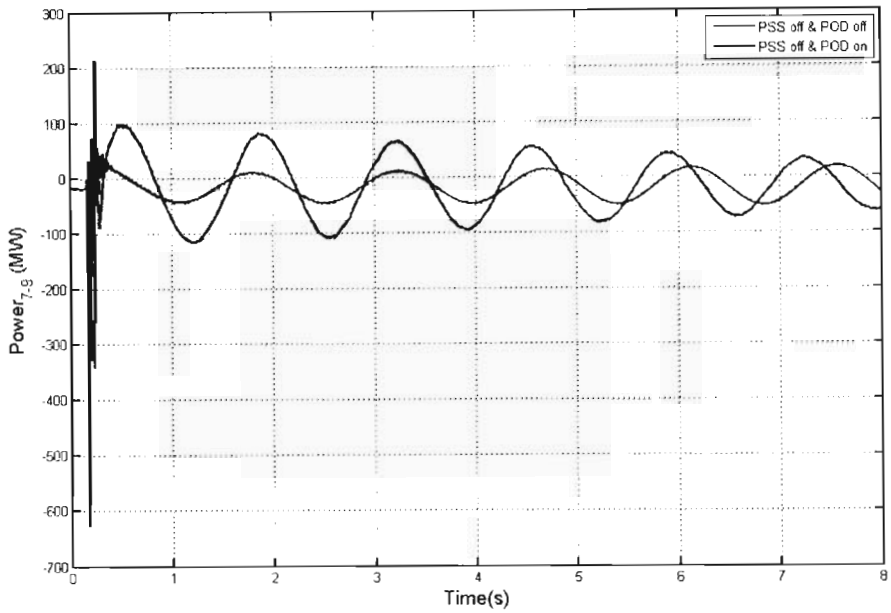

Figure 8.13: System response to a disturbance: without damping and with damping provided by the POD

Figure 8.13 shows the response of the study system following a 5ms three phase short circuit fault at bus 7 with and without damping of the inter-area mode oscillations. In this instance the damping of the inter-area mode oscillations is provided by using the TCSC-based damping controller. The PSSs on all four generators are switched off. Figure 8.13 shows that the inter-area mode oscillations are positively damped when using the TCSC-based damping controller and the TCSC to damp the inter-area mode oscillations.

Although the performance of the TCSC-based damping controller is not as good as compared to the damping provided by the PSSs, the results of Figure 8.13 show that the TCSC-based damping controller is capable of damping the inter-area mode oscillations in the study system. The next set of results was obtained using three different input signals to the TCSC-based damping controller. In all three instances the PSSs on all four generators were switched off.

8.4.3 Synthesised speed difference $\Delta\omega_{synth}$

The first input signal to the TCSC-based damping controller that was considered is the synthesised speed deviation, $\Delta\omega_{synth}$, between the two areas of the study system. The

synthesised speed deviation was obtained from the angular difference of two synthesised voltages at the centres of Area 1 and Area 2 respectively [Rigby2]. Figure 8.14 shows the intertie active power transfer $P_{7\text{-}9}$ following a 5ms three phase short circuit fault at bus 7. In this instance the PSSs were switched off, and the gain of the TCSC-based damping controller, K_D, is set to 4.

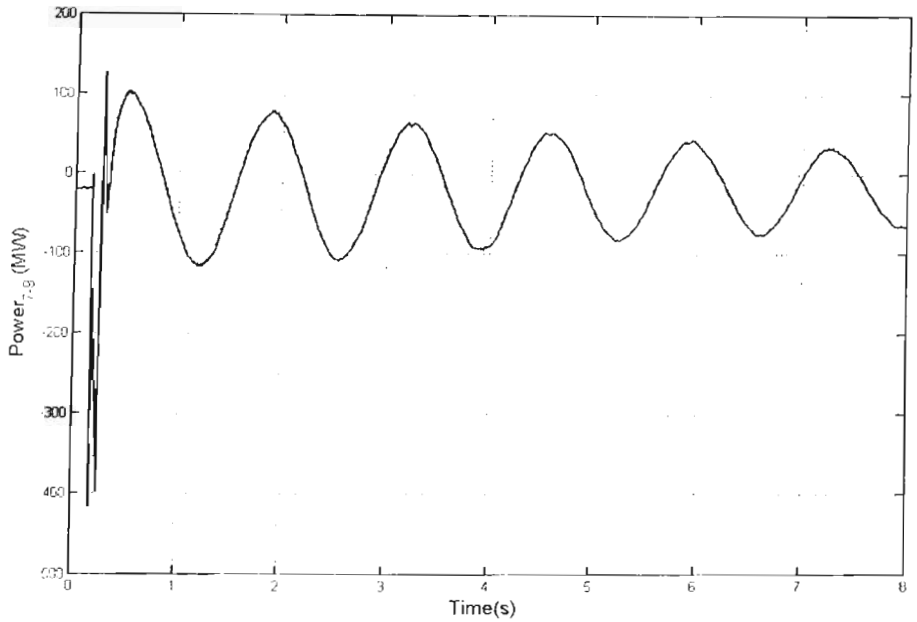

Figure 8.14: Intertie active power transfer following a system disturbance: synthesised speed difference used as the input signal to the POD controller

Figure 8.14 shows that the inter-area mode oscillations are positively damped which is seen as a decay in the amplitude of the oscillations with respect to time. The result therefore shows that the TCSC-based damping controller in conjunction with the external hybrid TCSC triggering controller is capable of damping the inter-area mode oscillations, when using the synthesised speed difference as an input signal to the TCSC-based damping controller. The next section investigates the use of the direct speed difference between two areas as an input signal to the TCSC-based damping controller.

8.4.4 Direct speed difference $\Delta\omega_{direct}$

An alternative method of determining the speed difference between the two areas is to use angular difference of the instantaneous voltage at busbars 7 and 9, by using phasor measurement units [Rigby2]. Figure 8.15 shows the intertie active power transfer $P_{7\text{-}9}$

following a 5ms three phase short circuit fault at bus 7. In this instance the PSSs were switched off, and the gain of the TCSC-based damping controller, K_D, is set to 4.

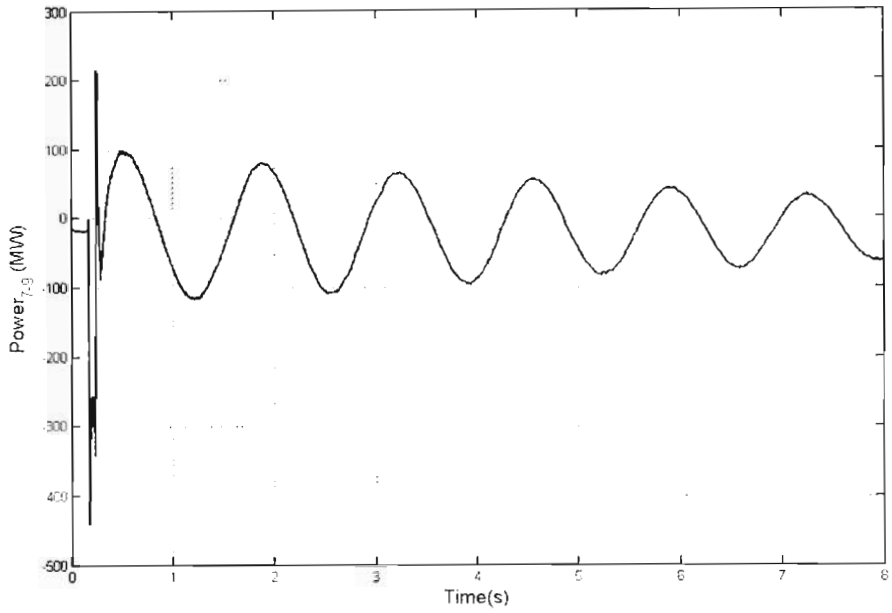

Figure 8.15: Intertie active power transfer following a system disturbance: direct speed difference as the input signal to the POD controller

Figure 8.15 shows that the inter-area mode oscillations are positively damped which is seen as a decay in the amplitude of the oscillations with respect to time. The result therefore shows that the TCSC-based damping controller in conjunction with the external hybrid TCSC triggering controller is capable of damping the inter-area mode oscillations, when using a direct measurement of speed difference between the two areas as an input signal to the TCSC-based damping controller. The next section investigates the use of the rate of change of power flow through the TCSC as an input signal to the TCSC-based damping controller.

8.4.5 Rate of change of power flow

The final input signal to the TCSC-based damping controller that was considered is the rate of change of power flowing through the TCSC itself. The rate of change of power flow was obtained from the calculating the active power flow through the TCSC and differentiating this (together with suitable filtering) with respect to time. The active power flow through the TCSC is calculated from measurements of the current flowing through the TCSC and the voltages at busses 8a and 8b [Rigby2].

Figure 8.16 shows the intertie active power transfer $P_{7\text{-}9}$ following a 5ms three phase short circuit fault at bus 7. In this instance the PSSs were switched off, and the gain of the TCSC-based damping controller, K_D, is set to 4.

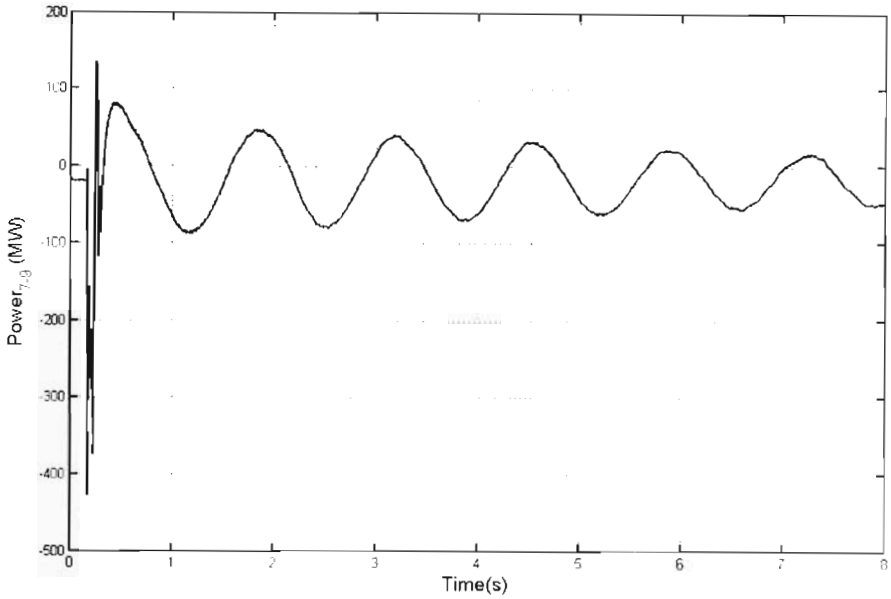

Figure 8.16: Intertie active power transfer following a system disturbance: rate of change of power flow as the input signal to the POD controller

Figure 8.16 once again shows that the inter-area mode oscillations are positively damped which is seen as a decay in the amplitude of the oscillations with respect to time. The result therefore shows that the TCSC-based damping controller in conjunction with the external hybrid TCSC triggering controller is capable of damping the inter-area mode oscillations, when using the rate of change of power flow as an input signal to the TCSC-based damping controller.

Three different signals: synthesised speed difference, direct speed difference, and rate of change of power flow were considered for use in a TCSC-based damping controller. In all three instances the TCSC-based damping controller exhibited positive damping in response to a system disturbance that resulted in inter-area mode oscillations. In all three instances a power oscillation damping controller from [Rigby2] was used to provide a dynamic variation in the commanded trigger angle to the external hybrid TCSC triggering controller designed in this thesis and in turn the external hybrid TCSC triggering controller provided the thyristor triggering signals

via the high-speed digital inputs to the RTDS model of the TCSC. The results demonstrate that the external hybrid TCSC triggering controller is capable of controlling the operation of the TCSC under transient conditions while forming part of a high-level FACTS device control scheme.

8.5 Conclusion

Chapter Seven presented measured results obtained from tests on the low voltage laboratory-scale TCSC. The results from Chapter Seven show that the performance of the original laboratory-scale TCSC was improved by using an improved hybrid TCSC triggering controller that is capable of controlling the thyristor trigger angle to a high degree of resolution. The results of Chapter Seven also showed that the performance of the low voltage laboratory-scale TCSC can be improved by decreasing the inductance of the TCR inductor such that the design parameter, λ, for the laboratory-scale TCSC lies within the limits proposed in the literature [IEE1].

However, the non-ideal effects evident in a low voltage laboratory-scale TCSC are not evident in a high voltage TCSC. Chapter Eight has presented the results obtained from a series of real time digital simulator (RTDS) tests that allowed for the simulation study of the performance of the hybrid controller on a high voltage TCSC without the parameter problems associated with a laboratory-scale TCSC. The RTDS is a digital simulation platform that is capable of solving a simulation model of a power system in real time. The most significant feature of the RTDS is that it has input and output capabilities which allow the simulated plant to be interfaced to, and controlled in real-time by external hardware. In this case the external hardware is the hybrid TCSC triggering controller developed in Chapter Five.

The study system modeled on the RTDS was based on a two area, four generator system that is well accepted for use in the study of inter-area mode oscillations [Kundur1]. The study system on the RTDS also incorporated a TCSC with realistic practical parameters (those of the 230 kV Kayenta TCSC [Christl1]). The Kayenta TCSC, together with a TCSC-based damping controller [Rigby2], was used to damp the inter-area mode oscillations in the study system. The external hybrid TCSC

triggering controller was used to generate the thyristor triggering signals, to trigger the real-time model of the TCSC, based on the commanded thyristor trigger angle it received from a higher level TCSC-based damping controller.

Three different input control signals (synthesised speed difference, direct speed difference, and the rate of change of power flow) to the TCSC-based damping controller were considered. In all three instances the results showed that the inter-area mode oscillations are positively damped and hence decayed in amplitude with time, which means that all three input control signals to the TCSC-based damping controller that were considered are suitable for use by the TCSC-based damping controller to damp inter-area mode oscillations.

The results obtained from the investigations demonstrated that the TCSC-based damping controller and TCSC are capable of damping inter-area mode oscillations. The use of the hybrid TCSC triggering controller, developed in Chapter Five, to control the operation of the Kayenta TCSC demonstrated that the hybrid TCSC triggering controller is capable of being used to control the operation of a practical TCSC under closed loop control transient conditions.

Chapter Nine

Conclusion

9.1 Introduction

This thesis provided and implemented solutions to improve the performance of a low-voltage laboratory-scale TCSC. A review of the literature and detailed simulation studies identified two areas of improvement of the laboratory-scale TCSC that would result in better performance. The actual improvements obtained in the performance of the laboratory-scale TCSC were determined by conducting practical measurements and comparing the results to theoretical expectations. This chapter summarises and reviews the principal findings and conclusions of the thesis, chapter by chapter, and finally suggests further research work that could be undertaken in this area.

9.2 Theory of operation

The literature review conducted in Chapter Two provided insight into the theory of operation of a TCSC and presented the theoretical operating capacitive reactance characteristic of the original laboratory-scale TCSC designed in [Mazibuko2]. The literature presented a theoretical equation of a TCSC that allowed for the calculation of the capacitive reactance of the laboratory-scale TCSC at a given thyristor trigger angle. This theoretical equation was derived assuming ideal conditions, that is with the TCSC connected to an ideal current source and neglecting component losses.

The theoretical equation was used to obtain the ideal capacitive reactance characteristic of the laboratory-scale TCSC. The capacitive reactance versus thyristor trigger angle characteristic of the laboratory-scale TCSC becomes highly non-linear at lower thyristor trigger angles, which makes the capacitive reactance of the TCSC extremely sensitive to changes in the thyristor trigger angle. The sensitivity of the TCSC to changes in the thyristor trigger angle is of importance since variations in the

thyristor trigger angle could result in unacceptable changes in the variable capacitive reactance of the TCSC, which in-turn could result in instability of the power system. The literature proposed that a thyristor trigger angle resolution of 0.1° is acceptable. Further review of the literature showed that the best manner in which to implement a TCSC triggering controller is to make use of a phase locked loop to synchronise to the transmission line currents in-order to determine the turn-on instants of the thyristors.

9.3 Detailed simulation studies

Chapter Three presented practical results obtained from the actual laboratory-scale TCSC. When the measured capacitive reactance characteristic of the laboratory-scale TCSC was compared to the theoretical expectation, it was observed that there was a significant difference between the results. The reason for the difference between the measured and theoretical results was due to the equation, which was used to obtain the theoretical results, being derived for ideal conditions. Specifically the theoretical equation obtained from the literature did not take into account the losses of the components in the TCSC.

In a low voltage laboratory-scale TCSC the losses (thyristor forward volt drop and TCR inductor resistance) contribute significantly to the poor performance of the TCSC. Therefore a detailed simulation model, that took into account the losses due to the thyristor on-state voltages and resistance of the TCR inductors was developed using the PSCAD simulation package. The accuracy of the simulation model was determined by simulating an ideal TCSC and comparing the resulting capacitive reactance characteristic obtained from simulation studies to the theoretical capacitive reactance characteristic. The capacitive reactance characteristic obtained from the ideal simulation model was almost identical to the theoretical capacitive reactance characteristic, thus proving the accuracy of the simulation model.

The simulation model was then developed to take into account the non-ideal properties of the laboratory-scale TCSC (thyristor forward volt drop and the TCR inductor resistance). It was found that the capacitive reactance characteristic of the laboratory-scale TCSC obtained from simulation studies using this more detailed

model agreed closely with the measured capacitive reactance characteristic. Therefore it was concluded that the non-ideal properties of the components in a low voltage laboratory-scale TCSC cannot be neglected since these non-ideal properties have a significant effect on the performance of a laboratory-scale TCSC.

9.4 Prototype TCSC triggering controller

Chapter four discussed the implementation of a prototype TCSC triggering controller that was developed to control the operation of the laboratory-scale TCSC. This prototype TCSC triggering controller was used to obtain the practical results discussed in Chapter Three. Although the prototype TCSC triggering controller was successfully implemented the resolution with which it could control the thyristor trigger angle was found to be 0.45°, which was not within the requirement of 0.1° as proposed in the literature.

The factors that affected this poor maximum attainable resolution in the thyristor trigger angle were found to be certain limitations of the M67 DSP platform on which the prototype TCSC triggering controller was implemented. The specific limitation is that the M67 DSP does not have an appropriate output peripheral that is capable of generating accurate timing signals. This inadequacy of the M67 DSP meant that the resolution of the thyristor triggering signals in the prototype TCSC triggering controller was dependant on the sampling period of the onboard ADCs.

9.5 Hybrid TCSC triggering controller

Chapter Five discussed the implementation of a hybrid TCSC triggering controller developed to meet the performance specification of 0.1° resolution in the thyristor trigger angle as proposed in the literature. The literature also proposed that the best manner in which to implement such a TCSC controller is to use a high level controller and a low level controller. The high level controller is responsible for accurately determining the time remaining until turn on of each thyristor, and the low level

controller is then tasked with the accurate generation of the appropriate thyristor triggering signals, which means that the hybrid TCSC triggering controller as a whole will accurately generate the thyristor triggering signal at the correct point in time.

The high level controller determined the turn-on instants of the thyristors using a three-step-ahead prediction algorithm. This three-step-ahead prediction algorithm worked by firstly determining if a thyristor needs to be triggered within the next three sampling intervals. If this is the case then the time delay until that specific thyristor needs to be triggered is calculated in terms of timer increments and transmitted to the low level controller. The low level controller uses this time delay information obtained from the high level controller to calculate the exact time-to-trigger a thyristor. The low level controller then uses a high speed output port, which is capable of accurately generating timing signals, to generate the thyristor triggering signals.

The hybrid TCSC triggering controller was subjected to several tests which demonstrated that the peripherals and algorithm were working as designed. The final test was to determine the resolution of the thyristor triggering signal. The triggering resolution of the hybrid TCSC triggering controller was determined by simulating 50 Hz transmission line currents within the high level controller and then measuring the variation in the turn on time of thyristor triggering pulses for a known and consistent value of commanded trigger angle. The outcome was that the resolution of the thyristor triggering signal generated using the hybrid TCSC triggering controller is 0.0324° which comfortably met the design specification of 0.1° resolution as proposed in the literature.

9.6 The effect of TCR inductor parameters

The negative effects on the performance of the laboratory-scale TCSC due to the non-ideal components used in the original design of its power circuit were identified in Chapter Three. The non-ideal properties of the components that were identified are the forward volt drop of the thyristors and the resistance of the TCR inductor. The forward volt drop of the thyristor is a characteristic of the device itself and hence cannot be minimised, however the parameters of the TCR inductor can be redesigned.

Chapter Six highlighted two important aspects of the TCR inductor used in the original design of the laboratory-scale TCSC power circuit: firstly that the resistance of the TCR inductor had an adverse effect on the performance of the laboratory-scale TCSC, and secondly that the inductance of the TCR inductor is too large such that the value of the design parameter, λ, for the laboratory-scale TCSC is 1.6, which is not within the range of 2 and 4, as proposed by the literature. The reason for choosing an inductor with a large inductance for the original design of the laboratory-scale TCSC power circuit [Mazibuko2] was to reduce the current ratings of both the TCR inductor itself and of the TCSC's thyristors.

Chapter Six used the detailed simulation model of the laboratory-scale TCSC, developed in Chapter Three, to aid in the selection of newly manufactured TCR inductors. The outcome of the simulation studies demonstrated that the performance of the laboratory-scale TCSC improves appreciably when the inductance of the TCR inductor is decreased such that the value of the design parameter, λ, for a TCSC is within the range of 2 and 4, as proposed in the literature. Finally Chapter Six identified two newly manufactured TCR inductors that could result in improved performance of the laboratory-scale TCSC.

9.7 Performance tests of the improved laboratory-scale TCSC

Chapter Seven firstly presented results obtained from practical tests using the hybrid TCSC triggering controller and the original design of the laboratory-scale TCSC power circuit. The purpose of the practical tests was to determine the performance improvement, if any, of the laboratory-scale TCSC due to the use of the hybrid TCSC triggering controller. The results demonstrated that the performance of the laboratory-scale TCSC improved markedly due to the use of the hybrid TCSC triggering controller. The improvement in the performance of the laboratory-scale TCSC was seen as improved agreement between the measured and theoretical capacitive reactance characteristic of the laboratory-scale TCSC.

Chapter Seven presented and discussed a second set of practical results that were obtained to confirm the findings of the simulation studies conducted in Chapter Six. The simulation studies of Chapter Six identified two newly manufactured TCR inductors that had a lower inductance as compared to the inductor used in the original design of the laboratory-scale TCSC power circuit. The practical measurement of the capacitive reactance characteristic of the laboratory-scale TCSC when using the two newly manufactured inductors demonstrated similar trends to those obtained in Chapter Six. Specifically the measured results showed that the performance of the laboratory-scale TCSC improved as the inductance of the TCR inductor was reduced.

9.8 Real Time Digital Simulator Tests

The real time digital simulator (RTDS) was used to simulate a high voltage TCSC, with representative parameters, connected to a two area, four generator study system. The RTDS is capable of interfacing with the external environment, meaning that the simulation model itself can accept and provide selected simulation signals externally using appropriate peripherals. This external interfacing capability of the RTDS is of significance as this would allow for the connection of the hybrid TCSC triggering controller developed in Chapter Five to the RTDS.

The performance of the hybrid TCSC triggering controller was tested using a high voltage TCSC simulated within the RTDS. The tests conducted using the hybrid TCSC triggering controller demonstrated that it is capable of controlling a high voltage TCSC with parameters from a real installation and hence controlling the operation of an actual TCSC connected to a high voltage system. The final test was to use the hybrid TCSC triggering controller to generate the thyristor triggering signals to the high voltage TCSC based on inputs from a high-level power oscillation damping controller that was implemented within the RTDS simulation model [Rigby2].

The power oscillation damping controller and the hybrid TCSC triggering controller, together with the real-time model of the high-voltage TCSC, were successfully used to damp inter-area mode oscillations within the study system. Three different input

signals to the power oscillation damping controller were considered and in all instances the inter-area mode oscillations were positively damped.

The significance of the input signals chosen for the power oscillation damping controller is that all three input signals are available locally at the TCSC. Therefore the power oscillation controller and hybrid TCSC triggering controller can be used in an actual TCSC installation due to the availability of the local signal required.

9.9 Suggestions for Further work

This thesis has presented the development, implementation and testing of a hybrid TCSC triggering controller for a low-voltage laboratory-scale TCSC. The results obtained from the testing of the hybrid TCSC triggering controller has proven that it is capable of controlling the operation a TCSC. However, the hybrid TCSC triggering controller presented in this thesis is a low level controller which leaves much scope for further work. The scope that exists for further research work is outlined below.

(i) The hybrid TCSC triggering controller was successfully tested on a real time digital simulator to damp inter-area mode oscillations in a transmission network, however the actual power oscillation damping controller was implemented within the RTDS simulation environment. Further work could include transferring the power oscillation damping controller onto the high level controller in the hybrid TCSC triggering controller.

(ii) The application of the TCSC was limited to damping inter-area mode oscillations. Further work could include the development of a variety of high-level FACTS controllers for the TCSC to improve the overall stability of a power system.

(iii) The operating range of the TCSC considered for analysis in this thesis was limited to the capacitive reactance region of operation. Further work could

consider the use of the full operating range of the TCSC, inductive and capacitive regions, to enhance the stability of a power system.

(iv) The power circuit of the laboratory-scale TCSC was redesigned using existing newly manufactured inductors. Further work could involve design and manufacturing inductors to improve the performance of the low voltage laboratory-scale TCSC.

Appendix A

PLL structure and theory

A.1 Introduction

One of the most important algorithms implemented on the TCSC triggering controllers is the phase locked loop (PLL) algorithm. The PLL algorithm is used to calculate the instantaneous angle of the TCSC capacitor voltage from the transmission line currents. The instantaneous angle of the TCSC capacitor voltage is then used to determine the turn-on-instants of the thyristors in the TCSC. The PLL algorithm used in the implementation of the TCSC triggering controllers can be divided into two distinct parts: the first part of the algorithm is concerned with the transformation and the second comprising a proportional and integral (PI) controller.

A.2 Phase locked loop theory

The PLL algorithm is based on phasor theory which is an alternative manner in which a sinusoidal waveform can be represented. In this instance the phasor representing the sinusoidal waveform corresponds to the transmission line current (50Hz or 60Hz). The phasor rotates in an anti-clockwise direction at the supply frequency.

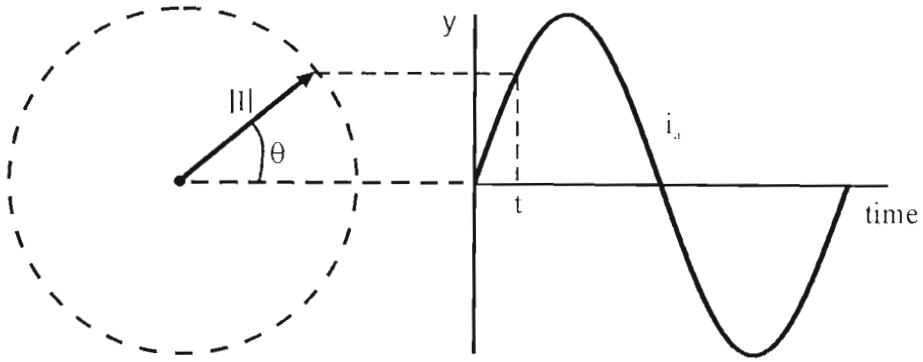

Figure A.1: Relationship between a phasor diagram and its sinusoidal waveform

The projection of the tip of the phasor, onto the y-axis at any time instant, t, will indicate the peak instantaneous current amplitude and the instantaneous angle will be given by θ. If at every time instant the y-component of the phasor is plotted as a function of time, the sinusoidal transmission line current waveform can be reconstructed, as shown in Figure A.1. Figure A.1 shows that to calculate the instantaneous angle of the transmission line current, θ, the position of the phasor needs to be known relative to a reference co-ordinate frame. Space vector theory is used to set up this stationary reference co-ordinate frame and a rotating co-ordinate frame that tracks the rotation of the phasor, which represents the transmission line current. The reference and rotating co-ordinate frames are shown in Figure A.2.

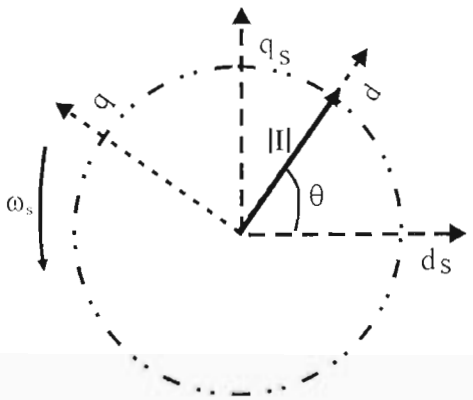

Figure A.2: Phasor diagram using Parks Transform showing the stationary and rotating co-ordinate frames

Figure A.2 shows the stationary co-ordinate frame d_s-q_s, the rotating co-ordinate frame d-q, and the phasor I. The d_s-q_s co-ordinate frame is stationary with respect to time and is used as the reference from which θ can be measured. The d-q co-ordinate frame rotates with respect to time and 'locks' onto the phasor, I. The rotating d-q co-ordinate frame tracks the rotation of the phasor, I, and in doing so, traces out the value of instantaneous angle θ. The equations used to obtain the stationary and rotating co-ordinate frames is discussed in the next section.

A.3 Phase locked loop transformation equations

The previous section discussed the use of space vector theory used in the implementation of the PLL algorithm in order to calculate the instantaneous angle of

the TCSC capacitor voltage. Two co-ordinate frames are used to calculate the instantaneous angle of the TCSC capacitor voltage: a stationary reference co-ordinate frame and a rotating co-ordinate frame. This section presents the transformation equations that are used to obtain these co-ordinate frames [Schauder1]. The first set of equations, equation (A.1) and equation (A.2), are used to obtain the reference stationary co-ordinate frame, d_s-q_s [Schauder1].

$$I_{ds} = I_a \tag{A.1}$$

$$I_{qs} = \frac{-1}{\sqrt{3}} I_a - \frac{2}{\sqrt{3}} I_c \tag{A.2}$$

The d_s-q_s components of the stationery co-ordinate are used to calculate the rotating co-ordinate frame. Equations (A.3) and (A.4) are used to obtain the rotating d-q co-ordinate frame [Schauder1].

$$I_d = I_{ds} \cos\theta + I_{qs} \sin\theta \tag{A.3}$$

$$I_q = I_{qs} \cos\theta - I_{ds} \sin\theta \tag{A.4}$$

Figure A.2 shows the case when the rotating d-q co-ordinate frame is aligned exactly with the phasor representing the transmission line current. The important observation here is that there is no q-component of the phasor when the rotating d-q co-ordinate frame is aligned with the phasor. Therefore, if there is a q-component of the phasor then this would mean that the rotating d-q co-ordinate frame and the phasor are not aligned. Equation (A.5) shows the calculation used to determine the error of the calculated instantaneous angle of the phasor [Schauder1].

$$I_q = \sin\theta_{error} \tag{A.5}$$

For small values of the error in the calculated instantaneous angle, equation (A.5) can be simplified to equation (A.6) [Schauder1].

$$\theta_{error} \approx I_q \tag{A.6}$$

A.4 Phase locked loop structure

The previous section presented the transformation equations that are used in the calculation of the instantaneous angle of the TCSC capacitor voltage. This section discusses the structure of the PLL algorithm and how the instantaneous angle of the

TCSC capacitor voltage is calculated. The final step in the PLL algorithm is the proportional and integral (PI) controller that is used by the rotating d-q co-ordinate frame to track the phasor representation of the instantaneous transmission line current.

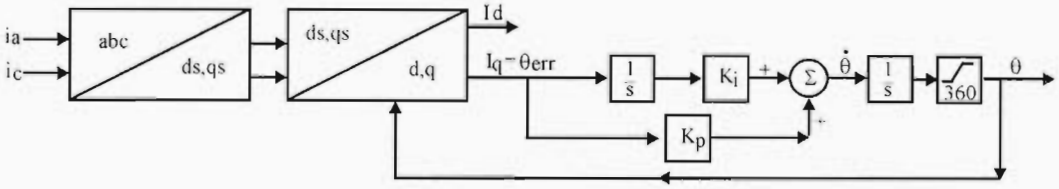

Figure A.3: Detailed flow diagram showing implementation of PLL

Figure A.3 shows the flow diagram of the PLL algorithm used in the implementation of the TCSC triggering controllers. The first part if the algorithm is concerned with the transformation of the magnitudes of the transmission line currents in order to obtain the stationary and rotating co-ordinate frames. The second part of the PLL algorithm uses a PI controller to track the phasor representing the transmission line current.

The end result of the PI controller is the calculation of the power system frequency $\dot{\theta}$, which is integrated with respect to time to obtain the instantaneous angle of the TCSC capacitor voltage, θ. The power system frequency, $\dot{\theta}$, is used by the three-step-ahead prediction algorithm to determine when to trigger a thyristor, while the instantaneous angle of the TCSC capacitor voltage, θ, is used to determine if and when a thyristor should be triggered.

Appendix B

Detailed PSCAD simulation model of the laboratory-scale TCSC

B.1 Introduction

Chapter Three discussed the development of a simulation model of the laboratory-scale TCSC using the PSCAD simulation package. The simulation model was developed to take into account the non-ideal properties of the components used in the construction of the laboratory-scale TCSC. This Appendix shows how the non-ideal properties of the components were actually taken into account in the PSCAD simulation model.

B.2 Detailed PSCAD simulation model

The laboratory-scale TCSC along with the complete power circuit used in the laboratory experiments were modelled using the PSCAD simulation package. Figure B.1 shows the PSCAD simulation model of the laboratory-scale TCSC and the power circuit (3-phase power source and transmission line simulator).

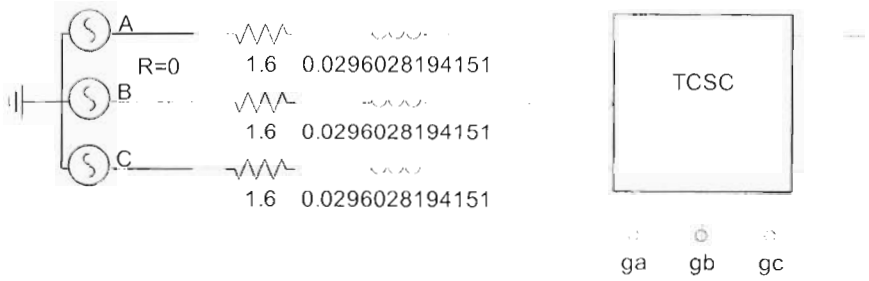

Figure B.1: PSCAD simulation model of the laboratory-scale TCSC and the power circuit

The 3-phase source voltage was chosen to be 28 V per phase which corresponds to the voltage used in the experiments conducted in the laboratory. The parameters (resistance and inductance) of the transmission line simulator were also represented in

the PSCAD model. The transmission line simulator consists of an inductor having an inductance of 0.0296 henries, which also has an associated resistance of 1.6 Ω. The details of the embedded laboratory-scale TCSC model are shown in Figure B.2.

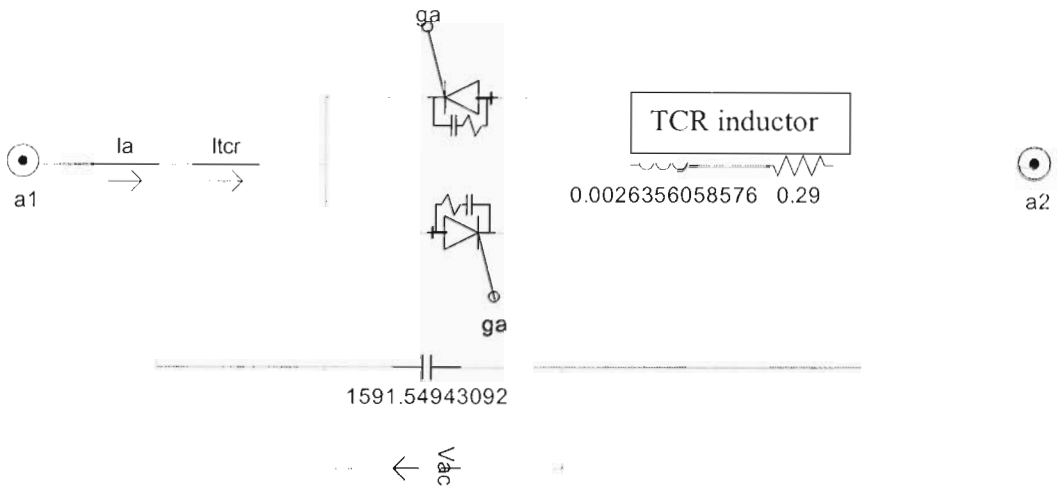

Figure B.2: PSCAD simulation model of the laboratory-scale TCSC showing the TCR resistance and reactance

Figure B.2 shows a single phase of the 3-phase laboratory-scale TCSC that has been represented in the PSCAD simulation model. Figure B.2 shows that the TCR inductor has been represented with its own inductance of 0.00263 henries and its associated resistance of 0.29 Ω. Figure B.2 shows the representation of the fixed capacitor used in the laboratory-scale TCSC having a capacitance of 1591.55 farads. Figure B.2 also shows the TCSC thyristors and its associated snubber circuits. The parameters of the TCSC thyristors and snubber circuit are shown in Figure B.3.

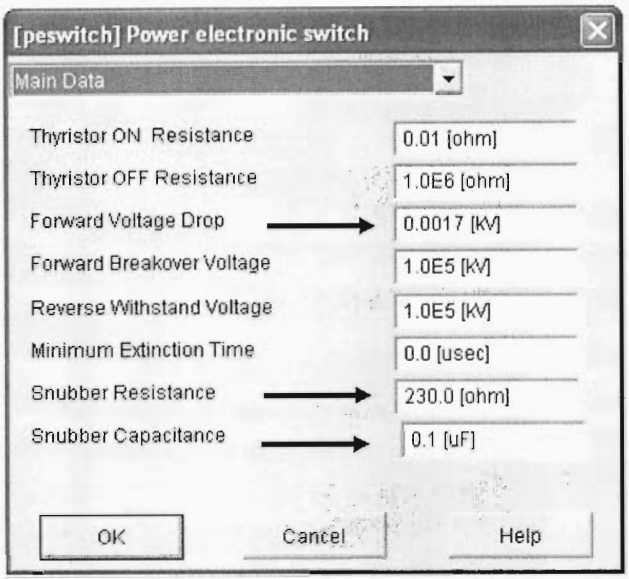

Figure B.3: Screen shot of the parameters used for the TCSC thyristors

The forward volt drop of the thyristors used in the laboratory-scale TCSC was found to be 1.7V [IRF1]. This forward volt drop of the TCSC thyristors are represented by specifying the "Forward Voltage Drop" to be 0.0017 kV in the PSCAD properties window of the thyristors, as shown in Figure B.3. Figure B.3 also shows the parameters used for the snubber circuit in the simulation model which corresponds to the parameters of the snubber circuit used in the actual laboratory-scale TCSC.

Figure B.4 shows the PSCAD representation of the algorithm implemented on the prototype TCSC triggering controller. The built-in PSCAD PLL functional block was used to calculate the instantaneous angle of the TCSC capacitor voltage from the transmission line currents. The instantaneous angle of the TCSC capacitor voltage was compared to the commanded thyristor trigger angle using a comparator to determine when a thyristor should be triggered. The prototype TCSC triggering controller used the same method to determine when to trigger a thyristor.

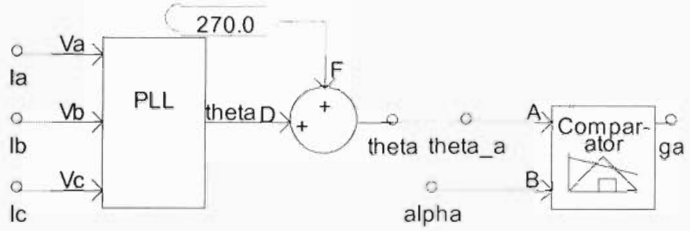

Figure B.4: PSCAD simulation model representation of the prototype TCSC triggering controller

The use of a comparator in the PSCAD simulation model to determine when a thyristor should be triggered also modelled the discrete nature of the actual prototype TCSC triggering controller. The other aspect of the prototype TCSC triggering controller that required modelling was the sampling period of 25 μs. Figure B.5 shows that the sampling period of the prototype TCSC triggering controller was taken in account by setting the PSCAD simulation time step to a value of 25 μs.

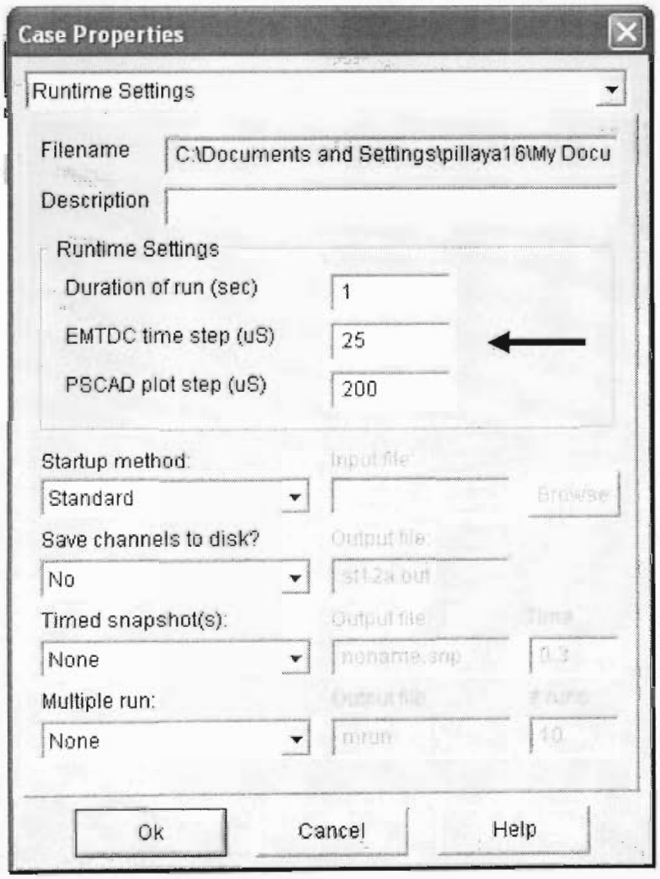

Figure B.5: Screen shot of the PSCAD simulation model properties window showing the time step to be 25 μs

For the case of the hybrid TCSC triggering controller the built-in PSCAD interpolation functional block was used in place of the comparator to determine when to trigger a thyristor. The use of the built-in PSCAD interpolation functional block represented the three-step-ahead prediction algorithm that was implemented on the hybrid TCSC triggering controller. Figure B.6 shows the built-in PSCAD interpolation functional block connected to the output of the built-in PSCAD PLL functional block.

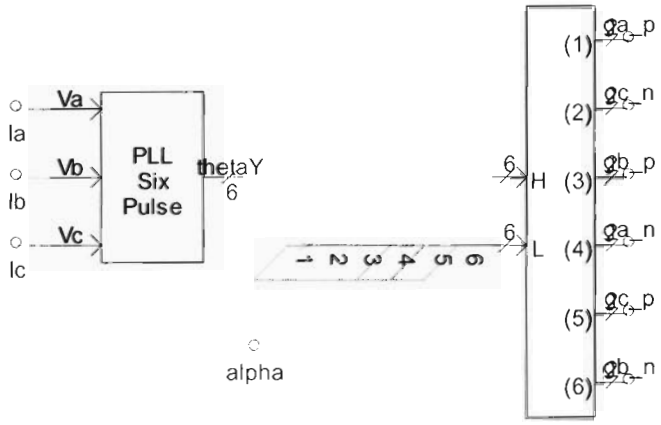

Figure B.6: Screen shot of PSCAD simulation model showing the built-in interpolation functional block

Figure B.7 shows that the PSCAD simulation model was configured to use the interpolation functional block by checking the "Interpolate network solution" check box in the simulation properties setup window.

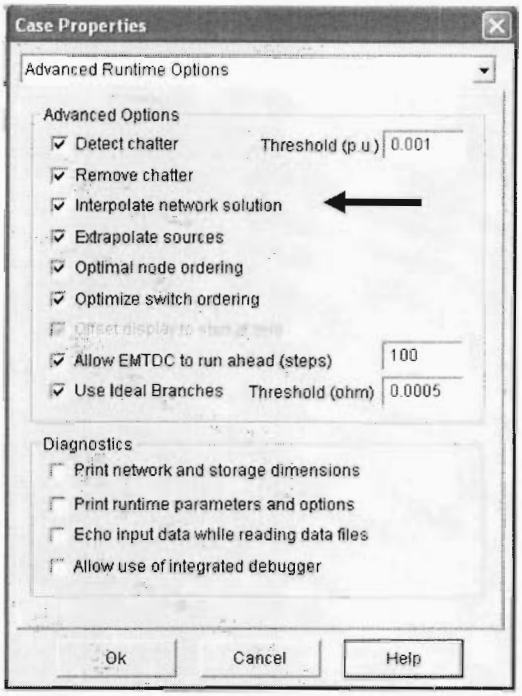

Figure B.7: Screen shot of the PSCAD simulation model properties window showing the interpolation function enabled

Finally the capacitive reactance of the TCSC was calculated at each thyristor trigger angle using the PSCAD Fast Fourier Transform (FFT) functional block, shown in Figure B.5. The TCSC capacitive reactance calculation used the TCSC capacitor voltage and transmission line current.

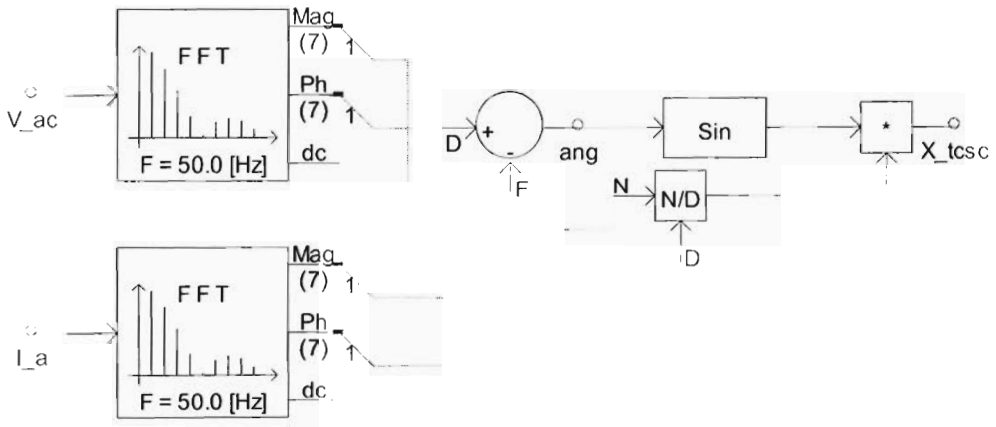

Figure B.8: Calculation of the TCSC capacitive reactance within the PSCAD simulation model

Appendix C

Hybrid controller flow charts and thyristor mapping

C.1 Introduction

This Appendix presents and discusses flowcharts representing the algorithm implemented on the hybrid TCSC triggering controller. The TCSC thyristor mapping is also listed in this Appendix.

C.2 Thyristor Mapping

Table C.1 shows the thyristor mapping that is used in the hybrid TCSC triggering controller algorithm. The binary value showed is the actual value that is transmitted from the high level controller to the low level controller using the 3-bit parallel communication link.

Table C.1: Table showing the thyristor mapping

Thyristor	PWM port	Thyristor ID	**Binary Value**
a+	T1PWM	1	**001**
a-	PWM1	2	**010**
b+	T2PWM	3	011
b-	PWM3	4	**100**
c+	T3PWM	5	**101**
c-	PWM5	6	110

C.3 Hybrid TCSC triggering controller flowcharts

Figure C.1 and Figure C.2 show the flowchart of the algorithms implemented on the hybrid TCSC triggering controller. Figure C.1 shows the flowchart of the algorithm implemented on the high level controller and Figure C.2 shows the flowchart of the algorithm implemented on the low level controller. The discussion will show that both the high level controller algorithm and the low level controller algorithms are triggered by events.

In the case of the high level controller algorithm it is the falling edge of the master clock signal that starts the execution of the algorithm. In the case of the low level controller algorithm it is the presence of data on the parallel port that initiates the algorithm. The high level controller algorithm is discussed first since the low level controller algorithm is dependant on the outputs of the high level controller algorithm.

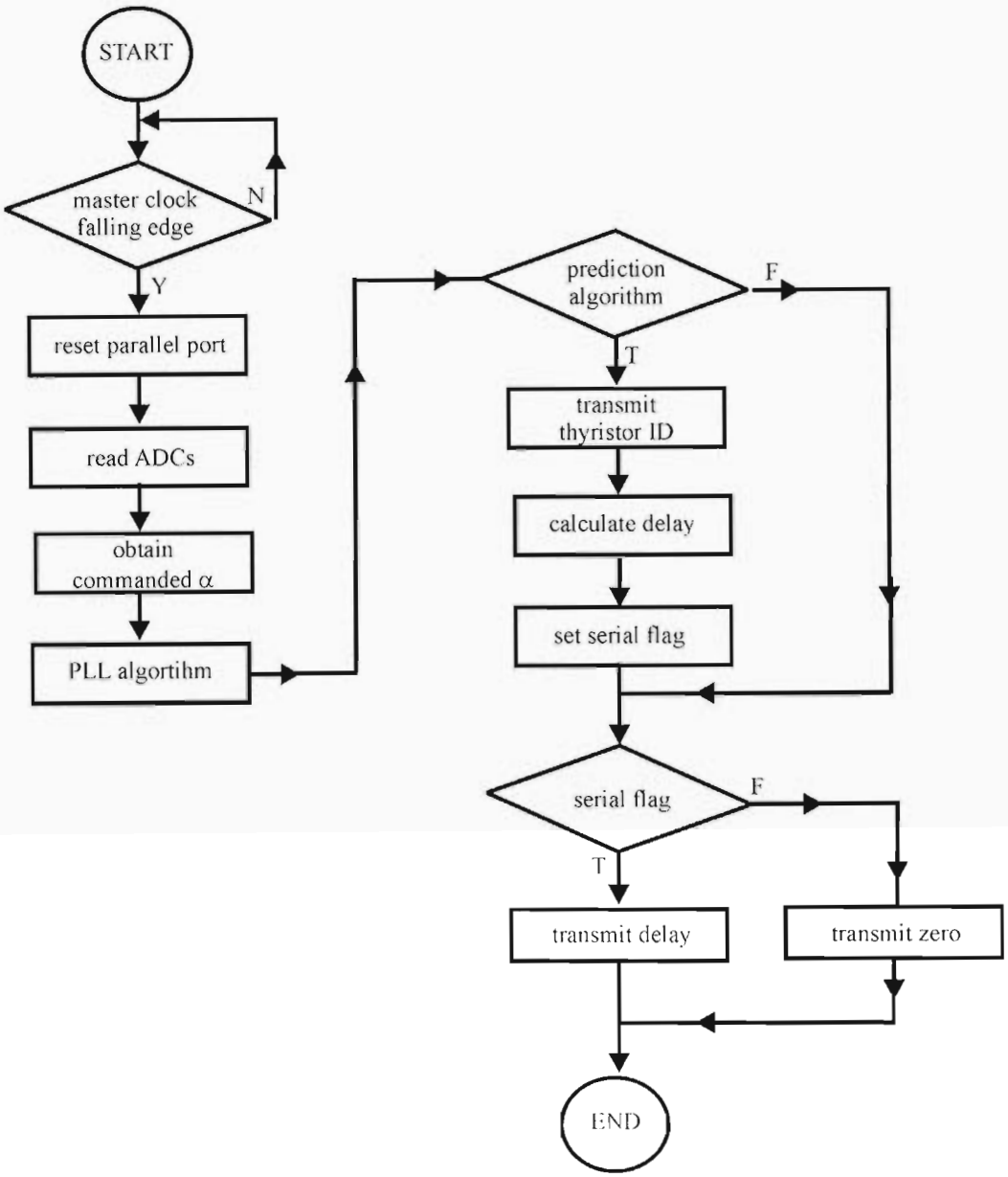

Figure C.1: High level controller flowchart

Figure C.1 shows the functional flow diagram of the algorithm implemented on the high level controller. The high level controller algorithm is started (triggered) by the falling edge of the master clock. The first major step of the algorithm is to obtain the required inputs (ADCs values and commanded thyristor trigger angle) to the algorithm. The next step is the execution of the PLL algorithm to obtain the instantaneous angle of the TCSC capacitor voltage.

The instantaneous angle of the TCSC capacitor voltage is used by the three-step-ahead prediction algorithm to determine if a thyristor is to be triggered within the next three sampling intervals. If the three-step-ahead prediction algorithm determines that a thyristor is to be triggered then the thyristor ID is transmitted via the parallel port to the low level controller. The serial flag is also set which allows the serial port to transmit the calculated delay value until a thyristor is to be triggered, in terms of timer increments, to the low level controller.

If the prediction algorithm determines that none of the thyristors is to be triggered then the value zero is transmitted by the serial port to the low level controller. The low level controller algorithm is driven by the high level controller algorithm by the transmission of the thyristor ID from the high level controller to the low level controller via the parallel port. The thyristor ID signifies to the low level controller that a thyristor needs to be triggered within the next three sampling periods and also specifies which of the six thyristors in the laboratory-scale TCSC will be triggered. Figure C.2 shows the functional flow diagram of the algorithm implemented on the low level controller.

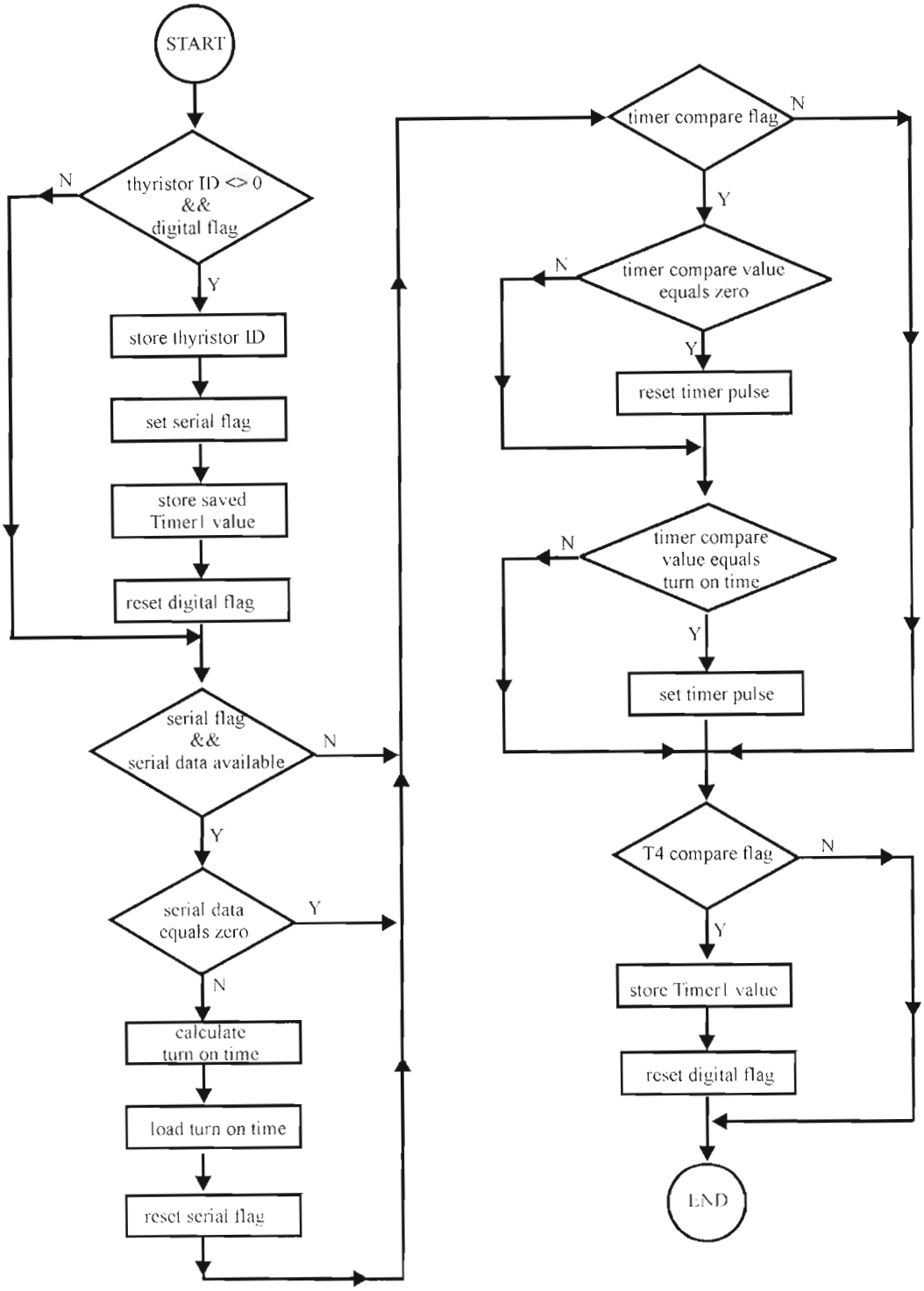

Figure C.2: Low level controller flow chart

Figure C.2 shows that the low level controller algorithm starts with the presence of data on the parallel port. The first major part of the low level controller algorithm is the reading and storing of the data that has been sent by the high level controller to the

low level controller. This received data is the thyristor ID from the parallel port and the delay in terms of timer increments (until a thyristor is to be triggered) from the serial port. The serial port data which is the delay until a thyristor is to be triggered is added to the saved value of Timer 1 to obtain the thyristor turn-on-time. The saved value of Timer 1 is the time at which the rising edge of Timer 4 occurred, which also corresponds to the time at which the ADCs were sampled on board the high level controller. Finally, the thyristor ID information specifies to the low level controller which of the compare registers should be loaded with the calculated thyristor turn-on-time.

When the timer value (Timer 1, Timer 2 or Timer 3) is equal to (matches) the calculated thyristor turn-on-time value loaded into the compare register, the output PWM pin associated with that compare register generates a logic high. The logic high signal that is generated upon a compare match then results in the triggering of the thyristor in the TCSC. The compare match operation also changes the state of the compare flag, associated with that compare register, to a logic high.

Two of the more important inherent characteristics that require mentioning when using this compare method to generate the thyristor triggering signals is that: firstly the thyristor triggering signal is automatically reset to a logic low when the timer count value overflows to zero, and secondly if the compare register value is not cleared then the PWM pin associated with that compare register will continuously generate a logic high on every subsequent compare match operation.

Both of the inherent characteristics mentioned above are undesirable, in this particular application, since an automatic reset of the thyristor triggering signal to a logic low could result in the duration of the thyristor triggering signal that is not long enough to trigger the thyristor, and subsequent compare match operations which result in the thyristor triggering signal generating a logic high could trigger a thyristor at the incorrect point in time.

To accommodate for automatic resetting of the thyristor triggering pulse to a logic low, the compare register is loaded the value zero immediately after a compare operation, which is detected by the changing in the state of the compare flag. The

loading of a compare value of zero ensures that the thyristor triggering signal is not automatically reset to a logic low following a timer overflow to zero.

However, if this compare value of zero is not cleared the thyristor triggering signal will remain in a logic high state which will trigger the thyristor as soon as the thyristor becomes forward biased. This is the subsequent compare match operation characteristic which is accommodated for by loading a value in the compare register that is not within the counting range of the timer. By loading a value into the compare register that is not within the counting range of the timer ensures that there will be no compare match operations which in turn means that the thyristor triggering signal will remain a logic low state.

The final part of the algorithm, shown in Figure C.2, shows that the Timer 1 value is saved on every occurrence of a rising edge of Timer 4, which corresponds to the initiation of an analogue-to-digital conversion on board the high level controller.

Appendix D

Hybrid controller signal waveforms

D.1 Introduction

This Appendix presents additional waveforms, from those shown in Chapter Five, obtained when the hybrid TCSC triggering controller was tested. The results contained in this section were obtained by simulating ideal 50 Hz transmission line currents within the high level controller and specifying a known and constant thyristor trigger angle.

D.2 Thyristor triggering signals

The width of the thyristor triggering signal is configured to have a minimum high time of 555.55μs (10° for a 50 Hz system) and a maximum high time of 1.11 ms (20° for a 50 Hz system). Figure D.1 and Figure D.2 demonstrate this configuration of the thyristor triggering signal. Figure D.1 shows that the minimum width of the thyristor triggering signal is 550 μs, which corresponds to the configuration setting. Figure D.2 shows the maximum variation of the falling edge of the thyristor triggering signal is 550 μs.

Combining the measurements obtained from Figures D.1 and D.2 effectively show that the thyristor triggering signal will have a minimum high time of 550 μs and a maximum high time of 1.10 ms, which corresponds to the manner in which the thyristor triggering signals are configured.

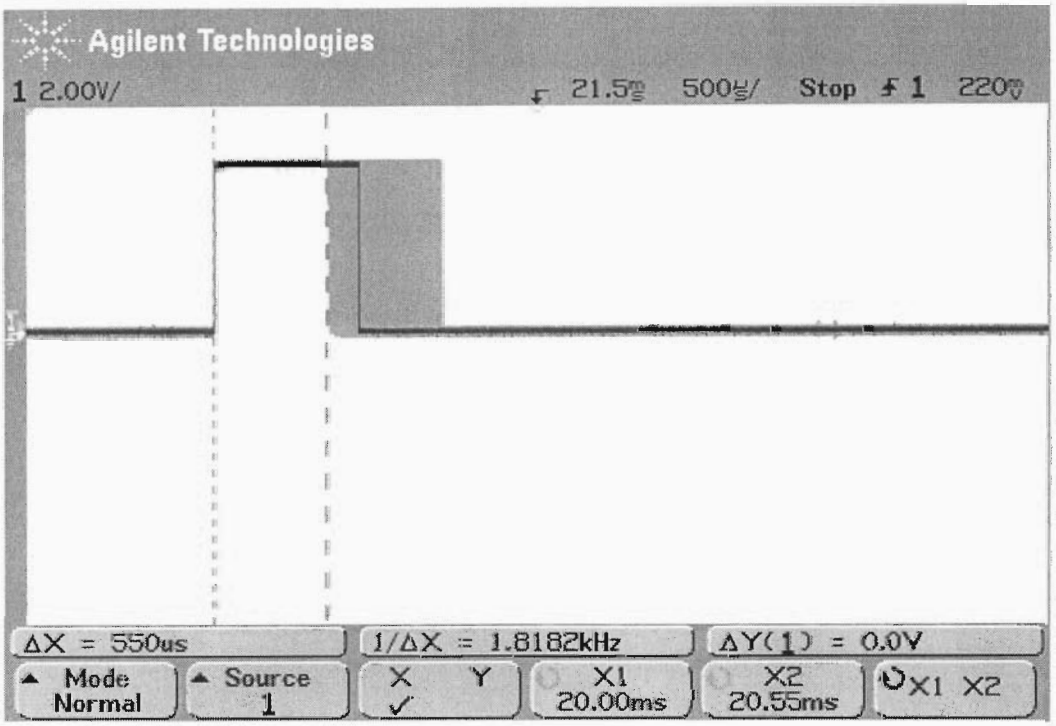

Figure D.1: Thyristor triggering signal showing the minimum high time of 550 μs

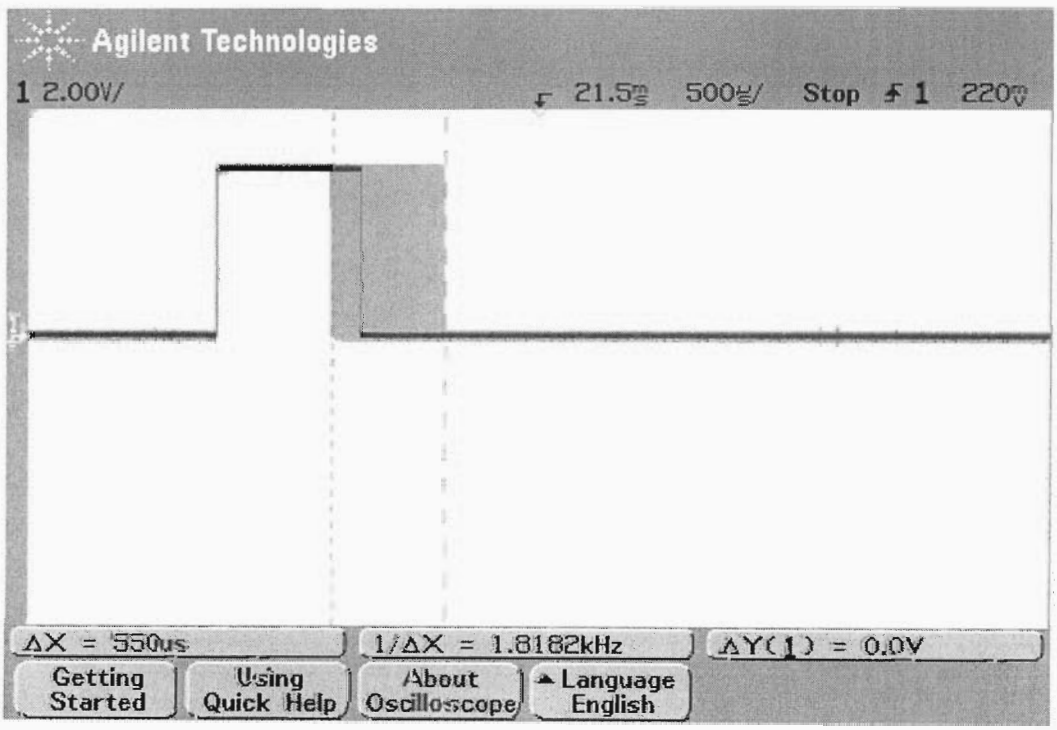

Figure D.2: Thyristor triggering signal showing the variation in the falling edge of 550 μs

The next important set of waveforms was captured to check and verify the phase difference between the thyristor triggering signals for the same phase. Figure D.3 shows that the phase difference between the thyristor triggering signals for the forward biased thyristor and the reverse biased thyristor are 180°, which is correct for the 50 Hz transmission line currents used during this test.

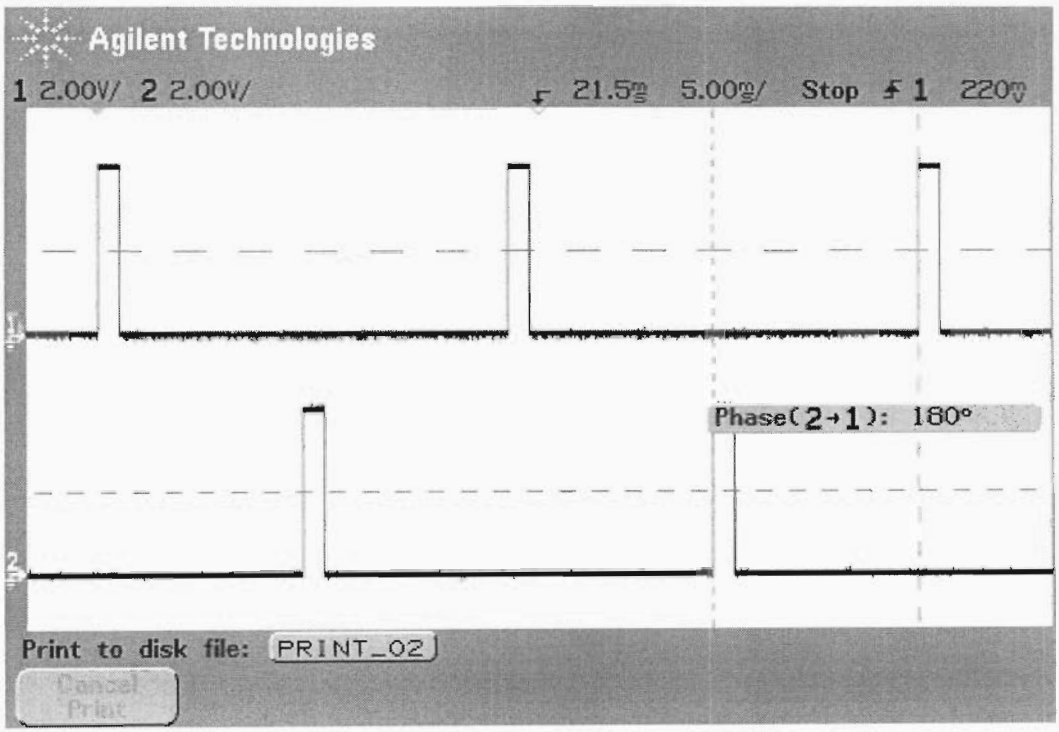

Figure D.3: Phase difference between the Phase A thyristor triggering signals

The phase difference between the phases were also checked and verified to be correct. Figure D.4 shows the captured thyristor triggering signals for the forward biased Phase A and Phase B thyristors.

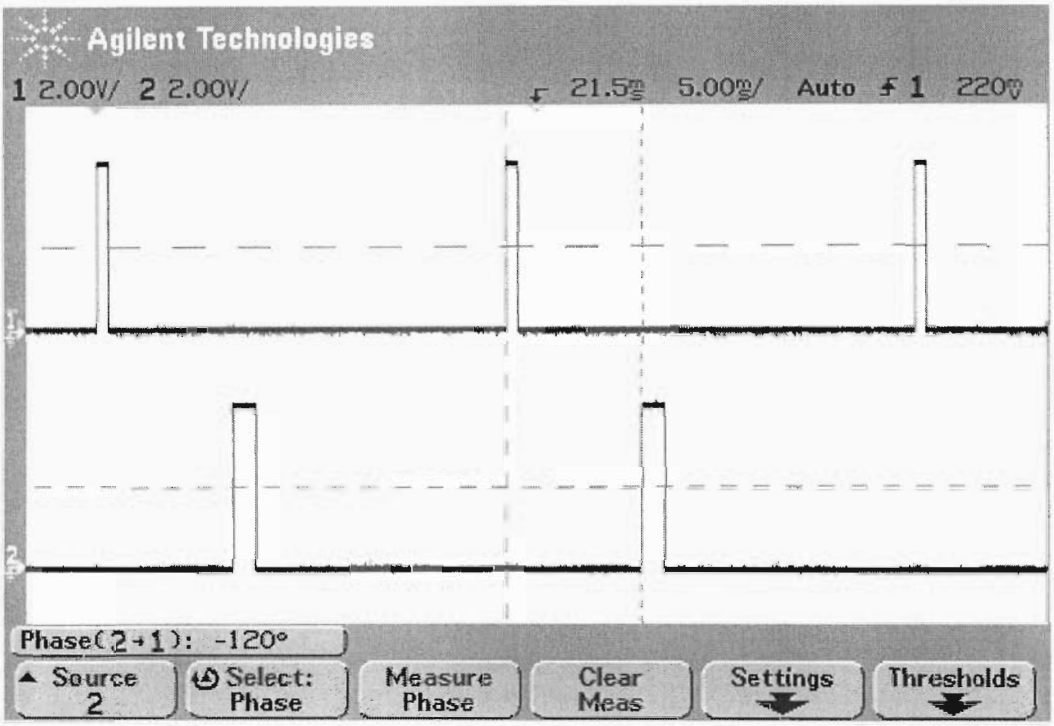

Figure D.4: Phase difference between the Phase A and Phase B thyristor triggering signals

Figure D.4 shows that the phase difference between the forward biased Phase A and Phase B thyristors is 120°, which is correct for a balanced 3-phase power system as is the case during this test. The difference in the width of the Phase A and Phase B thyristor triggering pulses is due to the manner in which the thyristor triggering pulses were configured, which was discussed earlier in this section.

D.3 Serial communication waveforms

The serial port was configured on board the high level controller. The serial communication link comprises three signals: data signal, a clock signal, and a read enable signal. The clock signal was configured to operate at 800 kHz, which is confirmed by the captured waveform shown in Figure D.5.

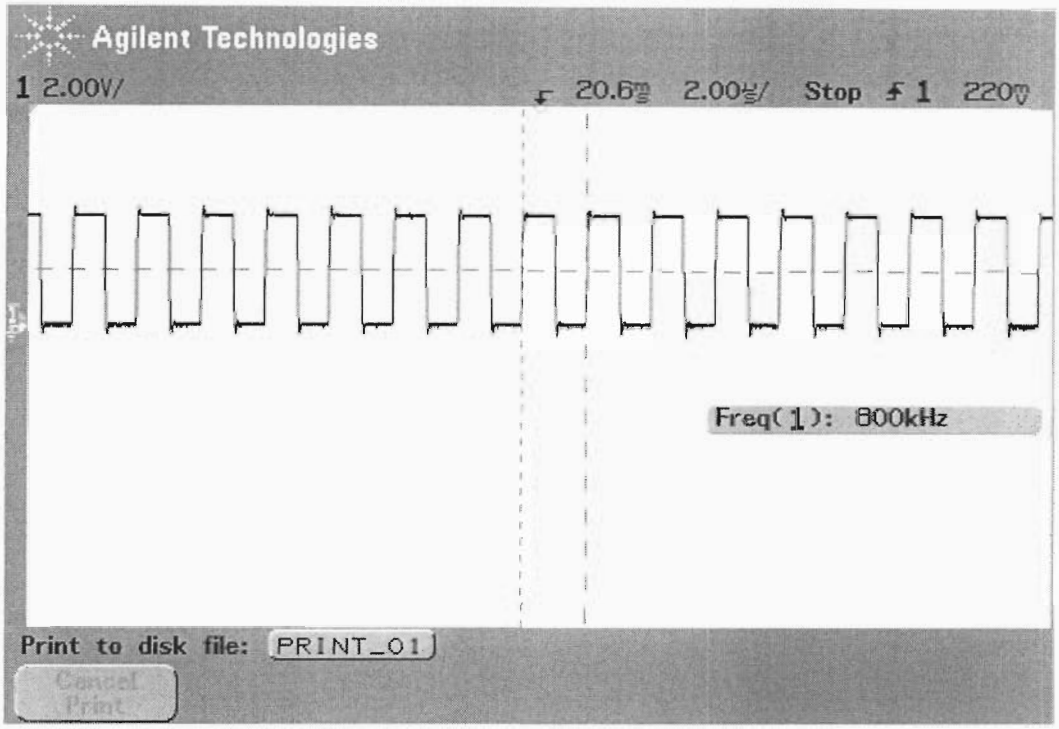

Figure D.5: Serial link clock signal waveform

The read enable serial communication signal is configured to be high for 16-bits, which signifies to the low level controller that the serial port should be read during this time. Figure D.6 shows the captured read enable signal along with the serial clock signal.

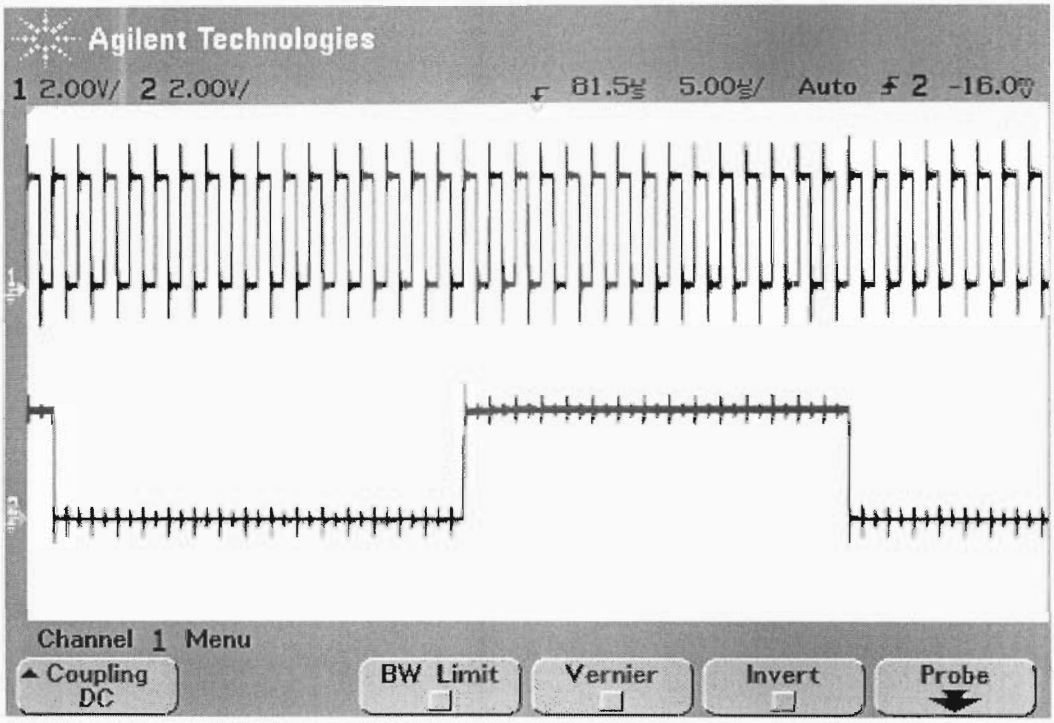

Figure D.6: Serial port clock signal (top) and 16-bit read enable signal (bottom)

The read enable signal is also configured to be active low, which means that when serial data is transmitted by the high level controller to the low level controller the read enable signal will be a logic low.

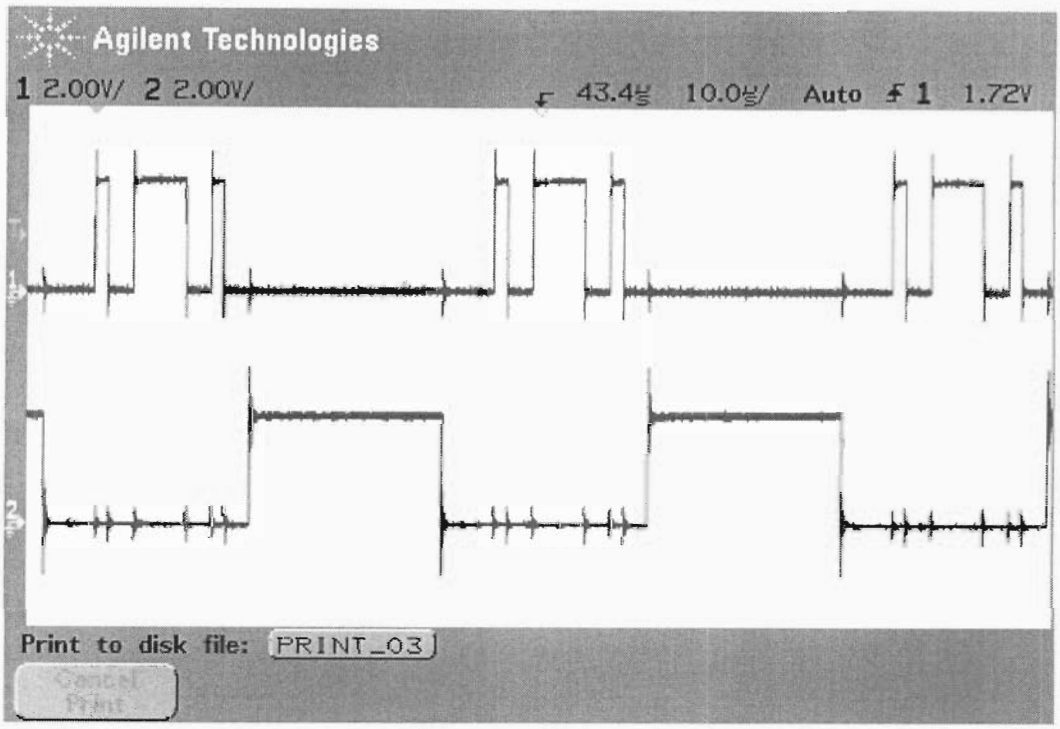

Figure D.7: Captured serial data waveform and active low read enable waveform

The final check on the serial waveforms was to ensure that the serial data is transmitted every 50 Hz for a specific thyristor. This would demonstrate that the high level controller algorithm is working as designed since, for a 50 Hz power system any given thyristor will be triggered every 20 ms.

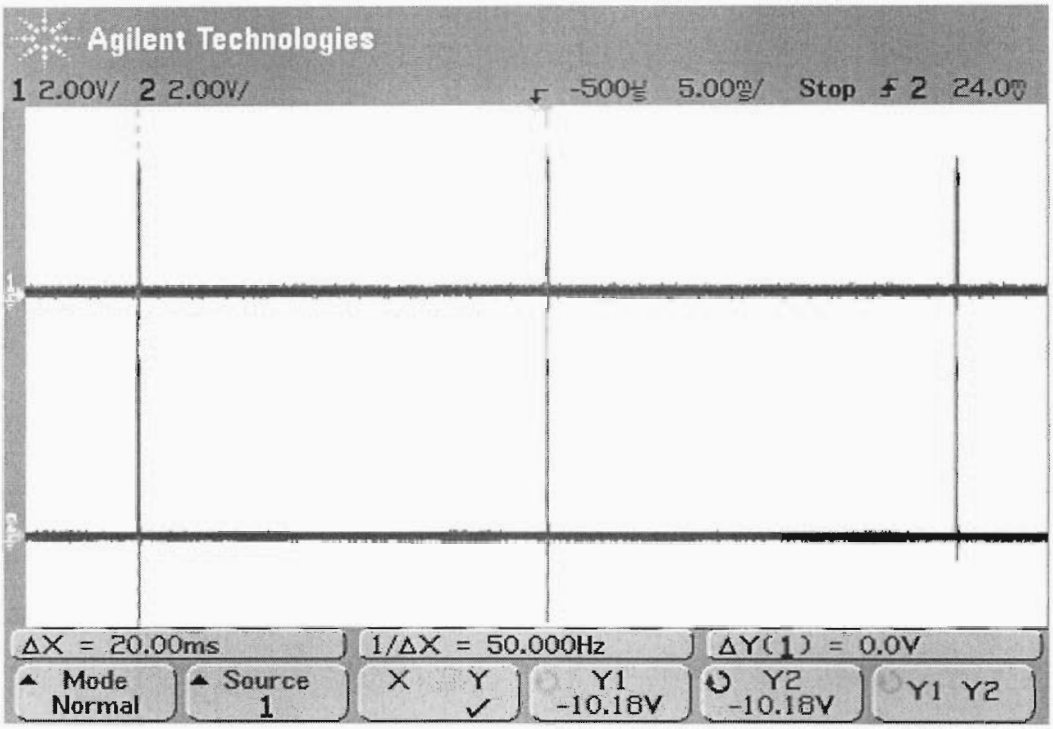

Figure D.8: Captured waveforms of the serial data and the read enable signal showing that serial data is transmitted every 20 ms for a 50 Hz power system

Appendix E

TCR inductor resistance measurement method

E.1 Introduction

The TCR inductors used in the laboratory-scale TCSC are of the air core type having copper windings. Chapter Three showed that the resistance of the TCR inductor has an adverse effect on the performance of the laboratory-scale TCSC, therefore the resistance of the TCR inductor needs to be taken into account during the analysis of results obtained for the laboratory-scale TCSC. This meant that the resistance of the inductors required measurement.

The inductors manufactured for us in the construction of the laboratory-scale TCSC have a relatively low impedance which meant that the impedance and hence the resistance of the inductors could not be calculated from voltage and current measurements. The reason is that the current required to generate a reasonable voltage across the impedance of the inductors would be high, such that the required current flow will exceed the current ratings of the copper windings used in the manufacture of the inductors.

E.2 Measurement procedure

An alternative method is to use a low power factor wattmeter to measure the active power consumed by the inductor, and from the power consumption of the inductor calculate its resistance. The inductance of the inductors was measured using an inductance measuring instrument. To reduce the required current flow, three inductors were connected in series as shown in Figure E.1.

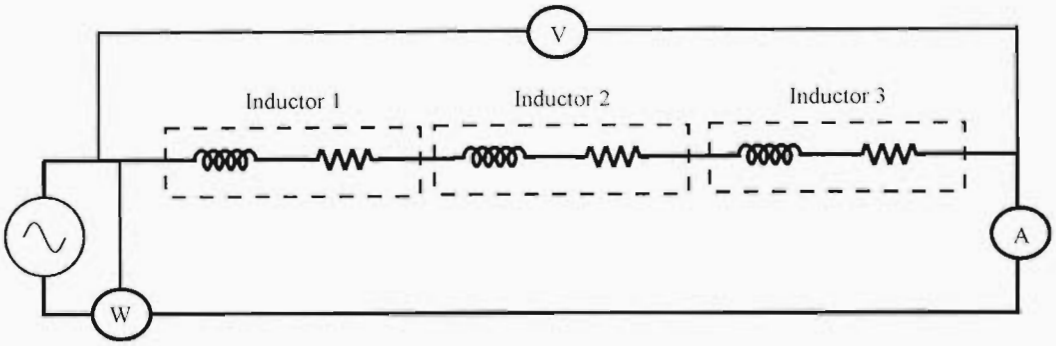

Figure E.1: Circuit used to measure inductor resistance

Figure E.1 shows the test circuit used to measure the resistance of the inductors used in the construction of the laboratory-scale TCSC. The active power, P, consumed by the three inductors was measured using the low power factor wattmeter and the current, I, flowing in the circuit was measured using the ammeter. The active power and current flow measurements were then used to calculate the total resistance of the three inductors as shown in equation (E.1).

$$R_{TOT} = \frac{P}{I^2} \tag{E.1}$$

The resistance of the individual inductors, $R_{inductor}$ was then calculated using the ratio and proportion method. Equation (E.2) shows the equation used to calculate the resistance of each inductor.

$$R_{inductor} = \frac{X_{inductor}}{X_{total}} \tag{E.2}$$

where

$X_{inductor}$ is the inductive reactance of the individual inductors at 50 Hz

X_{total} is the sum of the individual inductive reactance's of the inductors at 50 Hz

The resistance of the inductors calculated using this procedure were confirmed using a low resistance measurement instrument.

Appendix F

Original laboratory-scale TCSC step responses using the hybrid TCSC triggering controller

F.1 Introduction

Chapter Seven presented the results obtained for step responses conducted on the original laboratory-scale TCSC. This Appendix provides additional step response waveforms.

F.2 Step change in the thyristor trigger angle from 180° to 98°

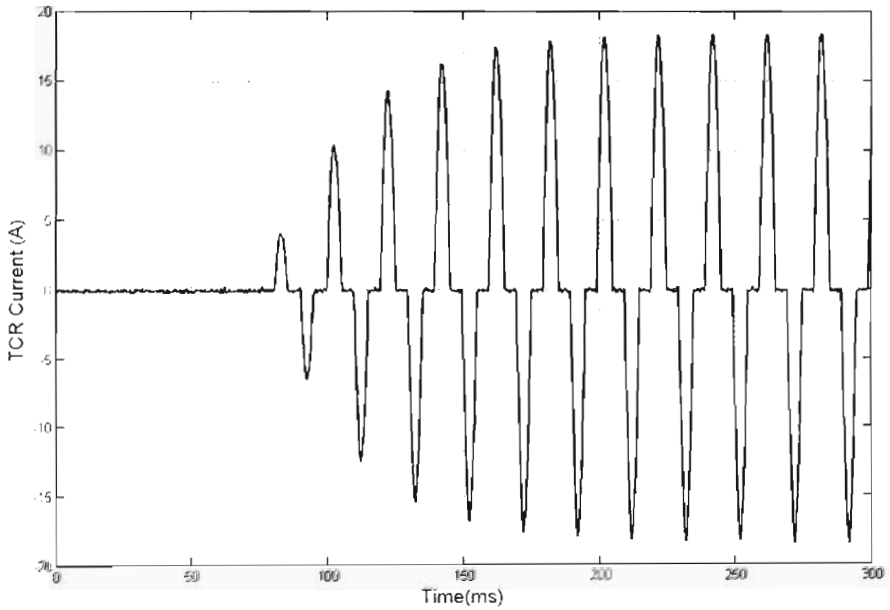

Figure F.1: TCR current waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 180° to 98°

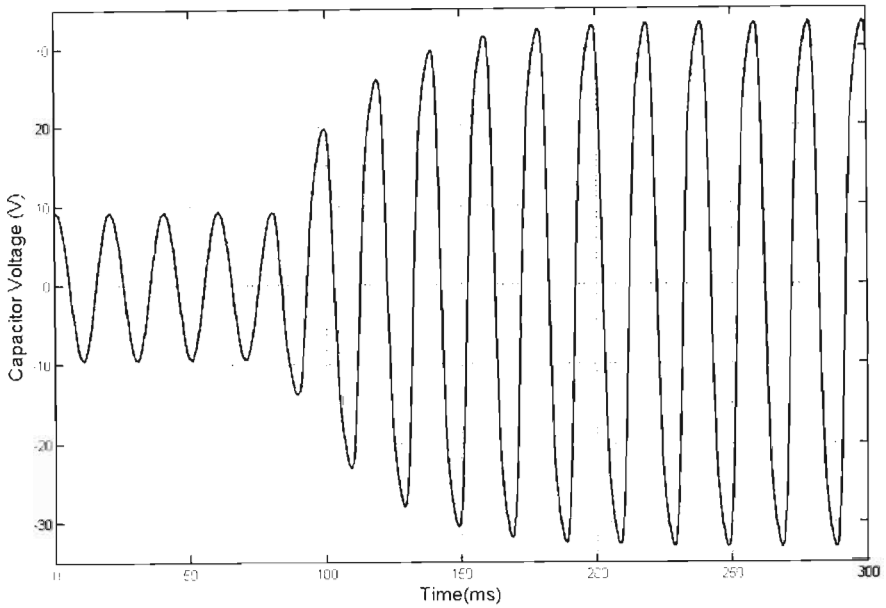

Figure F.2: TCSC capacitor voltage waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 180° to 98°

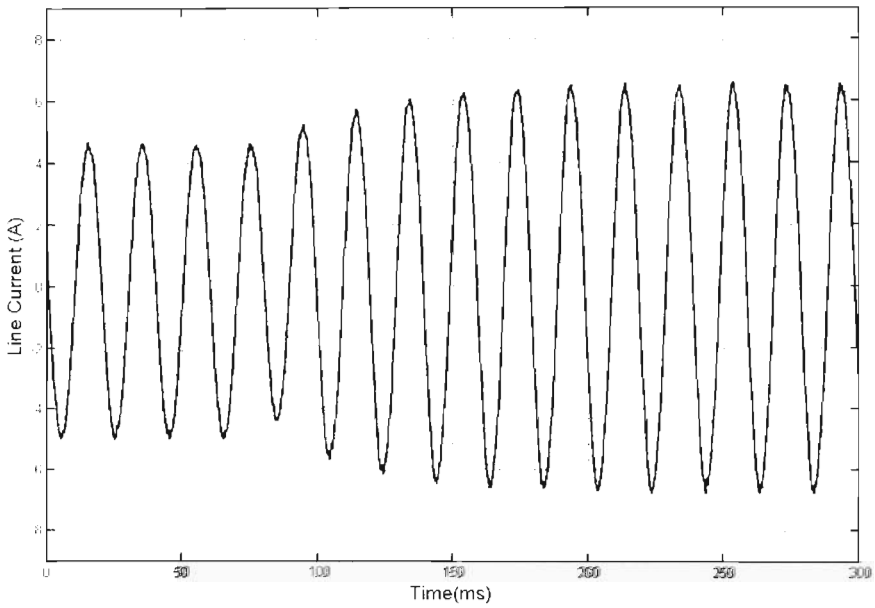

Figure F.3: Transmission line current waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 180° to 98°

F.3 Step change in the thyristor trigger angle from 98° to 130°

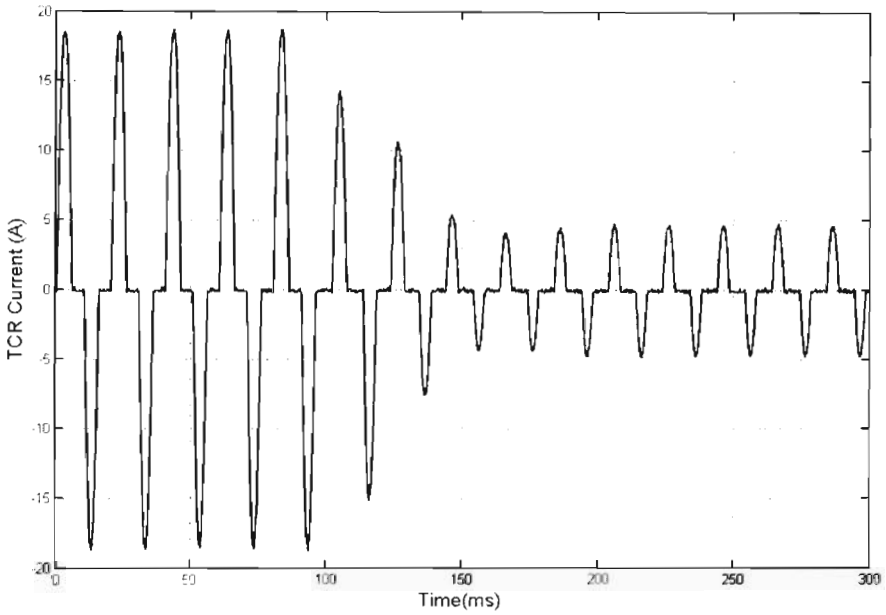

Figure F.4: TCR current waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 98° to 130°

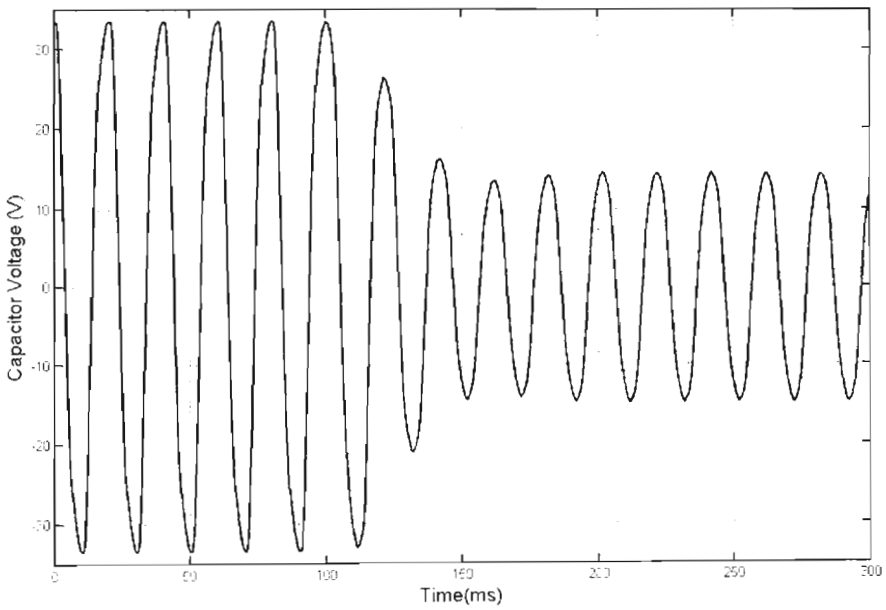

Figure F.5: TCSC capacitor voltage waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 98° to 130°

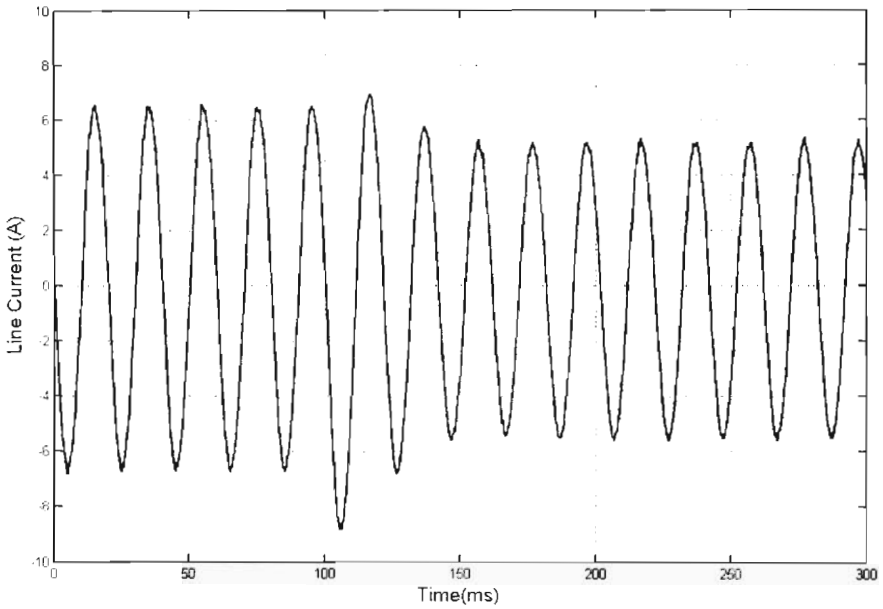

Figure F.6: Transmission line current waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 98° to 130°

F.4 Step change in the thyristor trigger angle from 98° to 180°

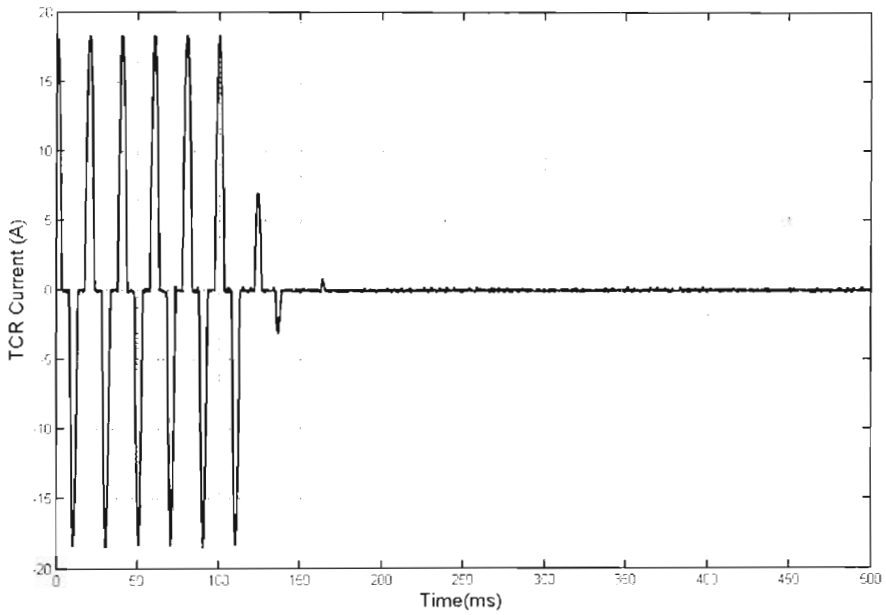

Figure F.7: TCR current waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 98° to 180°

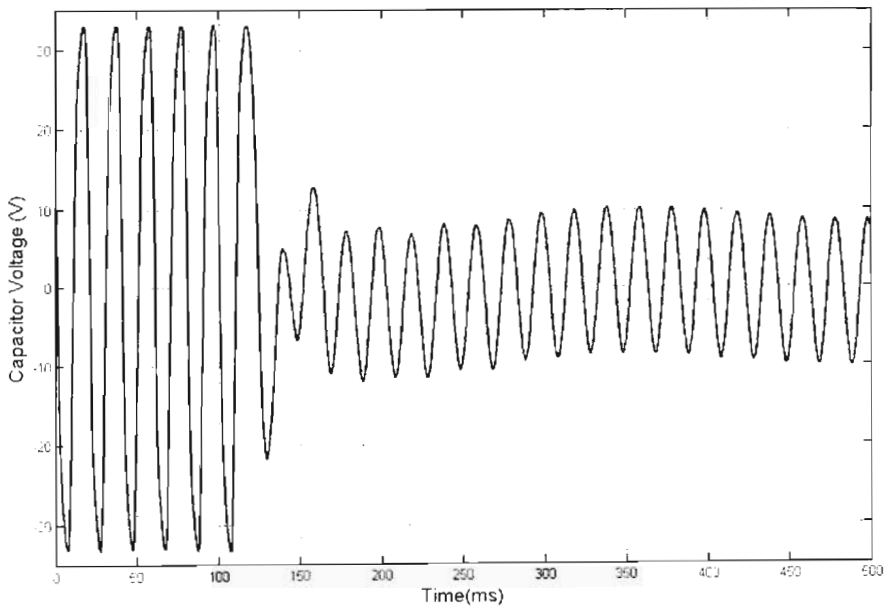

Figure F.8: TCSC capacitor voltage waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 98° to 180°

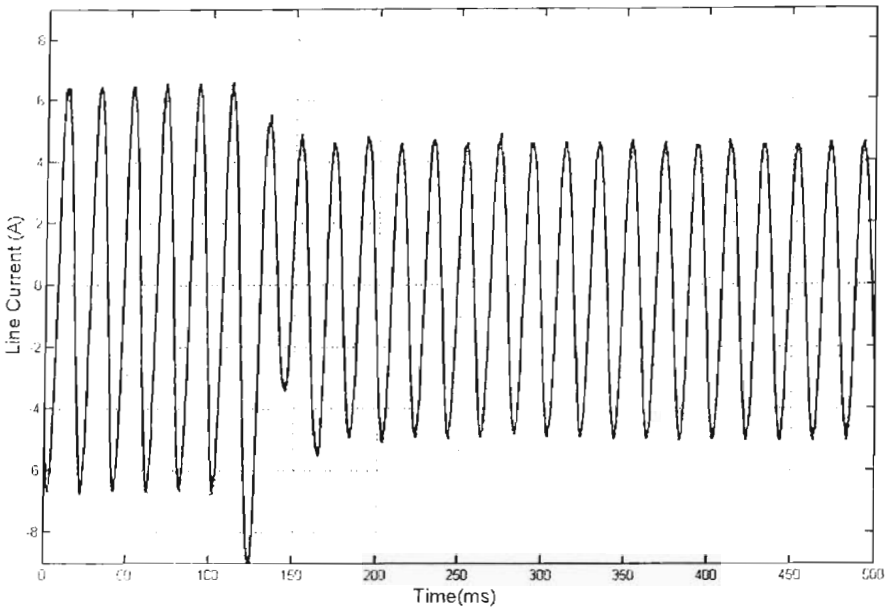

Figure F.9: Transmission line current waveform of the original laboratory-scale TCSC for a step change in the thyristor trigger angle from 98° to 180°

Appendix G

RTDS TCSC steady state waveforms using the hybrid TCSC triggering controller

G.1 Introduction

Chapter Eight presented and discussed selected TCSC waveforms obtained from the RTDS simulation studies, when the hybrid TCSC triggering controller was connected hardware-in-loop. This Appendix presents further TCSC steady state and step response waveforms obtained for different thyristor trigger angles.

G.2 Steady state TCSC waveforms

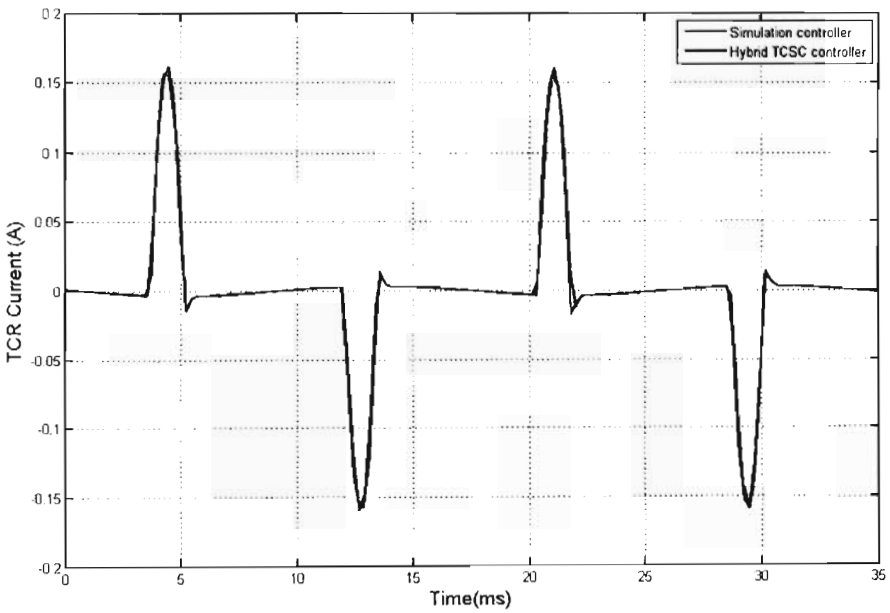

Figure G.1: Comparison of the steady state waveforms of the TCR current at a thyristor trigger angle of 163° for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

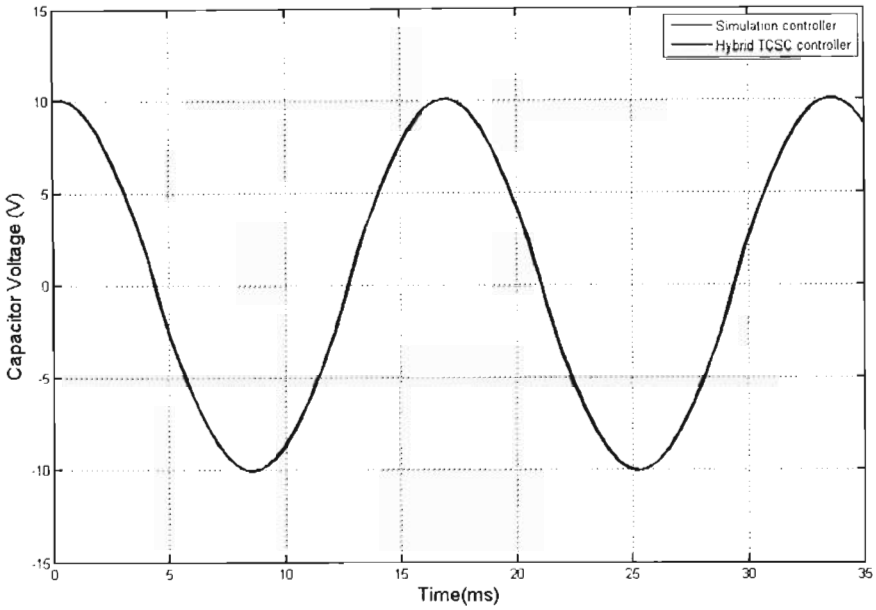

Figure G.2: Comparison of the steady state waveforms of the TCSC capacitor voltage at a thyristor trigger angle of 163° for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

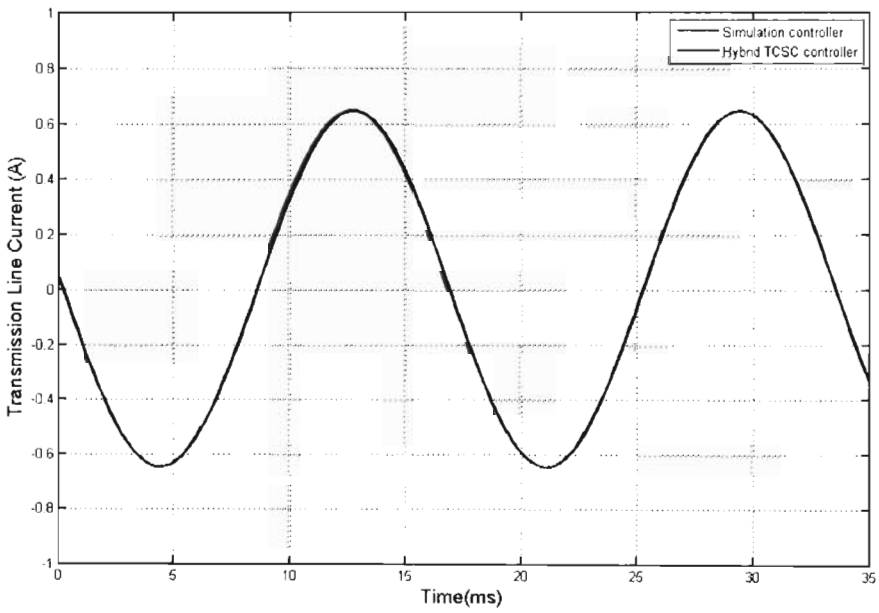

Figure G.3: Comparison of the steady state waveforms of the transmission line current at a thyristor trigger angle of 163° for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

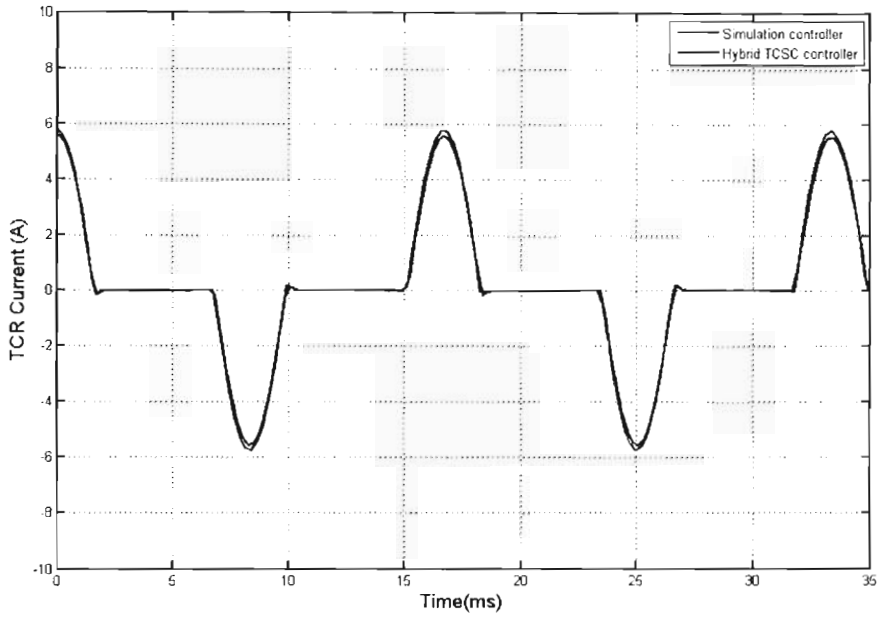

Figure G.4: Comparison of the steady state waveforms of the TCR current at a thyristor trigger angle of 144° for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

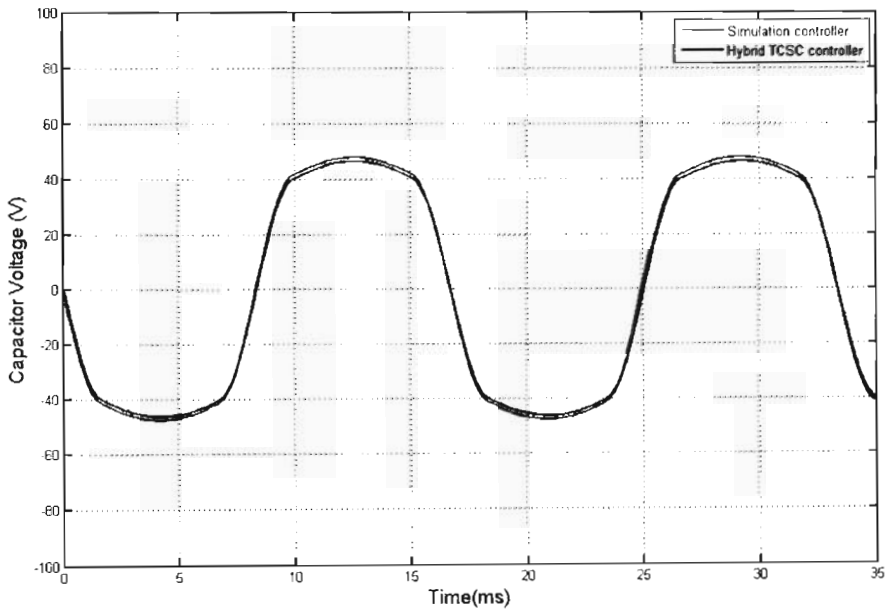

Figure G.5: Comparison of the steady state waveforms of the TCSC capacitor voltage at a thyristor trigger angle of 144° for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

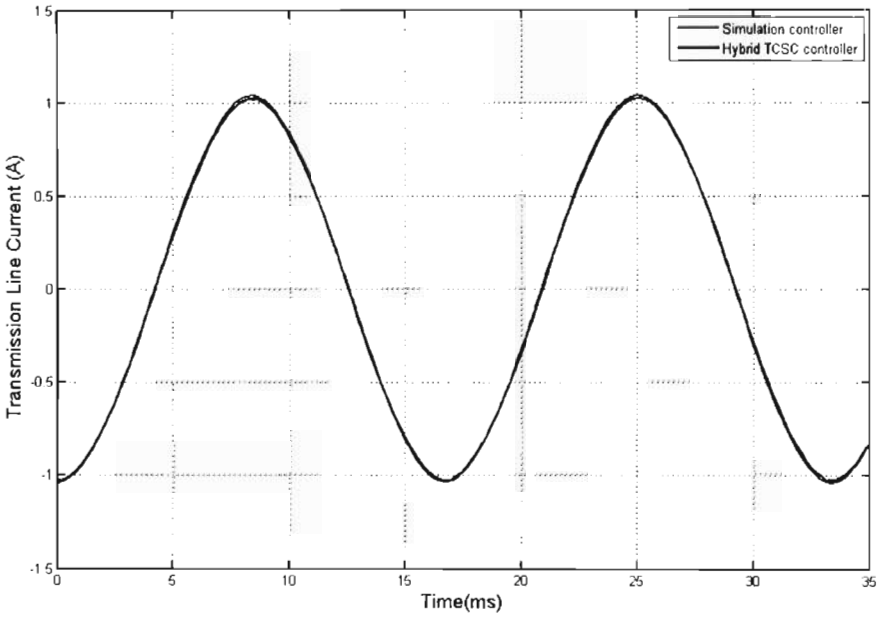

Figure G.6: Comparison of the steady state waveforms of the transmission line current at a thyristor trigger angle of 144° for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls

G.3 TCSC step response waveforms

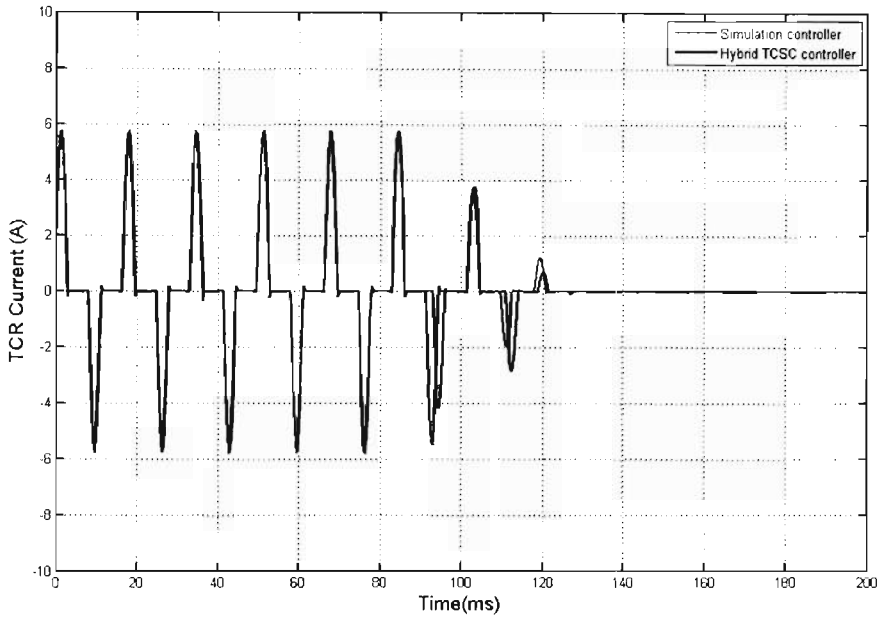

Figure G.7: Step response waveforms of the TCR current for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls obtained for a change in α from 144° to 180°

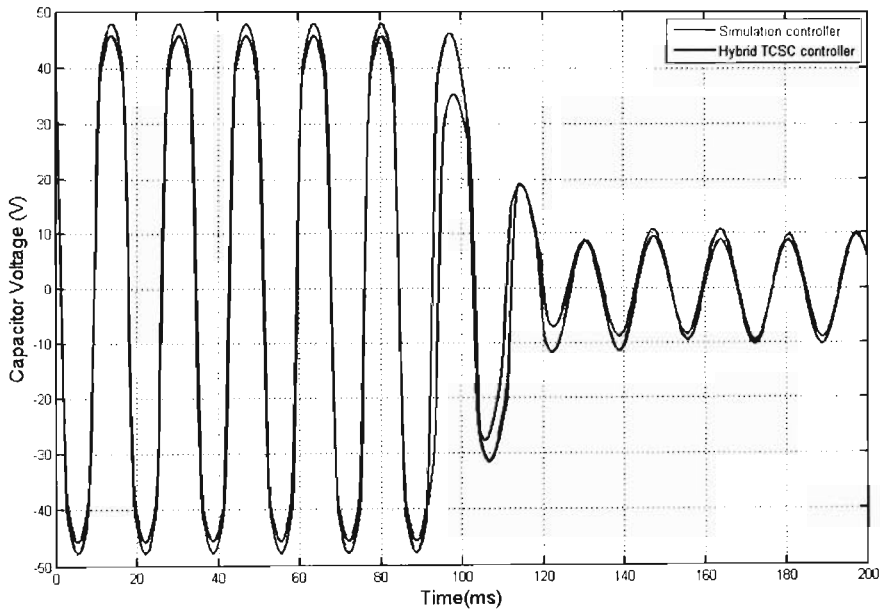

Figure G.8: Step response waveforms of the TCSC capacitor voltage for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls obtained for a change in α from 144° to 180°

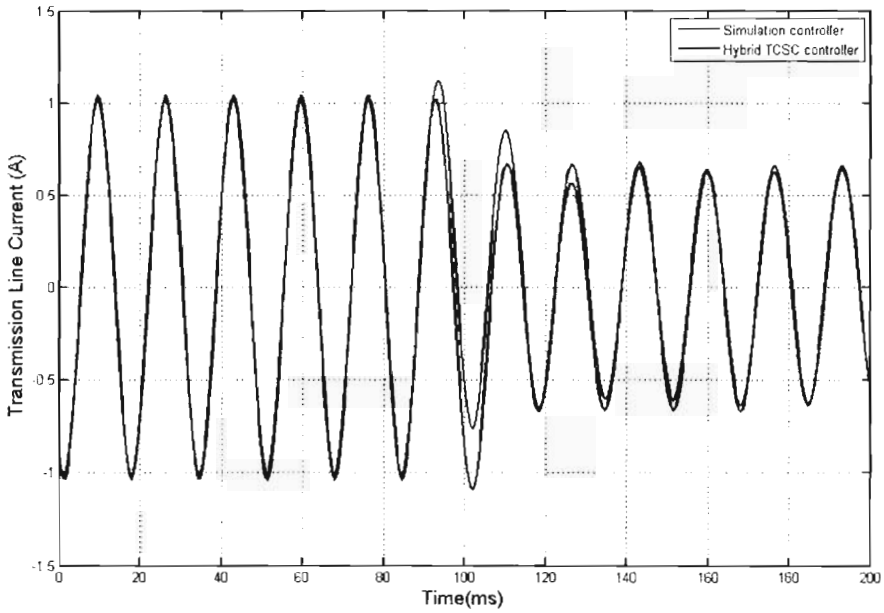

Figure G.9: Step response waveforms of the transmission line current for the hybrid controller connected hardware-in-loop and the all-simulation model of the TCSC controls obtained for a change in α from 144° to 180°

Appendix H

RTDS TCSC waveforms

H.1 Introduction

Chapter Eight presented and discussed results obtained from the RTDS tests. The hybrid TCSC triggering controller and the Kayenta TCSC (simulated within the RTDS) was used to damp inter-area mode oscillations. A power oscillation damping controller (simulated within the RTDS) was used to determine the level of series compensating reactance required to damp the inter-area mode oscillations. This Appendix provides additional waveforms showing specifically the TCSC waveforms when the hybrid TCSC triggering controller was connected hardware-in-loop to generate the triggering signals to the TCSC.

H.2 Synthesised speed difference

Figures H.1, H.2, and H.3 show the envelope of the transmission line current, TCSC capacitor voltage and TCR current. All three figures show that the amplitude and frequency of the envelope decay with time, meaning that the TCSC is damping the inter-area mode oscillations.

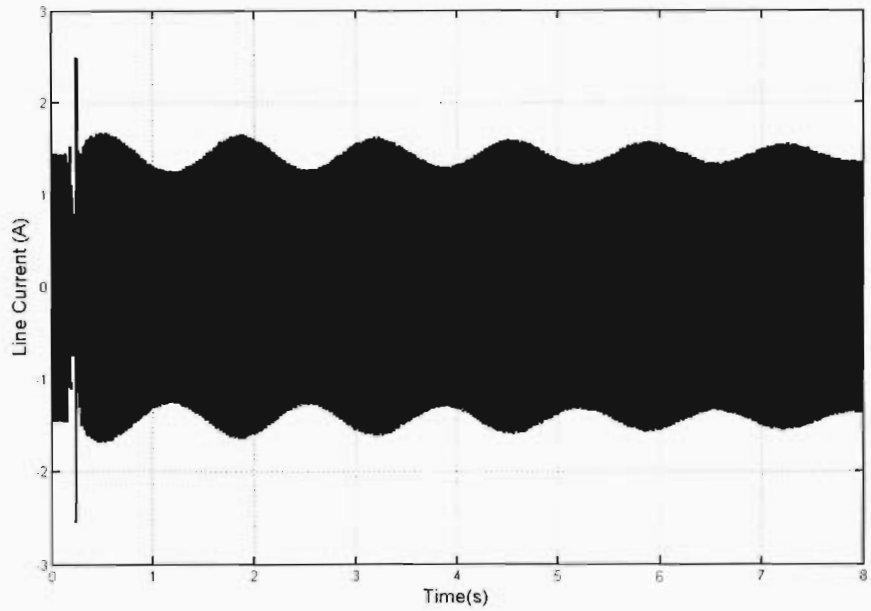

Figure H.1: Transmission line current envelope for inter-area mode oscillations: POD input signal - Synthesised speed difference

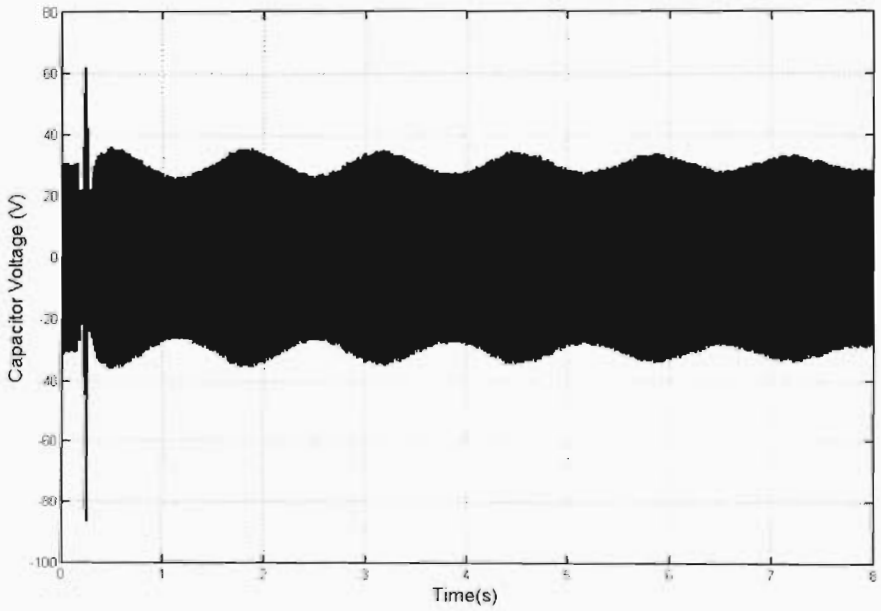

Figure H.2: TCSC capacitor voltage envelope for inter-area mode oscillations: POD input signal - Synthesised speed difference

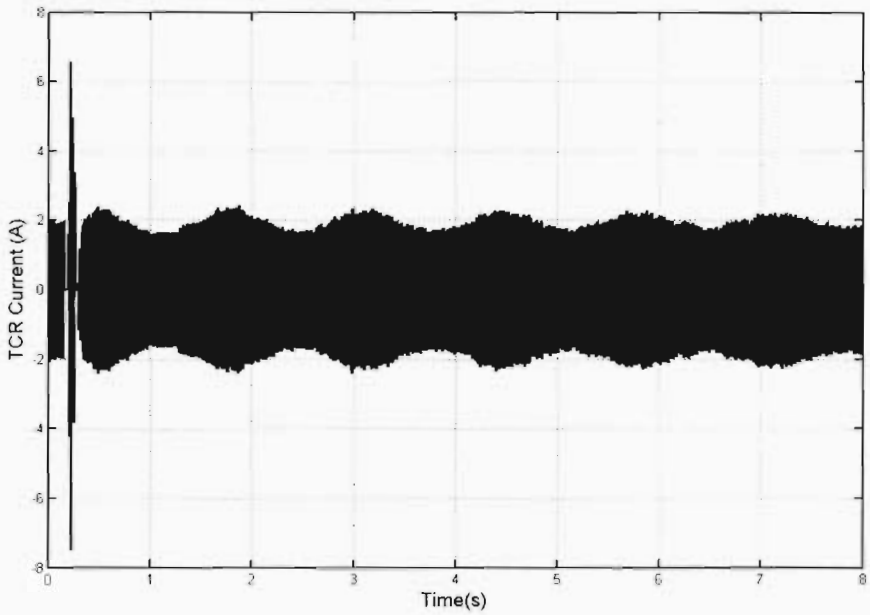

Figure H.3: TCR current envelope for inter-area mode oscillations: POD input signal - Synthesised speed difference

H.3 Direct speed difference

Figures H.4, H.5 and H.6 show a zoomed version of the TCSC waveform envelope presented in the previous section. Figures H.4, H.5 and H.6 show the initial response of the transmission line current, TCSC capacitor voltage and TCR current.

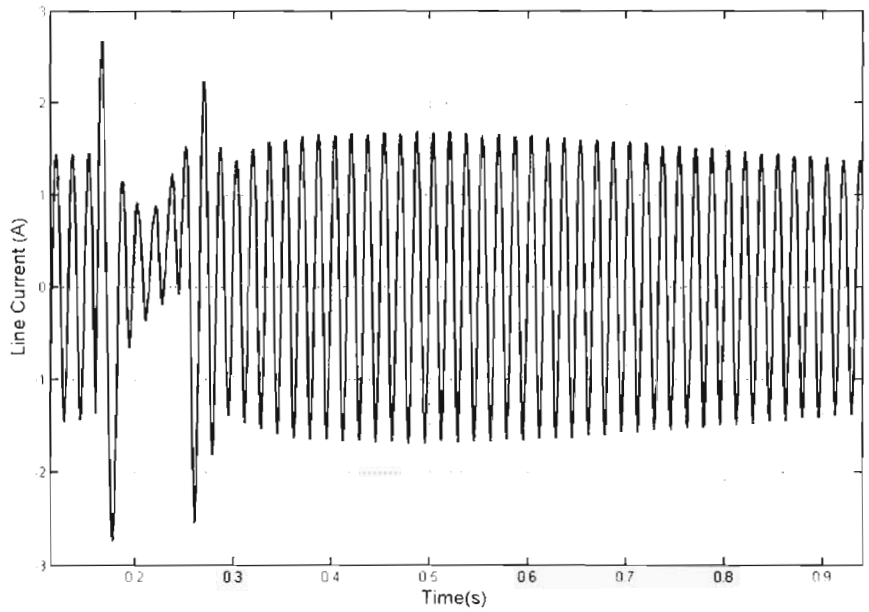

Figure H.4: Transmission line current response for inter-area mode oscillations: POD input signal - Direct speed difference

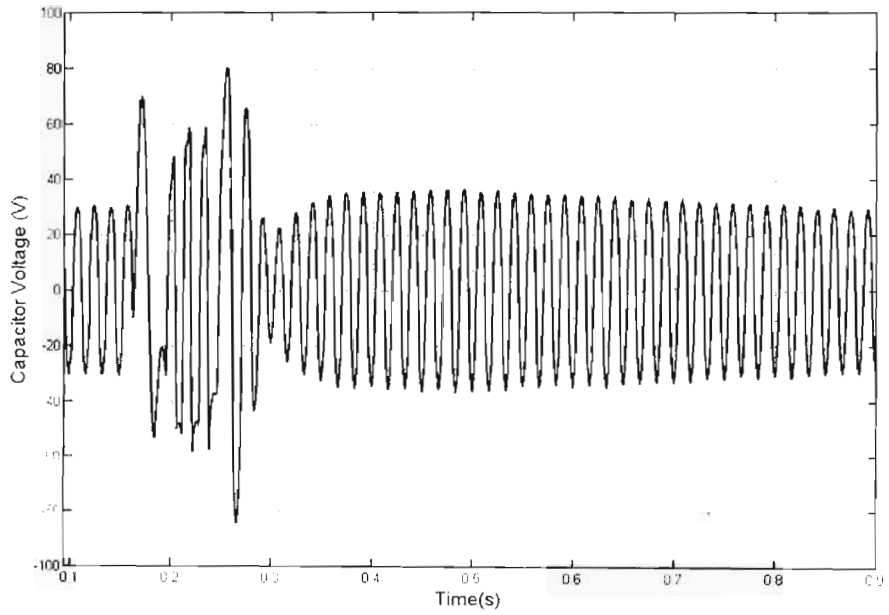

Figure H.5: TCSC capacitor voltage response for inter-area mode oscillations: POD input signal - Direct speed difference

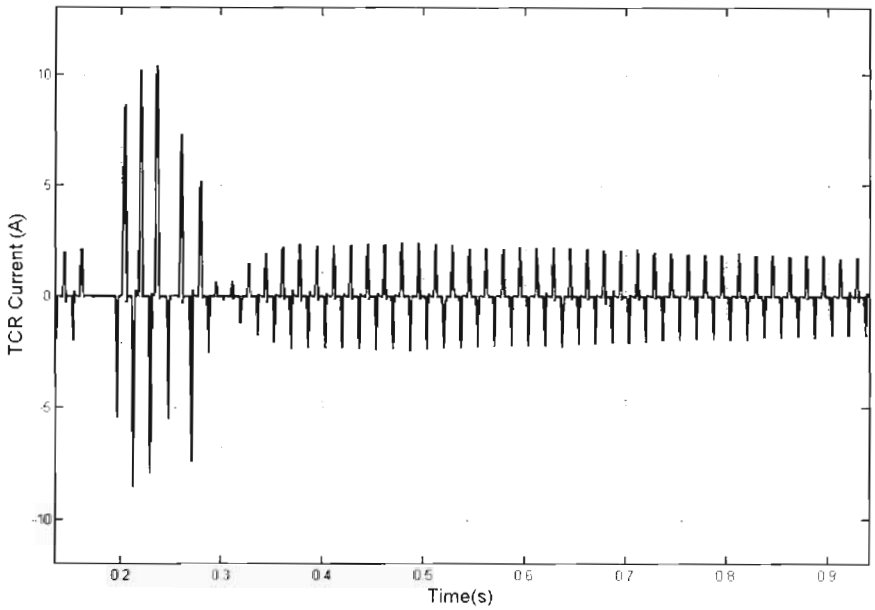

Figure H.6: TCR current response for inter-area mode oscillations: POD input signal - Direct speed difference

H.4 Rate of change of power flow

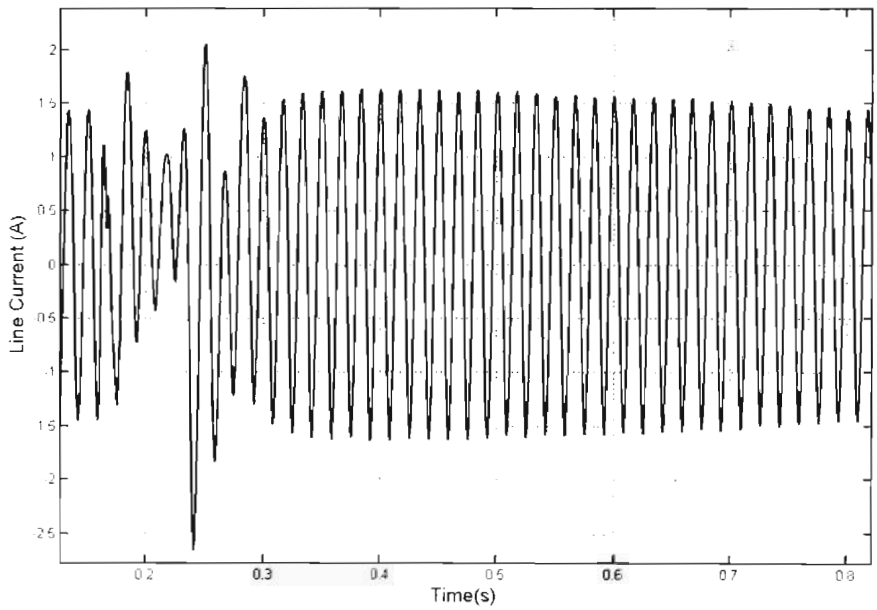

Figure H.7: Transmission line current response for inter-area mode oscillations: POD input signal – Rate of change of power flow

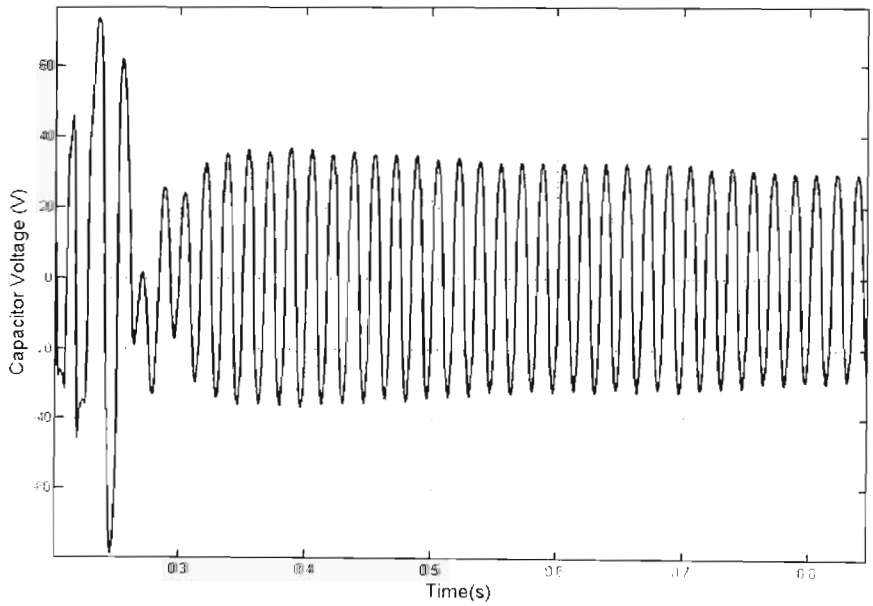

Figure H.8: TCSC capacitor voltage response for inter-area mode oscillations: POD input signal – Rate of change of power flow

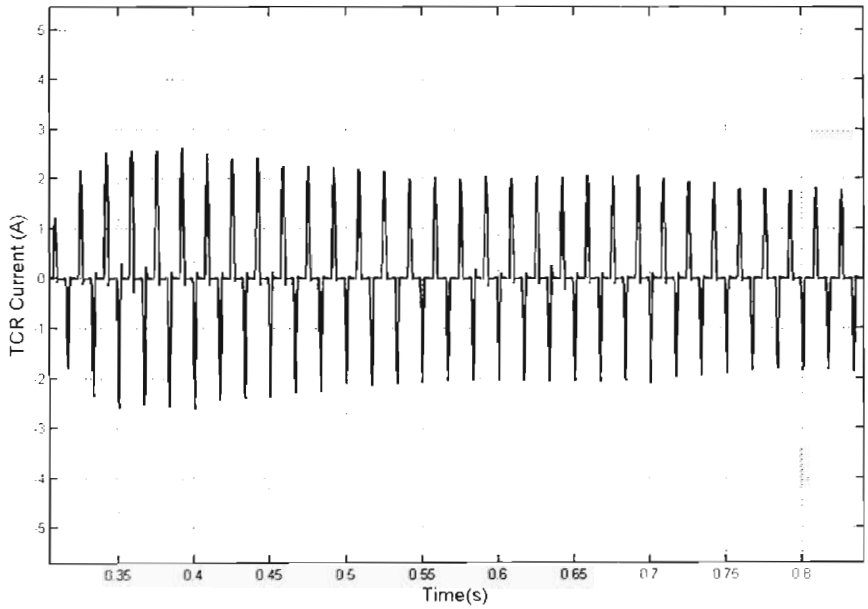

Figure H.9: TCR current response for inter-area mode oscillations: POD input signal – Rate of change of power flow

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