DESIGN AND PARAMETRIC ANALYSIS OF PROTOTYPED DIFFERENTIAL AMPLIFIER USING DOUBLE-GATE MOSFET

A dissertation submitted in fulfilment of the degree for the degree of

MASTER OF SCIENCE

In

Electronic Engineering

By

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Declaration-1

PLAGIARISM

I, **Thabiso Tekisi,** with Student Number **216035409** and the thesis entitled "Design and Parametric Analysis of Prototyped Differential Amplifier using Double Gate MOSFET',hereby declare that:

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I, Thabiso Tekisi declare that these publications were a result of my own work presented in this thesis:

- **Thabiso Tekisi** and Viranjay M. Srivastava**,** "Parametric analysis of prototyped differential amplifier using double-gate MOSFET," ***Int. J. of Engineering Trends and Technology*** *(ETT),* vol. 71, no. 6, pp. 33-46, June 2023.
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- **Thabiso Tekisi** and Viranjay M. Srivastava, "Analytical approach for losses in differential amplifier using double-gate MOSFET," ***14th IEEE Int. Conf. on Mechanical and Intelligent Manufacturing Technologies*** *(ICMIMT)*, Cape Town, South Africa, 26-28 May 2023, pp. 59-63.
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- **Thabiso Tekisi** and Viranjay M. Srivastava, "Analytical approach towards low power device (differential amplifier) using DG MOSFET," ***31st South African Universities Power Engineering Conference*** *(SAUPEC)*, Johannesburg, South Africa, 24-26 Jan. 2023, pp. 152-156.
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- **Thabiso Tekisi** and V. M. Srivastava, "Transient Analysis of Differential Amplifier Using Double-Gate MOSFET," *2023 International Conference on Electrical, Computer and Energy Technologies (ICECET)*, Cape Town, South Africa, 2023, pp. 1-4,
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Signe[redacted]…….... Date 23rd July 2023

Name: Mr. Thabiso Tekisi

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DEDICATION

This thesis is dedicated to my late mother, Busisiwe Nobono Mngxalaba, my father, George Cele, and my stepmother, Molly Mnguni, and the entire Mngxalaba and Cele family.

To God be the Glory.

ABSTRACT

Differential Amplifiers (DA's) are extensively utilized in a wide variety of electronic circuits, including operational amplifiers, instrumentation amplifiers, and Communication Systems (CS's). They are typically built with BJTs and MOSFETs. Nevertheless, each type of transistor presents its own set of barriers when designing a DA. Amongst other challenges with BJTs is suffering from input base-emitter junctions with non-ideal input impedance. Decreased gain and loading effects may come from this. Due to the base-to-emitter voltage's dependence on temperature, they are susceptible to temperature changes, and they have a limited input voltage range, beyond which the transistors can be damaged. On the other side, Because of gate-source capacitance and gate leakage current, Single-Gate (SG) MOSFETs are more prone to noise; they suffer from Short Channel Effect (SCE) and have a limited input voltage range.

The design process for a DA using a double gate MOSFET is presented in this work. The double gate MOSFET is a potential contender for use in analog circuit design because of its improved EC, low noise characteristics, reduced SCEs, and power consumption. The DA circuit proposed comprises two double-gate MOSFETs, BF998, constructed in a differential pair with a resistive load and a Constant Current Source (CCS). The proposed circuit is designed and simulated using a multism tool and was also constructed on Vero Board (VB). Various parameters are analysed on both simulated and practical circuits, such as differential output voltage gain, Common Mode Voltage Gain (CMVG), Common Mode Rejection Ratio (CMRR), Frequency Response (FR), and losses, to observe the performance of the proposed circuit. Simulated results for a differential voltage gain, common-mode gain, CMRR, and FR were obtained to be *24 dB, -224.22 dB, 246.86 dB,* and *65 MHz*, respectively. Practical results were obtained to be *24.44 dB, -73.81 dB,* and *98.29 dB.*

A comparison has been made between the proposed circuit and the already existing designs, and the findings demonstrate that, when compared to traditional BJT and MOSFET-based DA's, the presented DA using a double gate MOSFET offers considerable improvements in terms of differential voltage gain, cut-off frequency, CMRR, reduced SCEs, linearity, and noise performance. Therefore, based on these results, the designed DA is justified for use in operational amplifiers as input stage, RF, and other low-power electrical/electronic devices.

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LIST OF ABBREVIATIONS

DA	Differential amplifiers
BJT	Bipolar junction transistors
CS	Communication systems
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SCE	Short-Channel Effect
EC	Electrostatic Control
VB	Vero-Board
CMRR	Common Mode Rejection Ratio
CMVG	Common Mode Voltage Gain
ASM	Asymmetrical Mode
SM	Symmetrical Mode
CCS	Constant Current Source
FR	Frequency Response
SG	Single-Gate
HG	High Gain
VD	Voltage Difference
VLSI	Very Large-Scale Integration
ADC	Analog-to-Digital Conversion
CBJ	Collector-Base Junction
EBJ	Emitter-Base Junction
V	Voltage
W	Watt
VT	Vacuum Tubes
KVL	Kirchhoff's Voltage Law
DM	Differential Mode
DG	Differential Gain
CL	Conduction Loss
RLDA	Resistive Loaded Differential Amplifier

Chapter-1

INTRODUCTION

1.1 Background

The background of the technological development of electronic amplifiers is particularly fascinating since it demonstrates the value of chance and meticulous technological progress in research methods. The principles upon which electrical amplifiers function are nicely illustrated by a very simple glance at the important aspects of their development. *Thomas Edison* is often credited with inventing the electric light bulb. Few people realize that he also identified a phenomenon known as the "Edison effect" that also served as the foundation for the invention of the electronic amplifier [1]. At the beginning of the 20^{th} century, the first Differential Amplifier (DA) was built, marking a tremendous technological advancement. Vacuum tubes, the main electrical devices then, were used in the DA's design. The earliest DA's design presented a problem since precise common-mode rejection required perfect tube matching. The tube's temperature instability was a major impediment as well. Engineers employed various methods to address these issues, such as biasing the tubes with a constant current source and stabilizing the amplifier. Such methods had first been put forth by *Black* [2], who established the idea of negative feedback and enabled the amplifiers to operate steadily. Utilizing negative feedback in the design allowed for better control of the gain and input impedance and good common-mode rejection. *Heising* [3] designed a DA using vacuum tubes (VT's) in a push-pull configuration. A detailed analysis of the circuit's performance was also discussed, including the measurement of FR, gain, and distortion. Some of the external factors that affect the performance of the amplifier include temperature, humidity, and electromagnetic interference. *Sikora* [4] proposed the design of a DA using a 12AX7 tube, which was widely used in guitars and other audio devices. The effect of the load impedance on the circuit distortion and the gain of the amplifier was also discussed. Techniques were also provided to improve the performance of the designed amplifier.

The invention of solid-state transistors in the 1950s enhanced the DA performance even further, resulting in their extensive use in various applications such as diagnostics, control systems, and communications [2, 5]. Electronic signals can be amplified and switched by transistors, which are semiconductor devices. They are frequently built using Field-Effect

Transistors (FETs) and BJTs. These devices are three-layer semiconductor devices with bases, emitters, and collectors. The emitter and collector regions are doped differentially to make an NPN or PNP transistor. The base area, which is wedged between the emitter and collector, is minimally doped. Two BJTs are typically employed in a DA in a "long-tailed pair" configuration, where the emitters are coupled together, and the collectors are connected to a common load resistor. In contrast, FETs are voltage-controlled devices with a gate, source, and drain terminal. Two FETs are typically employed in a DA in a common source configuration, where the sources are coupled together, and the drains are connected to a common load resistor. Because FETs have such a larger input impedance than BJTs, they are appropriate for high-impedance applications [6-8]. Furthermore, because of their enhanced reliability and performance, as opposed to VT's and BJTs, they are frequently employed in the design of DA's. These devices draw extremely little current from the signal source due to their high input impedance, which minimizes loading effects and enhances amplifier performance overall, which is one of the main reasons they have been selected. Moreover, they have low noise characteristics, which adds the very least amount of noise possible to the amplifier circuit- a crucial factor in low-level signal applications. These devices also have high gain, which makes it possible for them to amplify small signals to significant amplitudes, which is essential in situations where the signal levels are minimal, just as in biomedical sensors and instruments. In situations where the amplifier needs to react quickly to changes in the signal, just as in communication systems, their high-speed features allow them to function at high frequencies [6,9]. The major role or impact played by BJT when used to design a DA is demonstrated in ref. [10], where a silicon carbide fully DA characterized up to 500 ^{o}C was designed. Achieving a low input impedance is very vital; as a result, a base current compensation technique was used to obtain it. A relatively high linearity and low offset demonstrated the potential of this device to be investigated to improve the amplifier's performance. *Hashem* [11] designed and analyzed a BJT-based DA to measure the performance of the circuit by determining the output resistance and DM voltage gain. It was obtained that when the biasing current decreases, it causes an increase in the circuit's output resistance and eventually causes a decrease in differential voltage gain.

The single-gate MOSFETs, with their high switching speed and high input impedance, made them more suitable than BJTs when designing a DA or any other electronic signal processing circuit. *Kokhtari* and *Kabiri* [12] proposed and designed a new multi-valued logic buffer and inverter that utilized a MOSFET-based DA. The operating voltage range and the

linear gain of the proposed circuit were obtained from 0 V to 5.5 V and 0.1 V to 5.3 V. The use of this low-powered device could achieve good results. Moore's law states that the number of transistors in an integrated circuit doubles every two years. *Gordon Moore* proposed the theory of technology scaling on transistors in 1965, and it has since become a driving force behind Intel's semiconductor technology. The lowering of horizontal and vertical dimensions of the transistor chip, as well as the reduction of supply voltage V_{DD}, minimizes power dissipation and overcomes oxide breakdown [13-15]. This has led to the developing a low-power and high-frequency device, double-gate MOSFET. DG MOSFETs are devices with two gates rather than one. The device comprises a thin Silicon body with a source and drain region on opposite sides and two gates on each side. The gates are electrically insulated from one another and regulate current flow through the channel region between the source and drain. These are especially beneficial in applications requiring high performance and low power consumption, including mobile devices, medical equipment, and sensors, because they have higher current density and improved electrostatic control [16].

1.2 Problem Statement

A fundamental component in analog integrated circuits, the differential amplifier plays a pivotal role by amplifying the voltage disparity between two input signals, commonly employed in operational amplifier input stages. However, downsizing silicon-based transistors presents significant challenges due to technological limitations, including thin insulating layers and shortened electron paths to meet the demands of nanotechnology. To address concerns surrounding power dissipation in older bipolar junction transistors (BJTs), MOSFETs were introduced in VLSI circuits, offering lower power consumption and enabling more components to be accommodated within the same chip area. Nonetheless, MOSFET-based short-channel devices encounter drawbacks like drain-induced barrier lowering, surface scattering, and hot carrier effects, leading to eventual degradation [17].

Resistive-load differential amplifiers (RLDAs) are essential components in various electronic systems, providing amplification and signal processing capabilities. However, despite their widespread use, previous research has predominantly focused on synchronous mode operation, where both gates are supplied with the same signal neglecting the potential advantages offered by asynchronous mode operation, where each gate is supplied with a different signal or drove separately. This provides more control on the channel since gate 2 is responsible for transconductance and current characteristics of the DG MOSFET.

A critical gap exists in the literature regarding the exploration and optimization of resistive-loaded differential amplifiers using DG MOSFET in asynchronous mode. Existing studies have demonstrated suboptimal performance in terms of output gain, CMRR, and FR, indicating a significant area for improvement and exploration. Furthermore, the lack of research into asynchronous mode operation of the DG MOSFET limits the understanding of its potential benefits, including enhanced flexibility, reduced power consumption, and improved noise performance.

Addressing these gaps is imperative for advancing the design and performance of resistive-load differential amplifiers, enabling their effective integration into a wide range of electronic systems and applications.

1.3 Research Objectives

The primary objectives of this research are to:

- Design and fabricate low-power reliable double-gate based DA.
- Achieve a high output voltage gain and wide bandwidth than existing solutions.
- Perform DC and AC analysis of the proposed solution.
- Do a parametric analysis of gain, common mode gain, FR, and losses.
- Result comparison with existing solutions to verify the performance of the proposed solution.

1.4 Significance of Research

The development of double-gate based Differential Amplifiers (DAs) represents a significant advancement in amplifier technology. This emerging design has garnered attention for its superior performance compared to traditional Bipolar Junction Transistors (BJTs) and Single-Gate (SG) based DAs. Notably, double gate-based DAs offer compelling advantages including enhanced switching speed, reduced power consumption, and minimized noise levels. At the heart of its superiority lies the unique structure of the device, which affords precise control over the channel, thereby optimizing amplifier performance while mitigating channel noise. This precise control translates into improved functionality across a spectrum of

applications, particularly in scenarios requiring high-speed operation, such as within Communication Systems (CSs) and medical equipment.

Moreover, double gate-based DAs demonstrate remarkable capability in operating at higher frequencies compared to BJTs and SG amplifiers, positioning them as ideal solutions for demanding high-frequency applications. By addressing prevalent challenges encountered in amplifier design, such as inadequate gain, excessive noise, and limited common mode rejection ratio, the double-gate (SiO_2) based DA emerges as a promising solution. Its potential to revolutionize amplifier technology is underscored by its ability to deliver superior performance across various parameters, thereby meeting the evolving needs of modern engineering applications.

1.5 Methodological Approach

Designing a DA using a double-gate MOSFET involves several sequential steps. Determining the requirements and the specifications for the DA is the most important in completing the project, and this involves determining single-ended and differential output voltage gain, common-mode output voltage gain, CMRR, and frequency response. Secondly, amongst different versions of double-gate MOSFETs, a suitable device, BF998, has been chosen for this work because it meets the requirements such as high switching speed, low threshold gate voltage, and low power consumption. Thirdly, the circuit topology is then chosen. The basic structure of a DA consists of two matched transistors, and their source terminals are connected together to form a common source amplifier. Two matched drain resistors are also utilized. This basic structure has been employed in this work to make the proposed solution compact and small. So, two matched double-gate MOSFETs; two matched drain resistors have been used to design this common-source DA. Simulation of the common-mode DA has been done using a software, Multism, because there are many features on this software that can be used to analyse the performance of the amplifier. This includes single-ended, differential probes, and oscilloscopes. The designed circuit is then analysed using the available tools on the software to determine voltage gain, CMRR, FR, etc. Afterward, the proposed circuit is then fabricated on the Vero-board using BF998 double-gate MOSFET, resistors, and other electronic components. The comparison between simulated, practical, and already existing results is done to verify the performance of the designed amplifier.

1.6 Thesis Organisation

This work is organized and divided into six chapters and is summarised as follows:

Chapter 1 – This chapter explains the background information on DAs and the work conducted, the problem statement, the significance of the research, and the method used to complete this research work.

Chapter 2 – Details the information about DAs and their different types, various devices, and transistors (VT's, BJT, SG, and DG MOSFET) used to construct DAs. The advantages and disadvantages of using these devices are also discussed.

Chapter 3 – Mathematical design and proposed solution for this research work have been analysed in this chapter. The components and tools used to design this work are also discussed.

Chapter 4 Presents the proposed design's parametric analysis with single-input, single-output, single-input, and differential-output results. Comparison is also performed with already existing work.

Chapter 5 – Provides an analysis of a differential amplifier's performance when utilized with both differential input and output configurations. Loses are also analysed, which include conduction, switching, and power losses.

Chapter 6 – This chapter presents the prototyped design of a DG-based DA. Parametric and comparative analysis has been done by comparing already simulated, prototyped, and existing designs.

Chapter 7 - In this section, the summary of this work is presented, with a comparison and validation of the proposed work. Future improvements in this work include what to include in the fabricated circuit to improve the system's performance.

1.7 List of Publications

- **Thabiso Tekisi** and Viranjay M. Srivastava**,** "Parametric analysis of prototyped differential amplifier using double-gate MOSFET," ***Int. J. of Engineering Trends and Technology*** *(ETT)*, vol. 7, no. 6, pp. 33-46, June 2023.
  (DOI: 10.14445/22315381/IJETT-V71I6P205) ***[SCOPUS]***

- **Thabiso Tekisi** and Viranjay M. Srivastava, “Analytical approach for losses in differential amplifier using double-gate MOSFET,” ***14th IEEE Int. Conf. on Mechanical and Intelligent Manufacturing Technologies*** *(ICMIMT)*, Cape Town, South Africa, 26-28 May 2023, pp. 59-63.
  (DOI: 10.1109/ICMIMT59138.2023.10200549*)* ***[IEEE Xplore]***

- **Thabiso Tekisi** and Viranjay M. Srivastava, “Analytical approach towards low power device (differential amplifier) using DG MOSFET,” ***31st South African Universities Power Engineering Conference*** *(SAUPEC)*, Johannesburg, South Africa, 24-26 Jan. 2023, pp. 152-156.
  (DOI: 10.1109/SAUPEC57889.2023.10057691) ***[IEEE Xplore]***

- **Thabiso Tekisi** and V. M. Srivastava, "Transient Analysis of Differential Amplifier Using Double-Gate MOSFET," ***2023 International Conference on Electrical, Computer and Energy Technologies (ICECET),*** Cape Town, South Africa, 2023, pp. 1-4.
  (DOI: 10.1109/ICECET58911.2023.10389255) ***[IEEE Xplore]***

1.8 Chapter Conclusion

A brief discussion about the background information on DA’s using VT’s and transistors (BJT's, SG, and DG MOSFETs) has been done. Challenges faced by engineers when designing DA have been highlighted as possible solutions. The problem statement, the significance of this research, and the methodology approach have been presented. Lastly, a list of publications that contributed to this work has been listed.

Chapter-2

LITERATURE REVIEW

The invention of amplifiers traces back to the late nineteenth century, marked by Lee De Forest's creation of the triode vacuum tube in 1906, widely acknowledged as the first amplifier. *Smith* [18] asserts that the triode tube revolutionized electronics by enabling amplification and long-distance transmission, playing a pivotal role in the early stages of radio technology and laying the foundation for subsequent electronic innovations, including television. Further significant advancements, notably the development of integrated circuits in the 1960s, as highlighted by *Jones and Lee* [19], led to more efficient and compact amplifier designs, expanding their applications across various industries and domains. Despite their long history and widespread adoption, amplifiers continue to be subjects of active research and development, as evidenced by ongoing efforts reported in ref. [20], aimed at enhancing their effectiveness and optimizing their design.

The exploration of double-gate MOSFETs in amplifier design represents a growing area of research, offering innovative insights and potential solutions to venerable challenges. Recent studies have highlighted the superior performance characteristics of double-gate MOSFETs compared to traditional transistor technologies. For instance, *Sood et al.* [21] reviewed the advancement MOSFET technologies for the next generation communication system and demonstrated that double-gate MOSFETs exhibit higher switching speeds, lower power consumption, and reduced noise levels, making them well-suited for high-speed applications such as communication systems and medical equipment.

However, despite these advantages, the integration of double-gate MOSFETs into amplifier designs remains relatively unexplored, particularly in the context of RLDAs operating in asynchronous or asymmetrical mode. Existing literature predominantly focuses on synchronous or symmetrical mode operation, overlooking the potential benefits of asynchronous operation. *Pillay and Srivastava* [22] has conducted a comprehensive comparative analysis of an active-loaded differential amplifier employing a double gate MOSFET in asynchronous mode. This study has illuminated the potential benefits of utilizing double gate MOSFETs in the design of differential amplifiers tailored for RF applications, low-

power scenarios, and cost-effective designs. Despite the utilization of the double gate MOSFET in asynchronous mode, the results highlight the necessity for further enhancements to augment the system's bandwidth, frequency response (FR), common-mode rejection ratio (CMRR), and output gain.

Pakaree and Srivastava [23] devised a resistive-loaded differential amplifier employing a double gate (DG) MOSFET in synchronous mode, meticulously analysing numerous parameters to evaluate the system's performance. This investigation has prompted inquiries regarding the operational state of the MOSFET necessary for amplification, particularly regarding the saturation region. The study prompts exploration into the methodologies employed to ensure MOSFET saturation and its implications for amplifier functionality.

The current research aims to address this gap by investigating the integration of double-gate MOSFETs into RLDAs operating asynchronously or asymmetrically. Leveraging the unique characteristics of double-gate MOSFETs, such as enhanced channel control and reduced noise levels, the study seeks to enhance amplifier performance and contribute to the advancement of analog integrated circuit design.

2.1 Basics of BJT and Single-Gate MOSFET

This section presents background information about BJT and SG MOSFET and their operation.

2.1.1 Bipolar Junction Transistor (BJT)

The Bipolar Junction Transistor (BJT) is a crucial three-terminal semiconductor device utilized extensively as either a switch or an amplifier within electronic and electrical circuits. Its three terminals - the collector, base, and emitter - are all constructed from semiconductor material, with the base typically being thinner and situated between the emitter and collector. By applying a voltage to the base terminal, the flow of current between the collector and emitter terminals is regulated. BJTs are categorized into two types: NPN and PNP, each possessing p-n junctions known as the Collector-Base Junction (CBJ) and the Emitter-Base Junction (EBJ). Depending on the bias conditions - forward or reverse - of these junctions, the transistor operates in various modes [24].

The most critical mode of operation for BJTs is the active region. In this mode, a voltage (VBE) applied to the base terminal creates a higher potential at the p-type base than at the n-type emitter, resulting in forward biasing of the device. Conversely, reverse biasing occurs between the collector and base terminals when the voltage (V_{CB}) applied causes the n-type collector terminal to have a higher potential than the p-type base terminal [24].

The current in the collector terminal, normally called collector current i_C, is carried by electrons that reach the collector terminal. The magnitude of this current is directly proportional to e^{v_{BE}/V_T}, which makes the collector current to be [24]:

$$i_C = I_S e^{v_{BE}/V_T} \tag{2.1}$$

where I_S is the constant proportionality; from Figure 2.1, it can be observed that the base current consists of two base currents, i_{B1}, and i_{B2}. Because i_{B2} is proportional to e^{v_{BE}/V_T}, the base current will also be proportional to this factor, which can be summarized as in Eq. (2.2) [24]:

$$i_C = \frac{I_S}{\beta} e^{v_{BE}/V_T} \tag{2.2}$$

where β is the transistor parameter typically 50 – 200 for normal transistors. The emitter current is the sum of both base and collector current: $i_E = i_C + i_B$, which can be summarized as [22]:

$$i_E = \frac{\beta+1}{\beta} I_S e^{v_{BE}/V_T} \tag{2.3}$$

The above currents determine the active region for a BJT, which simply means that to ensure that the device operates in the active region, the above current conditions must be met. The active mode can be maintained until V_{CB} reaches -0.4 V [24].

In the saturation region of a transistor, the collector current decreases. To verify saturation, ensure the Collector-Base Junction (CBJ) is forward biased by a voltage exceeding 0.4 V and the collector current to base current ratio is less than a certain threshold [24]. In a PNP transistor, operations mirror those of an NPN transistor but in reverse, with the emitter and collector composed of p-type material and the base of n-type material.

2.1.2 Single-Gate MOSFET

Having discussed the basic operation of a BJT and how one can control it to be in active or saturation mode and use it as a switch or amplifier, in this section, MOSFET's basic operation will be discussed. MOSFET stands for metal oxide semiconductor field effect transistor and is a four-terminal device with Gate (G), Drain (D), Source (S), and Body (B) terminals. Normally it is utilized in processing both digital and analog signals. They are classified into two types: (i) n-channel, which is made up of n-type semiconductor material, and (ii) p-channel, which is made up of *p*-type semiconductor material. The basic structure of a MOSFET is depicted in Fig. 2.1 [24, 26].

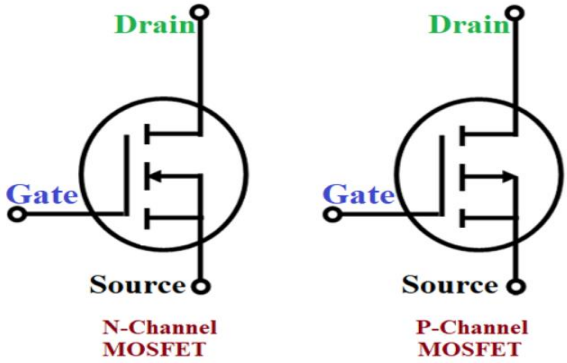


Figure 2.1 *n* and *p* channel MOSFETs [24].

In a MOSFET device, current, controlled by a gate terminal, flows from drain to source through a channel region with crucial dimensions W and L. Initially, with no voltage applied to the gate, back-to-back diodes between drain and source create high resistance, preventing current flow. Gradually increasing voltage V_{GS} alters this resistance, affecting device behaviour [24].

In an n-channel MOSFET, a small positive voltage applied to the gate induces an n-type channel between the drain and source terminals, allowing current flow via mobile electrons. The minimum voltage (V_t) required to form this conducting channel typically falls within a range of 0.3 V to 1.0 V. The gate terminal and channel region together form a parallel-plate capacitor, with the oxide layer as the dielectric. The voltage across this capacitor must exceed V_t for channel formation [24, 27].

Consequently, the current that flows from the drain to the source terminal is normally called drain current, denoted by i_D and can be represented using [24]:

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L} \right) (v_{GS} - V_t)^2 \tag{2.4}$$

where $(\mu_n C_{ox})$ is called process transconductance, which is normally represented by k_n' and v_{DS} is the drain to source voltage. Further increasing v_{DS} causes the formed channel region to be pinched off on the drain terminal, represented by a light grey area as depicted in [24].

Increasing the drain to source voltage above overdrive voltage has no effect on the shape of the channel and mobile electrons on this channel. This results in a situation called a saturation region, where the value of the drain current no longer changes even when one increases the value v_{DS} . This current is represented by the equation (2.5) [24],

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L} \right) (v_{GS} - V_t)^2 \tag{2.5}$$

In other words, from when $v_{DS} = 0V$ up to when $v_{DS} = v_{OV}$ the MOSFET is said to be operating in the triode region and above its saturation region. This can be observed in Figure 2.2. In the triode region, the device can be used as a switch, and in the saturation region, the device can be used as an amplifier [24,27]. In the upcoming section, the basic operation of a double-gate MOSFET will be discussed, and its advantages over BJT and SG MOSFET.

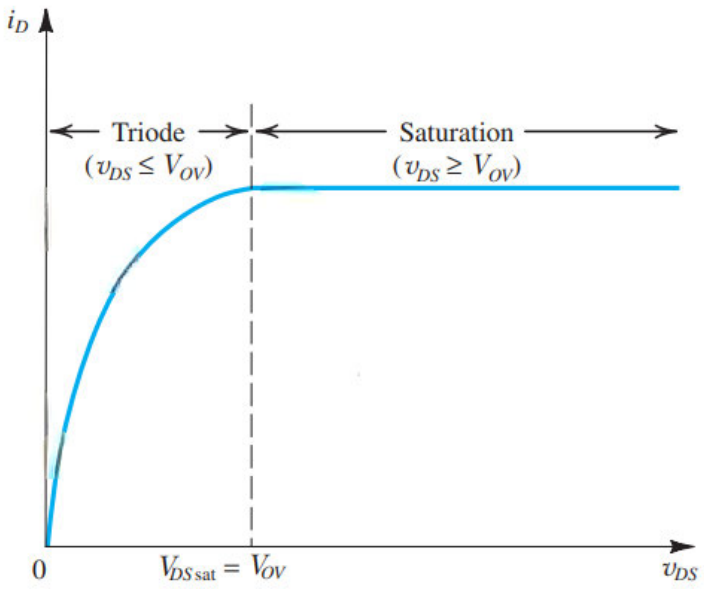
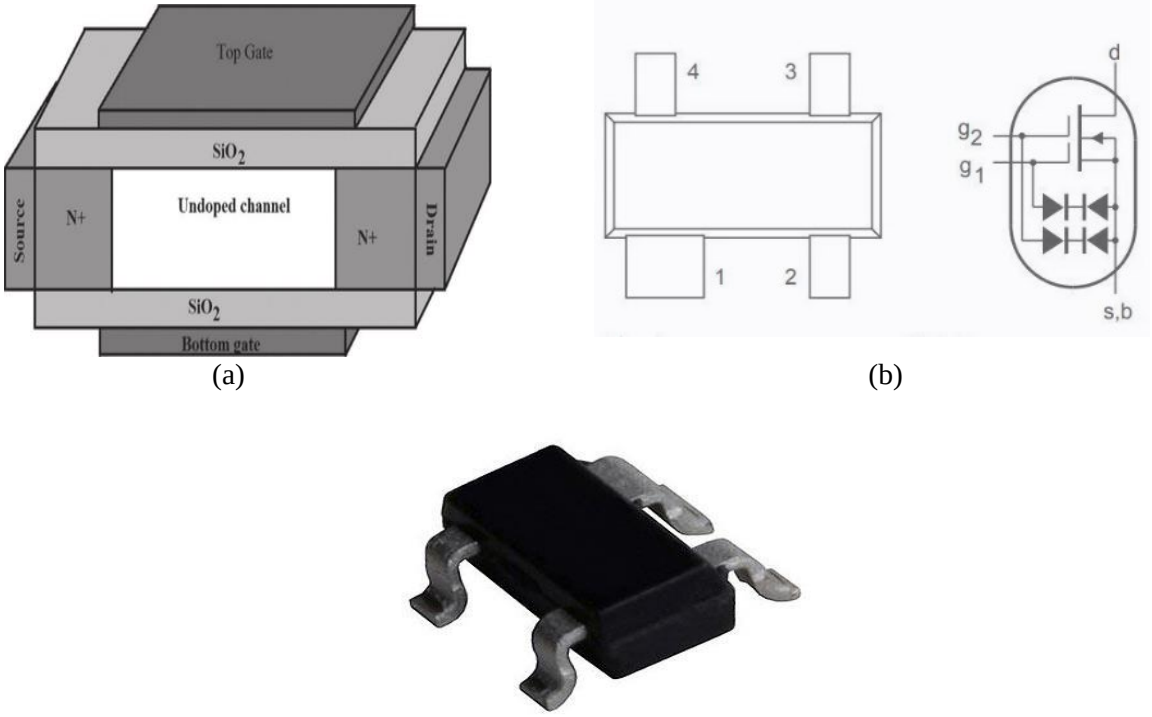


Figure 2.2 i_D vs V_{DS} that shows triode and saturation region.

2.2 Double-Gate MOSFET Basic Operation

The DG MOSFET is a distinctive modification of the standard MOSFET design that employs two gates to control the channel rather than the usual single gate. It has much potential for nanometre-scale transistors in extremely congested IC designs. The DG MOSFET's essence consists of putting two gate terminals at the top and bottom of the channel in an extremely thin SOI body, enabling effective gate control over the channel on both gates [28-30]. Both gates in a double gate device are paired, reducing the short channel effect and leakage. Compared to the planer CMOS circuit, the two gates circuit with a double-gate transistor can be operated with a lower input voltage, resulting in lower power consumption [28].



(a) (b)

(c)

Figure 2.3 (a) Double-gate MOSFET Structure, (b) BF998 double-gate MOSFET pinout, and (c) BF998 physical component [30].

Figure 2.3 (a) depicts the typical device structure of the DG MOSFET. It consists of a top and bottom gate, source, and drain terminals, (b) depicts the internal pinout of BF998 DG MOSFET, and (c) depicts the physical structure of the DG MOSFET. The two gates of the double-gate MOSFET can be operated in two different operation modes to enhance the performance of the device; symmetric and ASM.

2.2.1 Symmetric Mode

When operating in SM, the MOSFET is balanced, and both gates are biased simultaneously, as depicted in Fig. 2.4. As a result, the device is considered symmetrical, and the electron density in the channel is also uniformly distributed. The balanced operation of the symmetric mode makes it helpful in applications where the MOSFET must operate with minimal power consumption and enables effective control of the current flow [31, 32].

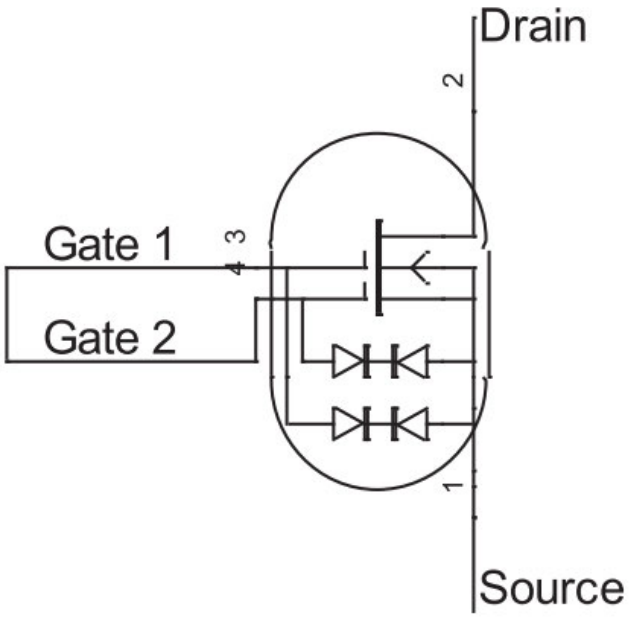


Figure 2.4 Symmetric DG MOSFET [35].

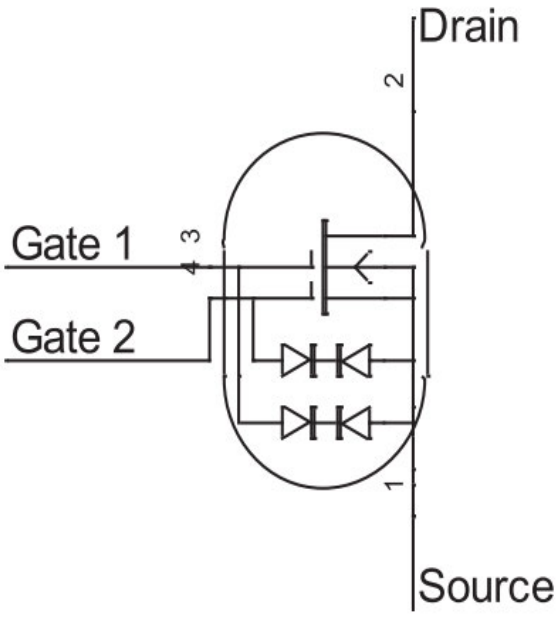


Figure 2.5 Asymmetric DG MOSFET [35].

2.2.2 Asymmetric Mode

Each gate is biased independently in ASM as depicted in Fig 2.5, which results in an unequal distribution of the channel's electron density. As a result, the relationship between the current and voltage becomes non-linear, which enhances efficiency for high-frequency applications. In cases where t

he device has to function at high speeds, the ASM is advantageous because it enables better control of the movement of electrons in the channel region [33, 34].

2.2.3 Advantages and Disadvantages of a DG MOSFET

The double gate MOSFET has the most important advantages compared to traditional MOSFETs, making it more suitable for designing electronic circuits. Table 2.1 summarizes these features.

Table 2.1 Advantages and Disadvantages of a DG MOSFET

Advantages	Disadvantages
• Higher drive currents at lower supply voltage and threshold voltage. • It lowered channel and gate leakage current when in the off state, saving power. • Isolated power gate control helps in saving power and chip area. • Better sub-threshold slop is provided (approximately 60 mV/decade). • No discrete dopant fluctuations exist. • Energy is a quadratic function of the supply voltage.	• Alignment of both gates w.r.t. one another. • Source and drain self-alignment to both gates • The same gates are required. • Using a low resistance path to connect two gates.

2.3 Types of Differential Amplifiers

Differential amplifiers (DAs) play a vital role in electrical circuits by facilitating the processing and amplification of differential input signals, finding applications in instrumentation, communication systems (CSs), audio amplification, and analog signal processing. Over the years, DAs have been implemented using various active devices, including vacuum tubes (VTs), bipolar junction transistors (BJTs), and metal-oxide-semiconductor field-effect transistors (MOSFETs). While early electronic devices favoured vacuum tube DAs for their high voltage gain and reliability, the advancement of solid-state technology has led to the widespread adoption of BJT and MOSFET-based DAs due to their portability, reliability, low power requirements, and compatibility with integrated circuit production techniques [36, 37].

This section provides a brief overview of the theoretical background, operational principles, and performance characteristics of vacuum tube, BJT, and MOSFET-based DAs.

2.3.1 Vacuum Tube (VT) Based Differential Amplifier

Differential vacuum tube amplifiers played a significant role in early electronic systems due to their high voltage gain and varied performance characteristics. While solid-state technologies have largely replaced them, vacuum tube DAs remain relevant in specialized applications and are prized by enthusiasts for their unique sound qualities. Operating a vacuum tube DA relies on using triodes, particularly VTs, in a differential configuration where input signals are applied to the grids and outputs are taken from the anodes. However, vacuum tube DAs have limitations including lower differential voltage gain compared to other technologies and degraded CMRR due to intrinsic tube property mismatches. Additionally, their intrinsic capacitance and inductance limit frequency response, especially at higher frequencies [38, 39]. This section aims to explore the operational principles, advantages, and limitations of vacuum tube-based DAs.

A. The basic operation of Vacuum Tubes based Differential Amplifier

A vacuum tube-based DA typically comprises two triodes connected in a differential configuration. The input signals are applied to the triode grids, and the output signals are then measured from the anodes. The cathodes are connected to a single voltage reference. The flow of electrons and current control within the VT's amplify the input signals [39]. Figure 2.11 depicts a typical resistive-loaded vacuum tube-based DA and the basic fundamental configuration of DA [40].

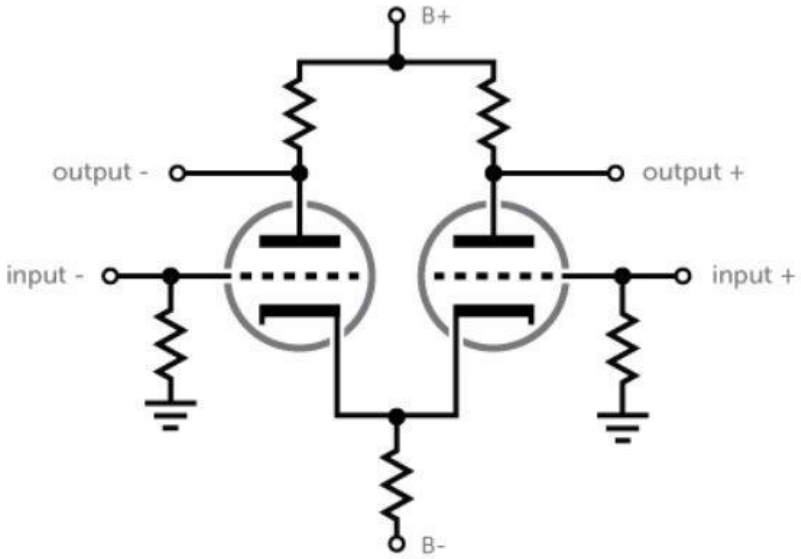


Figure 2.6 Typical Vacuum-Based DA [41].

B. Advantages of Vacuum Tube-Based Differential Amplifier

- VT's based DAs can amplify weak signals due to their significant voltage gain capability.
- They often have low input impedance, which is useful when communicating with high-impedance signal sources.
- They additionally provide fairly constant performance across a broad temperature range, rendering them useful for applications with significant temperature fluctuations.

C. Disadvantages of Vacuum Tube-Based Differential Amplifier

- Compared to modern solid-state components, VTs are physically huge and heavy, making them unsuitable for small and lightweight designs.
- They are typically more costly than their solid-state competitors, which can affect the entire cost of a vacuum-based DA.
- They use more power than solid-state devices, therefore, have a poorer overall efficiency.
- VTs have a restricted functional duration, and their performance might decrease with time, necessitating replacement regularly.

D. BJT Based Differential Amplifier

A typical kind of DA that uses BJTs as active components is extensively used in various applications, such as CSs, instrumentation, audio amplification, and analog signal processing. Two transistor devices, usually NPN type, make up the BJT-based DA. The base terminal of

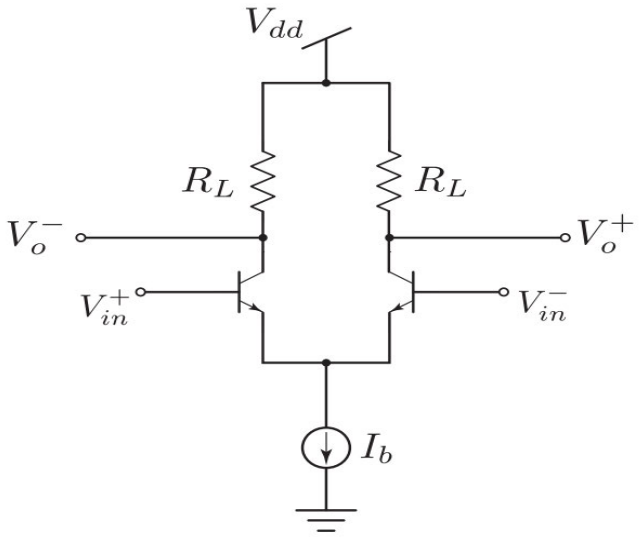


Figure 2.7 Typical BJT-Based Differential Amplifier [45].

one transistor receives the inverting input, whereas the base terminal of the other transistor receives the non-inverting input. Typically, a current source or resistor network is used to bias and connect the emitters of both transistors, which forms a common-emitter circuit [43,44]

Figure 2.7 depicts a typical BJT-based DA consisting of two matched transistors. I_b Denote a current source for the entire circuit and a resistor with a negative voltage source is normally used to generate the constant current. R_L denotes load or collector resistors, which act as load, and control the gain of the amplifier. The DA suppresses the common-mode signals (signals present in phase on both inputs), which enhances the VD between the two input signals. Through the differential-mode gain, which is determined by the transconductance g_m of the transistors, load resistors, and other circuit elements, the amplification is accomplished [45].

2.4 Small Signal Analysis Methods

Small-signal techniques and theories examine the DA's behaviour in small-signal conditions. The small-signal analysis enables the linear response of the circuit to small input signals and the linearization of the non-linear transistor characteristics around a DC bias region. A hybrid-pi model, which depicts the small-signal features of the transistor device, is part of

the BJT's small-signal model. A small-signal current source ($g_m \times V_{be}$), a small-signal output resistance (r_o), and a small-signal input resistance (r_{in}) make up the hybrid-pi model. The DA circuit can be evaluated using KVL, nodal analysis, and voltage division using the small-signal model. Voltage gain, input impedance, output impedance, and other key parameters can be determined using these procedures [45].

2.4.1 MOSFET Based Differential Amplifier

The MOSFET is the most extensively used device in digital and analog circuits and is the foundation of modern electronics. The development of DAs is one of the most common applications of MOSFETs in analog circuits. These types of devices are utilized as input stages in operational amplifiers, video amplifiers, high-speed comparators, and various other analog-based circuits. MOSFET DA's are utilized in integrated systems such as operational amplifiers because they have a high input impedance. Figure 2.11 depicts the typical MOSFET-based DA. It comprises two matched MOS transistors denoted by Q_1 ,and Q_2 . The two load resistors are connected to a positive voltage supply and the drain of transistors. They can control the voltage gain of the amplifier. The two devices' source terminals are connected with the CCS denoted with I_{BIAS} ,which provides the current to the entire circuit [46,87].

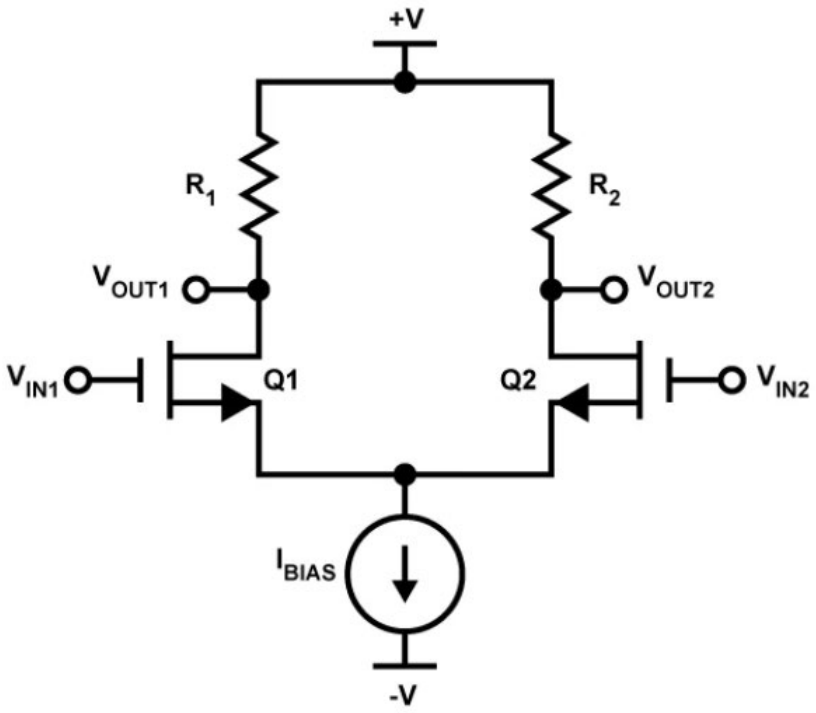


Figure 2.8 Typical MOSFET DA [47].

Assuming the input signals are denoted as v_{in1} and v_{in2}, they can be divided into two linear configurations, the DM and the common mode.

A. Differential Gain

A differential voltage gain is an essential parameter that indicates the capability of the amplifier to amplify the VD between its two input signals. It quantifies the amplification factor for the DM signal and provides insight into the amplifier's performance in amplifying the desired signal while rejecting common-mode noise. The differential voltage gain A_d is the ratio of the change in output voltage V_{out} to the change in differential input voltage $V_{in(d)}$. It is commonly measured in volts per volt (V/V) or decibels (dB). Various design parameters must be considered to attain a large differential voltage gain. For example, the transconductance values g_m of the DG-MOSFETs employed in the amplifier should be appropriate for efficient signal amplification. Gain is enhanced when the gm value increases. The load resistors (RL) used in the amplifier circuit affect the differential voltage gain. Proper R_D selection aids in optimizing the voltage signal and increasing the gain. The load resistors need to be specifically chosen to fit the DG-MOSFETs properties. The differential output signal is directly proportional to the difference between the two input signals in a DA. That is [24, 47]:

$$V_{out1} - V_{out2} \propto (V_4 - V_3) \tag{2.6}$$

where V_4 is the input voltage signal to gate-1 of M1 and V_3 is the input voltage signal to gate-1 of M_2. This $V_{out1} - V_{out2}$ is the differential output between the two DG MOSFETs. The DG can be measured with either a differential or a single-ended output. The difference between two signals is amplified and then measured at the output terminals, drain terminals. The DG is the proportion of the output signal to the input signal. This concept has been represented by [28]:

$$A_d = \frac{V_{out1} - V_{out2}}{V_4 - V_3} \tag{2.7}$$

This concept has been implemented to calculate the voltage gain in forthcoming sections, where the proposed circuit is operated with single input - single output and single input - differential output to determine the performance.

B. Common-Mode Input Voltage

The voltage supplied equally to both of the DA's input terminals is called the common mode input voltage. It refers to the typical or average voltage level the amplifier works at. A DA is meant to reject the common mode voltage and amplify the difference between the two input terminals. A DA should amplify only the differential voltage while rejecting the common mode voltage. In real life, however, the amplifier can become sensitive to the common mode voltage, resulting in common mode gain. The CMRR measures the capability of an amplifier to reject the common mode voltage. Figure 2.9 depicts common-mode input voltage, where both gates of the two matched MOSFET as supplied with the same signal. The common mode, which is the average value between the two signals, is also defined as [24, 28, 48]:

$$v_{(cm)} = \frac{v_{in1} + v_{in2}}{2} \tag{2.8}$$

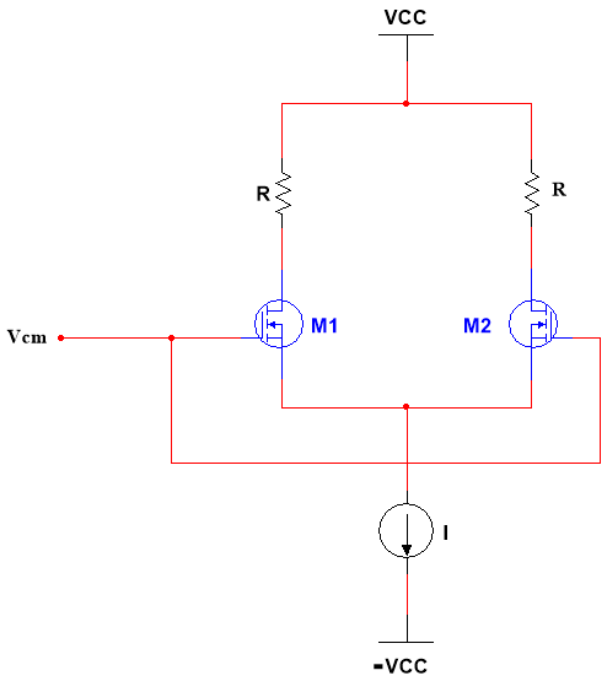


Figure 2.9 Typical Common-Mode Input Voltage.

The actual input signals v_{in1} v_{in2} can be described as linear combinations of their differential and common modes using these definitions [46,47,48,49]:

$$v_{in1} = v_{(cm)} + \frac{v_{(dm)}}{2} = \frac{v_{in1} + v_{in2}}{2} + \frac{v_{in1} - v_{in2}}{2} \equiv v_{in1} \tag{2.9}$$

Whenever the common mode input voltage varies, the biasing and operation of the DA are impacted, potentially resulting in distortions or undesirable effects in the amplified output signal. As a result, the common mode input voltage range must be considered. This is important because the input common-mode range is the range where the DA operates appropriately, and the highest value is determined by:

$$V_{cm(\max)} = V_t + V_{CC} - \frac{I}{2}R \tag{2.10}$$

and the lowest value can be determined by:

$$V_{cm(\min)} = -V_{CC} + V_t + V_{CS} + V_{OV} \tag{2.11}$$

and V_{CS} is the voltage across the current source.

C. Differential Input Voltage Mode

The differential input voltage mode is critical since it reflects the desired signal to be amplified while retaining HG and linearity. The DG of an amplifier measures the degree to which it amplifies the differential input voltage. A DA can provide great immunity to common-mode noise or interference that affects both input terminals equally by increasing the difference between the input voltages. This DM operation effectively rejects undesirable common-mode signals, improving signal quality and noise efficiency. The DM can be defined by (Eq 2.12) [24,47,49]:

$$v_{(dm)} = v_{in1} - v_{in2} \tag{2.12}$$

$$v_{in2} = v_{i(cm)} - \frac{v_{i(dm)}}{2} = \frac{v_{in1} + v_{in2}}{2} - \frac{v_{in1} - v_{in2}}{2} \equiv v_{in2} \tag{2.13}$$

The range of the differential input voltage for a DA can be determined by using (Eq 2.12):

$$-\sqrt{2}V_{OV} \leq v_{id} \leq \sqrt{2}V_{OV} \tag{2.14}$$

2.5 Chapter Conclusion

Finally, VT's, BJT, and MOSFET-based DA's all have unique features and capabilities. Vacuum tube DAs provide high voltage gain and robust performance, making them ideal for high-power and high-voltage applications. They are, nonetheless, limited by their massive size, substantial energy consumption, and susceptibility to temperature changes. BJT-based DAs, on the other hand, offer a solid compromise between efficiency and practicality. They have an acceptable voltage gain and acceptable linearity and are readily accessible. MOSFET DA's provide high input impedance and low power use and are compatible with IC technology because they are based on field-effect transistors. They are ideal for applications demanding low power and high input impedance.

Chapter-3

DESIGN OF A DOUBLE-GATE MOSFET-BASED DIFFERENTIAL AMPLIFIER

The DAs are essential components in many analog and mixed-signal circuits, providing amplification and signal processing. The introduction of DG MOSFETs has opened up new opportunities for circuit designers and engineers, enabling higher efficiency and distinctive characteristics above typical SG MOSFETs. Dual gates on DG MOSFETs permit engineers and circuit designers to control device parameters such as threshold voltage, transconductance, and channel length modulation. Because of these benefits, they are an interesting alternative for developing high-performance DAs. In this chapter, we will look at the design considerations and optimization methods unique to developing a DA that utilizes double-gate MOSFET. Software tools and other electronic components will be looked at. Figure 3.1 depict the design process utilised to design the proposed solution.

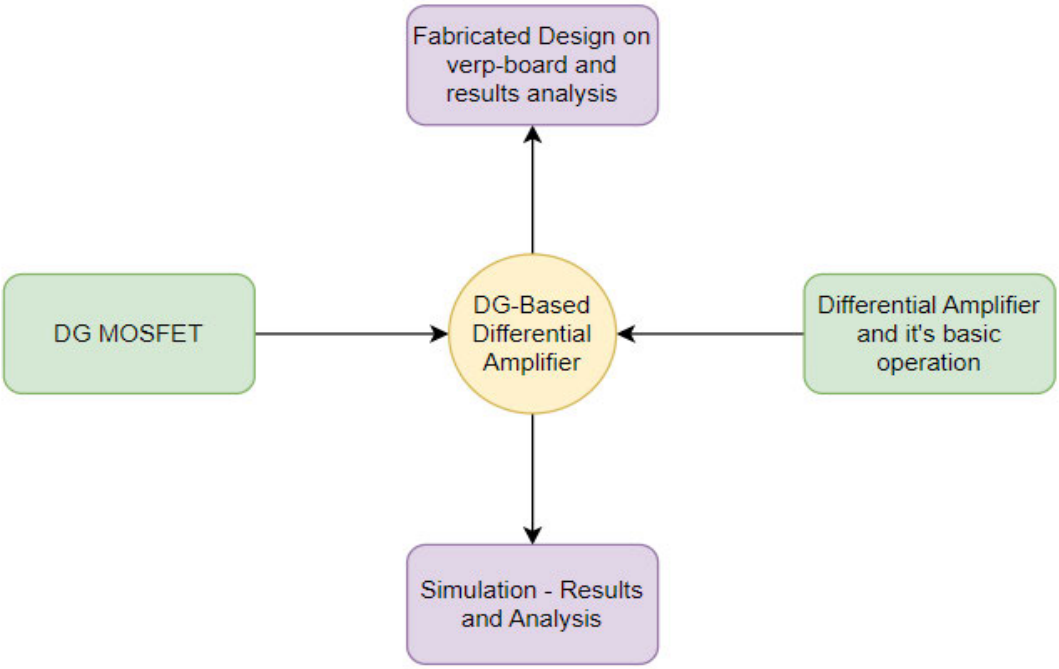


Figure 3.1 Design Process for a Proposed DG-Based DA.

3.1 Proposed Solution of a Differential Amplifier Using Double-Gate MOSFET

The DAs are primarily used to reduce noise, comprising typical differential and common-mode noise, which could be conveniently reduced with an operational amplifier. Two main factors cause common-mode noise; first, electromagnetic induction and other factors produce noise in the electrical wires and cables, resulting in a potential difference (noise) between the signal source and circuit ground. Secondly, a ground potential rise occurs when current flows into the ground of one circuit from another. Noise causes the ground potential to vary in both cases. Common-mode noise is challenging to eliminate with standard filters. DAs are employed to overcome this common mode noise [50, 51].

Utilizing the special features of a double-gate MOSFET allows for the design of DAs with HG, better bandwidth, high CMRR, and relatively low power consumption. Compared to conventional MOSFETs, the double-gate MOSFET performs better because it has two gates, improving control over the current flow in the channel region from drain to source terminals. In other words, the DG MOSFET can be operated in symmetric mode and asymmetric mode. The symmetric mode is when both gates are biased with the same signal, and the asymmetric is when each gate is biased independently [52,53].

In designing a DA, one needs to identify the circuit topology and biasing circuit for the gates. Important parameters to optimize the performance of the amplifier, including gain, CMRR, FR, noise, etc., need to be properly analyzed. Previous studies on the design of DAs using double-gate MOSFET have been done, and the work is incredible. Other recent work was done by [29] and [52], including the design of a resistive using SM and active-loaded using DA's with DG MOSFET, respectively. However, a resistive-loaded double-gate based DA using ASM has not been studied. A comprehensive study that explores the impact of biasing the two gates in a resistive-loaded DA is missing. This means that a detailed analysis of parameters that measures the performance of the amplifier is also missing. With this, this study aims to design a resistive-loaded DA using DG MOSFET in ASM because it has proved that it can reduce noise and SCEs and improve output gain. The forthcoming section will break down the design of this amplifier.

Figure 3.2 depicts a circuit design of the proposed DG-based DA. The amplifier comprises two DG-MOSFETs (M_1 and M_2) in a common-source configuration and then connected to a negative voltage source through a resistor to create a CCS for the circuit. While

the drain terminals are connected to a positive voltage source through resistors, normally called drain resistors (R_1 and R_2). Drain currents (I_{R1} and I_{R2}) are monitored via drain resistors, and the output voltage V_{out} is measured at the drain terminals, single-ended or differentially (V_{out1}-V_{out2}). The BF998 DG MOSFET is operated in ASM because this allows for the threshold voltage and transconductance control. It also reduces SCEs and gate leakage current, eventually enhancing the gain and common mode rejection ratio. Moreover, the BF998 is chosen because it can be supplied with a voltage source of up to ± *12 V*, which improves the gain, whereas MOSFETs such as BF904WR can only be supplied with a voltage source of up to *7 V*.

The DG-MOSFETs must be properly biased to achieve the desired operation and performance. To optimize the device properties and obtain the desired gain, linearity, and low energy consumption, the bias voltages for gate-1 and gate-2 gates should be carefully adjusted. When DG MOSFET is operated in ASM, it is advised that gate-1 be biased with a small signal and gate-2 be biased with 4 to 5 V. This ensures that the devices remain in saturation region where the drain current does not change. It further improves the electron mobility in the channel region, improving the system's performance [24, 28, 29].

As depicted in Figure 3.2, gate-1 is biased with a small AC voltage signal denoted by V_4 on M_1 and V_3 on M_2. Furthermore, gate-2 is used to bias the MOSFET into saturation region. Nevertheless, since gate-2 is in charge of the transconductance, threshold voltage, and current characteristics, operating each MOSFET asymmetrically allows much greater control [54]. A voltage divider is used to bias gate-2 using the *12 V* supply. Gate-2 is biased with 5 V from the voltage divider, and the voltage divider is depicted in Fig 3.3. The fundamental formula to calculate the required voltage is shown in Eq. 3.1 [55]. Voltage dividers are helpful to provide various voltage levels from a single supply voltage. This common supply could be across a dual supply, such as *5 V* or *12 V*, or a single supply that is positive or negative, such as *+5 V*, *+12 V*, *-5 V*, or *-12 V*, etc., with regard to a common point or ground, typically *0 V*. Figure 3.4 depicts the output characteristics of the BF998. Here BF998 MOSFET is in saturation, but start by getting into the triode region, and when the drain current is constant, that is where one knows it is the saturation region.

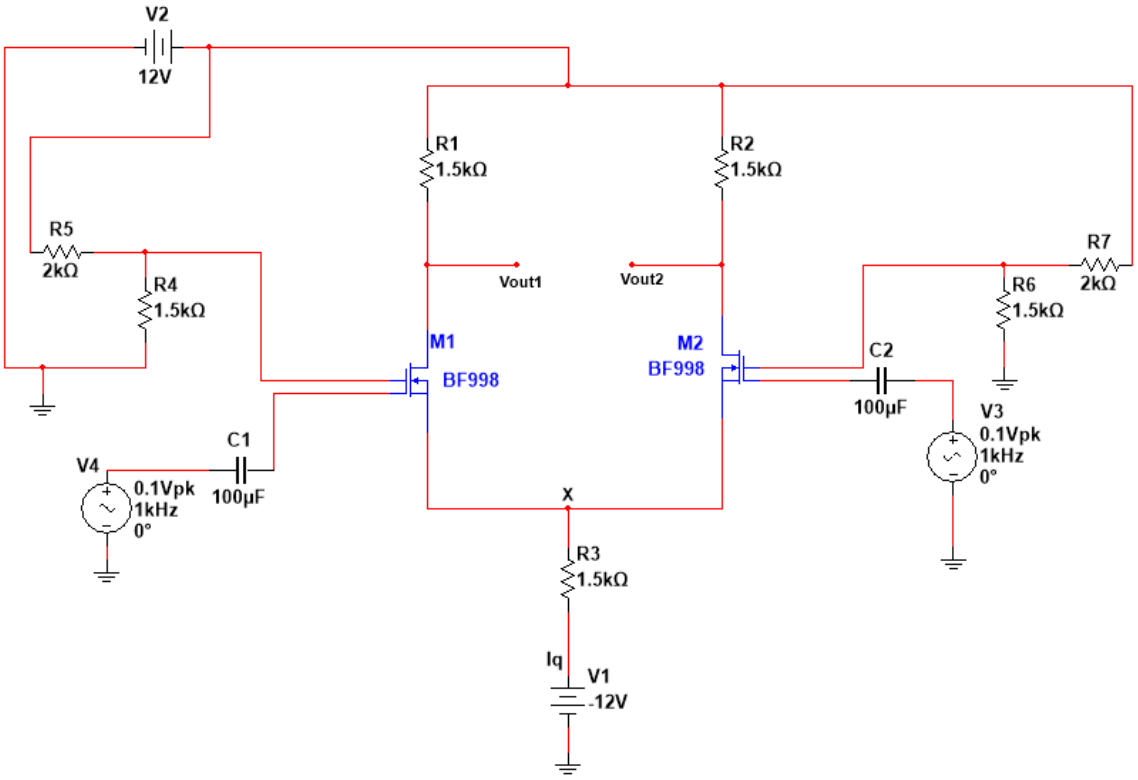


Figure 3.2 Proposed DG-based DA.

Depending on the drain current, gate-1 voltage may be varied between *-0.5 V* to *0.5 V*. To bias gate-2 terminal

$$V_{G2} = V_2\left(\frac{R_4}{R_4 + R_5}\right) \tag{3.1}$$

When a signal is applied, a change in V_{G2} results in an increased or reduced transconductance. This has been demonstrated by [22], where the device's linear section has a more significant gradient when V_{G2} is increased to *2 V*. Therefore, lowering V_{G2} results in a lower voltage at saturation and lower demand for drain current and this effect can be observed from Eq. (2.5).

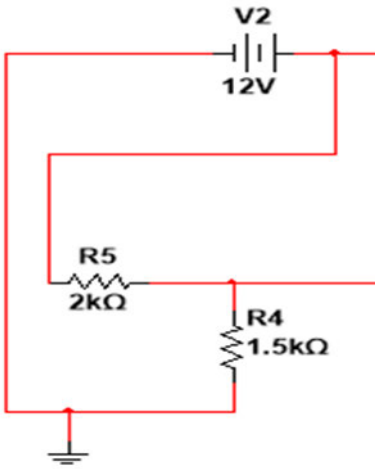


Figure 3.3 Typical voltage divider.

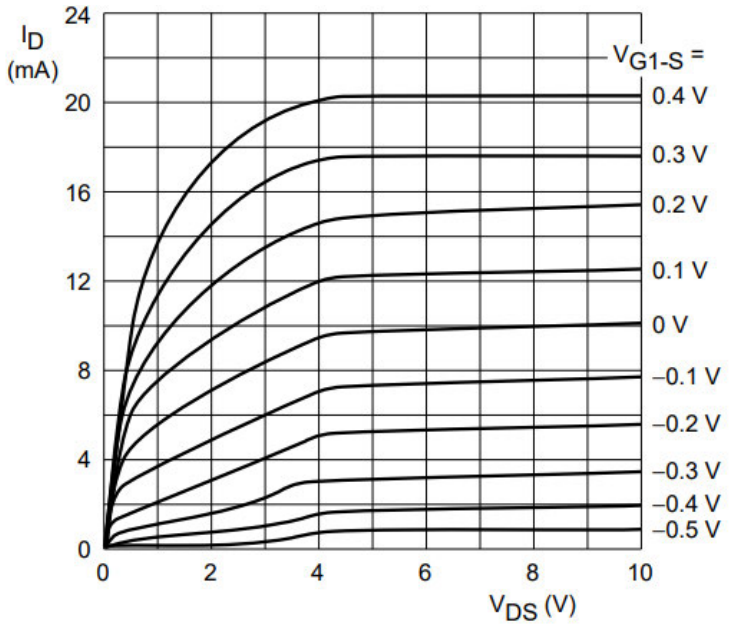


Figure 3.4 Drain current vs. drain to source voltage.

3.1.1 DC Analysis

The DC analysis of a DG-based DA is an essential step in establishing the system's operating point and determining the DC voltages and currents. It also details the amplifier's biasing conditions, stability, and overall DC efficiency. To perform this analysis, the gates on both transistors are grounded, drain terminals are connected to a positive voltage supply through drain resistors, and source terminals are commonly connected to a negative voltage supply through a resistor, as depicted in Figure 3.5.

Multiple presumptions are applied to simplify the computations when performing the DC analysis. The input signals are considered constant DC voltages, with no AC components

or transient. Second, phenomena such as channel-length modulation, which can affect drain current, are disregarded. Finally, to ensure optimal amplifier performance, the DG-MOSFETs are assumed to be in the saturation region [40]. Since both sources of the DA are symmetrical in all aspects, the operating point for one section is determined. The drain current can be found using Eq. (3.2).

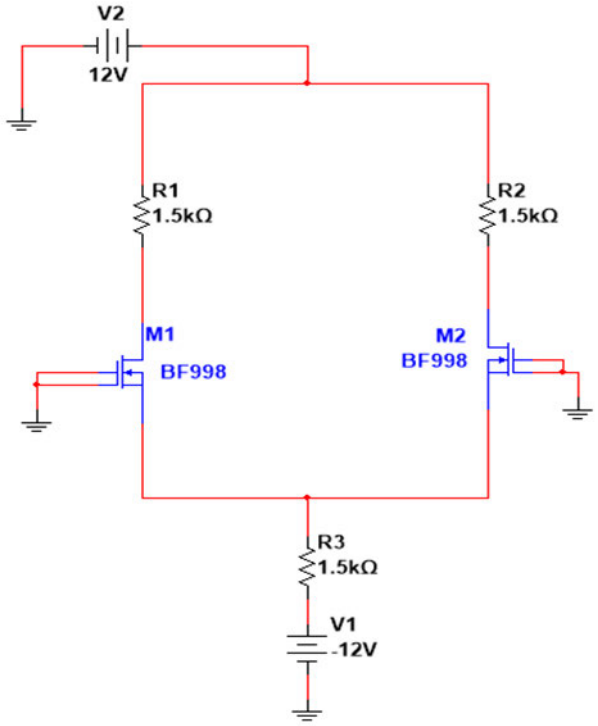


Figure 3.5 DC analysis with all gates grounded.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{3.2}$$

And to ensure saturation on transistors, the drain voltage should always be greater than the gate voltage subtracting the minimum voltage as [40]:

$$V_{DS} \geq V_{GS} - V_{TH} \tag{3.3}$$

When transistors are in the saturation region, the generated constant current will divide equally on both drains of transistors, as shown in eq. (3.4) [40]:

$$I_{R1} = I_{R2} = \frac{1}{2}\left(\frac{V_1}{R_3}\right) \tag{3.4}$$

And the current source is [52]:

$$I_{R3} = \frac{V_1}{R_3} = \frac{12}{1.5k} = 8mA \tag{3.5}$$

The value of R_3 determines the current source in both transistors for a given value of V_1. The source current in M_1 and M_2 is independent of the drain resistance R_1 R_2. The voltage at the source terminal M_1 is approximately equal to V_{GS}. The output voltage at the drain terminal can be determined as follows:

$$\begin{aligned} V_{out1} &= V_{out2} = V_2 - I_{R1}R_1 = V_2 - I_{R2}R_2 \\ &= 12 - (4x10^{-3})(1.5x10^3) = 6V \end{aligned} \tag{3.6}$$

Then the voltage drain to the source can also be determined as follows:

$$\begin{aligned} V_{DS} &= V_D - V_S \\ &= V_{DD} - I_D R_D * V_{GS} = V_1 - I_{R1}R_1 * V_{GS} \\ &= V_1 * V_{GS} - I_D R_D = 12 * 0.65 - (1\times10^{-3})(1.5\times10^3) = 6.3V \end{aligned} \tag{3.7}$$

3.1.2 Software and Hardware Tools

Multisim, Math Type, and Vero-board were chosen to construct a DG MOSFET-based DA because of their distinct capabilities in circuit modelling, mathematical equation representation, and fabrication.

Multisim - is a powerful circuit simulation software that allows researchers and engineers to virtually test and analyse the electrical/electronic circuit's performance before fabricating it.

Math Type - is a tool for editing mathematical equations that makes it easier to represent complex formulas and mathematical models used in the design, allowing for precise documentation and analysis.

Vero-Board - is a type of prototyping board that is flexible for constructing and testing physical circuit components, allowing for minor modifications and enhancements.
These tools offer a comprehensive technique for designing, modelling, and prototyping a DG MOSFET-based DA, enabling implementation and outstanding efficiency.

3.1.3 Components Used

Resistors, capacitors, and MOSFETs are all commonly employed in the design of differential amplifiers, and they all play a crucial role in the performance of the differential amplifier.

Resistors play an important role in setting a differential amplifier's gain, input, and output impedance. They are also used to design voltage dividers, bias the MOSFETs, and provide the required current for a better operation of a differential amplifier. In this work, they are used to design a constant current source and the setting of a gain.

Capacitors are often employed for AC coupling, DC component blocking, and noise filtering. They are normally inserted at the input or output terminals of the amplifier to achieve a desired frequency response, and in this work, they are used at the input for low signal filtering.

Double-Gate MOSFETs – They provide additional design flexibility to engineers and researchers and can enhance the performance of a differential amplifier. These devices also provide better linearity, low noise, reduced short-channel effects, and better gain than single-gate MOSFETs.

3.2 Chapter Conclusion

In closing, the functional specification of the project has been presented. A detailed analysis of the design of DG-based DA using BF998 has been presented. This includes the importance of using BF998 in ASM, which provides engineers and researchers control over the channel region and threshold voltage of the device, improving the circuit's performance. Moreover, dc analysis which assists with determining the operation point of the MOSFETs, has been done. Tools used to design and analyse the proposed solution have been discussed as their importance. The forthcoming section will analyse the proposed solution's performance using different modes that a DA may be used for, which include single input – single output and single input – differential output.

Chapter-4

SINGLE-ENDED INPUT AND SINGLE-ENDED OUTPUT ANALYSIS OF A DG-BASED DIFFERENTIAL AMPLIFIER

The parameters (two different circuit configurations: single input – single output and single input – single output), such as differential gain, common mode input voltage gain, CMRR, frequency response, etc., have been analysed here. The common mode input voltage, CMRR, and frequency for both these circuits have been analysed in sections *4.3 to 4.6*, respectively. This is done to prevent repeating almost similar analyses because they are almost the same.

4.1 Single Input – Single Output Mode

Figure 4.1 depict a proposed DG MOSFET single-input with single-output DA circuit configuration. A single device, M_1 is used, and the second transistor, M_2 input terminals are grounded. The single output is taken on the drain terminal M_1 denoted by V_{out1}. Whenever a DG-based DA is operated with a single input and output, the circuit's behaviour differs from that of a conventional differential mode operation. The supplied signal modulates the active DG-MOSFET's channel conductivity, allowing current to flow from the source to the drain.

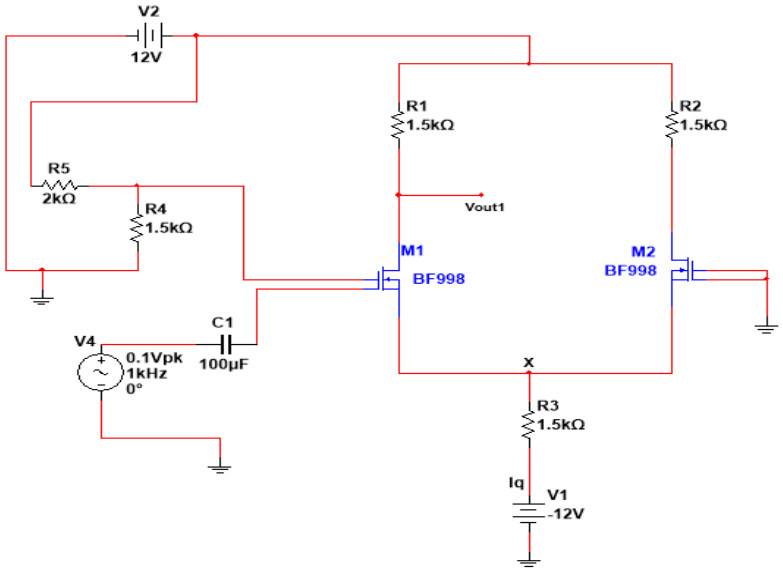


Figure 4.1 Single Input – Single Output of a proposed DA.

The applied voltage, transistor properties, and the load impedance connected to the output all control the current flow.

4.1.1 Circuit Operation

The circuit incorporates a capacitor in series with the AC signal source, connected to gate-1, effectively blocking any DC component. Gate-2 is biased at a fixed voltage of 5 V, achieved through a voltage divider network. When the input signal V_4 becomes positive, the current flowing through M_1 increases. This amplified current leads to a positive-cycle signal at the point *X*. Simultaneously, the source terminal M_2 perceives an inverted signal. As the base M_2 is grounded, a positive-cycle signal at the source terminal causes the current to decrease, causing a drop in the voltage across R_2. Consequently, the voltage at the drain terminal M_2 increases, resulting in signal amplification at the output.

Conversely, when the input signal becomes negative, the current flowing through M_2 decreases. This reduction in current at point *X* generates a negative-cycle signal at the source terminal M_2. As the source of M_2 becomes negative, the current flowing through M_2 increases. This higher current causes a greater voltage drop across R_2. Consequently, the voltage at the drain M_2 decreases, resulting in the output terminal V_{out} experiencing a negative-cycle signal.

4.1.2 Differential Gain

Figure 4.2 depicts the graphical result when the proposed circuit is operated in single input – single output mode. The input signal through gate-1 has an amplitude of $0.2\ V_{pk\text{-}pk}$ at a frequency of *1* kHz, and *5V* for gate-2. The same result is achieved up to a cut-off frequency of *65 MHz*. The obtained results signify the importance of the proposed circuit, and it shows that it performs better than already existing designs. In other words, this means that using DG-MOSFET in asymmetrical mode improves the performance of the amplifier by enhancing the output voltage gain, reducing SCE, and improving CMRR.

Although this DA amplifies AC or DC signals, the capabilities of a DA are not fully exploited. Table 4.1 summarizes the results and behavior of this circuit configuration when the input signal's amplitude and frequency are varied.

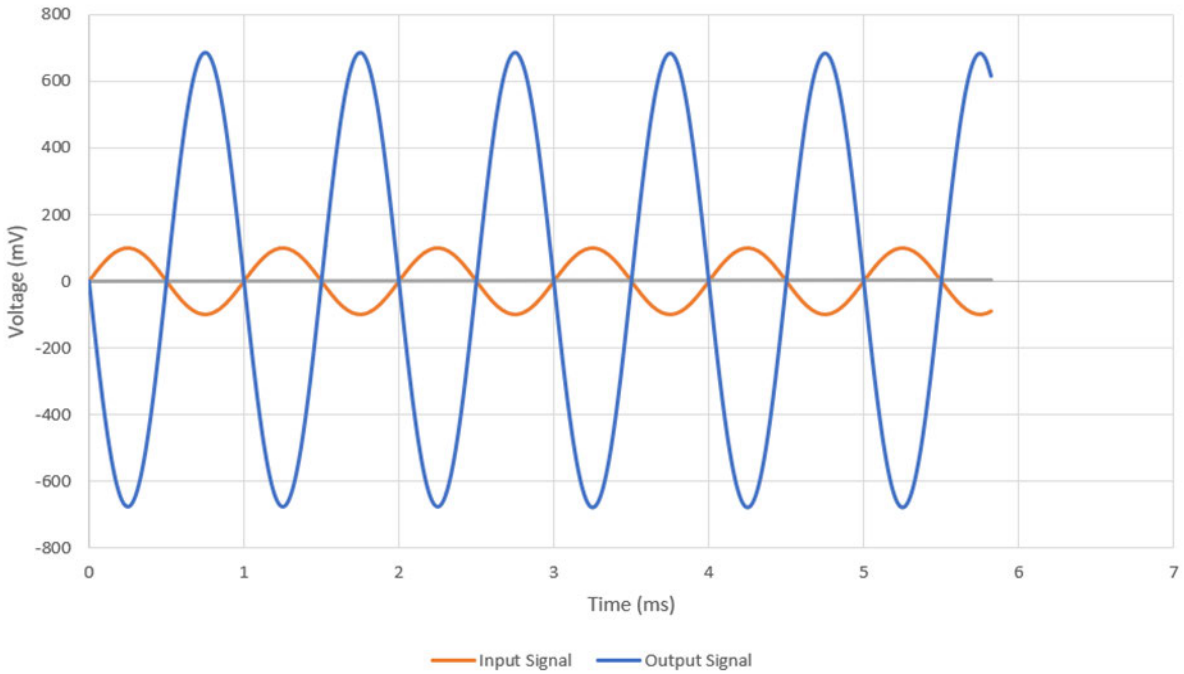


Figure 4.2 Single input – single output signal at 1 *kHz*.

Figures 4.3 and 4.4 give insight into the performance of this circuit configuration when the signal frequency on gate-1 is varied. This is very important because this shows that at what frequency this circuit cannot produce the maximum voltage gain above *65 MHz*. In Figures 4.3 and 4.4, the output voltage remains the same at *1.36 V* as the frequency changes. However, beyond *65 MHz*, the amplifier cannot produce a maximum DG, as depicted in Table 4.2.

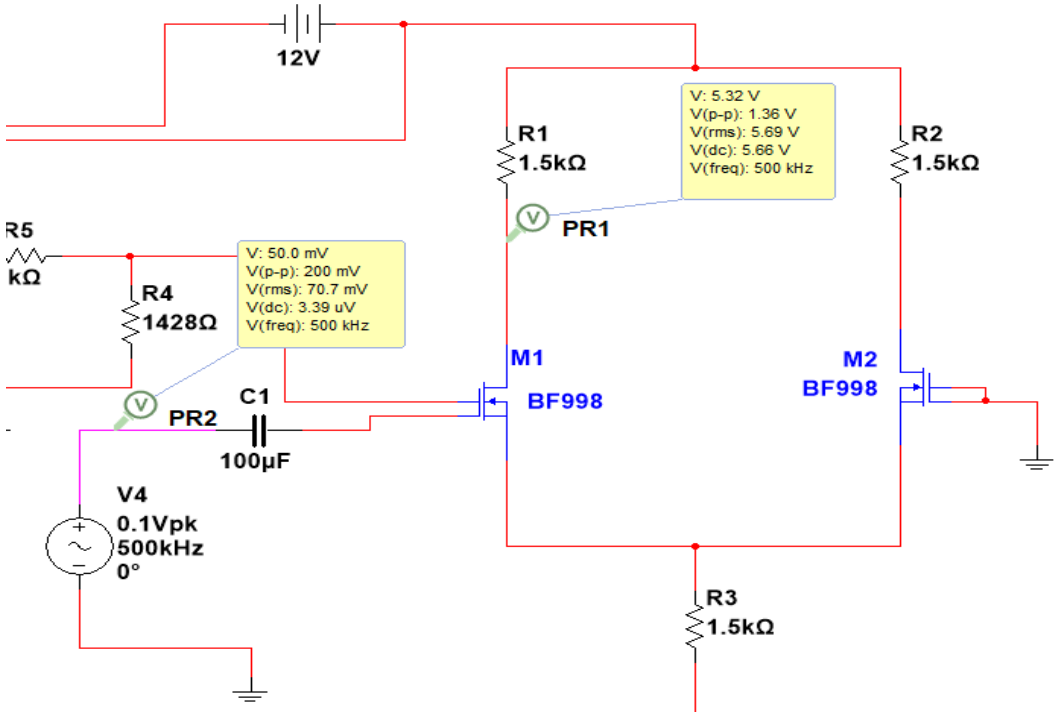


Figure 4.3 Single input – single output signal at 500 *kHz*.

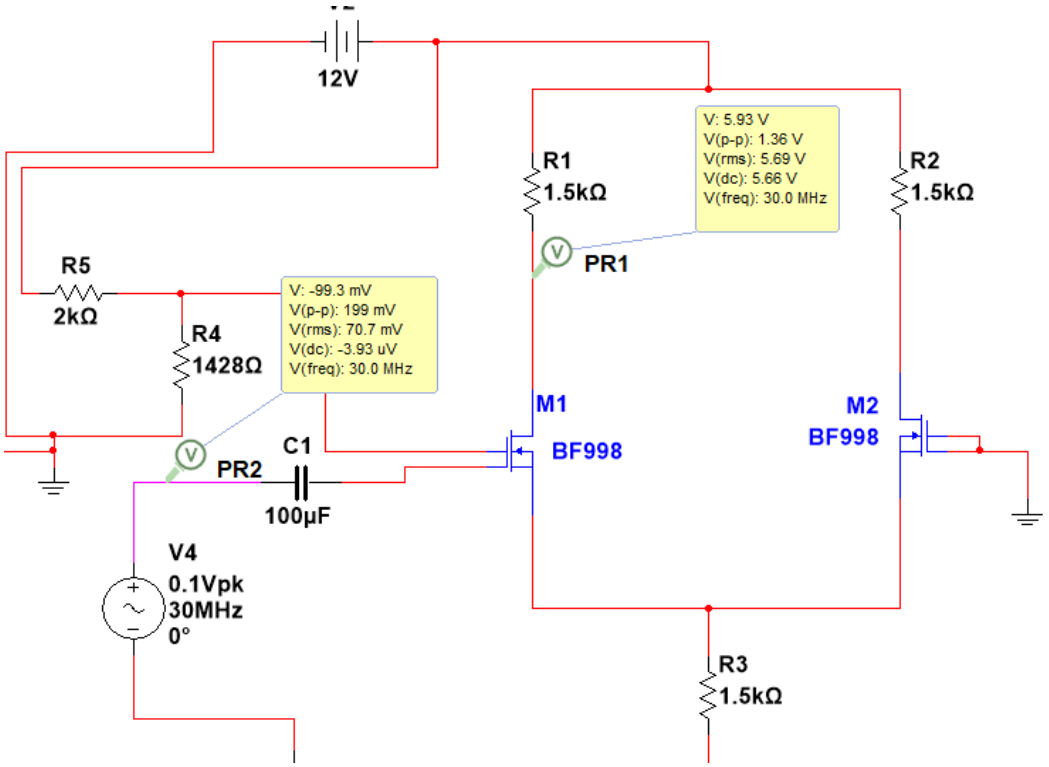


Figure 4.4 Single input – single output signal at 30 *MHz.*

Table 4.1 Single input – single output results for different values of V_4, where MOSFET-1 ($V_{G2} = 5\ V$) and MOSFET-2 ($V_{G2} = 0\ V$)

Frequency (Hz)	**MOSFET 1(V_4) ($V_{pk\text{-}pk}$)**	**Single Output Voltage ($V_{pk\text{-}pk}$)**	**Differential Gain (V/V)**
1k	0.2	1.36	6.80
1k	0.6	4.03	6.72
1k	1.0	6.59	6.59
1k	1.6	10.00	6.25

Table 4.2: Single input – single output results for different values of frequency where MOSFET -1(V_{G2} = 5 V, V_4 = 0.2 V) and MOSFET-2 (V_G = 0V)

Frequency (Hz)	**Single Output Voltage (V_{pk-pk})**	**Differential Gain (V/V)**
100k	1.36	6.80
1M	1.36	6.80
65M	1.36	6.80
70M	1.35	6.75

Varying the input AC signal is extremely important to observe the proposed circuit's performance over a wide range of amplitudes. As the amplitude of the input signal varied from *0.1* V_{pk} to *0.8* V_{pk}, the output signal was distorted from the values above *0.*5 V_{pk}. This means that the proposed DA can work as a single input and single output amplifier with an amplitude from *0.1* V_{pk} to *0.5* V_{pk}, with the highest gain at *0.*1 V_{pk}. This can be seen in Fig 4.5. This is because the MOSFET is no longer in the saturation region, and the gate-1 voltage is above the required value.

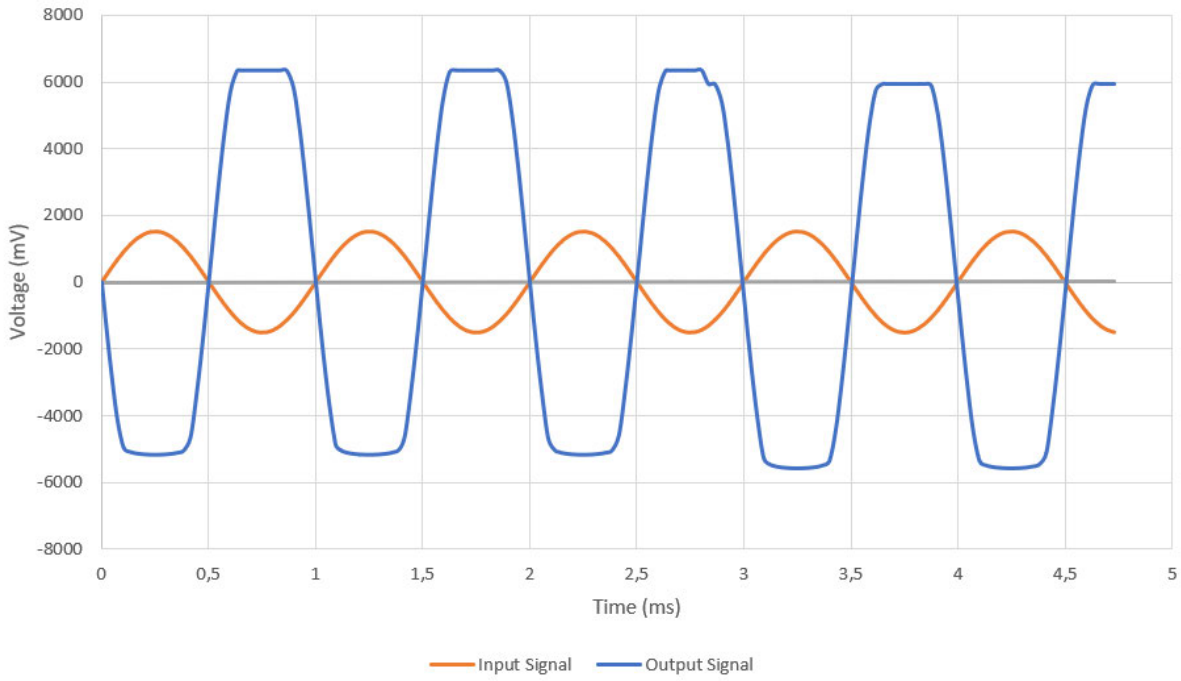


Figure 4.5 Distorted output signal with the AC input signal (V4) amplitude of *1 V*.

4.2 Single Input – Differential Output Mode

Whenever a DA has been set up with a single input and differential output, it can generate two amplified differential output signals from a single input signal. This configuration is often used in applications requiring differential signals, such as communication systems and instrumentation. In this design, the single-input signal is applied to one of the input terminals of a transistor; in this case, it is M_1. The other gate terminals of the second transistor M_2 are grounded. Figure 4.6 depicts a single-input to differential-output configuration.

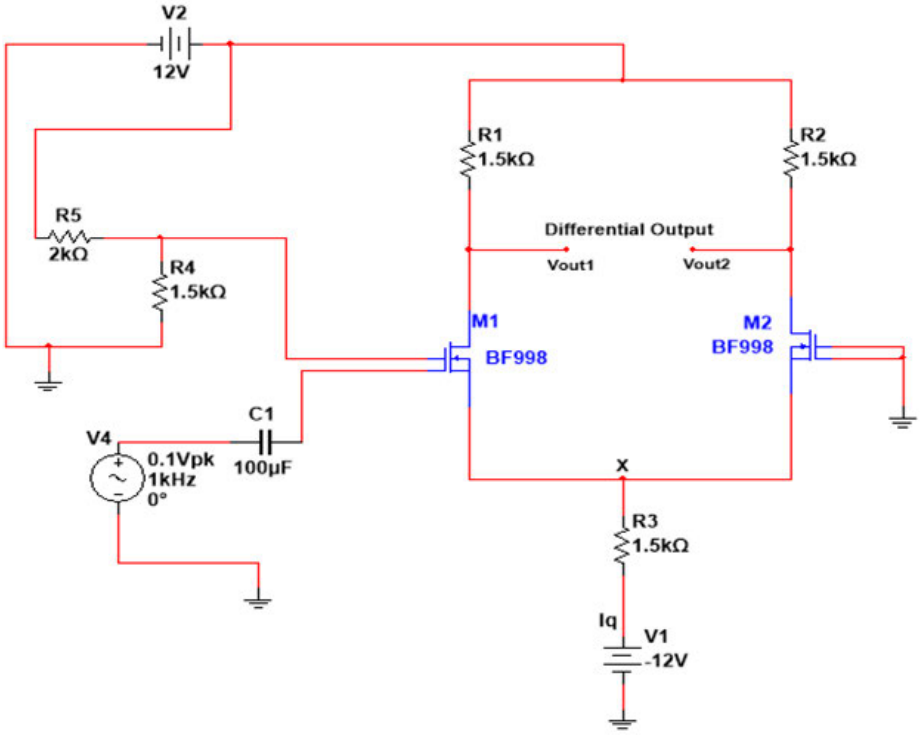


Figure 4.6 Single input – differential output circuit diagram.

4.2.1 Circuit Operation

The VD between the two input terminals is amplified by the amplifier, which produces two output signals, the differential voltage between the amplifier's output terminals. Compared with single-ended setups, this configuration provides great signal amplification, enhanced dynamic range, and enhanced noise rejection.

The differential output signal is obtained by measuring the voltage between the drains of M_1 and M_2, denoted as V_{out1} and V_{out2}, respectively. The operation of this circuit is similar to the single-input to single-output DA discussed previously, with the distinction that the output is taken differentially. When the input signal is applied to gate-1 (V_4) and its voltage rises, the signal is experienced by the source terminal M_1. Simultaneously, the signal on the source

terminal M_2 is inverted. Consequently, the output signal at the drain M_2 is in phase with the input signal, while the output signal at the drain terminal M_1 is out of phase with the input signal. This DA configuration allows the generation of two amplified differential output signals from a single-input signal. Combining the outputs from terminals one and two results in a combined signal with twice the amplitude of the individual outputs. This property makes the setup advantageous, as it effectively increases the gain of the DA by a factor of two. Furthermore, the input signal and the single-output signals are in-phase.

4.2.2 Differential Gain

The proposed DA depicted in Figure 4.6, gate-1 M_1, was supplied with an AC signal with an amplitude of *200 mV* at *1 kHz*. Gate-2 was biased with 5V to bias the MOSFET into the saturation region. The differential voltage output was measured between V_{out1} and V_{out2}, as depicted in Figure 4.6. Equation 2.2 is used to calculate DG, and the maximum differential output gain is:

$$A_d = \frac{2.62}{0.2} = 13.10(V/V)$$

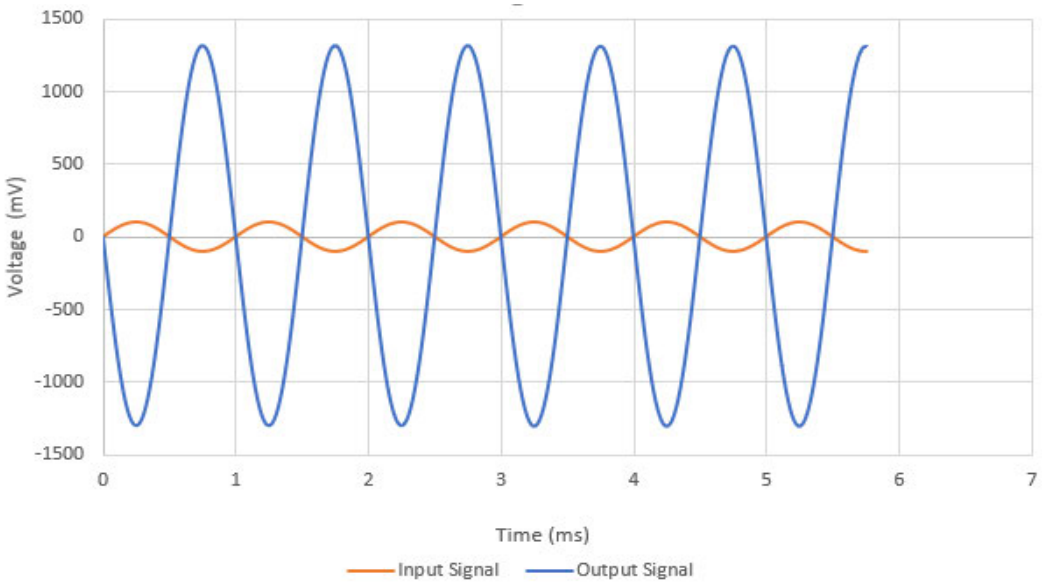


Figure 4.7 Single input – differential output signal.

One may recall that a primary reason for a DA is to amplify a difference between two input signals while rejecting common signals that might be on those input signals. The DG is typically determined by the input transistor transconductance g_m and the drain resistance R_D in the amplifier circuit. It can be observed that taking a differential output doubles the gain of the

amplifier. This is simply because, in single-ended output, only one signal is amplified, resulting in a small amplified output. In differential output, the amplified signal is measured between two input signals, resulting in a doubled output signal. This proves that operating DG MOSFETs in ASM improves the performance due to better electron mobility in the channel region and CMRR.

Figure 4.8 gives insight into the performance of this circuit configuration when the signal frequency on gate-1 is varied. In Figure 4.8, as the frequency changes, the output voltage remains the same at *2.62 V*, which is good. However, beyond *65 MHz*, the amplifier cannot produce a maximum DG, as depicted in Table 4.3. Tables 4.3 and 4.4 summarizes the results and the behaviour of this circuit configuration when the amplitude and frequency of the AC input signal are varied. Varying the signal's amplitude from *0.1 V* to *1 V* yields the depicted results in Figure 4.9. and frequency beyond *65 MHz* changes the cut-off frequency. One may observe that as the amplitude increases the differential output voltage increases, but the differential output gain decreases. As the variation occurs, the MOSFET exits the saturation region and enters the active region, where the drain current changes, lowering the DG.

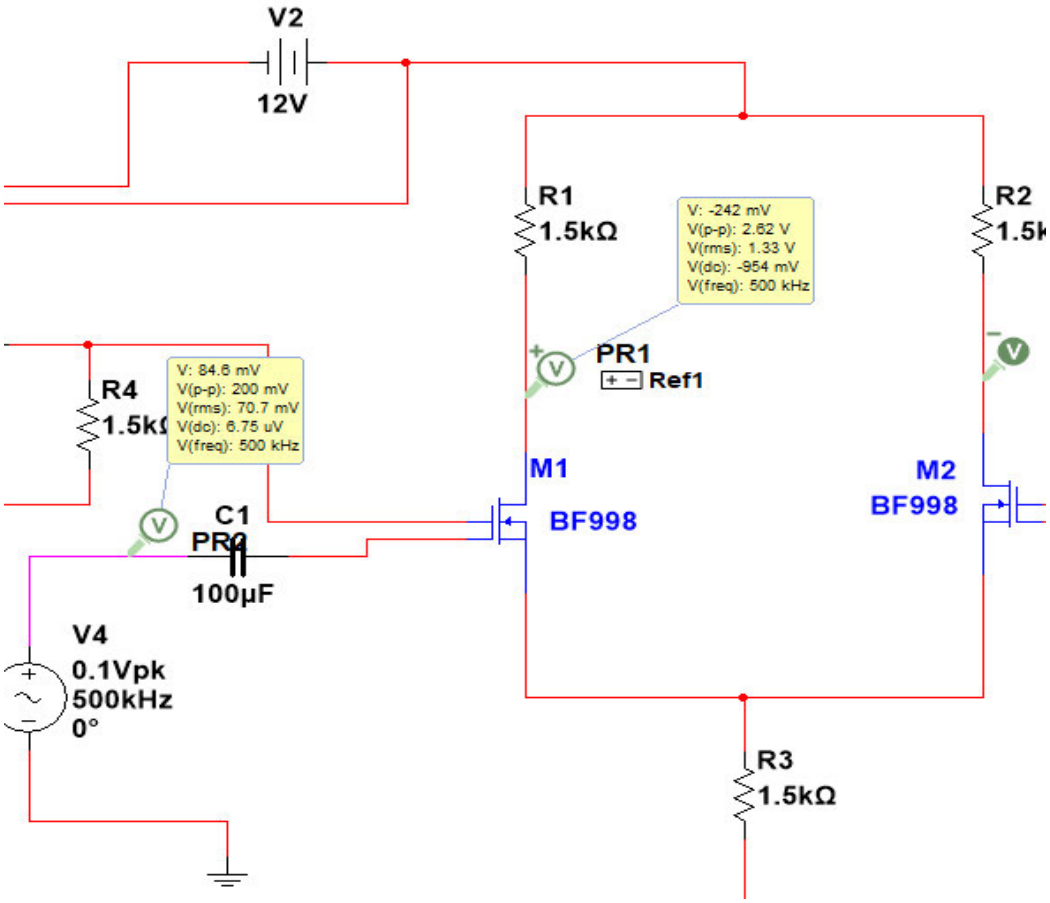


Figure 4.8 Single input – single output signal at 500 *kHz.*

Table 4.3 Single input – differential output voltage results for different values of V4 (for MOSFET-1 (V_{G2} = 5 V) and MOSFET-2 V_G = 0 V).

Frequency (Hz)	**MOSFET 1 (V_4) (V_{pk-pk})**	**Single Output Voltage (V_{pk-pk})**	**Differential Gain (V/V)**
1k	*0.2*	*1.36*	*6.80*
1k	*0.6*	*4.03*	*6.72*
1k	*1.0*	*6.59*	*6.59*
1k	*1.6*	*10.00*	*6.25*

Table 4.4 Single input – differential output voltage results at different frequencies, MOSFET-1 (V_{G2} = 5V, V_4 = 0.2 V) and MOSFET-2 (V_G = 0 V)

Frequency (Hz)	**Single Output Voltage (V_{pk-pk})**	**Differential Gain (V/V)**
100k	*1.36*	*6.80*
1M	*1.36*	*6.80*
65M	*1.36*	*6.80*
70M	*1.35*	*6.75*

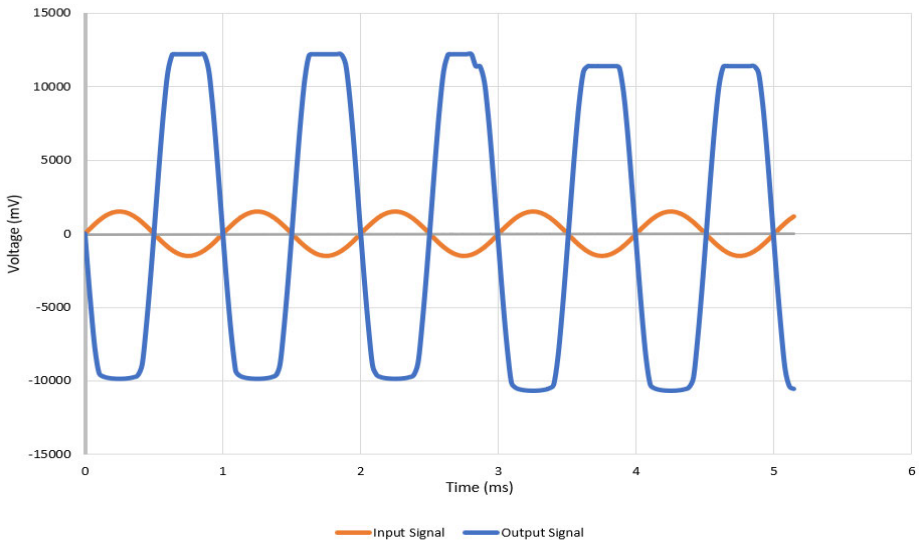


Figure 4.9 Distorted output signal with the AC input signal amplitude of *1V*.

4.3 Common Mode Input Voltage Gain (CMVG)

The amplification given to signals appearing on both inputs of the transistors relative to the common ground is called CMVG. Since a DA is intended to amplify the difference between the two voltage signals applied to the inputs of the transistors. The CMVG can be measured using the differential output voltage. Consider applying equal voltages to the inputs of the transistors as depicted in Fig. 4.10.

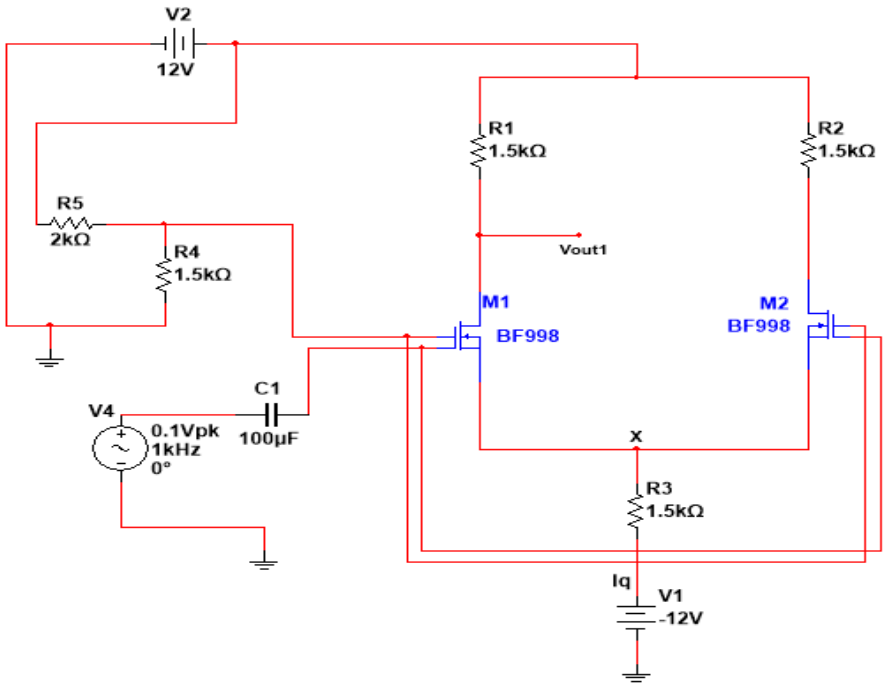


Figure 4.10 Common-mode input voltage circuit diagram.

The ideal result would be zero voltage at the output, but this is unrealistic. This is because the MOSFETs and resistors will not perfectly match in a practical situation. Whereas in simulation, the devices are assumed to match perfectly. A common mode signal can be developed by connecting the gate terminals of transistors M_1 and M_2, then attaching the connected terminals to a common voltage source. As shown in Fig. 14, gate-1 of M_1 is connected to gate-1 of M_2. This is the same as for gate-2. In ref. [57], modelling of a small common mode signal and the derivation change in drain resistance has been done. This mismatch will eventually affect the output voltage on both output sides of the DA. This means the DA will amplify that difference voltage sensed at the output. The drain resistance of M_1 is R_1, and for M_2 is R_2. This results in different output voltages. The common mode voltage gain without considering the mismatch (differentially) can be found using [58]:

$$A_{v(cm)} = -\left(\frac{\Delta R_1}{2R_3}\right) \tag{4.1}$$

And the common mode voltage gain with mismatch differentially is [58]:

$$A_{v(cm)} = -\left(\frac{\Delta R_1}{2R_3}\right)\left(\frac{\Delta R_1}{R_1}\right) \tag{4.2}$$

where ΔR_1 represents a mismatch in drain resistance. Figure 4.11 depicts the differential output signal of the common mode input signal. This proves that when the input signals have common signals and the output is measured differentially, it will be able to reject the noise and only amplifies the required signals

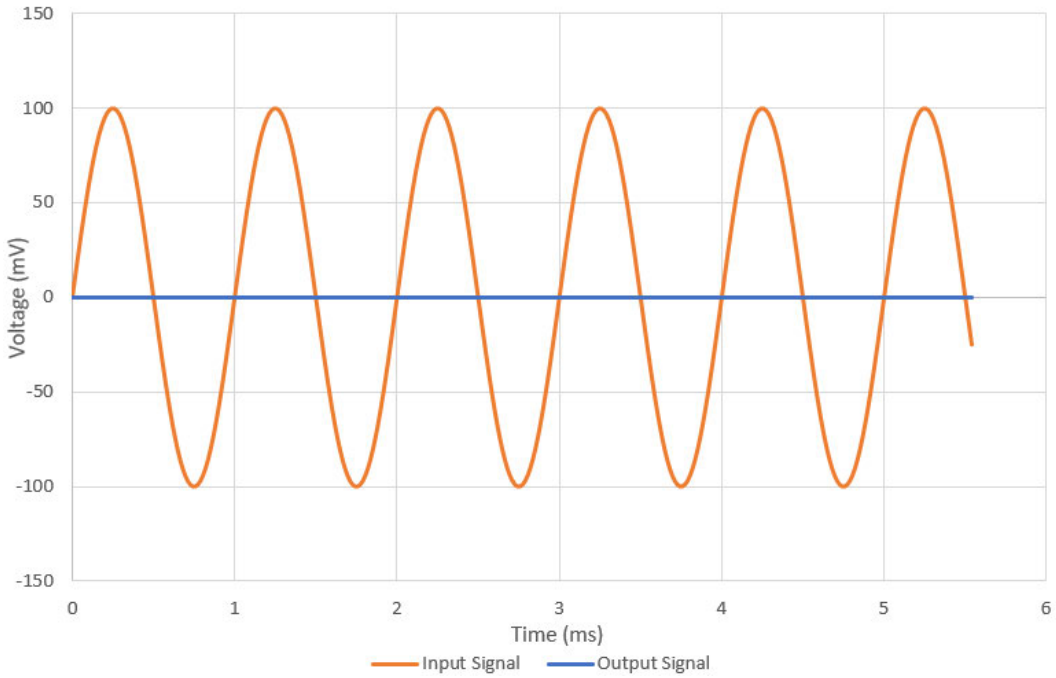


Figure 4.11 Differential output voltage signal with common mode input (DG MOSFET).

To cater to the mismatch, R_{D2} has been changed to *1.499 kΩ* instead of *1.50 kΩ* to observe the behaviour of the common mode input voltage – differential output voltage signal. The differential output voltage has been obtained as *39 μV* with the common mode input voltage of *0.1* V_{pk}, and the common mode output voltage gain has been obtained as *195 μ(V/V)*, and this is ideally zero.

4.4 Common Mode Rejection Ratio

The CMRR measures a DA's capacity to reduce signals shared by both inputs. The ideal DA has a high gain for single-ended (or differential) and no gain for common-mode signals [59, 56]. It is the magnitude of its DG $|A_d|$ divided by the magnitude of its common-mode gain $\left|A_{(cm)}\right|$ [28, 29] as:

$$CMRR \cong \frac{|A_d|}{\left|A_{(cm)}\right|} \tag{4.3}$$

and is normally expressed in dB,

$$CMRR(dB) \cong 20\log\left(\frac{|A_d|}{\left|A_{(cm)}\right|}\right) \tag{4.4}$$

The common mode rejection ratio for single input – single output and single input – differential output voltage is *34.87 k(V/V) (90.85 dB)* and *67.18 k(V/V) (96.54 dB),* respectively.

4.5 Frequency Response (FR)

The FR of a DA is critical for comprehending its behavior and performance at various frequencies. It provides various critical functions. It enables researchers and engineers to assess the stability of the amplifier's gain over the ideal frequency range, providing accurate signal amplification. Furthermore, it contributes to determining the amplifier's bandwidth, which defines the frequency range within which it can successfully amplify signals without distortion or loss. Obviously, it depends on the circuit's design requirements. The amplifier will not perform adequately above a certain cut-off frequency. Using Eq. 4.5, the FR can be calculated as follows [59, 60, 61]:

$$f = \frac{1}{2\pi C_T R_{DS}} = \frac{1}{2\pi\tau} \tag{4.5}$$

where τ as a time constant. Figure 4.12 depicts the FR of the single input – single output DA using double gate MOSFET. The designed DG MOSFET-based DA, cut-off frequency for single input – single output, and gain magnitude have been obtained as *30 MHz* and *17 dB,* respectively.

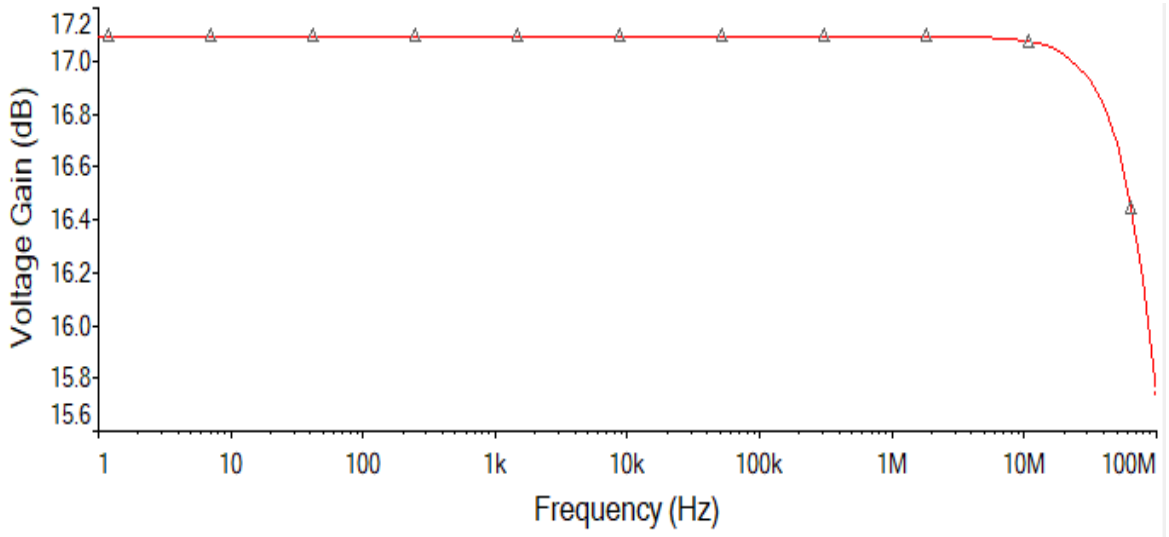


Figure 4.12 FR for single input – single output.

The cut-off frequency for single input–differential output was *60.167 MHz* with a gain magnitude of *23.4 dB*. Figure 4.13 depicts the FR of the single input–differential output DA using double gate MOSFET has a wide bandwidth. It will be able to accommodate or be used in different applications. A comparative analysis of various parameters has been summarized in Table 4.5. The results show that the proposed DA outperforms the existing designs, especially for the gain and FR.

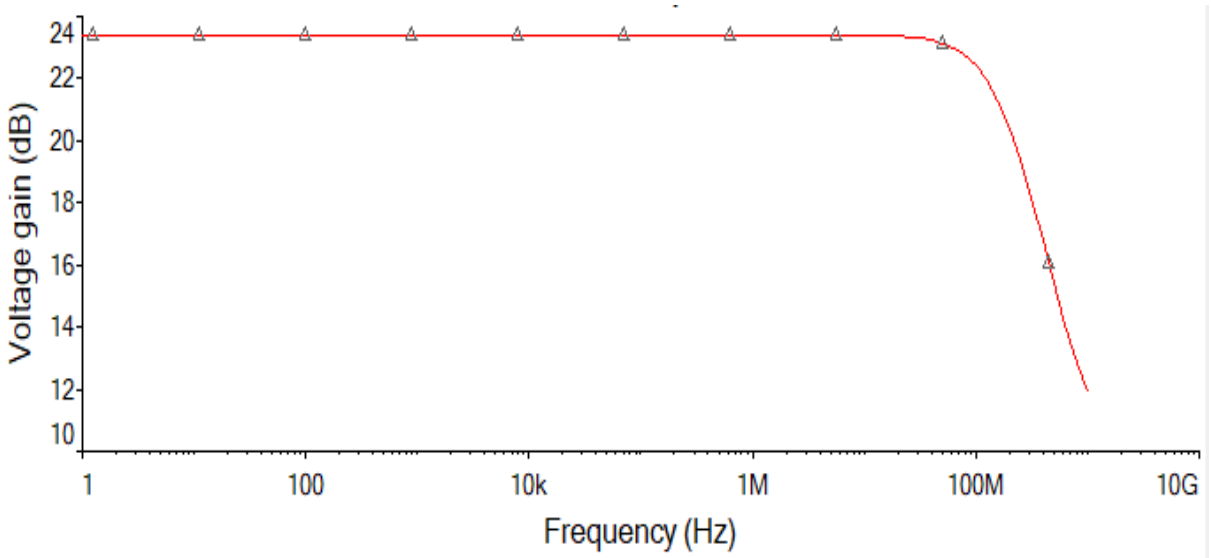


Figure 4.13 FR for single input – differential output.

4.6 Comparative Analysis

The aforementioned comparisons can be adapted from [28, 29], which includes a design and comparative analysis of active and resistive loaded DA using double-gate MOSFET. Further comparative analysis with existing designs that used SG MOSFETs has been done. Table 4.5 contains a list of them.

Table 4.5 Comparative analysis of the designed DA using DG MOSFET with existing models.

References	**Device**	**Gain (dB)**	**Common mode gain (V/V)**	**CMRR (dB)**	**Cut-off frequency (kHz)**
[62]	DG MOSFET	18.8	32×10^{-3}	19.06	29000
[63]	DG MOSFET	4.6-5.1	84.62×10^{-6} to 3.7×10^{-3}	>75	42000
[62]	SG MOSFET	18	-	11.34	0.0987
[58]	SG MOSFET	70	-	72	30000
[64]	SG MOSFET	50	-	-	200
[57]	SG MOSFET	59	-	-	-
This work	DG MOSFET	22.3	39×10^{-6}	96.54	60000

A proposed DG-based DA performs better than existing designs for several factors. The proposed design achieves a greater DG, enabling more precise and sensitive amplification of the VD between the input signals. As a result, signal quality and resolution are improved. Furthermore, it has improved linearity, which reduces distortion and ensures a precise representation of the input signal. Lastly, it provides a greater CMRR, allowing undesired noise and interference in both input signals to be efficiently rejected. Better and more precise differential output results from this. The amplifier is capable of functioning efficiently over a wider range of frequencies. Based on the comparison in Table 4.5, one can observe that the proposed design of DG MOSFET-based DA proves to outperform the already existing models/designs with respect to voltage gain, CMRR, and cut-off frequency. This proves that operating the DG MOSFET in ASM provides a wide room to control electron mobility, and the system is able to reject common signals and reduce SCE.

4.7 Chapter Conclusion

A detailed analysis has been conducted in this section, which discusses how the circuit configuration of single input – single output and single input – differential output operates. Parametric analysis has been explored that includes common-mode input, CMRR, and FR. Furthermore, a comparative analysis with existing designs has been conducted. Lastly, the obtained results have shown that the proposed solution can amplify the input signal (single-ended and differentially) with a much greater factor than the already existing design, which signifies that operating the DG MOSFET is asymmetrical mode and being able to bias the gate correctly has a great impact on the performance of the DA. Even though this circuit does not explore the full capacity of a differential, the upcoming section will analyse differential input–differential output circuit configuration, which explores the full capabilities of a DA.

Chapter-5

DIFFERENTIAL INPUT - DIFFERENTIAL OUTPUT AND LOSS ANALYSIS OF A DG-BASED DIFFERENTIAL AMPLIFIER

5.1 Differential Input with Differential Output

Figure 5.1 depict differential input with differential output DG-based DA configuration. In this configuration, both devices, M_1 and M_2, are used. The two input signals must be out of phase so that they will not cancel each other. One may remember that the primary aim of a DA is to amplify the difference between two input signals while rejecting common signals to both inputs. To achieve this, the signal M_1 has a phase of 0^o, and the phase in the M_2 is 180^o as depicted in Figure 5.1. This ensures that these two signals are out of phase.

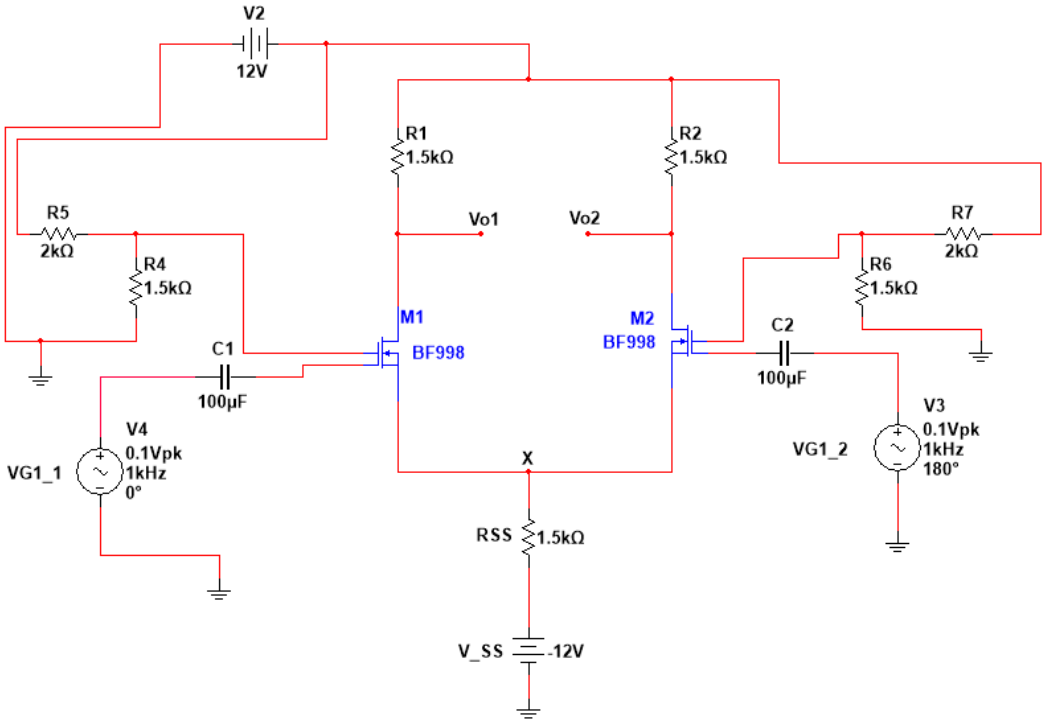


Figure 5.1 Differential Input–Differential Output circuit diagram.

5.1.1 Circuit Operation

The full capacity of the circuit is utilized when a DA is connected with a differential input and a differential output. Typically, two input signals that are 180^o out of phase are used in this topology. Due to this, the differential signal is doubled as large as each input. This is

similar to the two-input single-output DA having 180° out of phase input signals. The first output is a signal in phase with the second input, and the second output is a signal in phase with the first input signal. The amplitude of each output signal is equal to the input signal scaled by the amplifier's gain. With 180^o out-of-phase input signals, each output signal has an amplitude multiplier of the amplifier's gain larger than both input signals. When an output signal is measured between the amplifier's two output terminals, as indicated by V_{o1} and V_{o2} in Figure 5.1. The resultant output signal has double the amplitude of either signal at V_{o1} or signal at V_{o1} V_{o2}. This is because V_{o1} and V_{o2} are 180^o out of phase with each other. When the input signals are 180^o out of phase, the combined output signal has an amplitude equal to the amplitude of one input signal multiplied by two times the amplifier's gain.

5.2 Differential Gain

A differential voltage gain is an essential parameter that indicates the capability of the amplifier to amplify the voltage difference between its two input signals. It quantifies the amplification factor for the differential mode signal and provides insight into the amplifier's performance in amplifying the desired signal while rejecting common-mode noise. The DG can be measured with either a differential or a single-ended output. In this section, the differential output gain is measured differentially, and Eq. (2.7) is used to observe the proposed amplifier's performance when operated in this configuration.

$$A_d = \frac{V_{o1} - V_{o2}}{V_4 - V_3} = \frac{5.42}{0.4} = 13.55(V/V)$$

Figure 5.2 depicts the graphical results of the proposed amplifier's differential input and output mode. Gate-2 of both M_1 and M_2 are biased with *5 V*, and gate-1 of M_1 is supplied with a signal with a phase of 0 and an amplitude of $0.1\ V_{pk}$ with a frequency of *1 kHz*. The same is done on signal to M_2, except that it has a phase of 180^o. The depicted results show that the circuit configuration can achieve doubled gain than single-ended gain. It can utilize its full capability by amplifying the difference between two input-out phase signals.

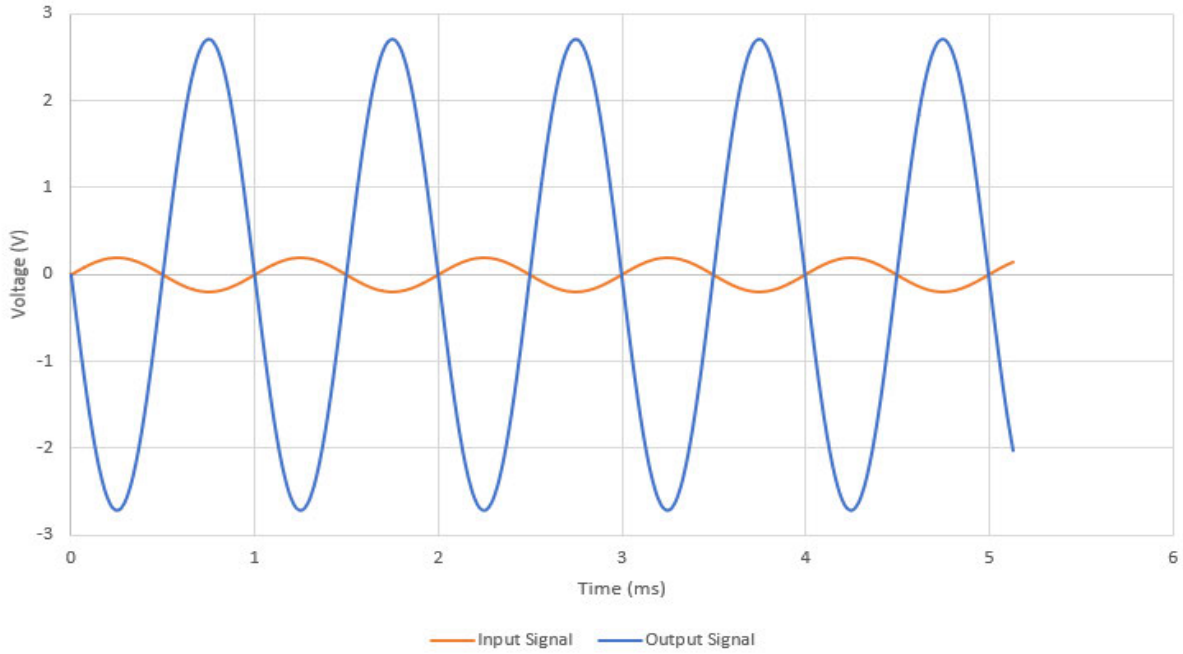


Figure 5.2 Differential input – Differential Output signal of a designed DA.

Varying the amplitude of input signals enables us to analyze the small-signal gain of the proposed DA. Applying small-signal input with different amplitudes helps in linearizing the behavior of the double gate MOSFETs around the saturation region. This helps by understating the capabilities and linearity of the proposed DA. Table 5.1 demonstrates the behavior of this circuit when the amplitude varied.

Table 5.1 Differential input – differential output voltage results for different values of V_{G1_2} *(for* $V_{G1\text{-}1}$ *(*V_{pk}*)= 0.1 V)*

Frequency (Hz)	**VG1_2 (V_{pk})**	**Differential Input voltage ($V_{pk\text{-}pk}$)**	**Differential Output voltage ($V_{pk\text{-}pk}$)**	**Differential Gain (V/V)**
1k	*0.1*	*0.4*	*5.42*	*13.55*
1k	*0.3*	*0.8*	*10.70*	*13.38*
1k	*0.5*	*1.20*	*15.70*	*13.08*
1k	*0.8*	*1.80*	*21.40*	*11.89*

From the values demonstrated in Table 5.1, it can be observed that when the amplitude increases, the differential gain decreases. This is because in order for the amplifier to maximize

the DG, MOSFETs must remain in the saturation region so that the electron mobility will increase in the channel region, which eventually increases the gain of the amplifier. As the amplitude of V_{G1_2} is varied from *0.1* to *0.8* while V_{G1_1} is kept constant at *0.1*, the maximum gain is achieved when both signals have *0.1* amplitude and decrease when V_{G1_2} is varied.

5.3 Common Mode Input Signal

Consider applying identical input voltage signals to the two gate terminals. As depicted in Fig. 4.10, Because the two MOSFETs gate terminals share the same signal, it is referred to as a common-mode input signal. It has been proved that if both MOSFETs remain in the saturation region, the drain current will divide equally amongst M_1 and M_2, and the drain voltage will not change [65, 66]. As a result, the DA rejects common-mode input signals, as shown in Figure 5.3. The output voltage is $1.23\ pV \approx 0\ V$, and this is ideally zero. In real life, the output voltage is not *0 V* because of a mismatch in transistors and resistors. The maximum common mode voltage gain is obtained as:

$$A_{(cm)} = \frac{V_{d(out)}}{V_{d(in)}} = 6.15\times10^{-12}(V/V) \tag{5.1}$$

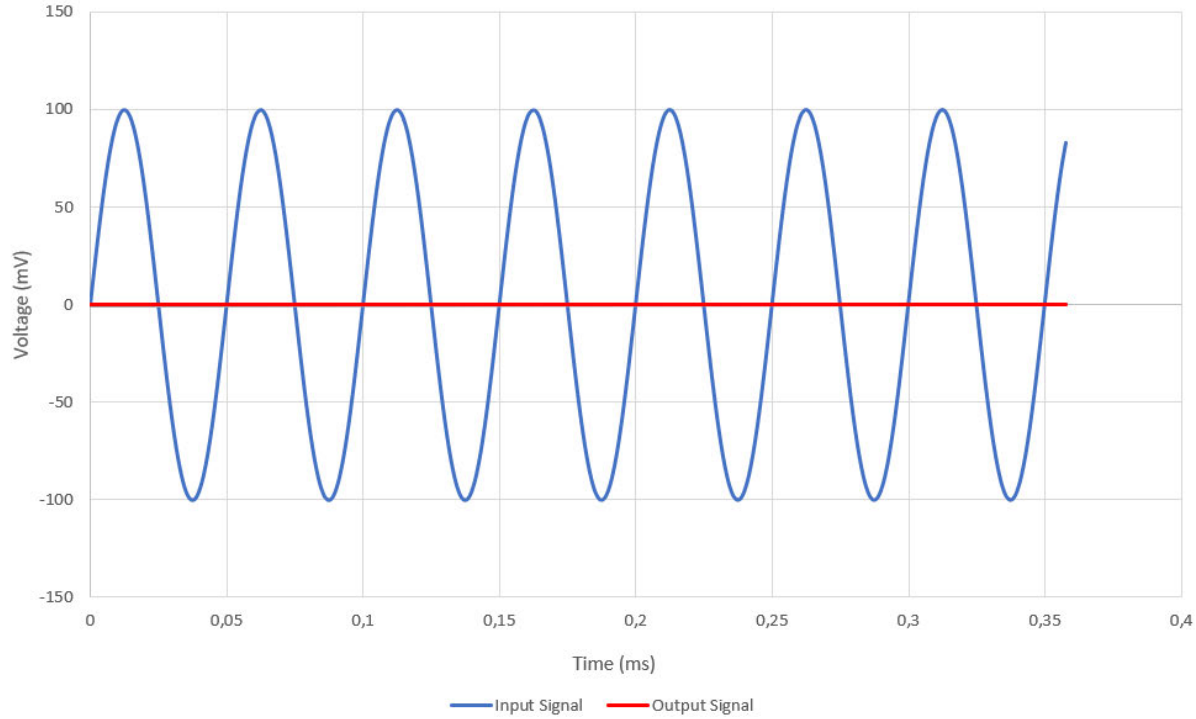


Figure 5.3 Common mode differential input voltage–differential output voltage signal.

These results show that the result will be zero regardless of one measure the output single-ended or differentially. The transistors share the same input signals, which shows the capability of this proposed DA to reject noise that might be in the system because, most of the time, the noise signal is the same.

5.4 Common Mode Rejection Ratio

The CMRR of a DA assesses the device's ability to discard input signals similar to both inputs. A high CMRR is significant in applications where a small voltage fluctuation represents the signal of importance superimposed (potentially substantial) voltage offset or when the voltage difference between two signals comprises a noise signal. The CMRR of a DA defines the offset attenuation [67] can be found as:

$$CMRR = \frac{|A_d|}{|A_{cm}|} \tag{5.2}$$

where $|A_d|$ is the absolute value of the differential output voltage gain and $|A_{cm}|$ is the absolute value of the common mode input voltage signal. Using Eq. (5.2), the value of *CMRR* is calculated as follows:

$$CMRR = \frac{13.55}{6.15\times10^{-12}} = 2203\times10^{9} \tag{5.3}$$

5.5 Frequency Response

The degree to which an amplifier functions appropriately with respect to a particular frequency range is measured by its FR. The DA will not work properly above a specific cut-off frequency [68-70]. Furthermore, varying the frequency allows one to analyse the FR of the DG-based DA. This helps to understand the bandwidth, cut-off frequencies, and stability of the DG-based DA. With reference, the FR can be determined using Eq. (4.5). The values demonstrated in Table 5.2 show that when the frequency increases, the DG decreases. The amplifier maximizes the DG, and MOSFETs must remain in the saturation region so that the electron mobility will increase in the channel region, which eventually increases the gain of

the amplifier. The maximum gain is achieved up to *65 MHz*, and this means that beyond this value, the electron mobility in the channel region decreases, and MOSFETs are no longer in the saturation region. Figure 5.4 depicts the FR of differential input – differential output amplifier having a magnitude of *35 dB*, which is far better than single-ended mode.

Table 5.2 Differential input – differential output voltage results at various frequencies

MOSFET-1 (V_{G1_1} = V_{G1_2} = 0.1 V)

Frequency (Hz)	**Differential Input voltage (V_{pk-pk})**	**Differential Output voltage (V_{pk-pk})**	**Differential Gain (V/V)**
1k	*0.4*	*5.42*	*13.55*
500k	*0.4*	*5.42*	*13.55*
65M	*0.4*	*5.41*	*13.52*
70M	*0.4*	*5.20*	*13.00*

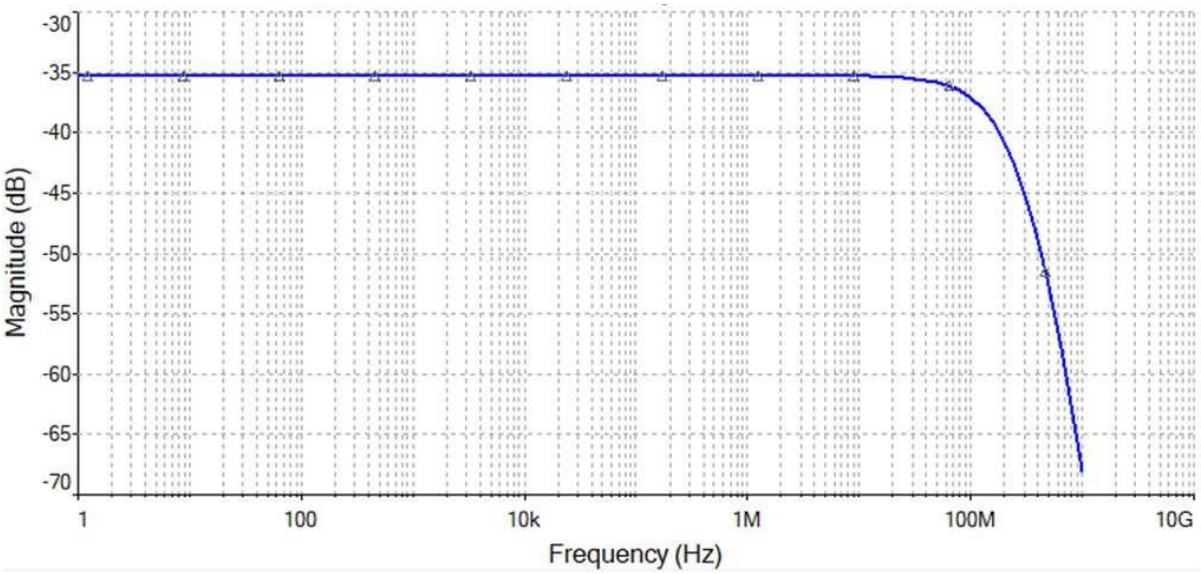


Figure 5.4 FR of a differential input – differential output amplifier.

5.6 Loss Analysis in DG-Based Differential Amplifier

5.6.1 Conduction Losses (CL)

Conduction Losses (CL) refer to the power loss whenever the transistor is in the conducting state (ON-state). Several factors cause CL which, amongst others, include channel resistance and leakage current. When the MOSFET conducts, the current flows through the channel region between the source and the drain terminals. Nonetheless, there is some resistance in this channel region, which causes power to be lost in the form of heat. The resistance in this channel region is caused by the doping profiles and dimension of the MOSFET, which is referred to as channel resistance.

On the other hand, leakage current occurs when the MOSFET is in the OFF state, but there is a flow of current. One would expect that when a transistor is OFF, there should be no flow of current, but that does not happen, and this is caused by various factors such as gate leakage and subthreshold leakage. This eventually leads to a current leakage which contributes to CL [71-73]. Analysing and calculating CL is very important because it shows how much the MOSFET loses power during its conducting state. The CL in MOSFETs can be calculated using MOSFET approximation with the drain-source on-state resistance $R_{DS(on)}$ shown on eq. (5.4):

$$u_{DS}(i_D) = R_{DS(on)}(i_D) \bullet (i_D) \tag{5.4}$$

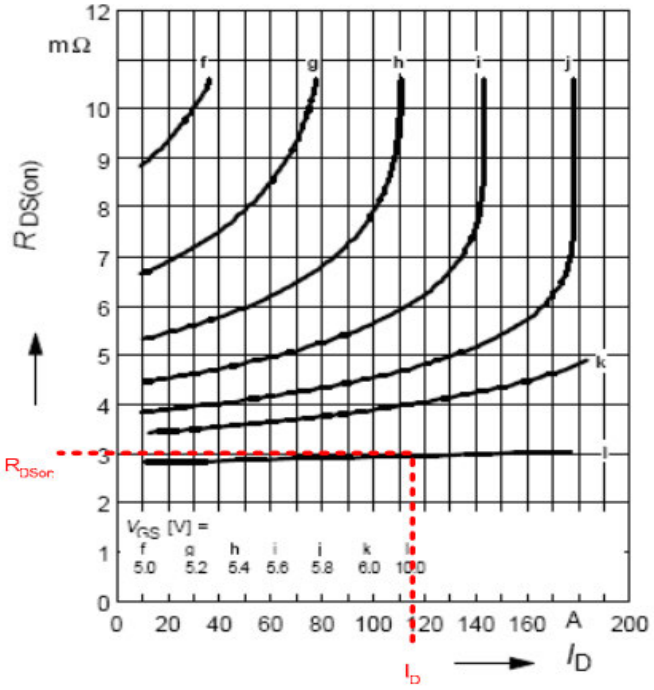


Figure 5.5 Drain-source resistance as the function of drain current.

u_{DS} and i_D are drain-source voltage and drain current, respectively. The value $R_{DS(on)}$ can be read from the diagram depicted in Figure 5.5. Here the value $R_{DS(on)}$ depends on the drain current [74,75]. The instantaneous value of the MOSFET conduction loss can also be determined using eq. (5.6) [76-78]:

$$p_{CM}(t) = u_{DS}(t) \bullet i_D(t) = R_{DS(on)} \bullet i_D^2(t) \tag{5.6}$$

The integration of the instantaneous power loss over the switching cycle of the MOSFET can be determined using eq. (5.7):

$$P_{CM} = \frac{1}{T_{SW}} \int_0^{T_{SW}} p_{CM}(t)dt = \frac{1}{T_{SW}} \int_0^{T_{SW}} (R_{DS(on)} \bullet i_D^2(t))dt = R_{DS(on)} \bullet I_{D(rms)}^2 \tag{5.7}$$

where $I_{D(rms)}$ is the root-mean-square value of a drain current in an ON-state of the MOSFET. An alternative technique using eq. (5.8) to calculate CL is to use the MOSFET's drain-source voltage (V_{DS}) and drain current (I_D):

$$P_{loss(cond)} = V_{DS} \times I_D \tag{5.8}$$

According to a BF998 data sheet, the maximum value for V_{DS} is *12 V* [77,78]. The drain current is then calculated as:

$$I_D = \frac{V_{DS}}{R_{SS}} = \frac{12}{1.5 \times 10^3} = 8mA \tag{5.9}$$

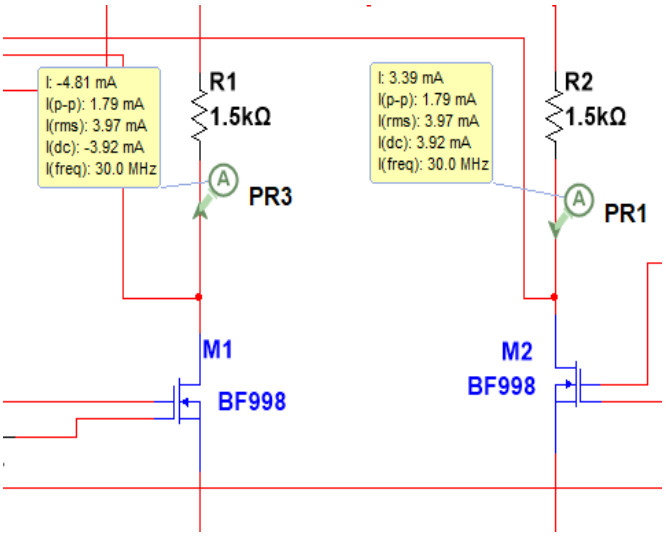


Figure 5.6 Measured drain current for M_1 and M_2

The result calculated in Eq. (5.9) is the drain current generated by the CCS. With the circuit configuration discussed in section 5.1, the amplitude and frequency of both signals are the same, and the only difference is phase. So, since the MOSFETs are in the saturation region, the drain current will be equally halved between the two devices [78]. Figure 5.6 depicts the measured drain current for M_1 and M_2. The conduction loss for each device is then determined using eq. (5.8):

$$P_{loss(cond)} = (12)(3.92\times10^{-3}) = 47.04mW$$

One may observe that the root-mean-square value of the drain current is slightly different due to a mismatch between resistors and transistors. However, this difference is negligible.

5.6.2 Switching Losses

Switching losses occur when a MOSFET switches from the ON-state to the OFF-state or vice versa. The energy needed to charge and discharge the device's parasitic capacitances, such as the gate-source capacitance C_{gs} and the drain-source capacitance, causes these losses C_{ds} [72].

The two gates of double-gate MOSFETs makes-up two in-series capacitors, and the sum of two in-series capacitors is less compared to a SG MOSFET. From the basis of science, the sum of two in-series capacitors is calculated using eq. (5.10) [80, 81]:

$$C_{TOT} = \frac{C_1 C_2}{C_1 + C_2} \tag{5.10}$$

Utilizing the MOSFET's turn-ON and turn-OFF times is a method for analyzing switching losses. The time it takes for a MOSFET to transition from its OFF-state to its ON-state is known as the turn-ON time, and the reverse is valid for the transition from its ON-state to its OFF-state or turn-OFF time. Eq. (5.11) can be used to determine switching losses.

$$P_{loss(SW)} = \frac{1}{2} * C * V^2 f_{SW} \tag{5.11}$$

where *C* is the parasitic capacitance, *V* is the voltage across the device, and *f* is the switching frequency, which can be used to calculate the switching loss. The BF998 data sheet shows the gate-source capacitances for gate-1 and gate-2 terminals; the typical values are *2.1 pF* and *1.2 pF*, respectively. Using Eq. (5.10) to calculate the capacitance between gate-1 and gate-2, the total capacitance is *0.76 pF*. The power loss due during switching for each device is:

$$P_{loss(SW)} = \frac{1}{2} \times (0.76 \times 10^{-12})(12)^2 (1k) = 0.055 \mu W \tag{5.12}$$

The calculated switching can be noticed that it is very, and that is a good thing because that means this device loose less power through heat during switching (ON and OFF). The losses increase as the switching frequency increases. For instance, the cut-off frequency for the proposed DA is *65 MHz*, the loss at this frequency will be:

$$P_{loss(SW)} = \frac{1}{2} \times (0.76 \times 10^{-12})(12)^2 (65 \times 10^{6}) = 24.7 \mu W \tag{5.13}$$

Comparing this power loss at higher frequency with low frequency, one may observe that the loss has increased significantly because switching frequency is directly proportional to the switching power loss, but it is still low.

5.6.3 Total Power Loss

When utilized in an amplifier design, DG MOSFETs can be advantageous over conventional SG MOSFETs due to their high thermal capacity, low switching losses, and CL. The comparisons between DG MOSFET and single gate-based amplifiers that are now available demonstrate that DG MOSFETs can produce an amplifier design that is more compact while also increasing system efficiency. The amplifier efficiency can be increased by employing DG MOSFETs, particularly at high switching frequencies and junction temperatures [82,83].

In this research work, switching and CL have been analyzed. In order to get insight into the total losses on the proposed DG-based DA, additional loss due to the CCS is also included.

The total power loss due to conduction and switching for both MOSFETs is *47.09 mW*. The power loss due to a CCS is *96 mW*. The total loss on the system is *143.09 mW*. The CCS contributes more losses; to reduce this effect, a current mirror that utilizes active devices would help reduce the power losses.

5.7 Chapter Conclusion

The parametric analysis of a DG-based DA that has differential input – differential output configuration. The circuit explores the full capabilities of a DA because it has two input signals 180 degrees out of phase, and the out is measured by taking the difference between the two output terminals. It has demonstrated that it can amply the difference between two input signals and has a wideband width. Conduction and switching losses have been analysed. The upcoming section will discuss the prototyped design.

Chapter-6

FABRICATED DESIGN AND ANALYSIS OF DG MOSFET BASED DIFFERENTIAL AMPLIFIER

The proposed design of a DG-based DA has been fabricated using VB to evaluate its practical performance further depicted in figure 6.1 and 6.2. The modes of operation analyzed on the simulated DG-based DA, which includes single input – single output, single input – differential output, and differential input – differential output, were also analyzed on the prototyped design. Parameters such as DG, common mode gain, and *CMRR* are measured using the oscilloscope. Figure 18 depicts the prototyped design and its setup. The function generator was used to generate a high-frequency signal injected on gate-1 of M_1 and M_2. A dual supply voltage source of $\pm$ *12 V* was used for the designed circuit, and 5 V was used to bias gate-2 of both transistors.

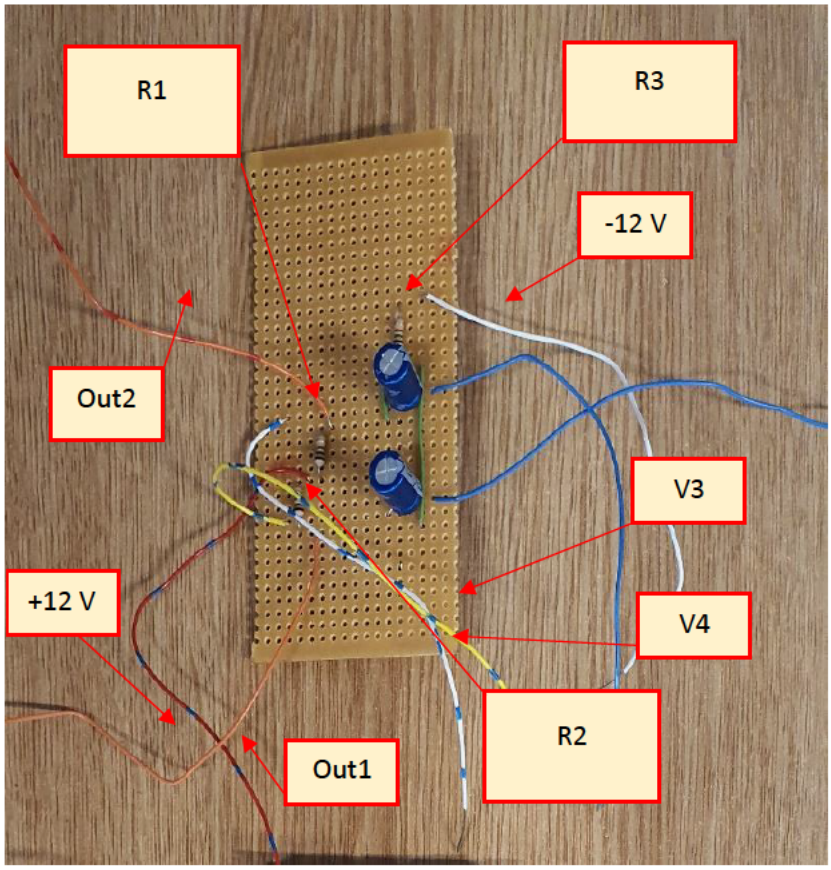


Figure 6.1 Top-view of a prototyped design.

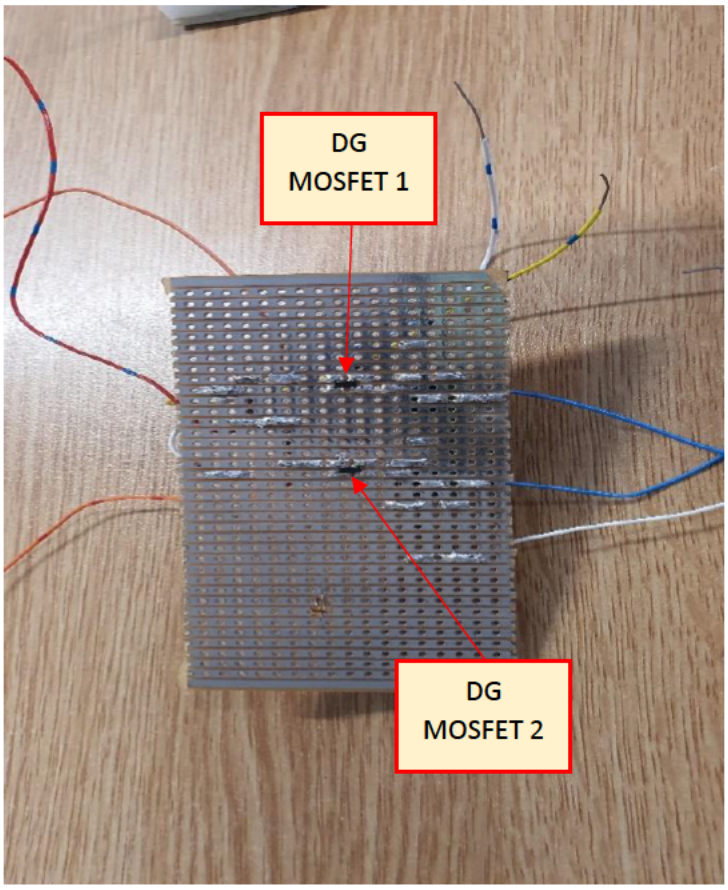


Figure 6.2 Bottom view of a prototyped design.

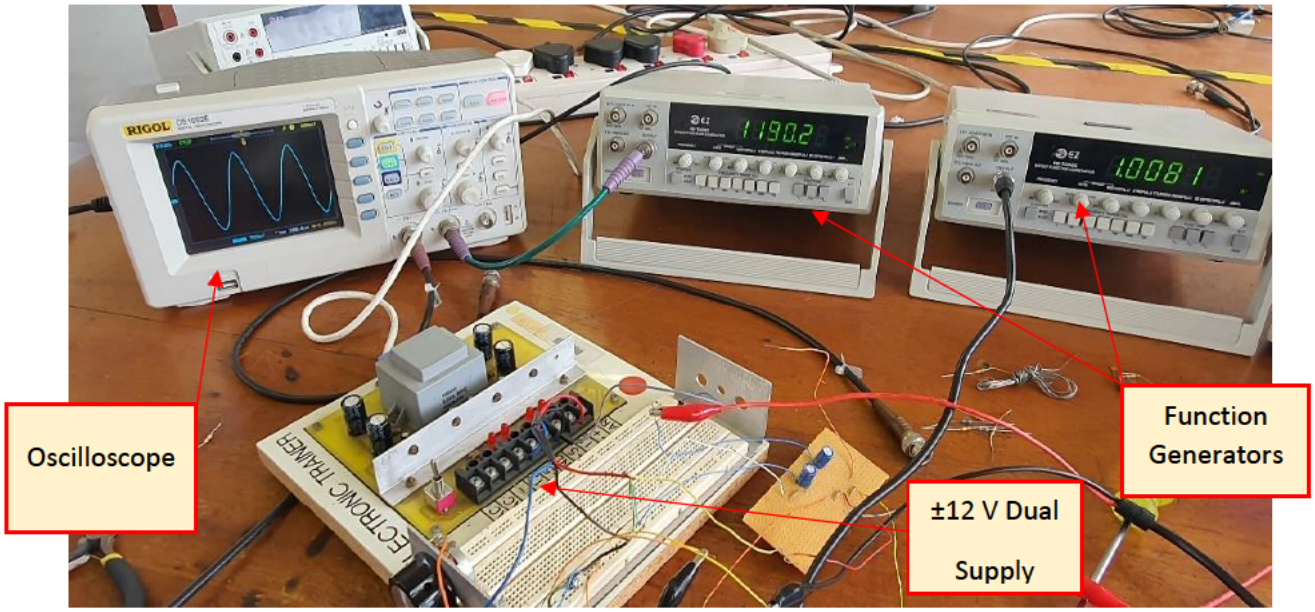


Figure 6.3 Complete setup for a prototyped design and measuring instruments.

The two signal generators were used as depicted in figure 6.3 to generate two signals for both transistors. Due to the model of these signal generators, it was not possible to tune

them to be 180 degrees out of phase to one another, and that became a challenge, but we had to design a simple phase shifter.

6.1 Single Input – Single Output mode

Using a signal generator, a signal with a frequency of *1 kHz* was generated for a single input–single output circuit configuration. This aims to test the behaviour and response of the prototyped design and compare it to the simulated design. The amplitude of the applied signal was then varied to observe the behaviour or response of the circuit, and Table 6.1 demonstrate the measured results. Figure 6.4 depicts the maximum output signal from the applied signal.

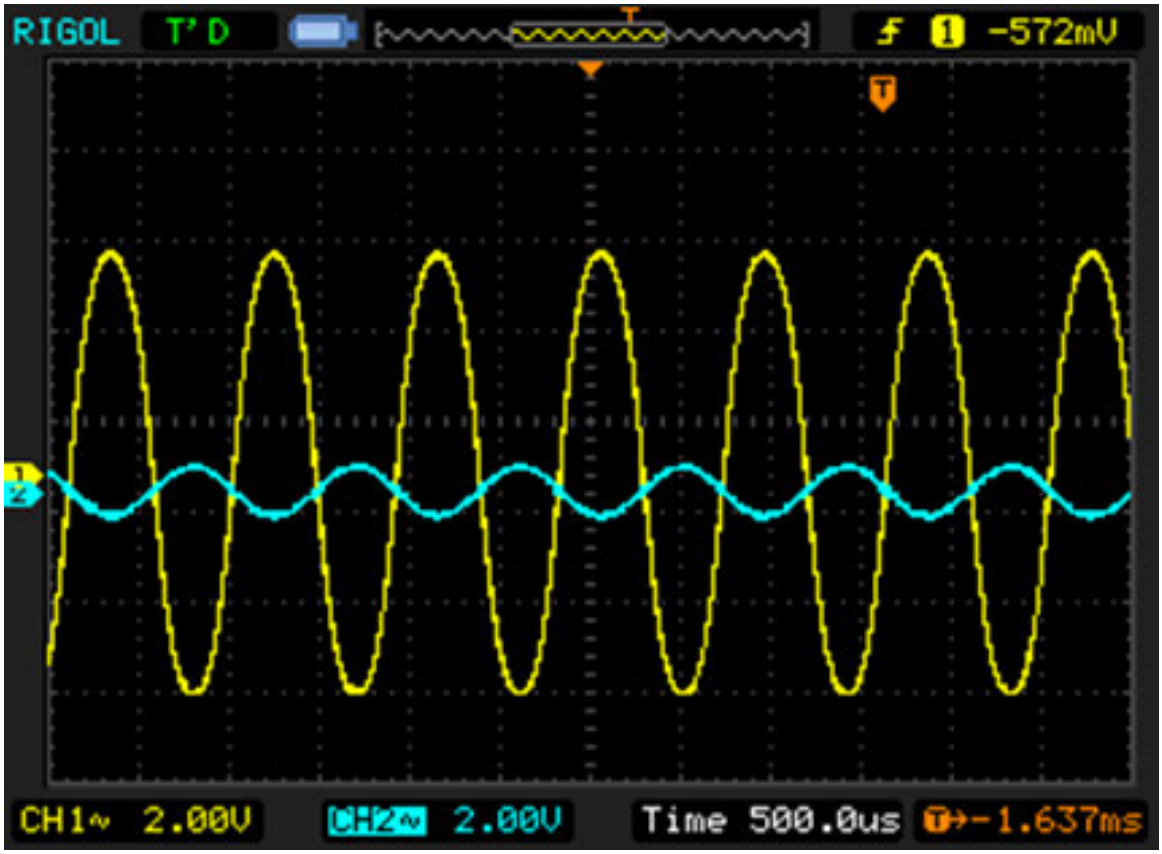
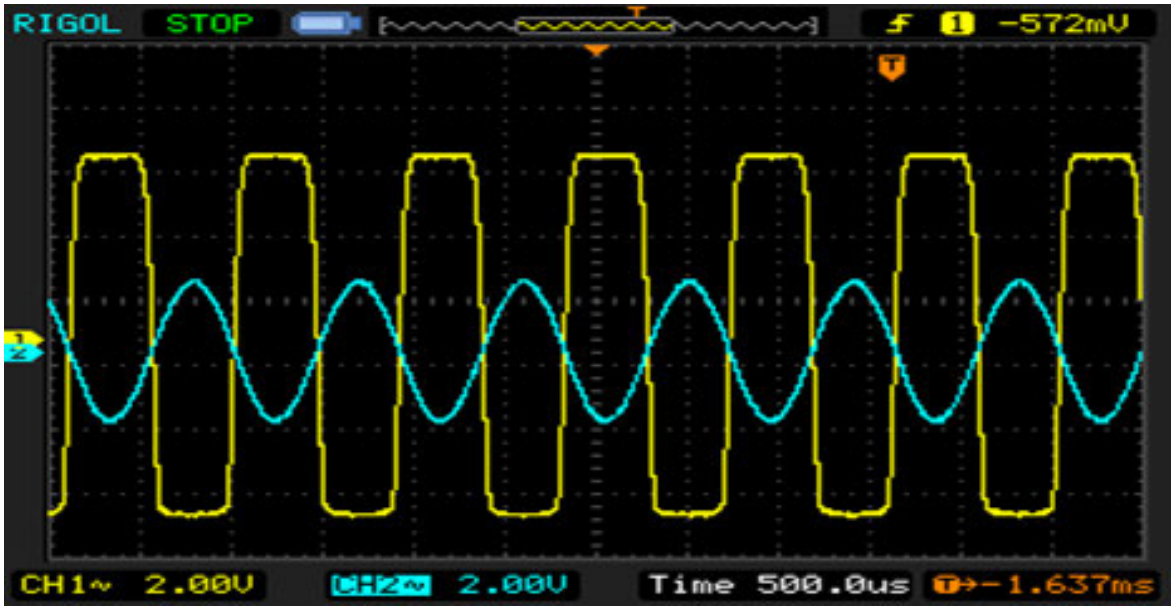


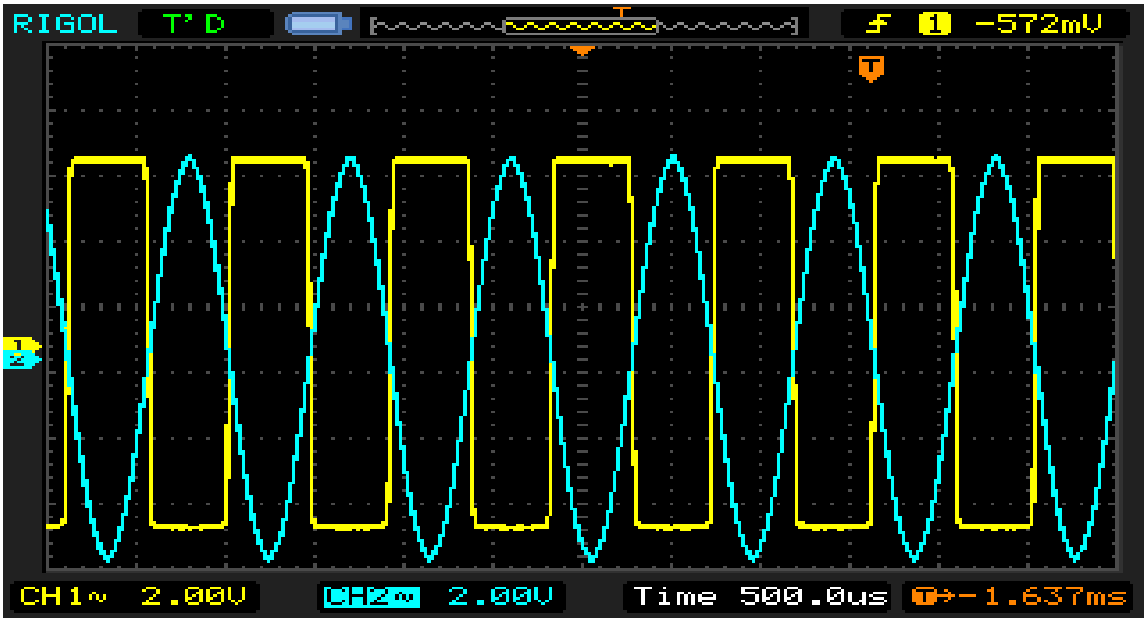
Figure 6.4 Single input – single output voltage signal.

Channel-1 is the output signal, channel-2 is the input signal, and the voltage per division for both channels is 2 V, the measured output signal. The single-ended output signal was measured to be *9.60* $V_{pk\text{-}pk}$. The gain can then be calculated as in Eq. (6.1):

$$A_V = \frac{9.6}{1.2} = 8.0(V/V) \tag{6.1}$$



(a)



(b)

Figure 6.5 (a) and (b) depict varied input signals vs. output signals.

It can be observed that when the amplitude of the input signal is increased, the output signal increases up to a point it is clipped off. This response we saw happening in the simulated design confirms that the simulated and fabricated design behaves almost the same. It can also be observed that as the amplitude of the input signal increases, the gain of the DA decreases. That could mean that the MOSFETs are no longer in the saturation region, which causes the electron mobility in the channel region to decrease, which then affects the performance.

Table 6.1 Single input-single output measured results by varying V_4 ($V_3 = 0\ V$ and $V_{G2} = 5\ V$)

$\mathbf{V_4}$ $(\mathbf{V_{pk-pk}})$	**Single Output Signal** $(\mathbf{V_{pk-pk}})$	**Gain (V/V)**
1.20	*9.60*	*8.00*
1.40	*8.02*	*5.72*
1.80	*7.06*	*3.92*
2.0	*4.02*	*2.02*

6.2 Single Input – Differential Output Mode

The prototyped design was also analysed, supplying a single input and then measuring the differential output signal. The purpose of this configuration was also to observe the response or behaviour when the output is measured differentially. The oscilloscope used had a feature to perform mathematical operations, such as getting the difference between two signals. Using the differential probe to measure the differential output would be better because the oscilloscope is not that accurate. Figure 6.6 depicts the measured differential output signal and has a voltage of *20* $V_{pk\text{-}pk}$; the DG is calculated as:

$$A_d = \frac{20}{1.2} = 16.67(V/V) \tag{6.2}$$

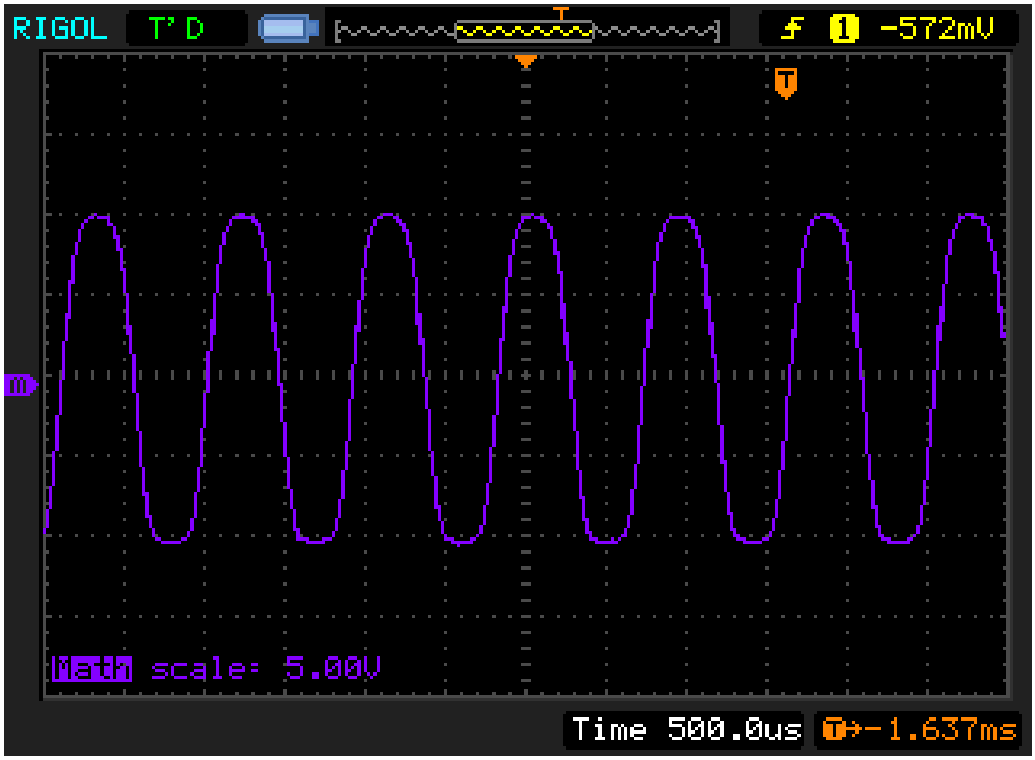


Figure 6.6 Measured differential output signal.

One may observe that when the amplitude of the input signal is varied between *1.20* and *2.0* $V_{pk\text{-}pk}$, the gain also changes, as depicted in Table 6.2. Amongst other reasons that may cause this variation is that the MOSFETs exit the saturation region causing a significant decrease in the ability to amplify. The use of VB also introduces the losses on the fabricated design because of the material used, which is copper. Moreover, these results show that the prototype design can amplify the difference between two input signals.

Table 6.2 Single input - differential output measured results by varying V_4 ($V_3 = 0$ *V* and $V_{G2} = 5$ *V*)

V_4 ($V_{pk\text{-}pk}$)	**Differential Output Signal ($V_{pk\text{-}pk}$)**	**Differential Gain (V/V)**
1.20	20.0	16.67
1.40	15.98	11.41
1.60	9.25	5.78
1.80	5.83	3.24

6.3 Common Mode Input Signal

The same signal was applied to both MOSFETs' gate terminals to measure the prototype design's capability to reject noise. One would expect to have zero output because the amplifier would just subtract those two signals because they are in phase. Figure 6.7 depict the measured output signal when a common mode input signal was applied.

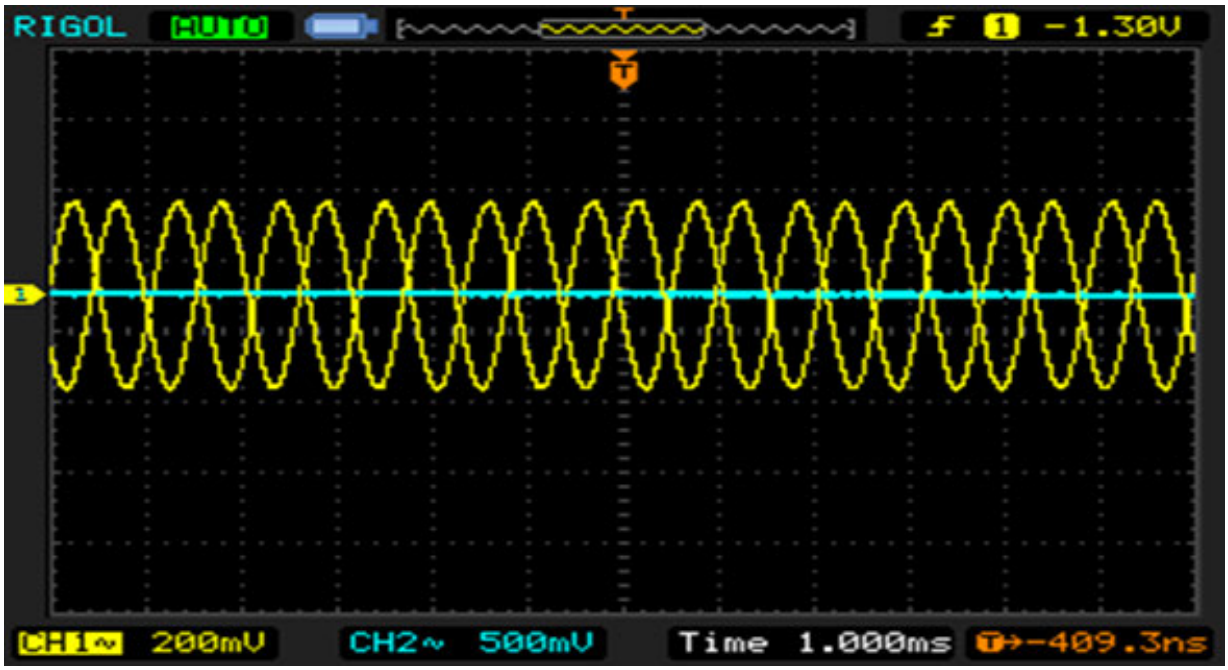


Figure 6.7 Measured output signal when common mode input signal was applied.

In Figure 6.7, channel 2 is the output signal, while channel 1 is the input signal. One would notice that the output signal is not zero exactly; there is some very small voltage. This is caused by the mismatch between resistors and MOSFETs. However, other than that, the measured results show that the prototype design can reject noise at any frequency. If we assume that the output signal has an amplitude of (*50 mV*), we can calculate *CMRR* for both single input – single output and single input – differential output. For single input – single output, *CMRR* is:

$$CMRR = \frac{8.0}{50 \times 10^{-3}} = 160(44.08dB)$$

And for single output and single input–differential output, *CMRR* is:

$$CMRR = \frac{16.67}{50 \times 10^{-3}} = 333.40(50.46dB)$$

Obviously, these values are not accurate, but they give insight into the capability of this circuit to reject noise.

6.4 Comparative Analysis

Tables 6.3 and 6.4 summarizes the comparative analysis of simulated and measured results for Single Input – Single Output (SI-SO) and Single Input – Differential Output (SI-DO) voltage signal at 1 kHz, respectively. It can be observed that measured results show a significant improvement compared to the simulated results on both SI-SO and SI-DO. These results prove that SCE and gate-leakage current has been reduced significantly, which resulted in better results. The difference in the measured values, especially common-mode gain and *CMRR*, is due to the loss and noise generated by the power supply and soldering of components using VB, which causes a mismatch.

Table 6.3 Comparative result for single input – single output signal

Parameters	**Simulated (dB)**	**Measured (dB)**	**Change**
Single-ended gain	16.62	18.62	+2.0
Common mode gain	-88.18	-87.33	-0.85
CMRR	90.85	100.50	+9.65

Table 6.4 Comparative result for single input – differential output signal

Parameters	**Simulated (dB)**	**Measured (dB)**	**Change**
Differential gain	22.35	24.44	+2.09
Common mode gain	-74.89	-73.81	-1.08
CMRR	96.54	98.29	9.20

In Table 6.5, a comparison between the proposed design and the already existing design is made. This comparison is very important because it highlights the importance of the proposed design and verifies the performance. One may observe that in terms of cut-off frequency and DG, it outperforms them. This means that the circuit can reject the common

signals between the two input signals. This leads to more accurate differential output. A wider bandwidth in the proposed design also enables the amplifier to operate effectively over a broader range of frequencies.

Table 6.5 Comparative analysis of the fabricated DA using DG MOSFET with existing models

Existing Designs	**Device**	**Differential Gain (dB)**	**Common Mode Gain (dB)**	**CMRR (dB)**	**Cut-off Frequency (MHz)**
[86]	BJT	-	-	-	161.1 to 186.7
[84]	SG-MOSFET	46.22	-	124.397	3.94
[85]	DG-MOSFET	6.02	-	33.96	1
[29]	DG-MOSFET	20	27.96	20	34
This work	DG-MOSFET	24.44	73.81	98.29	65

6.5 Chapter Conclusion

The proposed solution has been analysed using various parameters to observe the circuit's behaviour and performance. The amplifier was then fabricated using the available material, such as Vero-board, capacitors, and resistors, to verify the same parameters analysed in the simulation. After testing, it is observed that the prototyped design behaves almost the same way as the simulated design, but there are variations. These variations in results were expected because, in real life, it is always difficult to have matched transistors and resistors. Eventually, this introduces losses on the circuit, which then affect the ability of the amplifier to amplify. However, all in all, the measured results showed that the prototyped design is working and outperforms the already existing designs, which is demonstrated in Table 6.5.

Chapter-7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusion

In this research work, a DG-based differential amplifier has been designed by taking advantage of the DG MOSFET's unique features and benefits. The DG MOSFET has a number of benefits over conventional SG MOSFETs, including low power consumption, greater SCE control, and lower leakage current. It is a desirable option for developing high-performance differential amplifiers because of these qualities. Moreover, a DG MOSFET can be operated in asymmetrical where each gate is supplied with a signal independently, and in symmetrical mode, where both gates are supplied with the same signal.

A differential amplifier is a device that amplifies the difference between two input signals while rejecting common signals. It is also a primary building block in integrated circuits and is normally used in applications that involve communication systems, electrical circuits, and medical technologies.

In designing this differential amplifier, a full consideration of the project's functional specifications has been taken, including a constant current source of *8 mA* and a supply voltage of ± *12V*. A biasing circuit was also considered because for a MOSFET to act as an amplifier, it must operate in the saturation region, so the available data-sheet for BF998 DG MOSFET was analysed in order to saturate the MOSFETs. A differential amplifier has only one circuit topology, which has two matched transistors whose source terminals are connected together, which are then connected to a constant current source in a negative voltage source. Their drain terminals are connected to a positive voltage source via the resistors. In this work, this topology was used, which is normally called resistive-loaded differential amplifier, and the MOSFETs were operated in asymmetrical mode. The circuit's current source was designed using a resistor and a voltage source. Lastly, the circuit was then fabricated on a Vero board.

The performance evaluation of the differential amplifier revealed its effectiveness. Various parameters were analysed in different circuit configurations to observe the designed amplifier's performance. Differential gain, common mode gain, CMRR, and frequency are parameters that were analysed. Based on the simulated results, the designed amplifier

outperformed the existing designs, as demonstrated by a comparative analysis in chapters 4 and 5. The designed differential amplifier was then fabricated in a Vero-board to further analyse the performance and efficiency. A comparative analysis between simulated and measured results has been done in Chapter 6, and the results show that the simulated and prototyped design behaves the same way. It can be observed that the single-ended output gain of the implemented compare to the simulated has improved by *10.7%*, the common-mode gain has reduced by *0.96%*, and the *CMRR* has improved by *9.60%*. For the single-input and differential output gain of the implemented compare to the simulated has improved by *8.55%*, the common-mode gain has reduced by *1.46%*, and the *CMRR* has improved by *9.36%*.

Despite the success of this design, there were various challenges, especially with the prototype design, because the measuring instruments were not available, such as a signal generator that could generate two signals that were 180 out of phase. We tried to design a phase shifter using basic components such as resistors and capacitors; the output signal's amplitude and quality were very bad. This prevented me from evaluating the performance of the differential input-differential output signal.

In conclusion, the designed DG-based differential amplifier exhibited high gain, low noise, wide bandwidth, reduced SCE, and leakage current. This makes it more suitable for various applications such as audio amplification, communication systems, and medical equipment. The upcoming section will discuss the work that could be done to improve the performance of this work further.

7.2 Future Work

Given that the design of this differential amplifier was successful, there is still room for improvement. To improve its effectiveness, additional study and optimization might be conducted. Several possible improvement directions include using current mirrors that use active devices such as BJTs and MOSFET. This is because they possess less resistance than a current source with a resistor. The availability of more advanced instruments, such as oscilloscopes and signal generators, could go a long way in the design and performance evaluation.

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