# DESIGN AND PERFORMANCE ANALYSIS OF CLASS-B POWER AMPLIFIER WITH DOUBLE-GATE MOSFET

*Thesis submitted for the fulfilment of requirements for the degree of*

## *MASTER OF SCIENCE*

in

## *Electronic Engineering*

by

**SANDILE HANDSUM MBONANE**


**DEPARTMENT OF ELECTRONIC ENGINEERING, HOWARD COLLEGE,**

**UNIVERSITY OF KWAZULU-NATAL, DURBAN - 4041 SOUTH AFRICA.**

**STUDENT NO.: 217021191** **10 MARCH 2023**

# DESIGN AND PERFORMANCE ANALYSIS OF CLASS-B POWER AMPLIFIER WITH DOUBLE-GATE MOSFET

*Student:*

Sandile Handsum Mbonane

*Supervisor:*

Prof. (Dr.) Viranjay M. Srivastava

*This thesis submitted in fulfillment of the requirements*

*for the degree of Masters of Science: Electronic Engineering*

*in*

*Howard College of Agriculture, Engineering & Science*

*University of KwaZulu-Natal, Durban*

*South Africa.*

As the candidate's supervisor, I have approved this thesis for submission.

Signed……..... Date: 10 MARCH 2023

Name: Prof. (Dr.) Viranjay M. Srivastava

# Declaration 1 - Plagiarism

I, **Sandile H. Mbonane,** with Student Number **217021191** and the thesis entitled " Design and Analysis of Class-B Power Amplifier using Double-Gate MOSFET" hereby declare that:

(i) The research reported in this thesis, except where otherwise indicated, is my original research work.

(ii) This thesis has not been submitted for any degree or examination at any other university.

(iii) This thesis does not contain other person's data, pictures, graphs, or other information unless specifically acknowledged as being sourced from other persons.

(iv) This thesis does not contain other person's writing unless specifically acknowledged as being sourced from other researchers. Where other written sources have been quoted, then:

a. Their words have been re-written but the general information attributed to them has been referenced;

b. Where their exact words have been used, then their writing has been placed inside quotation marks and referenced.

(v) Where I have reproduced a publication of which I am an author, co-author, or editor, I have indicated in detail which part of the publication was written by myself alone and have fully referenced such publications.

(vi) This thesis does not contain text, graphics or tables copied and pasted from the Internet, unless specifically acknowledged, and the source being detailed in the thesis and in the references sections.

Signed……. Date: 10 Mar 2023

(Sandile H. Mbonane)

# Declaration 2 – Publications

Details of contribution to publications that form part of the research presented in this thesis include publications in preparation, already submitted, in press and published. They give details of the contributions of each author to the experimental work, simulation and writing of each publication.

## List of Publications

1. **Sandile H. Mbonane** and Viranjay M. Srivastava, "Class-B power amplifier with double-gate MOSFET: A circuit perspective," *Key Engineering Material (KEM),* vol. 907, pp. 50-56, Jan. 2022.

   **(ISSN: 1662-9795)** ***[SCOPUS, DoHET]***

2. **Sandile H. Mbonane** and Viranjay M. Srivastava, "Comparative parametric analysis of class-B power amplifier using BJT, single-gate MOSFET, and double-gate MOSFET," *Material Science Forum (MSF),* vol. 1053, pp. 137-142, Feb. 2022.

   **(ISSN: 0255-5476)** ***[SCOPUS, DoHET]***

Signed……. Date: 10 March2023

(Sandile H. Mbonane)

# ACKNOWLADGMENTS

Firstly, I give all glory and honour to the Almighty God for His infinite mercy, grace and strength I acquired to complete this research work. My sincere appreciation goes to my beloved parents, Velaphi J. Mbonane, and Zandile V Mbonane for their kindness, patience, support, understanding and encouragement all these years, they are indeed God sent. Thank you for your contribution towards my achievements. I also appreciate my Siblings Mbalenhle, Ntokozo, Slindokuhle, Mabutho, Thembelihle, Mpendulo, Banele Mbonane and my nephews Minenhle Thwala and Amahle Mbonane

I would like to express my appreciation to my girlfriend, Mbalenhle Patience Vilakazi for her encouragements, support and sacrifices all through the duration of my master's degree program.

My sincere appreciation goes to my supervisor Prof. (Dr.) Viranjay M. Srivastava for his patience, guidance, support, advice, time, and enthusiasm to undertake this research which has aided my thorough understanding of the study and the great flexibility and freedom he granted me in realizing the research objectives.

## Dedication

*This thesis is dedicated to my brother, Mabutho Mbonane*
*and the entire Mbonane family.*

*To God be the Glory.*

# ABSTRACT

This work presents the design of a class-B power amplifier with the use of Double-Gate (DG) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). It analyzes the indices of system performance indices for class-B power amplifiers using DG MOSFET. It presents a comparative analysis of three power amplifiers using different switching devices, i.e., BJT, traditional single-gate MOSFET, and designed amplifier using DG MOSFET.

It was realized that the class-B power amplifier with the use of DG MOSFET reduces the crossover distortion which is a major issue faced by class-B power amplifiers. The hardware design is also presented and tested with advanced electronic components such as oscilloscope, function generator, and DC power supply, it was observed that the crossover distortions are not exist in the output waveforms of the hardware circuit design. The class-B power amplifier is commonly used for power amplification due to its performance, such as high input signal fidelity at the output and high-power efficiency. These power amplifiers are being designed and simulated to test the switching speed to receive the output signal when an input signal is applied. The comparison of these three power amplifier circuits is taken to conclude which power amplifier circuit performs better regarding its switching speed. The basics switching speed is the time the power takes to amplify the signal, which is the same as the time to amplify the signal to a specific gain. In addition, the settling time for these three types of power amplifiers also have been tested and presented to justify the performance of these three types of power amplifiers.

Losses of the class-B power amplifier using DG MOSFET are presented and compared to the design of class-B power amplifier using traditional single-gate MOSFET. This thesis describes the design of a power amplifier having DG MOSFET, which is a device used to amplify any input signal; it can be an audio signal or any signal. The thesis provides information on the problem identification/description, design objectives/requirements, and the design specifications, both functional and non-functional, together with design constraints and simulation circuits. Various solutions to the problem are discussed and the preferred solution is proposed, together with analysis.

# TABLE OF CONTENTS

# LIST OF FIGURES

# List of Tables

# LIST OF ABBREVIATIONS

| | |
|---|---|
| 1D | One Dimensional |
| 2D | Two Dimensional |
| AC | Alternative Current |
| BJT | Bipolar Junction Transistor |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DC | Direct Current |
| DG | Double-Gate |
| EHF | Extremely High Frequency |
| ELF | Extremely Low Frequency |
| FinFET | Fin Field-Effect Transistor |
| IC | Integrated Circuit |
| ITRS | International Technology and Roadmap for Semiconductors |
| MEMS | Microelectromechanical System |
| MOS | Metal-Oxide Semiconductor |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| RF | Radio Frequency |
| SCEs | Short Channel Effects |
| SOI | Silicon-On-Insulator |
| VLSI | Very Large-Scale Integration |

# LIST OF SYMBOLS

| | |
|---|---|
| G | Gate |
| D | Drain |
| S | Source |
| $I_d$ | Drain Current |
| L | Channel length |
| W | Channel width |
| H | Channel height |
| $\phi_{MS}$ | Work Function |
| $Q_c$ | Surface charge |
| $n_i$ | Intrinsic carrier concentration |
| $N_a$ | Doping concentration |
| $V_T$ | Thermal voltage |
| $V_{th}$ | Threshold voltage |
| $V_{GS}$ | Gate-source voltage |
| $V_{DS}$ | Drain-source voltage |
| $V_{bi}$ | Built in Voltage |
| $V_{bs}$ | Substrate bias voltage |
| $I_{on}$ | Current-ON |
| $R_{on}$ | On-resistance |
| $C_{ox}$ | Oxide capacitance |
| $C_{si}$ | Silicon capacitance |
| $E_g$ | Band gap energy |
| $\psi_s$ | Surface Potential |
| $\psi_{ox}$ | Oxide potential |
| k | Boltzmann Constant |
| T | Temperature |
| $\varepsilon_{ox}$ | Permittivity of the oxide |
| $\varepsilon_{si}$ | Permittivity of the Silicon |
| $t_{ox}$ | Oxide thickness |

| | |
|---|---|
| $t_{si}$ | Silicon thickness |
| q | Electronic charge |
| μ | Carrier Mobility |

# Chapter-1

# INTRODUCTION

## 1.1 Background

Power amplification is one of the significant aspects of industrial application because of its performance to amplify high-noise signals to low-noise signals while amplifying the power and reducing crossover distortions [1]. A Power Amplifier (PA) is an electronic device; its output signal power (delivered to the load) is more significant than that of an input signal power (it takes from the driver stage) [2, 3]. Due to the change of networks from 4G to 5G, power amplifiers in 5G wireless applications will vary from other networks. The 5G wireless revolution brings drastic Radio-Frequency (RF) design changes and power amplifiers for radio base stations or handsets. Besides the emergence of 5G, the renewed interest in power amplifier technology was stimulated by technical challenges and modern digital communication systems [4, 5]. The broadband modulation for 5G transmissions requires stringent linearity and high-power efficiency from the power amplifiers compared to other networks; hence, there is a need to design more superior power amplifiers. Centimeter-wave 5G systems are likely to arrive in the market; it is their mm-Wave counterpart will challenge the RF design norms [6]. Hence Multiple-Input Multiple-Output (MIMO) antennas serving various devices in the densely deployed environment will need a power amplifier with high-power efficiency and stringent linearity [7, 8].

An appropriate characterizing definition of a power amplifier is that its output signal power conveyed to a load is more significant than the source signal power it absorbs from the driver stage of any device. Here in this research work, the main emphasis is concentrating on the class-B amplifier. The most common audio characteristics, such as load regulation and output power, are the requirements for designing a power amplifier. Various parameters affect power amplification in power amplifiers, power supplies, and power conversion circuits. These may vary based on the circuit design, which may cause various power losses [9, 10]. Class-B power amplifier performance has been analyzed by an active device (i.e., MOSFET and DG MOSFET), when it is closed and by the transient response of the load network when the switching devices are opened.

An ideal design also needs the slope of the drain voltage immediately when the device switches-ON is zero; this results in a device with zero current when it is turned ON. The efficiency of an ideal class-B power amplifier (i.e., one with immediate switching, zero saturation voltage and circuit resistance, and so forth) will be 100 % if the circuit components are picked to make the drain voltage arrive at zero at the moment the semiconductor turns-ON. Bipolar semiconductors are distinguished by a fixed Gate-to-Source voltage ($V_{sat}$) during the saturation. The little changes of this voltage with changes of the drain current can be represented by using $R_{on}$ in addition to saturation voltage [11, 12]; a fixed saturation voltage reduces the drain voltage downward swing to a powerful voltage. This thesis expands the work of using DG MOSFET in designing a class-B power amplifier with the comparisons with the use of SG MOSFET in switching time and power losses with its power gain and amplification,

Present-day fast power amplifiers (such as class A, B, AB) are designed with ‘settling time’ in the scope of nanoseconds. This settling time is brief to the point that estimating it inside a sensible error band presents a difficult task on automatic test equipment yet in addition on the bench [13, 14]. Transient investigation determines a circuit's reaction throughout some period of time characterized by the user. The accuracy of the transient inquiry is subject to the size of inner time steps, which together make up the total simulation time known as the *run time* or *stop time*. Class-B power amplifier transient analysis can be determined in several ways; for this research work, one main type of transient analysis that is determined is settling time. In the control hypothesis, the settling time of a dynamical system, for example, a power amplifier or other yield device, is the time slipped by from the use of an ideal instantaneous step input to the time at which the power amplifier output has entered and stayed inside a predefined error band. The settling execution of a class-B power amplifier is regularly calculated using small-signal models with fixed parameter values. Various parameters have to be considered in determining the transient analysis of class-B power amplifiers, which may affect the transient response of the class-B power amplifier [15, 16]. These parameters include internal resistances of the switching devices used to design a class-B power amplifier; these switching devices are BJT for the type of class-B power amplifier, SG MOSFET, and DG MOSFET for that type of power amplifier fabrication.

The high volumes of production of consumer wireless mobile devices have created a large market for high-quality, low-cost power amplifiers [17]. The most common audio

characteristics, such as load regulation and output power, are the requirements for designing a power amplifier. Generally, Single-Gate (SG) MOSFET has been used for large-scale amplifiers such as an audio amplifier, but to make it novel, the Si-based Double-Gate MOSFET has become a potential replacement [18, 19]. Common types of amplifiers, such as class-A, class-B, class-C, class-E, class-AB, etc., are used in signal amplification, but for this research work, Class-B power amplifier is being designed and analyzed.

## 1.2 Problem Statement

Besides the emergence of 5G, the renewed interest in power amplifier technology was stimulated by the technical challenges and the economics of modern digital communication systems. From this point forward, amplifiers of electrical signs have played a critical capacity in electronic frameworks. Most electronic devices, such as the radio, television, or telephone, would not work properly without Power Amplifiers (PA) capability.

Due to the change of networks from 4G to 5G, power amplifiers in 5G wireless applications are changing from other networks [20-22]. The basic reason it is going to change is that the broadband modulation for 5G transmissions requires stringent linearity and high-power efficiency from the amplifiers compared to other networks; hence, there is a need for the design of superior power amplifiers to be able to maintain the requirements of changed 5G networks since 5G network is daily improving due to the implementations of Artificial Intelligence. Therefore, a change in power amplifiers for such an improved 5G network needs to be also improved. The main problem faced by power amplifiers is that when an input signal (i.e. sinusoidal input) is applied to the amplifier, at the output stage, there are some losses and some signal shape infidelity which is caused by components used in designing such circuits such as different switching devices and other components which might affect the power gain and also the shape of the input signal.

The other problem faced by power amplifiers is that it takes some time to get the output signal when an input signal is introduced to an input stage of the circuit; such issues cause the power amplifier to have less amplification speed [23]. Amplification time or speed in determining the performance of a power amplifier is caused by the switching

device used. Hence different switching devices cause a power amplifier to have other performances and different amplification parameters.

With this problem at hand, there is a need to develop a better structure of class-B amplifiers. With this motivation, this work considers how to bring about stability in the output of an amplifier using various parameters and comparing them for better performance with its trending evolution shown in Figure 1.1. The set objectives for achieving this are listed in the following Sections.

## 1.3 Research Objectives

The objective of this research work is to:

- **A.** Design and implement the most suitable solution for a low-cost power amplifier with a DG MOSFET [24-27] based class-B amplifier,
- **B.** With the ability to amplify the input signal power,
- **C.** To make an analysis about the improvement of using the DG MOSFET instead of using Single-Gate (SG) MOSFET or any other type of switching device.
- **D.** The main focus of analysis is to test and analyze the power amplifier's transient or amplification speed or time using DG MOSFET,
- **E.** Comparison of results with other types of switching devices such as BJTs and SG MOSFET.

## 1.4 Significance of Research Work

This research work evaluates the technical improvement of class-b power amplifier design in terms of various parameters such as power efficiency, settling time, power losses, and reduction of crossover distortion. The input signal will be amplified using a class-B amplifier, and the output signal should be larger than the input signal. Due to the existence of various power amplifiers, it is possible that class-B power amplifiers can be designed and implemented with the use of DG MOSFET.

The existing power amplifiers have an issue with signal infidelity. Using DG MOSFET is one of the solution devices used to solve these technical issues while improving or maintaining the standard of power amplifiers, which always produces low

noise signals that may affect the ambient devices. However, DG MOSFET does not eradicate all of the problems of Class-B Power Amplifier, which are crossover distortions output waveforms, but it aims at reducing such issues but using the performance of DG MOSFET in switching transient.

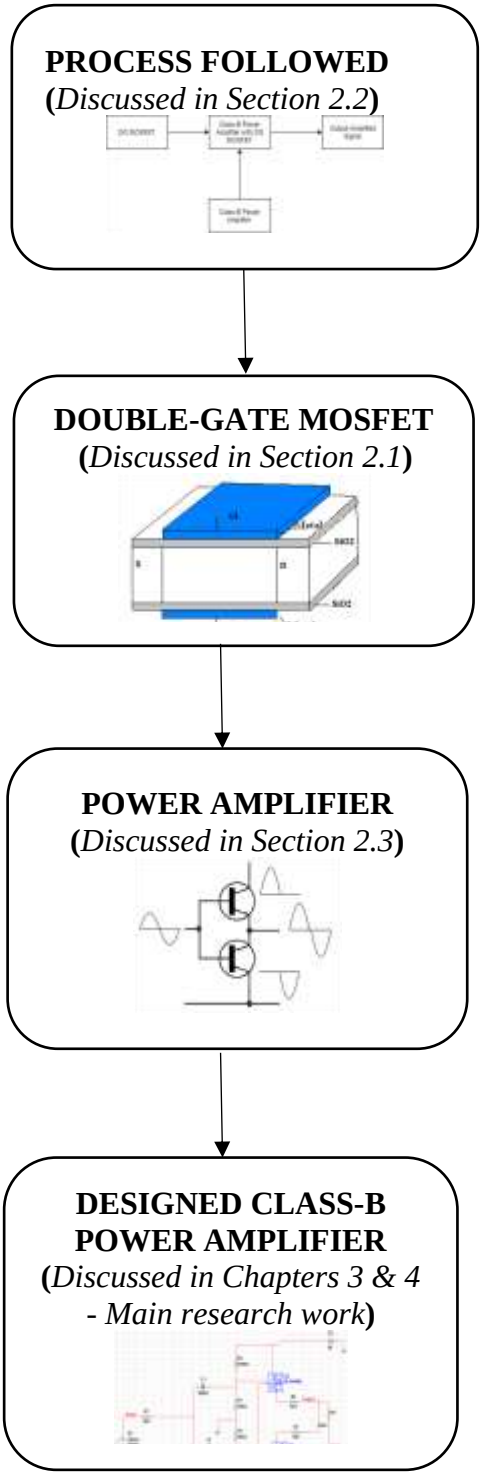


Figure 1.1 Flowchart of working strategies for this thesis work.

## 1.5 Methodological Approach

The class-B power amplifier has three subsystems; each performs a specific task. These three subsystems involve the input stage, driver stage, and output stage [28]:

- Input stage - The signal is applied,
- Driver stage - Input signal property such as voltage is used to control or switch on the switching devices or DG MOSFET, and
- Output stage - Output signal is analyzed.

The design approach is based on different stages, including mathematical analysis, the first stage of design methodology for each stage of Class-B power amplifier, followed by simulations where output characteristics of the mathematical design are being analyzed.

## 1.6 Thesis Organization

This research work has been divided into six chapters and each of these chapters is summarized as:

**Chapter one** explains the background of power amplifiers, the objective of the thesis, the thesis organization, together with problem statement where the main problem of the class-B power amplifier is explained.

**Chapter two** gives a detailed introduction to power amplifiers, including the history of power amplifiers, it has a detailed explanation of DG MOSFET and its operation, where the different DG MOSFET is explained with their advantages and disadvantages.

**Chapter three** presents a mathematical analysis and design of a class-B power amplifier where the design algorithm is explained fully with all the use of efficiency used to deliver the performance of class-B power amplifier with the use of DG MOSFET.

**Chapter four** has the analysis of class-B power amplifiers with the use of DG MOSFET, this analysis includes transient analysis and all non-ideal effects that affect the performance of class-B power amplifiers.

**Chapter five** presents the circuit losses of class-b power amplifiers where different losses are taken into consideration, i.e., conduction losses and switching losses.

**Chapter six** is the hardware design and results of the class-B power amplifier. The results of simulations are compared to the hardware results and also shows the detailed design steps used to implement the hardware circuit.

Finally, in **chapter seven**, the summary of the research work is presented. The conclusion and possible work that can be implemented in the future as regards the structure is also listed and suggested.

## 1.7 List of Publications

1. **Sandile H. Mbonane** and Viranjay M. Srivastava, "Class-B power amplifier with double-gate MOSFET: A circuit perspective," *Key Engineering Material (KEM)*, vol. 907, pp. 50-56, Jan. 2022.

   **(ISSN: 1662-9795)** ***[SCOPUS]***

2. **Sandile H. Mbonane** and Viranjay M. Srivastava, "Comparative parametric analysis of class-B power amplifier using BJT, single-gate MOSFET, and double-gate MOSFET," *Material Science Forum (MSF)*, vol. 1053, pp. 137-142, Feb. 2022.

   **(ISSN: 0255-5476)** ***[SCOPUS]***

## 1.8 Conclusion

It was discussed that power amplifier significantly impacts new technology applications, which may vary, such as 5G networks and other new technical innovations. These networks require enough power to function well due to the tasks that they are designed to do. Class-B power amplifier aims to meet the required power for 5G networks to perform properly.

## Chapter-2

# LITERATURE REVIEW

In early 1936, *Doherty* invented his unique amplifier approach [29]. This gadget, which incredibly improves the effectiveness of RF power intensifiers, was first utilized in a 500-kW transmitter that the Western Company intended for a radio broadcast in Louisville, Kentucky. Western Electric proceeded to consolidate Doherty power amplifiers into the event, 35 business radio broadcasts worldwide by 1940 and into numerous different stations, especially in Europe and the Middle East, during the 1950s [30, 31]. The Doherty power amplifier is an adjusted class-B RF power amplifier. In Doherty's day, inside the Western Electric product offering, this namesake electronic gadget worked as a direct power amplifier with a balanced driver. In the 50-kW execution, the driver was a finished 5 kW transmitter that could, if essential, be worked autonomously of the Doherty power amplifier, the Doherty power amplifier was utilized to raise the 5 kW level to the necessary 50 kW level [32].

The power amplifier was typically designed as a grounded cathode, transporter top intensifier utilizing two vacuum tubes in equal association, one as class-B transporter tube and the other as class-B top cylinder (i.e., power semiconductors). The cylinders' source (driver) and burden (reception apparatus) were part and consolidated through ± 90° stage moving organizations [33, 34]. Alternate configurations included a grounded-grid carrier tube and a grounded-cathode peak tube, whereby the driver power was effectively passed through the carrier tube and was added to the resulting output power—but this benefit was more appropriate for the earlier and less efficient triode implementations rather than the later and more efficient tetrode implementations.

Power amplification of electrical signals has played a key function in electronic systems ever since, enabled by *Lee de Forest's* invention of the vacuum tube triode in 1906 [35]. Given a particularly wide application space, it isn't surprising that electrical architects have immediately worked out the subtleties of planning great force intensifiers, first with vacuum tubes and afterward with discrete semiconductors. Common amplifiers, such as class-A, class-B, class-C, class-E, class-F, class-G, class-AB, etc. are used in signal amplification [36]. For the aim of this thesis or research work, class B amplifier becomes favored over class-A and class-AB. The class-AB amplifiers are not favored because of

the step alternate in loop gain that takes place as the amplifier output movements from class-A to class-B.

## 2.1 DG MOSFET and its operation

The Double-Gate (DG) MOSFET is an extended version of MOSFET that operates slightly different from the other MOSFET, and its structure is also different from the other MOSFET [37-40]. Starting from its structure, as shown in Figure 1, the gates are connected in series, and either one can operate independently to control the FET's operation. If the gate length is reduced, higher cut-off frequencies are Acquired. The transistor's switching activity degrades whenever the drain and source take over the electrostatic control of the channel by the gate. MOSFET has a gate electrode which is called Gate, this gate electrode is electrically insulated from the semiconductor P/N channel. They are insulated by a thin insulating layer which is silicon dioxide. The insulated metal oxide gate electrode act as one plate of a capacitor, the controlling gate, which is insulated from the main semiconductor P/N channel forms a high input resistance which is extremely high up to Mega Ohms, which makes it infinite. The gate terminal is electrically insulated from the semiconductor channel between the source and the drain; hence no current will flow into the gate or current from the drain to the source since the gate is insulated from the main current-carrying channel. This makes MOSFET act as a voltage controlled, which means the current flowing through the channel is directly proportional to the input voltage supplied to the MOSFET gate [41]. Adding another gate to the MOSFET with the same drain, body, and source imposes additional adjusting or control over the channel and puts back the gate control.

The total gain current increases because of a structure that is equivalent to two transistors mounted back-to-back. There is some capacitance between the gates, resulting in mutual coupling, but it is rarely important until higher frequencies of about 400 MHz - 500 MHz are considered. Most of the dual-gate MOSFETs operate in a depletion mode and are different from what one might expect after having been used to simple junction type FET's. In general, most of the DG MOSFETs circuits are arranged so that the gate closest to the drain is fixed biased and the gate closest to the source is used for an input signal.

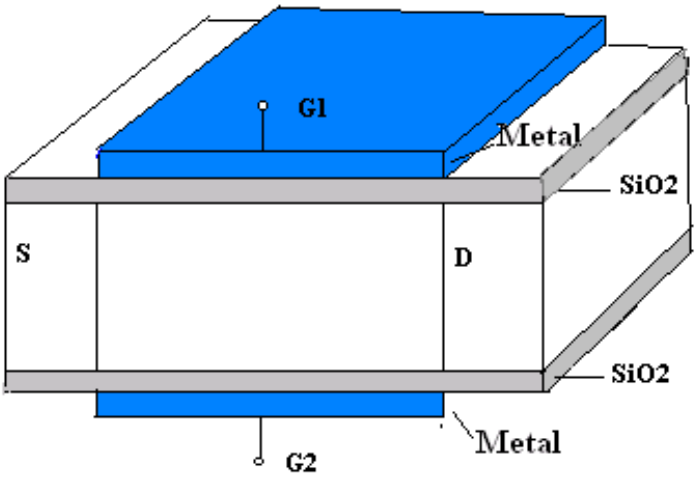


Fig. 2.1. Schematic of the DG MOSFET, where D: Drain, S: Source, G2 and G1: Gate-2 and Gate-1SiO2 [38].

The use of MOSFET is becoming an essential device in electronic applications, such as a requirement of switching circuitry [39, 40]. The DG MOSFET does not solve all the transistor problems, but its list of advantages such as low power dissipation when it is operating at saturation region help increase the efficiency of class-B power amplifier. There are two types of MOSFETs with different structures, different switching transients, and voltage drops when used as a switch. The following section describes the advantages of DG MOSFET over Single-Gate (SG) MOSFET w.r.t. amplifier application.

## 2.2 Class-B Power Amplifier Design steps with DG MOSFET (Block Diagram)

Figure 2.2 shows a block diagram of Class-B power amplifier with the use of DG MOSFET. The class-B power amplifier is implemented with DG MOSFET, where it is combined with a class-b power amplifier and used to amplify an input signal or drive a load.

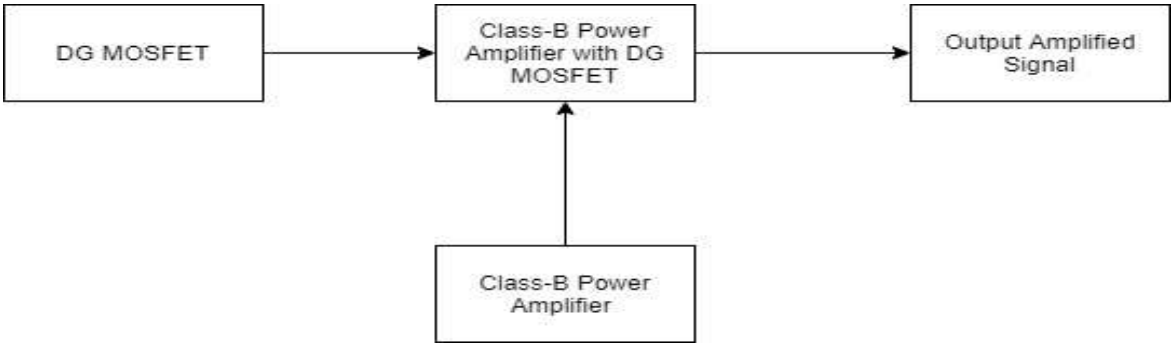


Fig. 2.2. Class-B power amplifier block diagram.

### 2.2.1 Advantages of DG MOSFET

The advantages of DG MOSFETs are switching transient $I_{on}/I_{off}$, low noise, better power gain, excellent dynamic range, low feedback capacitance, each gate has a lower leakage. In double-gate MOSFET as the name says, two gate terminals are used, the second terminal is used to reduce and control the feedback capacitance between input and output; hence the power amplifier becomes more stable. The gate oxide between the gate and the channel is an insulator layer and the metal used for the gate is a good conductor and the channel is also a good conductor, hence all these three layers together form a capacitor. This is like two capacitors in series and the total capacitor in a series is less than an individual capacitance. Using the following inductive reactance equation:

$$X_C = \frac{1}{2\pi f C}$$

where $f$ is the frequency of an input signal and $C$ is the capacitance. In DG MOSFET structure which forms two capacitances connected in series, the total capacitance in DG MOSFET is less than that of SG MOSFET, using the above equation capacitance decreases, the total reactance increases. Using ohms law which states that total resistance is equal to the voltage across the resistance divided by total current flowing through the resistance, this means that as the reactance increases, the total current through the resistance or device decreases. Therefore, DG MOSFET has lower current leakage across it due to the internal capacitances connected in series. It offers better scalability because it reduces Short-Channel Effects (SCE) and offers better control of channels from the gates. It also provides a better electrostatic over the channel [42, 43].

The electrostatic of the DG MOSFET can be portioned into two general classifications: symmetrical and asymmetrical. The symmetrical DG MOSFET has a similar gate bias and consequently switch-ON simultaneously. The asymmetrical DG MOSFET can have different work functions and biasing circuits. For this design, authors have considered the symmetric type, as the asymmetric type is very sensitive to the Silicon body, which influences the threshold voltage, thus impacting SCEs. The n-channel DG MOSFET (BF998, Fig. 3) has been used in this design [44].

Fig. 2.3. Used MOSFET in this thesis work (BF998) [44].

Figure 2.3 shows a DG MOSFET that has two entryways, for example, a front entryway or front gate and a back entryway or back gate. The terminals, i.e., gate terminals, control an electric field that decides the measure of flow through the channel; the channel flow is reliant on the Silicon thickness [4]. It tends to be scaled to the most limited conceivable length for a given oxide thickness and is more electrostatically hearty than the prior detailed MOSFETs because of the double door protecting and the diminished short channel impacts.

### 2.2.2 Symmetric and Asymmetric

In this type of DG MOSFET, both gates have identical work-functions where both the surface's channels turn-ON simultaneously [44-46].

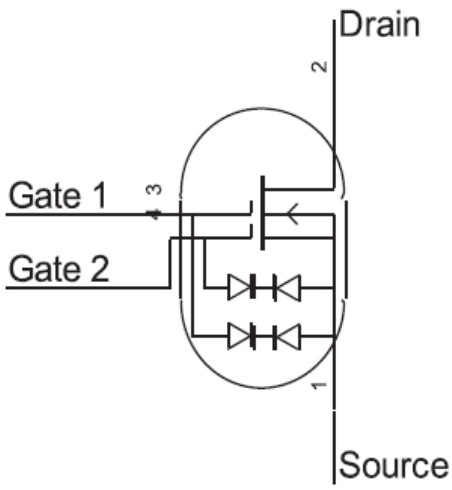


Fig. 2.4. Asymmetric (Independent) driven DG MOSFET.

At the point when (G_1) and (G_2) are turned on with a similar gate voltage for example combined. The activity method is considered to be asymmetric as appeared in Figure 2.4.

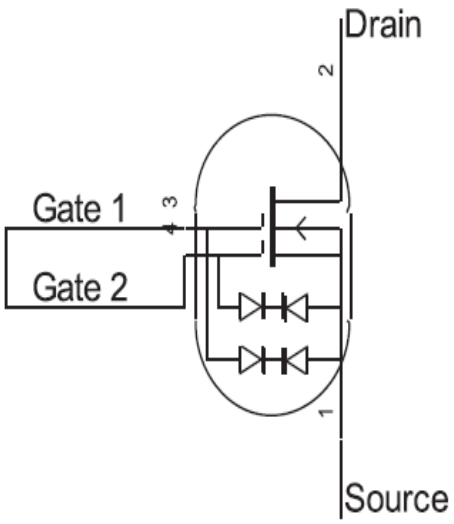


Fig. 2.5. Symmetric DG MOSFET.

It shows the dependent-driven DG MOSFET, in which gate-1 ($G_1$) and gate-2 () ($G_2$) do not have the same or common gate voltage. The main advantage of using DG MOSFET over other switching conductors is that its size is scaled in dimension, which

makes it more advantageous in power losses and because of that, the efficiency of power amplification is improved. When switching devices are used in power amplification, devices that are used must have low power dissipation through it when the system is fully functioning to improve the efficiency of the system; hence for class-B power amplifier, DG MOSFET makes it has low power dissipation through it because of the scaled size structure of DG MOSFET.

## 2.3 Design Solution of Class-B Power Amplifier

Class-B amplifier supplies an output signal changing over each half-cycle of the input signal [47]. Hence the biasing of dc voltage is zero volt. The power dissipation of this type of amplifier is zero at the quiescent condition (i.e. when no-load and input signal are connected to the amplifier) [48]. There is no power dissipation because the collector current is zero when there is no load or input signal. The circuit is forward biased when the positive half-cycle of the input signal is applied, and it is reversed biased when the input signal is negative; hence there will be no collector or drain current. In that case, only the positive input signal will be amplified. As a result, the negative half-cycle will be absent, as shown in Figure 2.6. This also results in more power dissipation if the input increases.

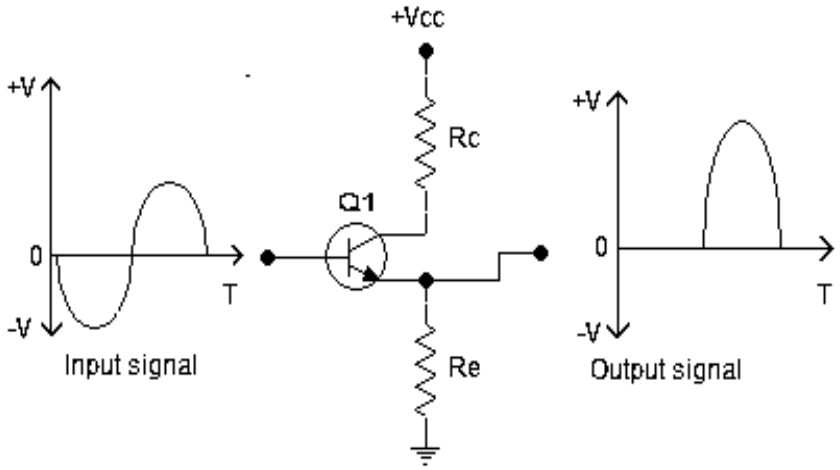


Fig. 2.6. Class-B amplifier common collector [49].

The class-B power amplifier is different from the other power amplifier classes (i.e., class-A, class-AB, class-C, etc.) in a way that each transistor will not conduct if there is no input signal applied to the input of the power amplifier [49]. Only half of the input signal will be amplified when the sinusoidal input signal is applied. This is because the operating point is selected to be at the collector in case BJTs are used and in the drain when MOSFETs are used. In this thesis work MOSFET has been used.

The common disadvantage of the class-B amplifier is that it has higher crossover distortion as a result that DG MOSFET will be used to minimize the crossover distortion in this work. Although the efficiency of class-B power amplifier is higher than class-A, as just a one-half cycle of the signal is utilized, the crossover distortion is high. Additionally, the input power is not used. The push-pull arrangement is presented in a class-B amplifier to solve these issues in this thesis work.

A two-semiconductor setup is important to get an adequately decent proliferation of the input signal waveform. This setup is known as a complementary-symmetry or push-pull amplifier (push-pull amplifier). The word push-pull comes from the way that two semiconductors in class-B amplifiers conduct an exchanging half-cycle of the input signal. The joined half-cycle at the output then created an output signal for a full $360^{o}$ of operation [50].

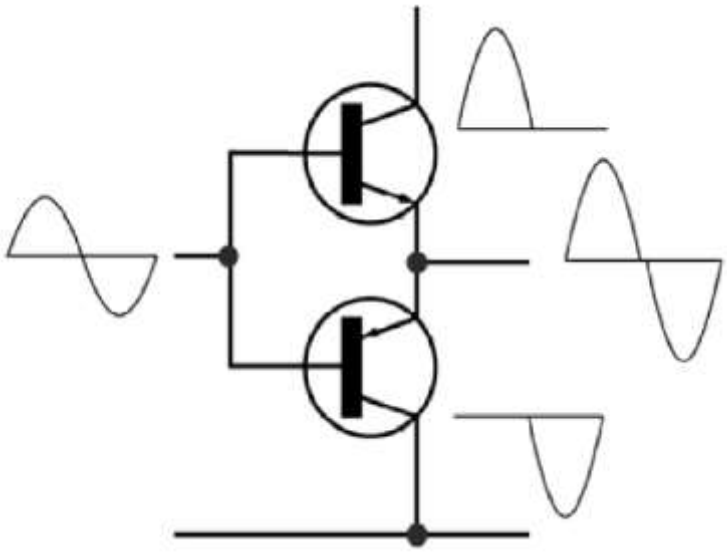

Fig. 2.7. Class-B power amplifier push-pull amplifier [50].

## 2.4 Types of Class-B Power Amplifiers

In this section, we have compared the different types of class-B amplifiers and chose the best type of class-B that will be implemented for a design of a class-B power amplifier using a Double-Gate (DG) MOSFET.

### 2.4.1. Class-B Power Amplifier With Transformer

The circuit of Figure 2.8 shows a class-B power amplifier circuit that utilizes a fair balanced center-tapped input transformer, which separates the input signal's waveform into equivalent two half' input waves, which are out of phase by 180 degrees with one another [51].

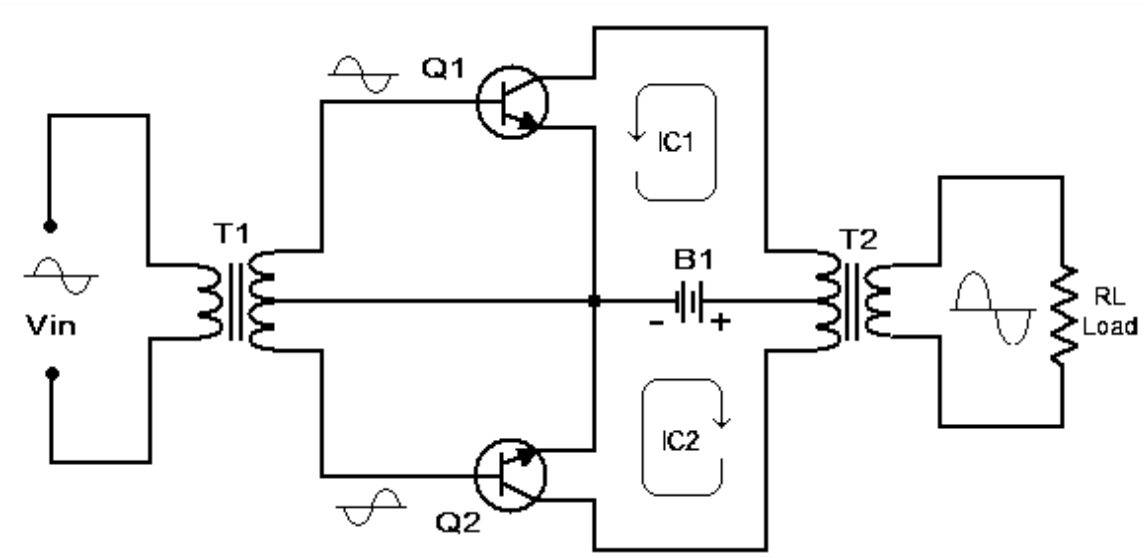


Fig. 2.8. Class-B power amplifier with transformers.

Another middle-tapped transformer on the output is utilized to recombine the two signals giving the expanded or increased power to the load. The semiconductors used for this kind of transformer push-pull power amplifier circuit are both NPN semiconductors with their producer terminals associated together [51, 52]. If the transformer is precisely center-tapped, the two-collector current will flow in inverse ways (ideal condition), and there will be no magnetization of the transformer core, limiting the crossover distortion.

### 2.4.2. Class-B Power Amplifier Without Transformer

One of the primary inconveniences of the class-B power amplifier (Fig. 2.8, using transformers) is that it utilizes adjusted center-tapped transformers in its way of design, making it costly to develop [53-55]. Nevertheless, another kind of class-B amplifier named a complementary-symmetry class-B amplifier that doesn't utilize transformers to design it along these lines. These are transformer-less utilizing instead of corresponding or coordinating sets of intensity semiconductors.

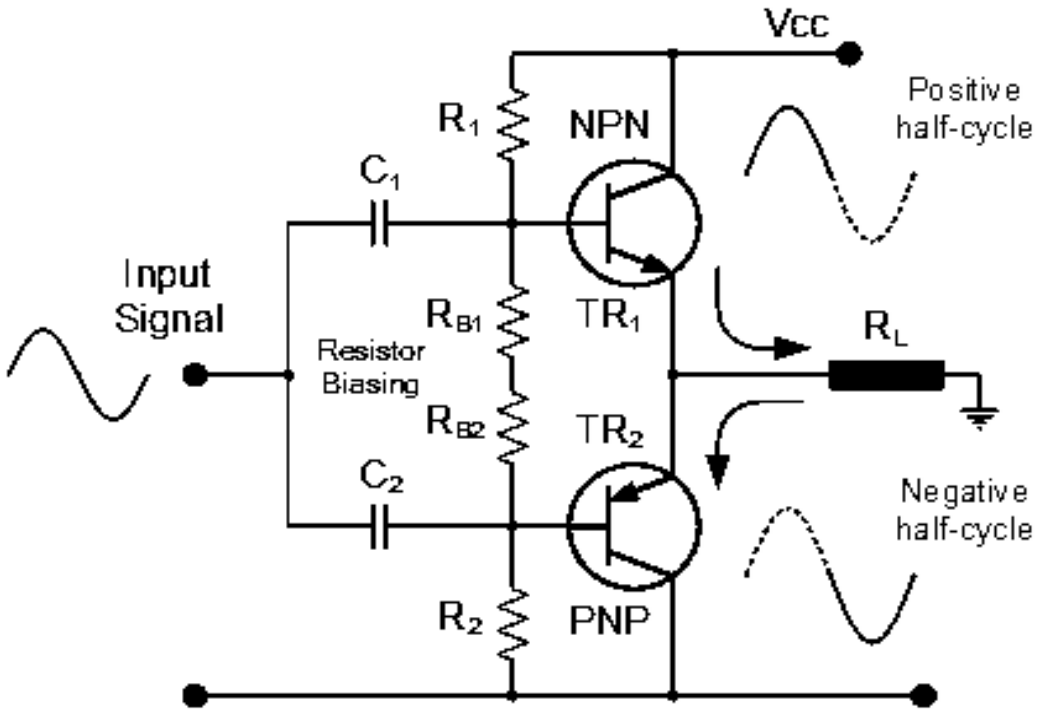


Fig. 2.9. Class-B power amplifier without transformers.

There is no use of transformers, which will make the power amplifier circuit smaller for a similar measure of the output signal; likewise, there will be no random magnetic field effects or transformer distortion that will affect the output waveform. Class-B without the transformer circuit is illustrated in Figure 2.9. The output semiconductors for every 50% of the waveform (negative and positive) will each have a 0.7 V region and they do not conduct. The outcome is that the two semiconductors are switched OFF simultaneously.

## 2.5 Conclusion

Class-B power amplifier with the use of DG MOSFET is properly designed in a block diagram that explains the purpose of each stage, starting from stage one to stage three. These stages were taken purposely because if they are not properly designed, then the power amplifier will not perform as expected. Hence, all the subtopics explained in this chapter were aimed and adequately explained the process of designing power amplifiers and also explained the device used in this research (i.e., DG MOSFET).

# Chapter-3

# MATHEMATICAL ANALYSIS AND DESIGN OF CLASS-B POWER AMPLIFIER

## 3.1 Design Algorithm

The design of a power amplifier is implemented by designing each stage of the amplifier, there are three stages (i.e. input stage, the driver stage, and the output stage). The design procedure for this includes mathematical analysis of the class-B power amplifier and deriving the formula using DG MOSFET [56, 57].

Class-B operation is when each semiconductor turn-ON for a positive portion of an AC signal, while the second semiconductor is off for the negative portion of an AC signal and DG MOSFET were used as semiconductors for this research. To get output for the full input signal, it is important to utilize two semiconductors and have each conduct on inverse half-cycles. The combined operation gives a total cycle of the output signal. The power amplifier's output power provided to the load is drawn from the power supply that gives the dc power or the input power. The value of this power can be calculated using the following equation together with the drain current of the DG MOSFET [58, 59]:

$$P_{in} = V_{CC} \times I_{dc} \tag{3.1}$$

where $V_{CC}$ is the voltage given to the first DG MOSFET drain current and $I_{dc}$ is the average DC current. Likewise, the amount of average current that is drawn in each transistor can be given as:

$$I_{dc} = \frac{\left(I_D\right)_{\max}}{\pi} \tag{3.2}$$

Hence,

$$\left(P_{in}\right)_{dc} = 2 \times \left[\frac{\left(I_C\right)_{\max}}{\pi} \times V_{CC}\right] \tag{3.3}$$

In Eq. (3.3) factor 2 is multiplied because of the two DG MOSFETs in a push-pull power amplifier. The RMS value of the drain current is given as follows:

$$I_{D-RMS} = \frac{(I_D)_{\max}}{\sqrt{2}} \tag{3.4}$$

The RMS value of the output voltage is also calculated as follows:

$$V_{O-RMS} = \frac{V_{CC}}{\sqrt{2}} \tag{3.5}$$

Assuming an ideal state of extreme power, therefore:

$$(P_O)_{ac} = \frac{(I_D)\max}{\sqrt{2}} \times \frac{V_{CC}}{\sqrt{2}} = \frac{(I_D)_{\max} \times V_{CC}}{2} \tag{3.6}$$

Hence the total maximum efficiency

$$\eta_{total} = \frac{(P_O)_{ac}}{(P_{in})_{dc}} \tag{3.7}$$

$$= \frac{(I_D)_{\max} \times V_{CC}}{2} \times \frac{\pi}{2(I_D)_{\max} \times V_{CC}}$$

$$= \frac{\pi}{4} = 0.785 = 78.5\%$$

which is the maximum efficiency of class-B power amplifier

It is important to design the component values to minimize the difference between the constructed circuit's approximated and actual operating conditions. This section of the thesis will show the calculations stage by stage, beginning at the output stage and working backward while making justifications for the choices and assumptions.

## 3.2 Circuit Analysis of Class-B Power Amplifier

Firstly, it is required to determine the voltage supply ($V_{cc}$) that would be able to deliver the required power to the load. Some conditions had to be imposed in the component calculations to minimize operating power losses in the output stage. The amplifier's output stage will use a DG MOSFET to get a high output current as BJT might

not be efficient to deliver the required current for high-power large-signal applications. The first step in the design of the output stage is to calculate the supply voltage required.

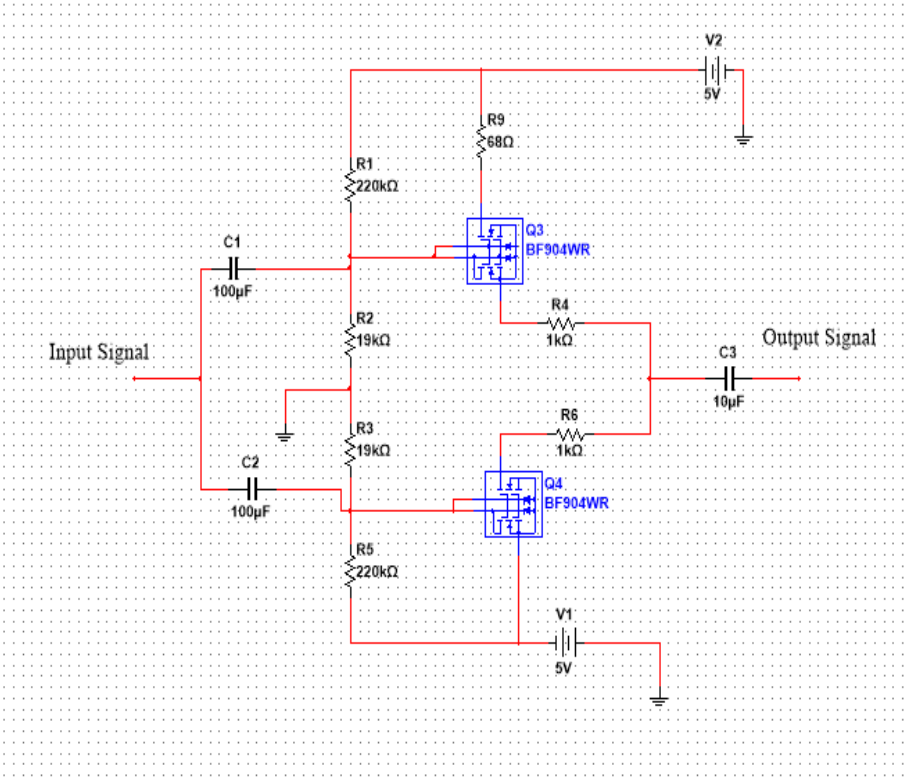


Fig. 3.1. Class-B power amplifier with DG MOSFET.

It is assumed that the power is 2.5W for a 4 Ω load and imposed 1 V drop across each of the output drains of the DG MOSFET. It is also required to bias the circuit mid-rail to achieve the desired class-AB operation with the symmetric push-pull configuration [60, 61]. To obtain $V_{cc}$ it is required to know the output voltage, it is known that:

$$P_o = \frac{V_{opk}^2}{R_L} = \left(\frac{V_o^2}{2}\right) \times \frac{1}{R_L} \tag{3.8}$$

For a single rail supply. This gives:

$$V_o = \sqrt{2 \times 2.5 \times 4} = 4.47V$$

Table 3.1 shows the power dissipation of a DG MOSFET when different supply voltages are applied. It is seen that power dissipation decrease with a decrease in source voltage, however, at voltages under 0.4 V - 0.3 V, the delay times shows an increase.

Hence for this design of class-B power amplifier, the chosen window of source voltage at the gate is 0.4 V, this is because the switching time is assumed to be compatible with the class-B amplifier to reduce crossover distortion.

Table 3.1. Power and time delay for a DG MOSFET

| **Supply Voltage (V)** | **Power Dissipated ($\mu W$)** | **Rise Time (ns)** | **Fall Time (ns)** | **Propagation Delay (ns)** |
|---|---|---|---|---|
| **0.9** | 1.0686 | 0.137 | 0.3617 | 0.2494 |
| **0.8** | 0.7986 | 0.1412 | 0.3626 | 0.2569 |
| **0.7** | 0.5758 | 0.1528 | 0.3689 | 0.2658 |
| **0.6** | 0.3967 | 0.1660 | 0.3745 | 0.2702 |
| **0.5** | 0.2630 | 0.1905 | 0.3854 | 0.2879 |
| **0.4** | 0.1605 | 0.1935 | 0.3997 | 0.2916 |
| **0.3** | 0.0870 | 0.2467 | 0.4875 | 0.3671 |
| **0.2** | 0.0382 | 0.9217 | 1.735 | 1.3283 |
| **0.18** | 0.0311 | 1.4391 | 2.5035 | 1.9713 |
| **0.15** | 0.0222 | 3.0720 | 4.9982 | 4.0351 |

Furthermore, from the datasheet of DG MOSFET, the worst-case $V_{DS}$ of 0.5 V for a BF904WR, the total source voltage that is required is given as:

$$V_{CC} = V_O + V_{DS1} + V_{DS2} \tag{3.10}$$

$$V_{CC} = 4.4 + 0.4 + 0.4 = 5.2V$$

A 5 V as power supply to the class-B power amplifier was chosen. Still, in the output stage of the class-B power amplifier, it is required to know the current flowing in the output stage to determine the output resistors [62, 63]. To do this, the maximum output current needs to be calculated that can flow in the output stage:

$$I_{OUtMAX} = \left(\frac{V_O}{2}\right)\left(\frac{1}{R_L}\right) = \left(\frac{5}{2}\right)\left(\frac{1}{4}\right) = 0.625A \tag{3.11}$$

Using Ohm's law [64, 65]:

$$R_7 = R_6 = \left( \frac{V_{R7}}{I_{OUTMAX}} \right) = \left( \frac{1}{1.5} \right) \geq 0.66\Omega \tag{3.12}$$

Here *1 k*Ω resistor was chosen. Looking at the output power dissipated in the two resistors ($R_6$ and $R_7$):

$$P_{O(R7\&R6)} = 2\left(I_{OUTMAX}\right)^2 \times R_7 = 2\left(1.5\right)^2 \times 0.66 = 2.97W \tag{3.13}$$

Table 3.2. The BF904WR limiting values [60]

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | | - | 12 | V |
| $I_D$ | Drain current | | - | 30 | mA |
| $\pm I_{G1}$ | Gate-1 current | | - | 10 | mA |
| $\pm I_{G2}$ | Gate-2 current | | - | 10 | mA |
| $P_{tot}$ | Total power dissipation; BF998 | Up to $T_{amb}$ = 60 ℃ | - | 200 | mW |
| | | Up to $T_{amb}$ = 50 ℃ | | 200 | mW |
| $P_{tot}$ | Total power dissipation; BF99R | Up to $T_{amb}$ = 60 ℃ | - | 200 | mW |
| $T_{sig}$ | Storage temperature | | -65 | +150 | ℃ |
| $T_j$ | Operating junction temperature | | - | 150 | ℃ |

Selecting the output DG MOSFETs is considered the worst-case current that can flow through both of them. Having calculated that close to a maximum of 0.625 Ω can flow through both MOSFETs and BF904WR is chosen because the datasheet of this MOSFET shows that this amount of current can flow through the drain to the source [69,

70]. Using the following table obtained from the datasheet of BF904WR MOSFET, the voltage across the drain is calculated with the help of the datasheet.

Table 3.2 shows the liming values of DG MOSFET (i.e. BF904WR), which is used to calculate the resistance in the drain of the DG MOSFET. It is seen in this table that drain to source voltage should not exceed 12 V and not exceed a drain current of 30mA to protect the drain of the DG MOSFET, it should be at least at 3 V, and the resistance needs to be connected between the source and the drain of the DG MOSFET. This is done to protect the DG MOSFET when it is in an active region. A resistor $R_9$ is calculated as follows:

$$R_9 = \frac{V_{CC} - V_{DS1}}{I_D} \tag{3.14}$$

$$R_9 = \frac{5V - 3V}{30mA} = 66.67\Omega$$

Using a resistance standard table 68 Ω was chosen. The value of $I_D$ (drain current) is obtained from the table of the BF904WR datasheet. The last component in this section to design was the output capacitor. Its purpose is to isolate the load from the DC signal, this is because the output is biased such that:

$$V_O = \frac{V_{CC}}{2} \tag{3.15}$$

when using a single rail power supply. This creates:

$$V_O = \frac{5}{2} = 2.5V$$

offset at the output, which means that the load will always have current flowing through it without the capacitor.

## 3.3 Software Tools and Chosen Solution

The chosen solution to implement the class-B power amplifier is an amplifier without transformers. The reason for choosing this type of amplifier is that it is easy to

implement and design the driver stage so that it is compatible with the DG MOSFET. Also, it is expensive to find the transformers to be used in this design. DG MOSFET can be biased by the resistors so that they operate in an active region [71-75].

**Multisim**- This software was used to build the full circuit for the design of the class-AB Power Amplifier, the reason why this simulation software was used is that it is easy to use and it has high accuracy meaning the simulation circuit from this Multisim is almost behave the same as the hardware circuit implementation. This software tool helps in developing high advanced circuit diagram, class-B power amplifier was also designed and simulated using this software tool.

## 3.4 Conclusion

Mathematical analysis or design plays an essential role in technical system designs such as power amplifiers; without it, power amplifiers or any other technical system might not work properly. After all mathematical designs and analysis, simulation for class-B power amplifier was tested and analyzed, giving the researcher the guild on what component values should be used in electronic components such as resistor and capacitor values.

# Chapter-4

# ANALYSIS OF CLASS-B POWER AMPLIFIER WITH DG MOSFET

## 4.1 Class-B Power Amplifier with DG MOSFET Simulation Circuit

The circuit in Figure 4.1 has the complete simulation of the class-B power amplifier, where two DG MOSFETs were used to implement the operation of a class-B power amplifier. The circuit consists of resistors and capacitors [76]. The purpose of using the fixed resistors is because resistors can bias the gates of the DG MOSFETs whenever the input signal is applied to the power amplifier. These biasing resistors are needed to minimize crossover distortion. Although this sort of circuit tries to limit crossover distortion, it doesn't remove all of it. Each power amplifier stage has its voltage divider that feeds the gates of each DG MOSFET, and they can be calculated as follows [77]:

$$\frac{V_{G1}}{V_{CC}} = \frac{R_1}{R_2 + R_1} \tag{4.1}$$

To get the gates voltage of 0.4 V so that DG MOSFET can operate at the active region and to have allowable delay time, resistor-1 and resistor-2 should be calculated. These resistors are calculated by fixing each resistor value i.e., resistor-1 and knowing the gates voltage, resistor-2 can be calculated as:

$$R_2 = \frac{V_{CC}}{V_{G1}} \times \left(R_1 + R_2\right)$$

$$= \frac{5}{0.4} \times \left(220k\Omega + R_2\right)$$

Solving this equation for resistor-2 is:

$$R_2 = 19k\Omega$$

These calculations are the same as the second DG MOSFET.

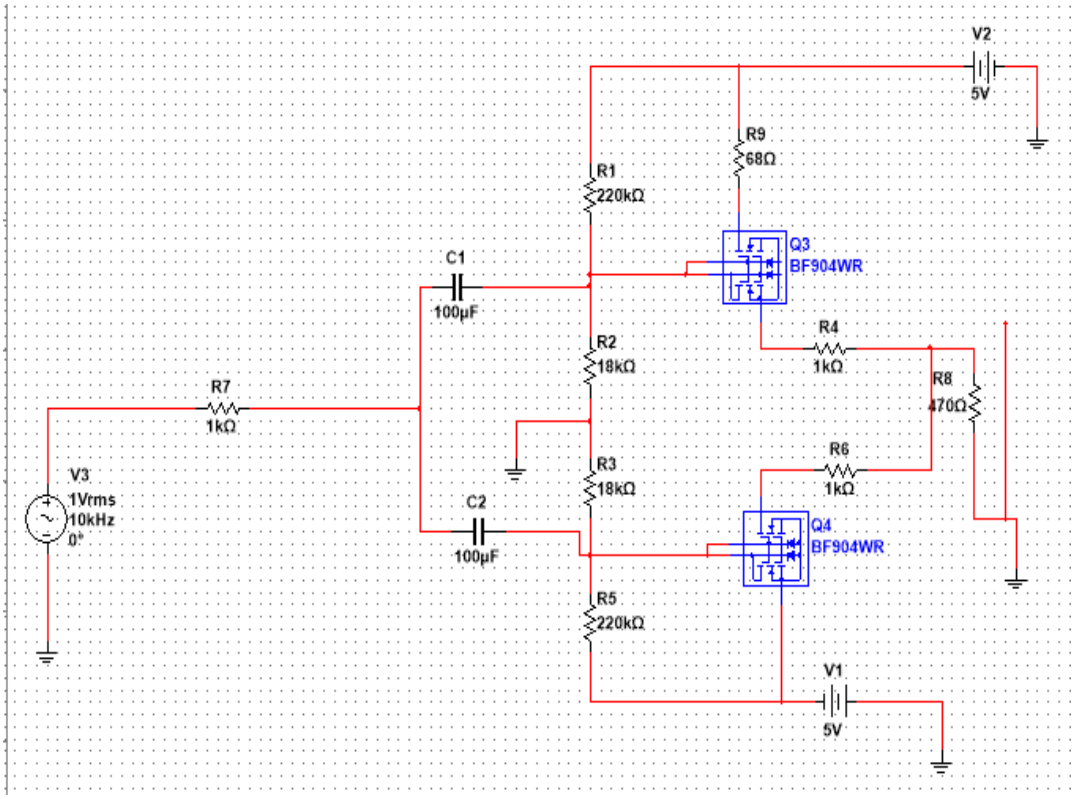


Fig. 4.1. Class-B power amplifier with AC source.

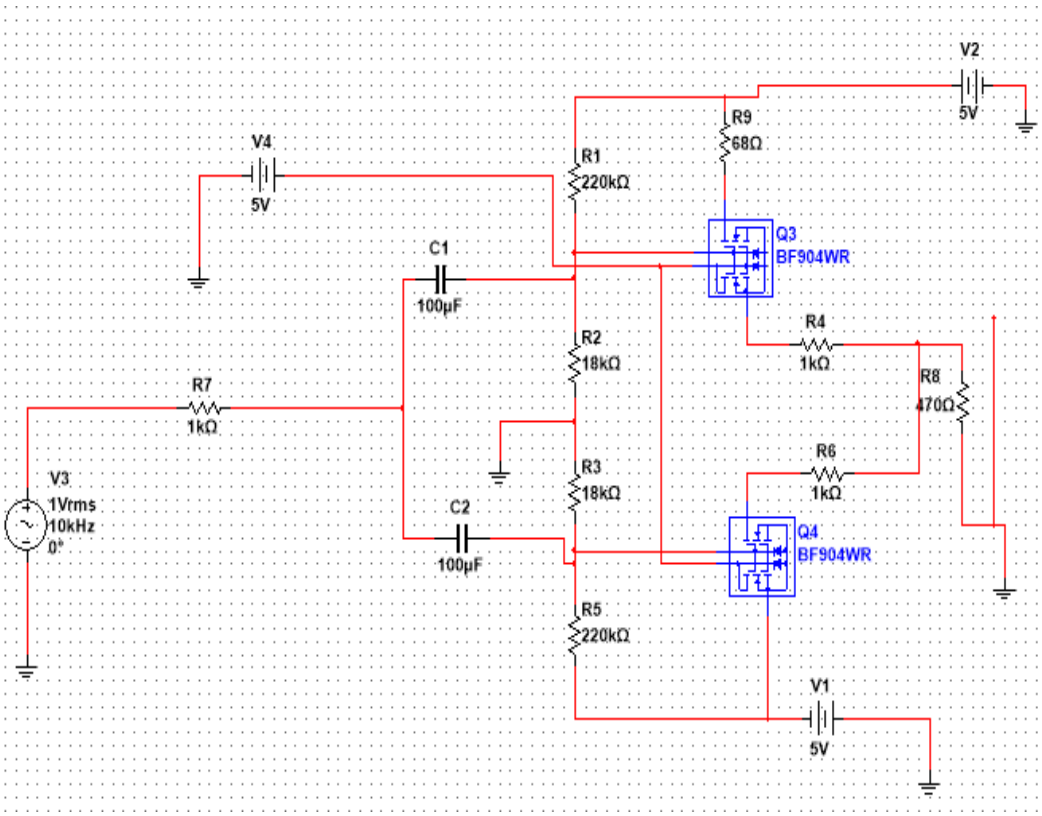


Fig. 4.2. Class-B amplifier to avoid crossover distortions.

Different input signals were applied to the class-B power amplifier's input to test the performance of the power amplifier. In this circuit, both gates (i.e., gate-1 and gate-2) of DG MOSFET were connected to avoid the crossover distortion during the power amplifier's operation mode. The input signal was fed into the class-B power amplifier to test the class-B power amplifier's performance when DG MOSFETs was used with the SiO2 dielectric. This structure differs from the basic power amplifier [78-80].

## 4.2 Simulation Results

The simulated circuit (Figure 4.1 and Figure 4.2) has been implemented aiming at eliminating one of the major problems faced by class-B, which is the problem of crossover distortion [81, 82]. In this circuit, the gates that are near the source are connected, and they are fixed biased to source voltage of 5 V. This has been performed so that both DG MOSFETs can partially operate in an active region and the other gate is connected to the signal that is coming from the input.

The implementation of the design was challenging. Learning from experience led to setting up the design one stage at a time, testing each stage, and then testing the amplifier as a whole. This systematic approach led to the entire design being fully functional in a relatively short amount of time.

Figure 4.3 shows the output signal, where the crossover distortions have been observed. These crossover distortions occur because of the transient switching time, it takes for one DG MOSFET to turn-ON. The delay time of the MOSFET to turn-ON increases the crossover distortion; hence, choosing a DG MOSFET with high switching transient will cause the class-B amplifier to have much crossover distortion at the output signal. The input AC signal was applied to the class-B power amplifier to test the performance of the class-B amplifier. The performance has been tested.

The output stage was the first to be built and tested. A voltage was applied to the input and a corresponding value was read at the output (with no load connected). It was noted that it followed the input voltage almost exactly but with crossover distortions. Therefore, the output stage was working correctly.

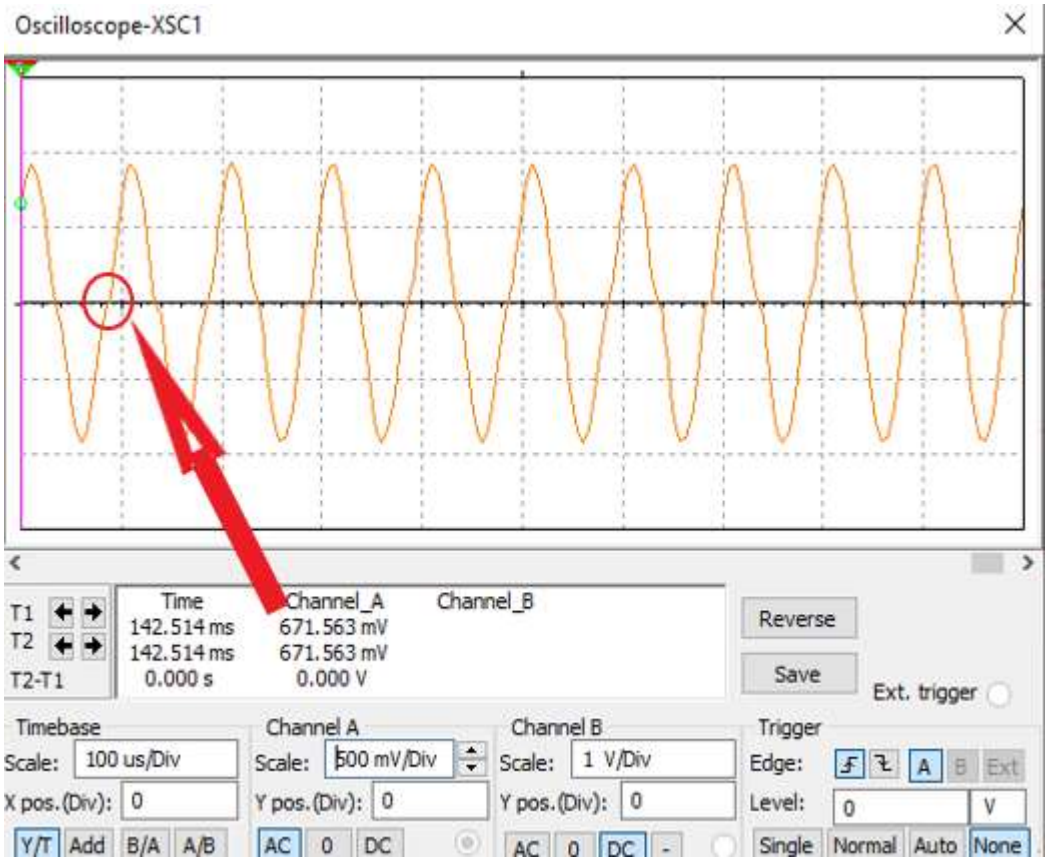


Fig. 4.3. Class-B output AC waveform.

Figure 4.3 shows two signals with different properties, i.e. amplitude. It is shown that the output signal is the same as the input signal, meaning that the output signal has some crossover distortions and an amplitude slightly less than that of the input signal. The signal in channel B, which is connected to the class-B amplifier's output stage, has the peak-to-peak voltage that is greater than that of channel A. the gain of the power amplifier is then calculated using these output signals (i.e., input signal and output signal).

From the Figure 4.3, the obtained parameters such as source voltage and dc current are used to calculate the circuit's input power and the output power of the circuit [83]. Table 4.1 shows the power amplifier parameters that were realized when the input signal had 1 V peak-to-peak. Figure 4.4 has been obtained from the class-B power amplifier circuit when the gate of each DG MOSFET was fixed biased to 5 V; this was done to reduce the crossover distortion of the class-B power amplifier.

Table 4.1. Power amplifier's parameters

| Realized Parameters | Value |
|---|---|
| $V_{cc}$ | 5 V |
| $I_{DC}$ | 215.4 mA |
| $V_{0-pp}$ | 263.426 mV |
| $V_{o-rms}$ | 186.27 mV |
| $P_o = (V_{o-rms})^2/R$ | 3.469 mW |
| $P_{in} = 2 \times V_{cc} \times I_{DC}$ | 2.145 mW |
| R | 10 Ω |

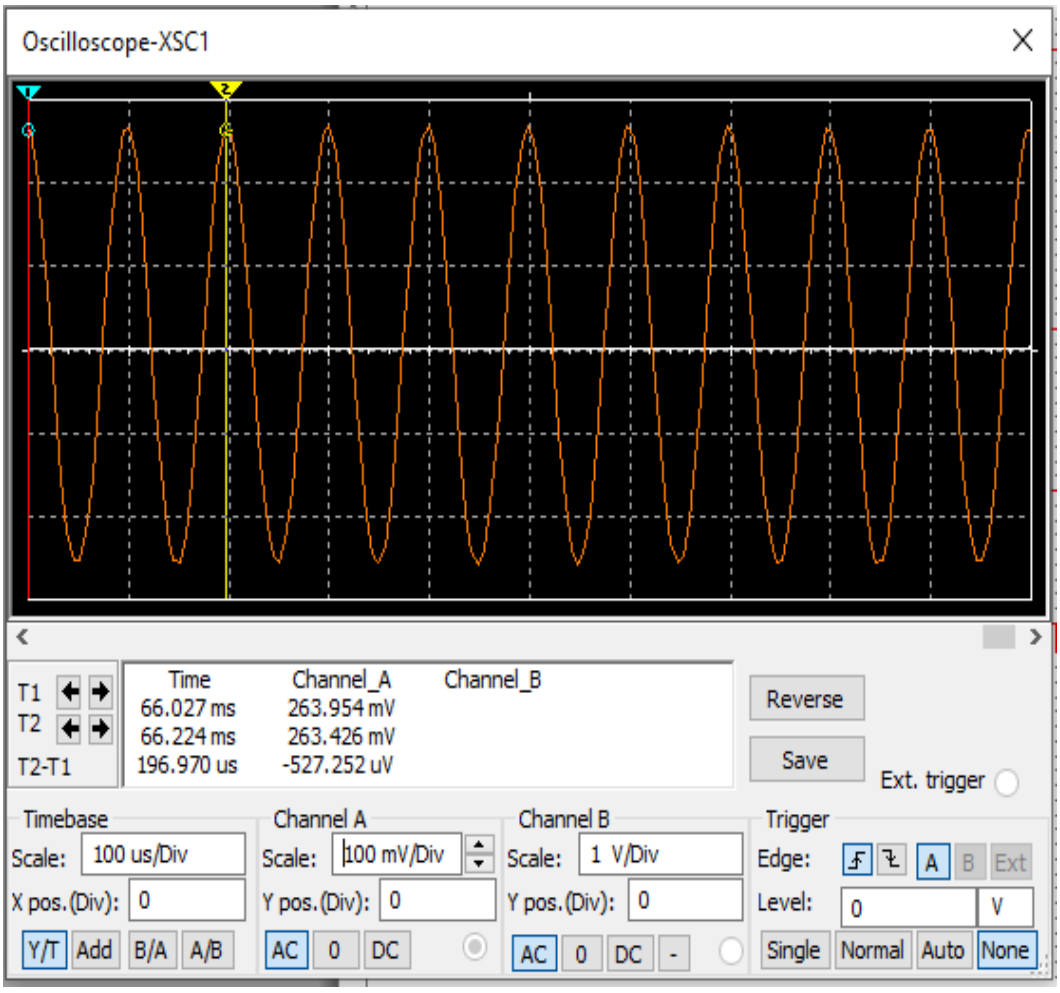


Fig. 4.4. Output waveform when DG MOSFETs is fixed biased.

### 4.3 Efficiency Calculation of Class-B Power Amplifier

Firstly, the calculations will be done by assuming that there will be no losses in the circuit, meaning if an input signal is applied to the circuit, the output signal will be the same as the input signal [84]. Generally, the efficiency is given by the ratio of output and input power as shown in the following equation [85]:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \tag{4.2}$$

For class-B amplifier the input power is given by:

$$P_{in} = V_{CC} \times I_{CC} \tag{4.3}$$

Where the $V_{CC}$ and $I_{CC}$ are the dc input voltage and dc output current.

$$I_{CC} = I_{Gate-bias} + I_{D-Avg} \tag{4.4}$$

The Eq. (4.4) is the total current source which contains two currents i.e. gate biasing current and average drain current. Gate biasing current is calculated as follows using the circuit diagram Figure 4.1 and Figure 4.2:

$$I_{Gate-bias} = \frac{5V}{220k\Omega + 18k\Omega} = 21\mu A \tag{4.5}$$

This current is too small, and it can be neglected. The average drain current is the peak current divided by pi (∏) as shown in the following Eq. (4.6) and assuming that there are no losses in the circuit such as voltage drops and current losses [86]. If the input signal source has a voltage of 5 V peak to peak and it drives the load of 10 Ω:

$$I_{D-avg} = \frac{I_{D-peak}}{\pi} = \frac{\left(\frac{5}{10}\right)}{\pi} = 159.15mA \tag{4.6}$$

Hence, $I_{cc}$ are approximately equals to the average drain current $I_{D\text{-}avg}$. Therefore, the total input power with the assumption that they are no losses in the circuit is calculated as follows:

$$P_{Out} = V_{CC} \times I_{CC}$$

$$= 5V \times 159.15mA \ = 795.77mW$$

The output power is the power dissipated across the load and the load is 10 Ω for this design, it has been calculated as:

$$P_{in} = \frac{\left(V_{Out-RMS}\right)^2}{R_L} \tag{4.7}$$

The Eq. 4.7 is then calculated in terms of the peak voltage as:

$$P_{in} = \frac{\left(\frac{V_{Out-RMS}}{\sqrt{2}}\right)^2}{R_L} = \frac{5^2}{2 \times 10} = 1250mW$$

Therefore, the efficiency of this class-B power amplifier without any losses in the circuit is calculated as follows:

$$\eta = \frac{795.77mW}{1250mW} \times 100\% = 63.66\%$$

This is the maximum efficiency of a class-B amplifier which is less than the theoretical efficiency. It can be seen from the Table 4.1 that a class-B power amplifier can amplify the power of an input signal, even though it has a small gain of power amplification.

## 4.4 Transient Analysis of Class-B Power Amplifier with DG MOSFET

### 4.4.1 Using BJT

The circuit diagram (using BJT) of a class-B power amplifier is shown in Fig. 4.5. It consists of the signal source, DC bias circuit, transistors, output matching circuit, and load [87, 88]. Based on the operation of class-B power amplifier, which is to operate only when the input signal is applied to it, hence the DC bias circuit is used to partially bias the transistors (i.e., BJT) such that when an AC input signal is applied to the power amplifier,

then it can operate and amplify the input signal. Voltage divider rule was used as a DC bias circuit with a DC supply source of 5 V, divider rule in the DC circuit was used to calculate the biasing voltage or base voltage. Knowing that the base voltage or biasing voltage of a BJT is 0.7 V and fixing each resistor 3 kΩ to 220 kΩ, then the biasing resistances were calculated as:

$$\frac{V_B}{V_{in}} = \frac{R_4}{R_4 + R_3} \tag{4.8}$$

$$\frac{0.7v}{5v} = \frac{R_4}{R_4 + 220k\Omega}$$

Therefore: $R_4 = 35.81k\Omega$

These resistor values are enough to bias the transistors to the saturation region. The graph in Figure 4.6 shows the transient analysis of a class-B power amplifier with BJT. The transient response of a power amplifier is most likely to be affected by the power amplifier's output impedance and the load connected to it. Like any load (i.e. resistance load) added to a circuit, a definitive objective is to control the progression of current and voltage inside the circuit. Load impedances are also essential in assessing the behavior of a circuit under different conditions. For instance, a circuit accomplishes most maximum power when the load impedance is equivalent to the circuit output impedance. In Fig. 2(b), the settling time starts roughly around 0.6 ms (i.e., this is where the system starts to remain at 90% of its final value) caused by the mismatch of circuit output impedance and the load connected to the circuit.

The power amplifier with BJT is at settling time when the signal's voltage is at the range from the minimum voltage of -600 mV to the maximum voltage of 600 mV. A change in load impedance will affect the settling time and the charging and discharging of the RC time constant. The advantage of having a short settling time in a power amplifier is that the power amplifier takes a short time to amplify the input signal. Since settling time is the time needed for the response to arrive at the consistent state and stay inside the tolerance band around the final value; hence this power amplifier takes a short time to amplify the input signal.

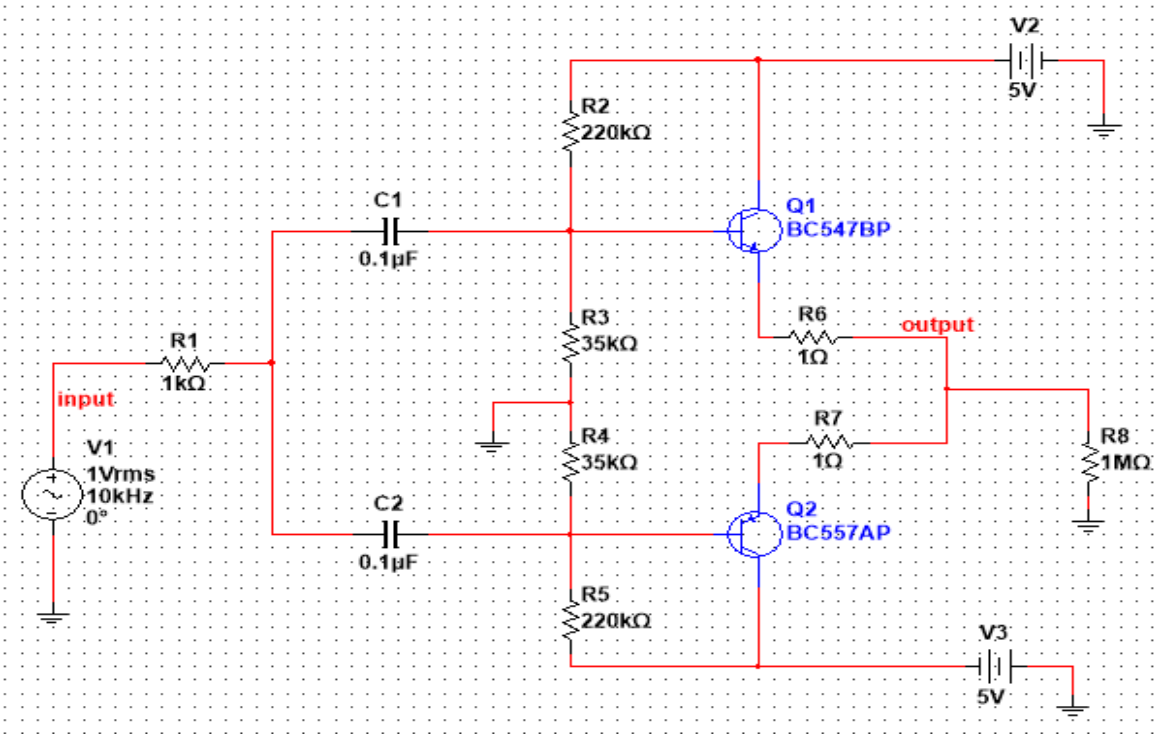


Fig. 4.5. Class-B power amplifier with BJT.

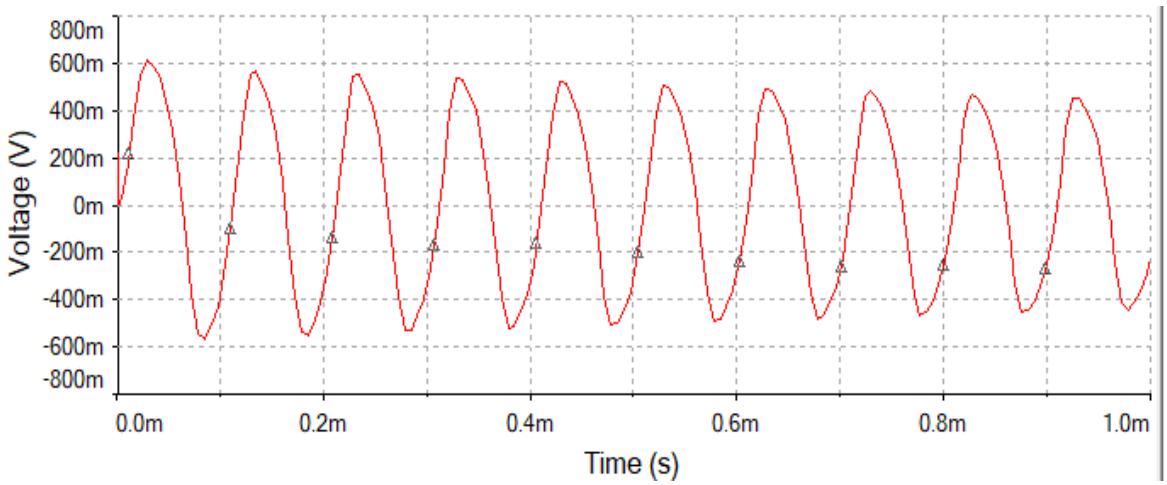


Fig. 4.6. Transient analysis with 1 MΩ resistive load.

### 4.4.2. Using Single-Gate MOSFET

The circuit diagram of Figure 4.7 shows a class-B power amplifier with a Single-Gate (SG) MOSFET. The class-B power amplifier must amplify an input signal, but this power amplifier only operates when an input signal is applied to it. Hence the biasing voltage for the SG MOSFET is essential so that SG MOSFET can turn on when an input signal is applied regardless of the amplitude of an input signal fed to the input stage of an amplifier [89, 90]. The voltage divider resistors are used to bias SG MOSFET. Gate voltage has been calculated using the voltage divider rule as:

$$\frac{V_G}{V_{in}} = \frac{R_8}{R_8 + R_1} \tag{4.9}$$

$$V_G = \frac{20k\Omega}{20k\Omega + 100k\Omega} \times 12v = 2v$$

This amount of voltage is sufficient to turn-ON a SG MOSFET because the threshold voltage of a MOSFET from the datasheet of any MOSFET is roughly 2 V to 3 V depending on the type of SG MOSFET.

The concept of settling time in a power amplifier is not that complicated; nonetheless, there are a few situations where the initial settling time is quick, followed by an extended time of settling to the final value. Thus, for this power amplifier with SG MOSFET, its settling time is much less than that of the power amplifier using BJT, as seen in the previous section. A thermal tail is found in this class-B power amplifier produced when the change in voltage within the class-B power amplifier. This thermal tail also affects the settling time of the power amplifier, which increases the settling time of the power amplifier. The advantage of a power amplifier with a lower settling time (0.4 ms) is that a power amplifier responds faster to the input signal to amplify it to a certain amount of voltage gain.

From Figure 4.8, the power amplifier with SG MOSFET is at settling time when the voltage range starts from the minimum voltage of 2.6 V to the maximum voltage of 4.1 V; this is when the power amplifier starts to enter at settling time which is 0.1 ms.

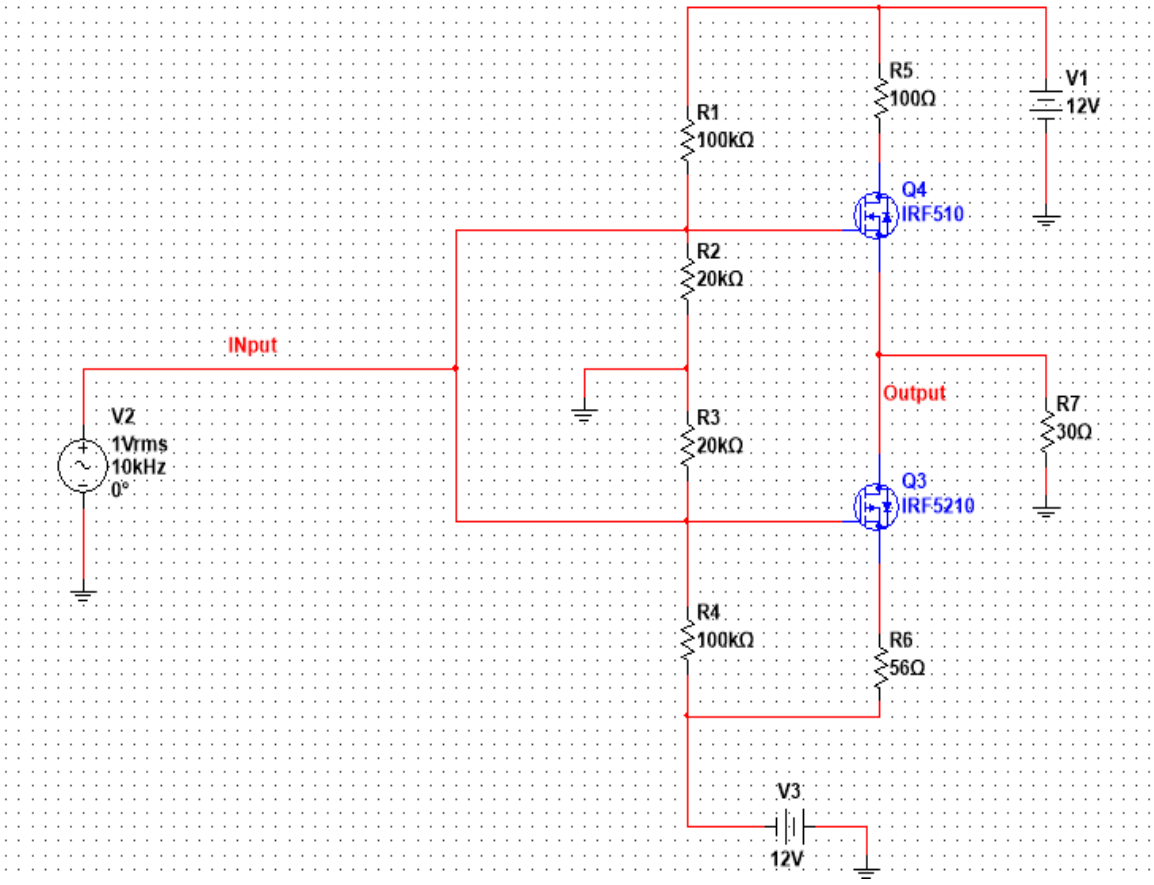


Fig. 4.7. Class-B power amplifier with single-gate.

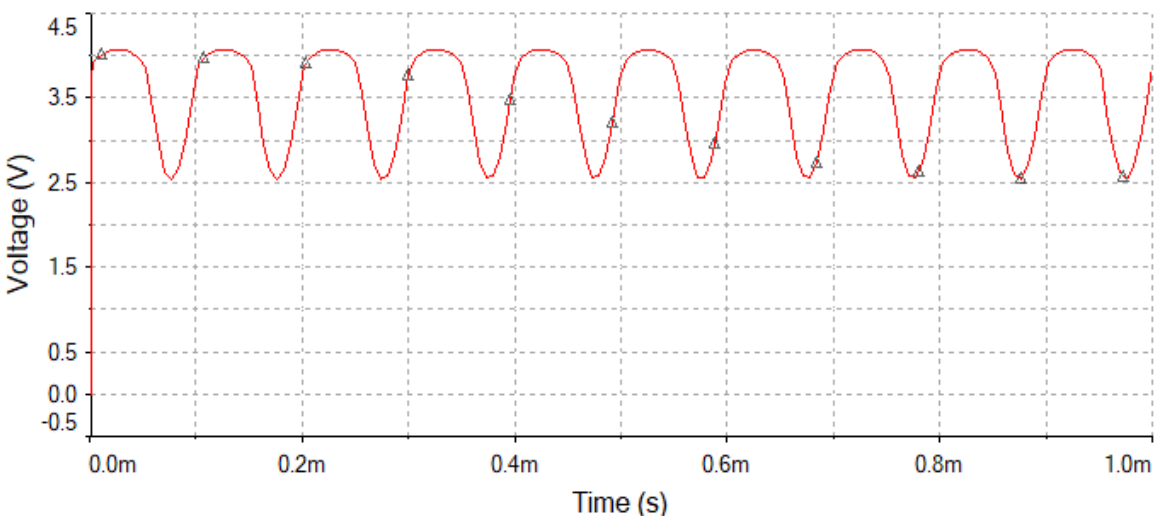


Fig. 4.8. Transient analysis with 1 MΩ resistive load.

This circuit of a class-B power amplifier with SG MOSFET has a smaller settling time compared to class-B BJT power amplifier, the main reason for that to happen is that the switching frequency of a SG MOSFET is higher than that of BJT. The advantage of this class-B power amplifier in terms of settling time is that high load impedances can be connected to it to match the circuit's output impedance and deliver the maximum power to the load.

### 4.4.3. Using Double-Gate MOSFET

The use of Double-Gate (DG) MOSFET has solved various problems other types of MOSFET face in terms of switching transients. The power dissipation of this type of amplifier is zero at the quiescent condition (i.e. when no load and input signal are connected to the amplifier). There is no power dissipation because the collector current is zero when there is no load or input signal. The circuit consists of resistors and capacitors [90 ]. The purpose of using the fixed resistors is because resistors can bias the gates of the DG MOSFETs whenever the input signal is applied to the power amplifier. These biasing resistors are needed to minimize crossover distortion. Although this sort of circuit tries to limit crossover distortion, it doesn't remove all of it. Each power amplifier stage has its voltage divider that feeds the gates of each DG MOSFET, and they can be calculated as follows:

$$R_2 = \frac{V_{CC}}{V_{G1}} \times \left( R_1 + R_2 \right) \tag{24}$$

$$= \frac{5}{0.4} \times \left( 220k\Omega + R_2 \right)$$

$$R_2 = 19k\Omega$$

In this circuit, the gates near the source are connected and fixed-biased to the source voltage of 5 V.

Complementary switching devices (i.e., BJT, single, and double-gate MOSFETs) are required for the push-pull class-B power amplifier [91]. The push-pull design takes an accurate copy of the single device transfer function and makes an image of the current (Y-axis) to form an output signal. When the amplifier is not operating (i.e., no input signal),

there are no voltage drops across each DG MOSFET; this is because the class-B power amplifier only operates when an input signal is applied to the circuit.

The output current of the power amplifier depends on the drain current of the DG MOSFETs, meaning as an input signal is applied to the power amplifier, each gate of the DG MOSFET is fixed biased to a source voltage of 5 V as shown in Figure 4.9. This is done so that when an input signal is applied to the power amplifier, then there will be no losses in the circuit by means of a DC biasing circuit because when there is no biasing circuit in the power amplifier, an input signal is responsible for biasing the switching devices which affects the output signal because most of the input signal voltage will be lost in the biasing the switching devices. Thus, by fixing biasing each gate of the DG MOSFET, authors are trying not to lose signal amplitude in biasing the switching devices; hence this technique of using DG MOSFET is suitable.

Figure 4.10 illustrates the transient response of a class-B power amplifier with DG MOSFET, where the load has been connected to the output side of a power amplifier. Load impedance influences the performance of circuits, specifically output voltages and output current, which also affect the settling time of the circuit. Although DG MOSFET reduces the power dissipation through the circuit and delivers the maximum power, the settling time of this type of circuit with DG MOSFET is much less compared to SG MOSFET and BJT circuits. The DG MOSFET gives such results when used in class-B power amplifiers because DG MOSFET prevents the electric field lines originating at the drain from terminating under the channel region. Figure 4.10 shows that when DG MOSFET are used, the settling time start early as the power amplifier is operating, meaning that once an input signal is fed to the circuit, the power amplifier amplifies an input signal and enters at the settling time at 0.2 ms or less than that time. It shows the response of the settling time at 0.2 ms when the power amplifier is in the range of 0 V to the maximum voltage of 3 V. That is a good advantage because when this circuit is used, the output signal is expected to be around less than 0.2 ms.

Table 4.2 shows a comparative analysis that is used to put all the essential characteristics and compare those values to the values that were theoretically mentioned in this chapter. These characteristics tell us that class-B power amplifiers with DG MOSFET switching devices perform in which way compared to other switching devices such as BJT, and SG MOSFET, in terms of trainset response when other characteristics are kept constant such as input signal frequency and voltage amplitude.

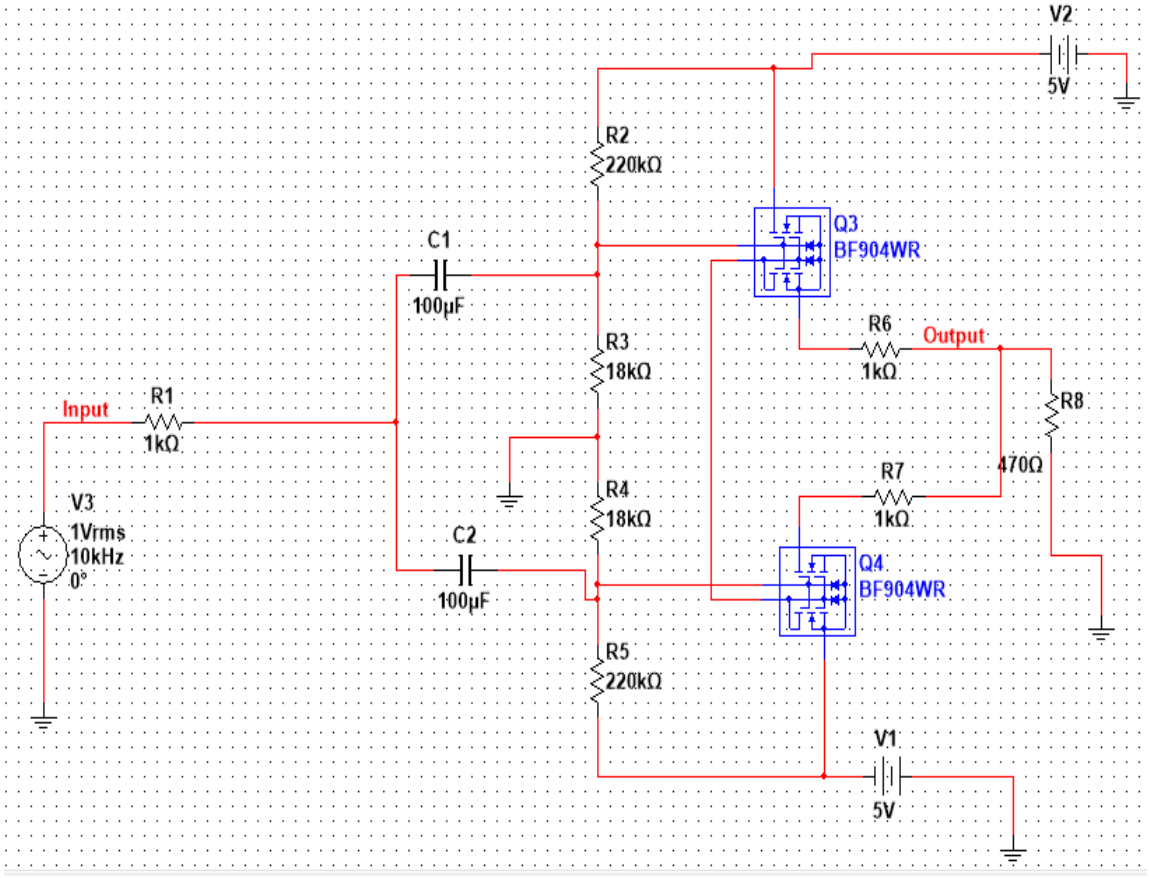


Fig. 4.9. Class-B power amplifier with DG MOSFET.

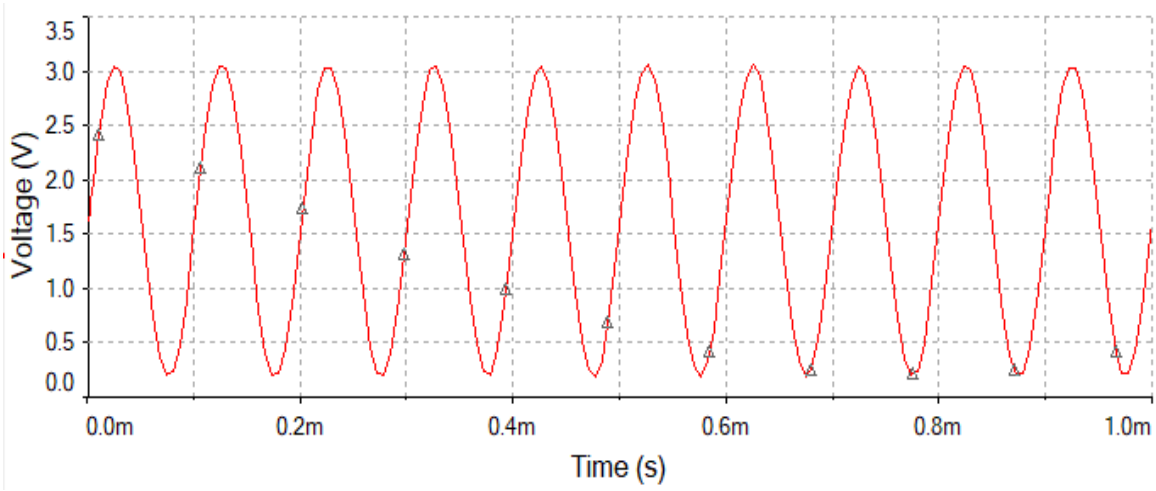


Fig. 4.10. Transient analysis with 0.47 MΩ resistive load.

Table 4.3 compares the comparative response table, which tabulates the results of this research about class-B power amplifiers compared to the other research of different power amplifiers such as class-AB, class-C, etc. [92, 93].

Table 1.2. Comparative analysis of model

| **Parameters** | **Settling time (ms)** | **Load Impedance (MΩ)** | **Output Circuit Impedance** | **Input Signal frequency (kHz)** | **Gain (V/V)** | **R** |
|---|---|---|---|---|---|---|
| **BJT** | 0.6 | 1 | High | 1 | 2 | 35 kΩ |
| **SG MOSFET** | 0.4 | 1 | Low | 1 | 2 | |
| **DG MOSFET** | 0.2 | 1 | Low | 1 | 2 | 19 kΩ |

Table 4.3. Comparative analysis of the proposed model

| **Parameters** | **Types of power amplifiers** | **Settling time** | **Operating Freq.** | **Closed Loop Bandwidth** |
|---|---|---|---|---|
| **[78]** | Class-AB | X | 1.609 MHz | 4.8 Hz-1.719 MHz |
| **[94]** | Class-B | 0.9m | 3 MHz | 22-32 KHz |
| **[95]** | Class-E | X | 4 MHz | X |
| **[96]** | Class-A | 0.54ms | 1.23 MHz | 3 Hz-100 kHz |
| **[97]** | Class-C | X | 15 MHz | 14.15-14.54 MHz |
| **This Work** | Class-B | 0.2 ms | 14.2 MHz | 2.3 Hz-300 kHz |

## 4.5 Conclusion

All the simulation results were analyzed. They were compared to the results of other power amplifiers to check if the results of designed class-B power amplifiers with DG MOSFET are still in range with other power amplifiers or if there are changes. It was analyzed that using DG MOSFET, class-B power amplifier reduces the crossover distortions, and also it has a better transient response than other power amplifiers, and the reason for that is because of the use of DG MOSFET.

## Chapter-5

# CIRCUIT LOSS ANALYSIS OF DESIGNED DG MOSFET BASED CLASS-B POWER AMPLIFIER

## 5.1 Losses of the Class-B Power Amplifier With SG MOSFET

The design of class-B power amplifier with SG MOSFET is vital in determining the losses in the power of the input signal at the output stage of the class-B power amplifier. Many factors may affect an input signal's power gain and amplification. One of the main factors that cause too many losses in power amplification is a type of design having so many stages in circuit design [98-101]. Figure 5.1 presents a class-B power amplifier with three steps, i.e., input, biasing, and output.

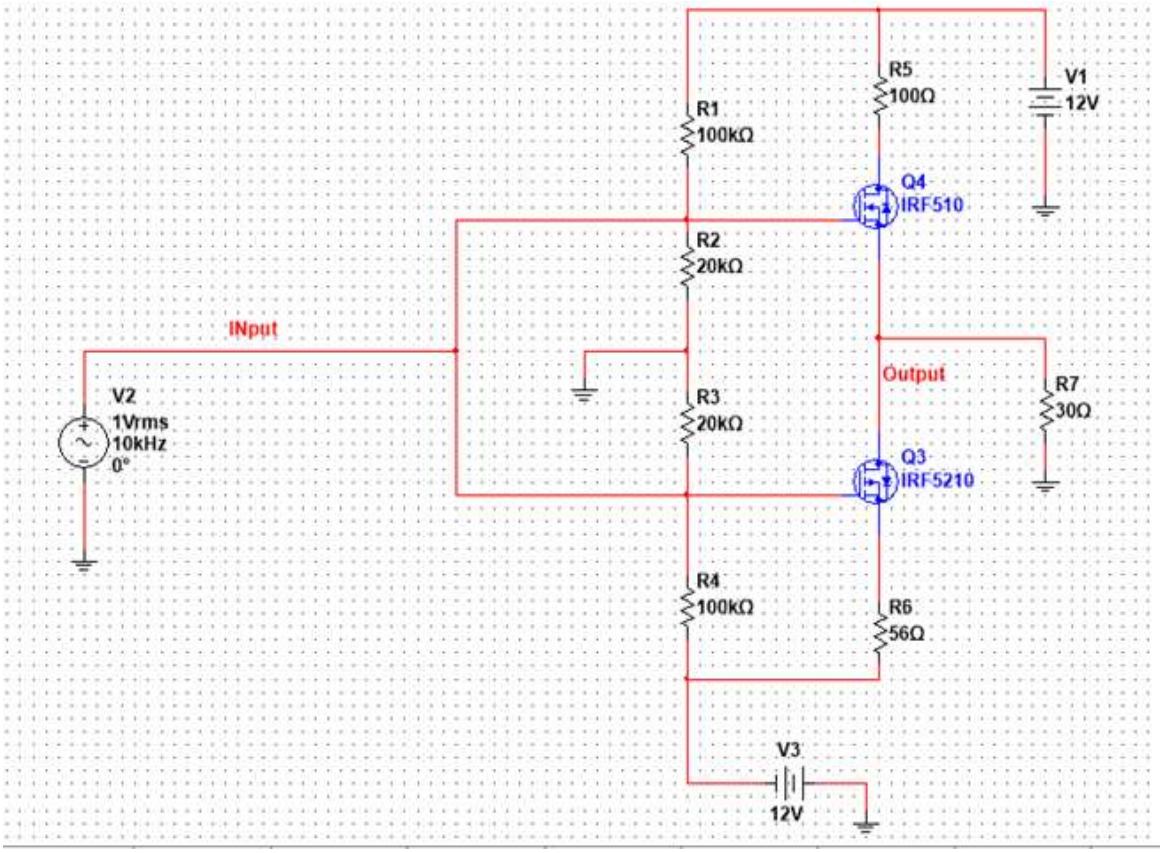


Fig. 5.1. Class-B power amplifier circuit with SG MOSFET

### 5.1.1 Dynamic Losses in SG MOSFET class-B power amplifier

In the ideal power amplifier circuit or switching devices shown in Fig. 5.1, the current is zero when there is no input signal (i.e., SG MOSFET turned-OFF) and the power is zero; thus, there is no power at the output stage [102]. When the signal is applied to the power amplifier, the voltage across SG MOSFET is zero, and the power loss is also zero. An ideal power amplifier suggests zero losses, hence offering 100% of efficiency. But in reality, a power amplifier cannot provide 100% of efficiency due to the components used in designing it. The following equations determine power losses and power efficiency:

$$Power_{Loss} = \left(V_{in} - V_{Out}\right) \times I_L \tag{5.1}$$

$$Efficiency = \frac{V_{out} \times I_L}{V_{in} \times I_L} = \frac{V_{out}}{V_{in}} \times 100\% \tag{5.2}$$

This research work focuses on the losses of using single-gate MOSFET in class-B power amplifiers [103]. This section focuses on three types of losses of class-B power amplifiers, i.e., conduction losses, switching losses, and static (quiescent) losses.

### 5.1.2 Conduction Losses

Conduction losses happen when the switching device is in full conduction. The current in the circuit (i.e., class-B power amplifier) is whatever is needed by the circuit. The voltage at its terminals is simply the voltage drop because of the actual switching device [104]. These conduction losses are in direct relationship with the duty cycle. Conduction losses in SG MOSFET can be determined using a SG MOSFET approximation with the drain-to-source on-state resistance. The following equation shows a drain to source voltage which is then used to determine the conduction losses (biasing voltage):

$$V_{DS}\left(i_D\right) = R_{DSon}\left(i_D\right) \times i_D \tag{5.3}$$

where $V_{DS}(i_D)$ is the drain-source voltage, as a function of drain current and $R_{DS\text{-}ON}(i_D)$ is an ON-resistance determined from the datasheet of a MOSFET, with the use of MOSFET approximation graph shown in Figure 5.2. This ON-resistance is also a function of drain current.

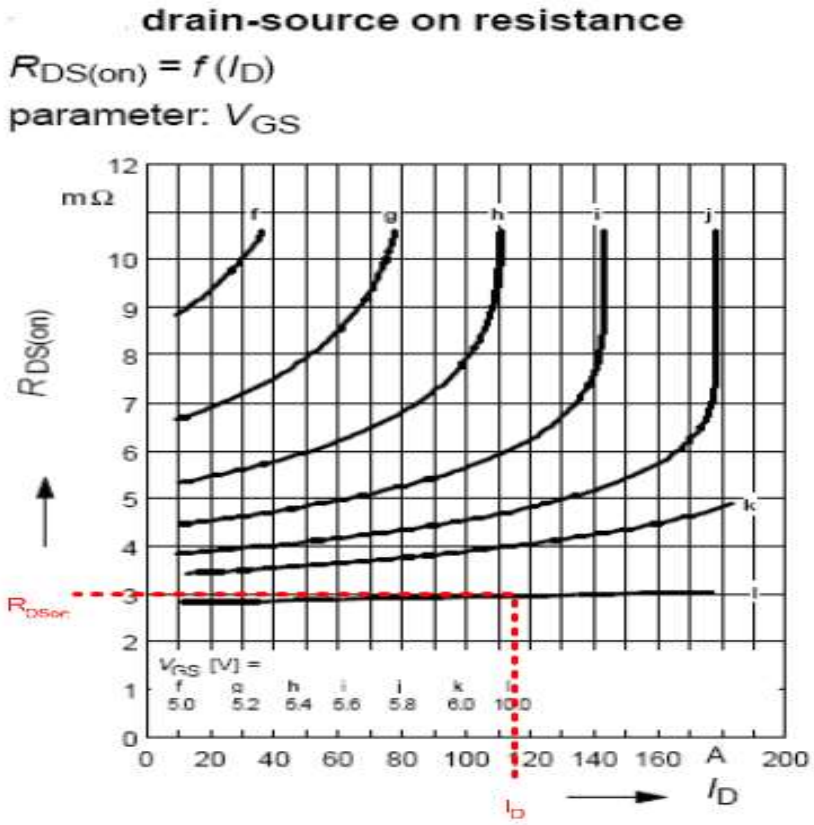


Fig. 5.2. SG MOSFET approximation graph.

From the Figure 5.2, ON-resistance can be found by using the drain current of the MOSFET from the class-B power amplifier circuit. Switching devices in class-B power amplifiers plays an essential role in power amplification [7]. Hence the instantaneous power through the MOSFET when a power amplifier is conducting is determined as:

$$P_C(t) = V_{DS}(i_D) \times i_D(t) = R_{DSon} \times i_D^2(t) \tag{5.4}$$

Calculating the total losses in the circuit of class-B power amplifier, instantaneous power losses through each MOSFET must be integrated to get an average of power losses in the circuit as follows:

$$P_{Conduction} = \frac{1}{T_{SW}} \int_0^{T_{SW}} P_C(t)dt = \frac{1}{T_{SW}} \int_0^{T_{SW}} \left( R_{DSon} \times i_D^2 \right) dt = R_{DSon} I_{Drms}^2 \tag{5.5}$$

where $T_{sw}$ is the period of an input signal and switching frequency and $I_{D,\mathrm{RMS}}$ is the drain RMS current at the output stage of a class-B power amplifier [105]. To determine the conduction losses of a class-B power amplifier, drain current have been measured from the class-B power amplifier circuit and it was found to be approximately 10 A from the DC biasing source at a low AC input signal having a frequency of 1 kHz with an amplitude voltage of 1 Vrms. Using this drain current to determine the ON-Resistance from the MOSFET approximation graph from Figure 5.2, it was analyzed to be 4 mΩ at atmospheric temperature. Using ON-Resistance conduction, power loss through each MOSFET can be calculated as follows:

$$P_{Total} = P_{C1} + P_{C2} = 0.4W + 0.4W = 0.8W \tag{5.6}$$

Therefore, total conduction power loss through each MOSFET when conducting is calculated as follows, assuming that the same power is the same as the second MOSFET:

$$P_{Total} = P_{C1} + P_{C2} = 0.4W + 0.4W = 0.8W \tag{5.7}$$

$$P_{Total} = 0.8\ W$$

Hence 0.8 W power is the total conduction power losses caused by each MOSFET in the circuit of the class-B power amplifier when it is conducting fully ON.

### 5.1.3 Static (quiescent) Losses

The power loss of semiconductors without an input signal and the load is the result of its Q-point current and voltage [106]. This section looks at the power losses when there is no input signal and the load is connected at the power amplifier's output stage. This is done by looking at the circuit components which contribute to designing the class-B power amplifier, i.e., input stage, DC biasing stage of MOSFETs and output stage. Figure 5.5 shows a class-B power amplifier with SG MOSFET without input.

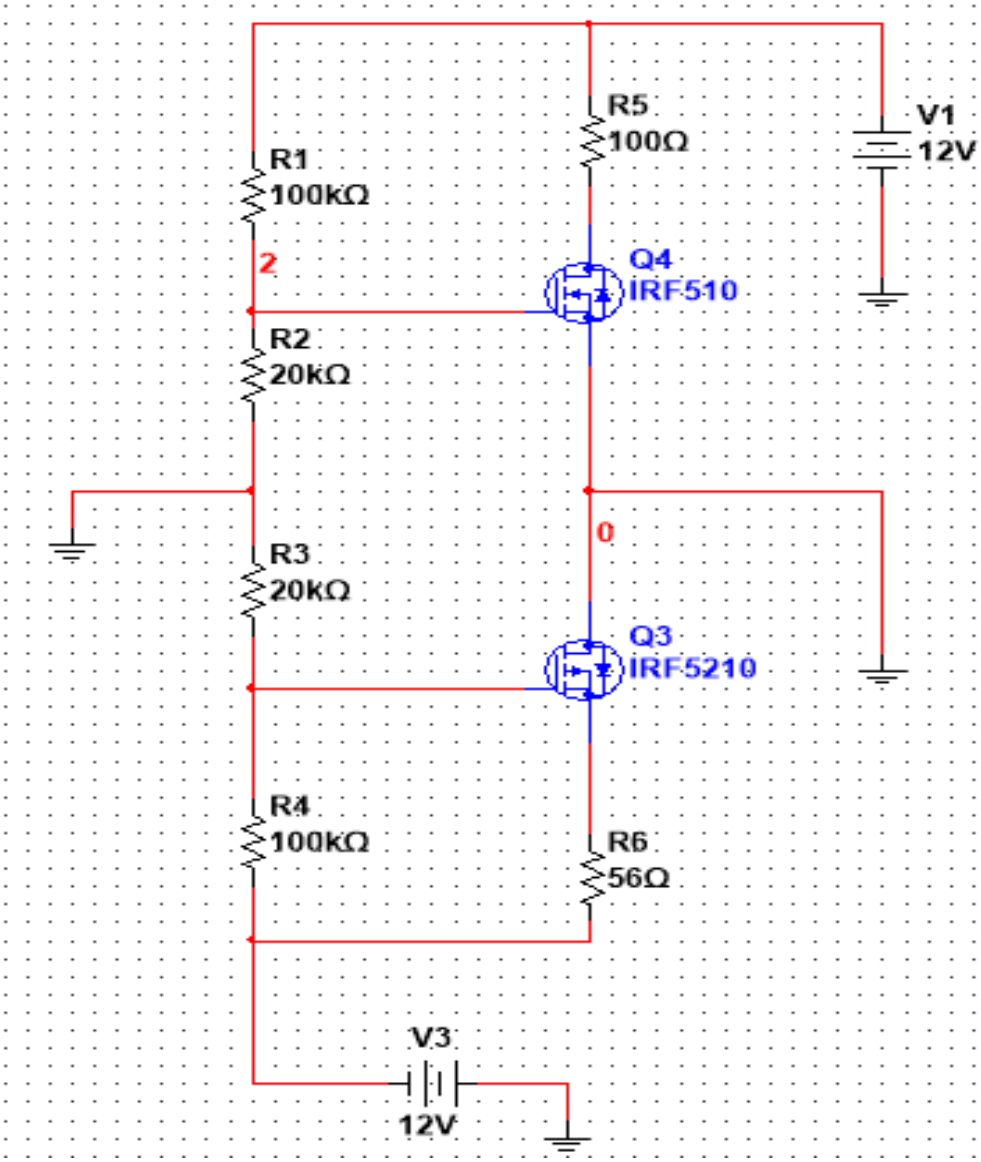


Fig. 5.3. Class-B power amplifier at the quiescent stage.

From Figure 5.3, power losses can be calculated when no input signal and load are connected to the power amplifier [107]. This is done by measuring drain current through each SG MOSFET and gate-source voltage which drives each MOSFET to turn-ON and -OFF.

The gate-drive losses are likewise static losses since they are needed to turn the FETs ON and OFF. In Figure 5.3, the method of biasing the gate of MOSFET was to use the voltage divider rule so that each MOSFET can conduct when the input signal is applied to the power amplifier. Eq. (5.8) has been used to calculate power to the load when there is no input signal and no load connected to the power amplifier's output:

$$P_{Quiescent} = V_{DS} \times I_D \tag{5.8}$$

where $I_D$ is the drain current of a MOSFET and $V_{DS}$ is a drain-source voltage. The drain current from this equation is calculated as:

$$I_D = \frac{V_{GS}}{R_{DSon}} \tag{5.9}$$

Gate-source voltage is measured from the circuit from Figure 5.4 using a multism software tool called multimeter. Figure 5.4 shows the measured gate voltage from the power amplifier circuit. Gate-source voltage is measured as 3.6 V, using the datasheet of a SG MOSFET to find the ON-resistance of a MOSFET. Figure 5.5 shows a MOSFET approximation graph for ON-resistance knowing gate-source voltage.

It was analyzed that the gate-source voltage is 3.6 V from Figure 5.5; hence drain current can be calculated because knowing the gate-source voltage, ON-resistance can be read from the graph in Figure 5.5. The gate-source voltage was 3.6 V. Therefore, ON-resistance is approximately 0.15 Ω at atmospheric temperature.

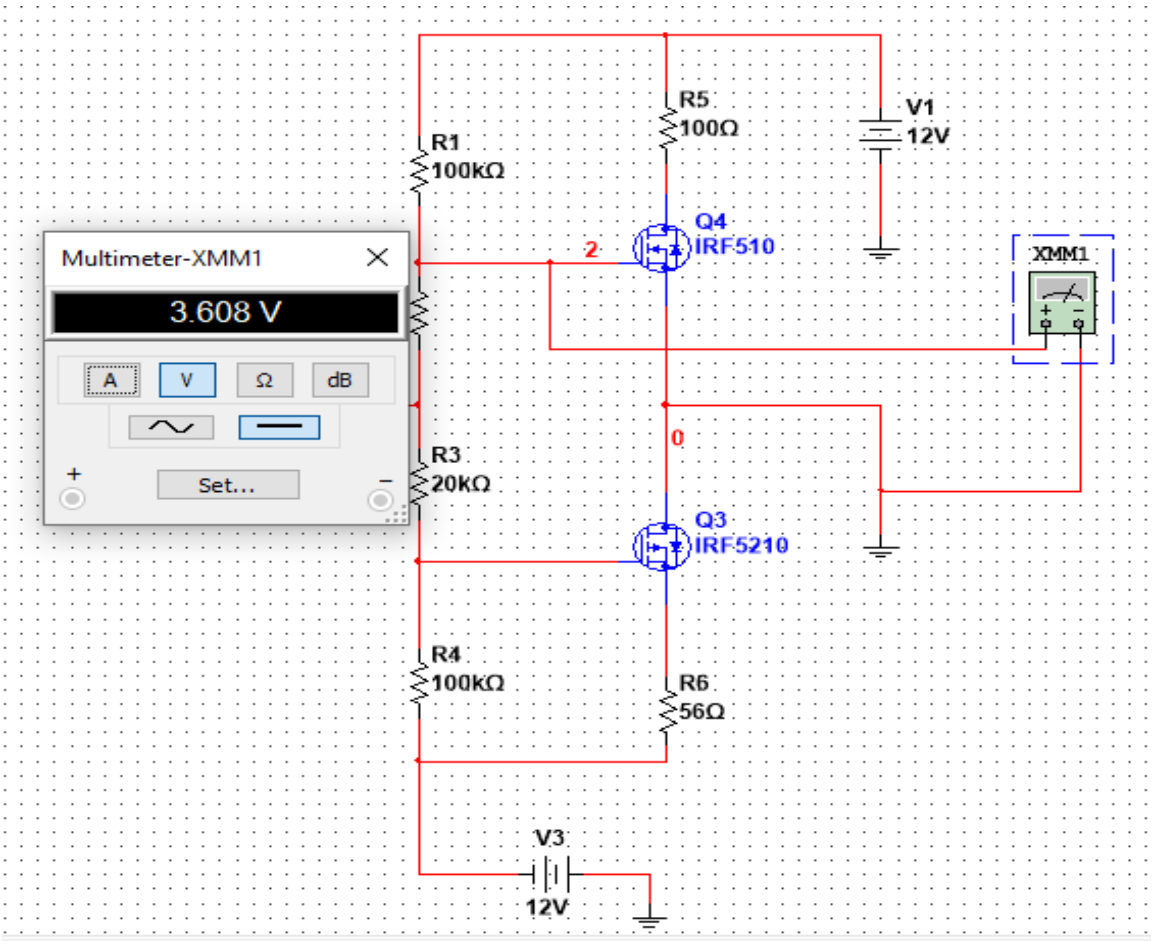


Fig. 5.4. Class-B power amplifier gate voltage at the quiescent condition.

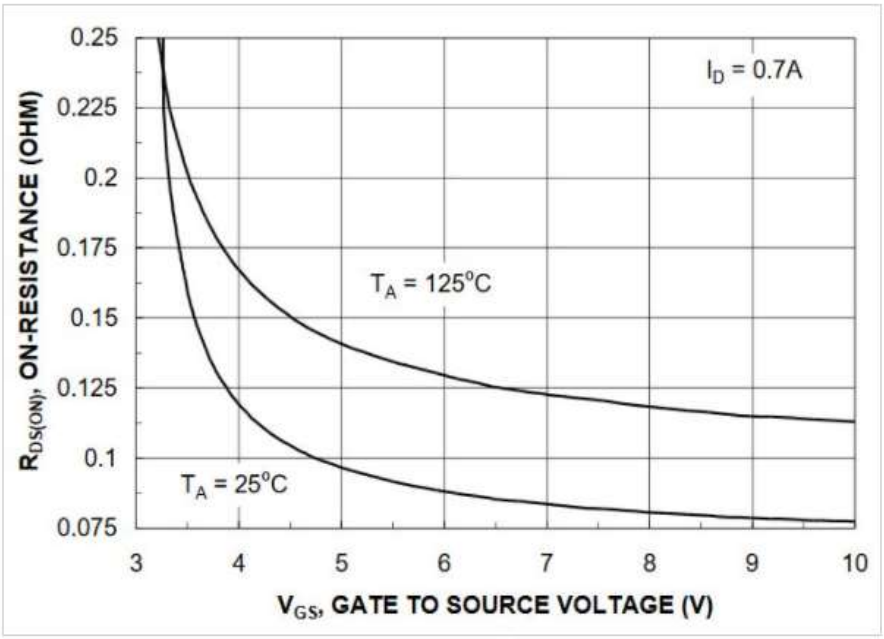


Fig. 5.5. SG MOSFET ON-resistance approximation graph.

### 5.1.4 Static (quiescent) Losses

The power loss of semiconductors without an input signal and the load results from its Q-point current and voltage. This section looks at the power losses when there is no input signal and the load is connected at the power amplifier's output stage. This is done by looking at the circuit components which contribute to designing the class-B power amplifier, i.e., input stage, DC biasing stage of MOSFETs and output stage. Figure 5.6 shows a class-B power amplifier with SG MOSFET without input.

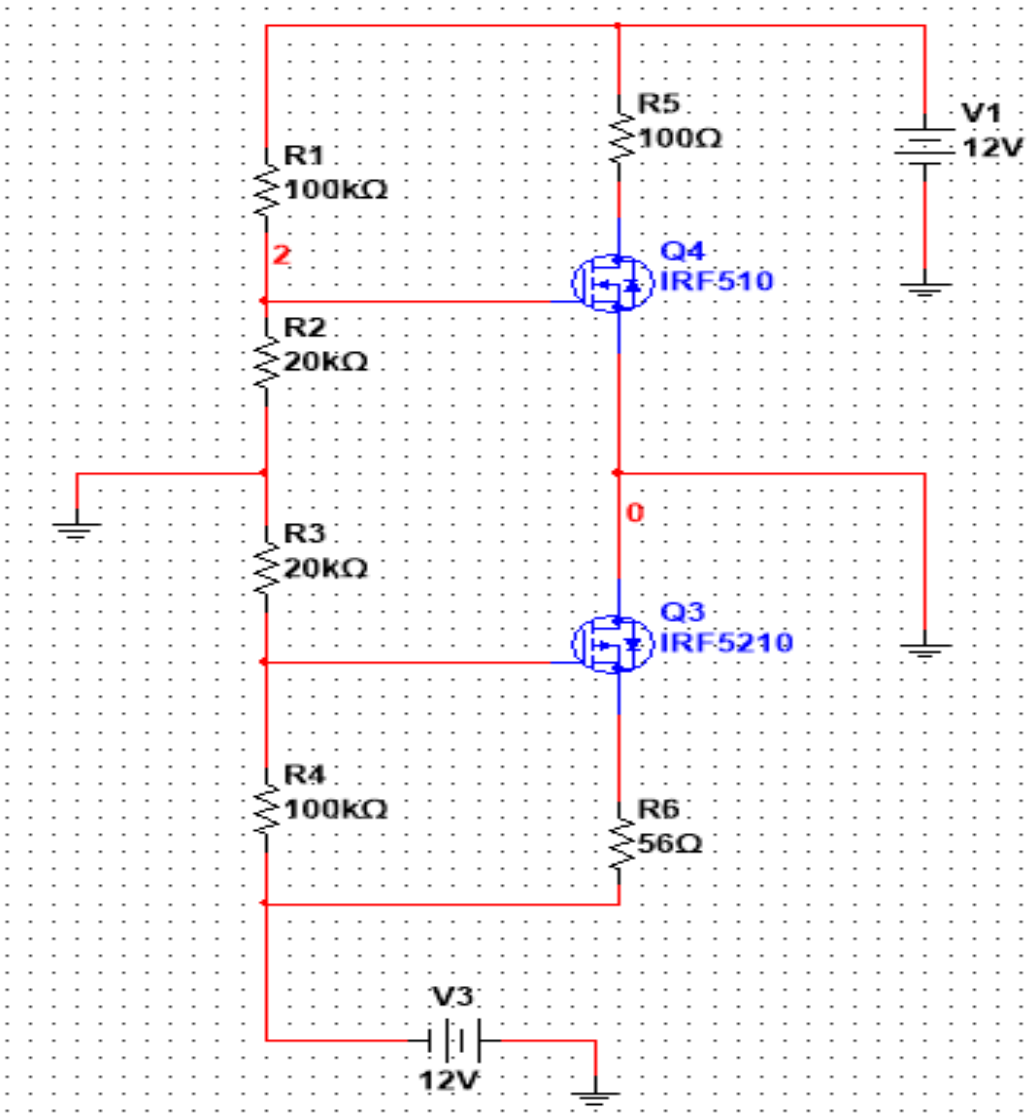


Fig. 5.6. Class-B power amplifier at the quiescent stage.

From Figure 5.6, power losses have been calculated when there is no input signal and load connected to the power amplifier. This is done by measuring the drain current through each SG MOSFET and gate-source voltage which drives each MOSFET to turn-ON and -OFF. The gate-drive losses are likewise static losses since they are needed to turn the FETs ON and OFF. In Figure 5.6, the method of biasing the gate of MOSFET was to use the voltage divider rule so that each MOSFET can conduct when the input signal is applied to the power amplifier. Eq. (5.10) is used to calculate power to the load when there is no input signal and no load connected to the output of the power amplifier:

$$P_{Quiescent} = V_{DS} \times I_D \tag{5.10}$$

where $I_D$ is the drain current of a MOSFET and $V_{DS}$ is a drain-source voltage. The drain current from this equation is calculated as:

$$I_D = \frac{V_{GS}}{R_{DSon}} \tag{5.11}$$

The gate-source voltage is measured from the circuit in Figure 5.6 using a multism software tool called a multimeter. Figure 5.7 shows the measured gate voltage from the power amplifier circuit.

Gate-source voltage is measured from the circuit, and it was analyzed to be 3.6 V, using the datasheet of a SG MOSFET to find the ON-Resistance of a MOSFET. Figure 5.8 shows a MOSFET approximation graph for ON-Resistance knowing gate-source voltage.

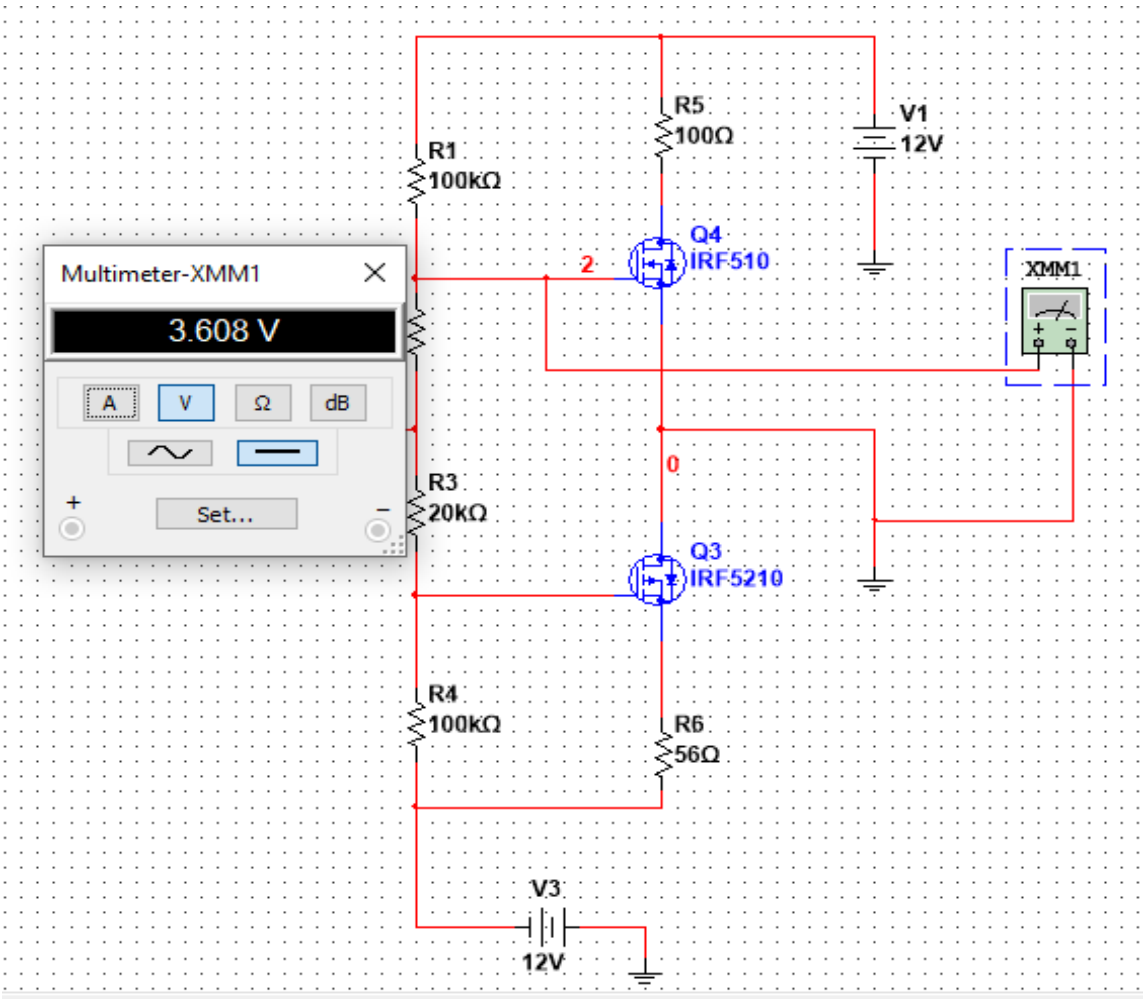


Fig. 5.7. Class-B power amplifier gate voltage at the quiescent condition.

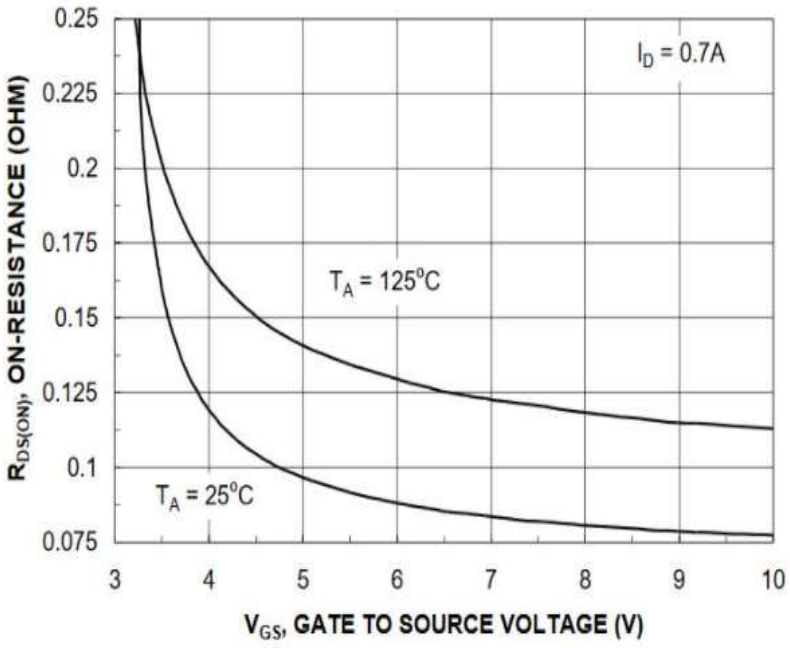


Fig. 5.8. SG MOSFET ON-resistance approximation graph.

It was analyzed that the gate-source voltage is 3.6 V from Figure 5.8, hence drain current can be calculated because knowing the gate-source voltage, ON-resistance can be read from the graph in Figure 5.8. The gate-source voltage was analyzed to be 3.6 V, hence ON-resistance is approximately 0.15 Ω at atmospheric temperature. Therefore, the drain current is calculated as:

$$I_D = \frac{V_{GS}}{R_{DSon}} = \frac{3.6}{0.15} = 24A$$

Measuring drain voltage through each MOSFET from Figure 5.7 it was measured that for the second MOSFET, which is responsible for the negative path of the input signal is approximately 0.12 V when there is no input signal and the second MOSFET it was found to 0.29 V. In contrast, drain currents were kept constant at 24 A as calculated due to the same biasing method [108]. The drain current for each MOSFET is the same due to the same biasing method that was used to bias each MOSFET; hence the power loss is then calculated as the sum of power through each of the MOSFET as follows:

$$P_{Total} = P_{LQu1} + P_{LQ2} \tag{5.12}$$

where $P_{LQu1} + P_{LQu2}$ are the quiescent power for both MOSFET of the class-B power amplifier. Therefore, the total power is then calculated as:

$$P_{Total} = P_{LQu1} + P_{LQ2} = 24A \times 0.29V - 24A \times 0.12A = 4.1W$$

Therefore, the total power loss when there is no input signal and no load connected to the class-B power amplifier is calculated and measured as 4.1 W.

## 5.2. Losses of Class-B Power Amplifier with DG MOSFET

Double-Gate (DG) MOSFET plays a crucial role in improving the performance of class-B power amplifiers, not only in class-B power amplifiers but also in many aspects of electronic devices or electronic systems. This section focuses on determining the effect of using DG MOSFET in class-B power amplifiers in terms of power losses which may affect the strength of the output signal. Figure 5.9 shows the DG MOSFET class-B power amplifier circuit, which determines its losses.

This section is focused on two types of losses, i.e., conduction losses and static losses. This type of loss plays a vital role in power amplification, and they need to be minimized so that the efficiency of the power amplifier can be maximized.

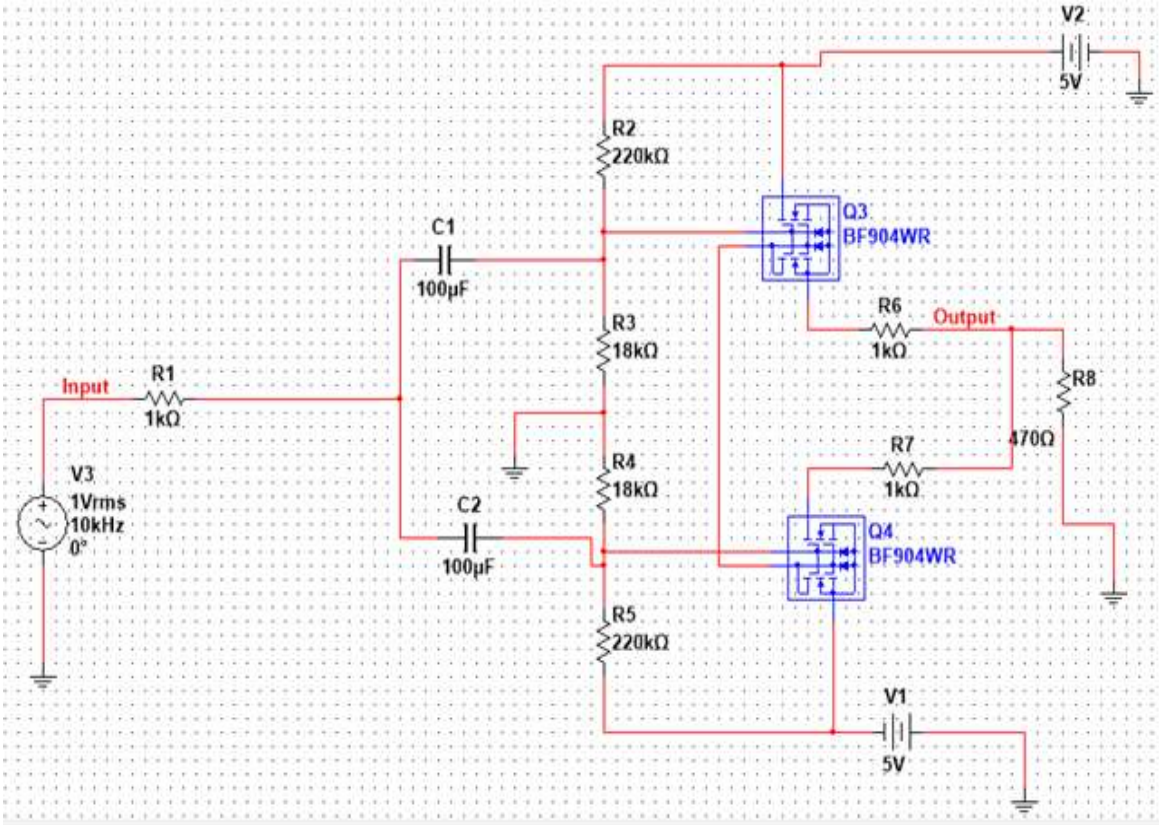


Fig. 5.9. Class-B power amplifier with DG MOSFET.

### 5.2.1 Conduction Losses of DG MOSFET Power Amplifier

Conduction losses occur when the semiconductors are fully operating at a certain region or at a certain state, i.e., active region or ON-state of the semiconductor. This section is focused on the conduction losses caused mainly by the use of DG MOSFET. Many DG MOSFET factors lead to various performances of using DG MOSFET, i.e., temperature, internal capacitance, on-state resistance, gate-drive voltages, drain current, etc.

$$P_{Conduction} = P_{Q3} + P_{Q4} \tag{5.13}$$

Conduction losses are calculated by summing the total power loss through each of DG MOSFET as shown in Eq. (5.13), i.e., conduction power loss through DG MOSFET $Q_3$ and power loss through DG MOSFET $Q_4$:

$$P_{Conduction} = \frac{1}{T_{SW}} \int_0^{T_{SW}} P_C(t)dt = \frac{1}{T_{SW}} \int_0^{T_{SW}} \left( R_{DSon} \times i_D^2 \right) dt = R_{DSon} I_{Drms}^2 \tag{5.14}$$

The conduction losses equation of DG MOSFET, when used in class-B power amplifier, is the same as the conduction losses for SG MOSFET. One of the main essential ways to get the actual conduction losses is to measure real values of the circuit directly when it is operating for amplification purposes like estimating drain current and also gate-source voltage. Not all the components can be measured directly from the circuit when it is operating, but some are measured by reading the datasheet of the device. Figure 5.10 shows the DG MOSFET approximation knowing gate-source-1 voltage.

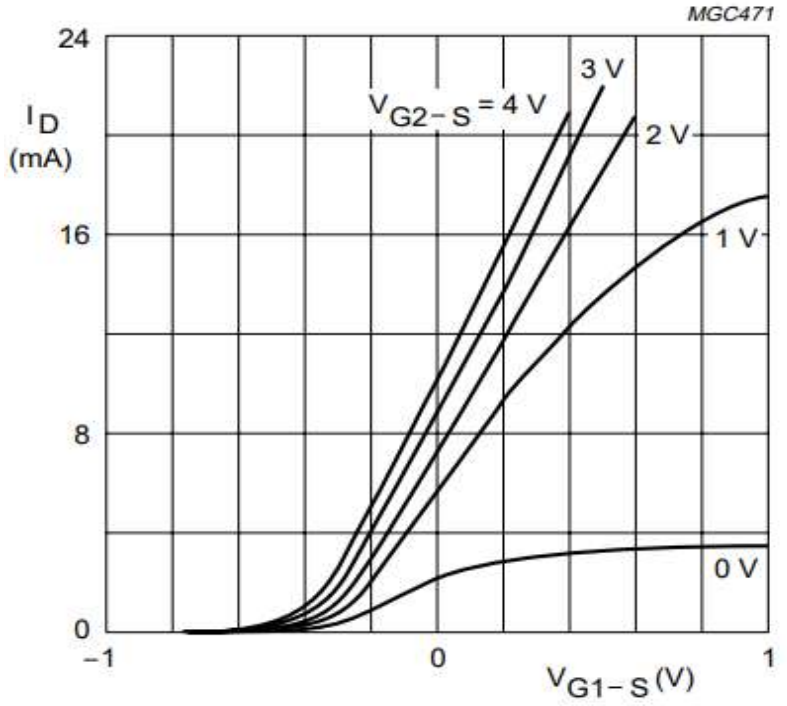


Fig. 5.10. Gate-source DG MOSFET approximation.

The gate-1 source voltage is measured from the circuit in Figure 5.7, so the drain current is calculated using the graph in Figure 5.10, when an AC input signal is applied to the circuit with an amplitude of 1 V peak-to-peak and a frequency of 1 kHz.

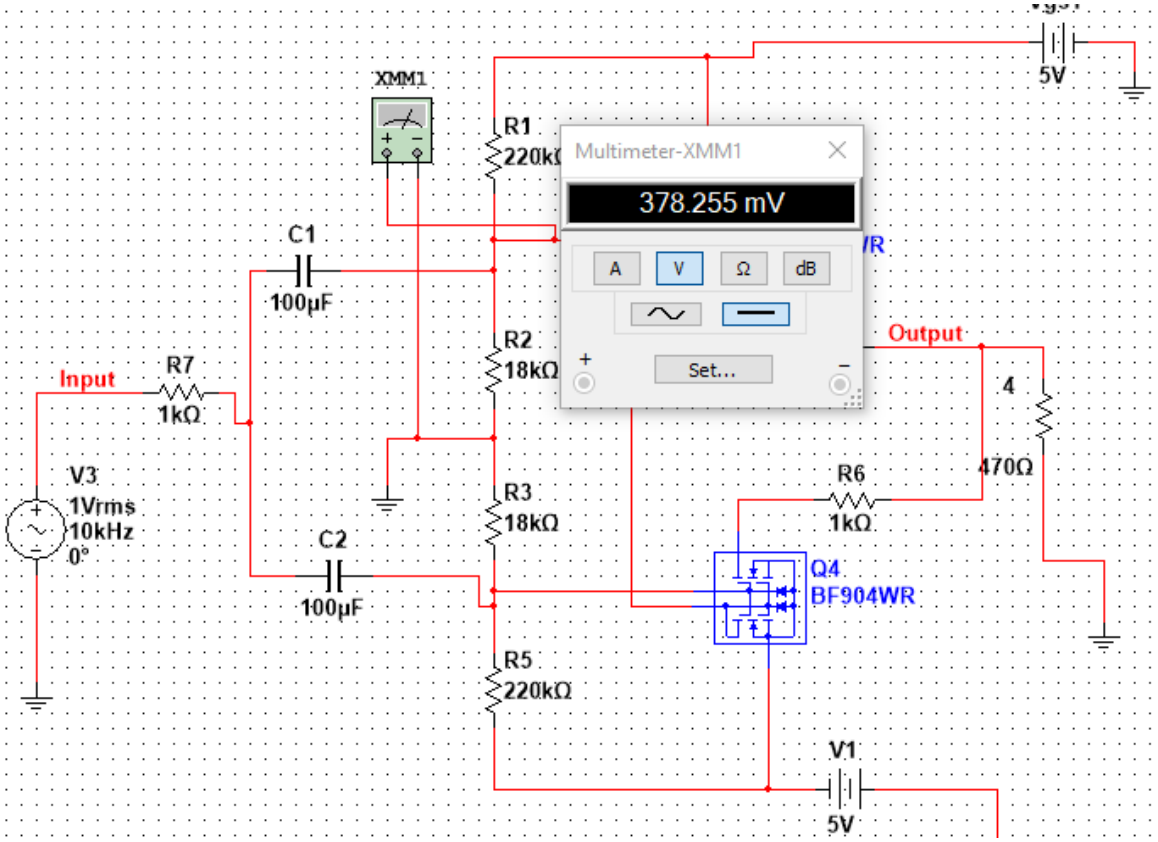


Fig. 5.11. Class-B power amplifier with DG MOSFET gate-1 source voltage.

This voltage of 378 mV was measured in the circuit of class-B power amplifier with DG MOSFET, it was also used to approximate the drain current of each DG MOSFET to calculate each conduction loss through each semiconductor. Using Figure 5.10 from the datasheet of DG MOSFET, the drain current was estimated to be 0.15 A when gate-2 source voltage was fixed biased at 2 V. The ON-resistance approximation from Figure 5.11 was also used to estimate the ON-state resistance of DG MOSFET, because drain current is known; hence on state resistance will also be known without calculating it and it was realized as 17 mΩ. Using these parameters, conduction power losses can be calculated as:

$$P_{Conduction} = R_{DSon} I_{Drms}^2 = 0.017 \times 0.15^2 = 0.38mW \tag{5.15}$$

This power is for each DG MOSFET, to calculate the total conduction power loss through each DG MOSFET, each power must be added to the other power for the second MOSFET as:

$$P_{Conduction} = P_{Q3} + P_{Q4} = 0.38mW + 0.38mW = 0.76mW \tag{5.16}$$

Therefore, when fully conducting, 0.76 mW is the total conduction power loss through DG MOSFET. The majority of the power is in the MOSFET gate driver. Gate-drive losses depend on the input signal's frequency and are a component of the gate capacitance of the DG MOSFETs. When switching the MOSFET on and off, the higher gate drive losses as the switching frequency increases. This is another reason the efficiency goes down as the switching frequency increases.

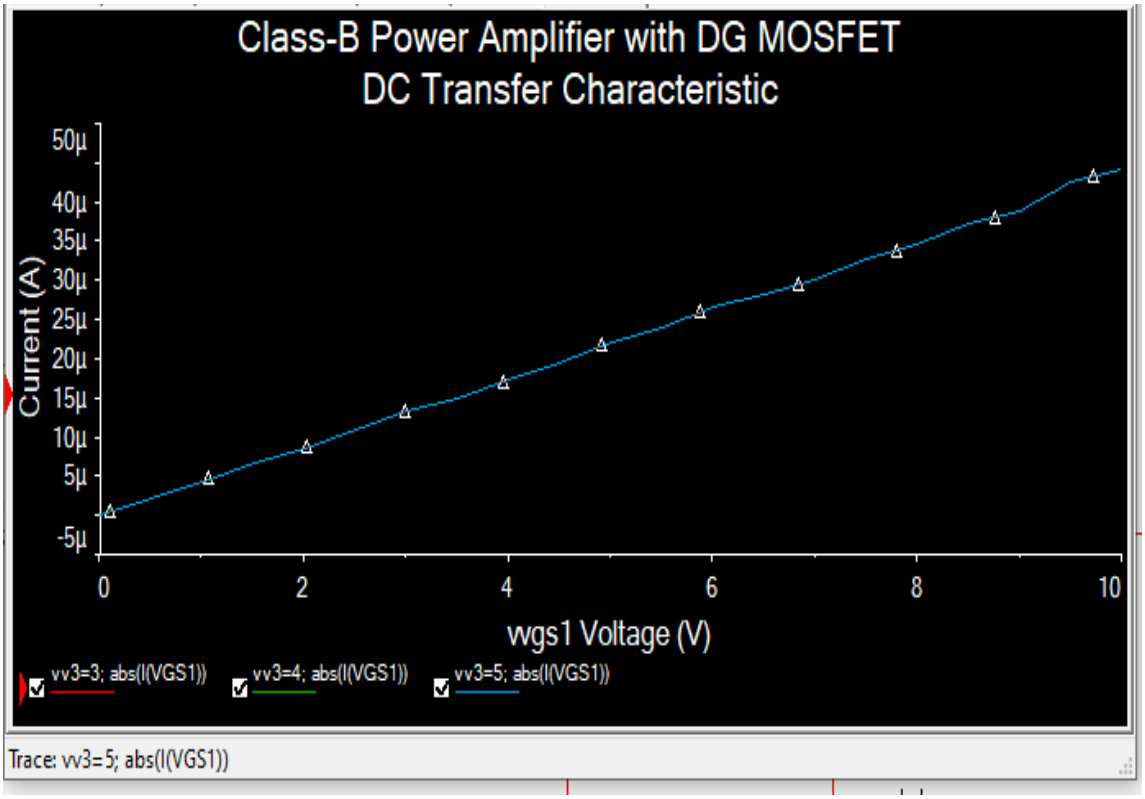


Fig. 5.12. Gate-1 source DC transfer characteristic.

Figure 5.12 shows the DC transfer characteristic of gate-1 source voltage was obtained when gate-2 source voltage was fixed biased at the voltage of 2 V. It can be shown from Figure 5.12 that as a gate-1 source voltage increases the current in the circuit also increases, this means that current in the circuit is linearly dependent to gate-1 source voltage. From Figure 5.12, both of these parameters i.e. start at zero, this is because of the operation of class-B power amplifier, meaning that there won't be any current and voltage when there is no input signal applied to the power amplifier. The conduction losses decrease as the input signal increases in value, such as amplitude and frequency.

### 5.2.2 Static (quiescent) Losses of DG MOSFET Power Amplifier

DG MOSFET in class-B power amplifier influences the output signal and those factors need to be taken into consideration when there is no input signal. These factors need to be reduced by how the power amplifier is designed. Each gate in DG MOSFET has its effect on power amplification, and these effects have to be minimized and reduced so that the output signal can have high strength in output power. This section considers losses when there is no input signal and the simulation of each gate to source effects.

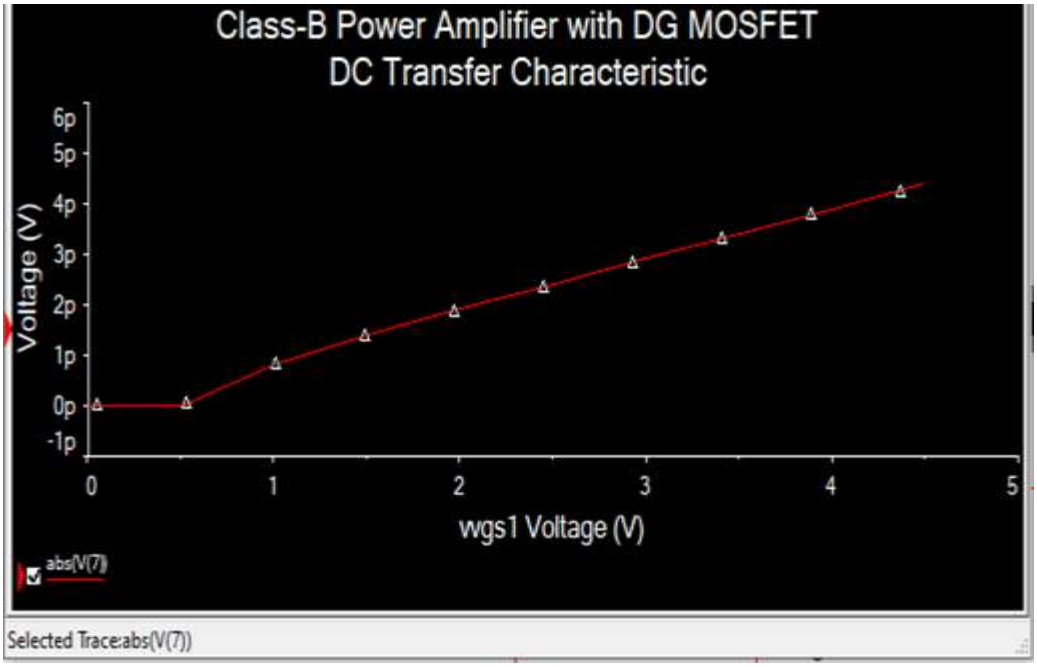


Fig. 5.13. The quiescent voltage of class-B power amplifier with DG MOSFET.

Both the DG MOSFET is partially conducting when no input signal is applied to the power amplifier. Figure 5.13 shows the relationship between the gate-1 source voltage when the gate-2 source voltage is fixed biased to 5 V as a function of the gate-1 source voltage. From Figure 5.13, it can be shown that when the gate-1 source voltage is zero, the output voltage loss is also 0 V, as a gate-1 source voltage increases, the voltage loss through DG MOSFET also increases.

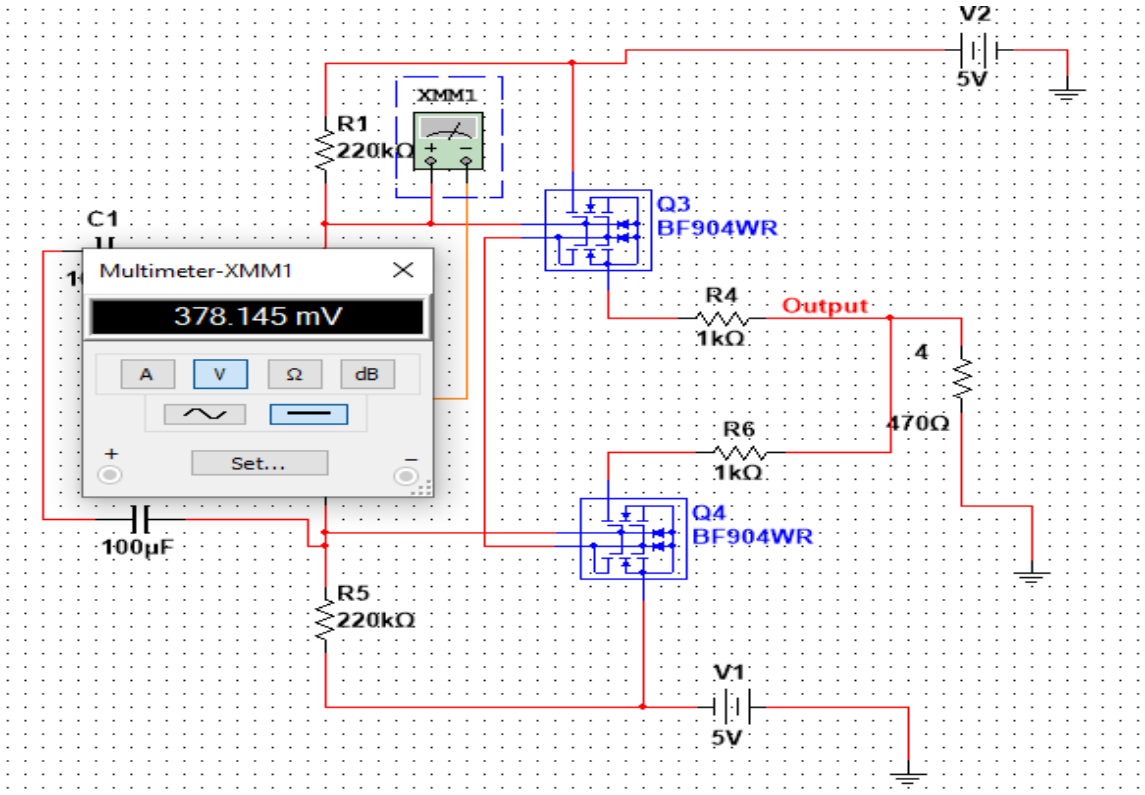


Fig. 5.14. DG MOSFET class-B power amplifier at the quiescent stage.

These voltage loss starts to occur when the gate-1 source is approximately 0.5 V as seen in Figure 5.14, and they are directly proportional to the losses through the DG MOSFET. From figure 5.14 the minimum voltage at each gate of DG MOSFET was measured to be 378.145mV at the quiescent stage. Using the following equation, static power loss can be calculated as:

$$P_{Quiescent} = V_{DS} \times I_D = 378.145mW \times 0.1A = 0.037W$$

Hence the total static loss through each DG MOSFET is 0.037W due to the use of two semiconductors. These voltage losses are minimal say in a range of pV, which concludes that the loss of DG MOSFET is limited and is of good use in Power Amplification. It was found that each quiescent power loss through each DG MOSFET is 0.037 and due to the structure of class-b power amplifier meaning that there is two DG MOSFET used, hence summing each quiescent power loss we get the total power of 0.074 W

### 5.2.3 Switching Losses of DG MOSFET Class-B Power Amplifier

Switching losses happen when the semiconductor changes from the blocking state to the conducting state and the other way around [18]. This interval is described by a huge voltage across its terminals and a huge current through it. The energy dissipation in each progress (i.e., transition from ON-state to OFF-state) should be multiplied by the frequency to get the switching losses:

$$P_{SW} = E_{MOSFET} \times f \tag{5.18}$$

Eq. (5.18) describes the amount of energy loss when a power amplifier is fully operating; the total energy is then multiplied by the input signal's frequency (i.e., time). The time it takes for the power amplifier to amplify the input signal is separated into two i.e. the time for the first DG MOSFET when it is conducting for the positive path of a sinusoidal input signal and the time for the second DG MOSFET to conduct for the negative path of the sinusoidal input signal. To get the total power for the switching loss =, the amount of energy dissipated into heat is multiplied by the frequency of the input signal or the frequency (time) for the input signal to be amplified at the output.

$$P_{SW} = E_{MOSFET} \times f \tag{5.19}$$

where $E_{MOSFET}$ is the energy dissipation through each MOSFET and $f$ is the input signal frequency. Multiplying this equation, we get the same usual power without considering the frequency of the input or assuming that the frequency does not change at all.

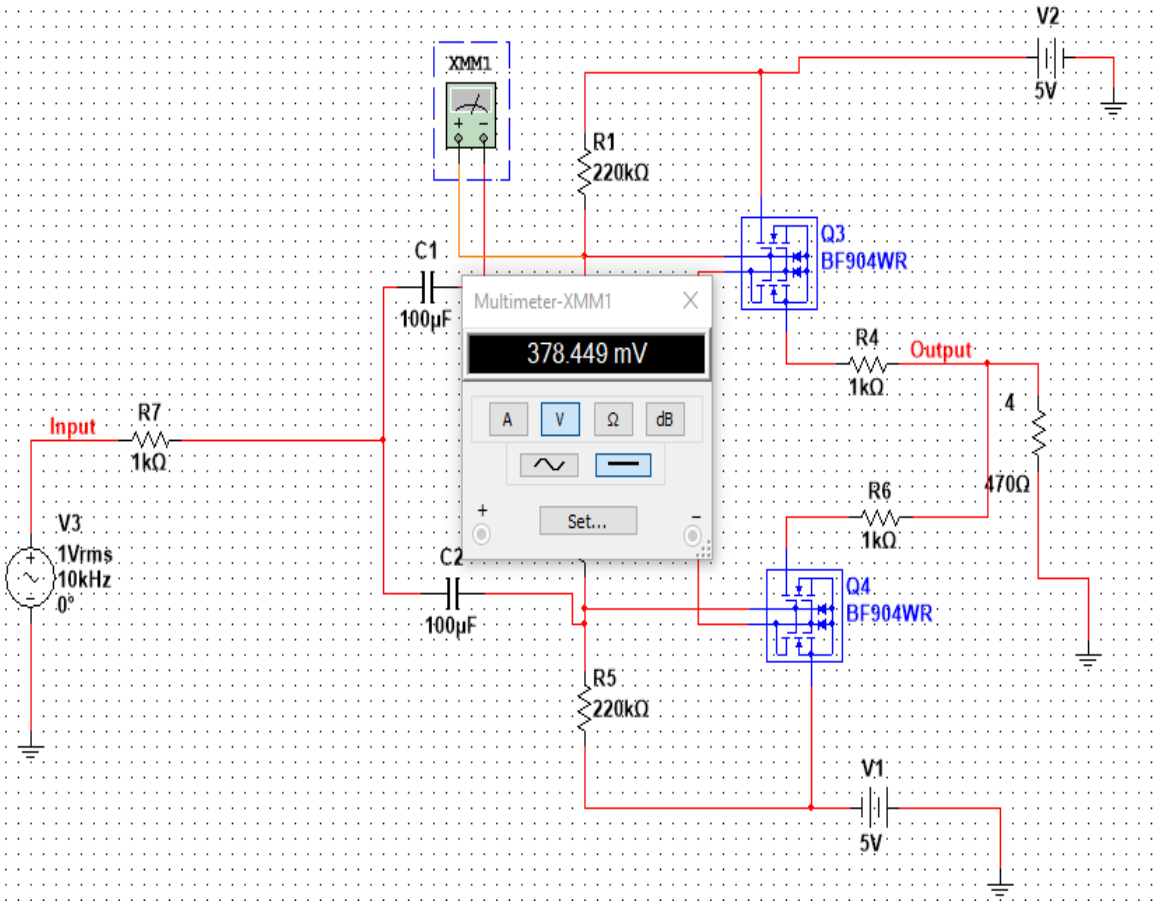


Fig. 5.15. Class-B power amplifier with the input signal.

Figure 5.14 shows a power amplifier with DG MOSFET when an AC signal is applied to it and measuring gate-1 source voltage. The obtained DC gate-1 source voltage, which is driving the DG MOSFET was 378.44 mV and the drain current at this stage is 0.2 A and calculating the power using the frequency of an input signal, assuming that the time used to calculate energy is inverse of the input signal, and it does not change.

$$P_{SW} = E_{MOSFET} \times f = 378.449mV \times 0.2A \times 1kHz = 0.075mW \quad (5.20)$$

This is the amount of switching loss through each DG MOSFET when the power amplifier is applied with an input signal that has a voltage amplitude of 1 V and a frequency of 1kHz. The switching power loss obtained through each DG MOSFET is 0.075 mW.

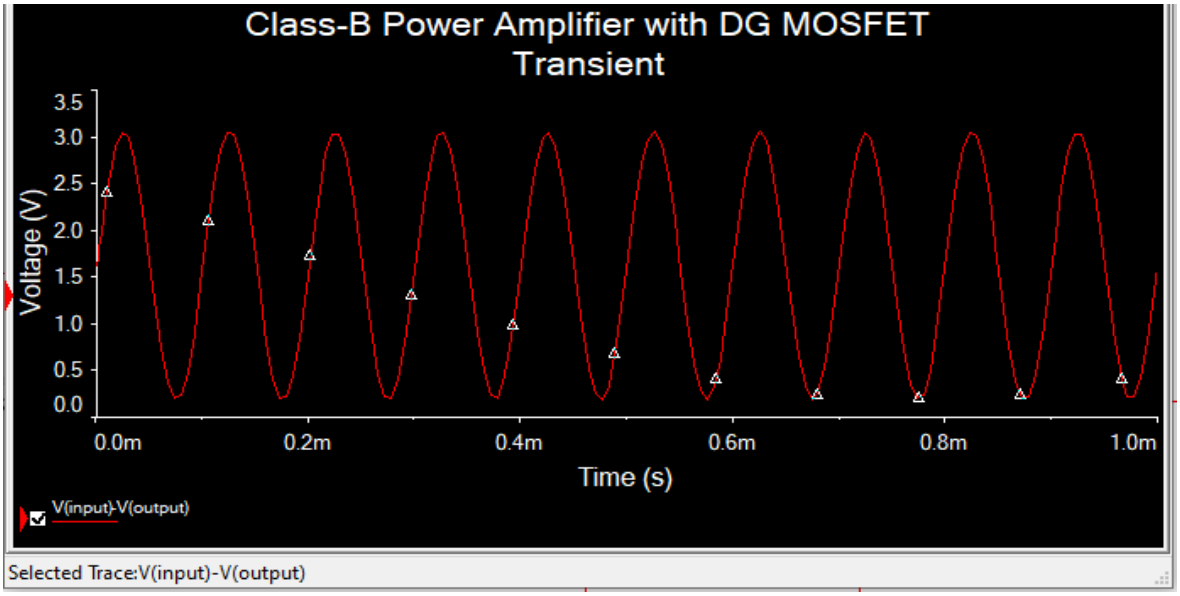


Fig. 5.16. Transient analysis of class-B power amplifier.

Using the result of Figure 5.14 to calculate the switching power loss using the same parameters obtained i.e. gate-1 source voltage of 378.449 mV and drain current of 0.2 A but changing the frequency or time of the input signal and replace it with the time it takes for a power amplifier to amplify the input signal from the Figure 5.15, the switching losses have also been calculated and tabulated in Table 5.1.

Table 5.1. Comparative analysis of model

| **Parameter** | **Conduction loss** | **ON-Resistance** | **Static (quiescent) Losses** | **Switching losses** | **Output Circuit Impedance** | **Input Signal frequency (kHz)** | **Gain (V/V)** | **R** |
|---|---|---|---|---|---|---|---|---|
| **Single-Gate MOSFET** | 0.80 W | 0.004 mΩ | 4.1 W | X | Low | 1 | 2 | |
| **Double-Gate MOSFET** | 0.76 mW | 0.017 mΩ | 0.074 W | 0.15 mW | Low | 1 | 2 | 19 kΩ |

### 5.2.4 Losses of Class-B Power Amplifier Discussion

Power losses were analyzed with the aid of each semiconductor datasheet, and it was realized using DG MOSFET is better in reducing conduction power losses. It was analyzed that the conduction power loss of class-B power amplifier with the use of DG MOSFET is less compared to that conduction loss of class-B power amplifier with SG MOSFET. The conduction loss of class-B power amplifier with DG MOSFET was 0.76 mW and the conduction loss of class-B power amplifier with SG MOSFET was 0.80 W which is higher than the DG MOSFET power amplifier. This is because semiconductors such as SG MOSFET have less capacitance compared to DG MOSFET, hence in SG MOSFET, more power is absorbed from the input source to drive or deliver power to the load.

## 5.3 Conclusion

Losses in the circuit of class-B power amplifier were conducted and it was found that to reduce circuit losses, high-value resistors must be used due to ohms law. If high resistors are used, a small current will be drawn from the input signal and power will be reduced. Reducing the switching transient from the ON to the OFF stage will minimize the switching power losses.

# Chapter-6

# HARDWARE DESIGN AND ANALYSIS

## 6.1 Hardware Design

The class-B power amplifier is designed with the use of electronic components such as resistors, capacitors, and various power sources. Hardware design is done by breaking a huge design into sub designs which are then integrated to form a hardware circuit of Class-B power amplifier with the use of double-gate MOSFET. The design procedure was first to get the same components as the components from the simulation design. However, the other essential devices that were needed to test the final design of the class-B power amplifier were a functional generator, oscilloscope, DC power supply, and soldering iron.

Fig 6.1 shows the design devices needed to implement, analyze, and test Class-B power amplifier input signal, DC biasing voltages and output signals. Fig 6.1 from left to right (i.e., labels A to G) shows various devices that were used to implement class-B power amplifiers. From Fig 6.1 from left to right labeled devices:

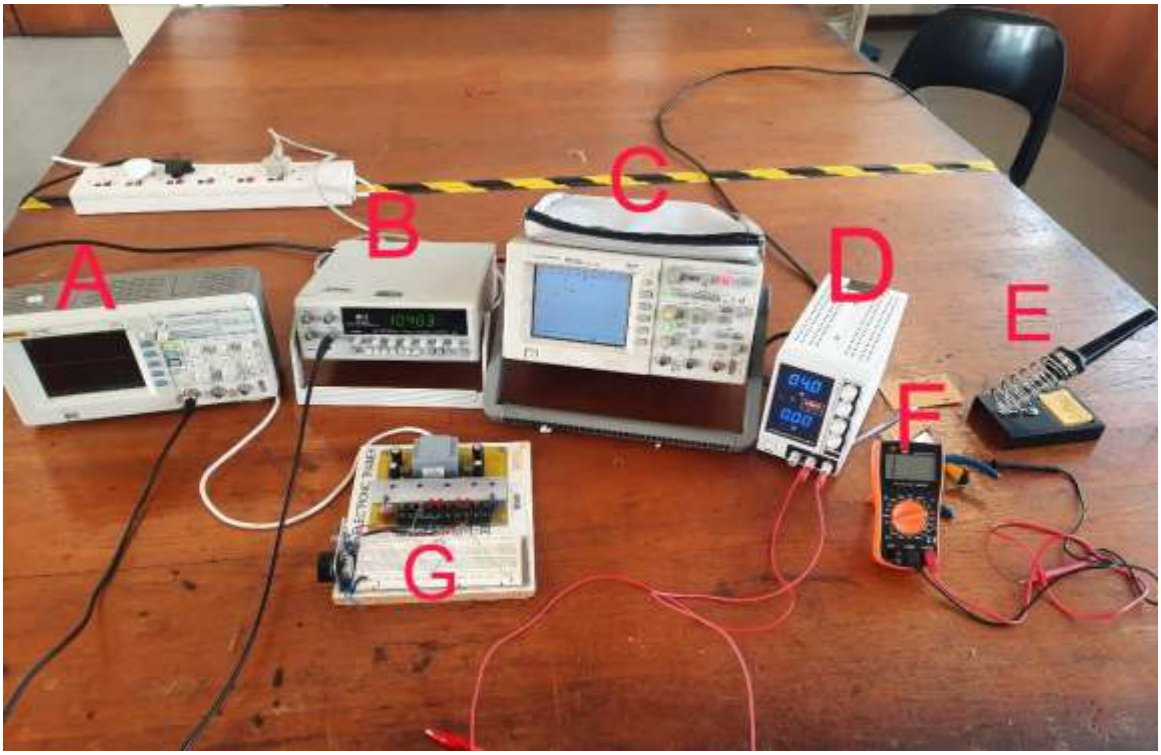


Fig. 6.1. Hardware design set-up.

A) **Oscilloscope -** it was used to analyze input waveforms and output waveforms from the output side of class-b power amplifier
B) **functional generator** – this device was used to generate various sinusoidal waveforms. Using this device, amplitude and frequency could be changed.
C) **Spectrum and Signal Analyzer** – this type of device was used to check the frequency response and analyze the frequency in the frequency domain.
D) **DC Power Supply** – dc power supply was used to fix the bias of the second gate of DG MOSFET with biasing voltage.
E) **Soldering iron** – this device was used for soldering the required components to the Vero board that was used to build a power amplifier circuit.
F) **Digital Multimeter** – A multimeter was used to measure different parameters such as voltage, current, and resistance.
G) **Electronic Trainer** – this device was used to apply positive and negative dc voltage to the drain of DG MOSFET.

After setting up the working station, the design of the circuit was done by breaking down the circuit task into subsections. These sections involve getting the required different components, soldering DG MOSFET into the Vero board, soldering resistance/voltage divider, soldering wires

Hardware design had challenges that needed to be taken into consideration, such as finding the right tools to test the implementation and building the hardware. The size of DG MOSFET is very small of which makes it hard to solder and to test it on its own accurately. DG MOSFET (BF909A215) is a self-mounted device, and it is not easy to solder it using the usual soldering machine/iron. The idea that was used to be able to break the Vero board in order to separate the tracks made it easier to be able to solder DG MOSFET due to its size, which is very small. The first design of class-B power amplifier with the use of DG MOSFET was done on a Vero board to test the biasing of DG MOSFETs and also to test the input and output waveforms. The main parameters tested are the input sinusoidal waveform and the output waveform using a function generator and oscilloscope. After designing and testing the hardware circuit of the class-b power amplifier with DG MOSFET, the simulation results and hardware results are compared and draw the conclusion. Many non-ideal effects might affect the performance of hardware design; however, they can be reduced by using different types of tools, such as designing a Printed Circuit Board (PCB). The size of DG MOSFET is very small, and it is easy to

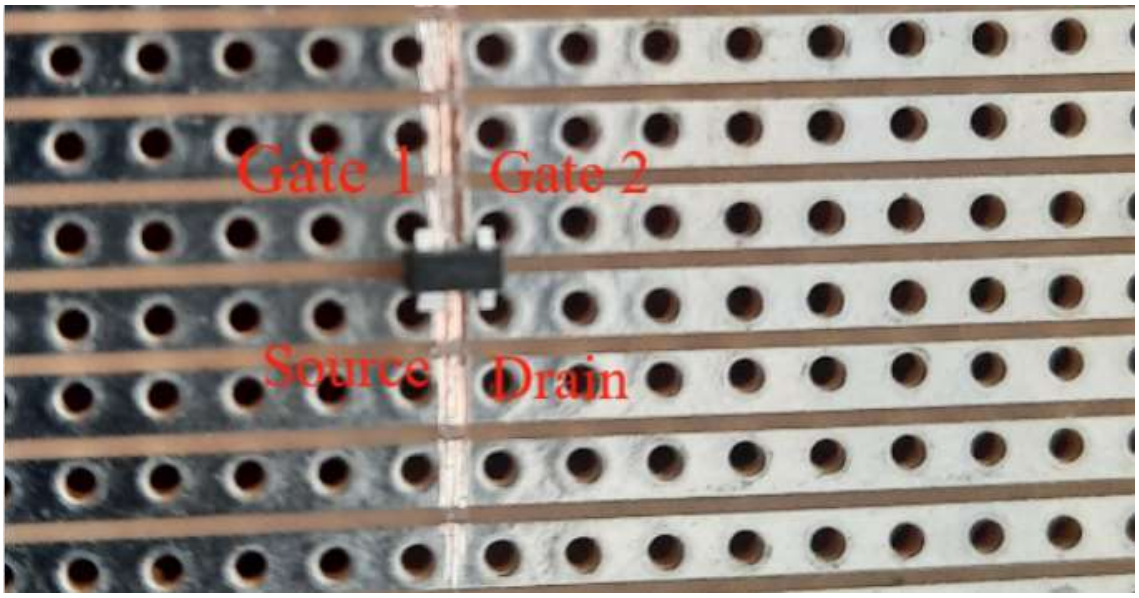


Fig. 6.2. DG MOSFET on a Vero Board.

damage a device when soldering it in the Vero board. The Fig. 6.2 shows the structure of DG MOSFET and its size of it when it is placed on a Vero board.

Vero board was cut into two boards by separating the tracks. From Fig. 6.2, the source and drain are so close to each other and gate-1 and gate-2 are also close to each other; hence tracks needed to be separated to avoid short circuits. Using a datasheet of BF909A215 type of a DG MOSFET, it is stated that the maximum operating temperature is 150℃ and the soldering iron that was used ranges from 200 ºC to 400 ºC. When soldering the BF909A215 type of DG MOSFET, it is required to be extra careful because once the soldering iron touches the body of a DG MOSFET, it can damage the device due to the maximum operating temperature. One method that was used to test of there are no short circuits from the separated Vero board, like the one on Fig 6.2 was to use a multimeter and manually test each track of the Vero board if there is no short circuit and if one is found, the board was retested and separated again.

There are several stages that were taken when designing the hardware circuit of the class-B power amplifier with the use of DG MOSFET, each stage was designed and tested before going to the next stage. If each stage failed, then that stage was redesigned and retested again. The following diagram shows the flow of how each stage of designing a fully integrated class-b power amplifier was done and tested.

Table 6.2: Description of the hardware design process

| Stage | Description | Testing | Results/Issues/Solutions |
|---|---|---|---|
| 1. Equipment | Equipment or tools that were required to implement and test the hardware design circuit | Testing this stage was done by checking that all the equipment (i.e., Functional generator, power supply, etc.) is able to supply the required DC voltage and sinusoidal waveforms | This stage was working fine without any issues, and it was supplying enough DC voltage because of an adjustable power supply and adjustable functional generator |
| 2. DG MOSFET | At this stage, DG MOSFET was mounted on the Vero Board and tested if there was nothing that causes short circuits between the tracks of Vero board. | Using a Digital Multimeter, each track was tested if a DG MOSFET connected with each track of a Vero board. | No issues were detected when testing this stage. |
| 3. Soldering both DG MOSFETs | Both switching devices i.e., DG MOSFETs, was tested on a Vero board to check if they were not damaged by high soldering iron temperature | They were tested to check if they operate at saturation region. This was done by connecting two gates, i.e., gate 1 and gate 2 and supplying DC voltage of 4 v | Each DG MOSFET was working even though the soldering wire was filled at each pin of a DG MOSFET which almost damaged the device |
| 4. Voltage Divider circuits | The voltage divider or biasing circuit of each DG MOSFET was designed with resistance and wires to | Supplying a DC voltage of 5 to the voltage divider circuit and using a digital multimeter to check if | 3.08 v was found at the output side of the voltage divider circuit, this was enough to bias the DG MOSFET. |

| | | | |
|---|---|---|---|
| | drop down DC voltage from 5 volts to 3.0 volts for each gate 1 of DG MOSFETs | 3.0 volts is found at the output side of the voltage divider circuits. | |
| 5. Back view of voltage divider circuits | The back view of the voltage diver rule was checked to see if there was no wire that causes the short circuits. | Using a Digital multimeter to check that there is no short circuit observed. | After testing this stage, it was found that it was working fine without any short circuit |
| 6 Input and Output stages | Input and output stages of the circuit were implemented by soldering wires that will make it easier for the probs of the function generator to supply waveforms and also for the oscilloscope | Supplying the input waveforms and checking if the output waveforms are found at the output stage | This was working and it first showed errors of output noise and effect on the output waveforms |
| 7 Back view of Input and Output stages | Both the input and output stages needed to be checked from the backend side of the Vero board and check the short circuits | Using a Digital Multimeter, each track of the Vero board and the wires connected to the board were tested | No errors or short circuit was found |
| 8 Final integrated Class-B power amplifier | After implementing and testing each stage from stage 1 to stage 7, integration was done to form the complete class-B power amplifier with DG MOSFET. | The oscilloscope, function generator and DC power supply were then used to test the input and output of class-B power amplifier waveforms. | The results show that the DC biasing is achieved and the waveforms were found at the output. |

Hardware design consists of 8 stages, as shown in the Fig. 6.3, each stage was tested to check if it is working before moving to the next stage. That reduces the work of troubleshooting the whole integrated circuit in case it is not working.

The final circuit of class-b power amplifier was done using a Vero board and all the components used to implement that hardware were found in stores and the school laboratory. The results of the hardware design will be compared with the simulation results and see if there is anything that might cause the change in hardware design.

The red arrow is pointing to the first DG MOSFET and the blue arrow is pointing to the second DG MOSFET, it can be seen that both devices were mounted on the Vero board and the size of these devices is very small, which made the design so hard and complicated if one is not extra careful when soldering the devices on the Vero board.

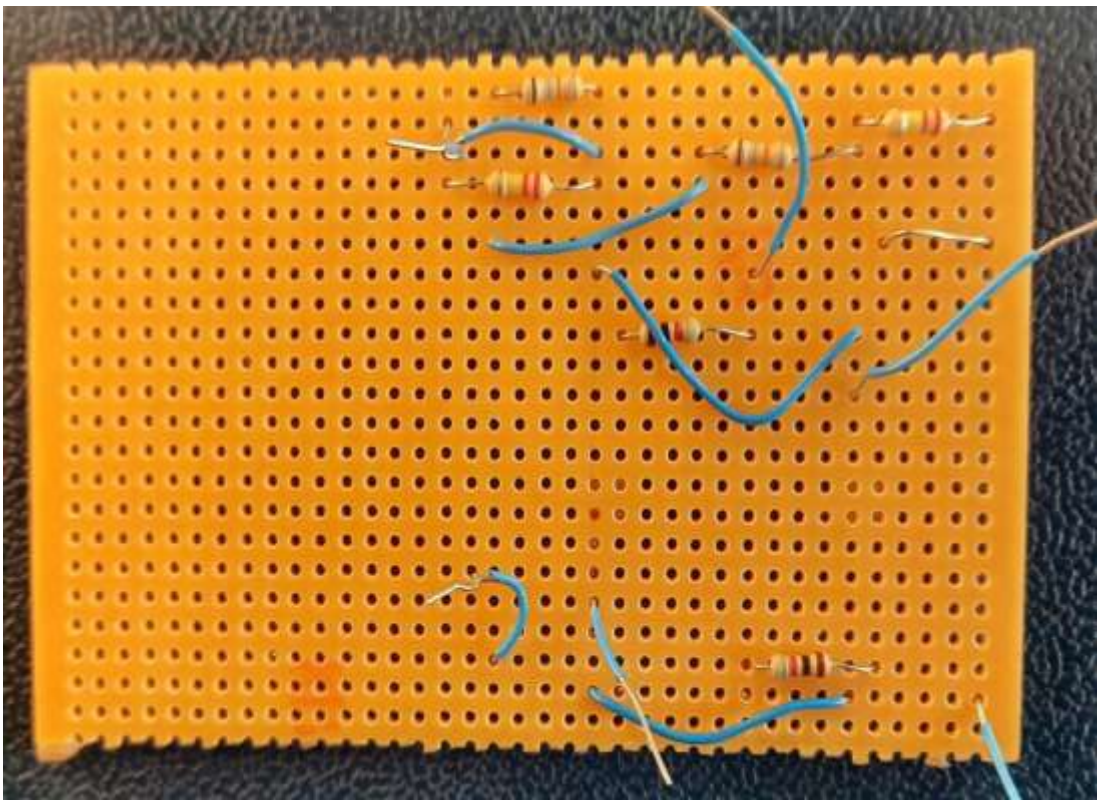

Fig 6.3. DG MOSFET based class-B power amplifier hardware circuit.

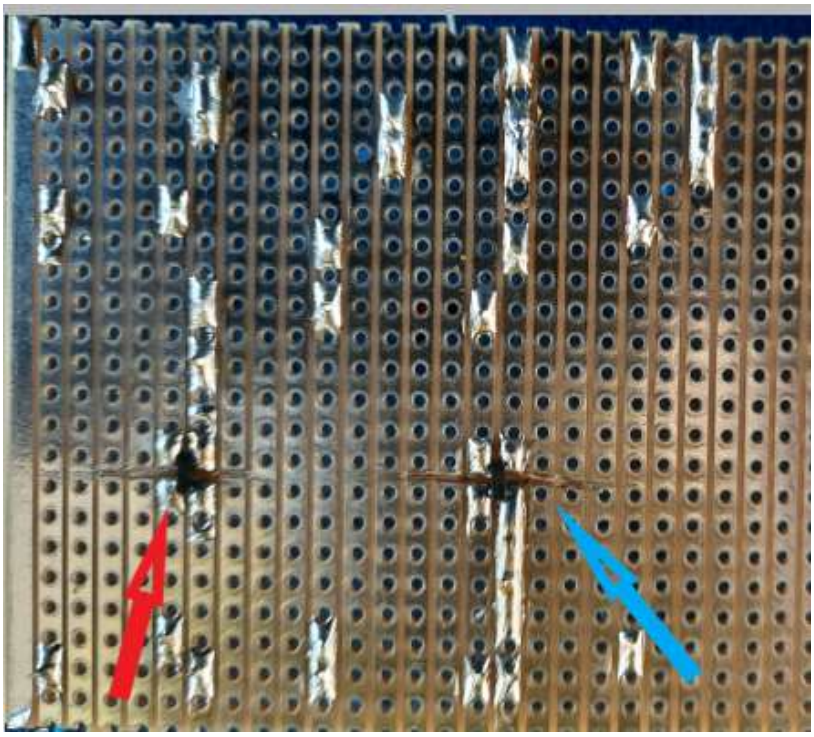

Fig 6.4. Back view of Class-B DG MOSEFs power amplifier.

## 6.2 Hardware Results

The results of hardware design were found using an oscilloscope and digital multimeter to see the difference between simulation results and hardware results. Using oscilloscope and functional generator, the first thing that was done was to check if the input waveform was a sinusoidal waveform with a certain frequency,


Fig 6.5(a) Input Frequency.

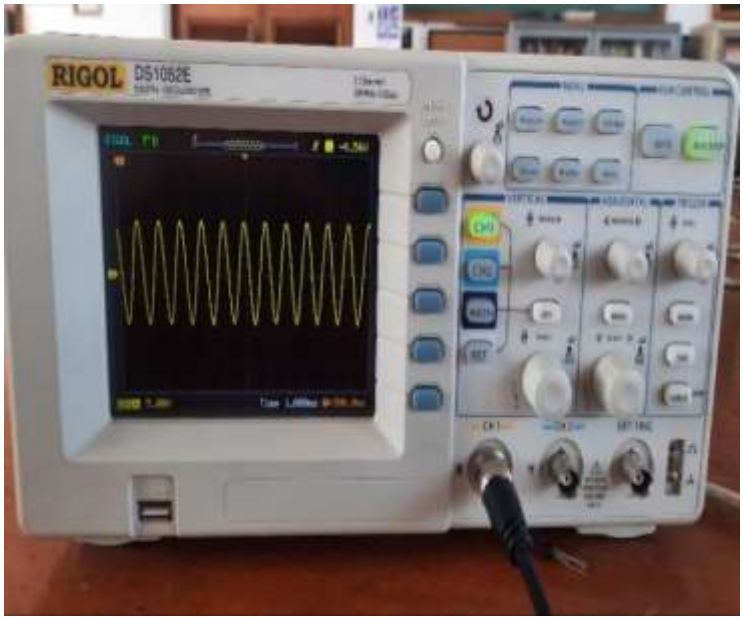


Fig 6.5(b) Waveform of an input Signal.

The input signal that was applied to the input side of class-B power amplifier was a sinusoidal waveform at a frequency of 1 kHz, as shown in Fig. 6.5(a) which shows the frequency of 997.69 Hz, which is approximately 1 kHz and Fig. 6.5(b) shows the waveform using an oscilloscope at channel-1. The output pin of the functional generator was directly connected to the input of channel-1 of an oscilloscope using channel-1 probes.

Fig. 6.6 shows three essential devices, i.e., oscilloscope with the output signal, function generator that supplies the input signal with a frequency of 1.0249 kHz, electronic trainer that was used to supply negative 5v and lastly class-b power amplifier with the use of DG MOSFET, Input signal was applied to the circuit as shown in Fig. 7.5 where an oscilloscope was used to check the output found from the output side of class-B power amplifier. The testing method used three devices, such as DC power supply, function generator, and oscilloscope, to test the output signal. The output waveform from Fig. 6.5 has a noise that is caused by non-ideal effects that cause it to have signal noise. There are many parameters that might add to the effect of getting output waveforms with noise, those parameters can be probs that were used to supply the input waveform and output waveforms, Vero board, and soldering wire in the pins of DG MOSFETs, and DC power supply.

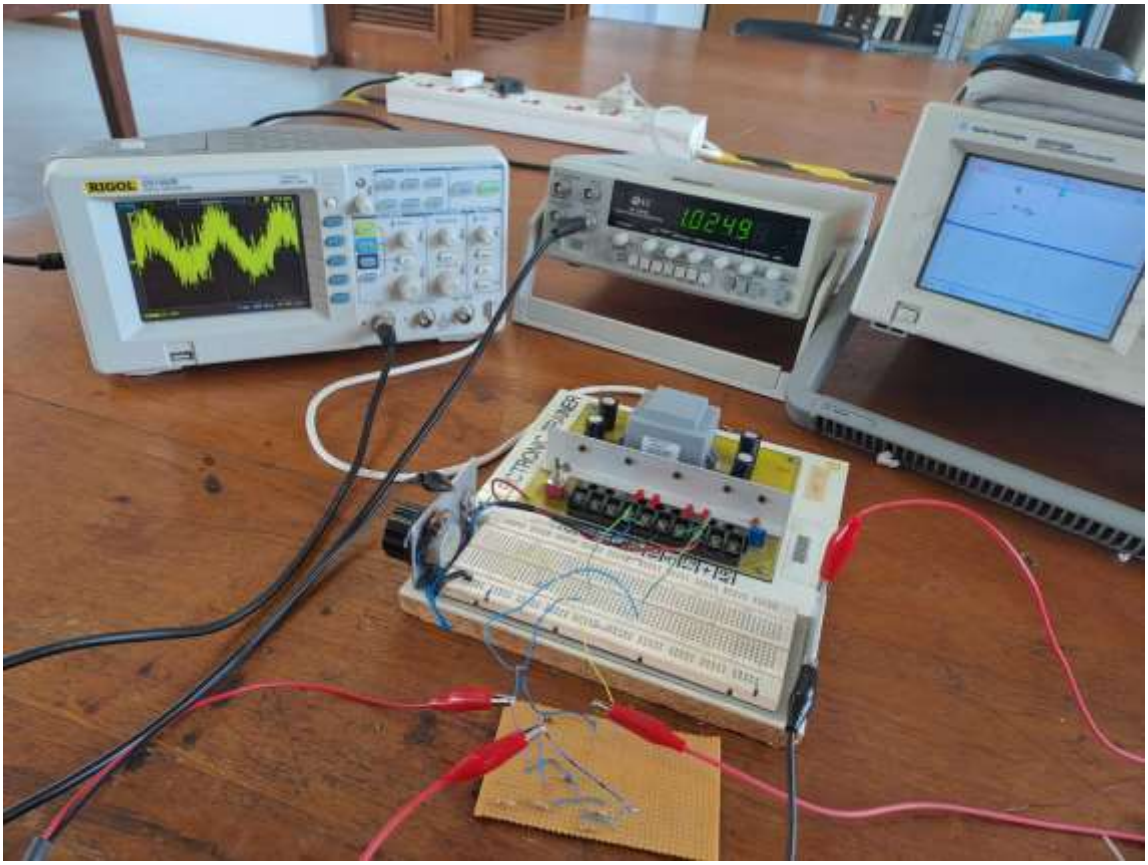

Fig 6.6. Testing set up for class-B DG MOSFET power amplifier hardware circuit.

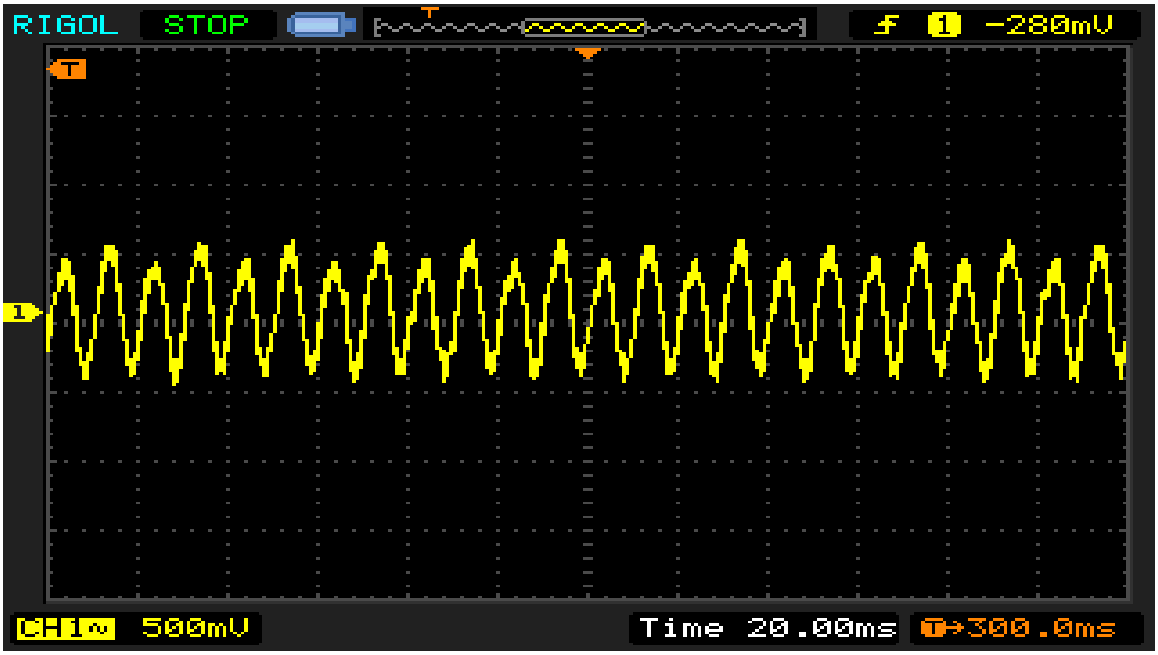


Fig 6.7. Output waveform from class-b DG MOSFET power amplifier.

The output waveform from the hardware circuit has various amplitudes, meaning that, as seen from the Fig. 6.7, the amplitude varies. This amplitude variation was caused by biasing the DG MOSFET with a voltage of 1 V and connecting both gates of each DG MOSFET while supplying an input sinusoidal waveform. From the simulations, it was found that when both gates of each DG MOSFET, the output waveforms have crossover distortions and the root cause of that was that the switching time of each DG MOSFET is less when both gates are connected. This changes the amplitude of the output waveforms, as shown in the Fig. 6.7 and other effect causes the noise since the output waveform has signal noise.

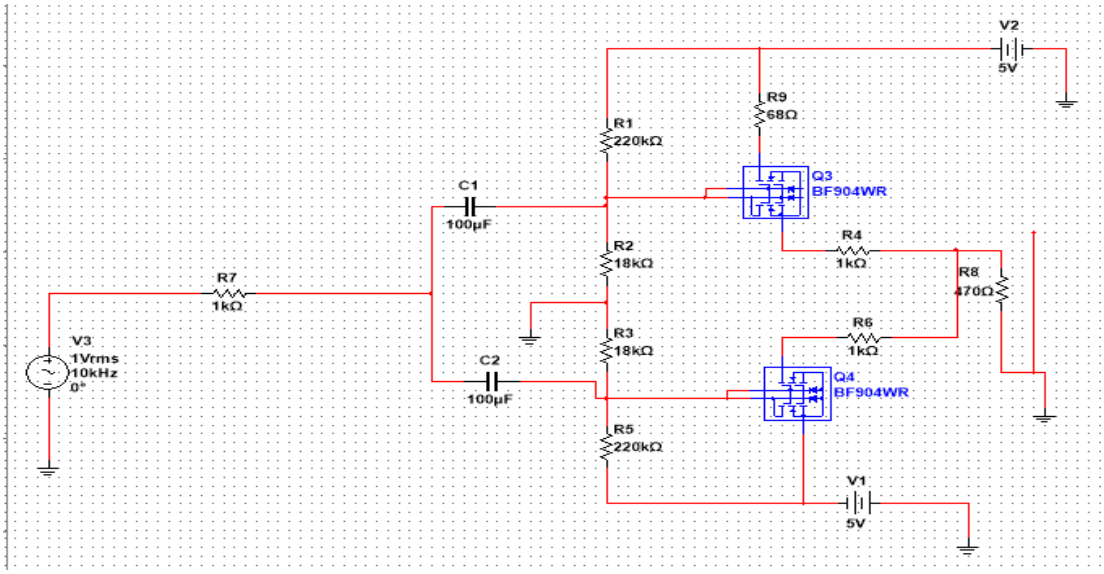


Fig 6.8. Class-B DG MOSFET power amplifier simulation circuit.

The circuit diagram (Fig. 6.8) is the simulation circuit that causes the crossover distortion when the input sinusoidal waveform is supplied to the input stage of the class-b power amplifier.

One solution to reduce the simulation's crossover distortion was to fix bias of each gate of DG MOSFET with a fixed voltage of 5 V and supply the second gate to the input signal and check the output side of the circuits. This method was also applied to the hardware design circuit and tested the output signal if the crossover distortions were observed from the circuit's output stage.

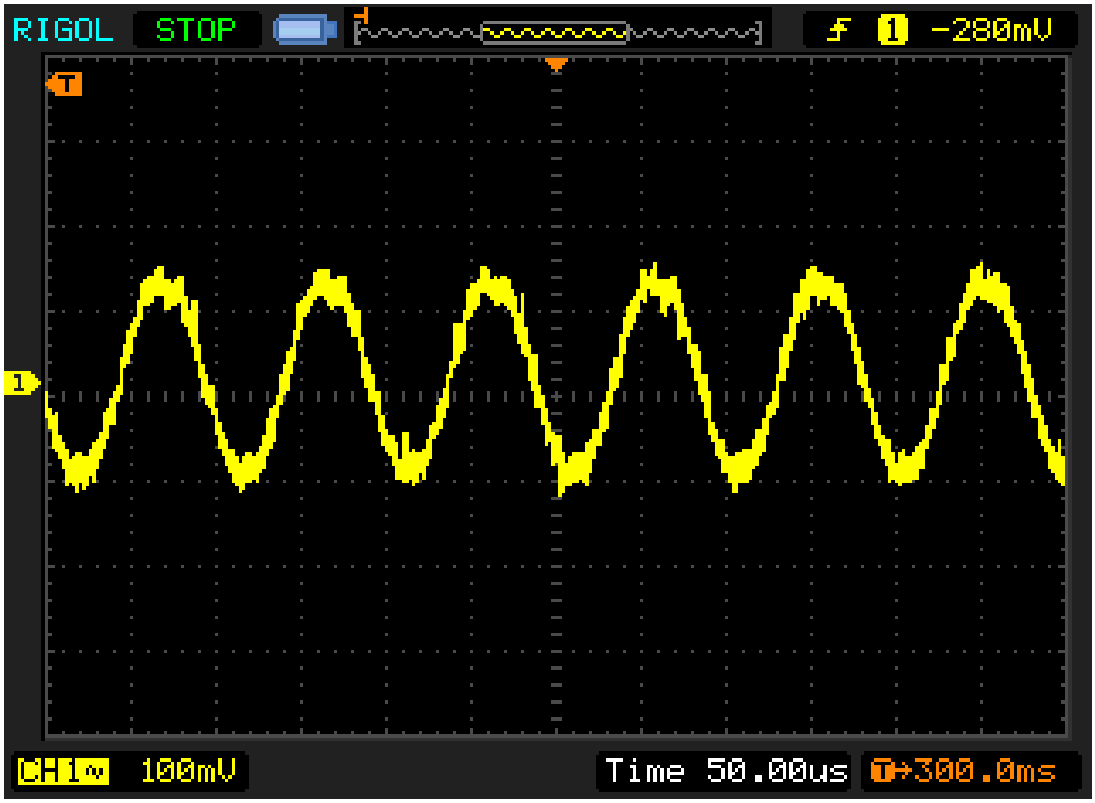


Fig 6.9. Output waveform of Class-B DG MOSFET power amplifier hardware circuit.

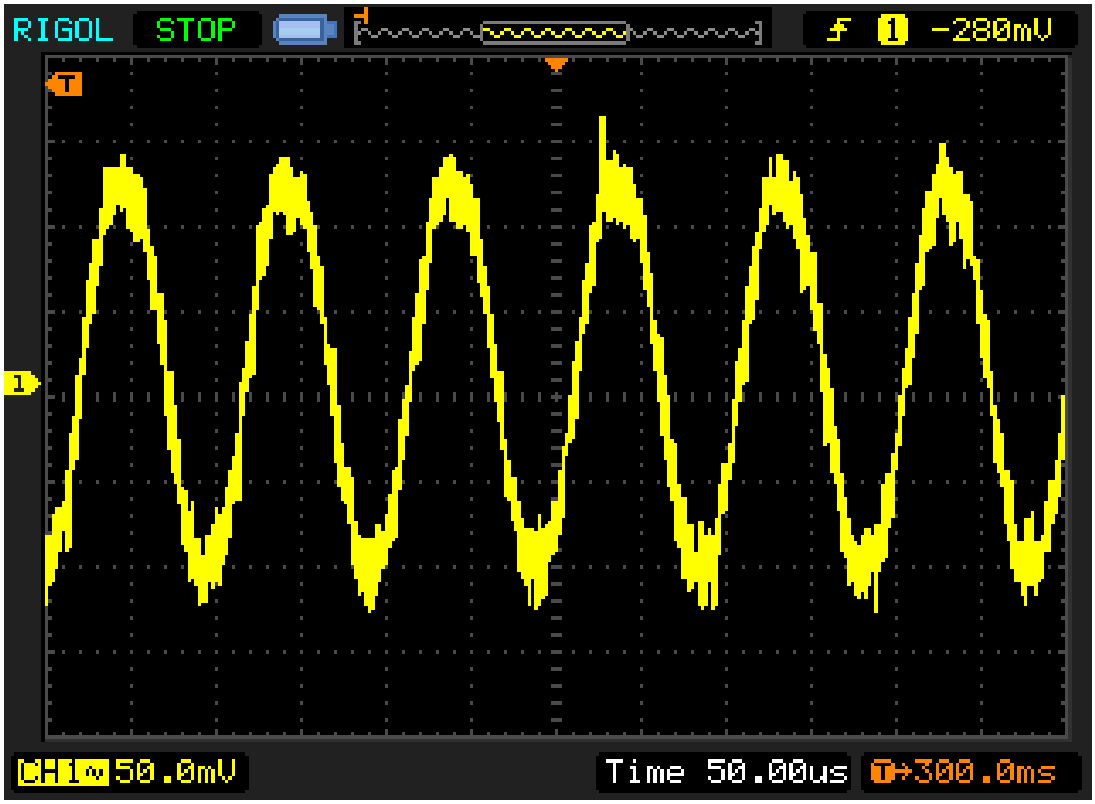


Fig 6.10. Output waveform by changing the voltage division.

Fig. 6.9 shows the output waveform of class-B power amplifier hardware circuit when gate-2 was fixed biased to 5 V and gate-1 was supplied with an input signal. This output waveform was observed by setting the oscilloscope to 100mV p/p so that the output waveforms can be clearly observed. It can be seen that there are no crossover distortions, and the amplitude of the output waveform is the same throughout the waveform. The output waveform has signal noise, which is caused by a non-ideal effect, as discussed in section 6.1 of the hardware design of class-B power amplifier.

Changing the setting of an oscilloscope to check the output waveform has no crossover distortions. The output waveform from Fig. 6.10 shows that there are no crossover distortions, but the waveform is not clean as compared to the simulated waveform, and there are many parameters that cause that, such as environmental temperature and devices that were used to test and build the circuits.

## 6.3 Conclusion

Class-B Power amplifier with the use of DG MOSFET hardware circuit design was implemented and tested, the results of simulations shows that the power amplifier with the use of DG MOSFET reduces the crossover distortion when gate-2 of DG MOSFET is fixed biased to 5 V. When the hardware circuit was designed, it showed different issue when both gate-1 and gate-2 of each DG MOSFET was connected, and the issue was that the output waveform shows different amplitude and signal noise which is a different parameter, and it was never found on the simulations. However, the simulation shows that if both gate-1 and gate-2 of each DG MOSFET were connected, the output waveform shows crossover distortions while the hardware circuit shows a different issue which is variation of amplitude. Crossover distortions were not observed in the hardware output wave except the signal noise, and signal noise was not observed in the simulations.

# Chapter-7

# CONCLUSIONS AND FUTURE RECOMMENDATIONS

## 7.1 Conclusions

All these designed circuits have different transient analyses depending on the output load connected to it. The output load connected to the power amplifier affects the transient response of the power amplifier. For better analysis, all three circuits (i.e., class-B power amplifier with DG MOSFET) had the same amount of load impedance connected to the power amplifier. In this work, only three-step responses have been indicated, i.e. percentage overshoot, rise time, and settling time are shown in the output transient graphs. The settling time is the time required by an underdamped system for its output voltage response to approach steady-state and stay within some specified percentage (for example, 5%) of the final steady-state value.

The problems faced by class-B power amplifiers, i.e., the presence of crossover distortion caused by the mismatch of the transistor, are solved a lot from the design of class-B power amplifier using DG MOSFET because of the performance of DG MOSFET which is its switching of its state from OFF to ON state. The efficiency of the class-B power amplifier is much greater than that of the class-A amplifier, which is calculated in this thesis. It was analyzed and found that the efficiency of the class-B amplifier is 63.66%.

Efficiency is the main concept that makes the power amplifier be able to drive the load when a load is applied to the power amplifier. When hardware implementation was done, signal noise parameter was observed from the hardware circuit.

## 7.2 Future Recommendations

The future work of this research is to physically implement the model of class-B power amplifier by using an advanced DG MOSFET using various materials such as high dielectric materials ($HfO_2$ etc.) that can operate with very small frequency signal input. When the physical implementation is done for this, then all the parametric performance can be compared with the theoretical values, including once are discussed in this thesis.

Also, hardware implementation will improve the accuracy of the output signal compared to the input signal and reduce the error.

All the work that was done theoretically and proved mathematically will act as a guild to improve the work of errors that might be found during the implementation of hardware implementations. The input stage of class-B power amplifier must be implemented such that all the input signal properties are not neglected because all those properties are essential in the amount of power delivered to the load and output stage.

In addition, in future, this DG MOSFET can be replaced with various other transistors, such as CSDG MOSEFT, FinFET, Multi-Gate MOSEFT, etc.

# REFERENCES


[1] Abraham Pressman, Keith Billings, and Taylor Morey, *Switching power supply design*, 3rd Ed., McGraw-Hill, 2009.

[2] Abdullah Eroglu, *Introduction to RF power amplifier design and simulation*, CRC Press, Taylor & Francis, USA 2016.

[3] Bob Cordell, *Designing audio power amplifiers*, 1st Ed., McGraw Hill, 2010.

[4] A. Vasjanov and V. Barzdenas, "A review of advanced CMOS RF power amplifier architecture trends for low power 5G wireless networks," *Electronics*, vol. 7, no. 11, pp. 271, 2018.

[6] Tommi Tuovinen, Nuutti Tervo, and Aarno Pärssinen, "Analyzing 5G RF system performance and relation to link budget for directive MIMO," *IEEE Transactions on Antennas and Propagation*, vol. 65, no. 12, pp. 6636-6645, Dec. 2017.

[7] Viranjay M. Srivastava, K. S. Yadav, and G. Singh: Performance of double-pole four-throw double-gate RF CMOS switch in 45 nm technology, *Int. J. of Wireless Engineering and Technology*, vol. 1, no. 2, pp. 47-54, 2010.

[8] Filipe M. Barradas, Pedro M. Tome, Jose M. Gomes, Telmo R. Cunha, Pedro M. Cabral, and Jose C. Pedro, "Power, linearity, and efficiency prediction for MIMO arrays with antenna coupling, *IEEE Trans. on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 5284-5297, Dec. 2017.

[9] Fabian Khateb, S. Bay Abo Dabbous, S. Vlassis, "A survey of non-conventional techniques for low-voltage, low-power analog circuits design," *Radioengineering*, vol. 22, pp. 415–427, 2013.

[10] Yuan Taur and Tak H. Ning, *Fundamentals of modern VLSI devices*, Cambridge University Press, 2013.

[11] Richard N. Tauber and Stanley Wolf, *Silicon Processing for the VLSI era - The submicron MOSFET*, vol. 3, Lattice Press, California, USA, Jan. 1994.

[12] Sung M. Kang, Yusuf Leblebici, and Chul W. Kim, *CMOS digital integrated circuit*, 4th Ed., McGraw Hill, New York, USA, 2014.

[13] S. C. Cripps, *Advanced techniques in RF power amplifier design*, Artech House, Norwood, MA, 2002.

[14] A. Pressman, K. Billings, and T. Morey. *Switching power supply design*, 3rd Ed., McGraw-Hill, 2009.

[15] M. Isaksson, D. Wisell, and D. Ronnow, "A comparative analysis of behavioral models for RF power amplifiers," *IEEE Trans. on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 348 – 359, 2006.

[16] L. A. Samoska, "An overview of solid-state integrated circuit amplifiers in the submillimeter-wave and THz regime," *IEEE Trans. on Terahertz Science and Tech.*, vol. 1, no. 1, pp. 9-24, 2011.

[17] Kok K. Yap, Rob Sherwood, Masayoshi Kobayashi, Te Y. Huang, Michael Chan, Nikhil Handigol, Nick McKeown, and Guru Parulkar, "Blueprint for introducing innovation into wireless mobile networks," *Proc. of the 2nd ACM SIGCOMM Workshop on Virtualized Infrastructure Systems And Architectures*, India, Sept. 2010, pp. 25-32.

[18] Ghanshyam Singh and Viranjay M. Srivastava, *MOSFET technologies for double-pole four throw radio frequency switch*, Springer International Publishing, Switzerland, 2013.

[19] Japheth E. Pakaree and Viranjay M. Srivastava, "Realization with fabrication of double-gate MOSFET based differential amplifier," *Microelectronics Journal*, vol. 91, pp. 70-83, 2019.

[20] D. Y. C. Lie, J. C. Mayeda, Y. Li, and J. Lopez, "A review of 5G power amplifier design at cm-wave and mm-wave frequencies," *Wireless Communications and Mobile Computing*, vol. 2018, Article ID 6793814, pp. 1-16, 2018.

[21] Sherif Shakib, Hyun C. Park, Jeremy Dunworth, Vladimir Aparin, and Kamran Entesari, "A highly efficient and linear power amplifier for 28-GHz 5G phased array radios in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 3020 – 3036, Dec. 2016.

[22] Tian Qi and Songbai He, "Power up potential power amplifier technologies for 5G applications," *IEEE Microwave Magazine*, vol. 20, no. 6, pp. 89-101, June 2019.

[23] Frederick H. Raab, Peter Asbeck, Steve Cripps, Peter B. Kenington, Zoya B. Popovic, Nick Pothecary, John F. Sevic, and Nathan O. Sokal "RF and microwave power amplifier and transmitter technologies — Part 1," *High Frequency Design RF Power Amplifiers*, pp. 22-54, May 2003.

[24] Yuan Taur, Xiaoping Liang, Wei Wang, and Huaxin Lu, "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Letters*, vol. 25, no. 2, pp. 107-109, Feb. 2004.

[25] Himangi Sood, Viranjay M. Srivastava, and G. Singh, “Advanced MOSFET technologies for next generation communication systems - perspective and challenges: A review,” *Journal of Engineering Science and Technology Review*, vol. 11, no. 3, pp. 180-195, 2018.

[26] R. Ramesh, “Influence of gate and channel engineering on multigate MOSFETs-A review,” *Microelectronics Journal*, vol. 66, pp. 136-154, Aug. 2017.

[27] M. H. Rashid, *Microelectronic Circuits: Analysis and Design*, 2nd ed., Cengage Learning, USA, 2011.

[28] David M. Snider, “A theoretical analysis and experimental confirmation of the optimally loaded and overdriven RF power amplifier,” *IEEE Transactions on Electron Devices*, vol. 14, no. 12, pp. 851-857, Dec 1967.

[29] W. H. Doherty “A New High Efficiency Power Amplifier for Modulated Waves,” *Proceedings of the Institute of Radio Engineers*, vol. 24, no. 9, pp. 1163-1182, Sept. 1936.

[30] Frederick H. Raab, Peter Asbeck, Steve Cripps, Peter B. Kenington, Zoya B. Popovic, Nick Pothecary, John F. Sevic, and Nathan O. Sokal, “Power amplifiers and transmitters for RF and microwave*,” IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814 – 826, March 2002.

[31] Frederick H. Raab “Efficiency of Doherty RF power-amplifier systems,” *IEEE Transactions on Broadcasting*, vol. 33, no. 3, pp. 77-83, Sept. 1987.

[32] Bumman Kim, Jangheon Kim, Ildu Kim, and Jeonghyeon Cha, “The Doherty power amplifier,” *IEEE Microwave Magazine*, vol. 7, no. 5, pp. 42-50, Oct. 2006.

[33] Nathan O. Sokal, “RF power amplifiers, classes A through S - How they operate, and when to use each,” *Professional Program Proceedings, Electronic Industries Forum of New England*, Boston, USA, 1997, pp. 179-252.

[34] Raymond Pengelly, Christian Fager, and Mustafa Ozen, “Doherty's legacy: A history of the Doherty power amplifier from 1936 to the present day,” *IEEE Microwave Magazine*, vol. 17, no. 2, pp. 41-58, Feb. 2016.

[35] Lee D. Forest, “The Audion: A new receiver for wireless telegraphy,” *Proceedings of the American Institute of Electrical Engineers*, vol. 25, no. 10, pp. 719 – 747, Oct. 1906.

[36] Lee D. Forest, “The Audion-detector and amplifier,” *Proceedings of the Institute of Radio Engineers*, vol. 2, no. 1, pp. 15-29, March 1914.

[37] Adel S. Sedra and Kenneth C. Smith, *Microelectronic circuits: Theory and applications*, 7th Ed., Oxford University Press, USA, 2014.

[38] Viranjay M. Srivastava, "Schematic of boost regulator with DG MOSFET: A device modeling for energy transmission," *13th Int. Conf. on Industrial and Commercial Use of Energy*, Cape Town, South Africa, 15-17 Aug. 2016, pp. 256-261.

[39] Yuan Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2861-2869, 2001.

[40] Qiang Chen, Keith A. Bowman, Evans M. Harrell, and James D. Meindl, "Double jeopardy in the nanoscale court [MOSFET modeling]," *IEEE Circuits and Devices Magazine*, vol. 19, no. 1, pp. 28-34, 2013.

[41] Rupendra K. Sharma, Charalabos A. Dimitriadis, and Matthias Bucher, "A comprehensive analysis of nanoscale single- and multi-gate MOSFETs," *Microelectronics Journal*, vol. 52, pp. 66-72, June 2016.

[42] Huaxin Lu and Yuan Taur, "An analytical potential model for symmetric and asymmetric DG MOS-FETs," *IEEE Trans. on Electron Devices*, vol. 53, no. 5, pp. 1161-1168, May 2006.

[43] Robert L. Boylestad and Louis Nashelsky, *Electronic devices and circuit theory*, 11th Ed., Pearson Prentice Hall, 2012

[44] Discrete Semiconductors, BF998; BF998R Silicon N-channel dual-gate MOS-FETs, Datasheet, Philips Semiconductor, Aug. 1996.

[45] Adelmo O. Conde, Francisco J. G. Sanchez, and Juan Muci, "Rigorous analytic solution for the drain current of undoped symmetric dual-gate MOSFETs," *Solid-State Electronics*, vol. 49, no. 4, pp. 640-647, April 2005.

[46] Adelmo O. Conde, Francisco J. G. Sanchez, and Slavica Malobabic, "Analytic solution of the channel potential in undoped symmetric dual-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1669 – 1672, July 2005.

[47] Jose C. Pedro, Luis C. Nunes, and Pedro M. Cabral, "A simple method to estimate the output power and efficiency load–pull contours of class-B power amplifiers, *IEEE Trans. on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1239-1249, April 2015.

[48] Shervin Moloudi and Asad A. Abidi, "The outphasing RF power amplifier: A comprehensive analysis and a Class-B CMOS realization," *IEEE J. of Solid-State Circuits*, vol. 48, no. 6, 2013, pp. 1357-1369.

[49] K. Mimis, S. Bensmida, K. A. Morris and J. P. McGeehan, "Continuous harmonically tuned class-B power amplifier: A closed-form equation design approach," *IEEE/MTT-S Int. Microwave Symposium Digest*, Montreal, QC, Canada, 2012, pp. 1-3.

[50] Bob Cordell, *Designing audio power amplifiers*, McGraw Hill, USA, 2011

[51] Andrei Grebennikov, *RF and Microwave Power Amplifier Design*, McGraw Hill, USA, 2005.

[52] Mel Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 2, pp. 165-168, Feb 1991.

[53] Yuan Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2861-2869, Dec. 2001.

[54] J. L. Dawson, and Thomas H. Lee: Feedback linearization of RF power amplifiers, Springer, New York, USA, 2004.

[55] Gianluca Giustolisi, Gaetano Palumbo, and Salvatore Pennisi, "Class-AB CMOS output stages suitable for low-voltage amplifiers in nanometer technologies," *Microelectronics Journal*, vol. 92, pp. 1-7, 2019.

[56] Douglas Self, *Audio Power Amplifier Design*, 5th Ed., Focal Press, UK, 2009.

[57] Sashin Ramdhani and Viranjay M. Srivastava, "Third-order high pass filter with double-gate MOSFET: A circuit perspective," *2020 International Conference on Computer Communication and Informatics (ICCCI)*, India, 22-24 Jan. 2020, pp. 1-6.

[58] M. Isaksson, D. Wisell and D. Ronnow, "A comparative analysis of behavioral models for RF power amplifiers," *IEEE Trans. on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 348 – 359, 2006.

[59] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Ed., Wiley, 2009.

[60] Vladimir Prodanov, Mihai Banu, "Power Amplifier Principles and Modern Design Techniques," *Wireless Technologies*, 1st Ed., CRC Press, 2008.

[61] B. Cordell, *Designing audio power amplifiers*,1st Ed., McGraw Hill, 2010.

[62] Carl Nelson, “Design Manual,” *Application Note-19, Linear technology*, June 1986.

[63] Hwiseob Lee, Jinhee Kwon, Wonseob Lim, Wooseok Lee, Hyunuk Kang, Keum Cheol Hwang, Kang Y. Lee, Cheon S. Park, and Youngoo Yang, “Optimized current of the peaking amplifier for two-stage Doherty power amplifier,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 1, pp. 209 – 217, Jan. 2017.

[64] Nahum Kipnis, “A Law of Physics in the Classroom: The Case of Ohm’s Law,” *Science & Education*, vol. 18, Article number: 349, 2009.

[65] Thomas L. Floyd, *Electric Circuits Fundamentals*, 8th Ed., Prentice Hall, 2009.

[66] Douglas A. Pucknell, *Basic VLSI design*, Prentice Hall, 1994.

[67] G. E. Moore, “Cramming more components onto integrated circuits,” *Electronics*, vol. 38, no. 8, pp. 1-4, 1965.

[68] Jean Pierre Colinge, “Multiple-gate SOI MOSFETs,” *Solid-State Electronics*, vol. 48, no. 6, pp. 897-905, June 2004.

[69] RS Components, https://docs.rs-online.com/c503/A700000006575967.pdf.

[70] M. R. Kumar, P. K. Agarwal, G. S. Pati, K. P. Pradhan, S. K. Mohapatra, P. K. Sahu, “Modeling of nanoscale double-gate MOSFET and its physical analysis,” *International Journal of Scientific & Engineering Research*, vol. 5, no. 5, pp. 11-16, May 2014.

[71] Proteus software, https://www.labcenter.com/pcb/.

[72] S. Mahata, A. Maiti, and C. K. Maiti, “Cost-effective web-based electronics laboratory using NI MultiSim, LabVIEW and ELVIS-I,” *2010 International Conference on Technology for Education*, India, 1-3 July 2020, pp. 1-2.

[73] Yan G. Hong, Zhang S. Ying, and Du J. Jing, “Practice and application of Multisim in digital electronic experiment teaching,” *2011 6th International Conference on Computer Science & Education (ICCSE)*, Singapore, 3-5 Aug. 2011, pp. 492-494.

[74] Krystyna M. Noga and Beata Palczynska, “The simulation laboratory platform based on multisim for electronic engineering education,” *2018 International Conference on Signals and Electronic Systems (ICSES)*, Kraków, Poland, 10-12 Sept. 2018, pp. 269-274.

[75] Li Y. Me and Cai Bo, “Electronic circuit virtual laboratory based on LabVIEW and Multisim,” *7th International Conference on Intelligent Computation Technology and Automation*, Changsha, China, 25-26 Oct. 2014, pp.

[76] Yuan Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Letters*, vol. 21, no. 5, pp. 245- 247, May 2000.

[77] Md. Abdus Salam and Quazi M. Rahman, *Fundamentals of Electrical Circuit Analysis*, Springer, Singapore, 2018.

[78] Suvashan Pillay and Viranjay M. Srivastava, "Realization with fabrication of double-gate MOSFET based class-AB amplifier," *Int. J. of Electrical and Electronic Engineering & Telecommunications*, vol. 9, no. 6, pp. 309-408, 2020.

[79] Ravinder Kumar, Munish Kumar, and Viranjay M. Srivastava, "Design and noise optimization of RF low noise amplifier for IEEE standard 802.11a WLAN," *Int. J. of VLSI Design and Communication Systems*, vol. 3, no. 2, pp. 165-173, 2012.

[80] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Double pole four throw switch design with CMOS inverter," *5th IEEE Conf. on Wireless Communication and Sensor Networks*, India, 2009, pp. 1-4.

[81] Sucheng Liu, Luowei Zhou, Xiaodong Liu, and Weiguo Lu, "Design and analysis of a high efficiency linear power amplifier," *International Journal of Electronics – Letters*, vol. 104, no. 5, pp. 1421-1432, 2017.

[82] Vamsi Paidi, Shouxuan Xie, Robert Coffie, Brendan Moran, Sten Heikman, Stacia Keller, Alessandro Chini, Steven P. D. Baars, Umesh K. Mishra, Stephen Long, and Mark J. W. Rodwell, "High linearity and high efficiency of class-B power amplifiers in GaN HEMT technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 2, pp. 643 – 652, Feb 2003.

[83] R. Mack, *Demystifying Switching Power Supplies*, 1st Ed, Newnes, Elsevier, 2005.

[84] Gabriele Manganaro and Domine Lenaerts, *Advances in analogue and RF IC design for wireless communication systems*, 1st Ed., Elsevier, May 2013.

[85] H. Zumbahlen, *Linear Circuit Design Handbook*, 1st Ed., Newnes, Elsevier, Feb. 2008.

[86] J. Gabelli, G Feve, J. M. Berroir, B Placais, A. Cavanna, B. Etienne, Y. Jin, and D. C. Glattli, "Violation of Kirchhoff's Laws for a Coherent RC Circuit," *Science*, vol 313, no. 5786, pp. 499-502, 2006.

[87] B. Cordell, *Designing audio power amplifiers*, 1st Ed., McGraw Hill, 2010.

[88] Sachchida N. Shukla, Beena Pandey, and Susmrita Srivastava, "New circuit models of Complementary-Symmetry Class-AB and Class-B push-pull amplifiers," *10th IEEE International Conference on Semiconductor Electronics (ICSE)*, Kuala Lumpur, Malaysia, 9-21 Sept. 2012,

[89] Qian Xie, Jun Xu, and Yuan Taur, "Review and critique of analytic models of MOSFET short-channel effects in subthreshold," *IEEE Transactions on Electron Devices*, vol. 59, no. 6, pp. 1569-1579, June 2012.

[90] Gabriele Manganaro and Domine Lenaerts, *Advances in analogue and RF IC design for wireless communication systems*, 1st Ed., Elsevier, May 2013.

[91] Earl McCune, "A technical foundation for RF CMOS power amplifiers: Part 2: power amplifier architectures," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 4, pp. 75-82, 2015.

[92] Ronald Montesinos, Corinne Berland, Mazen A. Hussein, Olivier Venard, and Philippe Descamps, "Comparative analysis of LINC transmitter performances with class AB and class F power amplifiers," *IEEE 9th International New Circuits and systems conference*, Bordeaux, France, 26-29 June 2011, pp. 233-236.

[93] Marco Berkhout and Lutsen Dooper, "Class-D audio amplifiers in mobile applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 5, pp. 992 – 1002, May 2010.

[94] G. R. Walker, "A class B switch-mode assisted linear amplifier," *IEEE Trans. on Power Electronics*, vol. 18, no. 6, pp. 1278 – 1285, 2003.

[95] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya, "Analysis and design of class-E power amplifier with MOSFET parasitic linear and nonlinear capacitances at any duty ratio," *IEEE Trans. on Power Electronics*, vol. 28, no. 11, pp. 5222-5232, 2013.

[96] J. H. Jeong, G. H. Kim, B. R. Min, C. H. Ahn, and G. H. Cho, "A high efficiency class A amplifier accompanied by class D switching amplifier," *28th Annual IEEE Power Electronics Specialists Conf.*, St. Louis, MO, USA, 1997, pp. 1210-1216.

[97] H. Choi, "Class-C linearized amplifier for portable ultrasound instruments," *Sensors*, vol. 19, no. 4, pp. 1-13, 2019.

[98] Vittorio Camarchia, Marco Pirola, Roberto Quaglia, Seunghoon Jee, Yunsung Cho, and Bumman Kim, "The Doherty Power Amplifier: Review of Recent Solutions and Trends," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 2, pp. 559 – 571, Feb. 2015.

[99] Junghwan Moon, Junghwan Son, Jungjoon Kim, Ildu Kim, Seunghoon Jee, Young Y. Woo, and Bumman Kim, "Doherty amplifier with envelope tracking for high efficiency," *2010 IEEE MTT-S International Microwave Symposium*, Anaheim, CA, USA, 23-28 May 2010,

[100] Patrick Reynaert, M. Bohsali, D. Chowdhury, and A. M. Niknejad, “Power Combining Techniques for RF and mm-Wave CMOS Power Amplifiers,” *Analog Circuit Design*, pp 115-143, 2008.

[101] Fabian Khateb, “Bulk-driven floating-gate and bulk-driven quasi-floating-gate techniques for low-voltage, low-power analog circuits design,” *AEU - International Journal of Electronics and Communications*, vol. 68, pp. 64-72, 2014.

[102] Fabian Khateb, “The experimental results of the bulk-driven quasi-floating-gate MOS transistor,” *AEU - International Journal of Electronics and Communications*, vol. 69, pp. 462-466, 2015.

[103] Bo Berglund, Jan Johansson and Thomas Lejon, “High efficiency power amplifiers,” *Ericsson Review*, no. 3, pp. 92-95, 2006.

[104] Marian K. Kazimierczuk, *RF power amplifiers*, 2nd Ed., Wiley, UK, 2015.

[105] Patrick Reynaert and Michiel Steyaert, *RF Power Amplifiers for Mobile Communications*, Springer, 2006.

[106] Helong Li and Stig M. Nielsen, “Detail study of SiC MOSFET switching characteristics,” *IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Galway, Ireland, 24-27 June 2014, pp. 1-5.

[107] Jiashu Chen and Ali M. Niknejad, “Design and Analysis of a Stage-Scaled Distributed Power Amplifier,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1274 – 1283, May 2011.

## NOTES

## NOTES