


*Implementation of a WCDMA
AAA Receiver on an FPGA
based Software Radio Platform*

By



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November 2001*

*Submitted in fulfilment of the academic requirements for the degree of Master
of Science in Engineering in the Programme of Electronic Engineering,
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Dedicated to my beloved parents

and most to my savior and lord

Jesus Christ

Preface

The research work in this thesis was performed by Mr. Saju P. Korah under the supervision of Mr. S. A. McDonald in the Programme of Electronic Engineering at the University of Natal, Durban, South Africa. This work was partially sponsored by Alcatel Altech Telecoms and Telkom SA as part of the Center of Excellence programme at the Centre for Radio Access technology.

Parts of the work documented in this thesis have been presented by the student author at following conferences:

- IEEE APBEM, SATCAM 2000, Cape town, South Africa.
- SATNAC 2000, Cape town, South Africa
- SATNAC 2001, Wild Coast, South Africa
- VTC 2001, IEEE Spring Conference (53rd), Rhodes Island, Greece

The whole thesis, unless specifically indicated to the contrary in the text, is the author's work, and has not been submitted in part, or in whole to any other university.

As the candidate's supervisor, I have approved this thesis for submission

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Signed: -----

Date: -----

Acknowledgements

First and foremost my sincere thanks to almighty God who showered blessings and strengthened me during this project.

Secondly, I would like to thank Mr. S.A. McDonald for his help, encouragement and constructive criticism during the past years. His patience and support have been truly appreciated. I would also like to express my gratitude to Prof. F. Takawira for his valuable advice and comments for the completion of this project.

I wish to express my sincere appreciation to my parents for their patience, prayer, encouragement and full support over the past years. I would also like to thank my brothers and sisters.

Thanks are also owed to Telkom SA Ltd, Alcatel Altech Telecoms and THRIP for their valued financial support for the completion of this project. I would like to extend this thanks to Agilent Technologies for the donation of Advanced Design System (ADS) software, which has allowed me to simulate the complete project before implementation and Alcatel for the donation of a software radio, otherwise this project could not have become a reality.

Last, but not least, I would like to express my appreciation to my colleagues and friends for their assistance and invaluable friendship. In particular, special thanks to my former colleague Mr. Kelesh Roopram for proof reading this thesis and finally to Tim and Bret for the technical support.

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Abstract

WCDMA promises to achieve high-speed internet, high quality image transmission and high-speed data services with larger system capacity. However, Multiple Access Interference is one of the major causes of transmission impairment, which reduces the link capacity in WCDMA systems. The Adaptive Antenna Array (AAA) technique reduces multiple access interference by directing antenna beam nulls towards the interfering signals by weighting the received signals from all antennas before combining the signals.

With the very rapid advancement of wireless personal communications services, a new challenge to the cellular industry is the integration of multiple systems and applications on a single device. A software radio technique offers a possible solution to achieve this goal including international roaming and multiple standard operations within the same geographical area. The main attraction of a software radio is its flexibility, in that it can be programmed for emerging cellular standards allowing it to be updated with new software without any changes in the hardware infrastructure. A software radio incorporating adaptive array beamforming at the receiver can increase the total carried traffic in a system and transmit power while the probability of call blocking and forced termination can also be decreased.

This dissertation examines WCDMA, AAA, power control and software radio techniques in the world of wireless communication systems. Once the theoretical background of CDMA and AAA has been substantiated, the thesis establishes the need for power control in mobile systems by examining simulation results.

An AAA receiver with six antenna elements is proposed and evaluated in different environments as a precursor to implementation. It can be inferred that when the link is interference limited, the link capacity can be increased and it has been shown that the AAA receiver with six antenna elements increases the link capacity to about 2.9 times that of the single antenna RAKE receiver.

This thesis also examines the basic concepts of VHDL and considers this as the principle means to program reconfigurable core FPGA's in the software radio. A three-layered (PC/DSP/FPGA) software radio test bed is used to implement an AAA receiver. The architecture of the test bed is designed in such a way that it can be used to evaluate the performance of various FPGA based transceivers and coding schemes etc. Many of the desirable features and flexibilities inherent in the software radio concept are available on this test bed and the system has proved to be capable of high speed digital processing and is ideally suited to the development of time critical system components. The bit error rate achieved using the implemented receiver is assessed and compared to simulation results in an environment incorporating Rayleigh fading and AWGN.

Chapter 1

Introduction

Communications has become the key to momentous changes in the organization of businesses and industries worldwide as they adjust to the shift towards an information economy. Historically, communication has been restricted primarily to voice traffic between two fixed locations rather than between two people. With the advent of wireless technology, a transition from point-to-point communication has begun. Testimony to this is the rapidly increasing penetration of cordless and cellular phones into the wireless communication market all over the world.

1.1 Motivation

Over the last decade the deployment of wireless communication systems has been significant. In the 1980s, the first commercial mobile telephony was introduced. The first generation of mobile systems were analog and based on Frequency Division Multiplex (FDM) technology. Due to limited technology, the size of phones was large. Advances in semiconductor technologies provided a vital boost to the cellular mobile industry. With the use of Application-Specific Integrated Circuits (ASICs), the size of the handsets reduced considerably. Second generation (2G) wireless systems employed digital modulation and advanced call processing capabilities, which fueled the growth of the cellular industry. Examples of 2G wireless systems include the Global System for Mobile communications (GSM, previously known as Groupe Speciale Mobile), Time Division Multiple Access (TDMA), examples of which are IS-54/IS134, and Code Division Multiple Access (CDMA). Specific CDMA examples are IS-95 in the

United States, Personal Digital Cellular (PDC) in Japan, Digital Enhanced Cordless Telecommunications (DECT), Personal Handyphone System (PHS) and Personal Access Communication Systems (PACS) [22-23]. Digital technology offered greater capacity, speech privacy and greater radio link robustness than analog systems which further enhanced its appeal to users and services providers alike.

Many technical features of CDMA enable the network to offer high quality on demand voice services to customers and it's ability to provide high capacity allows the service provider to better utilize its invested network assets. CDMA gained significant support among services providers because of the numerous advantages over other multiple access schemes like Frequency Division Multiple Access (FDMA) and TDMA. In a traditional FDMA scheme, increasing the required bandwidth per user decreases the total number of users a fixed spectrum can support. In TDMA systems data from each user are carried in time intervals called time slots; so additional users cannot be added once all time slots are assigned. Thus it is not possible for these schemes to increase the number of users beyond certain limits without causing an intolerable amount of interference to reception of a mobile station at the cell-site receiver.

CDMA uses a radically different approach. It assigns a unique code to each user to accommodate multiple users on the same wideband channel at the same time. The number of CDMA channels in the network depends on the level of total interference that can be tolerated in the system. Thus the CDMA system is limited by interference, and the quality of the system design plays an important role in it's overall capacity. Various promising techniques have been proposed to minimize the interference in a CDMA system. In [11], it is shown that multistage and successive interference cancellation techniques reduce interference by cancellation of one detected signal from another, the author also describe how adaptive detection algorithms can be applied to achieve this goal. In this thesis an Adaptive Antenna Array (AAA) technique is considered for suppressing the interference in the channel. The benefits and the capacity improvements achieved using the AAA technique is demonstrated in various investigations [34-36]. Various applications of AAAs in mobile communication

systems are discussed in [45-46] and [49]. CDMA systems also achieve capacity increase through the use of cell sectorization. Soft handoff, exploitation of multipath fading through RAKE combining etc are further advantages over FDMA and TDMA.

Power control techniques minimize the power in the channel, thereby reducing interference, which results in system capacity increase. Performance improvements using power control techniques is discussed in [84-86]. The performance of closed loop power control in a CDMA environment is demonstrated in [83] and [96]. This thesis investigates the performance of a closed loop power control technique. A joint power control and beamforming scheme is proposed and demonstrates the increase in system capacity via the combination of these two methods [87], [73].

The IS-95 CDMA standard was adopted by the Telecommunication Industry Association (TIA) and became a digital cellular standard in 1992. As the penetration of cellular services increased, so to did the demand for greater call capacity and higher data rates.

Third generation (3G) wireless systems evolved from the mature 2G networks, with the aim of providing universal access and global roaming. These systems are expected to support multidimensional high-speed wireless communication. The International Telecommunication Union (ITU) 3G mobile communication systems, called the International Mobile Telecommunications-2000 (IMT2000, or Universal Mobile Telecommunication Systems (UMTS) in Europe) are designed to support wideband services at data rates as high as 2 Mb/s, with the same quality as fixed networks. To realize true IMT-2000 systems, a new wideband wireless access technology incorporating as many technology developments as possible is necessary. WCDMA technology is considered to be the most promising technology to realize the IMT 2000 vision. WCDMA uses coherent demodulation in the uplink, a feature that has not previously been implemented in cellular CDMA systems. In the case of coverage, WCDMA demonstrated that it is possible to reuse GSM 1800 cell sites when migrating from GSM to WCDMA supporting high rate UMTS services [2]. The coverage of

WCDMA is determined by the link performance through link budget as shown in [25]. The results show that WCDMA speech service will tolerate a few dB higher path loss than a GSM speech service. It can be inferred from this that WCDMA gives better speech coverage than GSM, reusing the same cell sites when being deployed in the same or nearby frequency bands. Another important characteristic of WCDMA is the fact that power is the common shared resource for users. WCDMA became more attractive than other 3G systems which led to its commercial implementation. Recently, a commercial WCDMA network has been implemented by NTT, Japan.

The current challenge in radio networks is to provide integrated broadband services to every user. Third generation communication systems are intended to bring multimedia to mobile terminals. It is clear that if video applications become widely used in 3G networks existing capacity will be insufficient. This creates the need for a new system or standard which can provide higher traffic densities. As new radio standards are deployed without substantially supplanting existing ones, the need for multimode multiband handsets and infrastructure increases. In order to provide global roaming the need for a system that is reconfigurable without any change in the hardware infrastructure arises. With Software radio techniques, only one hardware infrastructure system is needed. The difference in frequency band and technology can be overcome through reconfiguring the system by downloading the software manually or through over the air command interface [119-121].

A number of enabling technologies have allowed the development of commercially viable platforms providing an efficient bridge to 3G wireless systems. Software radio offers a means to address the issue of infrastructure evolution from GSM to UMTS from the base station perspective. From the handset perspective it offers manufacturers the potential of a UMTS handset product capable of handing off to GSM in those areas that UMTS rollout has not yet reached. It also potentially allows manufacturers to address geographical markets at different stages of migration to UMTS with a single “future-proof” product. The basic concept behind software radios has been in existence for well over ten years. There is currently a resurgence of interest in the software radio.

This is partly driven by the idea that a truly global commercial communications terminal may be realized as a software radio [127]. Early software radio research focused on the military's goal of total flexibility across dozens of radio frequency bands and air interface modes. Current research focuses more on the economic viability of introducing 3G handsets and infrastructure. The recent renaming of the Modular Multifunction Information Transfer Systems (MMITS) forum to the Software Defined Radio (SDR) forum signals the shift from military to commercial emphasis in open architecture standards for software radio [122]. The commercial sector defines a software radio as one that implements a specific range of capabilities through elements that are software reconfigurable. The software radio includes a limited set of predefined hardware functions such as air-interface Application Specific Integrated Circuits (ASIC), among which one may be selected by software.

An ideal software radio is a multimode radio with dynamic capability defined through software in all layers of the protocol stack, including the physical layer. In base stations, a wideband ADC may digitize an entire service band at IF, with programmable digital filters for channel isolation and DSP's or Field Programmable Gate Arrays (FPGAs) for demodulation. Coupled with a corresponding wideband DAC and software re-programmable functions from IF to base band, such a radio supports arbitrary air interfaces within engineering limits. FPGA-based DSP platforms allow the designer to realize the data path that exactly matches the required processing, while at the same time maintaining the flexibility of a software approach. With the advance in FPGA technology a new dimension for signal processing engineers to maintain the flexibility of software radio with performance close to ASICs has been provided.

This thesis will examine a particular type of software radio with two high speed FPGAs as the reconfigurable core. Design and implementation issues of a WCDMA AAA system that exploits the benefits of these key technologies are also discussed. The implementation of a specific WCDMA AAA transceiver on the software radio will allow the reader to explore, how the radio flexibility can work towards easier development and overcome new system deployment problems.

1.2 Focus of the thesis

In order to amalgamate the techniques of spread spectrum, AAA, power control, and software radio into a working system a thorough investigation is required. From an implementation point of view, this thesis focuses mainly on three issues: the physical layer of a CDMA system, practical channel behavior model and the hardware level of the software radio.

Chapter 2 examines the theoretical concepts of spread spectrum techniques, where CDMA is considered as the basic structure to explain the concepts of a WCDMA wireless system. Pseudorandom Noise (PN) sequences are used to spread the incoming signal in the WCDMA system. Simulated results are presented to demonstrate the behavior of PN sequences. The physical layer of CDMA, presented in Section 2.4 familiarizes the reader with the component level of the system, simultaneously discussing the differences between the CDMA and WCDMA physical layers. An overview of the WCDMA standard is discussed in order to implement the proposed system using WCDMA standards. The benefits of WCDMA over CDMA are also discussed.

An Adaptive Antenna Array technique minimizes the multiple access interference in WCDMA systems, thereby increasing the system capacity. This thesis considers AAA techniques as a means of minimizing MAI in the system. Chapter 3 examines the theoretical concepts of antenna arrays, beamforming and the application of adaptive antenna arrays to mobile communication systems. The spatial filtering properties of the antenna array which reduces the cochannel interference and the capability of forming beams in certain directions and nulls in others, which provides the ability to cancel some of delayed signals, are the principle benefits of antenna arrays. Formation of multiple beams also reduces the handoff process in the network. The Least Mean Square algorithm is also discussed to demonstrate the weight adaptation method that could be employed in the implemented system.

In Chapter 4, a WCDMA receiver using a six element AAA to suppress the MAI is proposed for implementation. Mathematical representation of the proposed AAA receiver model is discussed. In order to justify the proposal for implementation, a system model is designed to carry out a performance evaluation. An AAA receiver with six antenna elements and a single antenna element RAKE receiver with ten users are considered for evaluation. The 3G mobile communication systems are expected to operate in various environments. It is infeasible to consider all environments but considering the essence of possible environments, four different environments are considered namely; vehicular, indoor, and outdoor to indoor pedestrian and finally a mixed environment (which is a practical channel with AWGN). The significant performance improvement of the proposed receiver in all environments justifies its implementation. The penultimate section of Chapter 4 establishes the need for power control in mobile CDMA environments using simulation results. Also described is a closed loop power control algorithm, which can be incorporated in the implementation in future developments. The simulations discussed in chapter 4 were completed as a precursor to the implementation of the proposed receiver in the software radio.

Chapter 5 explores the basic concepts of the software radio. Although the 3G wireless concepts address the goal of global standardization, an approach which is more realistic in the intermediate term and more flexible in the longer term, is to develop transceivers that will operate with several standards and in several frequency bands on a common hardware platform. Such a platform would allow flexible and programmable operations. This chapter introduces the concept of flexibility in a software radio and discusses the specific radio tasks via partitioning of radio architectures into the two core programmable technologies of DSPs and FPGAs. A PC/DSP/FPGA based software radio test bed is utilized and is presented in Section 5.4. This test bed can be used to evaluate various FPGA based transceivers and provides a good alternative to system simulation on a purely PC platform. The system is presented as a three layered architecture and the various interfaces and protocol specifications are also discussed. Alcatel Altech Telecoms (AAT) flexible software radio platform is discussed, giving

the reader a firm understanding of the environment in which the proposed system model was implemented. The benefits of the core programmable device (FPGA) in the software radio are also reviewed. The data sources for the FPGA include ADCs and serial data streams. VHDL is considered as the means of programming the FPGAs in the software radio. Section 5.7 introduces the features of VHDL, explains VHDL terms using a simple VHDL program and discusses the synthesis process.

Chapter 6 moves the reader into the implementation arena where the proposed implementation plan and actual system to be implemented are discussed. Measured results of each block are presented and discussed to justify the implementation. Section 6.3 tackles the system time critical components and the generation of various synchronization frame signals used in the design. A different approach is considered to explain the implementation issues. This approach uses simple block diagram rather than VHDL code explanation. Section 6.5 explores one of the core elements of the transmission aspects of the system; that of spreading and despreading of the base band data. A simulation is used to demonstrate the autocorrelation function of a PN sequence. The signals measured at the output of transmitter and receiver filters describe the basic filter concepts. The chapter familiarizes the reader with the theoretical aspect of Rayleigh fading and AWGN and the practical implementation of these channel distortions. A subsection is used to explain the realization of antenna arrays in the software radio. Due to the limited capacity in the FPGA, mobility of the desired user is avoided. The weights were calculated manually and stored in the DSP memory and fed to the multipliers used in the beamformers. A theoretical radiation pattern of a patch antenna is used to calculate the total array pattern in order to determine the appropriate weights for each of the desired users. The chapter concludes with the results obtained for system performance in both AWGN and uncorrelated Rayleigh fading channels and also exposes the reader to the high-speed capabilities of the software radio.

Chapter 7 concludes this thesis with suggestions for future development and improvement of the implemented system. The system developed on the software radio

test bed can be used as a basic structure to implement a complete WCDMA network as a part of Centre of Excellence Programme.

1.3. Original contribution of the thesis

The original contributions of this thesis are listed below.

1. Optimization of an AAA receiver using ADS software.
2. A system model is designed to carryout the comparative performance evaluation of an AAA receiver (with six antenna elements) and a RAKE receiver.
3. A comparative performance evaluation results in four different environments for the different receivers are presented.
4. A simple closed loop power control structure is derived and simulated using the ADS environment.
5. Implemented a rudimentary AAA receiver on a DSP/FPGA based software radio platform.
6. Generated and optimized code for the following system components in the software radio.
 - i. Frame synchronization signals
 - ii. Framing
 - iii. Spreading
 - iv. Rayleigh fading
 - v. AWGN
 - vi. Antenna array structure
 - vii. Despreader
 - viii. Beamformer
 - ix. RAKE combiner (equal gain)
 - x. Error counter

Since this work builds on developments of all students involved in the Centre of Excellence, it should have noted that only the transmitter and receiver filter used in this design are from Ellis, [114]

1.4 Published work

The following publications have resulted from this work, which have been presented by the student author at the following national and international conferences

- “A Comparative Performance Evaluation Of Coherent Adaptive Array Diversity DS-CDMA Receiver”, Proc. of IEEE APBEM, SATCAM2000, Cape town, South Africa.
- “Performance Evaluation Of Reverse Link Power Control in a Mobile CDMA Environment”, Proc. of SATNAC2000, Sept.11-13, Cape town, South Africa.
- “Towards the implementation of a WCDMA AAA receiver on an FPGA software radio platform”. Proceedings of 53rd VTC2001, IEEE Spring Conference (May6-11, 2001), Rhodes Island, Greece.
- “Operational Overview of a DSP/FPGA Based Software Radio”. Proc. of SATNAC2001, Wild Coast, South Africa.

Chapter 2

Code Division Multiple Access

2.1 Introduction

The demand for mobile radio services has continued to increase dramatically for many years and this expected high demand has led many service providers to investigate digital technology to satisfy the increasing demand. Many of the users are becoming increasingly interested in minimizing the possibility of their communication signals being intercepted or received by an unintended party. Spread spectrum modulation is a promising technique for communication signal protection against unauthorized interception as well as protection against intentional and accidental interference [18]. Spread Spectrum techniques provide the wireless communication developer with a host of exciting and powerful possibilities. For instance, it offers the prospect of its coexistence, in a near-transparent fashion, with narrow-band signals. From this, it is clear that spread spectrum signals are fairly immune to jamming signals. In this light, it may be asked why the technology has not been more widely used. The truth is that it has been used for decades in a military context, and the answer to its slow infiltration of civilian use lies in the fairly complex nature of its implementation. However, as the mobility of the world's telecommunications infrastructure has dramatically increased, so the demand for new signal transmission techniques such as spread spectrum has also amplified. This, coupled with formidable technological advances, has led to the feasibility of using spread spectrum within a civilian context. Spread spectrum has been used for a long time in military communications to resist intentional jamming and to achieve low-probability of detection. However, in recent years spread spectrum techniques have moved from military to commercial communications, culminating in

the introduction of Code Division Multiple Access (CDMA) technology as an alternative standard for commercial digital cellular systems.

2.2. Spread Spectrum

The definition of spread spectrum techniques [6] is as follows:

“Spread spectrum is a means of transmission in which the signal occupies a bandwidth in excess of the minimum necessary to send the information; the band spread is accomplished by means of a code which is independent of the data, and a synchronized reception with the code at the receiver is used for despreading and subsequent data recovery”.

The use of spread spectrum means that each transmission utilizes a large amount of spectrum, this may be compensated for by the interference reduction capability inherent in the use of spread spectrum techniques, so that a considerable number of users might share the same spectral band. The basic signal characteristics of the spread spectrum systems are [18]:

- The carrier is an unpredictable wide band signal
- The bandwidth of the carrier is much larger than the bandwidth of the data modulation
- Reception is accomplished by cross correlation of the received wideband signal with a synchronously generated replica of the wideband carrier.

Spread spectrum systems, because of the nature of their signal characteristics have at least five important attributes:

2.2.1 Multipath protection

In the receiver the arrived signal is not just a single path signal from the transmitter. Due to transmission through objects and reflections, the signal arrives at the receiver from different paths. These are the same as the transmitted signal but with phase differences, different amplitudes, delays and arrival angles. Combining these signals at the receiver will be constructive at some of the frequencies and can reject others. In the

time domain, this results in a dispersed signal. Spread spectrum modulation can combat this multipath interference and depends very much on the type of modulation used.

2.2.2 Increased privacy and security

The data signal is spread with coded sequences and can only be despread and recovered if the receiver knows the replica of the coded sequences. This increases privacy and security. Cryptographic capabilities result when the data modulation cannot be distinguished from the carrier modulation and the carrier modulation is effectively random to an unintended receiver. A system using indistinguishable data and spread spectrum carrier modulation is a form of privacy.

2.2.3 Multiple access

Transceivers using independent random carriers can operate in the same bandwidth with minimal cochannel interference. These systems are called spread spectrum Code Division Multiple Access (CDMA) systems [18]. In CDMA all the users have the same bandwidth at the same time, but separated with different Pseudorandom Noise (PN) codes which must be orthogonal to each other. If PN codes are orthogonal then their cross correlation over the one code length time of the PN codes is zero. In the receiver, correlating the received signal with the particular code signal from a certain user will then only despread the signal of the user, while the other spread signals will remain spread over a large bandwidth. Thus, within the information bandwidth, the power of the desired user will be larger than the interfering power provided there are not too many interferers, and the desired signal can be extracted.

2.2.4 Antijamming capability

The antijamming capability, especially narrow band signal jamming, has been exploited in military systems for a long time. This is more or less the same as interference rejection except the interference is unlawfully inflicted on the system.

2.2.5 Low probability of intercept (LPI)

LPI can be achieved with high processing gain and unpredictable carrier signals when power is thinly and uniformly spread in the frequency domain. The low density of spread spectrum signals is an inherent spread spectrum property, which exists because of the bandwidth expansion.

There are three general approaches to implementing spread spectrum systems

- a) **Frequency Hopping Spread Spectrum:** In frequency hopping spread spectrum, the carrier frequency is shifted in discrete increments in a pattern generated by a code sequence. It creates uncertainty at the hostile receiver by randomly shifting the base bandwidth between a number of possible frequency intervals or cells. Assuming the frequencies used are packed as tightly as orthogonality permits. Typically the new carrier phase cannot be predicted when a frequency hop occurs. Frequency hopping spread spectrum systems are of two types; fast and slow hop systems. In a slow hop system, the hop rate is less than the message bit rate and in fast hop system the hop rate is greater than the message bit rate.
- b) **Time hopping spread spectrum:** In time hopping spread spectrum systems the transmission time is divided into intervals called frames. Each frame is divided into time slots and during each frame only one time slot is modulated with a message. Uncertainty is created at a hostile receiver by varying the intervals of time. Time hopping is useful as a form of random time multiplexing allowing both transmitter and receiver use of the same antenna [18]. The pulse rate in time hopping is same as the bit rate of the message it transmits.
- c) **Direct Sequence Spread Spectrum:** In direct sequence spread spectrum the message carrier is modulated by a digital code in which the code bit rate is much larger than the information signal bit rate. Unlike time hopping, direct sequence typically transmits continuously during the bit interval, not just over a subinterval. Thus it transmits all the time and continually uses all of the spread spectrum bandwidth.

The excellent performance of spread spectrum techniques against interference signals has motivated cellular providers to implement this system for commercial use. In early 1990 QUALCOMM Inc. pioneered innovative implementation approaches using CDMA spread spectrum digital cellular systems. This CDMA system was standardized and is known as the IS-95 standard of the Telecommunications Industry Association and the Electronic Industries Association (TIA/EIA/IS-95).

In this thesis, the implemented system employs direct sequence spread spectrum techniques. A system in which the spreading signal has a bandwidth greater than the minimum bandwidth required to transmit the desired information satisfies the requirements of direct sequence spread spectrum techniques. At the receiver, despreading is achieved by the cross-correlation of the received spread signal with a synchronized replica of the same signal used to spread the data. In CDMA Pseudorandom Noise (PN) code signals are used to spread the information signal.

2.3 Pseudorandom Noise Sequences

A Pseudorandom Noise (PN) sequence is a sequence of binary 1's and 0's with autocorrelation properties similar to white noise. In CDMA systems, pseudorandom noise sequences are used to perform the following tasks:

- Larger bandwidth for transmission via modulation of the data signal
- Providing a unique identity for each user by using the same transmission bandwidth in the multiple access scheme

The PN sequences are not random but are deterministic, periodic sequences. The following are the important properties of PN sequences from [10]:

- The relative frequencies of zero and one are each $\frac{1}{2}$
- For zeroes or ones, half of all run lengths are of length 1; one quarter are of length 2; one eighth are of length 3; and so on
- If a PN sequence is shifted by any nonzero number of elements, the resulting sequence will have an equal number of agreements and disagreements with respect to the original sequence

A deterministically generated sequence that nearly satisfies the above three tasks within extremely small discrepancies is referred to as a pseudorandom sequence. PN sequences can be generated by using n -stage linear feed back shift registers. A feed back shift register consists of two memory storage stages. Binary bits are shifted through the different stages of the register in response to clock pulses connected to it. The output of the stages are combined to produce the input of the first stage. The contents of the initial stage and the feed back logic will determine the contents of the next stage. A feed back shift register and its outputs are called linear when the feed back logic consists of modulo-2 adders.

To explain the properties of PN sequences, consider a three-stage linear feedback shift register as shown in Figure 2.1. The output of the last stage (stage 3) is connected to the modulo-2 adder and a feedback path is connected to the first stage. The operation of the shift register is controlled by a sequence of clock pulses. In the case of CDMA the clock period can set to the chip time. At each clock pulse, the contents of the shift register at each stage will shift by one stage to the right. Also at each clock pulse the contents of the stages R1 and R3 are modulo-2 added, and the result is fed back to stage R1. The shift register sequence is defined to be the output of stage R3

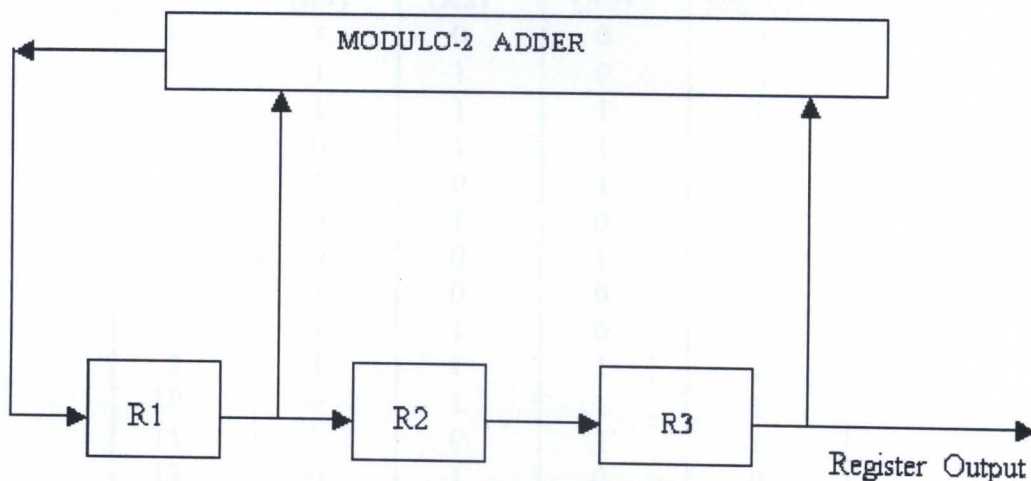


Figure. 2.1: Stage linear feedback shift register

If one assumes that the first stage of the shift register R1 is initially filled with a 1 and the other stages are filled with 0, the initial stage of the shift register is 1 0 0. After

Figure 2.2 shows the PN sequence generated in ADS simulation environment using a 3-stage linear feedback shift register.

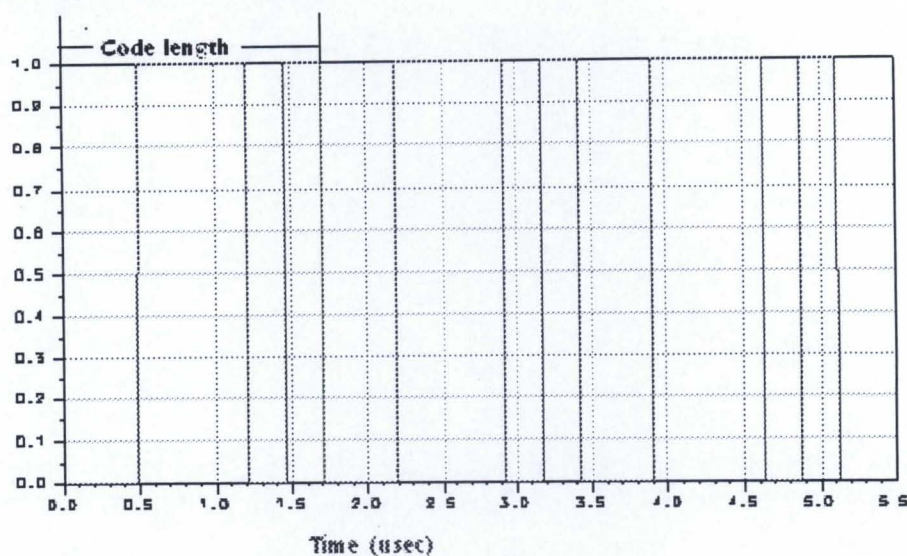


Figure 2.2: PN sequences

Autocorrelation is the degree of correspondence between a sequence and a phase shifted replica of the same sequence. When the autocorrelation reaches a maximum, then the two codes are in-phase and have a time shift of zero. In a CDMA system, this function is done by a mobile station to acquire the unmodulated pilot channel. The reverse channel in CDMA is the link from mobile station to the base station while the forward channel is from base station to mobile station. The reverse link uses a long PN code for channelization. The long code has a length of $2^{42} - 1$ chips and is generated using a 42-stage register. The forward link uses Walsh or Hadamard codes for channelizing individual users of a particular base station. However, the forward link also uses the PN code. Each base is assigned a unique PN code that is superimposed on top of the Walsh code. This is done to provide isolation among the different base stations because each base station uses the same 64 Walsh code set. The short PN codes that are used in the forward link have a length of $2^{15} - 1$ chips and are generated using a 15-stage register.

2.4 Physical layer overview of CDMA

As in depth presentation of a CDMA physical layer is provided, as it is necessary to understand the implementation issues that is addressed in Chapter 6.

As previously stated a CDMA channel consists of forward CDMA and reverse CDMA channels between the base station and mobile station. In the forward channel Walsh codes are used to distinguish different channels, while in the reverse channel PN sequences are used to distinguish the channels.

2.4.1 Forward link

The forward channel consists of four types of logical channels: pilot, sync, paging and traffic channels [20,95]. Figures 2.3 and 2.4 show the CDMA channel overview and block diagram of a CDMA (IS-95) forward link pilot channel respectively.

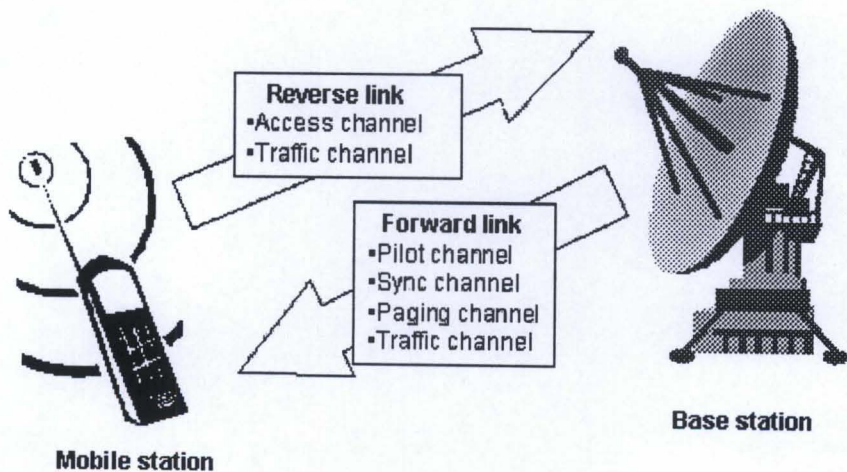


Figure 2.3: CDMA (IS-95) channel overview

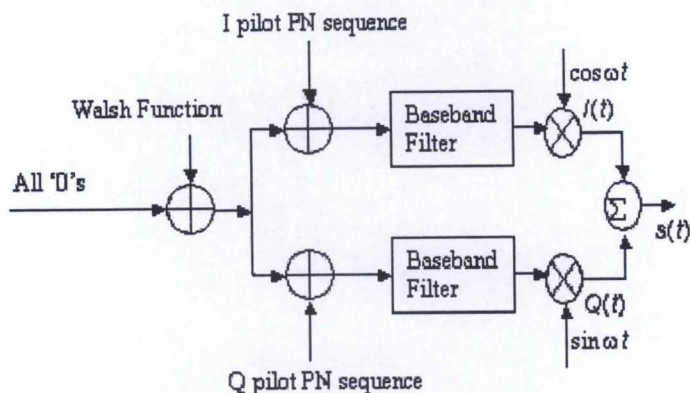


Figure 2.4: Forward link pilot channel [20,95]

2.4.1.1: Pilot channel: The pilot channel is an unmodulated spread spectrum signal, which is continuously transmitted by the base station on each active forward CDMA channel. The mobile station monitors the pilot channel at all times except when not receiving in the slotted mode [20]. The pilot channel provides the mobile with timing and phase reference. The SINR measurement of pilot channel in a mobile station provides information as to which is the strongest serving sector for that mobile.

2.4.1.2 Sync channel: Figure 2.5 shows a block diagram of forward link sync channel. The sync channel transports synchronization messages to the mobile station. The sync channel is convolutionally encoded and interleaved before transmission. Each sync channel frame begins with the start-of-message bit. '1' indicates the start of the sync channel message and '0' indicates that the current sync channel frame has the contents of a running sync channel message that started in the previous frame. The sync channel message contains information relating to the offset of the pilot PN sequence used by the transmitter sector and the information to enable the mobile to synchronize with the long PN code.

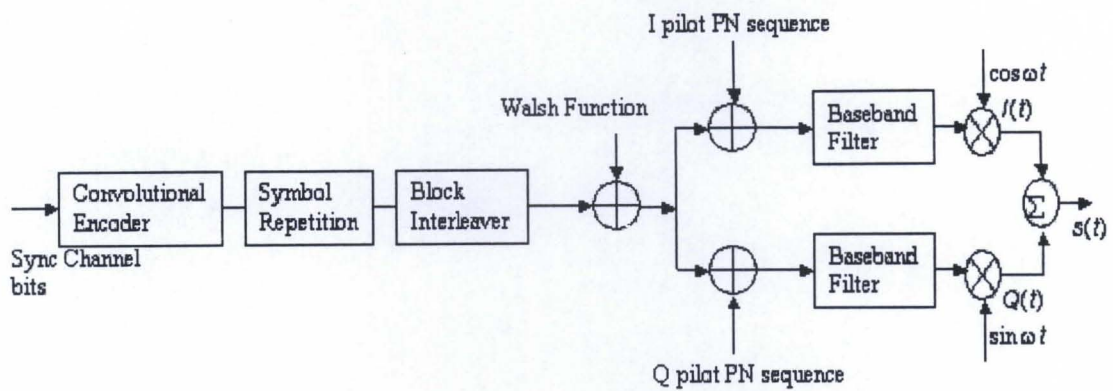


Figure 2.5: Forward link sync channel [20,95].

2.4.1.3 *Paging channel*: Figure 2.6 shows a CDMA paging channel structure. The paging channel carries the system overhead information and mobile station specific messages. A CDMA system uses data rate of either 4.6 or 9.6 kbps for the paging channel while WCDMA uses 16 kbps. The data is convolutionally encoded and processed by a symbol repetition and block interleaver stage. The interleaved data is passed through a data scrambler to prevent long sequences of ‘0’s and ‘1’s from appearing in the data stream.

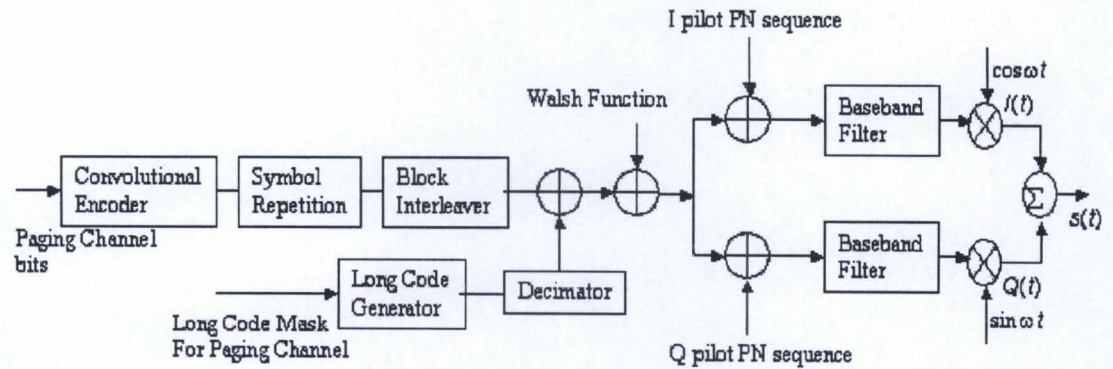


Figure 2.6: Forward link paging channel [20,95]

Data scrambling is accomplished by performing the modulo-2 sum of the interleaver output with every 64th bit from a long code generator. The use of 1 out of 64 bits is called decimation. WCDMA does not use a scrambler [9]. Finally, the resultant signal is spread by a specific Walsh function assigned to that paging channel and further spread by a short PN sequence assigned to the serving sector.

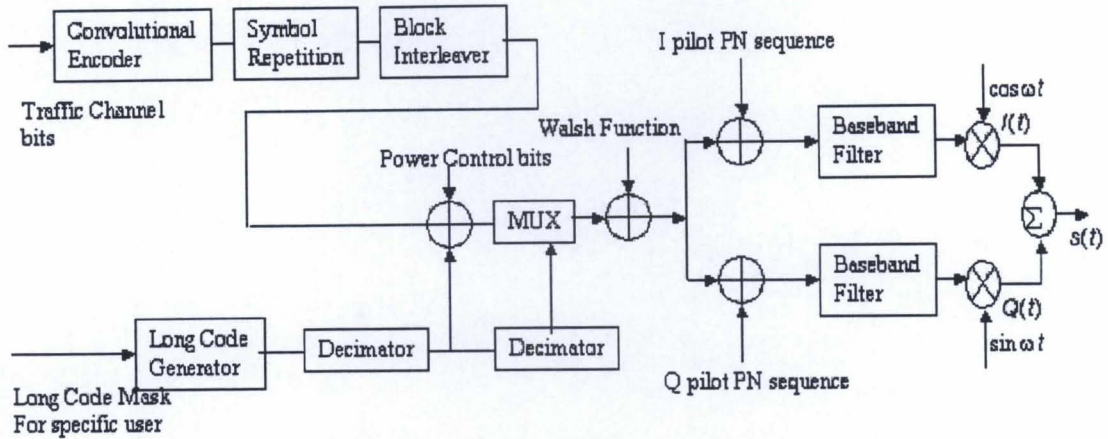


Figure 2.7: Forward link traffic channel [20,95]

2.4.1.4 Traffic channel: The traffic channel is used for the transmission of user and signaling information to a specific mobile station. The structure of the forward traffic channel is shown in Figure 2.7. The structure of the traffic channel is similar to that of the paging channel, the only difference is that traffic channel contains multiplexed power control bits. In CDMA the data and signaling bits are multiplexed together in the channel. WCDMA multiplexes the channel after the symbol repetition and always processes a separate signaling channel. A CDMA system scrambles the data using a decimated long code and multiplexes the power control bits. The multiplexed signal is then further scrambled by the decimated long code and modulo-2 added to Walsh or Hadamard codes for the channel being used.

2.4.2 Reverse link

The reverse link consists of only two channels: access channel and traffic channel. Due to the noncoherent nature of the reverse link, Walsh codes are not used for channelization but PN codes are used to distinguish the signals from different mobile stations. In a WCDMA system a pilot signal, which can be recovered on either side, is sent, so Walsh or Hadamard codes are used in both directions. Figure 2.8 shows the access channel structure.

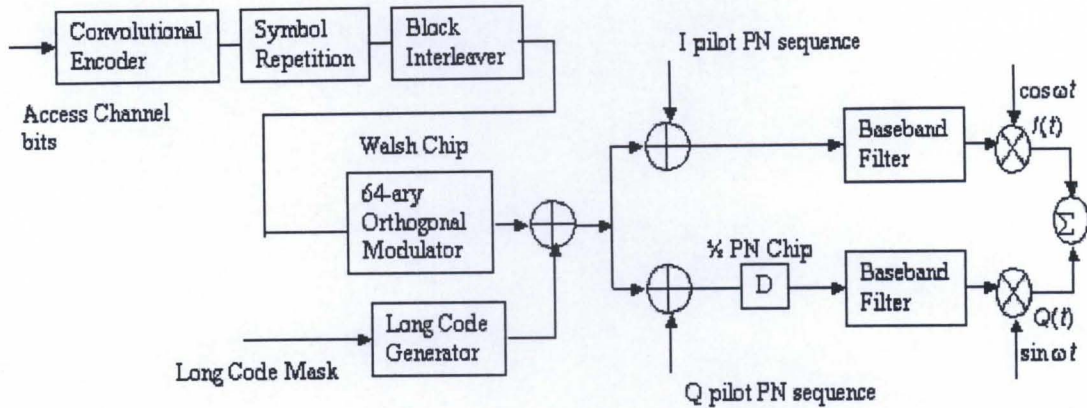


Figure 2.8: Reverse link access channel [20,95]

2.4.2.1 Access channel: The access channel is used by the mobile station to initiate communication with the base station and to respond to the paging channel messages. The channel operates at 4.8 kbps in CDMA and 16 kbps for WCDMA. The information bits are convolutionally encoded and processed by symbol repetition and interleaving functions. In this channel the repetition and interleaving stages are different for CDMA and WCDMA [9]. In CDMA each code symbol processes through an orthogonal 64-ary modulator to generate a Walsh symbol for each input symbol, but in WCDMA, the output of the repetition stage is modulo-2 added to a Walsh code for the access channel. M-ary modulation techniques in DSSSS is discussed in [33] and [96]. The M-ary modulator converts the incoming data symbols into complex valued symbols, the M-ary data modulator can convert m incoming data symbols into one of M ($M = 2^m$) possible data symbols represented by K channel symbols. These can then be transmitted using binary, balanced quaternary, or complex spreading schemes. The M-ary modulator spreads the transmitted signal in the frequency domain. The orthogonally modulated data are then spread by PN sequences. Long PN codes are used to distinguish the access channel from other channels. The data is further scrambled in the I and Q paths by short PN sequences. The data in the Q path is delayed by one-half a PN chip because the reverse link uses OQPSK modulation. The ease of bit synchronization at the receiver and the fact that the difference in the time alignment in the bit stream has no impact on the output power spectral density of OQPSK are the

main advantages of OQPSK over QPSK [21]. A response message or a request message are the two types of message sent over the access channel.

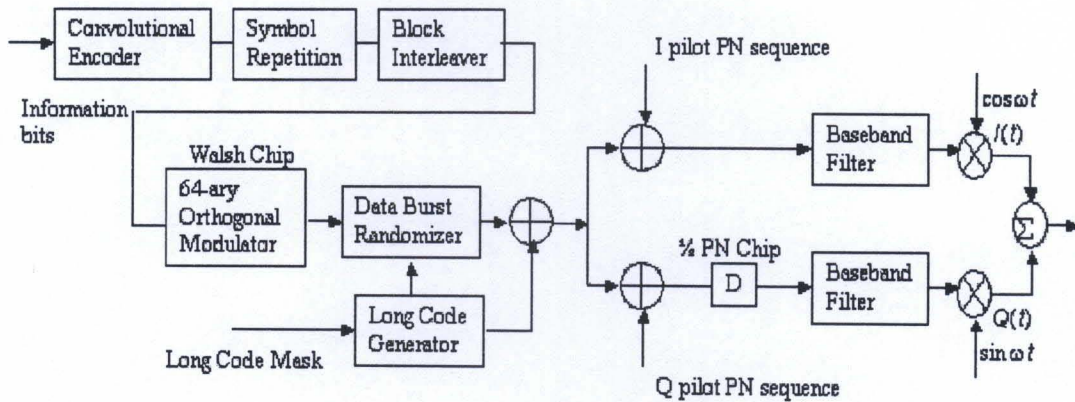


Figure 2.9: Reverse link traffic channel [20,95]

2.4.2.2 Traffic channel: Figure 2.9 shows the reverse link traffic channel structure. The reverse link traffic channel is used for the transmission of user and signaling information to the base station. The structure is similar to the access channel; the only difference is the data burst randomizer. The orthogonally modulated data is fed into the data burst randomizer in order to take advantage of voice activity factor on the reverse link. The data burst randomizer generates a masking pattern of '0's and '1's that randomly masks out redundant data. The output of the randomizer is then spread by the long code. The WCDMA systems do not use a randomizer.

2.5 Benefits of CDMA

CDMA has gained international acceptance by wireless system providers as an upgrade from conventional wireless systems. Some of the features of the CDMA are discussed below.

- Increased capacity
- Enhanced privacy and security
- No hard handoff

- Simplified system planning reducing deployment and operating costs
- Reduced average transmitted power, thus increasing talk time for portable devices
- Improved voice quality, eliminating the audible effects of multipath fading.
- Improved coverage characteristics which reduce number of cell sites.
- Coexistence with analog systems

Because of these attractive benefits, CDMA has gained considerable attention amongst cellular providers. Due to the rapid rise in the number of cellular users in wireless communication there is a need for a system that can support a range of services such as high speed data with larger system capacity and multimedia. The most promising candidate, Wideband Code Division Multiple Access (WCDMA), is being developed throughout the world [3-4].

2.6 Wideband Code Division Multiple Access (WCDMA)

The continuous growth in traffic volume and emergence of new services has begun to change the structure of wireless networks. WCDMA is based on the wide band DS-SS-CDMA technology. WCDMA systems are similar to the CDMA systems, but there are some differences in the physical layer, protocol and air interface standards. From an implementation point of view, this thesis focuses mainly on the physical layer and the interface standards. One of the main differences of WCDMA is that the Walsh or Hadamard sequences can be used in both forward and reverse directions. Fast Transmit Power Control (TPC) is another added advantage of WCDMA. However the most recent research results on wireless transmission technology have been incorporated into present WCDMA to improve performance and flexibility.

WCDMA has been chosen as the fundamental radio access technology for UMTS/IMTS-2000 in both Europe and Japan. Compared to the second generation narrow band CDMA, the WCDMA radio interface offers significant improvements, in addition to the support of higher data rate. Some important concepts of WCDMA are

the introduction of intercell asynchronous operation and pilot channels associated with individual data channels. The main technical features of WCDMA are [2,4,17]:

1. *Fast cell search under intercell asynchronous operation:* Intercell asynchronous systems can more easily realize continuous system deployment from outdoor to indoors than intercell synchronous system. This is because the previous stage does not require any external timing source such as Global Positioning System (GPS) used in IS95.

The fast cell search under intercell asynchronous operation can be explained as follows. The control channels in the forward link of all cell sites reuse the same short spreading code and the scramble code sequence is periodically masked over one symbol duration so that the particular code appears periodically during the scramble code [17,4]. The group identification code indicating the code group, to which the scramble code of each cell site belongs, is transmitted in parallel during the masking period. The cell search algorithm detects and identifies the scramble code group and finally identifies the group identity code by cross correlating the received signal with all scramble code candidates.

2. *Fast Transmit Power Control (TPC) on both reverse and forward links:* The time-multiplexed pilot radio frame structure used in WCDMA supports Signal to Interference Ratio (SIR) measurement. The SIR is measured and compared with the target SIR to generate a TPC command which is transmitted every 0.625ms to the mobile station to raise or lower the transmit power by 1dB. Target SIR values are controlled by an outer power control loop. This outer loop measures the link quality, typically a combination of frame and its bit error rates depending on the service, and adjusts the SIR targets accordingly. This ensures that the lowest possible SIR target is used at all times resulting in maximum capacity. The outer loop is used to independently control the relative power of the different physical channels belonging to the same connection. The pilot and the data symbols are used to measure instantaneous received signal power but only pilot symbols are used to measure the interference plus background noise. Fast TPC is applied to both the reverse and forward links. The instantaneous

SIR on each forward link varies in a random manner; this leads to the use of fast TPC that can increase the link capacity in both directions.

3. *Coherent Rake Combining*: Coherent detection will improve the performance of the uplink up to 3 dB compared to noncoherent reception used by the second generation CDMA system. Figure 2.10 shows a Coherent RAKE receiver structure. The matched filter resolves the frequency-selective multipath channel into M frequency non-selective propagation paths with different time delays. The output of the coherent RAKE combiner is represented at the n^{th} symbol position of the k^{th} slot associated with the m^{th} propagation path, $m=0,1, \dots, M-1$, as [17]:

$$\tilde{d}(n,k) = \sum_{m=0}^{M-1} r_m(n,k) \tilde{\xi}_m^*(k) \quad \text{-----}(2.2)$$

where $\tilde{\xi}_m^*(k)$ is the channel estimate and $r_m(n,k)$ is the matched filter output.

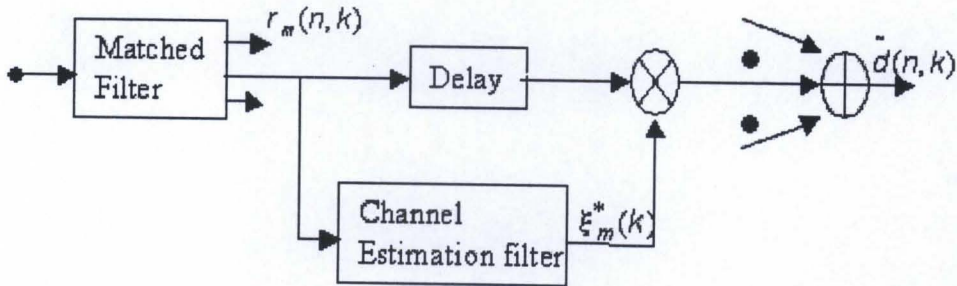


Figure 2.10 Coherent RAKE receiver structure [17]

4. *Coherent tracking of spreading code*: A non-coherent delay-locked tracking loop suffers from tracking jitter due to the noise enhancement arising from the square-law detector. This can be overcome by using coherent delay-locked tracking loop which leads to the improvement of transmission performance [17].

2.6.1 MAC and Radio link control

The Medium Access Protocol (MAC) and Radio Link Control (RLC) are responsible for transferring real time and non-real time services [2,4]. The transfer of non-real time data transfer includes the possibility of low-level automatic repeat requests offering higher protocol layers reliable data transfer. The MAC layer controls the multiplexing of data streams originating from different services. All the RLC protocol data units in WCDMA have the same size regardless of the transmission rate. In the case of networks, CDMA cell coverage is dependent on the cell load. WCDMA employs admission control and congestion, so the cell load and thus coverage can be controlled.

2.7 Summary

In order to provide global roaming the standardization of third generation mobile communications systems is now rapidly progressing all over the world. These systems, called International Mobile Telecommunications-2000 (IMT2000) in the International Telecommunication Union (ITU), will extend the services provided by second generation systems. Standardization of service capabilities includes standardization of bearers, quality of service parameters and additional mechanisms needed to realize the required services. These additional mechanisms include the service creation functionality of various network elements and the communication between element and the storage of associated data. Such standardized service capabilities should provide a defined platform which will enable support of speech, video, multimedia, access to Internet, messaging, data etc. A set of service capabilities should enable users, service providers and network operators to define services themselves according to their needs. WCDMA promises flexibility, provision for multirate services, packet data, and seamless interfrequency handover. The proposed air interface standard and the technical parameters of WCDMA are summarized in Table 2.2 [2-5,8]. Since there are so many possible combinations of settings, Table 2.3 show the parameters used in this thesis.

Channel Bandwidth		5,10,20 MHz
Chip rate		4.096/8.192/16.384 Mcps
Multiple Access		DS-CDMA
Roll-off factor		0.22
Frame length	Variable-rate speech	10 or 20 ms
	Packet data	10-80 ms
Modulation	Spreading	Balanced QPSK (downlink) Dual channel QPSK (Uplink) Complex spreading circuit
	Data	QPSK (downlink) BPSK (uplink)
Coherent detection		Pilot symbol assisted
Channel coding		Convolutional and Turbo coding
Scrambling code		10 ms
Interleaving		10/20/40/80 ms
Multirate		Variable spreading and multicode
Spreading factor		4-256 (4.096Mchips/s)
Spreading	Downlink	Variable length orthogonal sequences for channel separation Gold sequence for user and cell separation
	Uplink	Variable length orthogonal sequences for channel separation Gold sequence 2^{41} for user separation
Handover		Soft handover Interfrequency handover
Power control		Open and fast closed loop (1600 Hz)
Power control step size		0.25-1.5 dB
Inter base station timing		Asynchronous

Table 2.2: Parameters of WCDMA

Processing Gain		32x0.5x3	
Modulation	Data	QPSK	
	Spreading	QPSK	
Channel Coding		Convolutional Coding, R=1/3, K=9	
Frame Structure	Slot	Pilot	4 symbols
		Data	76 symbols
	Frame	0.625 ms X 16 Slots	
Chip Rate		4.096 Mcps	
Interleaving		10ms	
Spreading Code		Gold Code	
Channel Estimation		Linear Interpolation	
Demodulation		Pilot symbol assisted coherent detection	
Channel decoding		Soft-decision Viterbi decoding	

Table 2.3: Link parameters used for simulation

2.8 Conclusion

This chapter covered the fundamental principles of spread spectrum systems and for the implementation aspect, focused on the physical layer of IS-95 CDMA and underlying differences in the physical layer between CDMA and WCDMA. A summary of WCDMA parameters and an overview of air interface standards were also discussed. WCDMA technology provides improved capacity and coverage due to the wider bandwidth and coherent uplink. The possibility of asynchronous operation and refined radio-network algorithms will further reduce the deployment cost of WCDMA. WCDMA systems support full utilization of adaptive antennas through the use of dedicated pilot symbols on both uplink and downlink thus leads to further improvement in the network and its traffic capacity. To conclude, WCDMA is a promising technology, ready to provide the basis for a true third generation mobile communications system with full multimedia capabilities.

Chapter 3

Antenna Arrays

3.1 Introduction

An antenna is usually defined as the structure associated with the region of transition between the guided wave and free space or vice versa. The antenna plays a vital role in modern mobile communication systems, especially in the case of increased antenna gain, which increases received signal strength.

A single antenna element has low values of directivity (gain). A practical objective of directive communication is an improvement in the received signal as measured relative to the prevailing noise. At the receive end of the communication link, the increase in directivity means that the antenna receives less interference from its signal environment. The directivity improves the Signal-to-Noise Ratio (SNR). One useful method of achieving directive antenna characteristics is an arrangement of several individual antennas of the same kind so spaced and phased that their individual contributions add in one preferred direction while they cancel in others. This type of arrangement is known as an antenna array. The individual antenna in an array is called an element. An array can be arranged in various configurations such as straight line, circle, square, arc, etc.

An array that consists of a number of equally spaced individual antennas set up along a straight line is called a linear array, while two-dimensional planar arrays consist of elements oriented on a geometric grid in a plane. Rectangular arrays may be thought as

a set of linear arrays placed next to each other, equally spaced, forming a two-dimensional array. In this thesis, the proposed receiver makes use of a linear array with six antenna elements.

Linear and planar arrays can be designed with either a fixed beam, or a scanned beam, which is rapidly positioned in space by means of electromechanically or electronically actuated devices in the feed lines behind the array radiators. These devices change the phase progression along the array. The patterns of the linear arrays can be analysed in terms of the main beam, side lobes, and grating lobes. A broadside array is one in which the direction of maximum radiation is perpendicular, or almost perpendicular to the line (or plane) of the array. Figure 3.1 shows the broadside array pattern for a linear array placed on the z-axis.

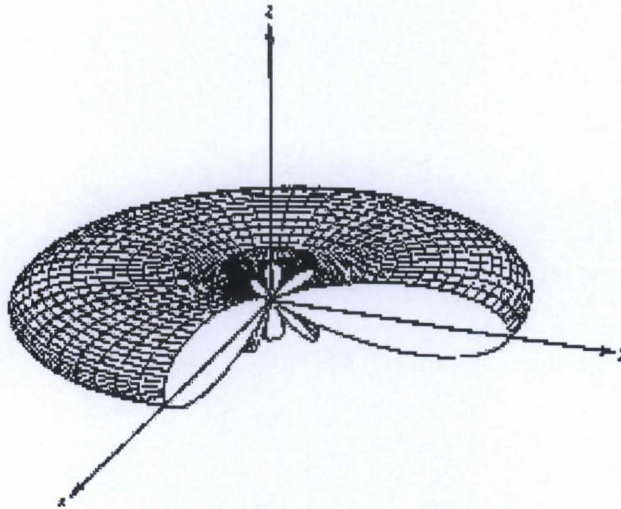


Figure 3.1: Broadside array pattern for a linear array placed on the z-axis

The elements of a linear array may also be driven by currents with a phase progressively varying along the array axis in such a way as to make the radiation substantially unidirectional. This array is referred to as end-fire array. Figure 3.2 shows the end-fire array patterns for a linear array placed on the z-axis.

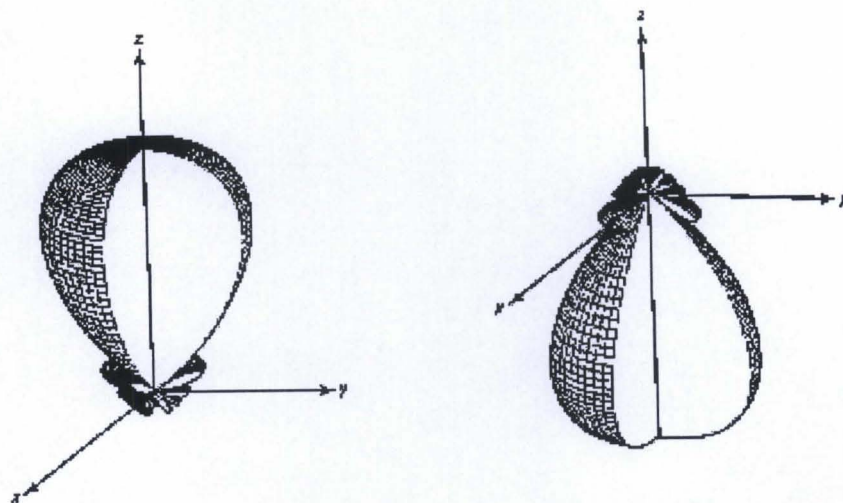


Figure 3.2: End-fire array patterns for a linear array placed on the z-axis

The main thrust in the development of antenna arrays is the provision of interference protection, reliable signal acquisition and tracking in communication systems. In [48], the capabilities of antenna arrays are discussed and tested for communication systems in real environments.

3.2 Antenna arrays in mobile communication

An application of antenna arrays has been suggested in recent years for mobile communication systems to overcome the problem of limited channel bandwidth, thereby satisfying an ever growing demand for a large number of mobiles on communication channels [46-47]. It has been shown by many studies that when an array is appropriately used in a mobile communication system, it helps in improving the system performance by increasing the channel capacity and spectrum efficiency, extending range coverage, tailoring beam shape, steering multiple beams to track many mobiles, and compensating aperture distortion electronically [40]. An array of antennas is used in a variety of ways to improve the performance of a communication system. In this thesis one of the most important effects of the consideration of an array is its

capability to cancel the cochannel interference, which is the main cause of signal impairment in CDMA.

The gain of the antenna is an important factor in determining the performance of any communication system. Electronically steered antennas based on phased array antenna techniques have been developed for applications in the military and aerospace industries. Such systems tend to be complex, expensive and high performance in nature [72]. Typical applications include long range surveillance radar, active jammer rejection in communication systems and multibeam antennas for space communication systems. With the continued advance in electronic integration techniques, the technology associated with adaptive antennas has now progressed to the stage where it may be considered for commercial communication applications.

3.3 Adaptive antenna arrays

An adaptive antenna array is an array that continuously adjusts its own pattern by means of feedback control. Adaptive antenna techniques offer the possibility of increasing the performance of mobile radio communication systems by maximising directional gain and enhancing protection against multipath conditions. Conventional communications and radar antenna systems are susceptible to degradation in SNR performance caused by undesired noise, which intrudes through the antenna sidelobes and mainlobes.

An adaptive antenna is one whose parameters are caused to vary as a function of the interference field so that it always stays in an optimal or fairly optimal condition. The problem with fixed parameter optimal solutions is that interference is seldom constant in space or time and an antenna which is initially optimum in some location will rapidly become sub optimal as the interference changes either because of the appearance of new interference transmissions, changes in local scattering environment through movement of vehicles, aircraft, or changes in operating frequency. At the receiver adaptive antennas adjust their directional patterns so as to maximise the signal-to-noise

ratio of the desired signal which is received in the presence of interference and noise. In other words an adaptive array is a system consisting of an array of antenna elements and a real-time adaptive receiver processor which, given a beam-steering command, samples its current environment and then automatically proceeds to adjust its element control weights towards optimisation of the output SNR in accordance with a selected algorithm. These antenna systems are sometimes referred to as “smart” arrays [36]. Adaptive arrays promise a possible solution to serious interference problems due to motion of the antenna, poor siting conditions, multipath and a changing interference environment. This is achieved through their flexible capabilities for automatic null steering and notching in the spatial domain, the frequency domain and in polarization.

In order to maintain the performance degradation of a communication system at an acceptable level as the radio traffic increases, it is necessary to adopt measures to improve the mutual interaction robustness. Several systems may be considered, spread spectrum techniques appear to be one of the technique to offer a reduction of the vulnerability of a communication system [6]. As an alternative, adaptive arrays sense the interference source and suppress them automatically, improving the performance of a mobile system, without any *a priori* knowledge of the interference location.

It is noticeable that an adaptive antenna array can achieve more reliable communication, in comparison with a conventional array [46]. If a single antenna of a conventional array fails, the sidelobe level and the mainlobe width increase, and the mainlobe and null locations are modified. Strict control of null placement for an adaptive array results in only a slight deterioration of the SNR. Thus, more reliable communications can be achieved.

3.4 Beam steering or beamforming

Adaptive Array Antenna (AAA) systems are a major attraction in mobile communication systems because of their ability to automatically steer nulls onto undesired sources of interference, thereby reducing output noise and enhancing the

detection of desired signals. These types of systems contain an array of antenna elements and a real time adaptive processor or beamformer, which has feed back control over the elements weights. The process of combining the signals from different antenna elements in an array is called beamforming. The signal from each antenna element is adopted in such a way that a desired signal is formed by the beamformer. The term beamforming *“relates to the function performed by a device or apparatus in which energy radiated by an aperture antenna is focussed along a specific direction in space”* [63].

For a given array, the beam may be focussed along specific directions by mechanically moving the array. This is known as mechanical beam steering. Beam steering or forming can also be accomplished by appropriately delaying the signals before combining them. This process is known as electronic steering, because there are no mechanical movements. For narrow band signals, phase shifters are used to change the phase of the signals before they are combined. The required delay can also be accomplished by inserting varying lengths of transmission line between the antenna elements and combiner. Changing the combinations of different lengths of the cables leads to different pointing directions. Switching between different directions is sometimes referred to as beam switching.

In conventional beamforming, only the phase of the signals from the different elements is adjusted to point a beam in a desired direction. The gain of each signal is kept the same. This determines the total gain of the array in the beam pointing direction. When the main beam is pointed in different directions by adjusting various phases, the relative positions of the sidelobes with respect to the mainlobe do not change, that is, the shape of the antenna pattern is fixed. This can be changed by adjusting the gain and phase of each signal to shape the pattern as required. The amount of change depends upon the number of elements in the array [48].

The gain and phase applied to the signals derived from each element may be thought of as a single complex quantity hereafter referred to as the weighting applied to the

signals. If there is only a single antenna element, no amount of weighting can change the pattern of that antenna. With two or more elements, changing of weighting of one element relative to other may adjust the pattern to the desired value at one place, that is, one is able to place one minima or maxima depending on element pattern.

The flexibility of array weighting to being adjusted to specify the array pattern is an important property. This may be exploited to cancel directional sources operating at the same frequency as that of the desired source provided these are not in the direction of the desired source. In situations where the directions of these interferences are known, cancellation is possible by placing the nulls in the pattern corresponding to these directions and simultaneously steering the main beam in the direction of the desired signal. Beamforming in this way, where nulls are placed in the directions of interferences, is normally known as null beamforming or null steering [46]. The cancellation of one interference by placing a null in the pattern uses one degree of the freedom of the array.

Null beamforming uses the directions of sources toward which nulls are placed for estimating the required weighting on each element. There are other schemes that do not require directions of sources. A constrained beamforming scheme uses the steering vector associated with the desired signal and then estimates the weights by solving an optimisation problem. Knowledge of the steering vector associated with the desired signal is required to protect the signal from being cancelled. A reference signal is used in situations where the steering vector associated with signal is not available. Beamforming using a reference signal is discussed in [55].

AAA systems may have either analogue or digital processor (beamformer) for the determination of the array element weight matrix. Some of the beamforming algorithms can be implemented in either analog or digital form.

3.3.1 Analogue beamforming

The signals received in each antenna element can be subjected to various forms of signal processing, wherein phase or amplitude adjustments are made to produce outputs that can provide concurrent angular information for signals arriving from different angles or directions in space. When the outputs from the antenna array elements is combined using some passive phasing network, the phasing will usually arrange for the output of all the antenna elements to add coherently for a given direction. Another phasing network can be implemented to get the desired information of the signals arriving from different region in space. Usually analog beamforming will be carried out either in RF or IF. Figure 3.3 gives an example of an analog beamformer. An analog beamforming network usually consists of devices such as phase shifters and power dividers which are used to adjust the amplitude and phases of the elemental signals in such a way as to form a desired beam.

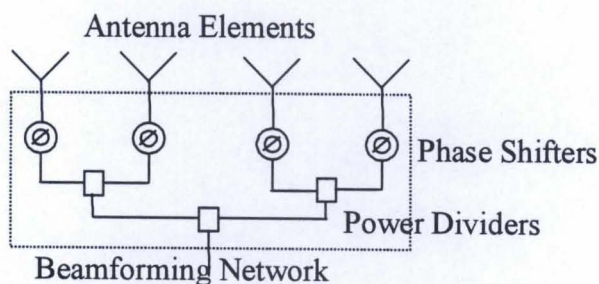


Figure 3.3: An analog beamforming network [63]

The above topology is capable of forming only one beam. It only provides for uniform weighting. It is sometimes desirable to form multiple beams that are offset by finite angles from each other. The design of a multiple-beam beamforming network is much more complicated than that of a single-beam beamforming network. A multiple-beam beamforming network is known as a beamforming matrix. In [38] and [43] the butler matrix is discussed. In a beamforming matrix, an array of hybrid junctions and fixed phase-shifters are used to achieve multiple beams.

3.3.2 Digital beamforming

The interest in digital beamformer implementation is further enhanced by its potential use in satellite communication systems where size, weight and power consumption become important design factors. Also technological advances in digital signal processing provide the possibility of developing a digital receiver. If such a receiver can be achieved, its performance may be superior in comparison to a conventional analog approach due to three major differences [90]:

- (a) More information can be maintained in the digital approach.
- (b) The digitized data can be stored for long periods of time.
- (c) More flexible signal processing methods are available to obtain the desired information directly from digitized signals.

Digital beamforming is a mixture of antenna and digital technology. The antenna converts the spatiotemporal signals into strictly temporal signals, thereby making them available to a variety of signal processing techniques to extract the desired information carried by these signals. An optimum antenna is one that carries out the conversion of the signals arriving at its face without introducing any distortions to the signals. Adjusting gains and phases of each element may be one way of canceling unwanted interferences to obtain maximum output SNR. It is for this reason that a digital beamforming antenna might be considered to be an optimum antenna [63]. This means that its sampled outputs represent all of the data arriving at the antenna aperture. In digital beamforming the major advantage is that once the RF information is captured in the form of a digital stream, the way is clear for the application of a multitude of digital signal processing techniques and algorithms to the digital spatial data. The signals received at each of the antenna elements are down converted into two streams of base band signals representing I and Q signals that have the same amplitude and phase as that of signal received at each element of the array.

The analog to digital conversion of the signals plays an important role in the beamforming technology. The receivers perform the functions of frequency conversion, filtering, and amplification of the signal to a power level that is commensurate with the

input requirements of the A/D converters or with the output power requirements. Since the elemental receivers are a significant factor in determining the cost of a digital beamforming antenna, it is important when designing receivers, to adopt an architecture that leads to receivers that are low in cost and yet meet performance requirements.

Figure 3.4 shows a simple structure that can be used for digital beamforming. The choice of the weight vector \mathbf{W} is based on the statistics of the signal vector \mathbf{X} received at the antenna array. The objective is to optimize the beamformer response with respect

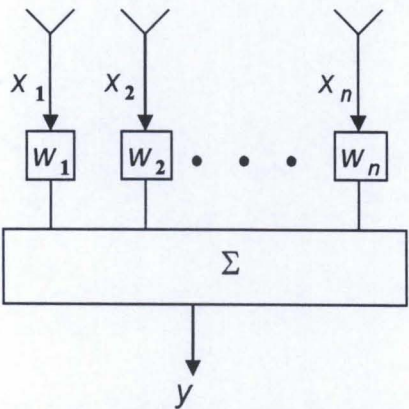


Figure 3.4: Digital beamforming network [63]

to a prescribed criterion, so that the output Y contains minimum contribution of noise and interference from the channel. There are a number of criteria for calculating the optimal weights. The criteria for choosing the optimal weights used in this project is the Minimum Mean Square Error (MMSE) algorithm. This algorithm is derived and explained in Appendix (A-1). Choosing the optimal weights plays an important role in beamforming. A perfect beamformer must satisfy two requirements. Firstly, the steering capability to protect the targeted signal and secondly, minimizing the effects of interference from different sources. This can be achieved by minimizing the average power (variance) of the beamformer output.

In order to enable a beamformer to respond to an unknown interference environment, it should be made adaptive in such a way that it places nulls in the directions of the

sources of interference automatically and in real time. By adapting the optimal weights in real time the beamformer can increase the system performance.

The adaptation process that is based on MMSE is the Least Mean Square (LMS) algorithm. The system operates with knowledge of the direction of arrival and spectrum of the signal, but with no knowledge of the noise field. Figure 3.5 shows the basic adaptive beamforming element. The input signals $x_1(t), \dots, x_n(t)$ are multiplied with the weights w_1, \dots, w_n as shown in Figure 3.5.

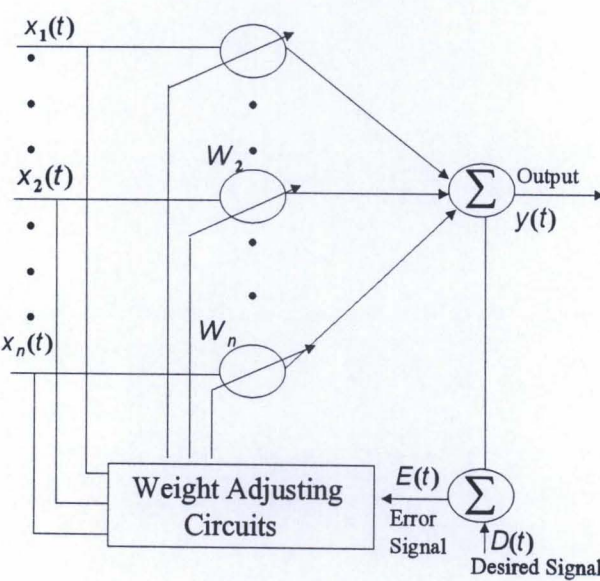


Figure 3.5: Adaptive beamforming network [46]

The weights will be updated in real time. The purpose of adaptation or the weight updating process is to find a set of weights that will permit the output signal of the adaptive element at each instant of time to equal or be as close to the desired signal $D(t)$.

3.4 Least Mean Square (LMS) algorithm

The operation of the LMS algorithm is descriptive of a feedback control system [52]. Due to the simplicity of the LMS algorithm [47], it is the most widely used adaptive algorithm in currently implemented systems. The application of the LMS algorithm to estimate the optimal weights of an array is widespread, and its study has been of considerable interest for some time now. It is mostly applicable when the weights are updated using a reference signal and no knowledge of the direction of the signal is utilized. The algorithm updates the weights at each iteration by estimating the gradient of the quadratic surface and then moving the weights in the negative direction of the gradient by a small amount. The mean-square-error defined in Appendix A1 (Eq 9-6) is a quadratic function of the weight values while the components of the gradient of the mean-square-error function are the partial derivatives of the mean-square-error with respect to the weight values. The constant that determines this incremental weight adaptation is normally referred to as the step size. When this step size is small enough, the process leads these estimated weights to the optimal weights. The convergence and the transient behavior of these weights, along with their covariance, characterizes the LMS algorithm. The way the step size and the process of gradient estimation affects these parameters is of great practical importance.

The LMS algorithm is based on the principle of steepest descent [70]. Changes in the weight vector are made along the direction of the estimated gradient vector.

Accordingly,

$$w(n+1) = w(n) + \mu \nabla(j) \quad \text{----- (3.1)}$$

where $w(n)$ = weight vector before adaptation

$w(n+1)$ = Weight vector after adaptation

μ = Gain constant controlling rate of convergence and stability ($\mu < 0$)

$\nabla(j)$ = Estimated gradient vector

The derivation of the LMS algorithm is discussed in Appendix A-2.

3.5 Applications of antenna arrays in mobile communications [45]

Arrays can be used in various configurations for mobile communications. Antenna arrays can combat multipath fading of the desired signal and suppress interfering signals, thereby increasing both the performance and capacity of a wireless system. The improvements in the system performance and capacity in due to the use of antenna arrays in CDMA mobile communication systems are discussed in [58-60]. Performance evaluation of adaptive arrays in a GSM base station is discussed in [57]. In most currently deployed systems, antenna arrays with spatial processing techniques can provide substantial improvement. However, various types of spatial processing techniques have different advantages and disadvantages in each of the system types.

Today's cellular systems usually use 120° sectorization at each base station, i.e, each base station uses three separate sets of antennas for each 120° sector [9], with dual receive diversity in each sector. Since each sector uses a different frequency to reduce cochannel interference, handoffs between sectors are required. For higher performance, small sectors can be used, but this results in too many handoffs. But with the use of antenna diversity, handoffs between beams can be avoided. In this section some of the applications of antenna arrays used in mobile communications are discussed.

3.5.1 Formation of multiple and adaptive beams

Antenna arrays used in the base station can be used to form multiple beams to cover the whole cell site. For example three beams with a beamwidth of 120° each or six beams with a beamwidth of 60° each may be formed. Each beam then may be treated as a separate cell, and the frequency assignment may be performed in the usual manner. The normal handoff process is used to handover the mobiles from one beam to another beam when the mobiles cross the boundary of the cells.

Arrays are also used to find the location of each mobile, and then beams are formed to cover different mobiles or groups of mobiles. An array of antennas with the capability to form independent beams may be used in the base station is discussed in [49] and

[50]. Each beam may be considered as a cochannel cell and thus may be able to use the same frequency or code, so it is of great benefit for GSM and CDMA cellular systems.

3.5.2 Null formation:

The main beam can be steered towards the desired mobiles while the nulls are steered towards the interference users. Null formation of the antenna pattern toward cochannel cells help to reduce the cochannel interference. In other words it reduces the transmit power, which leads to increase in channel capacity. Figure 3.6 shows a sample antenna array pattern that demonstrates beamforming, where the main lobe is directed towards the desired user and the nulls are placed in the directions of sources of interference.

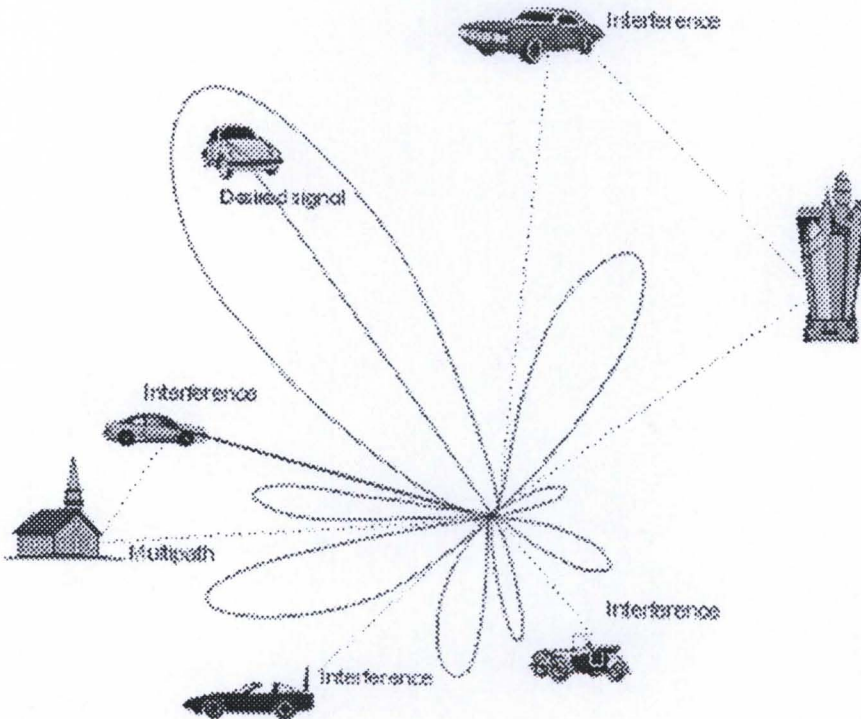


Figure 3.6: Antenna array pattern

3.5.3 Optimal combining:

Canceling unwanted cochannel interference while an array is operating in receiving mode is an effective use of an antenna array. This process combines signals received on various antennas in such a way that the contribution due to unwanted interferences is

reduced while that due to a desired signal is enhanced. Knowledge of the directions of the interferences is not essential to the process functionality; rather some characteristics of the desired signal are required to protect it from being cancelled. Optimal combining techniques that can be used to cancel the cochannel interferences in digital mobile radios is discussed in [42] and [97].

With the use of beamforming techniques, it is possible to combine the formation of nulls in the direction of unwanted mobiles while keeping the specified response in the direction of a desired mobile [50]. Beamforming is very effective when the desired signal is a point source. Its use in mobile communications is limited particularly in situations of multipaths. Optimal combining using a reference signal is more appropriate in this case. It requires a signal that is correlated with the desired signal. The algorithm then protects all the signals that are correlated with this reference signal and adds them in-phase to maximize their combined effect. It simultaneously cancels all the signals, which are not correlated to this reference signal, leading to the removal of cochannel interference. Thus, optimal combining using a reference signal is able to make use of multipath arrivals of the desired signal, whereas beamforming treats them as interferences and cancels them.

3.5.4 Dynamic cell formation:

The concept of adaptive beamforming allows for dynamic cell shaping. Instead of having cells of fixed size, the use of array antennas allows the formation of a cell based upon the traffic requirements, as shown in Figure 3.7. In order to adapt the system parameters to meet the traffic requirements, the base station requires an architecture that is capable of locating and tracking the mobile unit.

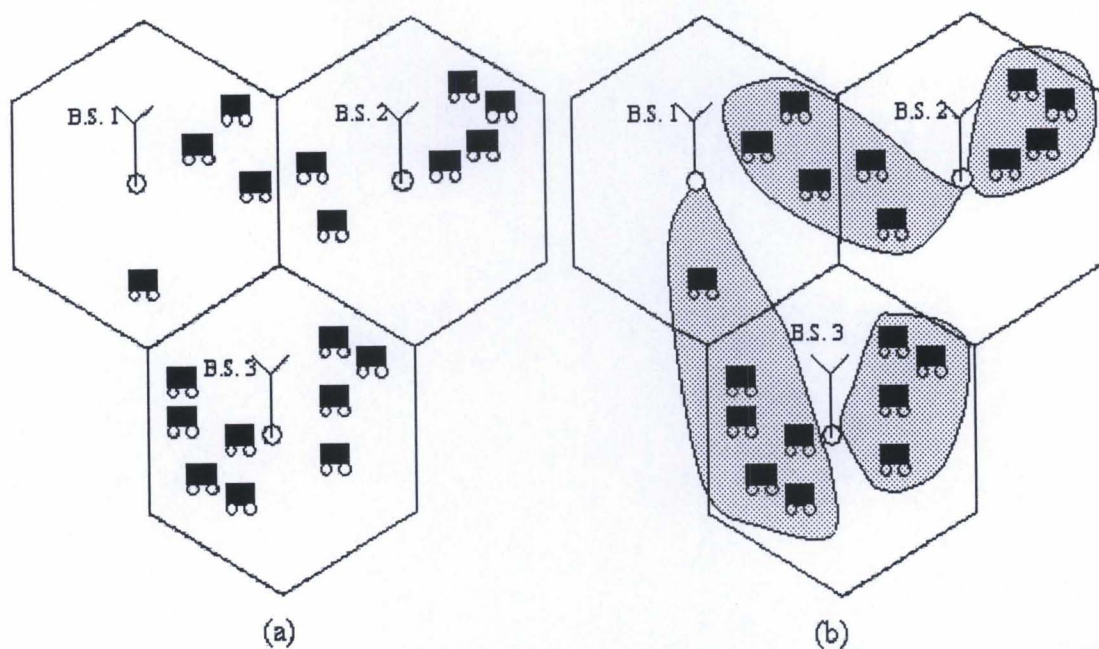


Figure 3.7: Cell shape based upon traffic requirements (a) cells of fixed shape (b) cells of dynamic shape. [45]

Technology that allows cell shapes and sizes to be changed based upon traffic conditions, channels to be assigned dynamically as per traffic needs, and transmitter power to be adapted according to the receiver requirements is referred to as intelligent technology [97]. Apart from variable cell size, adaptive transmitted power and dynamic channel allocation, this technology allows for variable speed for transmission and the use of adaptive modulation and demodulation techniques.

3.5.5 Feedback for beamforming:

In CDMA, transmit and receive modes use separate frequencies [10]. The knowledge of the directions of the mobile can be obtained during the receive mode and is used in the transmit mode to transmit in the directions of mobiles in a multiplexed manner. During the receive mode, once the position of the mobiles in a cell is determined and they are grouped in different clusters, the antenna pattern is adjusted such that the main beam is pointed towards one cluster while nulls are formed in the directions of other clusters. Alternatively the nulls can be directed towards mobiles in other cochannel cells. The process is repeated to transmit to all clusters.

Some of the base stations used in CDMA systems are able to form beams by estimating the array response vector corresponding to a mobile without knowledge of the direction of the mobiles [61]. The array response vector can be estimated from a received signal from a mobile with whom the base is code locked. The same is done in transmit mode by processing the feedback from the mobile to a special tone transmitted by the base. The array response vector can also be estimated from the knowledge of the user code or the reference signal in a CDMA system.

Most of the beamforming techniques use a reference signal from a desired user to estimate the weights of each antenna before combining the signals to form a desired signal. This approach is used and discussed in [64] and [67]. A specific transmitted signal is used to determine the initial weights. Once the initial weights are determined, the received signal may then serve as the reference for updating the weights and tracking the mobile later.

3.5.6 Blind estimate of cochannel signals:

Blind estimation of cochannel signals does not require the knowledge of the directions or other parameters of the mobile, but exploits the temporal structure that might exist in signals inherited from the source of their generation. Blind estimation using antenna arrays is discussed in [51]. A base station that consists of multiple sensors may be able to exploit the fact that signals arriving from different mobiles follow different paths and arrive at various elements at different times. This allows independent measurements of signals superimposed from different mobiles. This, along with the properties of the modulation technique used, allows separation of signals arriving from different mobiles. Thus, by using the measured signals at various elements of the array at the base, one is able to simultaneously separate all signals. This process is referred to as the blind estimation of cochannel signals. The temporal structure inherent in BPSK signals can be used to separate cochannel signals and can obtain the array weights [45].

It is possible for a vehicle mobile unit to carry an array of antennas and the required processing equipment. Optimal combining at the vehicular mobile is applicable for a

situations where desired signal and cochannel interferences arrive from many directions due to multipaths.

3.6 Benefits of using antenna arrays

Wireless communications systems are limited in performance and capacity by three major impairments. Firstly multipath fading, which is due to multipath signal components arriving at the receiver. The signals from these paths arrive with different phases, resulting in a received signal amplitude and phase that varies with antenna location, direction and polarization, as well as with time due to the movement in environment. This increases the required average signal power for a given bit error rate (BER). Secondly there is a delay spread due to the difference in the propagation delays among the multipaths. When the delay spread exceeds about 10 percent of the symbol duration, significant intersymbol interference can occur, which limits the maximum system data rate. The third impairment is cochannel interference. Cellular systems divide the available frequency channels into channel sets, using one channel per cell, with frequency reuse. This results in cochannel interference, which increases as the number of channel sets decreases. In this section the use of antenna arrays to overcome these impairments and the benefits thereof are discussed.

3.6.1 Reduction in cochannel interference:

The spatial filtering property of the antenna arrays can be exploited in the transmit and receive modes to reduce cochannel interference. In the transmitting mode, it can be used to focus radiated energy by forming a directive beam in a small area where a receiver is likely to be. This in turn means that there is less interference in other directions where the beam is not directed. Forming specialized beams with the nulls in the directions of other receivers in transmitting mode can further reduce the cochannel interference. This scheme deliberately reduces transmitted energy in the direction of cochannel receivers and requires knowledge of their positions. In [49], the analysis of a base station using multiple beams covering various mobile indicates that cochannel

interference decreases as the number of beam increases. The reduction of cochannel interference in the receive mode is a major strength of antenna arrays.

3.6.2 Spectrum efficiency and capacity improvement:

Spectrum efficiency refers to the amount of traffic in a given system that a certain spectrum allocation could handle. An increase in the number of users of the mobile communication systems without a loss of performance causes the spectrum efficiency to increase. Channel capacity refers to the maximum data rate a channel of given bandwidth can sustain. An improved channel capacity leads to more users of the specific data rate, implying better spectrum efficiency. In CDMA systems the capacity depends on the spreading gain and the corresponding number of equal-power cochannel interferers [95]. A multibeam antenna with N beams reduces the number of interferences per beam by a factor of N , and thereby increases the capacity.

Multipath fading is a severe problem for indoor mobile communications. However due to the slow speed of mobiles, the fading rate is much lower inside a building than outside. This means that there is enough time to compute antenna weights for optimal combining using slow converging algorithms. This offers the advantages of robustness and computational efficiency along with the possibility of its implementation using a single chip which is discussed in [60]. Using theoretical and computer simulations it is argued in [60] that using optimal combining at a base station with M antennas may lead to an M fold capacity improvement in indoor mobile communication systems.

3.6.3 Reduction in delay spread and multipath fading:

An array with the capability to form beams in certain directions and nulls in the others is able to reduce delay spread (caused by multipath propagation) in two ways [45]. Firstly, in the transmit mode, it focuses energy in the required direction, which helps to reduce multipath reflections causing a reduction in the delay spread. Secondly, in the receive mode, an antenna array provides compensation in multipath fading by diversity combining, by adding the signals belonging to different clusters after compensating for

delays, and by canceling delayed signals arriving from directions other than that of the main signal.

With diversity combining techniques the rate of fading can be reduced by increasing the signal level based upon the level of signal strength at different antennas, whereas in multipath cancellation methods, it is achieved by adjusting the beam pattern to accommodate nulls in the direction of late arrivals, assuming them to be as interferences. The signal arrives at the receiver in clusters after getting scattered and reflected from objects along the way. This is particularly true in scenarios with large buildings and hills where delayed arrivals are well separated. These clustered signals could be used constructively by grouping them as per their delays compared to a signal available from the shortest path. Individual paths of these delayed signals may be resolved by exploiting their temporal or spatial structure. The resolution of paths using temporal structures depends upon the bandwidth of the signal compared to the coherence bandwidth of the channel and increases as this bandwidth increases. In a CDMA system, the path may be resolved provided their relative delays are more than the chip period. When the paths are well separated spatially, an antenna array may be used. An antenna array can reduce delay spread by nulling the delayed signals arriving from different directions [40],[72].

3.6.4 Reduction in handoff rate: Proliferation of micro and macro cells increases the handoff rate. This can be overcome using an array of antennas. Instead of splitting the cell into smaller sizes, the capacity is increased by creating independent beams using more antennas. Each beam is adjusted or adapted as the mobile locations change. The beam follows a cluster of mobiles or a single mobile, as the case may be, and no handoff is necessary as long as the mobiles served by different beams using the same frequency do not cross each other.

The mobile unit location information available from antenna array technology can be used by the system to substantially improve handoffs. With sufficiently accurate

position estimates, prediction of velocities is possible which allows further improvements in handoff strategies [63].

3.6.5 Dynamic channel assignment: In mobile communications, channels are generally assigned in a fixed manner depending upon the position of a mobile and the available channels in the cell where the mobile is positioned. As the mobile crosses the cell boundary, a new channel is assigned. In this arrangement, the number of channels in a cell is normally fixed. The use of an array provides an opportunity to change the cell boundary and thus to allocate the number of channels in each cell as the demand changes due to changed traffic situations. This provides the means whereby a mobile or group of mobiles may be tracked as it moves and the cell boundary may be adjusted to suit this group.

Dynamic channel assignment is also possible in a fixed cell boundary system and may be able to reduce the frequency reuse factor up to a point where frequency reuse in each cell might be possible [31]. There may be situations when it is not possible to reduce cochannel interferences in certain channels, and the call may be dropped due to large BER caused by strong interferences. Such a situation may arise when a desired mobile is close to the cell boundary and the cochannel mobiles are near the desired mobile's base-station. This could be avoided by dynamic channel assignment, where the channel of a user is changed when the interference is above a certain level.

3.6.6 BER improvement: By reducing the cochannel interference and multipath fading, antenna arrays improve the quality of the services in the mobile communication systems which results in the improvement in BER for a required SNR. This relationship has been recognized by many authors [32], [67], [74] etc. The BER in a system normally decreases as the SNR is increased. These results, however, show that in an irreducible error rate environment, where no amount of SNR increase in a single antenna system would be able to reduce the BER, the system with an adaptive array is able to achieve large reductions.

3.6 Conclusion

This chapter provided a tutorial introduction to antenna arrays and their applications and benefits in mobile communication systems. A bright picture of the field has been described. Some of the issues may appear ambitious at present, however the above-mentioned benefits of antenna arrays are very attractive to cellular based service providers. From the preceding discussion it can be deduced that a system using an adaptive array should improve the performance of a mobile communication systems. As mentioned in the Chapter 2, this thesis considers adaptive array techniques as the principal means to suppress MAI in a CDMA receiver. A WCDMA AAA receiver is proposed for implementation in Chapter 4. The proposed receiver uses six antenna elements, which are equally spaced and separated by half a wavelength. This receiver makes use of pilot symbols for channel estimation. An MMSE algorithm is used to minimize the mean square error in the beamformer output. The antenna array weight is updated using the LMS algorithm. In order to achieve fast convergence of the antenna weights, the pilot symbols and the data symbols tentatively recovered after RAKE combining are used. The mathematical representation, overview and performance evaluation results of the receiver are discussed in Chapter 4.

Chapter 4

AAA receiver: An overview and evaluation

4.1 Introduction

Current 2.5G cellular systems (which are limited to voice, facsimile and low data rate services) are facing system capacity challenges due to the rapid rise in the number of users in wireless communication systems. The third generation of wireless communication systems provide a new range of services such as multimedia and high-speed data with larger system capacity. DS-CDMA technology is attractive for wireless access because of its numerous advantages over time-division multiple access (TDMA) and frequency-division multiple access (FDMA) schemes including soft handoff, exploitation of multipath fading through RAKE combining and direct capacity increase via the use of cell sectorization [17].

The capacity of a cellular system is limited by MAI and intersymbol interference (ISI). MAI is due to interference caused by the users sharing the same channel. If the delay spread (due to reflected paths) in a multipath channel is larger than a fraction of a symbol, the delayed components will cause ISI. In order to reduce both MAI and ISI an adaptive receiver beamforming scheme can be used. This results in improved uplink capacity by adjusting the beam pattern such that the effective Signal to Interference Noise Ratio (SINR) at the output of the beamformer is optimally increased. To counteract CCI, the beamformer places nulls in the directions of interference, while the gain in the direction of the transmitter is maintained constant [39]. In single tap (single

antenna system) diversity, the signal from the main path is considered as the signal of interest. If the multipath signals with large delay spread arrive at different angles, the single tap beam former rejects the ISI terms by placing nulls at the directions of multipath signals. Thus space-time processing can be used at the base station to minimize the MAI and ISI in mobile environments with large delay spread and will improve system performance [61].

Recent investigations [5], [87] claim that beamforming and power control are two promising approaches that can be used to reduce the amount of MAI. Significantly it was shown in [73] that joint beamforming and power control schemes minimize the total transmitted power in a network for a target SINR at each mobile. In [87], power allocation and beamforming are considered as a joint problem and the benefits of using antenna arrays at the base station includes an increase in network capacity and fast convergence of the power control algorithm.

Multipath fading, propagation loss and shadowing cause further channel degradation and reduce the system reverse link capacity. A fast Transmit Power Control (TPC) algorithm can minimize MAI by keeping the received SINR at a prescribed value. Multipath fading signals can be resolved, by a receiver matched filter, into several signal components that have propagated along different paths with different delays before combining. Usually a combination of RAKE combining and fast TPC is applied to the reverse link in practical systems and promises the reduction of multipath fading effects [92]. Another approach to reduce the MAI is Adaptive Antenna Array (AAA) techniques. In WCDMA, Pilot Symbol Assisted (PSA) channel estimation [2] is used for beamforming as well as for RAKE combining. It is shown in [66] that a PSA decision directed Coherent Adaptive Array Diversity (CAAD) receiver with six antenna elements can increase the link capacity up to 4.2 times that of a single antenna (per sector) case, and is 1.2 times that of a 6 branch antenna diversity reception with an antenna spacing of 10λ , Interference from high bit rate users is also reduced. PSA decision directed CAAD techniques are used in this thesis for the reverse link in the proposed AAA receiver. An AAA and path diversity (RAKE combiner) technique are

combined and applied to PSA reverse link with fast TPC, which is referred to as CAAD in [2].

An overview of an AAA receiver is presented in the next section as a precursor to the implementation of this receiver in an FPGA based software radio platform. In the proposed AAA receiver the array weights needed to generate the antenna pattern associated with each resolvable path are adaptively updated via the MMSE adaptive algorithm using both the pilot symbols and tentative detected data symbols after RAKE combining as the references.

4.2 AAA receiver

Figure 4.1 shows a block diagram of the AAA receiver using PSA CAAD techniques. The proposed receiver model is based on the receiver model presented in [66]. The mathematical representation of this model is presented in this section for continuity from [66]. The simulation model of the above receiver is also discussed in this section. The receiver consists of a matched filter for each antenna element and beamforming section for each received path. Input signals from multiple antenna elements are despread separately by multiple matched filters. The MMSE algorithm is then used to combine these multipath signals. A detailed description of the receiver is given in Section 4.2.2.

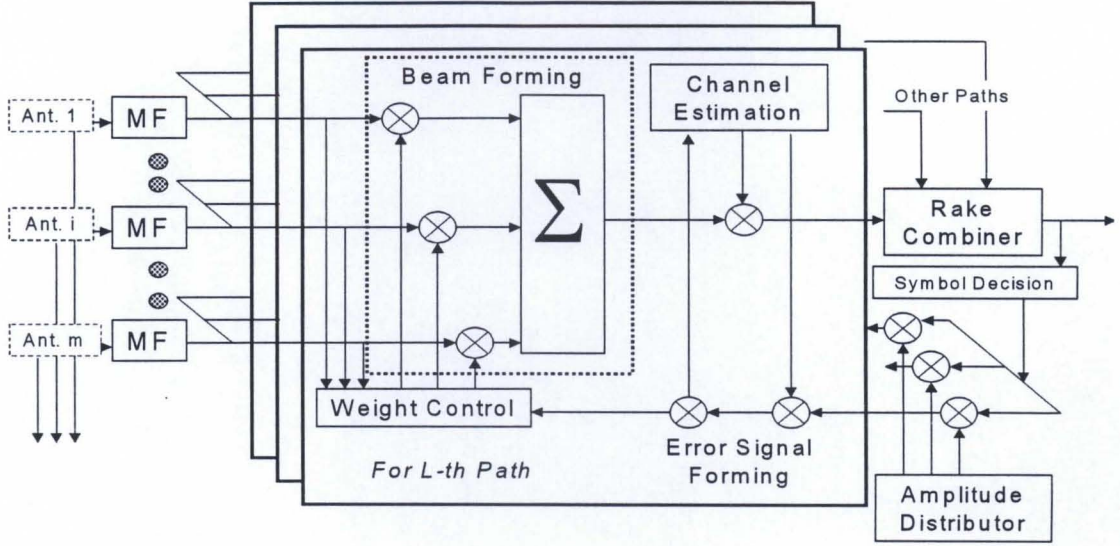


Figure 4.1: Functional block diagram of adaptive antenna array receiver

4.2.1: Mathematical representation

Let $s_k(t)$ be the transmitted signal of the k^{th} user, $k = 1, 2, \dots, K$. with unity power this can be represented in the complex form as:

$$s_k(t) = \sqrt{2}d_k(t)p_k(t) \quad \text{-----}(4.1)$$

where $d_k(t)$ and $p_k(t)$ are the QPSK modulated wave and spreading waveform represented as:

$$d_k(t) = \sum_{a=-\infty}^{\infty} [\exp m\Phi_k(a)]u(t/T - a)$$

$$p_k(t) = \sum_{b=-\infty}^{\infty} c_k(b)u(t/T_c - b) \quad \text{-----}(4.2)$$

where T_c is the chip interval of the spreading code sequence $c_k(b)$,

T is the QPSK data symbol, with $\Phi_k(a) \in \{q\pi/2; q = 0, 1, 2, 3\}$ being the QPSK modulation phase and $u(t) = 1$ for $0 \leq (t) < 1$ and $u(t) = 0$ elsewhere.

The channel associated with the k^{th} user has L_k resolvable multipaths having independently faded complex gains $\xi_{k,l}(t)$ and time delays $\tau_{k,l}, l = 1, 2, \dots, L_k$. At the receiver, assuming that each L_k multipath component arrives at M antennas with the same time delay $\tau_{k,l}$ for all m but with slightly different channel gains then the received composite signal $r^{(m)}(t)$ on the m^{th} antenna, $m = 1, 2, \dots, M$ is represented as:

$$r^{(m)}(t) = \sum_{k=1}^K \sum_{l=1}^{L_k} \sqrt{2S_{k,l}} \xi_{k,l}^{(m)}(t) s_k(t - \tau_{k,l}) + n^{(m)}(t) \quad \text{-----}(4.3)$$

where $S_{k,l}$ is the average signal associated with l^{th} path and $n^{(m)}(t)$ is the background noise component. Quaternary phase shift keying is used for data modulation.

The spread signal received at each antenna is despread by the Matched Filter (MF) and resolved into L_k received signal sample sequences associated with L_k resolvable paths. Consider the a^{th} symbols, $a = 1, 2, \dots, N_p + N_d$, where N_p is the known pilot symbol and N_d is the information data symbol (discussed in Section 4.3.1.1). The symbols associated with $a = 1, 2, \dots, N_p$ represent unmodulated pilot $\Phi_k(a) = 0$ and those associated with $a = N_p + 1, \dots, N_p + N_d$ represent data symbols $\Phi_k(a) \in \{q\pi/2; q = 0, 1, 2, 3\}$.

The matched filter output sample $y_{k,l}^{(m)}(m)$ at time $t = aT + \tau_{k,l}$ associated with l^{th} resolved path is given by:

$$y_{k,l}^{(m)}(a) = \frac{1}{T} \int_{aT + \tau_{k,l}}^{(a+1)T + \tau_{k,l}} r^{(m)}(t) p_k^*(t - \tau_{k,l}) dt \quad \text{-----}(4.4)$$

where $*$ denotes the complex conjugate.

The despread signal samples $y_{k,l}^{(m)}(a)$'s of M antennas are weighted and combined to form a receive antenna beam pattern to maximize the SIR of the combined signal

associated with the l^{th} resolvable path. The resulting l^{th} signal sample $z_{k,l}(a)$ is represented as (l^{th} path beamformer output):

$$z_{k,l}(a) = \sum_{m=1}^M y_{k,l}^{(m)}(a) w_{k,l}^{(m)*}(a) \quad \text{-----}(4.5)$$

where $w_{k,l}^{(m)}(a)$ is the weight associated with the m^{th} antenna. In order to coherently combine the L_k beamformer outputs $z_{k,l}(a)$'s, the resultant composite channel gain (multiplied with rms amplitude) at time $t = aT + \tau_{k,l}$, which is given by:

$$\eta_{k,l}(a) = \sum_{m=1}^M \sqrt{2S_{k,l}} \xi_{k,l}^{(m)}(a) w_{k,l}^{(m)*}(a) \quad \text{-----}(4.6)$$

needs to be estimated using periodically received known pilot symbols. The channel estimation is performed using $2N_p$ pilot symbols of two succeeding slots. $\eta_{k,l}(a)$ is estimated using the simple average estimation method:

$$\hat{\eta}_{k,l} = \frac{1}{2N_p} \sum_{a=1}^{N_p} z_{k,l}(a) + \frac{1}{2N_p} \sum_{a=N_p+1}^{2N_p+N_d} z_{k,l}(a) \quad \text{-----}(4.7)$$

where the 1st and 2nd terms are the channel estimates using the pilot symbols associated with the present and next slots. Using the channel estimate $\hat{\eta}_{k,l}$, the random phase of the l^{th} beamformer output $z_{k,l}(a)$, $a = N_p, N_p+1, \dots, N_p+N_d$, is removed to be coherently combined by the RAKE combiner.

The RAKE combiner output is given by:

$$zk(a) = \sum_{l=1}^{L_k} z_{k,l}(a) \hat{\eta}_{k,l}^* \quad \text{-----}(4.8)$$

The antenna weight $w_{k,l}^{(m)}(a)$ of Eq (4.5) is updated based on an LMS algorithm (refer to Appendix A2). The weight adaptation algorithm is used to minimize the mean square error (MMSE- refer to Appendix A1) in the beamformer output $z_{k,l}(a)$. In order to generate an error signal $e_{k,l}(a)$ for the l^{th} beamformer a reference signal is required. The received pilot symbols can be used for this purpose. The pilot symbols and the

tentative recovered data symbols after RAKE combining are used in order to achieve fast convergence of the antenna array weights. The tentative data decision is performed after RAKE combining as:

$$\hat{\Phi}_k(a) = \max_{\tilde{\Phi} \in \{q\pi/2; q=0,1,2,3\}} \operatorname{Re} \left[\sum_{l=1}^{L_k} z_{k,l}(a) \hat{\eta}_{k,l}^*(a) \exp -j \tilde{\Phi} \right] \quad \text{-----(4.9)}$$

From Eq.(4.9), the reference signal $\hat{z}_{k,l}(a)$ is then generated as:

$$\hat{z}_{k,l}(a) = \sqrt{2\hat{Q}_k(a)} \left(\frac{\hat{\eta}_{k,l}(a)}{\sum_{l=1}^L |\hat{\eta}_{k,l}(a)|} \right) \exp j\hat{\Phi}_k(a) \quad \text{-----(4.10)}$$

where $\hat{Q}_k(a)$ is the estimate of the average signal power of the RAKE combiner output and is obtained by a 1st order filter represented as:

$$\hat{Q}_k(a) = \alpha_Q \hat{Q}_k(a-1) + (1-\alpha_Q) \frac{1}{2} |z_k(a)|^2 \quad \text{-----(4.11)}$$

where α_Q is the forgetting factor ($\alpha_Q = 0.999$) which corresponds to the equivalent measurement interval of 1000 symbols.

Note that $\hat{\Phi}_k(a) = 0$ when $a = 1, 2, \dots, N_p$ (pilot symbols). The reference signal represented in Eq (4.10) was heuristically found [66] based on computer simulations and convergence of the array weights.

The term $\sqrt{2\hat{Q}_k(a)} \exp j\hat{\Phi}_k(a)$ in Eq (4.10) is a reference signal whose rms amplitude varies slowly according to variations in the average power measured at the RAKE

combiner output. The term $\left(\frac{\hat{\eta}_{k,l}(a)}{\sum_{l=1}^L |\hat{\eta}_{k,l}(a)|} \right)$ provides the l^{th} path reference signal by

distributing the amplitudes among L_k resolved path in proportion to the measured instantaneous channel estimates $\hat{\eta}_{k,l}(a)$'s.

The error signal $e_{k,l}(a)$ is generated as:

$$e_{k,l}(a) = \hat{z}_{k,l}(a) - z_{k,l}(a) \quad \text{-----}(4.12)$$

Since the PSA channel estimation incurs one time slot delay $[(N_p + N_d)\text{symbols}]$, the error signal associated with the a^{th} time position of the present slot. The weight vector $w_{k,l}^{(m)}(a+1)$ can be updated using normalized LMS algorithm as:

$$w_{k,l}^{(m)}(a+1) = w_{k,l}^{(m)}(a) + \mu \frac{y_{k,l}^{(m)}(a - (N_p + N_d))}{\sum_{m=1}^M |y_{k,l}^{(m)}(a - (N_p + N_d))|^2} e_{k,l}^*(a - (N_p + N_d)) \quad \text{-----}(4.13)$$

where μ is the step size (LMS algorithm).

4.2.2: Simulation

The proposed receiver is realized using Agilent's Advanced Design System 1.3, [29] and the reader is referred to the ADS documentation for further information. Realization of the AAA receiver of Figure 4.1 using the ADS software is shown in Appendix A-3 Figure A.5. The AAA receiver consists of matched filter, beamformer, weight control, PSA channel estimation, RAKE combiner, tentative symbol decision and error signal forming sections each of which is discussed below.

4.2.2.1: Matched Filter: Figure 4.2 shows the functional block diagram of a matched filter. A matched filter realization using ADS is shown in Appendix A-3 (refer Figure A.3)

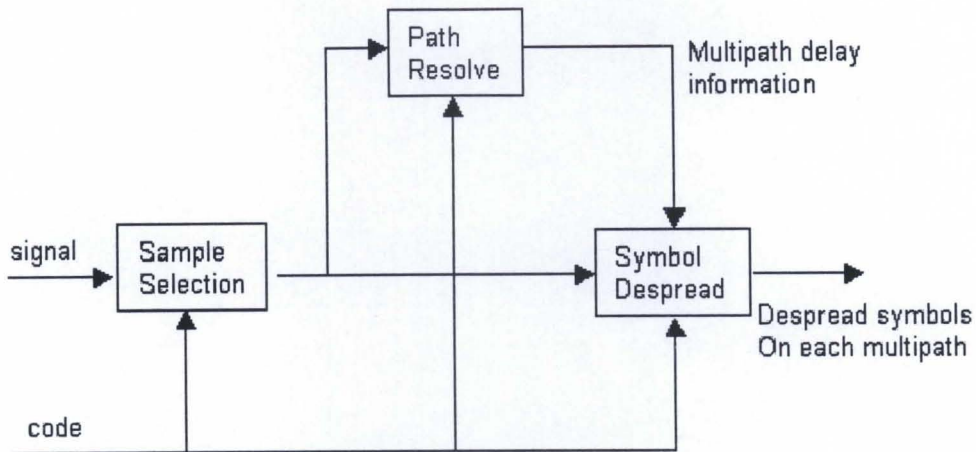


Figure 4.2: Functional block diagram of a matched filter

The matched filter consists of three functional blocks namely; sample selection, path resolution and despreading. Because of the existence of the shaping filter in the transmitter, which is a squared root raised-cosine filter, sampled values of the same chip are different. The optimum sample point (which has the maximum power and the least intersymbol interference) should be found at the same time in each chip [29]. In order to determine the optimum sample points of a chip one needs to select an optimum sample from “S” existing sample points of a chip. There are “S” samples per chip since the input signal is discrete and is sampled at the rate of $\frac{1}{T_s}$, where $\frac{1}{T_s} = R_c \times S$ [R_c =chip time, S= no. of samples].

The optimum sample point can be determined by comparing correlation values between a certain symbol’s spreading code and received signal starting at each sample point, which could be a sample point of the first chip of that symbol (since the magnitude of the correlation values indicates the magnitude of the sample value of symbol). After finding the optimum sample, the optimum sample sequence is selected and taken as the received signal sampled at the rate of R_c .

Correlation values between the received signal at each possible delay, in terms of chips, and pilot symbols are calculated. After path delays are known, symbols on each

path are despread. The despreading process is the same as the process of computing correlation value between the received signal and the spreading code sequence. These despread signals are weighted and combined and the resultant is combined at $t = aT$ where T is the symbol period of the a^{th} symbol. The weights of the signals are updated based on the LMS algorithm for minimizing mean square error.

4.2.2.2: PSA Channel estimation and beamforming: Linear interpolation is used for the channel estimation process. Pilot symbols at the head of the current and the next slots are used for channel estimation. One of the main problems associated with coherent demodulation in a non-frequency selective fading channel is carrier synchronization, both in terms of acquisition and tracking. This is particularly so when the channel is fast and when a line of sight component is absent [93]. PSA channel estimation is one of the more popular techniques to maintain coherent demodulation for digital modulation schemes. The main idea of PSA channel estimation is to multiplex known pilot symbols into an unknown data stream [91]. The receiver firstly obtains tentative channel estimates at the positions of the pilot symbols by means of re-modulation, and then computes final estimates by means of interpolation. WCDMA systems often use a pilot channel on the forward link for synchronization. With the use of these pilot symbols the timing of the forward traffic channel can be acquired as well as a phase reference for coherent demodulation by means of signal strength comparison between different base stations which in turn forms the basis for handoff.

Pilot measurement is a key component of a WCDMA mobile terminal. It is used to estimate the received pilot strength from neighboring base stations for handoff purposes. It is also used to detect the presence of multipath components and their time lags in signals being received from base stations with which the terminal has established handoff. Further more the pilot measurements can be used to assign demodulation finger delays of a RAKE receiver to independently fading multipath components. The timing of multipath components is acquired by measuring power at different phase offsets within a search window in order to detect the presence of multipath components. The timing acquisition performance for Rayleigh fading

channels under the assumption that the fading is fixed over a symbol, but varies independently from symbol to symbol is discussed in [94].

Channel estimation is implemented in the AAA receiver by using the slot averaging method. Let $r(n, m)$ be the m^{th} symbol of the n^{th} slot and $p(n, m)$ be the m^{th} local standard pilot symbol of the n^{th} slot.

$$\text{Let } \eta(n) = \frac{1}{N_p} \sum_{m=0}^{N_p-1} \frac{r(n, m)}{p(r, m)} \quad \text{-----}(4.14)$$

be the instantaneous channel estimate of the n^{th} slot, where N_p is the number of pilot symbols per slot. Then the channel estimate $\zeta(n)$ of the n^{th} slot is calculated using two consecutive channel estimates as:

$$\zeta(n) = \frac{1}{2}(\eta(n) + \eta(n+1)) \quad \text{-----}(4.15)$$

Using the linear interpolation method, the channel estimate for the m^{th} symbol of the n^{th} slot is:

$$\zeta(n, m) = \left(1 - \frac{m - \left(\frac{N_p - 1}{2} \right)}{N_s} \right) \eta(n) + \left(\frac{m - \left(\frac{N_p - 1}{2} \right)}{N_s} \right) \eta(n+1) \quad \text{-----}(4.16)$$

where $N_p \leq m \leq N_s - 1$ and N_s is the number of data symbols per slot.

4.2.2.3: RAKE combining and symbol decision: Using the channel estimate the random phase of the l^{th} path beamformer is removed and coherently combined by RAKE combining. A tentative symbol decision is made after RAKE combining. The reference signal is obtained by using the tentative symbol, the channel estimate and an amplitude distribution factor [29], [30]. The difference between this reference signal and the symbol before decision is the error signal. The error signal of the previous slot is used in the beamformer for weight updating of the current slot.

A performance evaluation is conducted in order to justify the implementation of an AAA receiver in the FPGA software radio platform. Implementation issues and the measured results are discussed in Chapter 6. The performance evaluation is carried out with a single element PSA RAKE receiver and a six element AAA receiver both evaluated in a range of environments. Fast TPC is not considered in the performance evaluation (See Section 4.5 for TPC evaluation). A simulation model is designed with ten users, nine of whom are the interference users. The simulation parameters in the channel meet the requirements of the UMTS/IMT2000 channel incorporating Rayleigh fading and Additive White Gaussian Noise (AWGN). The system model is designed according to WCDMA standards [2], [17] and is discussed in Section 4.3 below.

4.3 System model

Figure 4.3 shows the system model for the comparison of RAKE and AAA receivers in different environments. The model is divided into three blocks the transmitter, channel and the receivers used for comparison, each of which will be discussed in Sections 4.3.1, 4.3.2, 4.3.3 respectively. Figure 4.4 shows the realization of this system model using ADS.

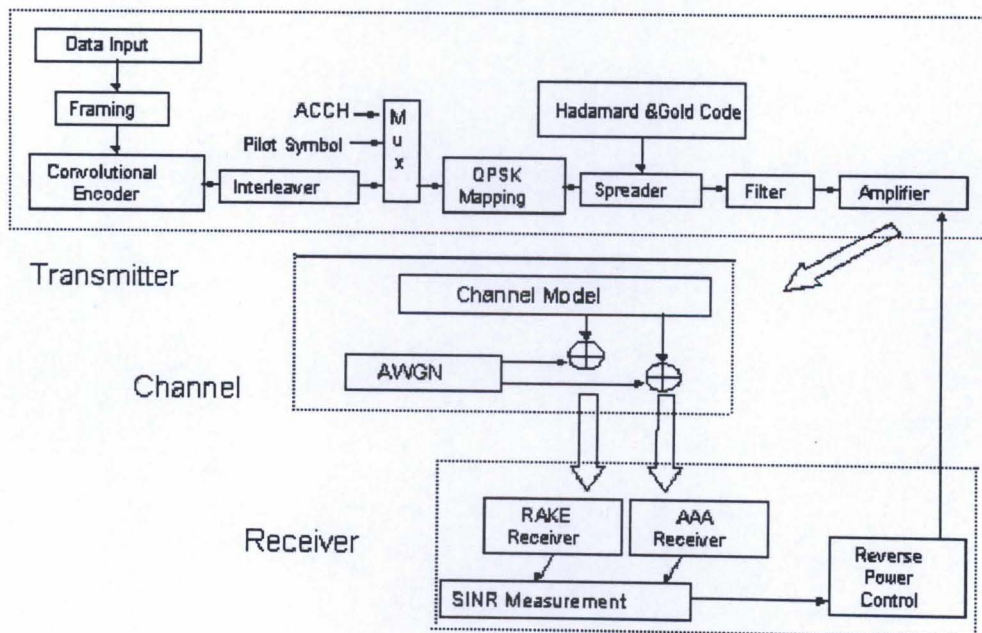


Figure 4.3: Simulated system model for AAA vs. RAKE comparison

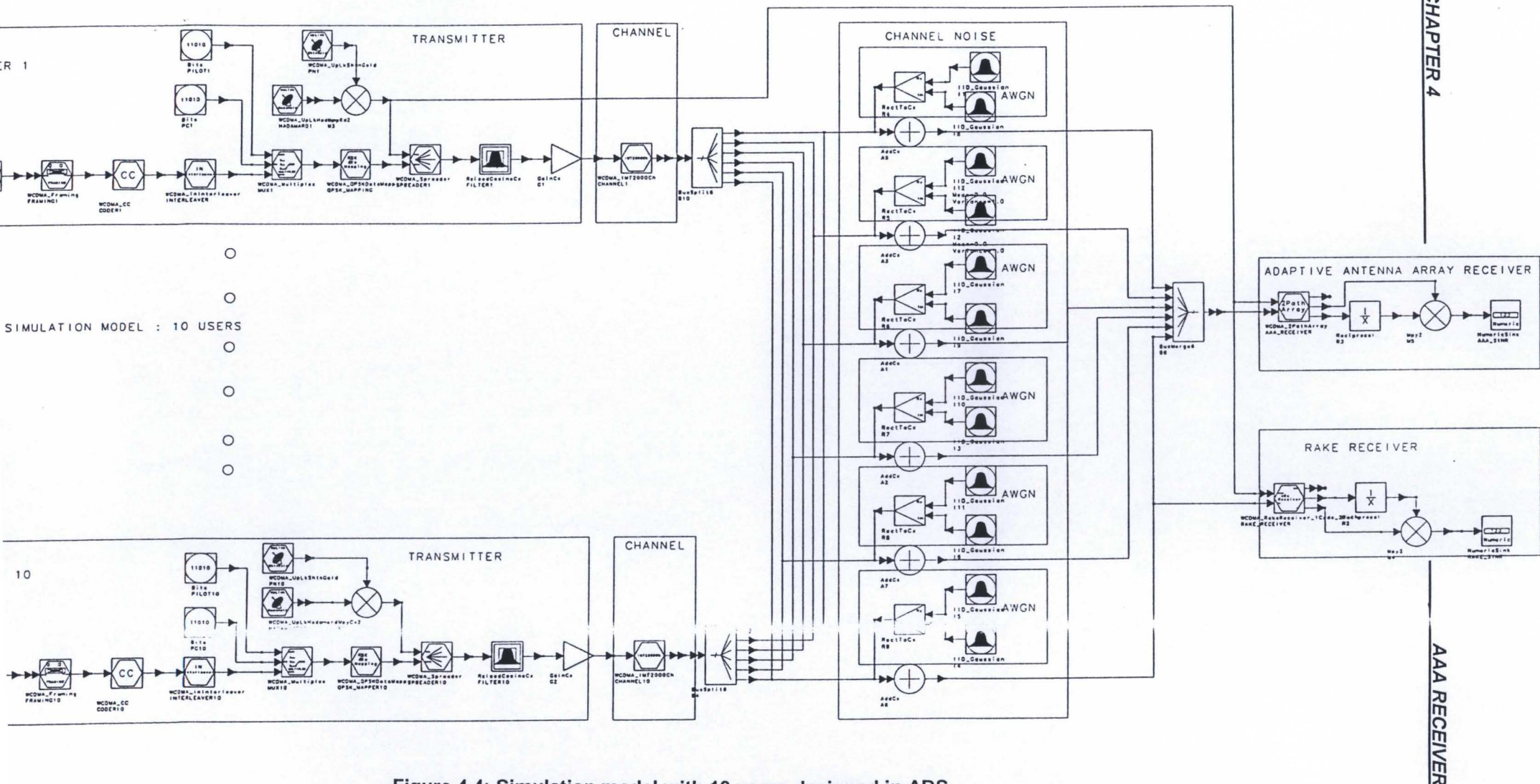


Figure 4.4: Simulation model with 10 users designed in ADS

4.3.1: The Transmitter:

The transmitter section consists of framing, convolutional encoding, interleaving, multiplexer, QPSK mapping, spreading and filter functional blocks. These functional blocks are discussed below. The transmitter model was designed using ADS as shown in Figure A.2 in Appendix A-3.

4.3.1.1: Framing: In WCDMA the data arrives on the transport channel in the form of transport blocks. A variable number of transport blocks arrive on each transport channel at each transmission time constant. The size of the transport blocks varies according to different transport channels and can also vary in time for the specific transport channel as shown in Table 4.1.

Service	Frame length	No: of transport blocks per frame	Transport block size
Speech	10 or 20 ms	Fixed (=1)	Variable
Packet data	10-80 ms	Variable	Fixed (=300bits)
Circuit-switched data	10-80 ms	Fixed (≥ 1)	Fixed

Table 4.1: Transport channel formats for different class of service [2].

The length of the radio frame is different for different transport channels but is limited to the set [10,20,40,80 ms] [2]. The frame length typically corresponds to the interleaver span (length) applied by the physical layer and depends on the service requirements and desired radio performance. In order to obtain good performance in a fading channel, the frame length has to be long enough to support a reasonable interleaving depth. The longer the interleaving, the better an error burst is spread over the interleaving period.

Consequently, individual errors can be better handled with error correction coding than errors appearing at the decoder in bursts. In practice the interleaving depth cannot be so

long as to exceed the transmission delay service requirement. A simplified structure of the transmission frame is depicted in Figure 4.5. The length of the radio frame is 10 ms and consists of 16 equally divided slots of length 0.625 ms, corresponding to one power control period

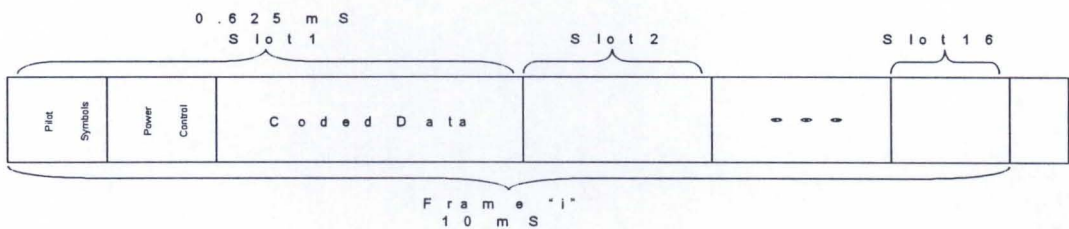


Figure 4.5: Frame and slot structure

Each slot contains power control bits, known pilot bits for channel estimation and Associated Control CHannel (ACCH) or Transport Frame Indicator (TFI) signals. The ACCH or TFI informs the receiver about the instantaneous parameters such as block size and number of blocks of each transport channel multiplexed on the physical channel. The number of data bits are not fixed and may vary corresponding to a physical channel bit rate.

The inevitable presence of noise in a channel causes errors between the output and input data sequences of the mobile communications system. The principle goal of channel coding is to increase the resistance of a digital communication system to channel noise. CDMA is subject to self-interference (MAI) from users in the same cell. Without coding, the system’s tolerance to this interference is poor, thus severely limiting it’s capacity. Hence, quite powerful coding is used to increase tolerance to interference, and thereby allowing more users.

4.3.1.2: Convolutional coding: CDMA uses convolutional coding to improve the error performance [95]. For convolutional codes, the encoded bits are functions of information bits and constraint length. Specifically, every encoded bit is a linear combination of some previous information bits. The error correcting codes are designed to combat errors resulting from fades and keep the signal power at a reasonable level.

Most error correcting codes perform well in correcting random errors but they fail in the case of long streams of successive or burst errors.

4.3.1.3 Interleaving: DSCDMA supports simultaneous services for digital communication among a considerably higher community of users than any single user. This will be reflected in how this excess of dimensionality or redundancy is exploited to improve the performance. Two processing techniques are considered to achieve improvements: interleaving for the excess redundancy and forward error-correcting coding. Interleaving is a technique used for randomizing the bits in a message stream so that burst errors introduced by channel can be converted to random errors or in other words it is the process of permuting a sequence of symbols. The performance improvement due to interleaving depends on the diversity order of the channel and average fade duration of the channel. The interleaving depth is determined by the delay requirements of the service.

Table 4.2 shows the link parameters used in the simulations. In the simulation the data to be transmitted is CRC coded, framed and convolutionally encoded at rate of $1/3$ with constraint length of 9. The coded data is block interleaved and time multiplexed with Pilot, Transmit Power Control (TPC) and Associated Control CHannel (ACCH) signals.

Processing Gain		32x0.5x3	
Modulation	Data	QPSK	
	Spreading	QPSK	
Channel Coding		Convolutional Coding, R=1/3, K=9	
Frame Structure	Slot	Pilot	4 symbols
		Data	76 symbols
	Frame	0.625 ms X 16 Slots	
Chip Rate		4.096 Mcps	
Interleaving		10ms	
Spreading Code		Gold Code	
Channel Estimation		Linear Interpolation	
Demodulation		Pilot symbol assisted coherent detection	
Channel decoding		Soft-decision Viterbi decoding	

Table 4.2: Link parameters used for simulation (repeated from section 2.4)

4.3.1.4: Spreading: The *multiplexed* data is transformed into Quaternary Phase Shift Keying (QPSK) symbols. The QPSK symbols are orthogonally spread by the assigned Hadamard code. Each channel is identified by its assigned Hadamard function. The *spreading* Hadamard function is at a rate of 4.096 Mcps. During simulation a tree-structured Hadamard sequence family is used with the length of each Hadamard short code being variable to meet multi-rate transmission requirements. Since the cycle of the short code is one symbol length, the cycle of a short code of the same chip rate differs from the symbol rate. The data stream is further spread by the assigned PN sequence of the transmitting sector. The PN sequence provides a second layer of isolation that distinguishes among the transmitting sectors. In this way, all Hadamard functions can be reused in every sector. In the simulation the sequence generator generates shortened Gold code sequences, which are used as long spreading codes in the uplink. The uplink long code has a cycle of 2^{16} frames [29], [30]. The spread signal is raised cosine filtered, this filtered signal is amplified and transmitted at 2 GHz.

4.3.2: The channel

A radio channel is a generally hostile medium in nature. It is very difficult to predict its behavior. Radio channels are usually designed in a statistical way using real propagation measurement data. In a radio environment, generally speaking the signal fading can be decomposed into a large-scale path loss component together with a medium scale slow varying component having a log-normal fading distribution, and a small scale fast varying component with a Rician or Rayleigh distribution, depending on the presence or absence of a Line-of-Sight (LOS) between the transmitter and receiver [9]. Large-scale propagation models are designed to determine the path loss (due to diffraction, reflection etc) because they characterize the received signal strength by averaging the power over large propagation distances. Medium scale propagation models determine the medium scale variation of the received signal power due to shadowing. Small scale propagation models characterize the fast variation of the signal strength due to the multipath reflection of a transmitted wave by local scatterers such as houses, buildings, mountains, man-made structures and natural objects like forests, surrounding a mobile unit.

Third generation mobile systems are expected to operate in a variety of environments such as large and small cities (with variations in building construction), tropical, rural, desert and mountainous areas. To evaluate the performance of the base station it is necessary to consider all environments. In this thesis a number of generic environments are considered namely vehicular, indoor, outdoor to indoor and pedestrian.

4.3.2.1: Vehicular environment:

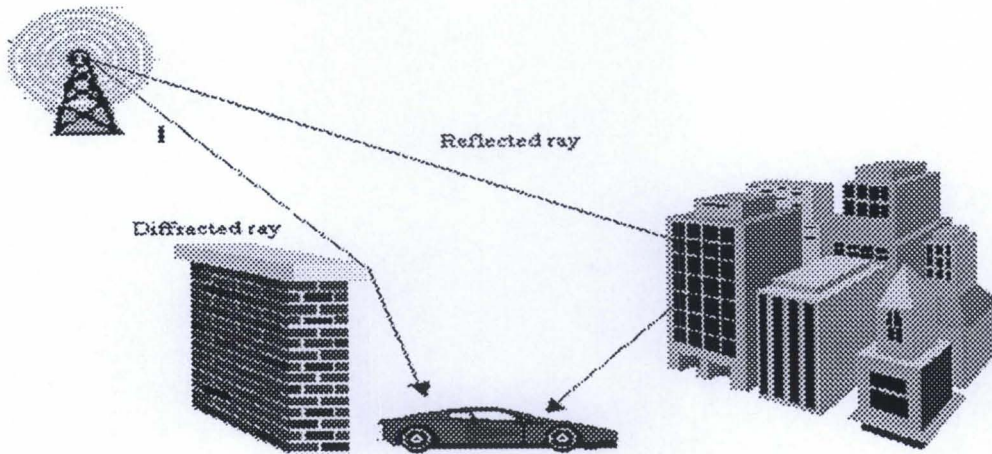


Figure 4.6: Vehicular environment

Figure 4.6 illustrates the vehicular environment, which is characterized by large macrocells and high transmit powers. Mobile velocity has been assumed to be 100 Km/hr with maximum Doppler frequency of 185 Hz. In such fast fading cases the received signal power varies by at least 10 dB in suburban and urban areas [79]. In the simulation a maximum multipath time delay of 20 chips ($4.9\mu\text{s}$) was assumed. Typically the delay spreads in the vehicular environment are on the order of $0.8\mu\text{s}$ and maximum can be up to $10\mu\text{s}$ [9]. The effect of mobile velocity in fading channels is discussed in [77].

4.3.2.2 Indoor environment: The indoor environment differs from the normal mobile radio environment in two aspects; the interference environment and the fading rate. The interference environment is often caused by spurious emissions from electronic equipment such as computers and the level can sometimes be much greater than that measured outdoors [78]. Moreover there are great fluctuations in the received signal strength from place to place within a building. For example the signal can be highly attenuated after propagating a few meters through walls, ceilings and floors or may still be very strong after propagating several hundred meters along a corridor. In this type of environment the signal to interference ratio is highly variable and unpredictable. For an indoor environment radio communication covers a wide variety of situations such as

communication with individuals walking in office buildings, in lifts, etc. Here, shadowing is considered to be log normal with a typical standard deviation of 12dB [30] and penetration loss was normalized to between 13 and 20 dB [9]. Mobile station speeds are slow ranging from stationary up to 5 km/hr. In this case the Doppler frequency is negligible, but the fading varies from Rician to Rayleigh. Quantification of propagation between floors is important for indoor mobile system of multifloor buildings that needs to share frequencies within the buildings. Frequencies can be reused on different floors to avoid cochannel interference. The greatest floor attenuation occurs in the case when the receiver and transmitter are separated by a single floor. For five or more floors of separation, the path loss will increase only a few dB for each additional floor [10]. Typical average rms delay spreads for indoor office environment are on the order of 50ns and maximum can be up to 250ns [9].

4.3.2.3: Outdoor to Indoor and Pedestrian environment: A great deal of attention has been given to propagation in built-up areas, in particular to the situation where the mobile is located in the streets. Considering a scenario where the mobile can be taken into the buildings and moves towards a local communication network like cordless PABX systems etc, there is likely to be a substantial increase in the use of cordless phones. This leads to a legitimate interest in characterizing the radio communication channel between the base station and a mobile located inside the building. The outdoor to indoor pedestrian environment is characterized by small macrocells and low transmit powers. The shadowing varies from 10 to 12 dB with a typical building penetration loss average of 12dB, and maximum mobile speed of 8 km/hr. In circumstances when there is No-Line-of-Sight (NLOS) path, the large-scale signal variations will exactly fit a log-normal distribution and the standard deviation is about 4dB in the case of the building penetration loss [80]. A mobile station can experience a sudden drop of 15 to 25 dB when it moves around a corner and typical delay spread for a small-scale fading is on the order 0.2μs [9].

Figure 4.7 depicts the outdoor to indoor and pedestrian environment. In this environment both the LOS and NLOS conditions exists.

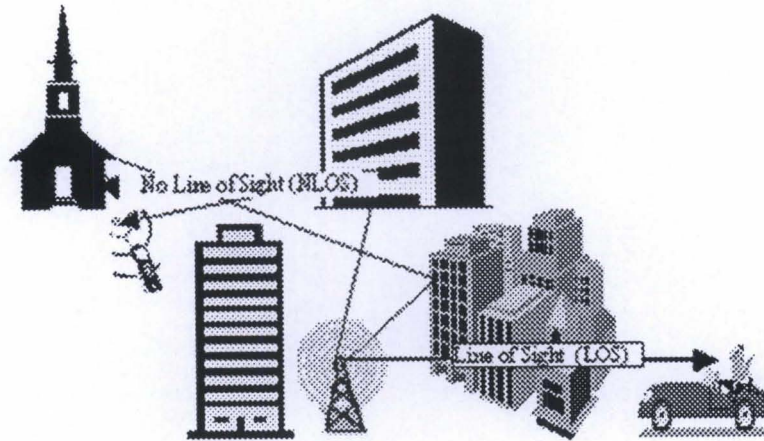


Figure 4.7: Outdoor to indoor environment

4.3.3 PSA RAKE Receiver

The functional block diagram of a RAKE receiver is shown in Figure 4.8. The RAKE receiver consists of a matched filter, channel estimator and RAKE combiner. The matched filter, channel estimator and RAKE combiner have been discussed in Section 4.2.2.1, 4.2.2.2, and 4.2.2.3 respectively. The matched filter despreads the received signal and detects the delays of L paths. The channel estimation uses pilot symbols to estimate channel characteristics. After channel estimation, symbols of the current slot and the first half of next slot are available and the RAKE combiner combines the l^{th} path's despread signal coherently to generate a soft output. Figure A.6 in the Appendix A-3 shows the RAKE receiver designed using ADS.

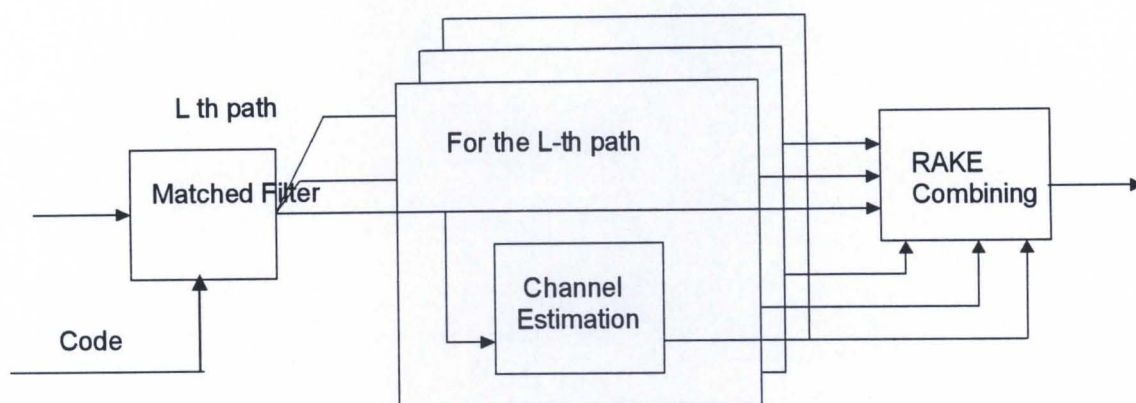


Figure 4.8: Functional block diagram of RAKE receiver

4.4 Performance Evaluation

The performance of an AAA receiver and a conventional RAKE receiver was evaluated. The AAA has six elements, each element separated by 0.5λ while the RAKE receiver is fed from a single antenna. For simplicity only one cell sector has been considered. The SINR calculated in both cases is the ratio of signal power to the interference plus the noise power. The systems described thus far have been designed and simulated using Agilent Technologies Advanced Design System (ADS) software [29] [refer Figure 4.4]. The simulation considered a Rayleigh fading environment with Additive White Gaussian Noise (AWGN), having mean of zero and variance of 0.8, being added into the channel. The AWGN channel realization is shown in Figure A.4 in the Appendix A-3. Ten users, nine of whom are interference users, with the same transmit power of 0.8W were considered. Power control is not applied in this simulation. The performance is evaluated by means of SINR of the two receivers in the various environments. In each case 100 frames were simulated. The results for the various environments are presented below.

4.4.1 Vehicular environment

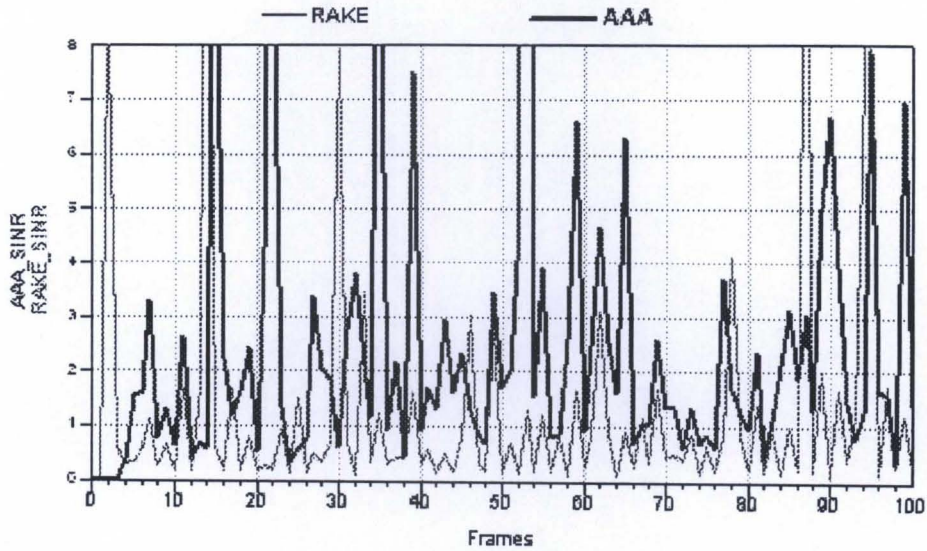


Figure 4.9: SINR in vehicular environment (100 km/hr)

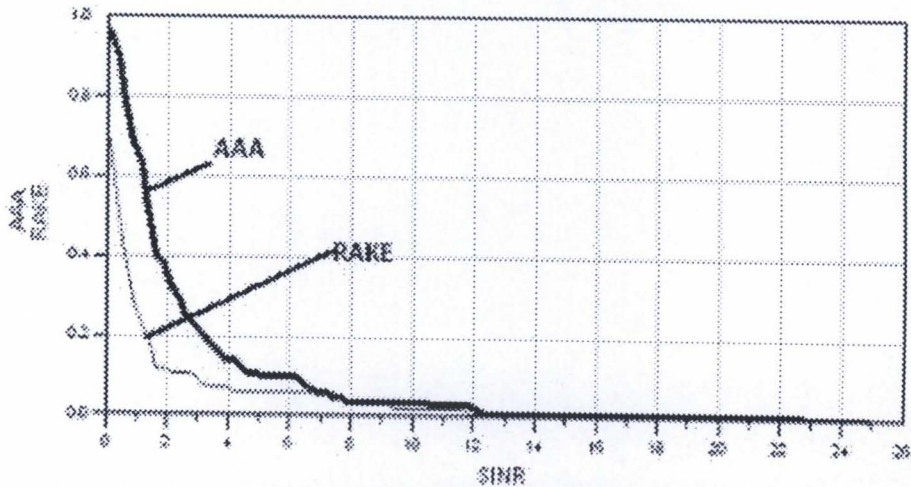


Figure 4.10: CCDF of vehicular environment (100 km/hr)

Figure 4.9 shows the SINR of the two receivers, in a vehicular environment with all mobiles traveling at 100 km/hr. Using this data it is possible to extract a complementary cumulative density function (CCDF) for the SINR over 100 frames, this is presented in Figure 4.10. In vehicular environment the probability of a frame lying above 12 dB SINR is negligible; say less than 3 %. For AAA receiver 60 % of frames lie between 0-2dB SINR while for RAKE receiver it is 90 %. In the case of

SINR between 2-12 dB, 40 % of frames for AAA receiver but only 10 % for RAKE receiver.

b) Outdoor to indoor and pedestrian environment

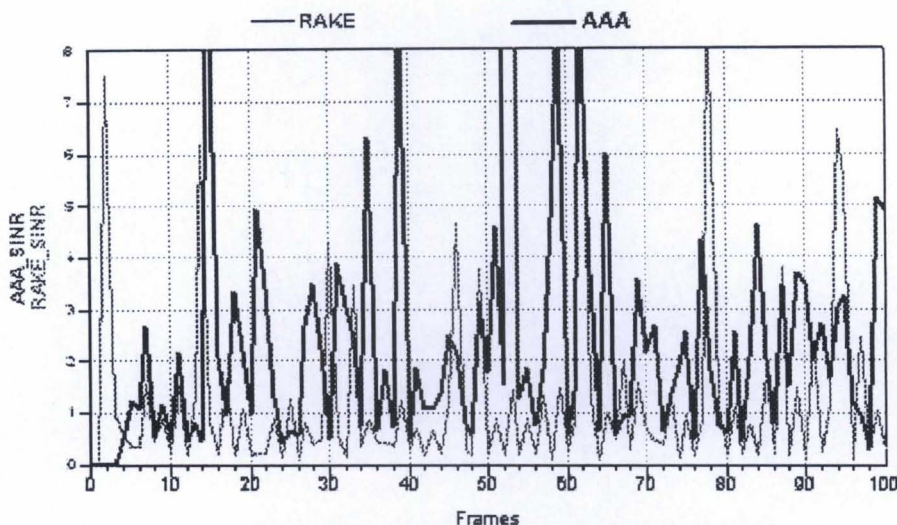


Figure 4.11: SINR in pedestrian environment (8km/hr)

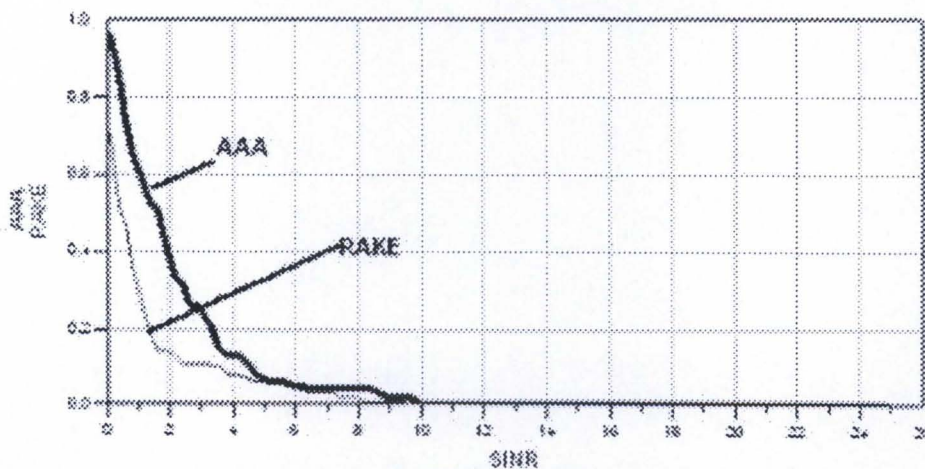


Figure 4.12: CCDF of pedestrian environment (8km/hr)

In the pedestrian environment all the users are moving at 8km/hr. Some of the mobiles were considered to migrate from the outdoor to the indoor environment. Figures 4.11 and 4.12 present the SINR and CCDF of both receivers in pedestrian and outdoor to indoor environments. In the outdoor to indoor environment the probability of a frame

lying above 10 dB SINR is negligible; less than 3 %. In this case, for AAA receiver only 65 % of frames lie between 0-2 dB while for RAKE receiver it is 85 %. The 35 % of frames lies between 2-10 dB for AAA receiver and only 15 % of frames for RAKE receiver.

c) Indoor environment

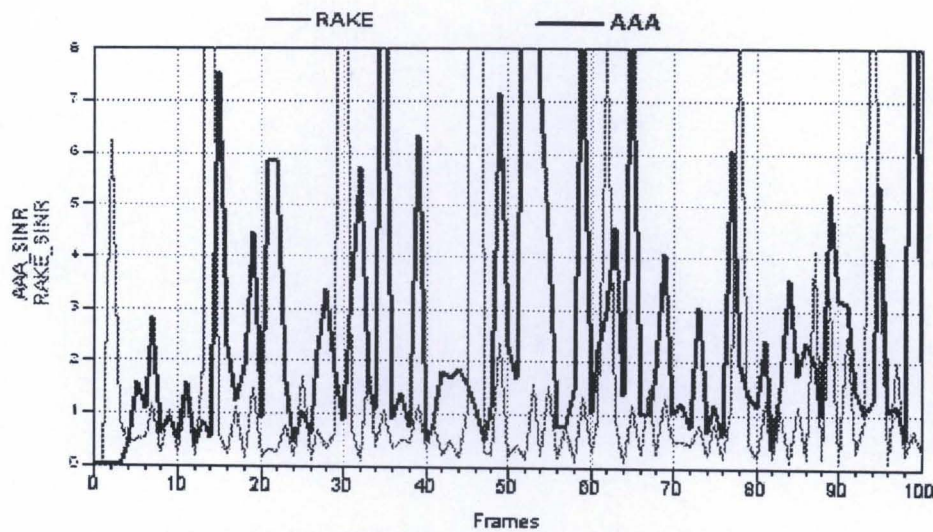


Figure 4.13: SINR in indoor environment (5km/hr)

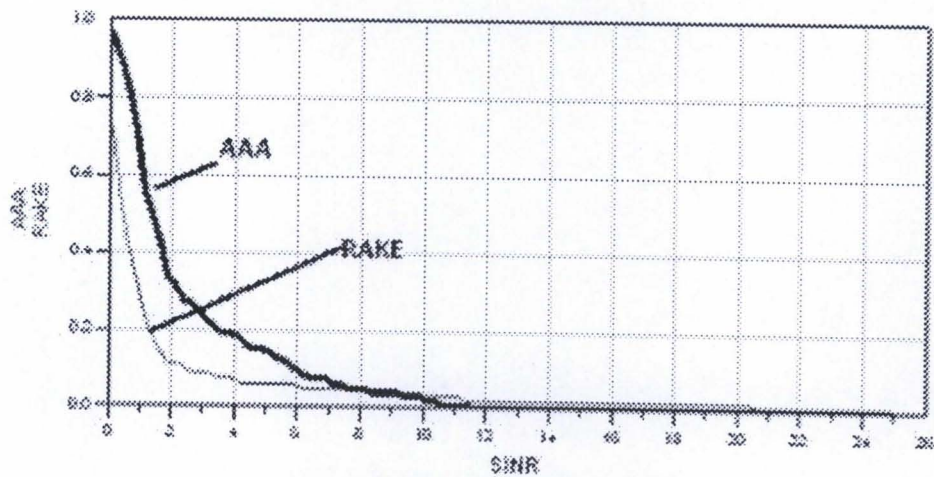


Figure 4.14: CCDF of indoor environment

In the indoor environment a very low velocity of 5 Km/hr is assumed. The Doppler shift is thus negligible. These results are presented in Figures 4.13 and 4.14.

d) Mixed environment

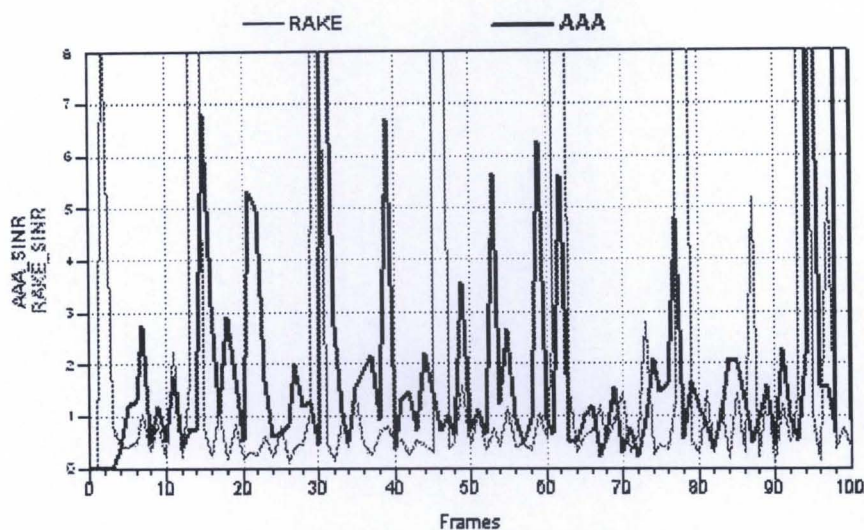


Figure 4.15: SINR in mixed environment

A practical channel consists of mobile users in different environments. Thus a mixed environment was considered. Four vehicular users and six pedestrian and indoor environment users were simulated. Figures 4.15 and 4.16 show the results from this mixed mobile environment

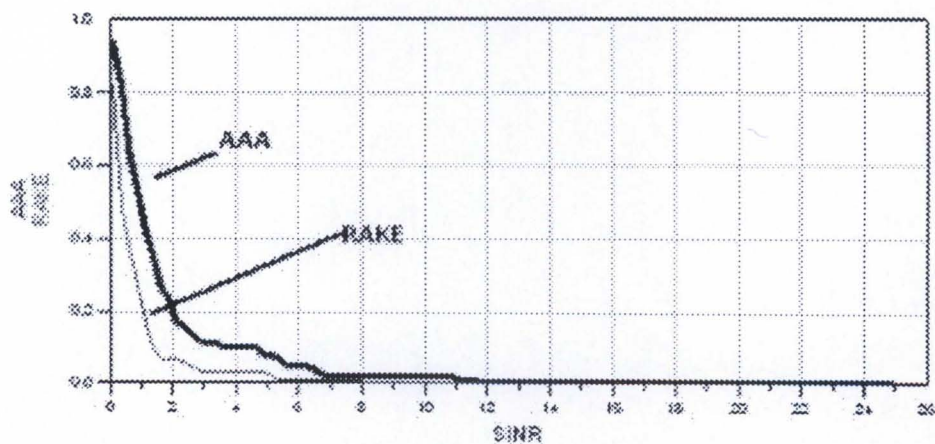


Figure 4.16: CCDF of mixed environment

In this case the probability of a frame lying above 7 dB SINR is negligible for the RAKE receiver and 11 dB for AAA receiver. For the AAA receiver 70 % of frames lie between 0-2dB SINR while for RAKE receiver it is 90 %. The 10 % of the frames lies between 2- 7 dB for the RAKE receiver and almost 20 % of frames in between 2-11 dB for the AAA receiver.

4.4.1: Discussion of simulation results

SINR [dB]	Vehicular	Outdoor to Indoor	Indoor	Mixed
0	1.4	1.4	1.4	1.25
2	3.3	3.0	3.5	2.8
4	2.6	2.5	2.7	3.6
6	2.3	1.2	3.3	4

Table 4.3: CCDF ratio AAA/Rake at various SINRs

Table 4.3. summarizes the expected improvement in system performance (AAA vs. RAKE) at various simulated SINRs for the environments considered above. At 6dB SINR the AAA receiver in a mixed environment performs 4 times better than the RAKE receiver. On average, this performance improvement is 2.9. The SINR measured at the AAA receiver is high compared to RAKE receiver in all environments. This could be due to the antenna diversity and beamforming techniques used in the AAA receiver, because the matched filter, PSA demodulation, channel estimation and RAKE combining (diversity) functions are also used in the PSA RAKE receiver. The antenna diversity (in the receiver) can be used to average out the receiver noise in addition to providing diversity against fading and interference [9]. In the RAKE receiver the multipath not captured by RAKE processing contribute to the overall interference.

The above simulation results indicate that an AAA receiver performs better than a “stand-alone” RAKE receiver in all the simulated environments. From these results it can be inferred that when the link is interference limited, the link capacity can be increased. By using average SINR it has been shown that the AAA receiver with six antenna elements increases the link capacity to about 2.9 times that of the single antenna RAKE receiver. This work, which confirms the results presented in [66], has

been completed as a justification for implementation of an AAA receiver on an Alcatel software radio platform which will be discussed in Chapter 6.

4.5 Power Control

Power control is essential to the smooth operation of a CDMA system. The major objective of power control is to alleviate the cochannel and cross-channel interferences in mobile communication systems [85]. Figure 4.17 illustrates the need for power control in CDMA systems: The mobile M2 is closer to the base station B than mobile M1. If there is no power control, both mobile units would transmit a fixed amount of power, but because of the difference in the distance, the received power from the M2 would be much greater than the received power from M1. This means that M2 has a greater advantage than M1. The mobile units M1, M2, M3, M4 would have different SNR. This inequity is known as the near-far problem in spread spectrum multiple access system [9], [95].

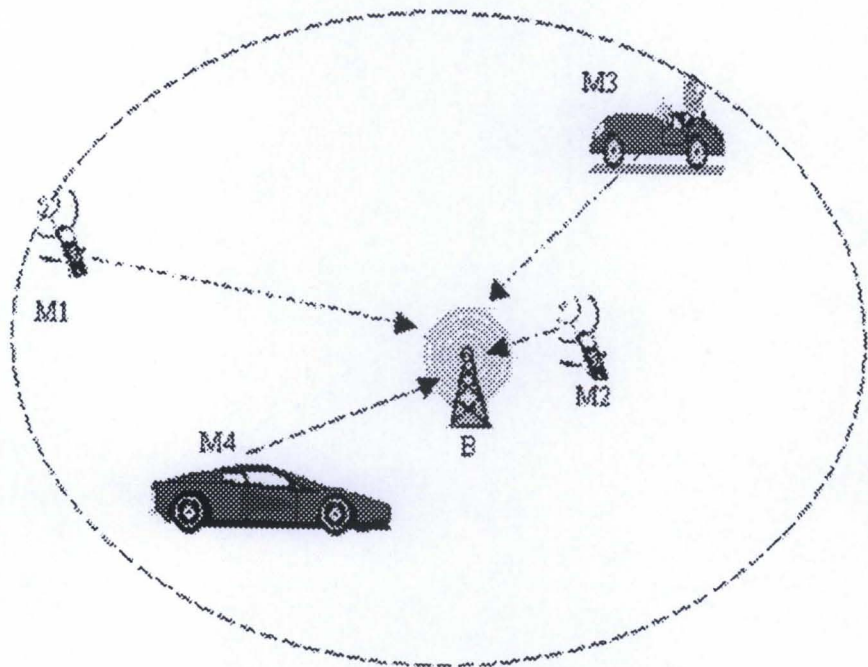


Figure 4.17: Base station with four users

The mobile stations, which are near to the base station, receive a stronger signal from their own base station and less interference from other base stations and mobile stations. By adjusting the transmitted power to satisfy the required SIR the overall capacity can be increased [86]. To achieve acceptable channel capacity, all mobile signals must arrive at the base station with the same mean power, irrespective of distance. Power control, which attempts to achieve a constant received mean power for each user, minimizes the interference to the other cells and compensates against interference from other cells. Recent investigations ([83], [84], [86]) discussed the performance of different power control algorithms used in CDMA systems.

In DS-CDMA cellular systems reverse link power control is essential to reduce the amount of interference caused by other cochannel signals transmitted from the mobile stations in the same cell or from the neighboring cells. In [84], different power control algorithms and the advantages/disadvantages thereof, are discussed. The performance of a fixed step power control algorithm and the issue of quantization are addressed and its capability is demonstrated in [86]. The interference reduction capability of antenna arrays and power control techniques is incorporated in [87] to increase the capacity of wireless communication networks. In power control, the transmitter powers are constantly adjusted, which improves weak links and receivers employing antenna arrays adjust their beam pattern such that they have fixed gain toward the direction of their transmitters, while the aggregate interference power is minimized at their output. In [87], an algorithm is derived to compute transmission powers and the beamforming vectors to achieve the target SINR for each link with minimum transmission power. A similar algorithm, discussed in [73], finds a set of feasible transmit beamforming vectors and downlink transmit power allocations such that the SINR at each link is greater than a target value and demonstrates that the proposed algorithm minimizes the total transmitted power in the network. The level of the cochannel interference at each receiver depends both on the gain between interfacing transmitters and receivers, as well as on the level of the transmitter powers, i.e., the optimal beamforming vector may vary for different powers. Hence beamforming and power control should be considered jointly.

4.5.1 Open-loop power control

Open-loop power control is implemented on the mobile station and not on the base station. The path loss between the mobile and the base station will vary when the mobile starts moving around the cell after establishing the call. Open-loop power control will monitor the received mobile power and adjust the mobile power. This method of power control is used to compensate for slow-varying and log-normal shadowing where there is a correlation between the forward link and reverse link fades. But it is inadequate and too slow to compensate for fast Rayleigh fading [95]. Closed-loop power control is used to overcome this problem. The closed-loop power control process operates along with open-loop power control and the process involves both the mobile and the base station.

4.5.2 Closed-loop power control

Closed-loop power control in the base station continuously monitors and measures reverse link quality. If the link quality is weakening, the base station will send a command to the mobile to power up or vice versa. The base station sends power control commands to the mobile using the forward link. These power control commands are in the form of power control bits. As mentioned in the Section 4.3.1.1 the power control bits are multiplexed onto the traffic channel after convolutional encoding. So the power control bits are not error protected [10], [95]. There are mainly two reasons forth; firstly to reduce the delays that are inherent in decoding and extracting error protected bits. Secondly, closed-loop power control is used to combat fast Rayleigh fading, quick recovery of power control bits is needed to adjust the transmit power. The error probability of the power control commands is very high. However, since the power control commands are transmitted very often and the step size is small, the power control loop converges to the desired value despite the high probability of errors. The error probability of power control command is discussed in [84].

This thesis considers a closed loop power control structure based on the system used in [96]. The Signal to Interference Ratio (SIR) is the ratio of bit energy (E_b) to Interference (I). The purpose of closed loop power control is to maintain SIR or E_b / I at a constant level in an environment where the propagation loss varies significantly. Closed loop power control is based on the received signal strength, where power is adjusted every 1.25ms in IS-95 CDMA while in WCDMA the power is adjusted every 0.625ms based on commands from the base station. Closed-loop power control has an inner and outer loop. The inner and outer loops are shown in Figure 4.18. The premise of the inner loop is that there exists a predetermined SIR threshold by which the power-up and power-down decisions are made. In order to maintain the required Frame Error Rate (FER), the E_b / I threshold is dynamically adjusted and is referred to as the outer loop of the closed-loop power control [95].

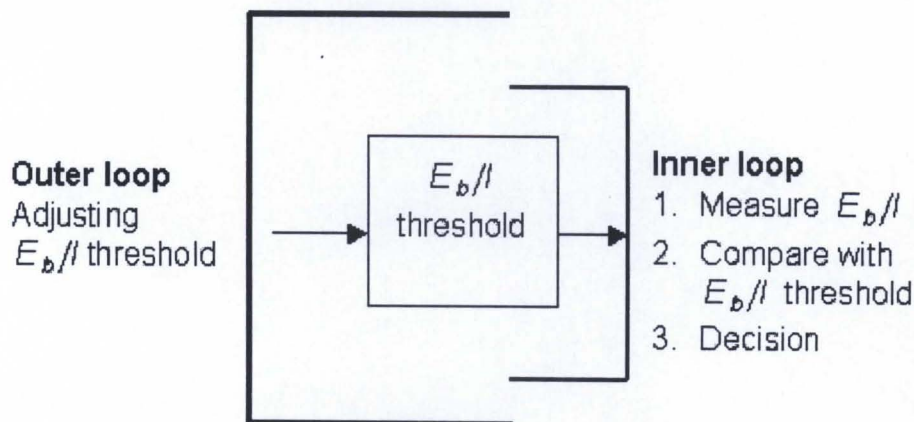


Figure 4.18: Inner and outer loops of the closed loop power control [95]

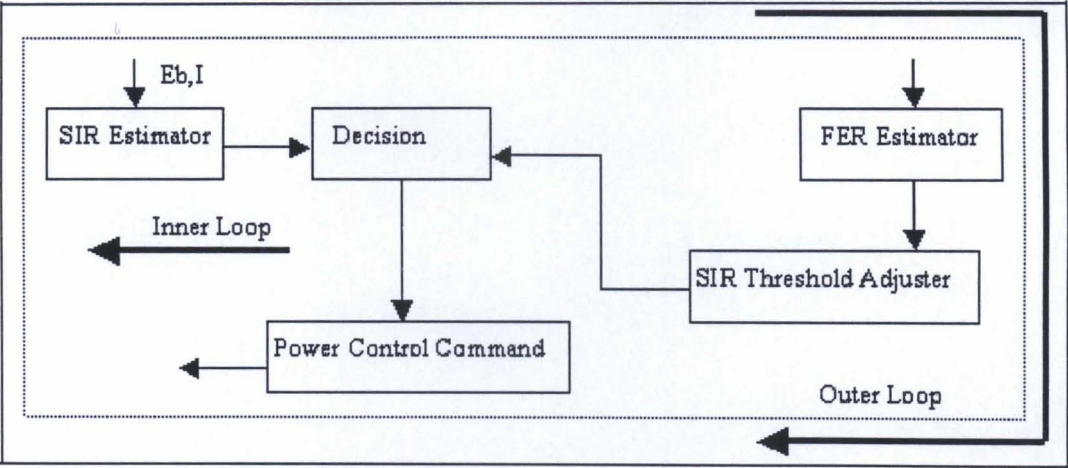


Figure 4.19: Block diagram of power control structure

Figure 4.19 shows a block diagram of the power control structure used in the system model. The SIR Estimator calculates the received SIR. The FER estimator is used to predict the FER. CRC is employed to determine whether a frame is valid or not. The FER is the ratio of number of good frames to the total number of frames. The SIR threshold adjuster will calculate the actual SIR and adjust the SIR threshold according to the current environmental requirements.

If the FER is greater than the FER_Min (minimum required FER), the SIR threshold will be increased otherwise it will be decreased. The new SIR threshold cannot be less than SIR_min. The decision was made by comparing the current SIR and required SIR. If the current SIR is greater than the required SIR (SIR_Min) the power Control Command sets the power control bit to be “0”, otherwise it is set to “1”. The power control command will be repeated, so the power control bit will be two repeated bit values because the power control bits are not error protected. The SIR threshold refers to the minimum SIR requirement at the receiver to maintain a specified Bit Error Rate in certain environment and quality of service. The SIR threshold is inversely proportional to the capacity of the system

During the simulation users with and without power control were considered. The simulation system model discussed in Section 4.3 is used. For simplicity only a RAKE receiver is considered. All the users are assumed to be moving with a velocity of 100

km/hr and transmitting simultaneously with initial power of 0.7 W. The channel is a typical urban area environment with Rayleigh fading and AWGN with mean of 0 and variance of 0.8. Figure 4.20 shows the fluctuations in the SIR of a user without power control in the simulated urban area. In this case, when the SIR is high, the user will have a very high quality of service but causes interference to other users.

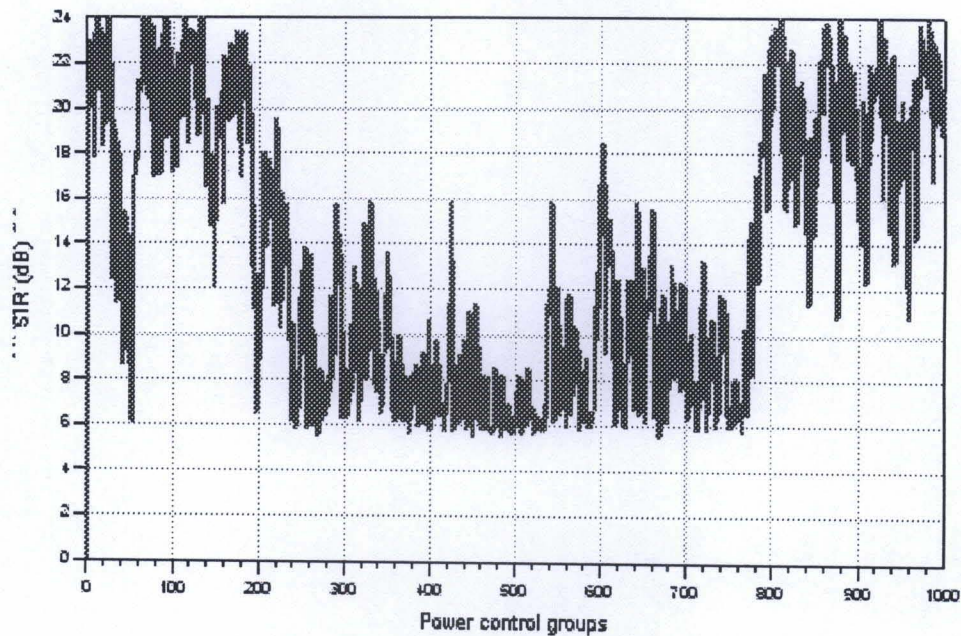


Figure 4.20: SIR without power control

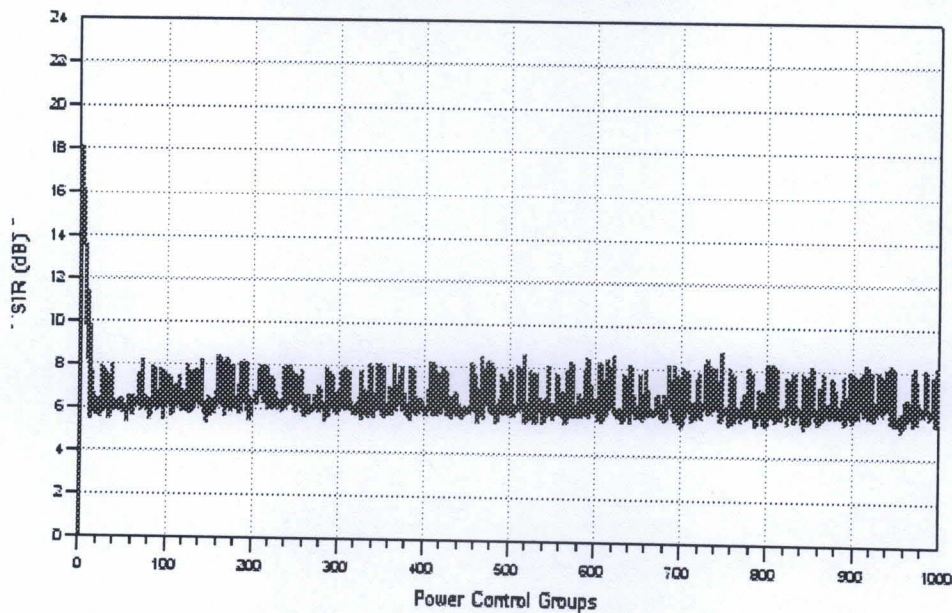


Figure 4.21: SIR with power control

Figure 4.21 shows the SIR in dB versus the power control groups of a user with power control. One radio frame is divided into 16 power control groups. The SIR of this user maintains a constant SIR that is the required SIR based on the specified quality of service. In a vehicular environment the Doppler frequency is quite high (185Hz), so there is a slight deviation of SIR from the target threshold even after power control. In the receiver a delay of one frame is introduced, caused by multipaths and filters. So the power control will track the required SIR after one frame. The E_b/I gain depends on the channel characteristics, the bandwidth of the system, and the mobile speed. Since a wide bandwidth gives better diversity, power control is not as critical for WCDMA as for narrowband CDMA systems [5]. The improvement in performance using fast power control is largest in a small delay spread channel. Fast power control is beneficial, especially in micro and picocell channels, due to limited multipath diversity. In a macro cell channel, the gain of fast power control in E_b/I is not very large because of the high degree of multipath diversity. Fast power control is used in WCDMA.

4.6 Conclusion

An adaptive antenna array structure and power control techniques are considered to be useful methods for reducing cochannel interference and thus increasing CDMA system capacity. In this chapter a comparative performance evaluation between an Adaptive Antenna Array (AAA) receiver using PSA CAAD techniques and a conventional RAKE receiver was presented. In the receiver model, AAA and path diversity (RAKE combiner) are combined and applied to PSA reverse link. The simulation channel was modeled using an UMTS/IMT 2000 channel incorporating Rayleigh fading and Additive White Gaussian Noise (AWGN). Because a critical component of CDMA systems is the ability to control the power of the mobile station instantaneously a power control structure and the benefits thereof were also discussed. The mobile station extracts the power control command bits and adjusts its transmission power accordingly. The SIR required to produce a certain BER varies according to the radio

environment and depends on the amount and type of multipath. The power control structure discussed in Section 4.4 employs an outer loop that adjusts the target SIR. The base station measures the signal quality (BER) or the SIR. However, this outer loop will increase the power control error resulting in a total standard deviation of 1.5 to 2.5 dB in SIR.

Table 4.3 summarized the improvement in the system performance in various environments. In the mixed environment, which is a practical environment, the receiver performs approximately 4 times better than that of the RAKE receiver, while considering all other environments, in different SINRs, an average performance increase of 2.9 times over a RAKE receiver is achieved.

This work was carried out as a precursor to implementation of a base station receiver utilizing adaptive array techniques in a software radio. A software radio incorporating adaptive array beamforming at the receiver can increase the total carried traffic in a system while at the same time reducing transmitted power and probability of call blocking and forced termination. An Alcatel Altech Telecoms (AAT) software radio is used to implement the system model expounded in this chapter. The flexibility of the software radio and the hardware structure of the software are addressed in Chapter 5.

Chapter 5

Software Radio

5.1 Introduction

A software radio may be defined as a radio whose function is software reconfigurable. Software radios are evolving to become one of the world's leading technologies [22] in mobile communications due to their flexibility in terms of re-programming without any changes to the hardware infrastructure. The software radio has emerged from military applications. It mitigates the traditional hardwired radio platforms to a flexible software radio platform that can support multiple modulation waveforms and multiple air standards. Recent advances in high-speed Digital Signal Processors (DSPs) and Analog-to-Digital Converters (ADCs) have made commercial implementations of the software radio more feasible [111], [116]. Current cellular base stations use three-sector antennas. These require one receiver per carrier per antenna element in each sector. With the introduction of AAA into cellular systems, the number of channel receivers for each base station linearly increases the size and cost of the base station due to analog components used in the RF front end. With the wide-band receivers used in a software radio, a single analog front end can be used to receive all the channels [105], [106].

Various mobile communication standards will continue to exist even in the future and different frequency bands have been allocated to cellular communications in different countries around the world. This presents a dilemma for handsets since each handset will need to support different cellular standards when roaming between service providers and countries. It is therefore important to develop a handheld terminal that can be used as a multimode transceiver. This can be achieved using software radio

technology [117]. Software defined air interfaces are becoming increasingly feasible for handsets and base stations due to the reconfiguration functionality of Software Defined Radio (SDR). A SDR will allow equipment/air interface re-configuration via either manual or over-the-air command or software download. The SDR forum has developed a set of scenarios in order to support software download. The scenarios are discussed in detail in [122]. The multimode software radio hardware should consist of a reconfigurable Baseband DSP or Field Programmable Gate Array (FPGA) and a broadband analog RF front end [120]. Various applications of the software radio are discussed in [104] and [107]. Figure 5.1 shows a functional block overview of a generic software radio. These functional blocks are discussed in Sections 5.4 and 5.5.

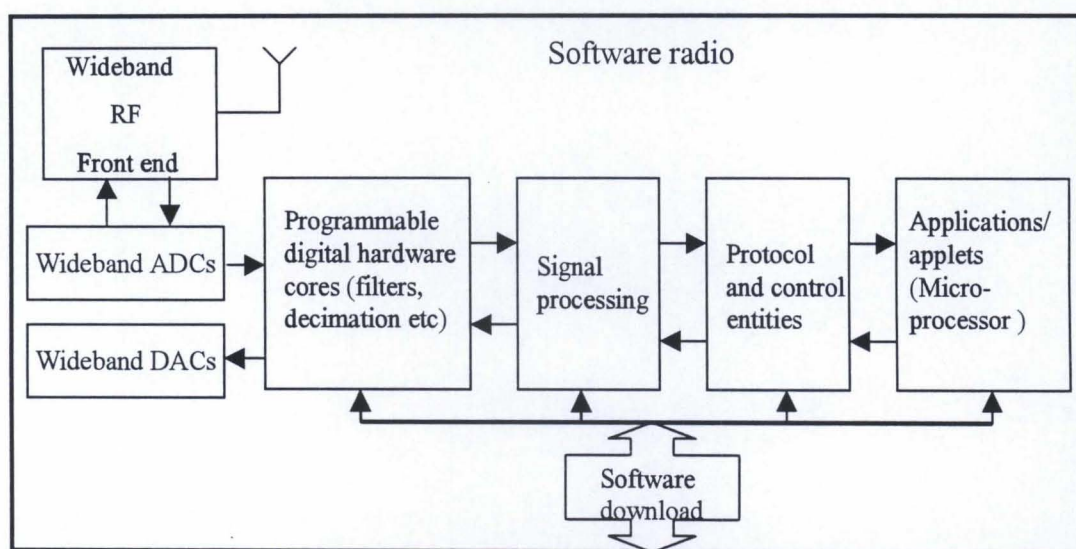


Figure 5.1: High-level view of a generic software radio [119]

5.2 Benefits

The benefits of a software radio are summarized below:

1. It reduces the cost, size and complexity of the base station
2. It provides flexibility to optimize the system performance over time and reduces the system deployment risks.
3. The implemented system can easily be tailored to specific customer needs for mass and niche markets.

4. A software radio incorporating adaptive array beamforming at the receiver can increase the total carried traffic in a system
5. It reduces the transmitted power and probability of call blocking and forced termination.
6. The FPGA based software radio platform allows real time system simulation

5.3 FPGAs in Software Radios

An FPGA is an array of gates with programmable interconnect and logic functions that can be redefined after manufacture. Recently, FPGA technology has undergone remarkable advances in density, performance and power [121]. FPGA based software radio platforms allow the designer to realize a data path that exactly matches the required processing, while at the same time maintaining the flexibility of a software approach. FPGA's are used for fast Application Specific Integrated Circuits (ASIC) prototyping. FPGA's are off-the-shelf commodity items that provide a silicon feature set ideal for constructing high performance DSP systems. The benefits attainable via the use of ASIC's are a core motivation for the use of FPGA's in many systems. Application specific configurations can be implemented on FPGAs at run time. The FPGA's are usually configured when the system power is switched on and it thereafter performs fixed operations until the system power is switched off. Modern FPGAs allow dynamic reconfiguration, where a portion or the entire chip can be reconfigured "on the fly" while it is busy with signal processing tasks [104]. Furthermore, FPGAs can be configured to provide DSP functions such as array multiplication and accumulation. The benefits and functions of FPGAs are discussed in [104].

The implementation of the proposed receiver of Chapter 4 uses an FPGA based software radio (SWR) platform. A PC/DSP/FPGA SWR based test bed based on an Alcatel Altech Telecoms (AAT) SWR is utilized in order to generate frame synchronization signals and communicate with the implemented receiver in the software radio. This test bed can be used to evaluate the performance of various FPGA

based transceivers. The test bed is designed as a three-layered architecture and the various interface and protocol specifications are discussed in Section 5.4.

5.4 System overview of the Test bed

The test bed consists of three components; a PC, a DSP interface (plugged into the PC) and an FPGA based software radio. Within each of these components are various functional blocks. These functional blocks are shown in Figure 5.2.

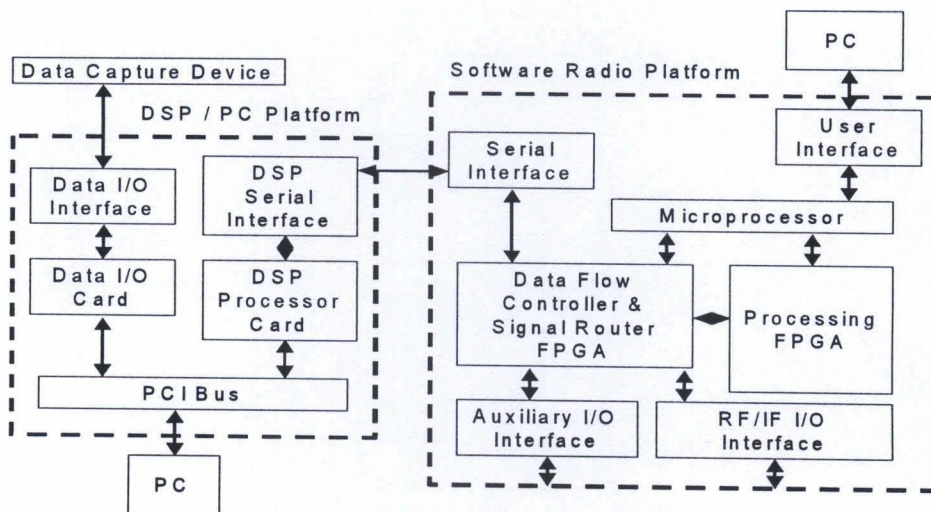


Figure 5.2: SWR test bed block diagram

In order for the three primary components to effectively communicate, various interfaces and protocols are required. It is convenient to describe these interfaces in a three-layered format presented graphically in Figure 5.3.

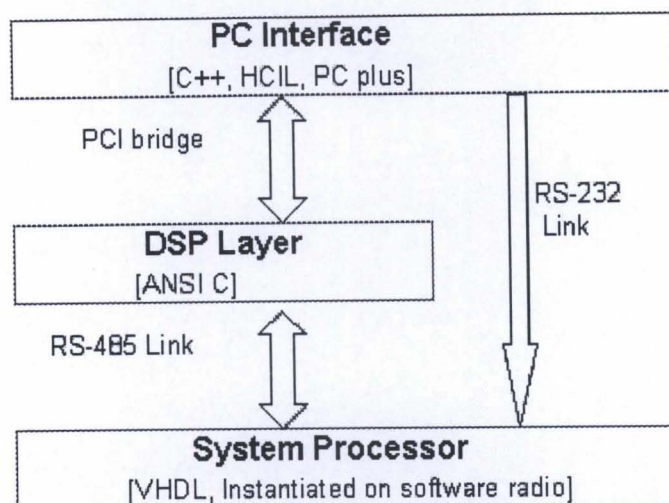


Figure 5.3: Three-layered system

5.4.1 PC interface

The PC interface between the DSP and the PC is written in C++ programming language (ANSI C libraries can be used for the portability across C/C++ compilers). The Host Communications Interface Library (HCIL) is the primary means of interfacing the PC to the DSP board.

5.4.2 The DSP layer

The DSP layer is responsible for data processing, formatting and transmission from the PC to the SWR. In the DSP layer, the PCI/C6200 DSP card has two on-board telecommunications specific devices, namely a controller chip (MT90810) and an SC4000 telecommunications IC. Both of these ICs are essentially temporal switches, which allow framed data, packed in time slots, to be switched between the DSP and the ports of the respective ICs. The DSP board uses a PCI bus to communicate with the PC, while an RS-485 link is used to transmit bi-directional data to the software radio. An RS-485 I/O board, required for interfacing the SWR to the DSP card, contains the necessary RS-485 line driver and receiver circuitry. The connection between the RS-485 I/O board and the SWR is achieved using a multi-twisted cable equipped with 64-way connectors on either end. The RS 485 interface carries the signals for both the SCI

and SDI interfaces which are discussed in Section 5.6.2. The RS485 receivers exhibit high immunity to common mode noise, which allow significant transmission distances to be achieved over the interface

The PC provides a number of utilities to aid the development process; one of these is the Host Communications Interface Library (HCIL). HCIL is a library of functions that provides easy access to the DSP hardware. The library removes the need for a detailed knowledge of the interface between the PC host and the DSP board. This library is based on object-oriented technology and presents DSP systems and their associated components as objects. For example when an application performs an operation such as downloading DSP code to a processor, it will use exactly the same library function independent of the processor type, board type and host operating system [103].

HCIL provides functionality to perform the following tasks:

- Download and run DSP code on the processors in the system
- Transfer data between the PC host and DSP boards in the system
- Communicate with the DSP boards in the system
- Access a system containing different board and processor types.
- Control and interrogate the configuration of peripherals

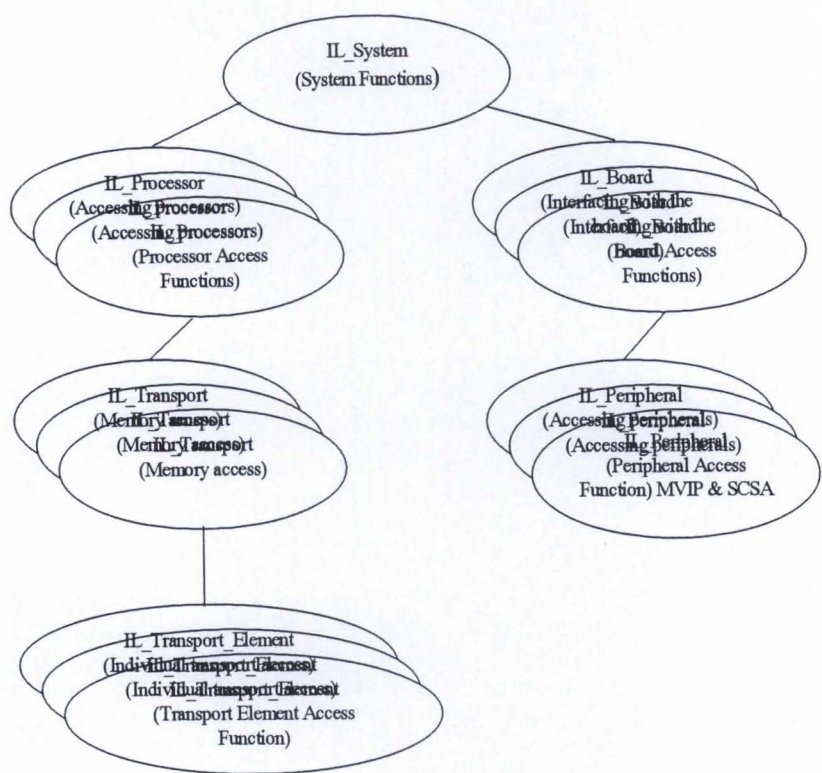


Figure 5.4: Overview of HCIL [103]

Figure 5.4 provides an overview of the HCIL. The library is categorized into several groups of functions, each of which provides access to different aspects of the DSP system. Normally a system contains one or more DSP boards, each containing one or more DSP processors. The boards and processors may be of different types. The HCIL categories shown in Figure 5.4 are discussed below.

5.4.2.1 System access functions: System access functions are provided for accessing the system boards and processors. A System Description File (SDF) must be created to define the boards in the system. This function uses the SDF to initialize the library for the particular system and returns a ‘system handle’, which can be used in all system and group access function to calls to reference the system. User defined applications can perform operations on user defined groups of processors in the system by referencing the ‘system handle’ to the system. The functions provided to allow these operations are referred to as group access functions, which allow DSP programs to be downloaded to

the processors [103]. A group specification list must be created to define which DSP programs to download to which processors. Group access functions do not initiate the data transfer between the PC and the DSP board. This can be done by using the process access and transport access functions.

5.4.2.2 Processor Access Functions: These are used to send interrupts to a specific (individual) DSP thereby allowing data to be transferred between memory on the DSP boards and PC. Processor access data transfer functions are referred to as simple transfer functions and provide access to any memory accessible from the processor. This function removes the need for a detailed knowledge of underlying PC/DSP transfer mechanisms provided by the board, by exploiting the HCIL's knowledge of the system.

5.4.2.3 Transport Access Functions: Transport access (memory) functionality establishes transport objects, which allow the PC to communicate with memory attached to the DSP. Once a transport object is instantiated, the elements that it encapsulates may be used to physically transfer data between the PC and the DSP memory. These functions are provided by the *transport element access routines*. Transport element access functions are parameterized according to address, block size and block length. Data transfer can take place using the transport element functions. Multiple transfers can take place using a single transport element. Each system can contain one or more boards, which can be accessed individually through *board access function*.

5.4.2.4 Peripheral access functions: These provide a means of controlling the configuration of peripherals which are attached to the board, for example Multi Vendor Interface Protocol (MVIP) and System Control System Architecture (SCSA) devices. Several interface functions are discussed in Section 5.6. The third layer is the system processor layer, which is the software radio (explained in detail in Section 5.5). The proposed receiver is implemented in this layer.

5.5 Alcatel Altech Telecoms (AATs) software radio platform

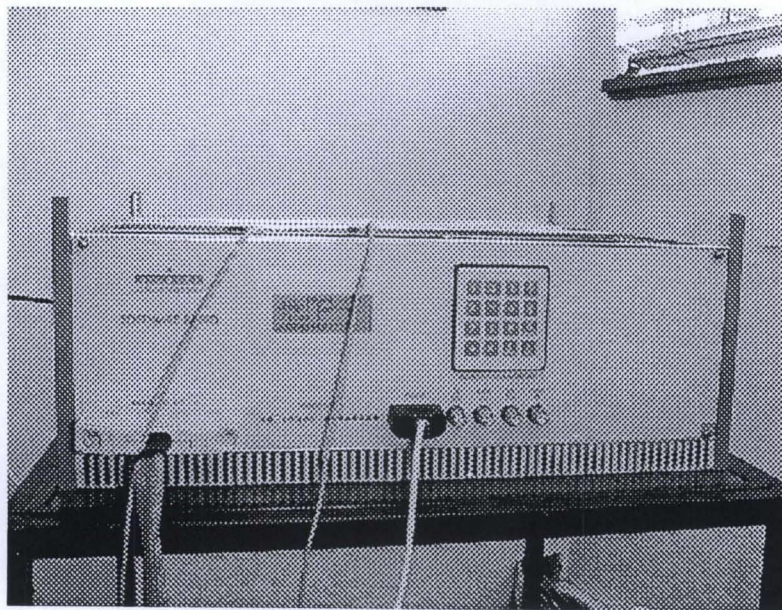


Figure 5.5: AATs software radio

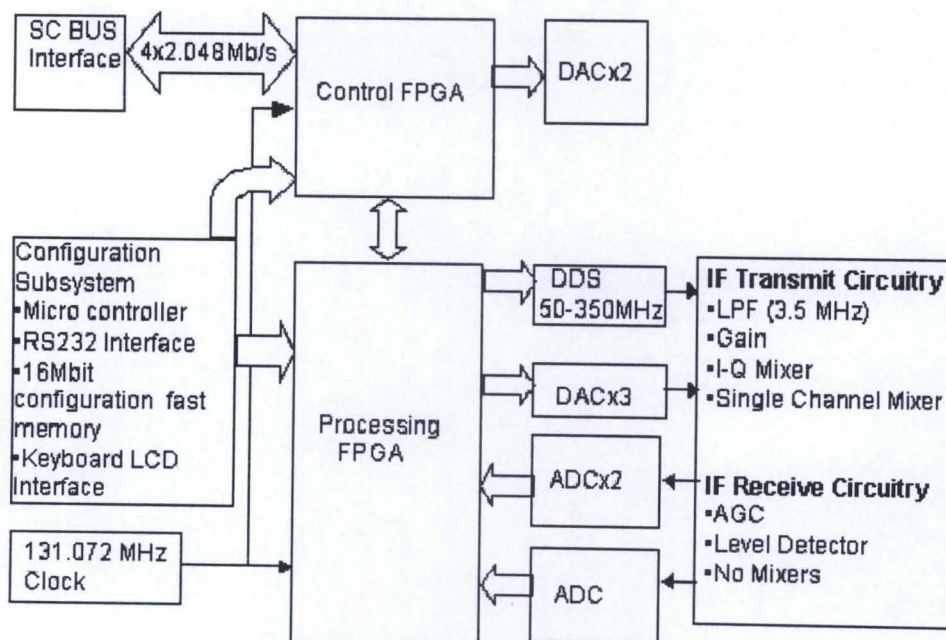


Figure 5.6: The software radio block diagram (AAT)

Figure 5.5 shows the AAT software radio, while Figure 5.6 depicts the functional block diagram of the radio. The digital core of the SWR consists of two high speed FPGAs,

namely a “Control” FPGA (CFPGA) and a “Processing” FPGA (PFPGA). The CFPGA can be used for such functions as pre-processing of Baseband input and output data. The PFPGA is intended for implementing the digital radio and data processing functions. The PFPGA interfaces to the three RF transmitter channels with three 12-bit 100 Msps DACs and three RF receiver stages with a 12-bit 65 Msps ADC and two 12-bit 40 Msps ADCs. The designer can select the appropriate channels as per particular design requirements. The DAC outputs have a bandwidth of 8 MHz and are low pass filtered prior to amplification in order to reject spectral alias components in the output signal. The ADCs and associated analog circuits implement the analog receiver functions on the software radio. Each receiver stage includes level detection circuitry and automatic gain control for each ADC in order to keep the input signal to the ADC within the full scale input range of the ADC.

An RS232 interface from the PC to the SWR micro-controller (87C51) is used for a variety of tasks. First, it is a means of receiving configuration information from the PC. This configuration information will allow the FPGAs to be configured with valid hexadecimal files. These configuration files are not sent directly to the FPGAs. Rather, they are stored in one of 10 file areas in the 16Mbit flash memory. Since there are two FPGAs, these files are divided into two sets of 5 file areas. Once a valid file has been downloaded to the flash memory, the micro-controller can use this information to configure one of the FPGAs. The micro-controller is also capable of performing various boot-up operations such as configuring the FPGAs with the configurations from file area for each of the FPGAs. Once the FPGAs are configured, they interface with several peripherals that may use in the system design. Firstly, the SC bus is implemented in the hardware on the control FPGA. A 131.072MHz clock drives both FPGAs, so the timing for the SC bus can be derived from this master clock. Secondly, to test any base-band signal processing, these signals need only to be written to DACs. There is a bi-directional interface between the two FPGAs, which provides added functionality. Finally, the processing FPGA interfaces directly with 3 DACs and ADCs. Also in the SWR there is a Direct Digital Synthesizer (DDS) used for up conversion from the base-band to IF. These up-converter mixers are present on the software radio

board. These DDS can operate over a frequency range from 60 MHz- 350 MHz, but component changes are required in the synthesizer circuit hardware to achieve a given frequency range. The current hardware allows a programmable frequency range between 60 MHz and 80 MHz.

5.6 The Interfaces

In this section details relating to the interconnection between the three test bed components are provided.

5.6.1 DSP layer and PC platform interface

The DSP card is inserted into one of the Peripheral Component Interconnect (PCI) slots of the host PC platform. The PC and DSP will swap both data and command information and the interface is thus subdivided into three layers namely, physical, data transfer and the command transfer layers.

5.6.1.1 Physical layer: All the information flow between the DSP card (PCI/C6200) and the PC is achieved by means of a PCI bridge. The information that is to be transferred over the interface will be written or read by the PC into or from the DSP card's specified and pre-allocated memory locations. Two mailbox registers are provided on the DSP card. One mailbox is used for conducting a short message from the DSP card to the PC, while the other one is used to conduct a message in the opposite direction. Interrupts may be generated to both the PC and DSP when those registers are read and written. A new message can be generated only if confirmation has been received that the previous message has been read.

5.6.1.2 Data transfer layer: The transfer of data (user information) is accomplished in packets. The packet contains a 16-bit header field indicating the size of the packet in bytes. The data transfer is bi-directional and transmission and reception processes are independent. The transmission of a data packet is a sequence whereby the PC reads a

data packet from the DSP card memory location while the reception of data is the process in which the PC writes a data packet to the DSP memory location. These sequences are governed by handshaking routines in which the availability and reception of data is controlled by “Rx Ready”, “Rx Available”, “Tx Available”, and “Tx Ready” messages as shown in Figure 5.7

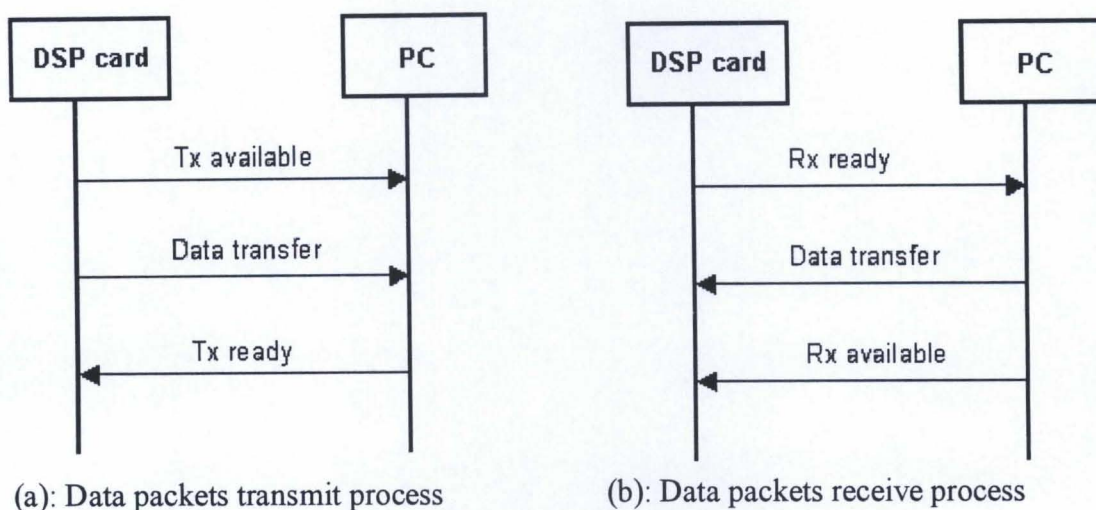


Figure 5.7: PCI/DSP data transfer process [124]

The data packet transmit process is shown in figure 5.7 (a). When the DSP card has a data packet that is available for transmission to the PC, it issues a “Tx available” message. As shown in figure 5.7 (b), the DSP card issues an “Rx Ready” message to the PC when it is ready to receive a data packet. Upon completion of the packet transfer the PC/DSP should be notified. Signaling is used on this interface in order to facilitate information flow control. Signaling is conducted using messages that are passed through mailbox registers.

5.6.1.3 Command transfer: Figure 5.8 shows the PC/DSP command packet format. The transfer of command information between the DSP and PC is achieved in command packets. The packet has a width of 16 bits. The first field in the packet is the “length” field. This field indicates the size of the packet in bytes, excluding the size of the “length” field. The maximum length of the packet is 1022 bytes [124]. The next field is

‘command code’ field as shown in Figure 5.8. The command code field indicates the type of command that is being communicated over the interface. The command field is followed by 16 bit parameters (parameters of SCI command word).

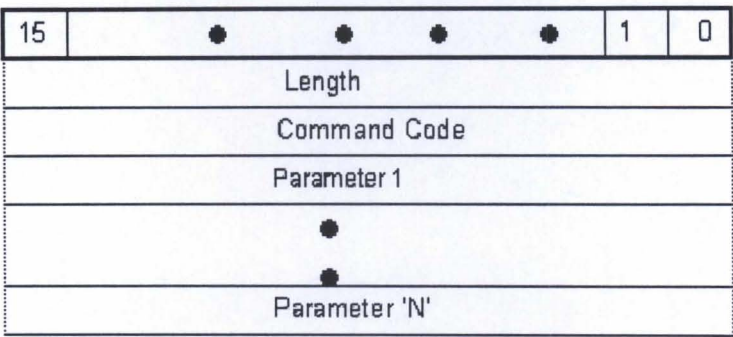


Figure 5.8: PC/DSP Command Packet Format

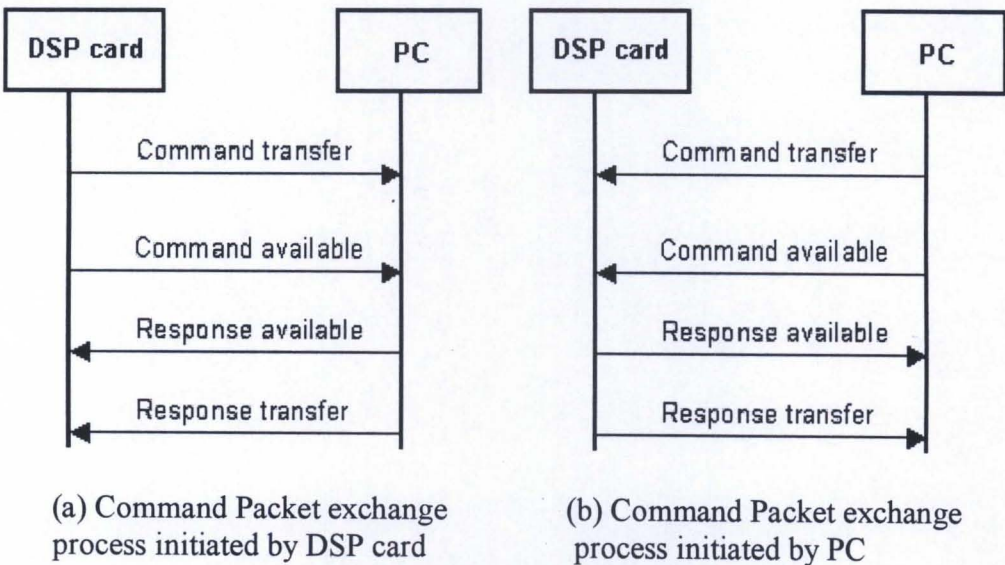


Figure 5.9: PC/DSP command packet exchange

Figure 5.9 shows the command packet exchange process. The PC notifies the DSP card about the completion of packet transfer by sending a ‘command available’ message and ‘response available’ to indicate the availability of response from the DSP card. Figure 5.9 (b) shows the packet exchange initiated by the DSP. The DSP card signals availability of a new command by issuing a ‘command available’ message to the PC when it is allowed to send a command packet. The PC performs the command and response is generated and notified to the DSP card by issuing a ‘response available’ message. A time out condition is declared if there is no response received within 1

second and a new command packet is issued only if the sending party is not expecting any reply for the previous received command.

5.6.2 The SWR platform and the DSP platform interface

The DSP platform consists of two physically separate interfaces, namely a Serial Data Interface (SDI) which is driven by an SC4000 IC and a Serial Control Interface (SCI) controlled by the Multi Vendor Interface Protocol (MVIP) controller chip. The physical link between the DSP card (PCI/C6200) and the software radio is implemented over an RS-485 interface which will carry the necessary SCI and SDI signals separately, in order to ensure the signal integrity on these signals. The RS-485 interface is implemented by means of RS-485 line driver and receiver circuitry (RS-485 interface card) located at the DSP card side and on the software radio. The physical connection of the RS-485 interface is achieved by a multi-twisted pair cable with 64-way connectors equipped on the other side. The SDI and SCI consist of four 2.048Mb/s serial streams to and from the DSP processing platform and the SWR, together with related timing/framing signals [103].

5.6.2.1 SCI: The SCI interfaces only with the CFPGA. The SCI uses four bi-directional 2.048Mb/s streams, called SCI channels. Each parallel channel is subdivided into frames of 125 μ s and each frame is equally divided into 32 8-bit time slots of 3.906 μ s. An SCI word consists of four slots (32 bits) belonging to the four channels of the same direction and the frame is the same for the input and output channels. The SCI protocol defines the interchange of SCI words between the DSP card and the SWR. Figure 5.10 shows the single command transfer initiated by the SWR.

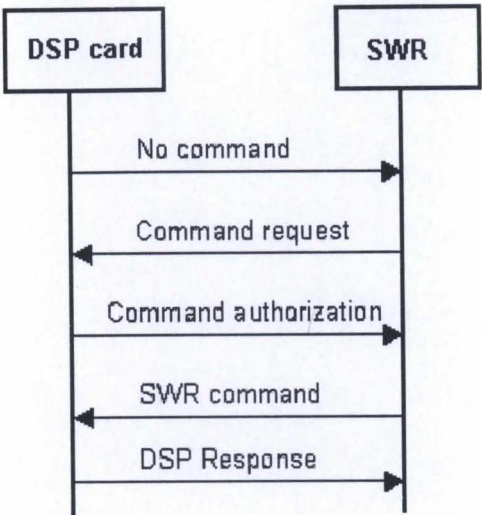


Figure 5.10: Single command transfer sequence by SWR [124]

When the DSP card sends a command it expects a response within two time slots and waits for another two time slots to send a new command i.e. a new command is issued every fourth time slot. If a command or response word has been corrupted, the DSP card should retransmit the affected command. A timeout will be declared and the command is discarded if it fails three consecutive events. The DSP card is the master of the SCI protocol, however the SWR can initiate a single command transfer to the DSP card from the SWR as shown in Figure 5.7. This is achieved by the SWR requesting permission to send a command. The transfer can only be initiated if the DSP sends an empty command word to the SWR. Once the DSP card has granted permission the process (as shown in the Figure 5.7) is followed. This sequence occupies 3 command words and 2 response words [124]. If any of the command words are corrupted, the transfer sequence is interrupted. The SWR will have to restart the sequence when it detects an empty command word from the DSP card

5.6.2.2 SDI: The SDI uses four 2.048Mb/s transmit and four receive signals of the SC (SCSA) bus on the DSP card as well as the SC bus clock and framing signals. These four parallel streams are called SDI channels. Each channel is subdivided into 125µs frames and each of these frames is subdivided into 64 4-bit granules, allowing 256 granules in the same direction on the four parallel channels [128]. Transmission of data is accomplished in SDI packets; each packet contains an 8-bit header field and a

variable length data field. The packet length is measured in granules and the header contains information about the number of granules in one packet. The most significant bit of the header is given as the first bit of the first header granule. The construction of SDI frame is shown Figure 5.11, where grX denotes a particular granule.

TS	0		1			30		31	
Channel									
SDI0x	gr0	gr4	gr8	gr12		gr240	gr244	gr248	gr252
SDI1x	gr1	gr5	gr9	gr13		gr241	gr245	gr249	gr253
SDI2x	gr2	gr6	gr10	gr14		gr242	gr246	gr250	gr254
SDI3x	gr3	gr7	gr11	gr15		gr243	gr247	gr251	gr255

Figure 5.11: SDI Frame Format [128]

TS	0								1	
Channel										
SDI0x					d3	d2	d1	d0	gr8	gr12
SDI1x	h7	h6	h5	h4					gr9	gr13
SDI2x	h3	h2	h1	h0					gr10	gr14
SDI3x	d7	d6	d5	d4					gr11	gr15

Figure 5.12: SDI Protocol Fields [128]

The same principle applies for the data field of the packet, whereby the most significant bit of the data is given as the first bit of the first data granule. The minimum data length of a packet is zero granules (i.e. an empty packet) and the maximum data length is 254 granules. An example of packet with data length of 2 granules (8 bits) is given in Figure 5.12. This packet occupies granules 2-5, with the header occupying granules 2,3 and with data occupying granules 4 and 5. The value of the header field is 2, that is, bit h1 is set while all other header bits are zero.

In order to accomplish the data transfer between the DSP card and the SWR, a unidirectional channel called SDI logical channel is used. All the SDI packets that are to be transmitted are associated with a specific SDI logical channel. Only one SDI packet is transmitted per SDI frame per logical channel. The SDI packets that are associated with a specific channel start at a predetermined granule within the frame. The start of the packet is configured upon setup of the SDI logical channel. The length of the channel may vary from 0 to a maximum length of 1 granule and the maximum

length can be configured upon the setup of the logical channels. Data transmission on a particular logical channel terminates with the logical channel deletion (achieved by issuing specific SCI commands from the DSP).

Utilizing all the above-mentioned facilities in the SWR and associated components makes the test bed attractive for the testing of various FPGA based transceivers. An FPGA based software radio can be used as the third layer of the test bed. Many traditional software constructs and techniques are available in current FPGA design tools. The language of choice in this project is VHDL. Specific design tools used are Synopsys FPGA Express 3.5 for the VHDL synthesis and Max+Plus II software for compiling exported EDIF files to the target Altera (FPGA) devices.

5.7 VHDL

VHDL (Very High speed integrated circuit Hardware Description Language) is an offshoot of Very High Speed Integrated Circuit (VHSIC) program that was funded by the US department of Defense in late 1970s [126]. The goal of the VHSIC program was to produce the next generation of integrated circuits. The goals were achieved admirably, but in the process of developing these extremely complex integrated circuits, the designers found out that the tools used to create these large designs were inadequate for the task. Creating complex designs using gate level tools was a challenging task and therefore a new hardware description language was proposed in 1981, called the VHSIC Hardware Description language or VHDL. VHDL was embraced as the universal communication medium of designing FPGAs. In 1986, VHDL was proposed as an IEEE standard. VHDL is widely used to model digital systems at different levels of abstraction ranging from the algorithmic level to the gate level. Recently the language has been used to model communication systems and protocols [125].

Hardware description languages can be used in several ways; they can be an alternative way of representing a circuit diagram for a digital circuit or a higher level algorithmic

‘program’ that solves a particular problem. Such structural or behavioral representations are two ways of describing a model of a digital system. In VHDL every portion of a VHDL design is considered a block. A VHDL design may be completely described in a single block, or it may be decomposed into several blocks. Each block in VHDL is analogous to an off-the-shelf part and is called *entity*. The entity describes the interface to that block and a separate part associated with the entity describes how that block operates. The interface is similar to a pin description in a data book, specifying the inputs and outputs to the blocks. The description of the part is like a schematic for the block. A block is a design, and a complete design may be a collection of many blocks interconnected. Signals exist between the blocks and are more complex than the variables of traditional programming languages. Signals know about time and need a finite time to change. Variables also exist in VHDL but these can only be used inside processes, procedures or functions.

VHDL is a strongly typed language and does not possess the automatic promotion of one type to another which is present in C programming. For example, while adding a float to integer, each type conversion needs a specific conversion function written for it, or a reference made to a library of such resolution functions. The second part of the description of a VHDL design is a description of how the design operates. This is defined by the *architecture* declaration. The architecture describes the behavior of the entity. A single entity can have multiple architectures. The following is an example of an entity and architecture declaration in VHDL and explanation of codes are discussed below.

1. entity latch is
2. port (s, r : in bit;
3. q, nq : out bit);
4. end latch;
5. architecture dataflow of latch is
6. begin
7. q<=r nor nq;
8. nq<= s nor q;
9. end dataflow;

Each declaration contains a list of names, a mode, and a type. In the entity declaration, two input signals are defined (s and r). The declaration also contains the nature (type) of the signals and the mode. The mode specifies whether this is an input (in), output (out) or both (inout). The signals s and r are of mode in (input) and type bit. Notice the particular use of the semicolon in the port clause. Each interface declaration is followed by a semicolon, except the last one, and the entire port clause has a semicolon at the end.

Line 5 indicates the definition of a new architecture call dataflow and it belongs to the entity named latch. So this architecture describes the internal operation of the latch entity. The lines 7 & 8 describe the latch's operation. Line 7 shows that the data coming from signal 'r' and 'nq' flow through a NOR gate to determine the value of signal 'q'. The 'nor' represents a built-in component called an operator. The right side of the <= operator is called an expression. Evaluating the expression is performed by substituting the values of the signals in to the expression and computing the result of each operator in the expression. The signal 'q' depends on 'r' and 'nq' since data flows from 'r' and 'nq' to 'q'. In general, the signal on the left side of the <= operator depends on all the signals appearing on the right side. If a signal depends on another signal that upon which an event has occurred, then the expression in the signal assignment is re-evaluated. If the result of the evaluation is different than the current value of the signal, an event will be scheduled to update the signal with the new value.

VHDL simulators can be used for removing syntactical errors and isolating a limited number of logical errors. The simulator will ‘perform’ the VHDL code and indicates considerable information about the timing perspective of the ‘performed’ design or a resource usage perspective in vendor-specific tools. The simulation is based on the timing and resource usage derived from an actual implementation, not an algorithmic version; as a result it will perform comparably on the final target. Synthesis tools transform VHDL code into a file (Hexadecimal (HEX)) that can be used for downloading to an FPGA device. In this project, the synthesis operation is shared between Synopsys FPGA Express and Max+Plus II. FPGA Express is used to create an optimized netlist and can analyze the timing constraint of the design. Max+Plus II is used to extract the netlist, synthesize the logic, fit, extract timing information and finally assemble the project to a HEX file for downloading to the FPGA. Interface software PC Plus is used to download this file to the software radio over the RS-232 interface. This method of implementation was used to generate all the functional blocks discussed in Chapter 6.

5.8 Conclusion

This chapter has briefly explained the theoretical concepts of a software radio. The flexibility of a software radio is derived primarily from the fact that a large percentage of the radio functions are defined at the time of use, rather than the time of design. The reconfigurability of the software radio makes it suitable as a component in future 4G communication systems that require flexibility to achieve global roaming goals.

A useful test bed is presented and explained graphically in three layers. This familiarizes the reader with the implementation background. An FPGA based AAT software radio platform offers many of the features inherent in the software radio concept. The system has proved to be capable of high speed digital processing and is ideally suited to the development of time critical system components. It is a highly useful tool in developing various CDMA and digital transmission system entities such as the AAA receiver which is presented in the Chapter 6. An FPGA based SWR

provides a good alternative to system simulation on a purely PC platform for two main reasons. Firstly speed, FPGAs provide parallel computing capabilities and a high rate system clock. The FPGA can outperform a PC when it comes to lengthy bit-level simulations. Secondly, once the system has been coded in VHDL, it is ready to be used in a practical system. There is no need to build hardware to emulate the simulation code written in C. Rather, the system is ready and implementable. These two factors make the software radio an attractive development tool. Having established the benefits of this platform an understanding of the various SWR components and their interfacing requirements was then presented. The logical steps for the synthesis and design tools, and environments employed to design the FPGA to implement the communication system entities are also discussed. It is the intention of this research to pursue the development of the AAA receiver to a point where its functionality can be used to compare measured BER results with those obtained from simulation.

Chapter 6

FPGA Implementation of AAA Receiver

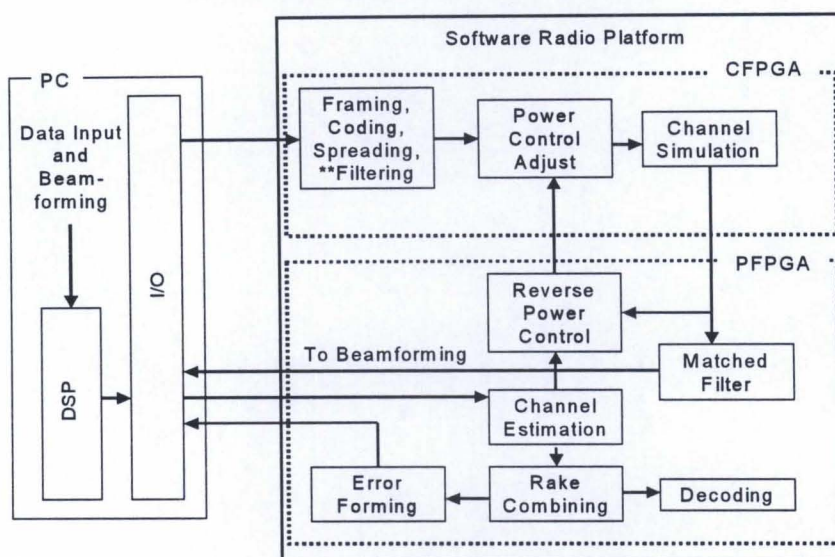
6.1 Introduction

This chapter will discuss the implementation issues and measured results of the WCDMA AAA receiver in the FPGA based software radio platform. In order to implement the model assessed in Chapter 4, an Alcatel Altech Telecoms (AAT) prototype software radio is used. As mentioned in Chapter 5 the software radio consists of two FPGAs namely “Control” and “Processing” FPGAs each with a 100,000 logic gate capacity. It is not feasible to implement the whole system model (transmitter & receiver) within this limited capacity. As a result some of the blocks were removed. The functional split in the receiver is discussed later in the chapter. These blocks and the justification for their removal is explained in the appropriate sections. In this thesis, a simple block diagram technique is used rather than VHDL code explanation to explain the implementation of various functional blocks implemented on the FPGAs. Measured results are shown in the appropriate sections to verify the implementation success. Examples of VHDL code written by the author can be found in Appendix A-5.

6.2 Implementation overview

The AAA components are allocated to the available hardware as shown in Figure 6.1. The DSP card has 16 channels that have been divided into 8 transmit and 8 receive channels. If one considers the transmit path, data is generated on the PC and passed to the CFPGA for framing and power control adjustment. In a full implementation of the system this would then be passed to the IF / RF / amplification stages for transmission, where the signal would be impaired by the physical channel. In this work IMT2000 channels are modeled on the CFPGA. For the receive path all receiver blocks except for

the beamforming (implemented on the PC) will be completed on the PFPGA. Beamforming is left for the PC due to the limited capacity in the FPGA (Altera's FLEX10K). In order to achieve this functional split, output from the matched filtering stage is transferred to DSP memory and the weights of the desired beam, generated on the PC, will be stored in a specified memory location of the DSP card. The I/O processing board will update the weights for the channel estimation with respect to the data from these memory locations. Functions such as channel estimation, error forming, RAKE combining and encoding are implemented in the PFPGA.



** Codes from [114]

Figure 6.1: Proposed implementation overview

The data from an input device can be transferred to the DSP card via the PCI bus, processed by the DSP, and passed to the SW radio. The reverse procedure is applicable in the receive direction. As mentioned in Chapter 5 (Section 5.6), the DSP platform to SW radio I/O interface consists of two distinct interfaces, namely serial data interface (SDI) and Serial Control Interface (SCI) either of which can be used for this application. All serial data transfer between the CFPGA and the PFPGA occurs over the Logical Channel Interface (LCI) between the two FPGAs. In order to demonstrate the functional split, a direct link is shown from the PFPGA (matched filter) to the DSP card in Figure 6.1. But there is no direct interface between the PFPGA and the DSP

card. A bi-directional interface block is designed in the CFPGA to realize this functional split as shown in Figure 6.2.

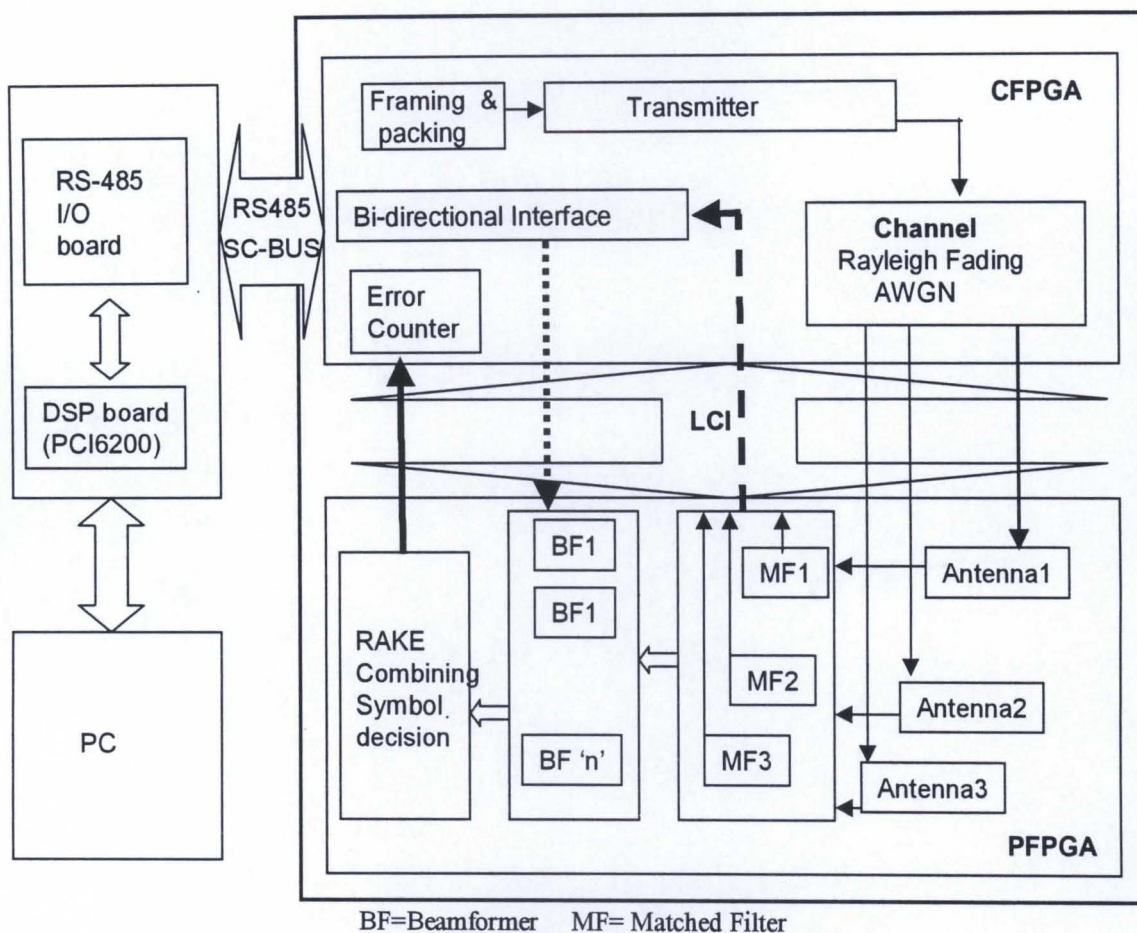


Figure 6.2: System overview

The PFPGA can communicate with the DSP through the bi-directional interface block in the CFPGA. The data from the PFPGA can be sent over the LCI to the CFPGA and can write to the specified DSP memory location. The PC will read the information from the specified DSP memory and process the data (i.e. update weights). The processed data is stored in another DSP memory location and sent over the RS485 channel (SCI or SDI) to the PFPGA via the bi-directional interface. The beamformer block in the PFPGA will read and utilize the processed data.

A detailed description of each functional block is presented in Sections 6.3 to 6.8. In the simulation, performance evaluation of the proposed receiver was carried out with

six antenna elements. Due to limited capacity and resources in the software radio, only three antenna elements and three multipath components can be accommodated since an increase in the number of antenna elements and multipath components will linearly increase the required number of beamformers. An increase in the number of beamformers leads to the need for greater FPGA capacity and will require extra channels on the SC-bus because the weight updating process is performed in the PC. Further degradation of the system performance occurs since the SC-bus consists of only four bi-directional 2.048 Mbps serial links. This division of resources leads to a decrease in the spreading (chip) rate of the system. Various timing complexities were encountered during implementation; these will be highlighted at the appropriate point in the subsequent sections and appropriate solutions proposed.

The software radio transmits to the PC using an RS-485 connection as the physical layer (SCSA telecommunications protocol data). Thus, the TTL logic levels, generated on the DSP card by an SC4000 device (to implement an SC-BUS), are first converted to paired RS-485 differential signals before they are transmitted to the software radio. This conversion is achieved on a daughter-board, which plugs into the PC. On the software radio, the signals are converted back to digital logic levels before being routed to specific pins of both the FPGAs in the software radio. Clearly, on a feed-through net, the signal is delayed by four physical layer signal-type conversions. This introduces a round-route delay (FPGA-DSP-PC-DSP-FPGA) of 200ns, an important factor for the timing of the system

6.3 SC-Bus signals

Different clocking signals and frame synchronization signals are needed, in order to send data over the DSP to the software radio. So it is useful to provide some information regarding SC-BUS signals since their timing and configuration will be required during FPGA configuration.

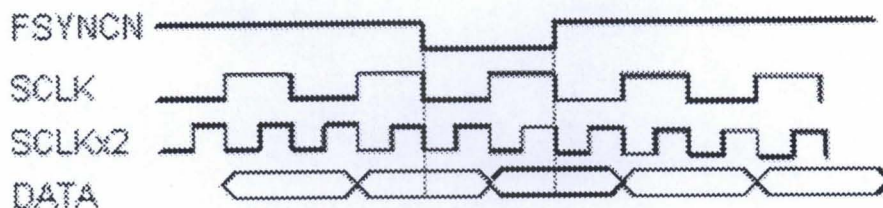


Figure 6.3: SC bus timing diagram [124]

The synchronous relationship between the serial data clocks, the frame sync pulse and the data bits is shown in Figure 6.3. From a design perspective, it is better to allow the software radio to act as the master clock source, and the DSP system as the data source. This may present a serious timing problem because the SCLK is also sent over the SC-BUS and is subjected to delays. The associated data bit will arrive at least 200 ns after SCLK is driven high. In this design, a data rate of 2.048 Mbps was considered. So it is not feasible to allow sampling in the middle of a bit (244 ns) because it is dangerously close to the 200 ns boundary. It has been noticed that the return delay often violated the 244 ns critical delay. Since the data source is interrupt driven, it has to generate data when it receives a bit boundary pulse. Considering the critical delay factor, sampling in the middle of the returned bit had to be avoided. Sampling at $\frac{3}{4}$ of the duration of the bit was considered. SCLKx2 is extremely useful for this purpose, which allows for the bit-level transmission delays.

The SC-BUS is divided into a message bus and a data bus. The message bus is not implemented in the DSP card. Figure 6.3 depicts the three basic SC bus signals. The FSYNCN is an 8KHz frame synchronization signal, indicating the start of a 125 μ s frame. SCLK (serial data clock) and SCLKx2 (double speed serial data clock) are required for bit sampling as discussed.

Figure 6.4 shows the timing diagram of the fundamental signals generated on the CFPGA, which are the same as the frame sync signals from the DSP card. These SC-BUS signals are derived from the 131.072 MHz system clock to synchronize with the SC-BUS signals from the DSP card. The FSYNCN is used to differentiate between the start and end frames. Unfortunately the SC-BUS standards do not match the WCDMA

standards (refer Table 2.1 in Chapter 2), that is the length of the radio frame used in the proposed receiver is 10 ms and consists of 16 slots with each of 0.625 ms duration. The duration of the FSYNCRN frame (in SC-BUS) is 8KHz (125 μ s) and the required frame length is 10 ms (refer Figure 6.5). The easiest way to achieve this standard is to derive the frame sync signals from the system clock. But these must synchronize with the SC-BUS signals because the SC-BUS signals are used to clock other components and functions in the receiver.

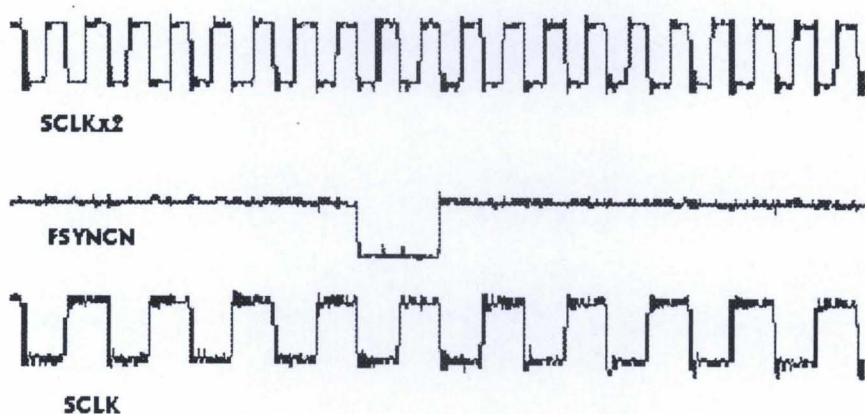


Figure 6.4: SC bus signals measured/generated in FPGA

In order to implement the proposed receiver in the WCDMA standard, various frame sync signals are required. The frame length of 10 ms (100Hz) can be derived from the system clock, but a critical timing problem arises with the SCLKx2 and SCLK signals. Considering the fact that the SC-Bus signals are the basic signals for the system, a new frame standard is considered which is close to the WCDMA standard. Instead of 10 ms, an 8ms (125 Hz) frame length was considered. This is easily derived and can synchronize with the system clock (131.072 MHz), SCLKx2 (4.096 MHz), and SCLK (2.048 MHz) signals. The new frame structure is similar to the WCDMA frame structure shown in Figure 6.5. Figure 6.5 (a) shows the WCDMA frame considered in the simulation and Figure 6.5 (b) shows the frame structure of the implemented frame in the software radio. One frame consists of 16 equally divided slots, each of 0.5 ms duration. Each slot consists of pilot and power control bits and the power control and beamforming algorithms will update every 0.5 ms instead of 0.625 ms. In order to

differentiate the pilot and the power control signals, separate frames are required and derived.

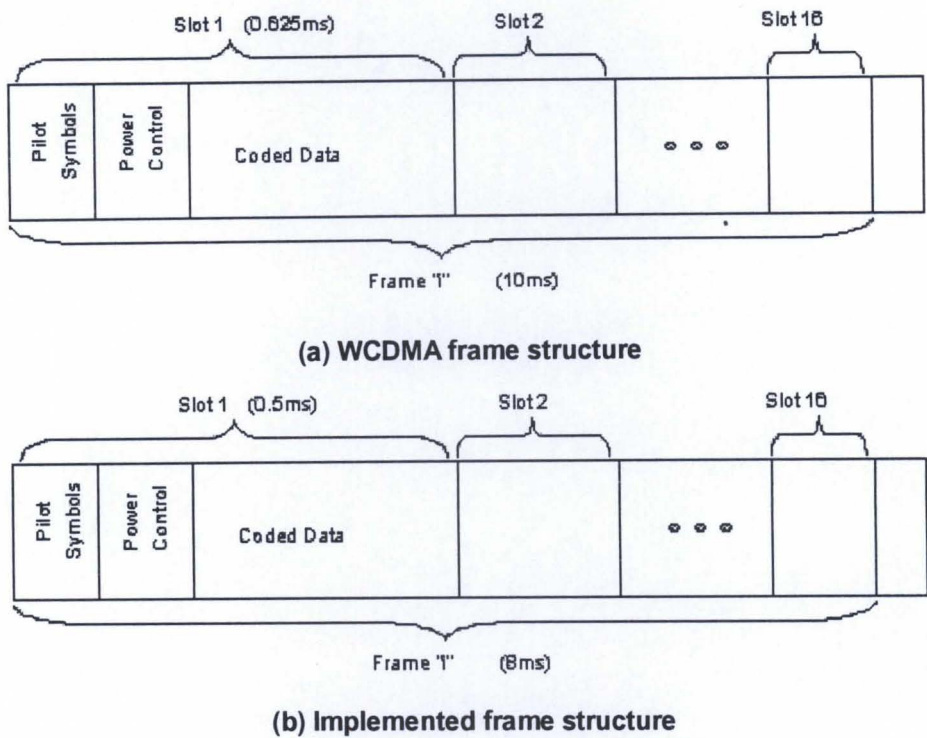


Figure 6.5: Frame structure comparison

Name	Nomenclature	Frame length
Double-speed Serial Clock	SCLKx2	4.096 MHz
Serial Clock	SCLK	2.048 MHz
Frame Sync from DSP	FSYNCN	8 KHz (125μs)
Frame sync for Frame	FSYNCNF	125 Hz (8 ms)
Frame sync for Slot	FSYNCNS	2 KHz (0.5 ms)
Frame sync for Pilot bits	FSYNCNP	2 KHz (0.5 ms)
Frame sync for Power Control	FSYNCNPC	2 KHz (0.5 ms)

Table 6.1 Frame sync signal standards

Table 6.1 shows the frame sync standards used in this design. The synchronization of these signals are critical from an implementation point of view, because if these signals are not perfectly synchronized then the system will misjudge the pilot and power

control signals and data bits, which will affect the performance of the system. The derived signals are carefully examined before implementation using the simulated results. The simulated results of various frame synchronization signals with the data clock 64 KHz are shown in Figure 6.6. Figure 6.7 depicts the comparison of different frame sync signals (simulated using MAX+II). Detailed comparison of each frame signal are shown in Appendix A-4 (Figure A.7-A.8). The VHDL codes used to implement/generate these frame synchronization signals are given in Appendix A-5.

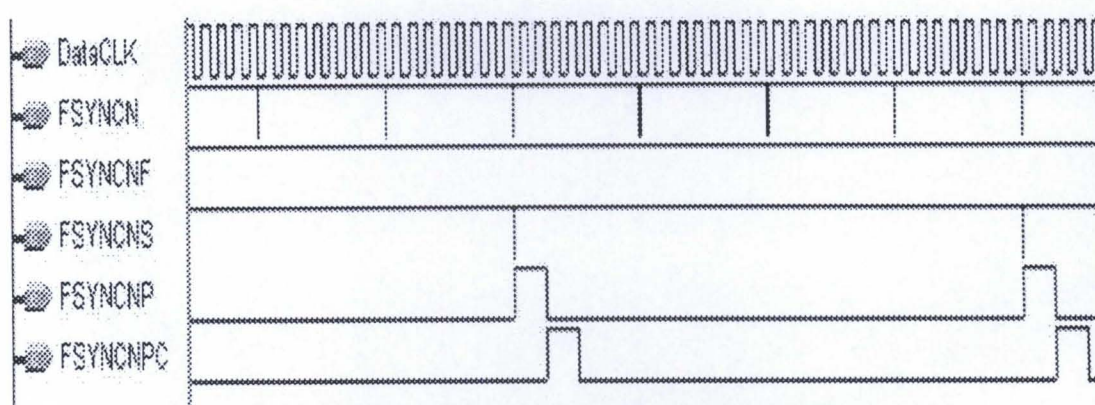


Figure 6.6 Frame sync corresponding with data clock of 64 KHz

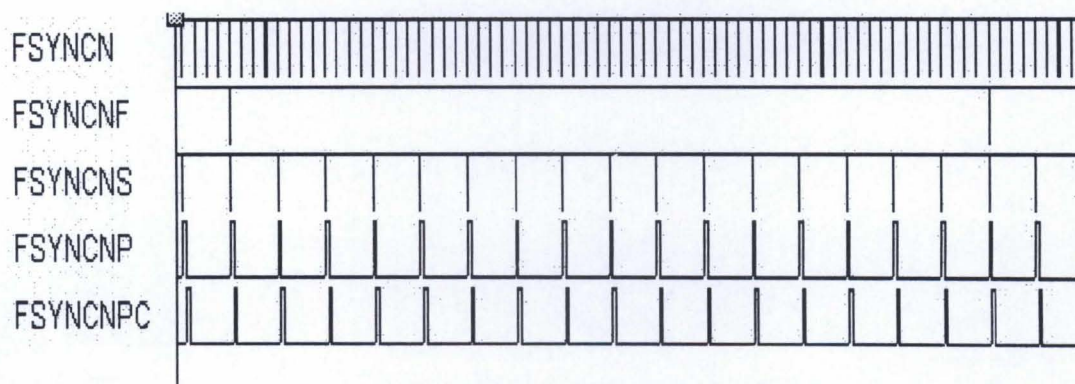


Figure 6.7 Comparison of various frame sync signals

When considering Figure 6.7 one notices that FSYNCNF differentiates the “start” and “end” of the radio frame and FSYNCNS represents the slot in each frame, while the FSYNCNP and FSYNCNPC represent the pilot and power control respectively. When FSYNCNP and FSYNCNPC are high the system will detect the corresponding bit as pilot & power control bits from the traffic channel. Figure 6.8 shows the

measured/generated results from the software radio and corresponding comparison result is shown in Appendix A-4 (Figure A.9).

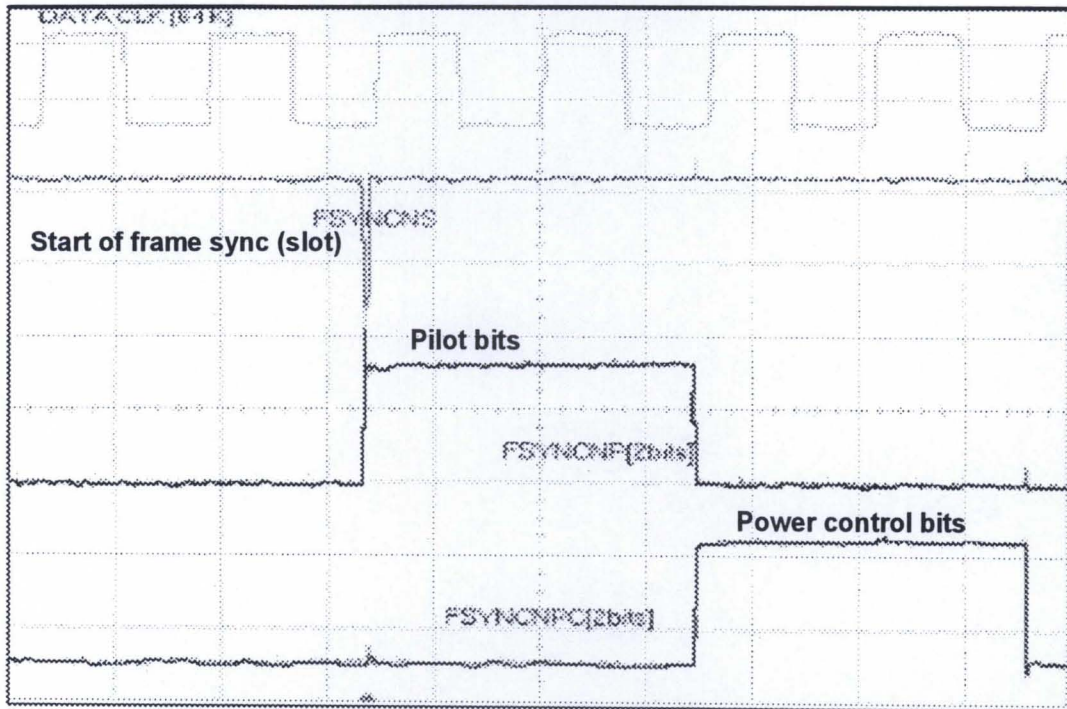


Figure 6.8: Measured frame sync signals with data clock from CFPGA

All the above figures clearly show that the frames are correctly synchronized. Figure 6.7 shows that the 4 FSYNCS frames will exactly fit in one FSYNCF and 64 FSYNCF frames in one FSYNCFPC frame sync. Since the FSYNCS frame sync is a basic frame sync that is included in SC-BUS signals, the FSYNCS frame is considered as the reference frame signal in the design. What has been shown is that the critical aspect of synchronization has been addressed. Necessary frame synchronization and clocking signals are derived and implemented, now the next step is to pack the incoming user data from the PC and time multiplex the pilot and power control signal into a frame (as shown in Figure 6.5 (b)).

6.4 Framing and packing

As mentioned in the previous section the personal computer acts as a data source, giving the designer control over the nature of data sent to the physical layer. The DSP

card is responsible for packing the data, which includes the framing and packing of the data into bytes for the software radio. The data sent from the DSP card is formatted as a series of user bytes, each one stored in a time slot.

A further implementation issue is to re-order the received bytes into bits, so that the user data can be spread and transmitted (the stream needs to contain successive user bits, not bytes). The data from the DSP card is a serial data stream. To carry out the addition or multiplication (required for inclusion of AWGN, Rayleigh fading and beamforming) these need to undergo a serial to parallel conversion. Furthermore, the parallel data needs to be synchronized with allocated time slots. An entity is created to extract bytes and words from the serial data stream. This entity is very useful when dealing with a parameterized system, that is if the system needs to generate the AWGN of a specific SNR, then the parameter would be at the desired noise level. Figure 6.9 illustrates the framing and packing process. Serial to parallel conversion can be achieved by creating a buffer entity, which is capable of re-ordering the received bits.

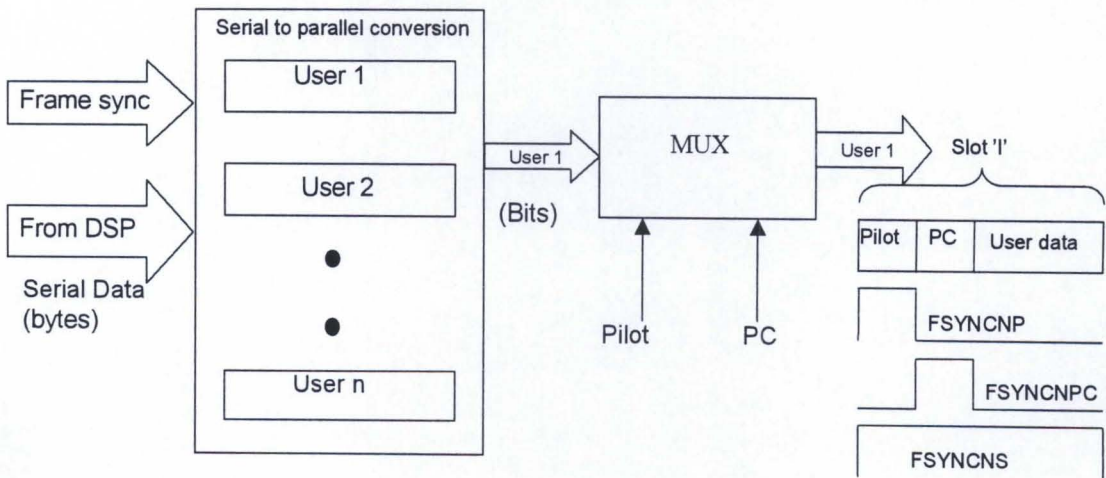


Figure 6.9: Framing & packing process

Conversely, the process needs to be reversed when the data is sent back to the DSP system. Recall that for a SC-BUS standard using a 2.048 Mbps bit rate, the channel consists of 32 time slots, which can be treated as separate user data. The system that

was implemented can support only 16 users. Since there are 32 time slots available and only 16 users are supported by the system, the second half of the frame will be discarded. After reordering the bytes to bits (desired user), known pilot and power control bits are time multiplexed with the data bits in each slot. These known bits are not used in this design. Their inclusion here allows for their use in future work. Justification for this statement is discussed in Section 6.8. These framed data should be convolutionally encoded and interleaved before spreading but due to the limited capacity in the FPGA these functional blocks were removed from the design. Expected BER degradation from this omission can be up to 10^{-3} at 8 dB for a 2-path Rayleigh fading channel (assuming ideal coherent combining of diversity branches) [9]. Once the data is packed in frames it needs to be spread with the PN codes. The spreading function and the results measured at the output of the spreader are presented in Section 6.5.

6.5 Spreader and de-spreader

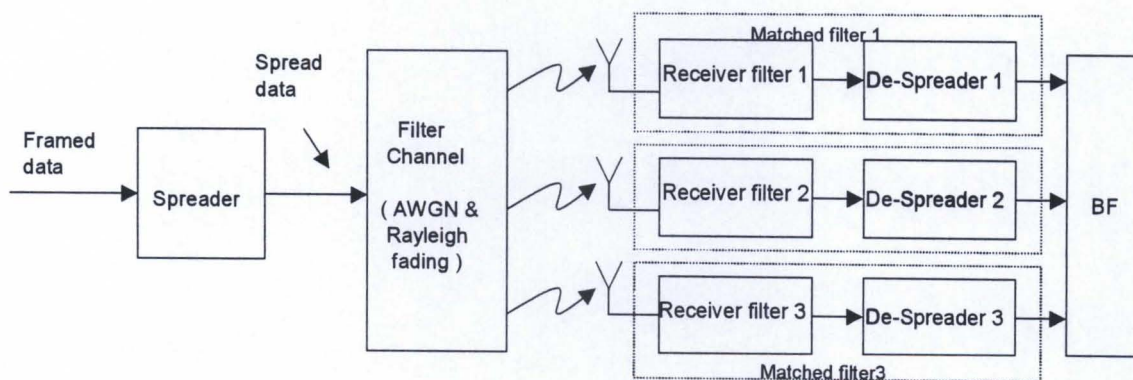


Figure 6.10: Spreading system block diagram

Figure 6.10 shows the spreading/despreading system block diagram. The framed data is coupled to the spreader block for spreading with a PN code. Chapter 2 discusses the generation of the PN sequences. It is important to examine the theoretical aspects of the autocorrelation function of the PN codes before discussing the implementation. If the PN sequence is maximal length, the period of the sequence is $P = 2^n - 1$. Figure 6.11

shows simulated results of the auto correlation function for a maximal length sequence of order 8. The autocorrelation function helps the initial acquisition and synchronization of the PN code at the receiver. If the codes are aligned perfectly, a high correlation occurs. The receiver acquires an incoming sequence with arbitrary phase shifts; then it slides and calculates the autocorrelation. When the autocorrelation reaches its maximum, then the two codes are in-phase and have a zero time shift.

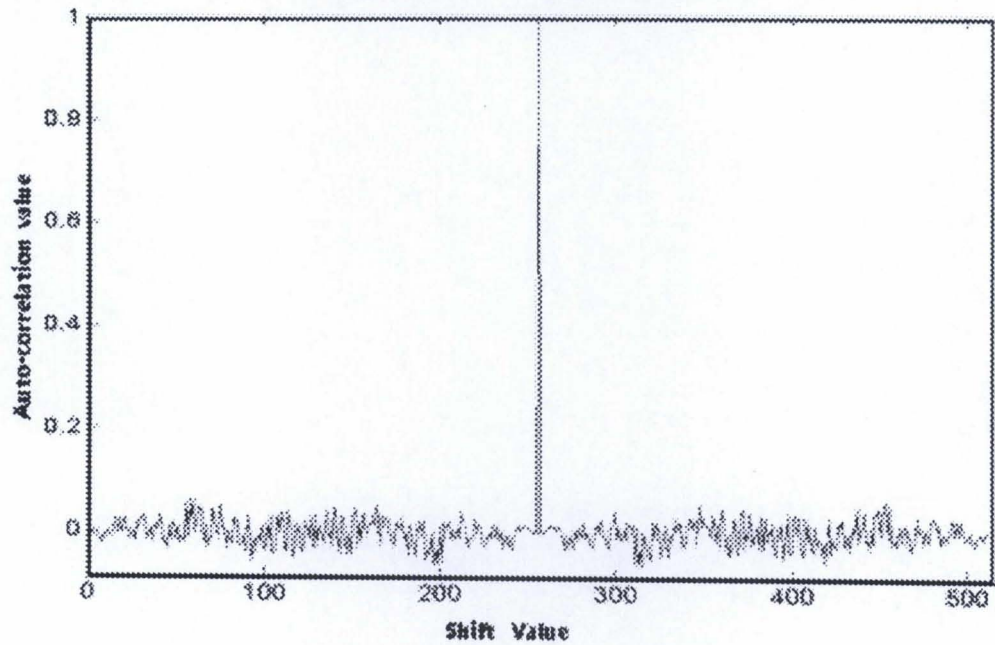


Figure 6.11: Autocorrelation of maximal length order of 8

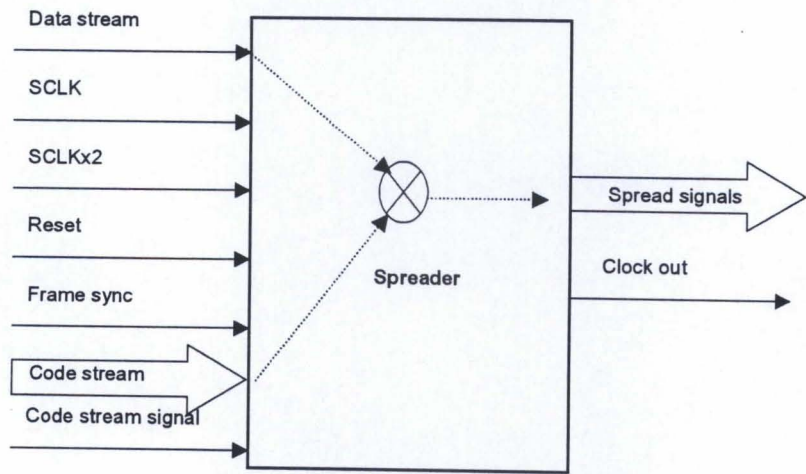
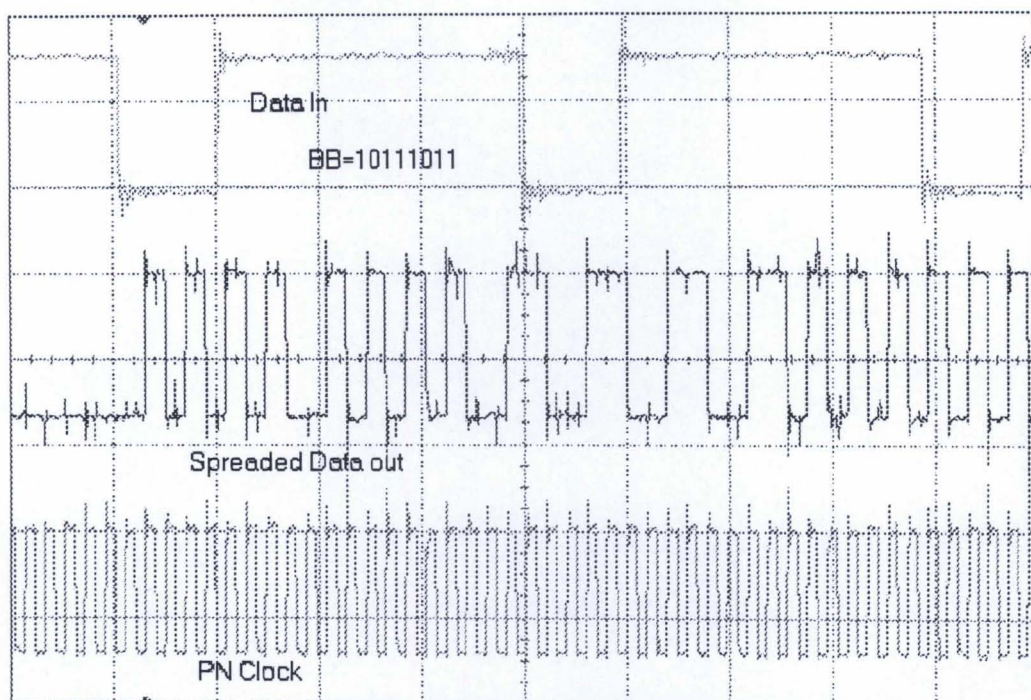
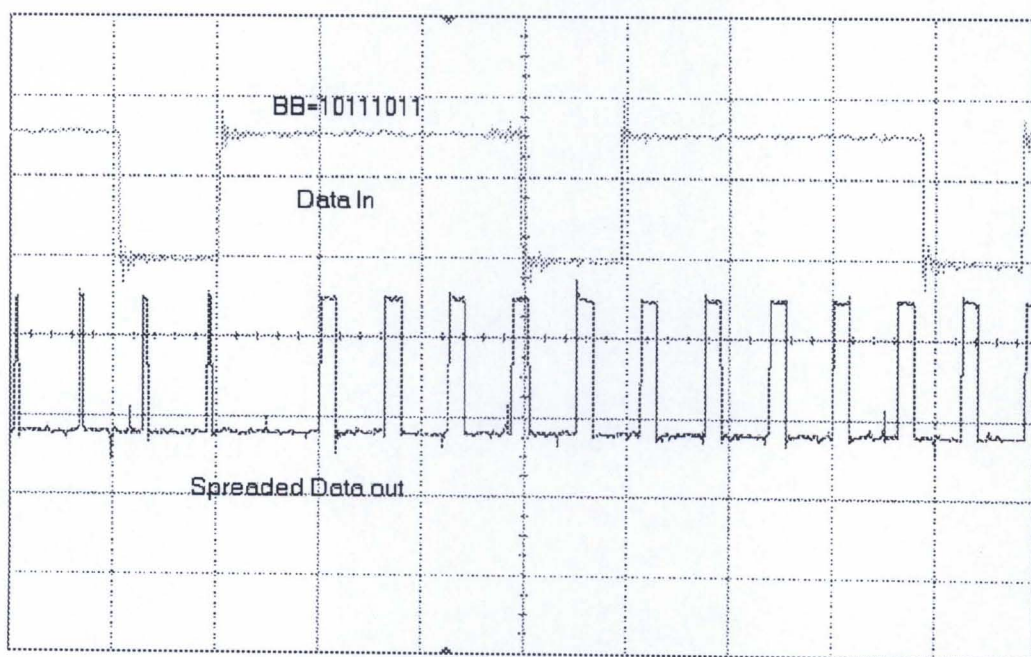


Figure 6.12: Entity diagram for the spreader

Figure 6.12 shows the entity diagram of the spreader used in the design to implement spreading of the incoming base band (64 Kbps) data. A simple multiplier circuit can be used to spread the incoming data stream. The spreader makes use of several clocks and synchronization signals to achieve the correct spreading process. The code stream signal will be in a high state during the spreading process, otherwise low. The frame synchronization signals that are used in this block are discussed in Section 6.3. A reset signal is used in the design to reset the entity. When low, it indicates that the entity needs to enter a reset state. A storage area or database is included in the spreader entity, which provides the PN sequences for spreading. This database is fairly dynamic in that its contents can be programmed from the DSP. In order to provide the designer with a high degree of flexibility, a separate pin is included for the code stream in the entity. For future development of this system one can design a long PN code or Gold code in the PC and send this to the system over the DSP card. The codes are stored in a reconfigurable logic manner in the database that allows for easy access. The spreading process ties in closely with the fact that the output is a multi-level signal. The PN sequences are stored in the database as a mono-polar signal (0,1). It is treated, as a non-return to zero (NRZ) stream, that is 0 will be considered as -1 and 1 as 1. The same is the case with the data stream which, when multiplied with the relevant code, will also produce a NRZ stream.

Figure 6.13 shows a measurement of the spread data with the PN clock measured at the output of the spreader. Figure 6.14 shows the same user data spread with another code generated from the PN database in the spreader. The duration of a PN sequence is one slot. In the output stage of the spreader, spread data is accompanied by its relevant clock, which provides the transmitter filter with necessary timing for its filtering operation.

**Figure 6.13: PN clock and spread signal using code 1****Figure 6.14: Spread signal using Code 2**

An alternative method for spreading is to use Walsh codes; the PN code database can be used for this purpose. The despreading is carried out by a similar process in the

receiver. Once the data has been spread, it is essential to subject it to a filtering process before transmission.

6.6 Filtering (Transmitter and receiver)

The transmitter and receiver filter used in this design are from Ellis, [114] since this work builds on developments of other students involved in the Centre of Excellence.

Raised cosine filters are used for shaping pulses for transmission through digital channels to prevent intersymbol interference [99].

The raised cosine frequency is characterized by [100]:

$$P(f) = \begin{cases} T, & 0 \leq |f| \leq (1-\alpha)/2T \\ \frac{T}{2} \left[1 + \cos \frac{\pi T}{\alpha} \left(|f| - \frac{1-\alpha}{2T} \right) \right], & \frac{1-\alpha}{2T} \leq |f| \leq \frac{1+\alpha}{2T} \\ 0, & |f| > \frac{1+\alpha}{2T} \end{cases} \quad \text{-----6(1)}$$

where α is the roll-off factor, which ranges from $0 \leq \alpha \leq 1$. The bandwidth occupied by the signal beyond the Nyquist frequency $\frac{1}{2T}$ is called the excess bandwidth. The pulse $p(t)$, having the raised cosine spectrum, is:

$$\begin{aligned} p(t) &= \left[\frac{\sin \pi t/T}{\pi t/T} \right] \left[\frac{\cos(\pi \alpha t/T)}{1 - 4\alpha^2 t^2/T^2} \right] \\ &= \text{sinc}(t/T) \left[\frac{\cos(\pi \alpha t/T)}{1 - 4\alpha^2 t^2/T^2} \right] \end{aligned} \quad \text{-----6(2)}$$

Figure 6.15 shows the simulated results (using MATLAB) of the time domain response of the raised cosine filter with $\alpha = 0.3$. WCDMA systems use the raised cosine filter with roll-off factor (α) of 0.22 (refer Table: 2.2). This parameter ($\alpha = 0.3$) was considered as the proposed parameter for this WCDMA system as, at the time of

implementing the system model, no standard value of α for WCDMA had been identified and $\alpha = 0.3$ was being used by a number of researchers.

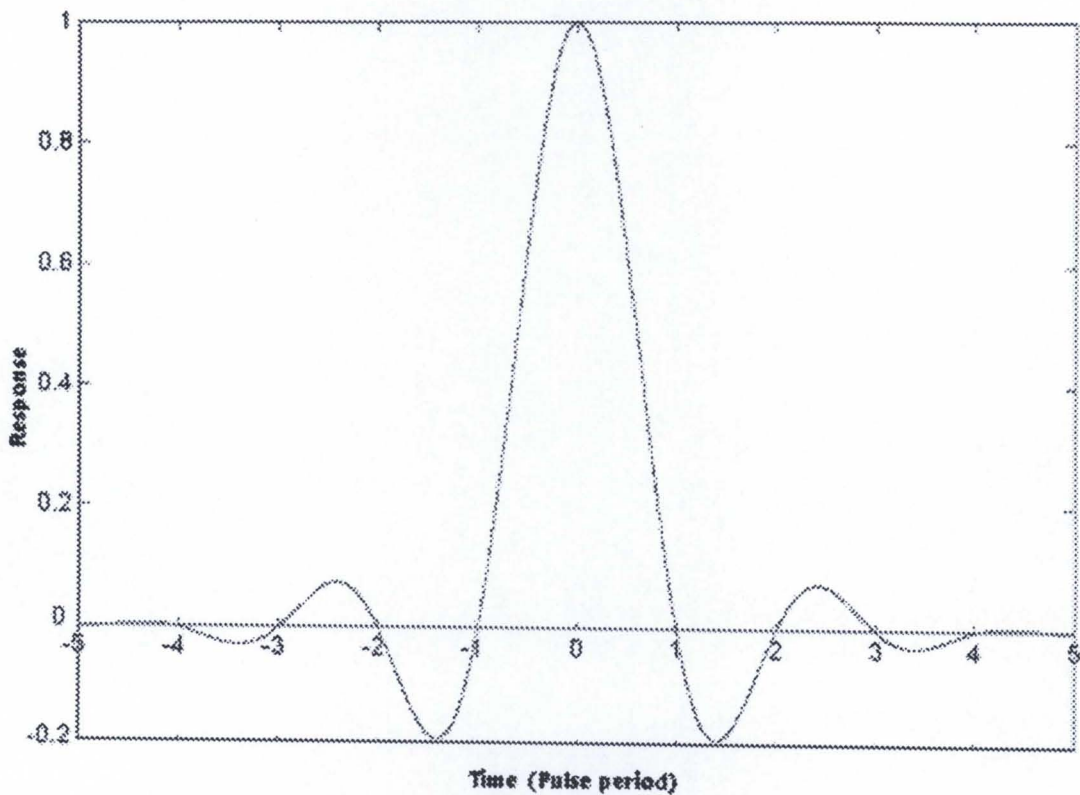


Figure 6.15: Time domain response of the raised cosine filter with $\alpha = 0.3$

The measured filter time domain response from the CFPGA is shown in Figure 6.16.

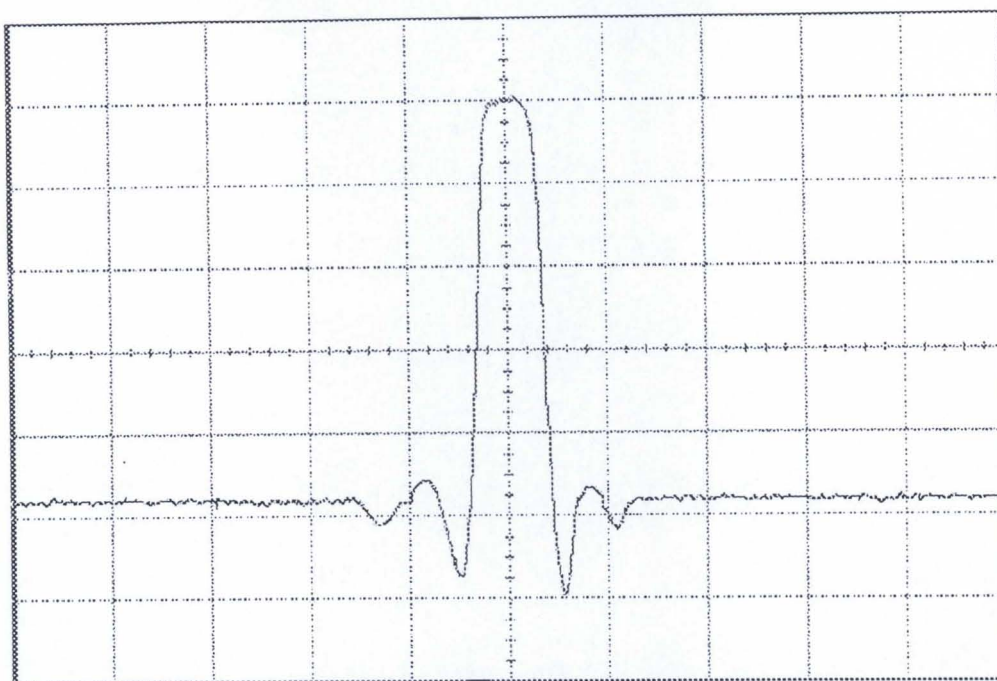


Figure 6.16: Measured time domain response graph

Since the shaped data will normally be transmitted over a real channel, it will undergo some form of distortion. This distortion may include Additive White Gaussian Noise (AWGN) and Rayleigh fading. Matched filtering is an optimum method of overcoming the effects of white noise. It is feasible to design the transmitter filter in such a manner that the receiver filter is aware of the received signal characteristics. Once the data has been received, it is necessary to pass it through some form of linear filter so as to remove as much of the channel distortion as possible. If the signal characteristics are known, then it is possible to design a filter such that the signal to noise ratio is maximized. However, this requires some prior knowledge of the parameters of the transmitted signal. This is best achieved by processing the signal before it is transmitted. In this manner, the receiver can estimate the nature of the received signal quite accurately. From this perspective, it is imperative that the receiver filter is designed in conjunction with the transmitter filter.

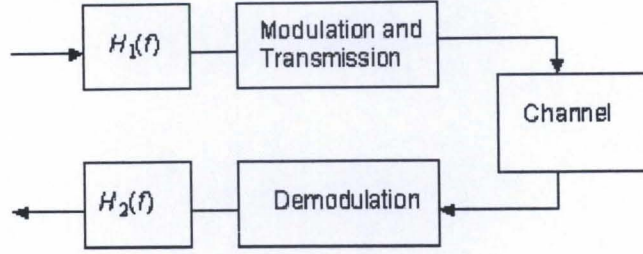


Figure 6.17: The Matched Filter communication path [114]

Figure 6.17 shows the matched filter communication path, where $H_1(f)$ is the transmitter filter function and $H_2(f)$ is the receiver function. The VHDL codes used to design the transmitter and receiver filter are from [114]. A detailed description of these filter designs can be found in [113-114]. For continuity a few points are mentioned in this thesis. In terms of the matched filtering process, the transmitter filter will perform one half of the overall raised cosine filtering with a root cosine filter. The realization structure of the Finite Impulse Response (FIR) transmitter filter may be optimized to take advantage of the nature of the input data.

6.6.1 Transmitter filter

The general formula for the FIR convolution is given by:

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \quad \text{-----6(3)}$$

where $h(k)$ are the impulse response curve, N is the number of the coefficients, $x(n-k)$ are delayed samples of the input waveform and $y(n)$ are the filtered samples based on the previous N input samples. As can be seen from the defining equation, there are N multiplications and $N-1$ additions.

Figure 6.18 shows the optimized structure of the transmitter filter using the interpolation method. Once the new symbol event (symbol to be filtered) is loaded (1.024 MHz), the appropriate filter coefficient is loaded by rotating the N filter coefficients to the right at a rate of 8.192 MHz (8 times higher than the spread signal rate).

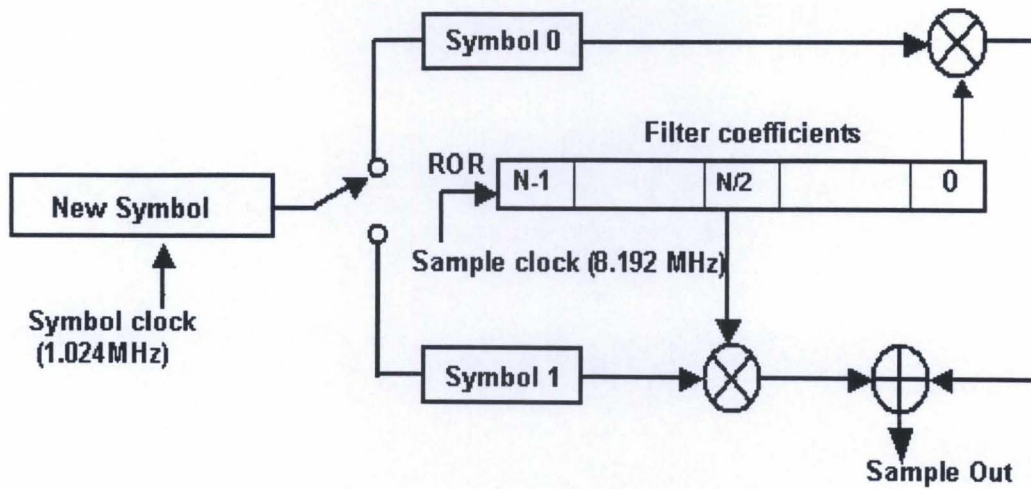


Figure 6.18: Interpolation optimized transmitter filter structure [114]

Since there are 16 filter coefficients, and each symbol needs to be multiplied by each coefficient at least once, a symbol will remain loaded in a symbol register for at least 16 sample clock edges. Figure 6.19 shows the frequency domain response of the transmitter filter measured at the DAC outputs of the software radio. The cut-off frequency of approximately 1.024 MHz meets the system requirement.

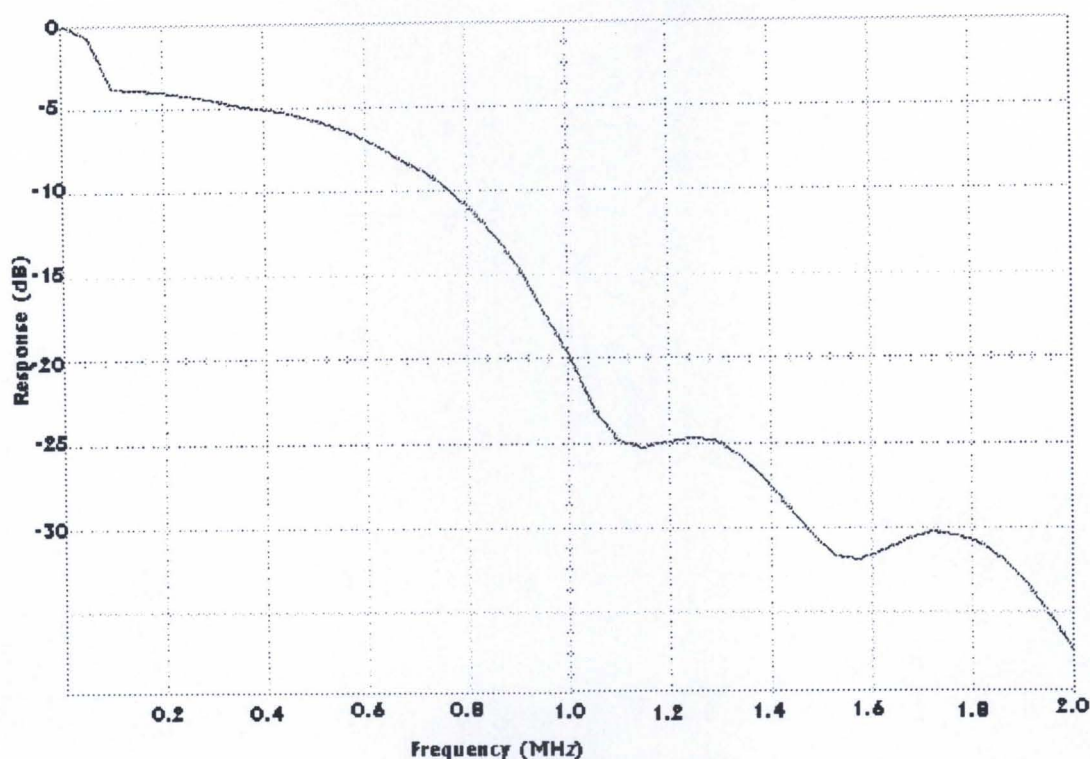


Figure 6.19: Measured filter response (Transmitter)

6.6.2. Receiver filter

In the transmitter filter the convolution occurs at $1/N$ times the sample rate. This is not possible for the receiver filter that convolves the coefficients and samples at the true sample rate. As a result, every input sample is involved in the generation of the output sample in a single cycle. The receiver filter realization is discussed below.

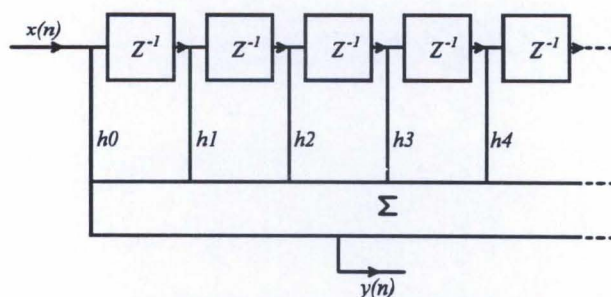


Figure 6.20: Transversal filter implementation [114]

Figure 6.20 shows the structure of the transversal filter, which is easy to realize when implementing the direct FIR equation. The samples are merely delayed using a lengthy

shift register and then multiplied by the coefficients. Figure 6.21 shows the frequency domain response of the transmitter filter measured at the DAC outputs of the software radio.

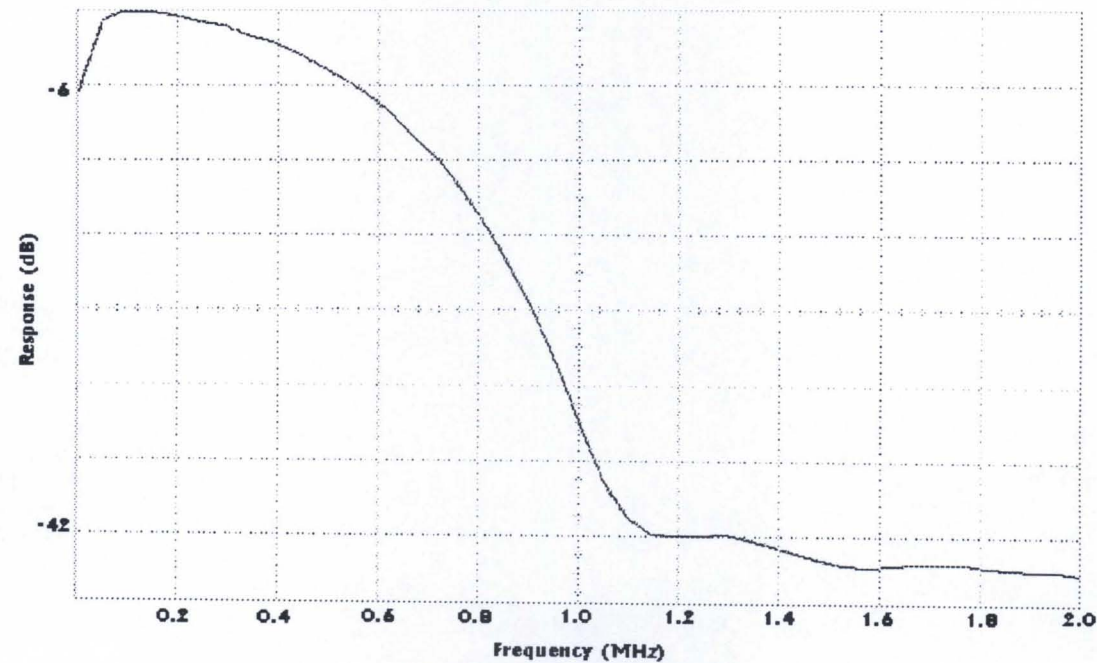


Figure 6.21: Measured filter response (Receiver)

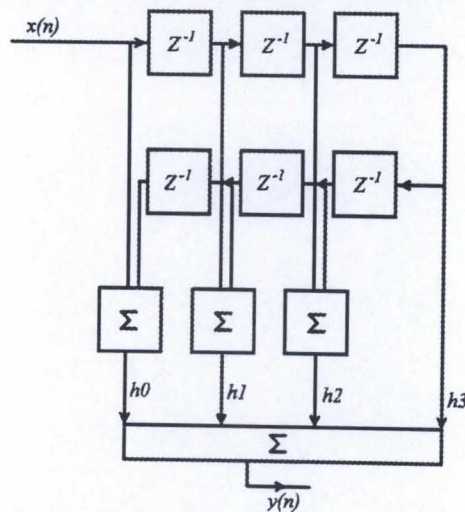


Figure 6.22: Linear phase structure for filter [114]

The structure of the FIR coefficients is such, that they cannot be used directly in the transversal filter. In order to take advantage of the FIR filter coefficients a linear phase structure is suggested as shown in Figure 6.22. This method has only $N/2$

multiplications and N additions compared to the transversal method that requires N multiplications and $N-1$ additions. Vector-based multiply and accumulate operations are fundamentally logic multiplications and can be embodied in a look-up table. A MATLAB function was developed to generate the look-up table data. Figure 6.23 shows the measured filter response at the output of DAC.

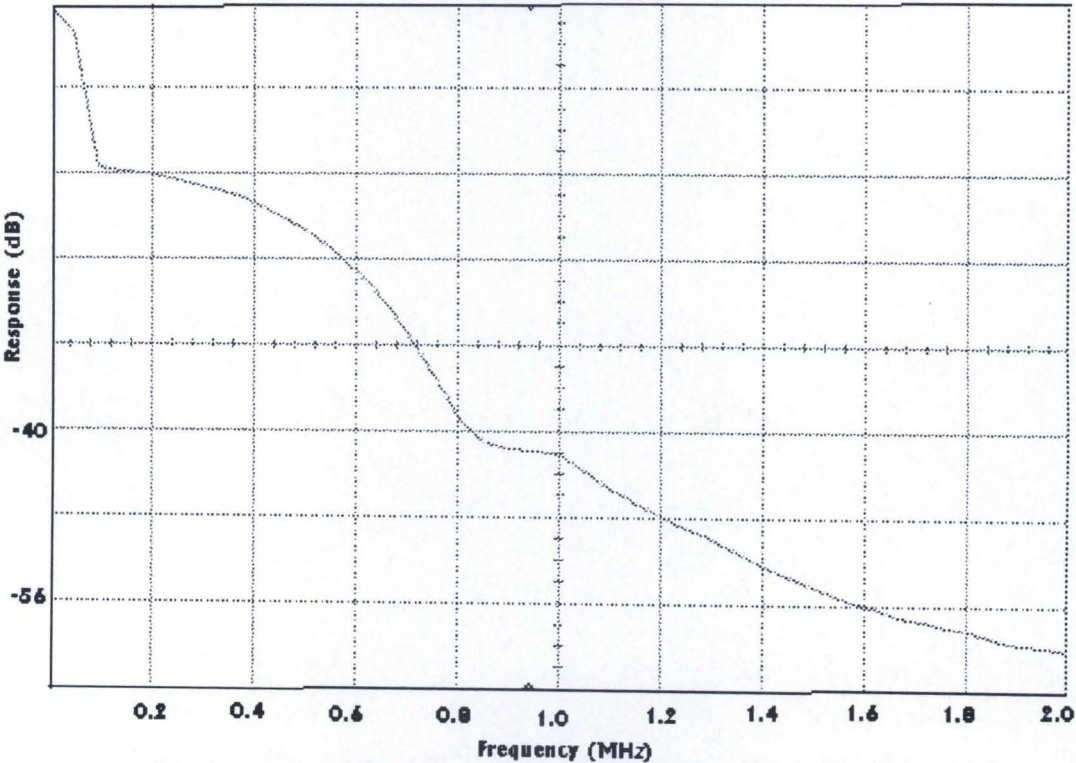


Figure 6.23: Measured filter response for linear phase structure (receiver)

Detailed implementation issues of the transmitter filter and the receiver filter are discussed in [114]. The output of the linear filter is coupled to the sample selection section to find the optimum sample. After finding the optimum sample, the signal is despread with a replica of the PN code used in the transmitter. The despread signal is then fed to the beamforming section, which is discussed in Section 6.8. The filtered data in the transmitter goes through a Rayleigh faded channel with AWGN. These are discussed in Section 6.7.

6.7 Channel

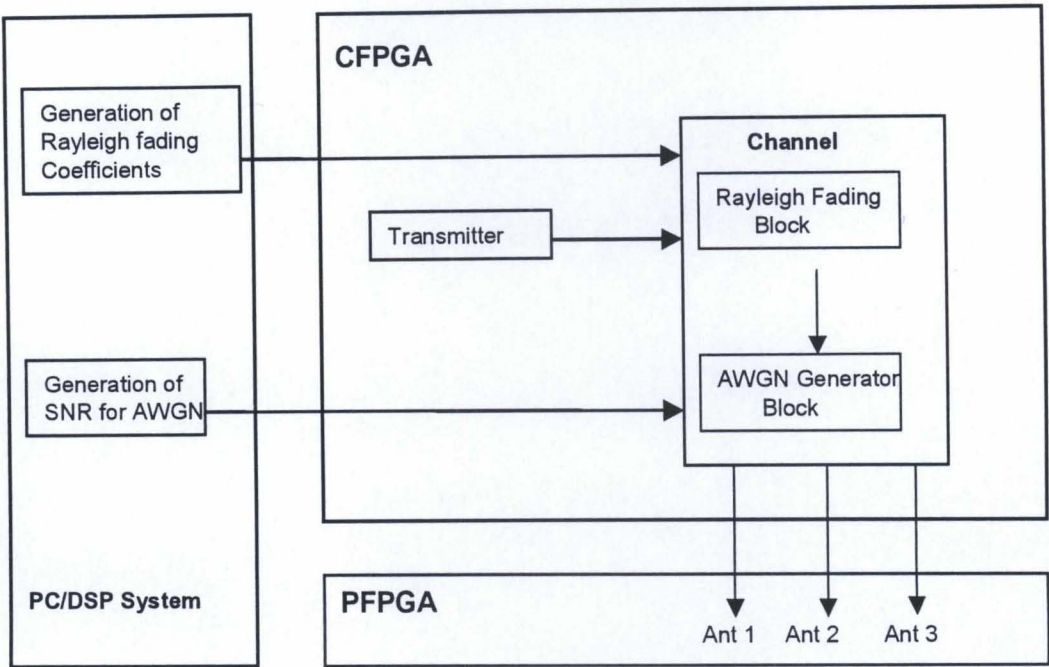


Figure 6.24: Channel block overview

Figure 6.24 depicts how the resources are shared to optimize the channel block in the CFPGA. The complexities involved in the type of fading and the limited FPGA resources point to the need for resource sharing. This section will discuss the reproduction of two channel distortions namely; AWGN and uncorrelated Rayleigh fading. These two channel distortion factors are used in the software radio to distort the relevant signals and provide an estimate of the BER of the system. The Rayleigh fading coefficients, which are generated in the PC and stored in DSP memory locations, are sent to the software radio on each transmit interrupt as shown in Figure 6.24. These are then multiplied with the relevant signal in the FPGA to produce a Rayleigh faded signal. The generation of AWGN samples in the FPGA is less complex than Rayleigh fading. However the calculation for converting the desired SNR to a coefficient, which can be used by the FPGA is performed in the DSP to reduce implementation complexity.

6.7.1: Rayleigh fading

Consider a mobile radio channel with multi-path components. The transmitted band pass signal can be expressed as [100]:

$$s(t) = \text{Re} \left[\tilde{s}(t) \exp(j2\pi f_c t) \right] \quad \text{-----6(4)}$$

where $\tilde{s}(t)$ is the complex envelope of $s(t)$ and f_c is the carrier frequency. The impulse response of the channel is delay dependent due to the multipath effects and therefore a time-varying function. The impulse response of the channel is expressed as:

$$h(\tau; t) = \text{Re} \left[\tilde{h}(\tau; t) \exp(j2\pi f_c t) \right] \quad \text{-----6(5)}$$

where $\tilde{h}(\tau; t)$ is the complex impulse response of the channel, which is the input delay-spread function of the channel and τ is a delay variable. The complex envelope of the channel output is defined by the convolution integral:

$$s_0(t) = \frac{1}{2} \int_{-\infty}^{\infty} \tilde{s}(t - \tau) \tilde{h}(\tau; t) d\tau \quad \text{-----6(6)}$$

where the scaling factor $\frac{1}{2}$ is the result of the complex notation.

For analytical purposes, the delay-spread function $\tilde{h}(\tau; t)$ may be modeled as a zero-mean complex-valued Gaussian process. Then at any time t the envelope $|\tilde{h}(\tau; t)|$ is

Rayleigh distributed and the channel is referred to as a Rayleigh fading channel [100].

The Rayleigh probability density function is given as [99]:

$$f_V(v) = \begin{cases} \frac{v}{\sigma^2} e^{-\frac{v^2}{2\sigma^2}}, & v \geq 0 \\ 0, & v < 0 \end{cases} \quad \text{-----6(7)}$$

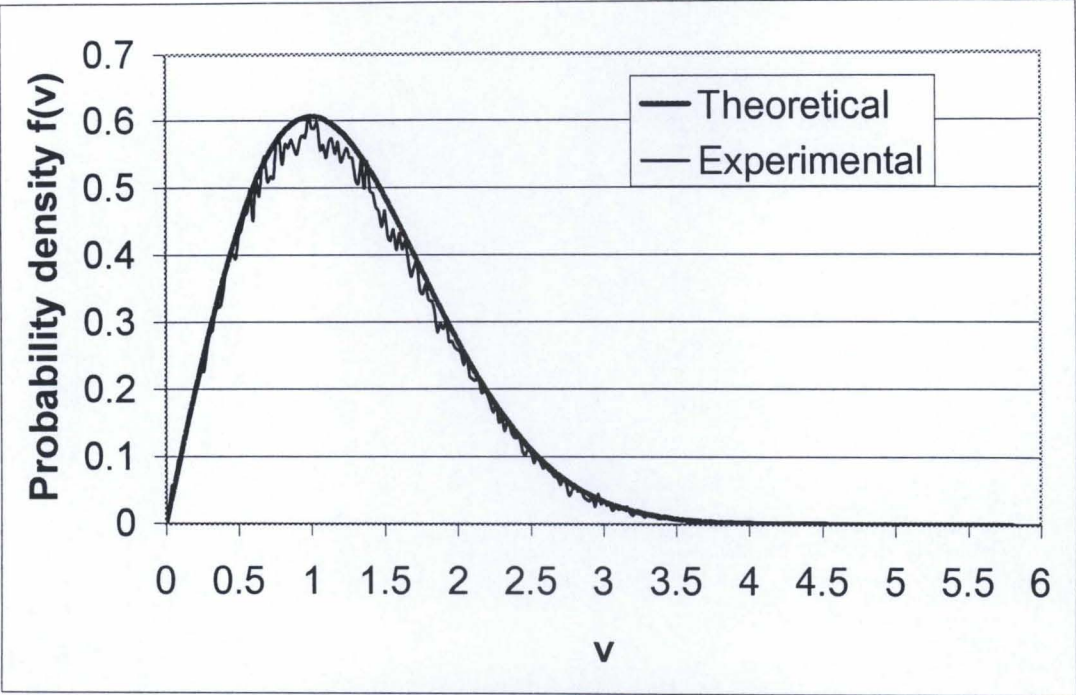


Figure 6.25: Rayleigh fading distribution

Figure 6.25 shows the Rayleigh fading distribution for both the theoretical and practical results generated in C++. The graph presents the actual density function of $f(v)$ data generated for the case of 100000 samples. There is a close agreement between the theoretical and practical curve. Both the uniform distribution and the Gaussian (normal) distribution are used to generate practical Rayleigh fading coefficients. Two Gaussian random variable samples are required to generate the uncorrelated Rayleigh random variable. This can be generated using equation 6.8.

$$R_r = \sqrt{N_1^2 + N_2^2} \tag{6.8}$$

where N_1 and N_2 are Gaussian random variables.

The DSP card was used to generate the Rayleigh fading samples in order to implement the Rayleigh fading in the software radio. The generated samples are stored in the DSP as a long byte-valued array, because the DSP is not capable of producing a new sample from the random variable space on every byte that is transmitted. So, on each transmission interrupt the Rayleigh sample is read from the array and transmitted to the software radio. The DSP loops back to the beginning when it reaches the end of the

array, which generates the required stream of Rayleigh samples. These samples need to be packed to 8-bit values before sending them to the software radio.

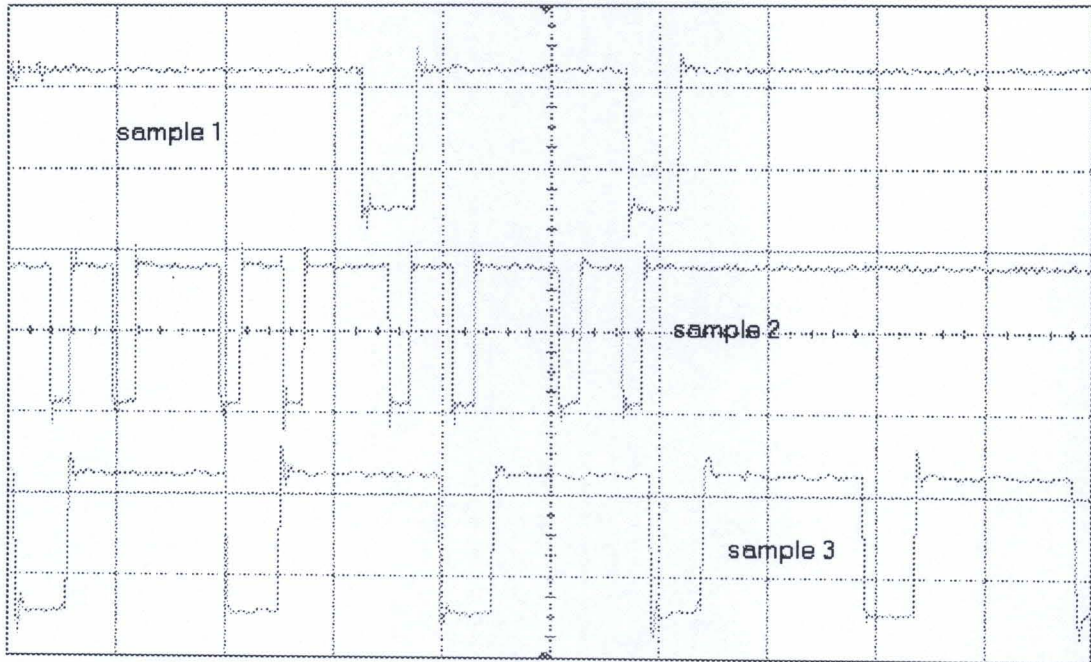


Figure 6.26: Measured Rayleigh samples received from DSP

Figure 6.26 shows the generated Rayleigh sample received from the DSP. These samples were packed into 8-bit values and used to multiply the main transmitted signal to generate the effect of fading. In order to achieve this the values calculated in the DSP have to be correspondingly scaled. Choosing a feasible scaling factor of 64 to correspond to a maximum realistic value attained in the distribution, [i.e; $(4 \times 64 = 256)$]. The effect of scaling is removed by shifting the post-multiplication storage register right by 6 bits after the multiplication of the Rayleigh sample by the signal. The transfer byte rate of the samples is 256 KBytes/s, because the serial link rate is set to be 2.048Mb/s. Thus the Rayleigh fading coefficient will change on every 4th symbol or 32 samples per symbol, with a sample rate of 1.024MS/s. Figure 6.26 depicts different Rayleigh samples from the array in the DSP. Figures 6.27 and 6.28 illustrate the effect of Rayleigh fading on the transmitted signal measured at the output of the DAC in the software radio.

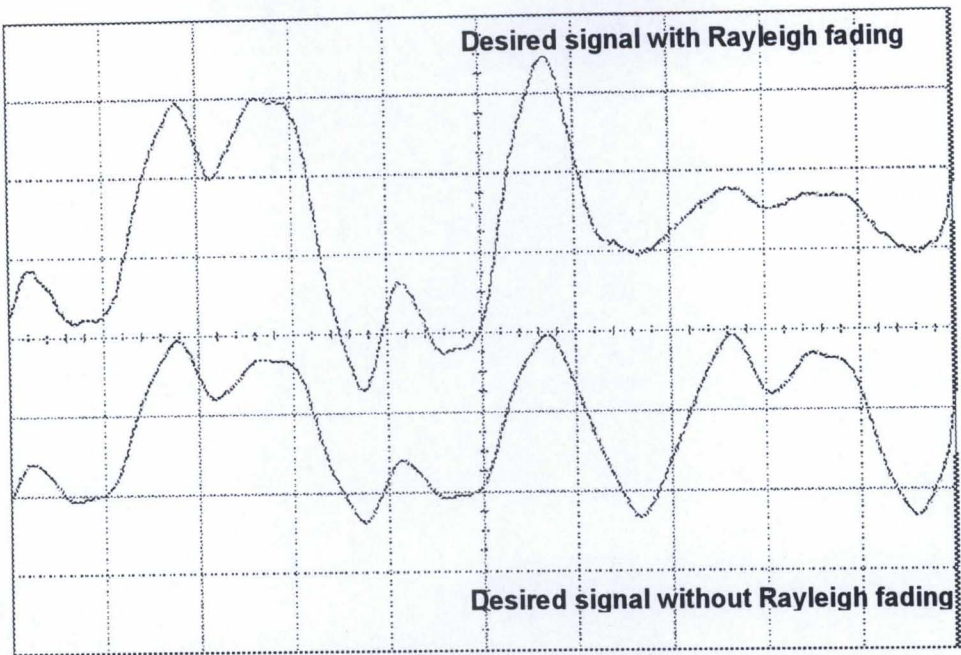


Figure 6.27: Transmitted signal amplified in Rayleigh fading

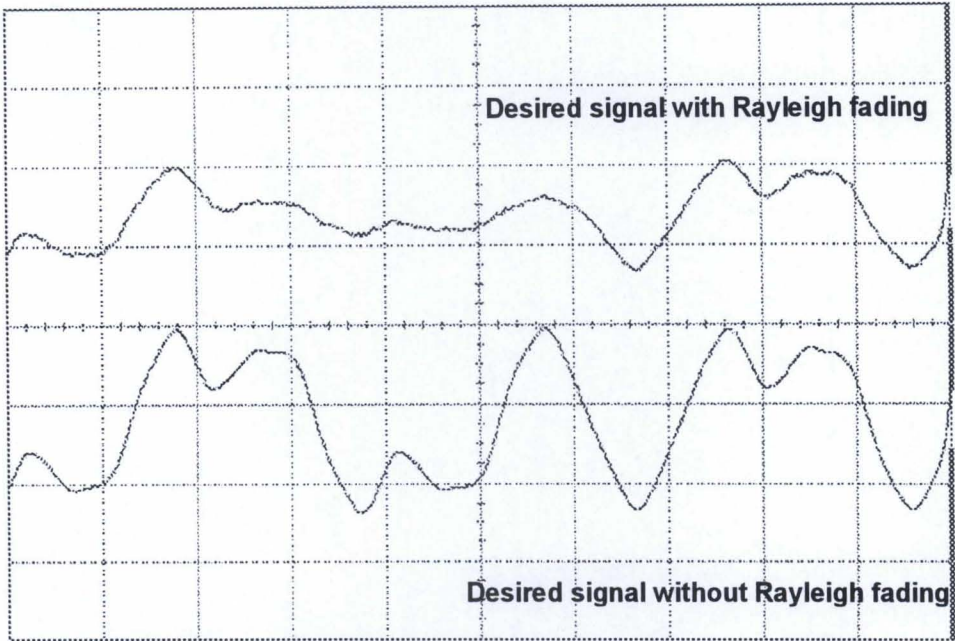


Figure 6.28: Transmitted signal attenuated in Rayleigh fading

These figures (Figures 6.27 & 6.28) demonstrate worst case constructive and destructive signal degradation to a signal transmitted in a Rayleigh fading channel. In practice, the fading varies randomly with time for mobile users and similarity between transmitted and faded signals are small. In this thesis the user has been assumed to be stationary

and the fading depths are thus small which give rise to the similarities of signal shown in Figures 6.27 and 6.28.

6.7.2: AWGN

White noise is a stochastic process that is defined to have a flat power spectral density over the entire frequency range [99]. The AWGN samples are generated in the FPGA and the calculation for converting the desired SNR to coefficient is performed in the DSP due to computation complexity. These parameters are sent to the software radio over the SC-BUS and the generated samples are added to the relevant signal. The mathematical approaches to generate the normal distribution in the FPGA are discussed below from [115].

$$P_r(a \leq x \leq b) = \int_a^b f(x) dx \quad \text{-----6(9)}$$

$$1 = P_r(\alpha \leq x \leq \beta) = \int_{\alpha}^{\beta} f(x) dx \quad \text{-----6(10)}$$

where $[\alpha, \beta]$ is the interval over which $f(x)$ is defined. The density function of uniform distribution over the interval $[0, 1]$ is constant. So

$$1 = P_r(0 \leq x \leq 1) = \int_0^1 c dx = c \quad \text{-----6(11)}$$

Thus the density function of this distribution is $f(x) = 1$

Given a density function $f(x)$ defined over the interval $[\alpha, \beta]$, the mean μ is given by:

$$\mu = \int_{\alpha}^{\beta} x f(x) dx \quad \text{-----6(12)}$$

and the standard deviation σ is given by:

$$\sigma^2 = \int_{\alpha}^{\beta} (x - \mu)^2 f(x) dx \quad \text{-----6(13)}$$

Using these formulas, one can calculate the mean and standard deviation of the uniform distribution over $[0, 1]$:

$$\mu = \frac{1}{2} \text{ and } \sigma = \sqrt{1/12}$$

The normal distribution with mean μ and standard deviation σ is described by the density function:

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}}, \quad -\infty \leq x \leq \infty \quad \text{-----6(14)}$$

Approximation, using the central limiting theorem, states that if x_1, x_2, \dots, x_n are independent random numbers chosen from a distribution $f(x)$ with mean μ and standard deviation σ , then the distribution of:

$$y = \frac{\frac{1}{n} \sum_{i=1}^n x_i - \mu}{\sigma} \sqrt{n} \quad \text{-----6(15)}$$

approaches the normal distribution with mean 0 and standard deviation 1. Substituting the value of σ and μ gives:

$$y = \frac{\frac{1}{n} \sum_{i=1}^n x_i - \frac{1}{2}}{\sqrt{1/12}} \sqrt{n} = \left(\frac{1}{n} \sum_{i=1}^n x_i - \frac{1}{2} \right) \sqrt{12n} \quad \text{-----6(16)}$$

which is an approximation of the normal distribution with mean 0 and standard deviation 1. The normal deviation with mean M and standard deviation S , can be obtained using:

$$y = M + S \left(\frac{1}{n} \sum_{i=1}^n x_i - \frac{1}{2} \right) \sqrt{12n} \quad \text{-----6(17)}$$

Since $n = 12$ is probably large enough for most applications, this can be simplified to

$$y = M + S \left[\frac{1}{n} \sum_{i=1}^{12} x_i - 6 \right] \quad \text{-----6(18)}$$

This equation can be optimized using simple addition, multiplication, and shifting (division) functions. As can be seen from the equation 6 (18), the equation is directly

proportional to n and can be as small as six for a sufficiently accurate and high-speed normal distribution generator. This means that with the use of this small number of samples from a uniformly distributed sample space, further samples can be obtained from the normal distribution.

In order to generate the random bits for generating AWGN samples, a primitive polynomial generator can be used, with the following equation of order n=31:

$$x^{31} + x^3 + x^0$$
-----6(19)

If the generating polynomial is correct and if the starting seed is non-zero, then this generator is guaranteed to be of maximal length. This means it will repeat only after 2^{n-1} iterations.

Figure 6.29 shows the block diagram of the uniform random generator. The bits are individually XOR'ed with the MSB and the register is rotated once to the left.

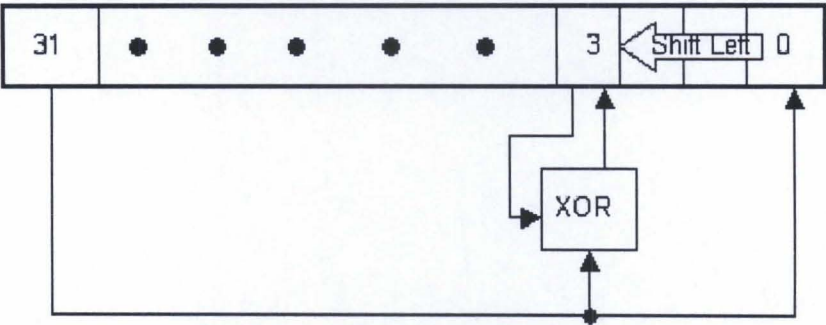


Figure 6.29: Feedback method for Uniform Random Generator

The procedure is repeated n times (n being the width of the register), generating a new sample from the uniform distribution with range $(0,2^n - 1)$. For example (31,3,0):

$$r_3=r_3 \text{ XOR } r_{31}$$
$$r_0=r_{31}$$
-----6(20)

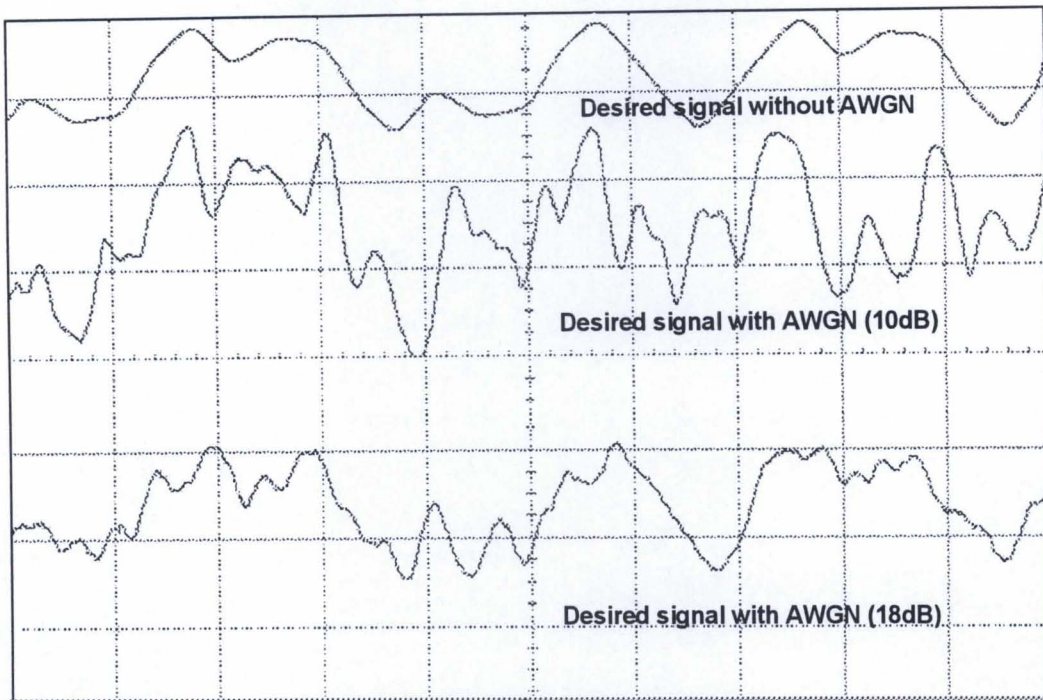


Figure 6.30: Measured AWGN channel

Figure 6.30 shows the measured transmitted signal in an AWGN channel. The figure depicts the effect of the AWGN generator. The top trace is the desired transmitted signal without AWGN and the middle and bottom traces are the same transmitted signal with AWGN at a SNR of 10 dB and 18 dB, respectively. The noise samples of a specific SNR are added to the desired signal to optimize the effect of the AWGN channel. The traces are captured using an Agilent oscilloscope. The oscilloscope has mathematical features such as addition, division and RMS signal value. This was useful in validating the SNR levels produced.

From the measured results, the second stage of the implementation was also successful. The third and the last stage of the implementation is the receiver with three antennas and three multipaths. The realization of the antenna arrays is discussed in Section 6.8.

6.8 Receiver

As discussed in Section 6.2, due to the limited capacity in the FPGA, some of the functions were moved from the FPGA to the PC. A fair compromise for this problem is

to avoid the mobility of the desired user so that the weights can be calculated manually and stored in the DSP memory and fed to the multipliers used in the beamformers. In this manner the channel estimation and error-forming blocks used for the weight calculations can be avoided. Channel estimation estimates multipath delay and complex tap coefficients. Manual calculation of delays reduces the need of channel estimation. This reduces the complexity of the receiver. Figure 6.31 shows the functional blocks of the receiver after eliminating the channel estimation and the error forming function in the PFPGA. As shown in the Figure 6.31, the despread signals from the matched filter are fed to the appropriate multipliers for beamforming. The output signals are equal gain combined in the RAKE combiner and the desired signal is fed to the symbol decision block to extract the user data. The calculations of the appropriate weights ($w_{11}, w_{12}, \dots, w_{33}$) are discussed later in this section.

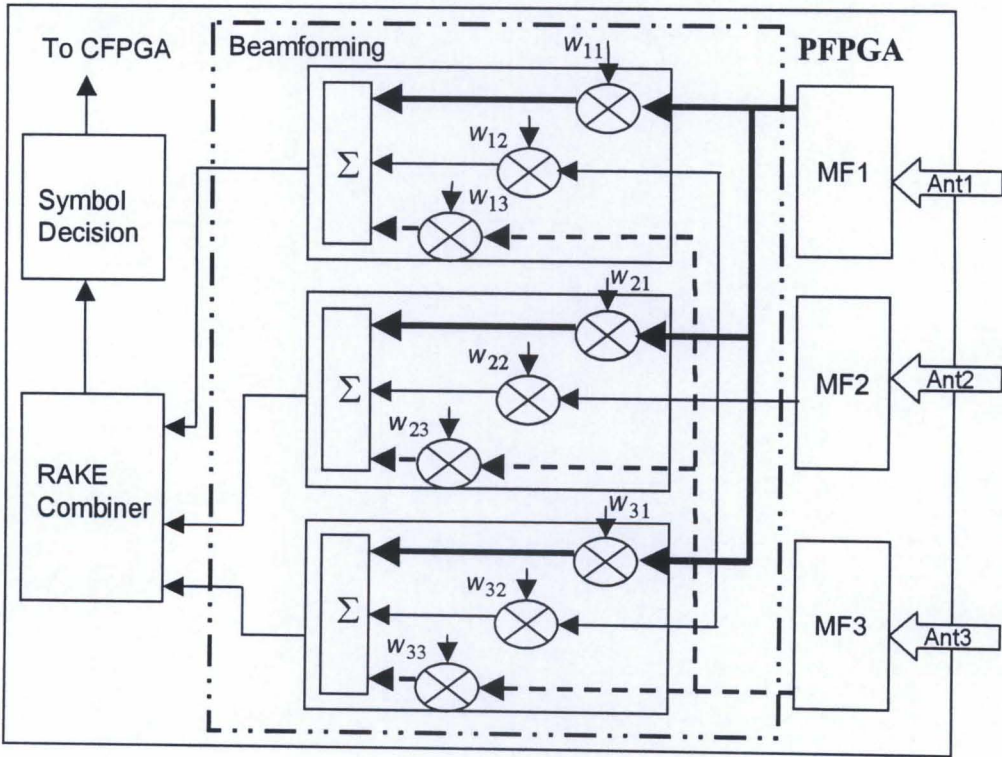


Figure 6.31: Functional blocks of the receiver

Figure 6.32 depicts the realization of antenna array elements. D is the total delay (due to multipath, filters etc) and d is considered as the delay introduced to compensate for the spacing between the elements.

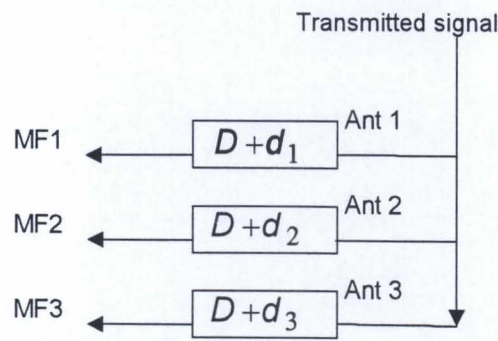


Figure 6.32: Structure of antenna realized in PFBGA

The desired user is assumed to be stationary for simplicity. The spacing between the two antenna elements is considered to be half a wavelength. One direct path and two reflected paths were considered in the design. An approximation of a patch antenna radiation pattern is used in the design. Figure 6.33 depicts the propagation path scenario.

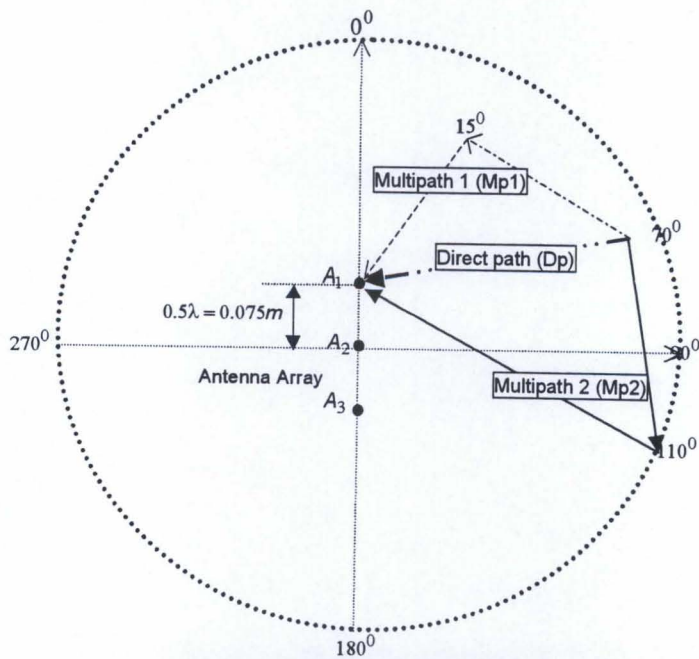


Figure 6.33: Multipath propagation model

From Figure 6.33 one seen that the angle of arrival of the direct path of the desired user signal is 70° and the reflected paths are 15° and 110° respectively

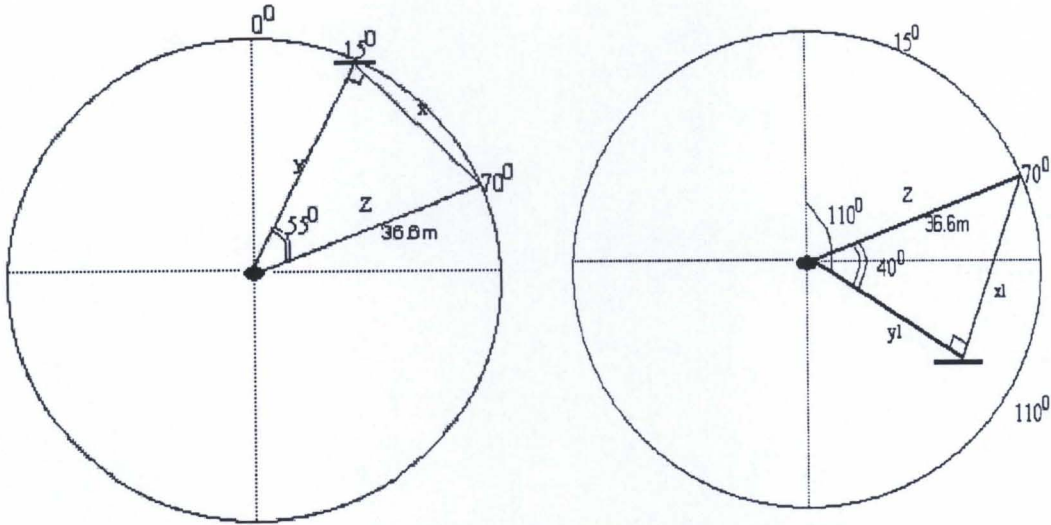


Figure 6.34: Angle of arrival of reflected path

Figure 6.34 shows the angle of arrival of the reflected paths. The distance dependent path loss and time delay of each resolvable path are determined from the propagation distance between the desired user and the antenna via large reflectors. In the simulation model discussed in Chapter 4, the scatterers are assumed to surround the mobile station at distance r (scattering radius). It was assumed that r is small enough to prevent resolution into discrete paths, so N scattered waves arrive at the base station within 1 chip time delay and can be resolved by the receiver-matched filter. Since the chip time used in the simulation is $0.244\mu\text{s}$ and the corresponding propagation distance is 73.2 m ; so r was assumed to be 36.6 m . So for simplicity in the design, the direct path distance is assumed to be 36.6 meters ($1/2$ chip time distance- ($0.122\mu\text{sec}$)). Practically this distance is small and possibly unrealistic but will suffice in demonstrating system performance.

From the angle of arrival and the direct path distance, the propagation delay can be calculated. The calculations of the multipath delay (D) and the delay (d) introduced to optimize the antenna arrays are discussed in Appendix A-6. Figure 6.35 shows the

element pattern, array factor, and total pattern respectively of the patch antenna with 0° phase shift. The total array pattern is obtained by multiplying the pattern of the single element by that of the array factor. The theoretical concepts and design of the antenna are discussed in [27].

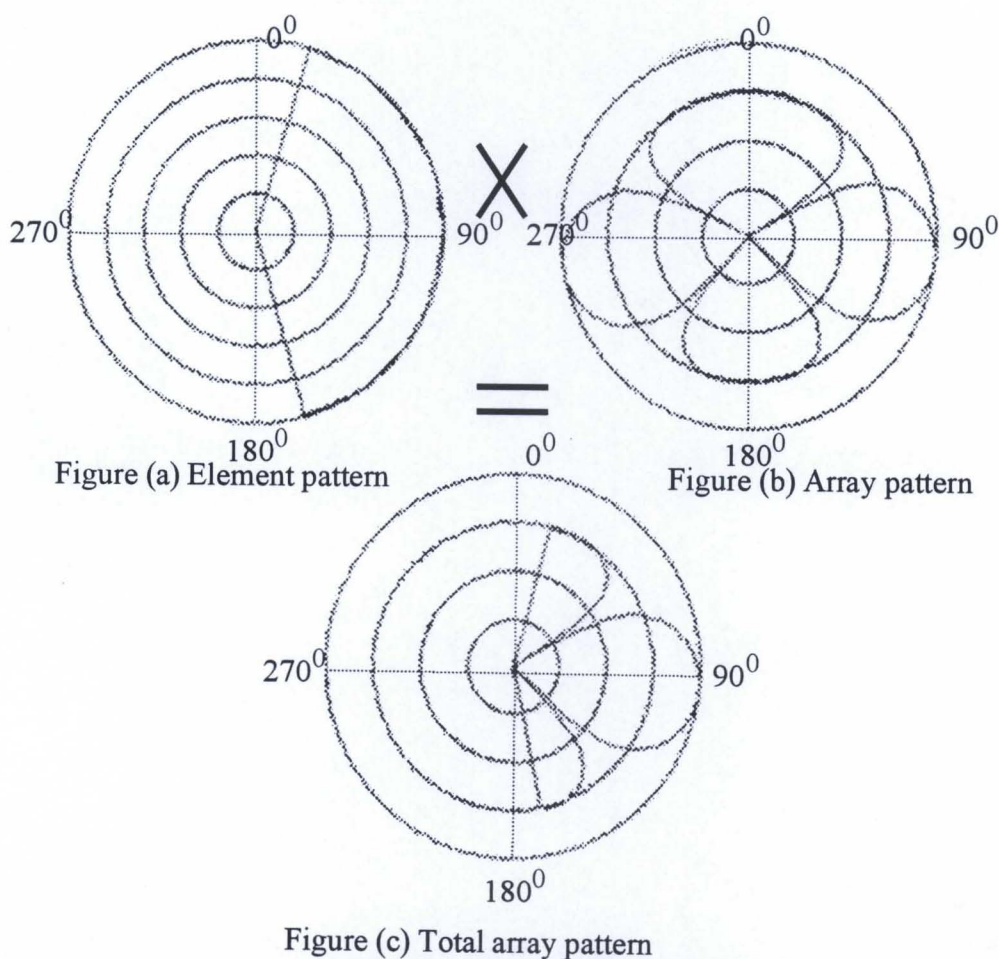


Figure 6.35: Patch antenna array pattern

In the receiver design complex multipliers were used to multiply the weights to form the desired beam for each path. So the number of paths will linearly increase with the number of beamformers. Since the users are stationary the weights can be computed manually and multiplied with each path received in the antenna. The implementation of a complex multiplier consumes most of the logic cells in the PFGPA. As mentioned the angle of arrival of the direct and the reflected paths are 70° , 15° and 110° respectively. In order to track the three paths three different weights are required. The antenna beam

can be steered towards the direct path and the two reflected paths, so that the maximum gain can be obtained. A -60° phase shift is required to track or steer the beam towards the direct path (that is at 70°) or desired user. The field patterns of the patch antenna array at -60° phase shift is obtained from simulation as shown in Figure 6.36 below . The element patterns are the same in all cases.

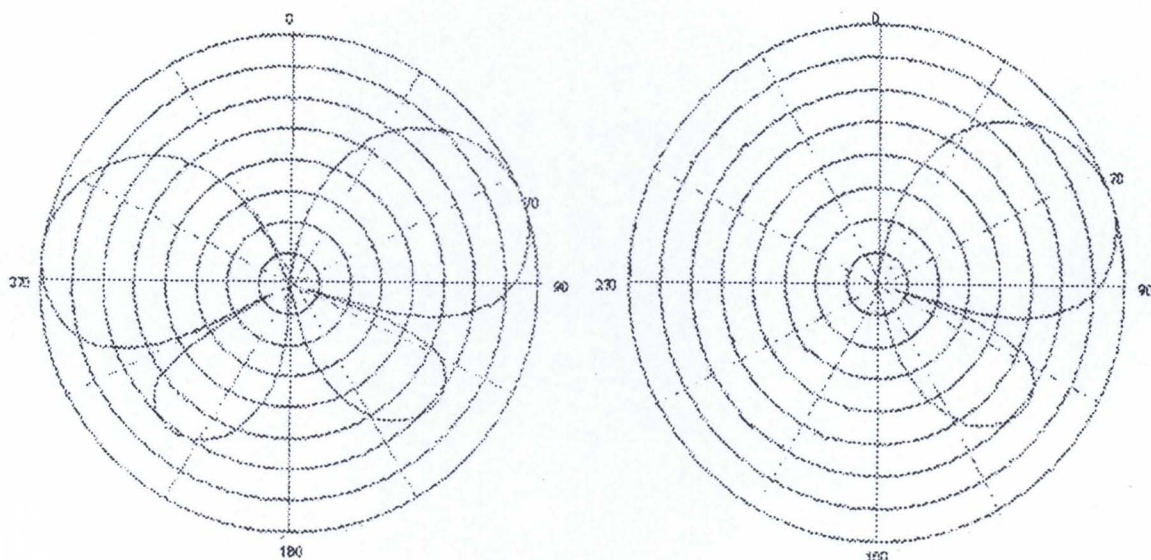


Figure 6.36: Array and total array pattern at -60° phase shift

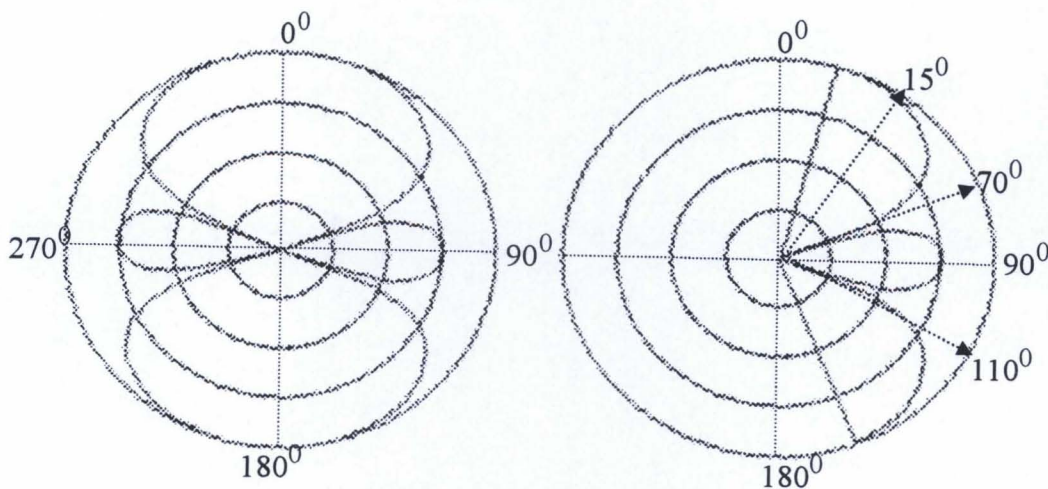


Figure 6.37: Patch antenna pattern at -175° phase shift

The antenna beam is steered towards the second path arriving at angle 15° simultaneously steering the direct path (70°) and third path (110°) towards the null. A phase shift of 65° is introduced to track the third path. The simulated array and total pattern for the third path are shown in Figure 6.38.

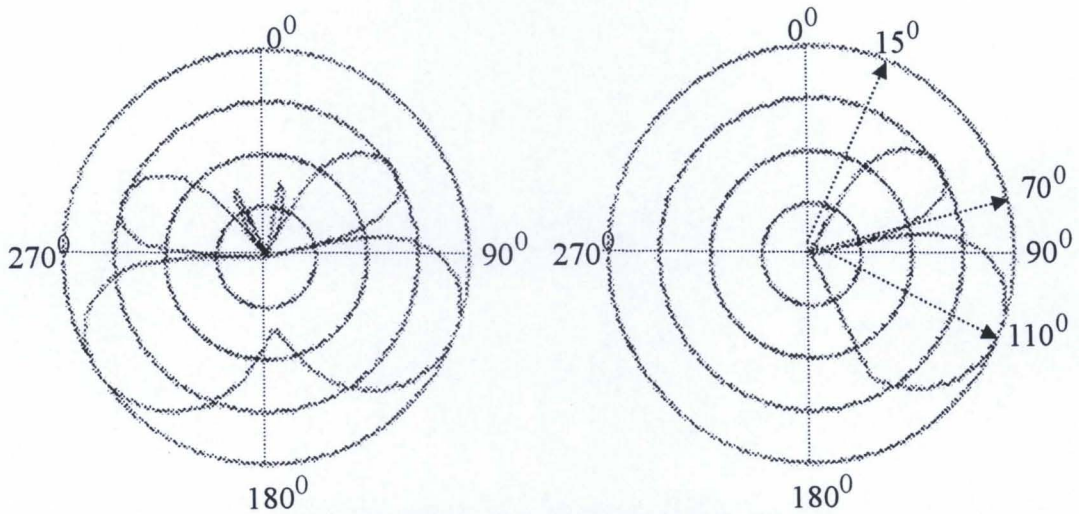


Figure 6.38: Patch antenna pattern at 65° phase shift

The radiation pattern for the different phase shifts demonstrates beam steering in different directions. These results are used to calculate the different weights used for different paths to form a desired beam.

The next block in the system is the receiver filter (Figure 6.10), which has already been presented along with the transmitter filter (Section 6.6). Figure 6.39 shows the measured signal at the output of the receiver filter. These signals are measured at the output of the filter with and without AWGN at different SNRs. The first and third traces represent the signal without AWGN (ideal signal). The second and the fourth traces are with the AWGN of a specific value with SNR of 18dB and 10 dB respectively.

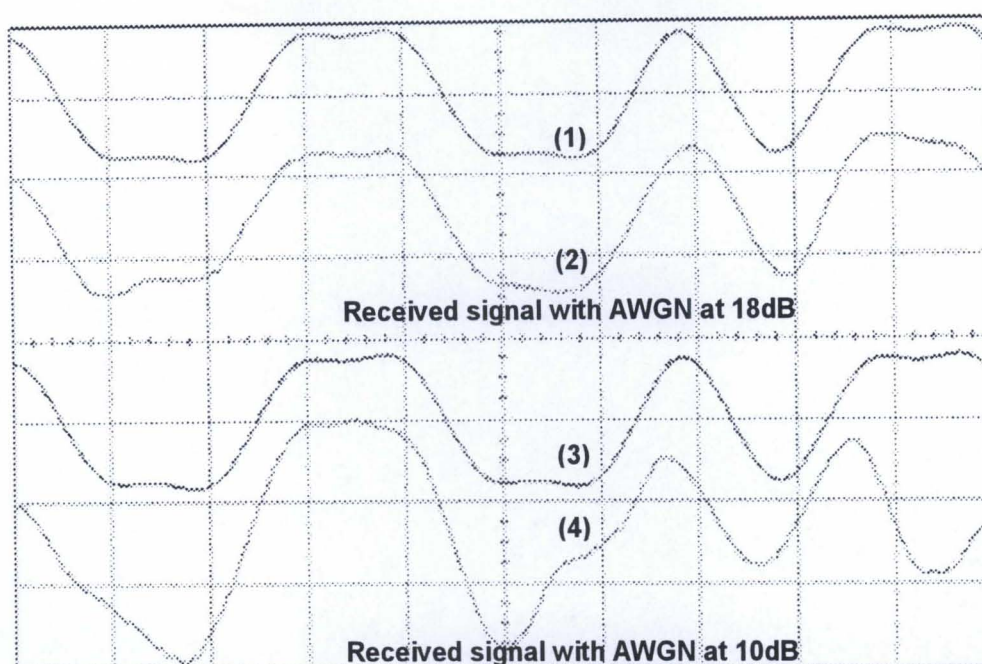


Figure 6.39: Measured signal at the output of the filter

The received signals are despread with a replica of the PN sequence used in the transmitter and coupled to the corresponding beamforming block for beamforming. The outputs of each beamformer are equal gain combined in the RAKE combiner to form the desired output. The receiver structure and the evaluated results discussed in Chapter 4 used channel estimation for maximal ratio combining in the RAKE combiner. Equal gain combining in the RAKE combiner with the appropriate delays is implemented due to the absence of the channel estimation function in the design. The signals after the symbol decision are reordered and packed in bytes and then fed to the CFPGA. In the CFPGA an error counter block is designed to compare the output and input data for error calculations. The error counter counts the number of bits that it processes, in conjunction with the erroneous bits. These bit counts and the error bit counts are send to the DSP/PC layer to compute the bit error rate.

6.9 Evaluation of the implemented receiver

To evaluate the performance of the implemented receiver, several simulation interface functions are required. Firstly, it makes use of bi-directional interfaces with the DSP layer in order to set parameters and read back counting variables. These counting variables count the number of bits received, along with the number that are erroneous. Secondly, the simulation interface polls the DSP card at regular intervals to retrieve the necessary data and update the SNR parameters. As discussed in Chapter 5 the HCIL provides a flexible means of interfacing with the DSP system. The DSP layer is responsible for receiving the data from both the PC and the software radio, formatting it correctly and passing it on to the correct layer. The received 32-bit bit count and bit error count from the software radio are formatted and stored in the appropriate memory locations by the DSP. As discussed in Chapter 5 (Section 5.4), the transport element, addressed to this point (memory location) from PC is responsible for retrieving this data from the DSP. The software radio is responsible for sending the bit count and the erroneous bit count to the DSP. The software radio sends the total number of bits and the erroneous bit count in a frame as shown in figure 6.40. The first 26 bits in the frame represent the bit count and next 26 bits in a frame represent the erroneous bit count [114].

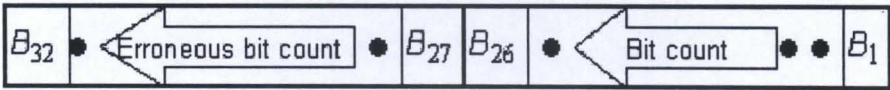


Figure 6.40: Structure of the error count frame

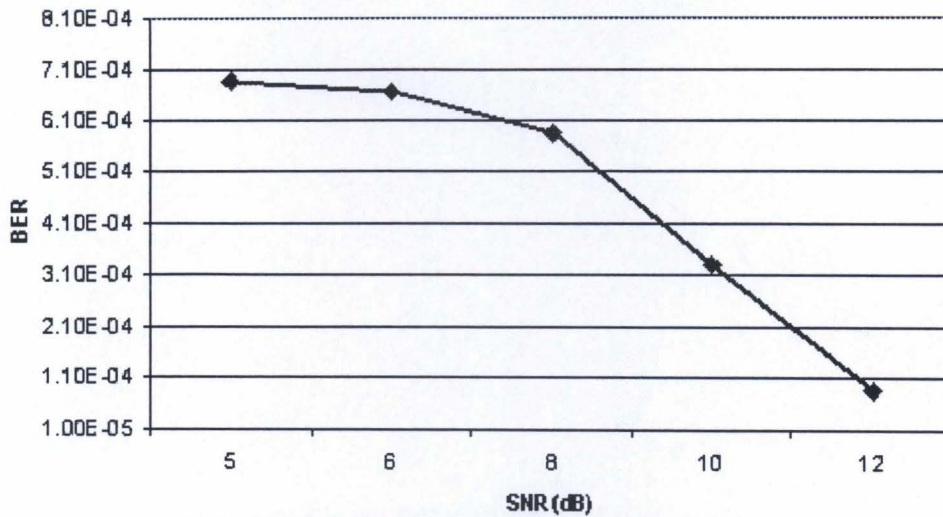


Figure 6.41: BER with AWGN and fast Rayleigh fading

Figure 6.41 shows the results obtained when the implemented receiver is operated on the software radio. The result depicts the performance of the receiver under various SNR conditions with AWGN when the channel is subjected to fast Rayleigh fading. Performance degradation up to 10^{-3} (8 dB) was expected in the absence of power control, error control (convolutional coding & interleaving) schemes, error forming and channel estimation functions. A significant improvement in the BER (about 10^{-3}) can be achieved using proper error control schemes [9]. Imperfect power control in the system causes degradation of the system capacity. Fast Rayleigh fading is implemented by introducing 4 samples of fading coefficients to a bit. Figure 6.42 shows the bit error probability when a bit experienced 2 different fading coefficients, which is considered as slow fading. Both graphs show the general trend associated with decrease in BER as the SNR improves.

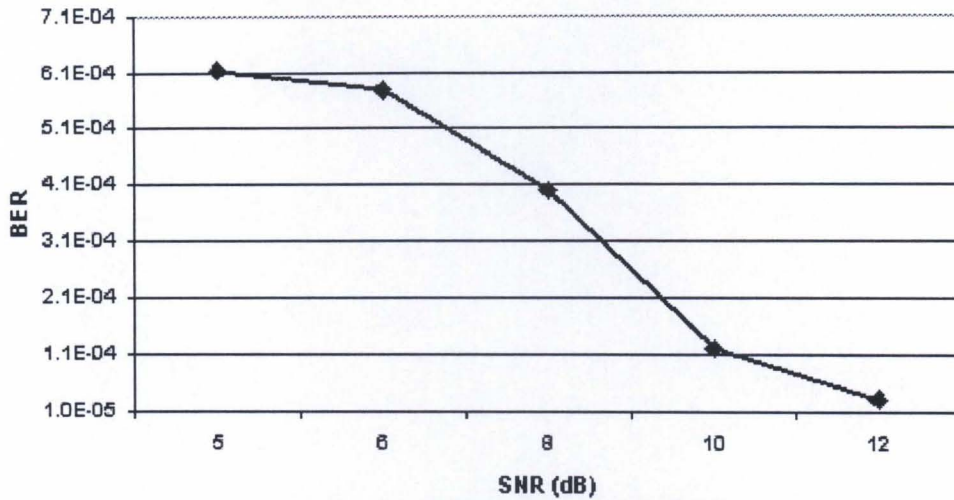


Figure 6.42: BER with AWGN and slow Rayleigh fading

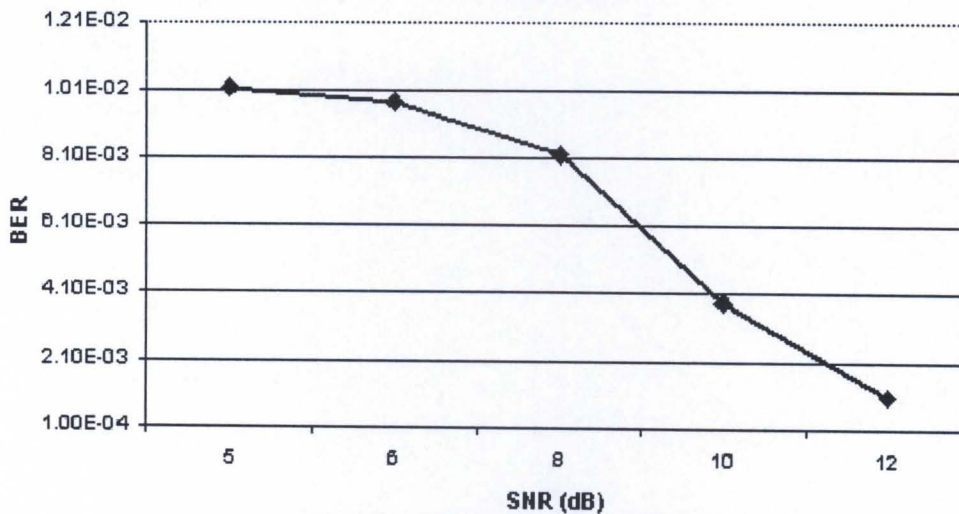


Figure 6.43: BER with arbitrary weights and delays

Figure 6.43 shows the BER of the same system but with improper weights and delays considered for beamforming (system BER without the beamforming unit). This result highlights the necessity of accurate weights and delays. This graph also shows the general trend associated with decrease in BER with higher SNR, which is due to the functionality of the SNR, RAKE combiner and filter blocks. In this case, the delays associated with the rake combiner are considered to be 0 sec. The RAKE combiner is used after the beamformer (Figure 6.28) i.e; after spreading so the data rate is 64 Kbps. The influence of an arbitrary delay in the bit error rate is comparatively small, because the delay considered in the previous cases is in the order of nano seconds due to small

propagation distances. So it can be inferred from these results that weights considered in this design were accurate and improve the performance of the system.

In order to compare the implemented system's BER results with the simulated system model discussed in Chapter 4, the simulated system model presented in Chapter 4 was redesigned using ADS 1.5. Rayleigh fading and AWGN are incorporated in the simulation. The error control schemes, channel and the error forming functions are eliminated from the redesigned system model. Figure 6.44 shows the BER of the simulated model with Rayleigh fading. The BER of the implemented system with Rayleigh fading is also included in the figure for comparison. With the increase in SNR the effect of fading diminishes the performance of the system. In slow fading, the variance of the fading statistics is small in comparison to fast fading. At 12 dB the difference in the BER is negligible. However, the BER results of the implemented receiver at various SNR clearly demonstrate the potential utility of the implemented receiver both in slow-fast Rayleigh fading and AWGN channels.

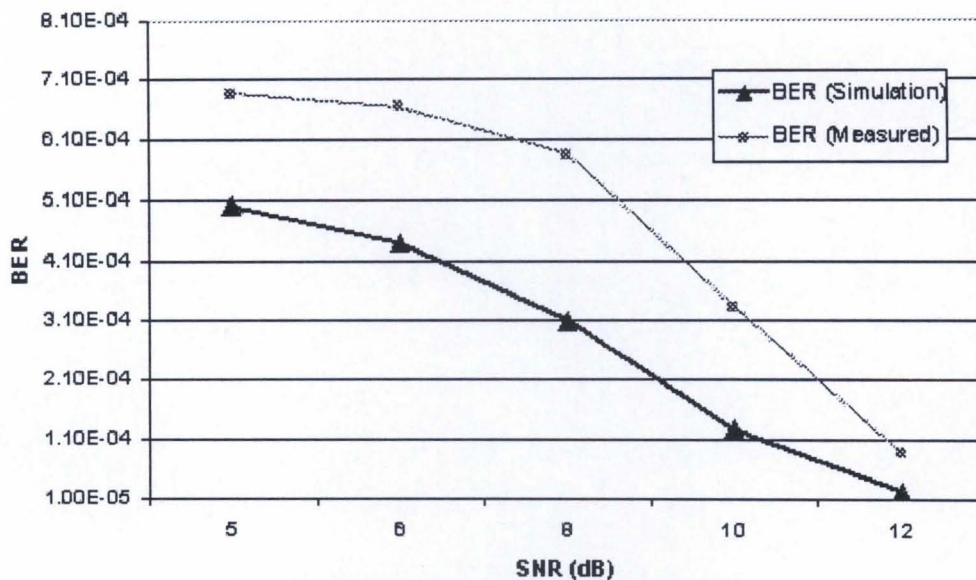


Figure 6.44: BER (Simulation) with Rayleigh fading

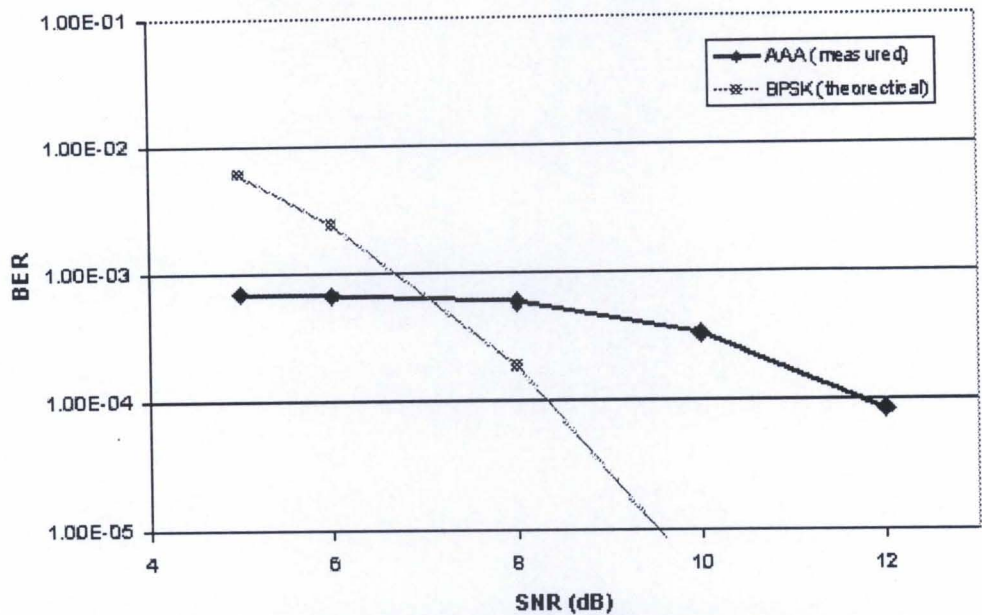


Figure 6.45: Comparison of measured and theoretical BER

The theoretical results (BER) [100] of a coherent BPSK receiver are shown in Figure 6.45. Comparing these results with the measured results (at SNR's of 5 and 6 dB) the measured results appear anomalous; the reasons for these anomalies have not been addressed in this thesis.

6.10 Conclusion

This chapter discussed AAA receiver implementation issues and measured results. In the first section, the issue of interfacing the software radio to the DSP subsystem and the synchronization of frames is examined. Different frame synchronization signals are derived and discussed. With regards to this, it was seen that VHDL simplifies the critical timing problems. The approach considered for spreading techniques in this chapter provides a flexible means of modifying the PN sequences. The code database is dynamic in that its contents can be programmed from the DSP if necessary. This technique has been used in preference to the standard generation techniques since it allows the designer a higher degree of flexibility when testing various codes. Base band filtering presents a challenge for the FPGA designer. The complexity of the pulse

shaping filter depends heavily on the input word length. This chapter also explained and implemented the filters to reduce bandwidth while maximizing signal to noise ratios at the input to the beamformers. The speed enhancement offered by the FPGA makes it a very attractive alternative to the traditional DSP based filtering systems. The channel estimation function estimates multipath delays, amplitude and phase. The main target of the multipath delay estimation unit is to provide accurate delay estimates at fast enough rates. The BER results (Figure 6.43) with arbitrary weights and delays prove the importance of the beamformer. The system achieved a better BER with the proper weights and delays used in the design. Considering the fact that the expected degradation in the fast/slow Rayleigh fading channel, the implemented system BER results become more optimistic compared to the simulation results.

The flexibility of the software radio has been used to simulate a simple communication channel incorporating AWGN and Rayleigh fading. The measured results depict the behavior and characteristics of the simple communication channel. The process involves many interfaces and techniques for passing data and control parameters between these interfaces which is also pointed out in this chapter. The great speed advantage of the software radio is exploited in the simulation, which makes it appealing for investigating and improving its performance further. From the discussions in this chapter it is evident that the software radio is a very useful tool in quickly and easily transforming mathematical processes into hardware implementations.

Chapter 7

Conclusion

7.1 Summary and conclusions

The wireless communications industry has been undergoing tremendous change in the last decade due to the rapid rise in demand for cellular services. The demand for improved performance began to draw on mathematical and technological innovations. Second generation mobile radio systems, which use digital technology in contrast to the analog based first generation systems, are very successful worldwide in providing services to users. CDMA promises tremendous capacity increases under conditions where the link is interference limited. With the introduction of interference techniques, CDMA has gained a lot of support among cellular providers. This led to the innovation of higher capacity or wider bandwidth systems, resulting in the evolution of WCDMA. Fast cell search under intercell asynchronous operation and the coherent demodulation are the principle benefits of WCDMA.

In order to maintain the performance degradation of a communication system at an acceptable level as the radio traffic increases, it is necessary to adopt measures to improve the mutual interaction robustness. Several systems may be considered, spread spectrum techniques appear to be one of the techniques to offer a reduction in vulnerability of a communication system. Chapter 2 described the technical details of CDMA using spread spectrum techniques. Multiple access is illustrated with the use of PN codes, and some inherent benefits and difficulties of DS-CDMA in a mobile environment are addressed. The PN sequence generator and the physical layer of CDMA are examined from an implementation point of view. Since WCDMA has evolved from CDMA, the basic concepts of CDMA were examined. The underlying differences between CDMA and WCDMA have been examined in the appropriate

sections. The WCDMA air interface parameters are also reviewed in Section 2.5. MAI is the major cause of channel impairment in DS-CDMA. An AAA receiver can suppress the MAI by directing the beam nulls towards the interference. The theoretical concepts and benefits of AAA techniques have been addressed in Chapter 3.

WCDMA is designed to exploit the benefits of AAA techniques. Adaptive arrays sense the interference source and suppress them automatically, improving the performance of a mobile system, without any *a priori* knowledge of the interference location. Chapter 3 dealt with antenna array theory and its benefits. The applications of antenna arrays in the mobile communication systems have also been discussed here. The weights of all antennas are controlled to maximize the signal to interference ratio for each user. In order to minimize the mean squared error between the combined signal and the reference signal an MMSE algorithm was considered.

An AAA receiver has been proposed in Chapter 4 for implementation in the software radio. In the proposed receiver, PSA channel estimation is used for coherent RAKE combining and weights of the antenna array are adaptively updated using both pilot symbols and decision directed data symbols after RAKE combining as references for MMSE criteria. In order to evaluate the performance of the proposed receiver a system model is designed (refer Appendix A-3) using ADS 1.3. The performance evaluation is carried out with a single element PSA RAKE receiver and a six element AAA receiver in different environments. The results obtained from the simulation clearly indicate the performance improvement of AAA receiver in all environments. During simulation power control was not considered. Section 4.4 established the need for power control in a DS-CDMA environment. A closed loop power control algorithm and structure was also discussed. The chapter concludes that it can be inferred that when the link is interference limited, the link capacity can be increased up to 2.9 times that of a single antenna RAKE receiver.

The need for flexible or reconfigurable radio platforms is enhanced due to the rapid deployment of various cellular standards and to provide global roaming. A software

radio is considered as a promising means to achieve this goal. Investigations show a software radio base station incorporating antenna arrays and power control techniques can significantly reduce the transmit power and reduce the call blocking in the mobile network.

Chapter 5 explores the theoretical and hardware concepts of the software radio. Flexibility and hardware configuration of AATs software radio platform are discussed. It offers many of the features and flexibility inherent in the software radio concept. Two FPGAs are used as the reconfigurable core in this software radio. VHDL is used to program these FPGAs. Benefits of FPGAs are reviewed in Section 5.3. Designing in VHDL involves a process of describing the desired operation of a complex circuit. A simple program is used to demonstrate the VHDL parameters. In order to test various codes as well as FPGA based transceivers a three-layer test bed was utilized. This test bed was used for the implementation of AAA receiver and also used to evaluate the performance of the implemented receiver.

Functional block allocation of the transceiver is presented in the first section of the Chapter 6. Subsequent sections of Chapter 6 presented the critical timing components and the generation of various frame synchronization signals used in the receiver. Generation of these frame signals are carefully designed and simulated because any discrepancies between these frame signals can affect the overall system performance. The spreader block is introduced as a code storage database with associated spreading circuitry. Filters are incorporated in this design for filtering purposes. Due to the limited capacity of the FPGAs a number of blocks were removed from the design during the implementation phase. The implemented receiver is subjected to AWGN and uncorrelated Rayleigh fading environments in order to evaluate its performance. The DSP layer is responsible for storing the Rayleigh fading coefficients and sending it to the software radio. These coefficients are then multiplied with the relevant signals in the software radio to produce a Rayleigh faded signal. AWGN samples generated by the AWGN generator in the FPGA are added to the relevant signal to produce a noise degraded output. Considering the significant performance degradation of a system in

fast/slow Rayleigh fading channels, it can be inferred that the BER of implemented system compares favorably with the simulated system BER results. Evaluation results show the performance of the implemented receiver both in AWGN and Rayleigh fading channels. Degradation in BER is expected due to the removal of the error control, channel estimation and power control blocks. In spite of the success of the project, there are many future developments that would allow this flexible platform to become an even more useful tool. Future developments of this system are suggested in the next section. The proposed suggestion can overcome the capacity limitations and develop a complete WCDMA network system.

7.2 Future development of the system

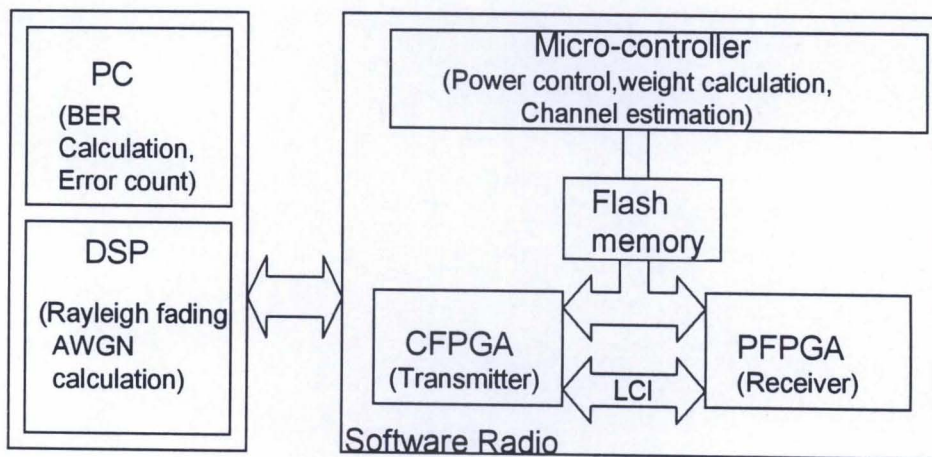


Figure 7.1: Functional split for the future development of the system

Figure 7.1 depicts the suggested functional split for future development of the system. Power control, weight calculation and adaptation and channel estimation can be performed in the micro-controller in the software radio. The error counting can be removed from the CFPGA to the PC. Rayleigh fading coefficients and the AWGN coefficients can be generated in the DSP layer. The removed error control block in the implemented system can be considered for the future development of the system. The coder and the interleaver can be implemented in the CFPGA while the decoder and the

de-interleaver can be implemented in the PFPGA. The micro-controller is capable of updating the appropriate weights every 0.5 ms as proposed in the implemented system.

Another future development proposal is to build a complete WCDMA network, adopting the implemented system as the basic shell. Since this project is developed as a part of Centre of Excellence programme, other research contributions in coding, power control, propagation channel effects etc can be included. Each functional block in the implemented system was considered as a separate entity, so these entities can be replaced with appropriate work developed in the research centre. This will boost the overall performance of the system.

This thesis has examined three cutting edge technologies namely WCDMA, AAA, and software radio that serve to complement each other as much as they each stand as individual milestones. WCDMA promises the security and privacy and performance of the mobile communication systems, while the AAA techniques ensure minimal interference and maximum capacity increase in the system. Software radios offer the flexibility to reconfigure the system for new standard deployment. Together, these technologies will invade tomorrow's world of mobile communications.

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Appendices

A-1: Minimum Mean Square Error

A-2. Least Mean Square (LMS) algorithm

A-3: Simulation Model

A-4 Various Frame synchronization signal comparisons

A-5 VHDL code used to generate various frame synchronization signals.

A-6. Calculation of Multipath delays

A-1: Minimum Mean Square Error (MMSE)[64]

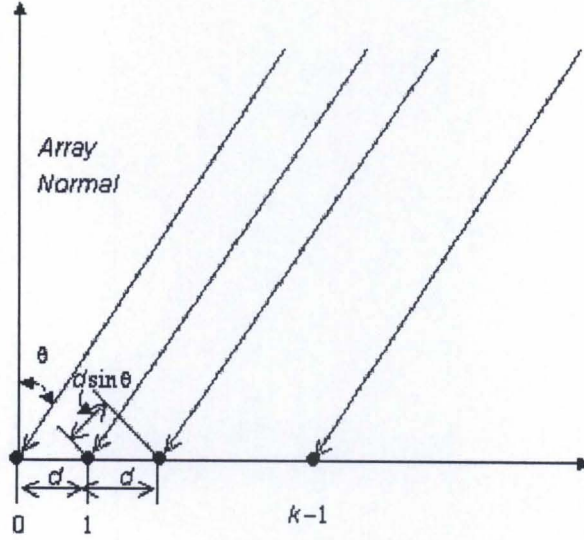


Figure A.1 Uniformly Spaced linear array [64]

Figure A.1 shows a uniformly spaced linear array with K identical isotropic elements, which operates in a signal environment where there is a desired signal $s(t)$, as well as N_u interfering signals $\{u_i(t)\}_{i=1}^{N_u}$. Assuming the desired signal arrives at an angle θ_0 and the i^{th} interfering signal arrives at an angle θ_i . The Array output is represented as:

$$x(t) = s(t)v + u = s + u \quad \text{-----}(9.1)$$

where v is the array propagation vector.

$$v^T = [1, e^{jkd \sin \theta}, \dots, e^{jk(K-1)d \sin \theta}] \quad \text{-----}(9.2)$$

and u represents the sum of all the interfering signal vectors,

$$u = \sum_{i=1}^{N_u} u_i(t)\eta_i \quad \text{-----}(9.3)$$

and η_i is the array propagation vector for the i^{th} interference signal,

$$\eta_i^T = [1, e^{jkd \sin \theta_i}, \dots, e^{jk(K-1)d \sin \theta_i}] \quad \text{-----}(9.4)$$

If the desired signal $s(t)$ is known, one may choose to minimize the error between the beamformer output $w^H x(t)$ and the desired signal, where w is the weight vector. But the knowledge of the desired signal eliminates the need for beamforming. For many applications however, characteristics of the desired signal may be known with the

sufficient detail to generate a signal $d^*(t)$ that closely represents it, or at least correlates with desired signal to a certain extent. This signal is called a reference signal, which is expressed in complex conjugate form only for mathematical convenience. The weights are chosen to minimize the mean square error between the beamformer output and the reference signal:

$$\varepsilon^2(t) = [d^*(t) - w^H x(t)]^2 \quad \text{-----}(9.5)$$

Taking the expected values of both sides of (5) and carrying out some basic algebraic manipulation:

$$E\{\varepsilon^2(t)\} = E\{d^2(t)\} - 2w^H r + w^H R w \quad \text{-----}(9.6)$$

where $r = E\{d^*(t)x(t)\}$ and $R = E\{x(t)x^H(t)\}$. R is usually referred to as the covariance matrix. The MMSE is given by setting the gradient vector of (6) with respect to w equal to zero:

$$\nabla_w(E\{\varepsilon^2(t)\}) = -2r + 2Rw = 0 \quad \text{-----}(9.7)$$

It follows that the solution is:

$$W_{opt} = R^{-1}r \quad \text{-----}(9.8)$$

which is referred to as the wiener-Hopf equation or optimum Wiener solution. If $s(t) = d^*(t)$, $r = E\{d^2(t)\}v$. One can then further express $R = E\{d^2(t)\}vv^H + R_u$, where $R_u = E\{uu^H\}$ and apply Woodbury's identity for R^{-1} .

$$\text{Therefore: } R^{-1} = \left[\frac{1}{1 + E\{d^2(t)\}v^H R_u^{-1}v} \right] R_u^{-1} \quad \text{-----}(9.9)$$

So the Wiener solution can be generalized as:

$$W_{opt} = \beta R_u^{-1}v \quad \text{-----}(9.10)$$

where β is a scalar coefficient. In the case of MMSE,

$$\beta = \frac{E\{d^2(t)\}}{1 + E\{d^2(t)\}v^H R_u^{-1}v} \quad \text{-----}(9.11)$$

A-2. Least Mean Square (LMS) algorithm

According to the method of steepest decent, the updated value of the weight vector at time $(n+1)$ is computed by using a simple recursive relation

$$w(n+1) = w(n) + \frac{1}{2} \mu [-\nabla (E\{\varepsilon^2(n)\})] \quad \text{-----}(9.12)$$

from (1.7)

$$w(n+1) = w(n) + \mu [r - R w(n)] \quad \text{-----}(9.13)$$

Practically exact measurement of the gradient vector is not possible, since this would require a prior knowledge of both R and r . The most obvious strategy is to use their instantaneous estimates, which are defined as:

$$\hat{R}(n) = x(n)x^H(n) \quad \text{-----}(9.14)$$

and

$$\hat{r}(n) = d^*(n)x(n) \quad \text{-----}(9.15)$$

the weights can be updated as:

$$\begin{aligned} \hat{w}(n+1) &= \hat{w}(n) + \mu x(n)[d^*(n) - x^H(n)\hat{w}(n)] \\ &= \hat{w}(n) + \mu(n)\varepsilon^*(n) \end{aligned} \quad \text{-----}(9.16)$$

where μ is the gain constant controls the convergence characteristics of the random vector sequence $w(n)$. The performance is acceptable in many applications. However, its convergence characteristics depend on the eigen structure of \hat{R} .

A-3: Simulation model

Figure A.2 shows the block diagram of the transmitter of the first user. Figure A.3 shows the block diagram of the matched filter designed in ADS. This matched filter block is used in the AAA receiver as well as in the RAKE receiver. Figure A.4 shows the block diagram of the AWGN noise channel. The complex AWGN noise signal is added to the transmitted signal. Figure A.5 shows the functional block diagram of the proposed PSA AAA receiver designed in ADS. Finally Figure A.6 depicts the functional blocks of the PSA RAKE receiver.

USER 1

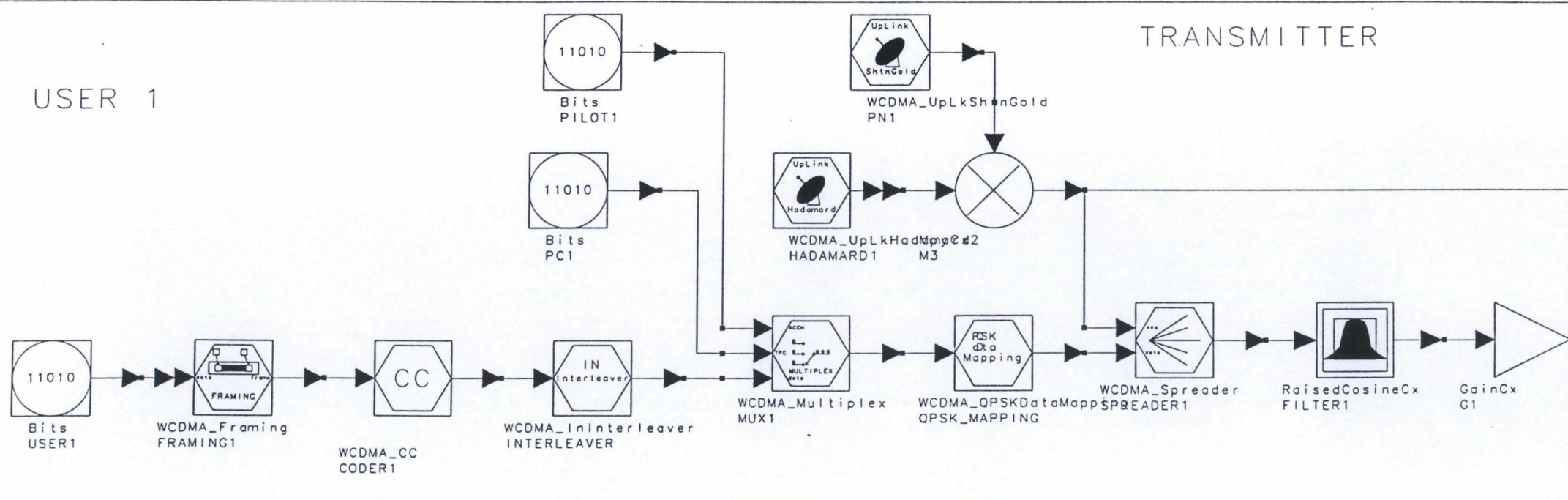


Figure A.2: block diagram of Transmitter designed in ADS

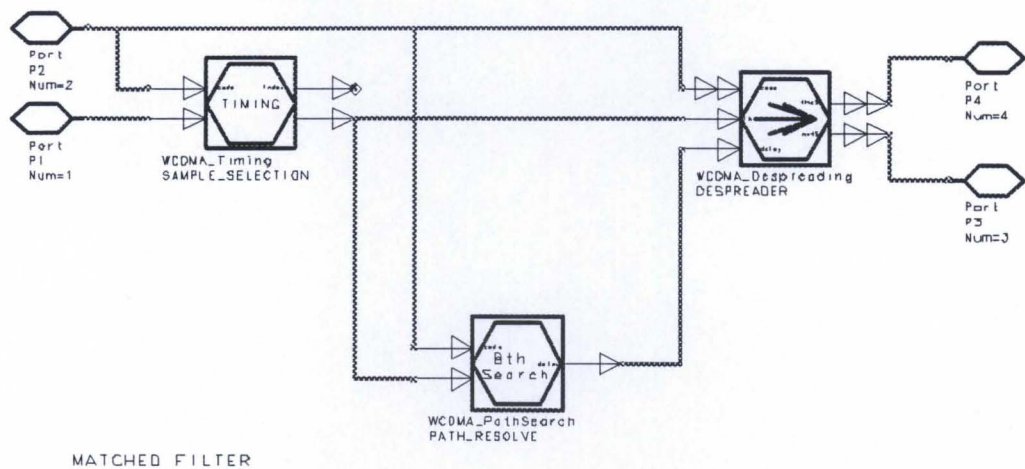


Figure A.3: Block diagram of Matched filter designed in ADS

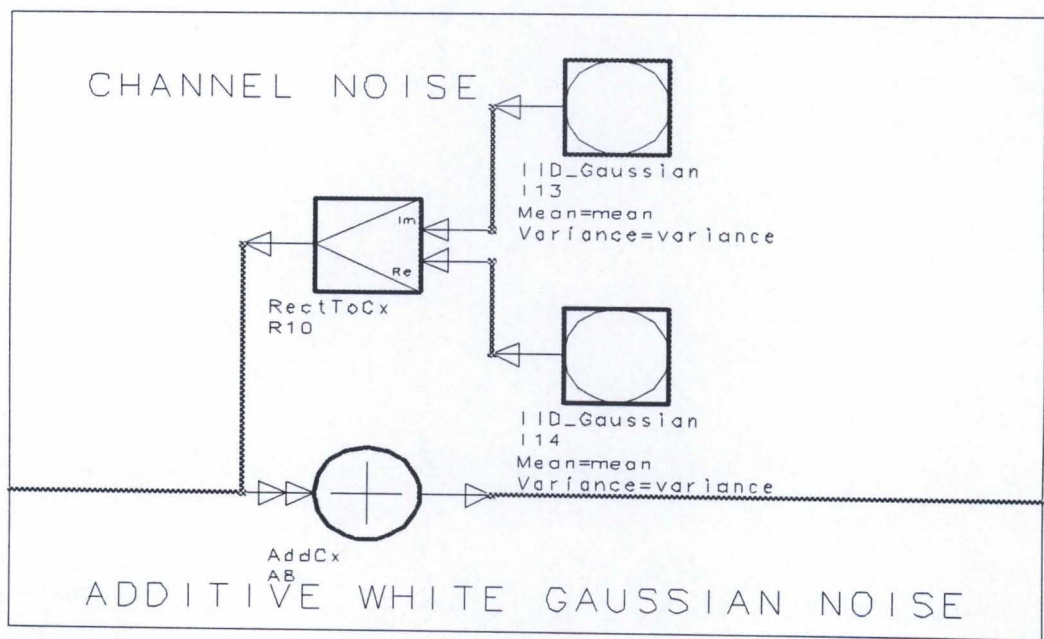


Figure A.4: block diagram of AWGN channel designed in ADS

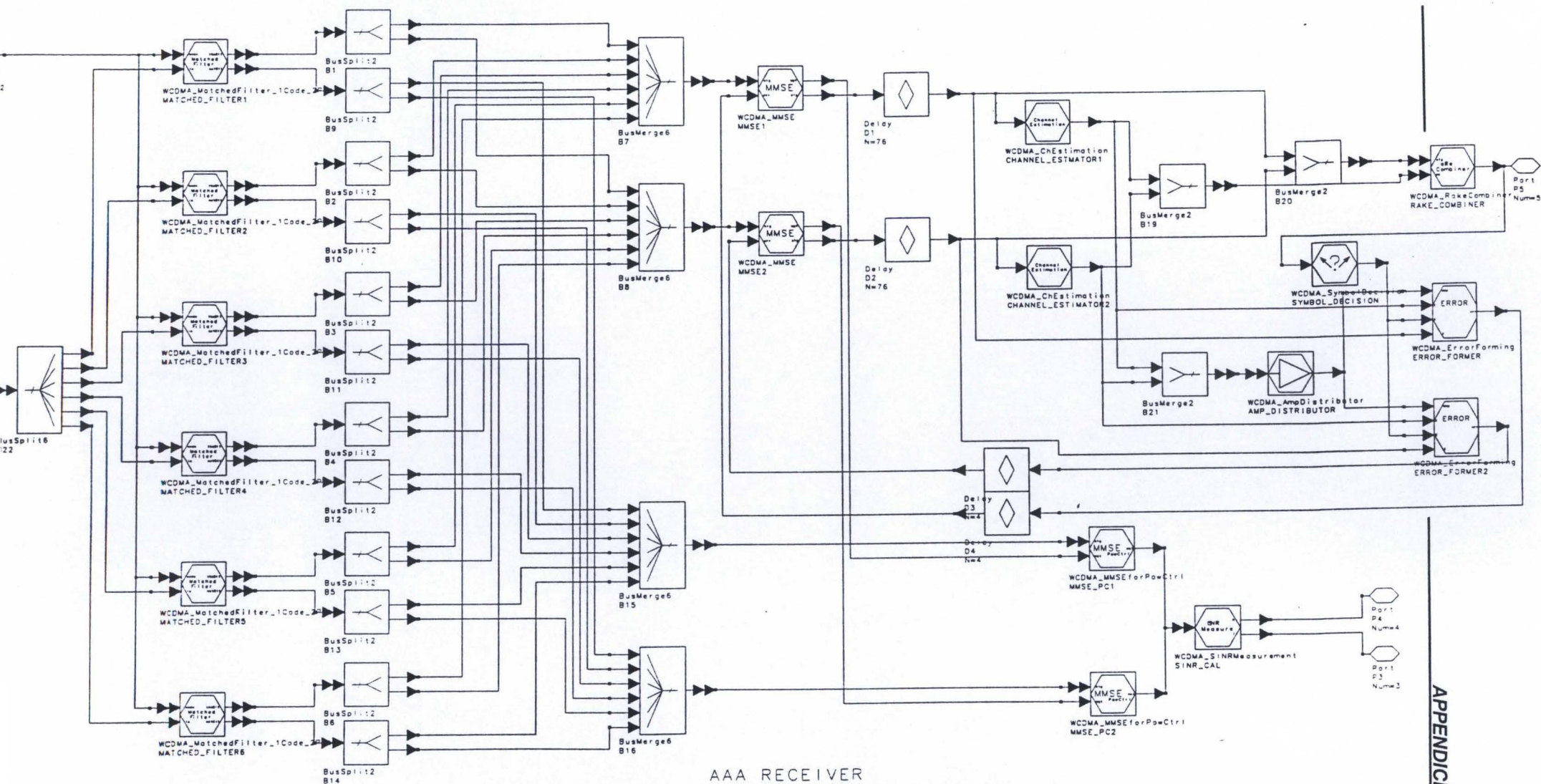


Figure A.5: Block diagram of AAA receiver designed in ADS

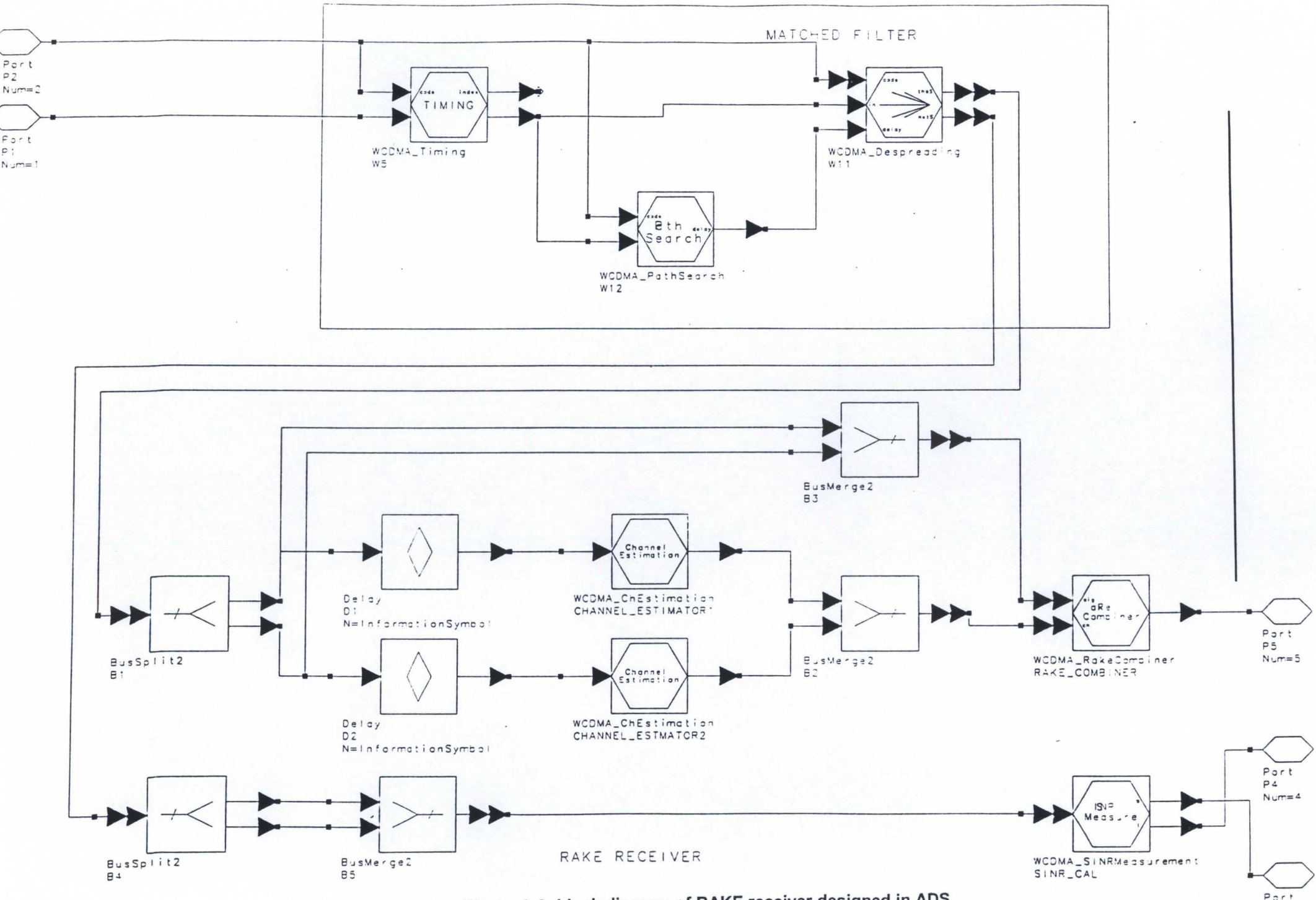


Figure A 6: block diagram of RAKE receiver designed in ADS

A-4 Various Frame synchronization signal comparisons

Figure A.7 shows the various synchronization signals used for the implementation of proposed receiver. When the FSYNCNP is high indicates the presence of pilot bits in the radio frame. This means that when it is high the corresponding bits in the radio frame are identified as the pilot bits. The same process is in the case of FSYNCNPC frame.

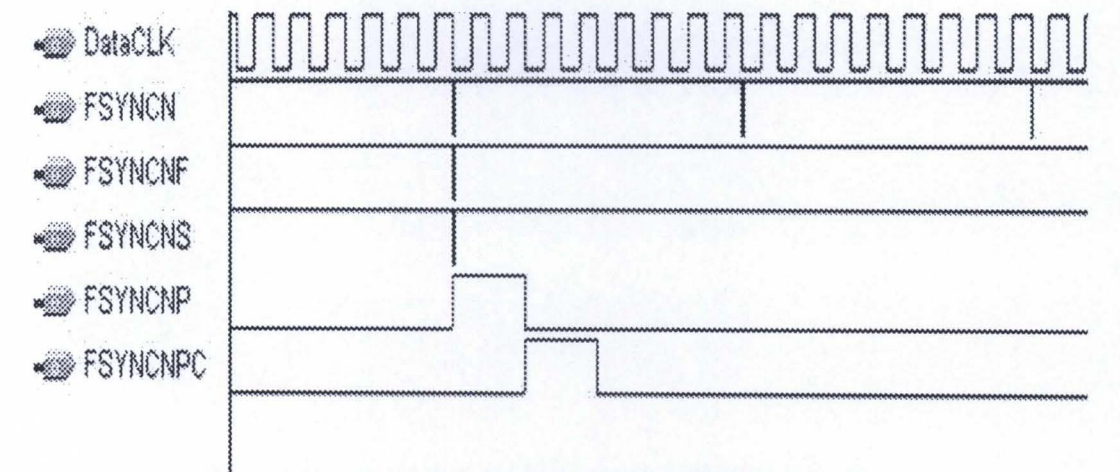


Figure A.7 Frame sync corresponding with data clock 64 KHz

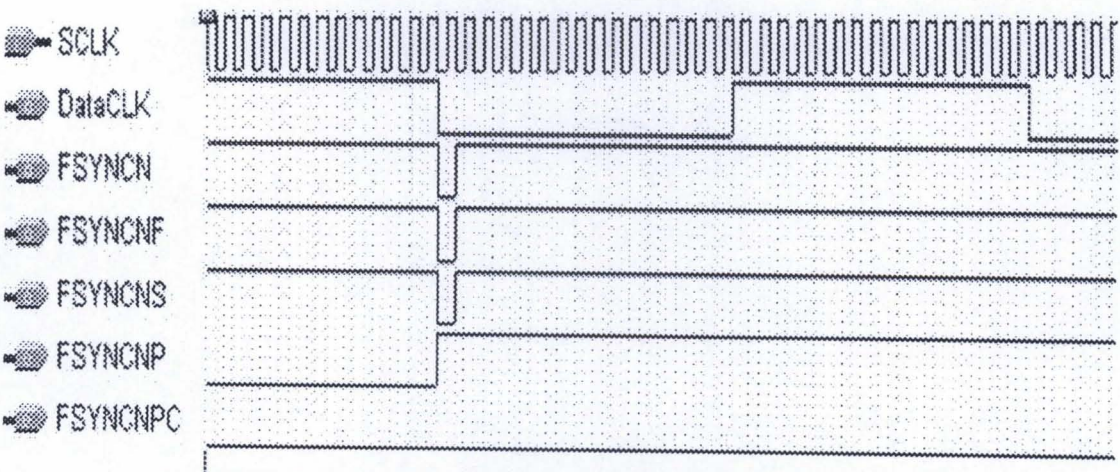


Figure A.8 Frame sync corresponding with data clock 64 KHz & SCLK

Figure A.9 shows the measured frame synchronization signals from the CFPGA.

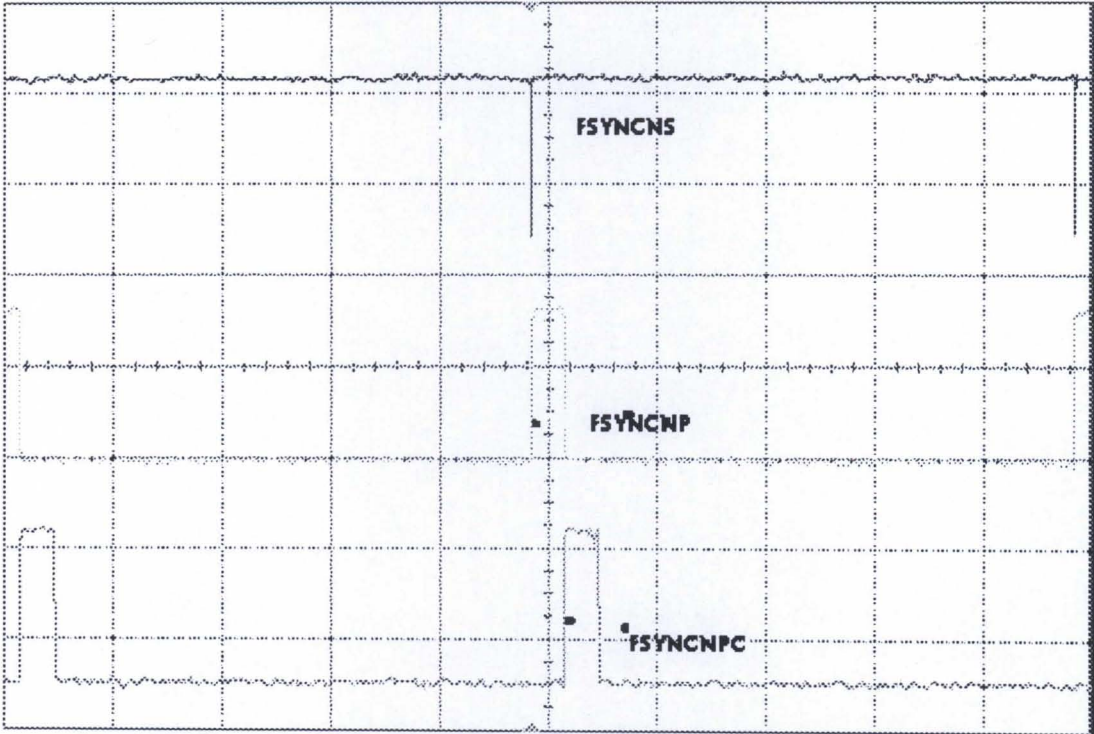


Figure A.9: Measured frame sync signals from CFPGA

A-5: VHDL codes used to generate various frame synchronization signals

```
--//=====//
--Author      : Saju
--Purpose     : To derive useful frame synchronization signals
--Entity Name : eSystemClock
--//=====//

Library IEEE;
Use IEEE.std_logic_1164.all;
Use IEEE.numeric_std.all;
Use IEEE.std_logic_arith.all;

**Defining the number and type of ports in the entity.
entity eSystemClock is

Port ( CLK132M   : In  STD_LOGIC; -- System clock
      SCLKx2     : Out STD_LOGIC; -- Double rate serial clock
      SCLK       : Out STD_LOGIC; -- Single rate serial clock
      CLK64K     : Out STD_LOGIC; -- 64 KHz clock
      FSYNCN     : Out STD_LOGIC; -- Frame synchronization signal (8 KHz)
      FSYNCNS    : Out STD_LOGIC; -- Frame synchronization signal for slot
      FSYNCNP    : Out STD_LOGIC; -- Frame synchronization signal for pilot
      FSYNCNPC   : Out STD_LOGIC; -- Frame synchronization signal for power
                                control
      FSYNCNF    : Out STD_LOGIC; -- Frame synchronization signal for
                                WCDMA frame (125 Hz)

```

```
end eSystemClock;
```

**** Architecture, which determines the implementation of an entity, can range in abstraction from an algorithm (a set of sequential statements within a process) to a structural netlists (a set of component instantiations).**

architecture aSystemClock of eSystemClock is

**** signals** localCLK4M, localSCLK, localSCLKx2, localFSYNCN, localFSYNCNP
Pcreg, localCLK64K, clk32k and clk8k are local signals declared in the architecture.
These signals are local to architecture aSystemClock and cannot referenced outside the
architecture.

```
Signal localCLK4M    : STD_LOGIC;
Signal localSCLK     : STD_LOGIC;
Signal localSCLKx2   : STD_LOGIC;
Signal localFSYNCN   : STD_LOGIC;
Signal localFSYNCNP : STD_LOGIC;
Signal PCreg         : STD_LOGIC;
Signal localCLK64K   : STD_LOGIC;
Signal clk32k, clk8k : STD_LOGIC;
Signal clk2k, clk125 : STD_LOGIC;
Signal tmpCounter    : IEEE.numeric_std.unsigned (4 down to 0);
Signal count64k      : IEEE.numeric_std.unsigned (3 down to 0);
Signal count32k      : IEEE.numeric_std.unsigned (0 down to 0);
Signal count8k       : IEEE.numeric_std.unsigned (1 down to 0);
Signal count2k       : IEEE.numeric_std.unsigned (1 down to 0);
Signal count125      : IEEE.numeric_std.unsigned (3 down to 0);
```

begin

GenSCLKx2 : Process (CLK132M)

****Generation of SCLKx2 from CLK132M**

begin

```
    if (CLK132M' event and CLK132M = '1') then ---wait for positive transition (edge)
        tmpCounter <= tmpCounter + "00001";
```

```

        if (tmpCounter = "11111") then -- need to set the count 32
            tmpCounter <= "00000"; -- reset the counter
            localCLK4M <= not localCLK4M; --not any delay
        end if;
    end if;
end process;
SCLKx2 <= localCLK4M;

```

GenSCLK : Process (localCLK4M)

****Processing localCLK4M to generate SCLK**

```

begin
    if (localCLK4M' event and localCLK4M = '0') then
        localSCLK <= not localSCLK;
    end if;
end Process;
SCLK <= localSCLK;

```

GenFRAMES : process (localSCLK)

****Processing localSCLK to generate various frame synchronization signals.**

```

begin
    if (localSCLK'event and localSCLK = '0') then
        if count64k = "1111" then --divide by 32
            localCLK64K <= not LocalCLK64K; ---data CLK

            if count32K = "1" and localCLK64K = '1' then
                clk32K <= not clk32K;

                if count8K = "11" and clk32k = '1' then
                    if clk8k = '1' then

```



```
FSYNCN <= '0'; -8 Khz frame
end if;
clk8K <= not clk8K;

if count2K = "11" and clk8k = '1' then
    if clk2k = '1' then
        FSYNCNS <= '0'; --frame sync for slot
        localFSYNCNP <= '1';
    end if;
    clk2K <= not clk2K;

    if count125 = "1111" and clk2K = '1' then
        if clk125 = '1' then
            FSYNCNF <= '0'; --125Hz frame
        end if;
        clk125 <= not clk125;
    end if;
    count125 <= count125 + 1;

end if;
count2k <= count2k + 1;

PCreg <= '0';
else
    if clk32k = '1' then
        PCreg <= localFSYNCNP;
        localFSYNCNP <= '0';
    end if;
end if;
count8k <= count8k + 1;
```

```
        end if;
        count32k <= count32k + 1;

    else

        FSYNCF <= '1';
        FSYNCS <= '1';
        FSYNCF <= '1';

    end if;
    count64k <= count64k + 1;
end if;
end process;

FSYNCF <= localFSYNCF;
FSYNCS <= PCreg;
CLK64K <= localCLK64K;
end aSystemClock;
```


A-6. Calculation of multipath delays

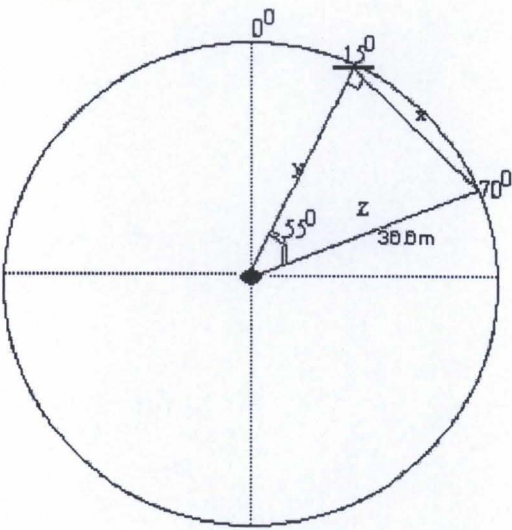


Figure A.10: Multipath 1

Assuming the distance between the antenna and the desired is 36.6 meters. As shown in the Figure A.10 the line Z is the direct path to the antenna and xy is the reflected path.

The distance x is calculated as follows

$$x = Z \sin 55^\circ = 36.6 \sin 55^\circ = 29.981m \quad \text{-----(9.17)}$$

$$y = Z \cos 55^\circ = 36.6 \cos 55^\circ = 20.99m \quad \text{-----(9.18)}$$

from (9.17) and (9.18)

$$\text{Total distance} = 29.981 + 20.99 = 50.971m$$

$$\text{Difference} = 50.971 - 36.6 = 14.371m$$

$$\text{Delay of first path} = \frac{14.371}{3 \times 10^8} = 47.903 \eta \text{sec.} \quad \text{-----(9.19)}$$

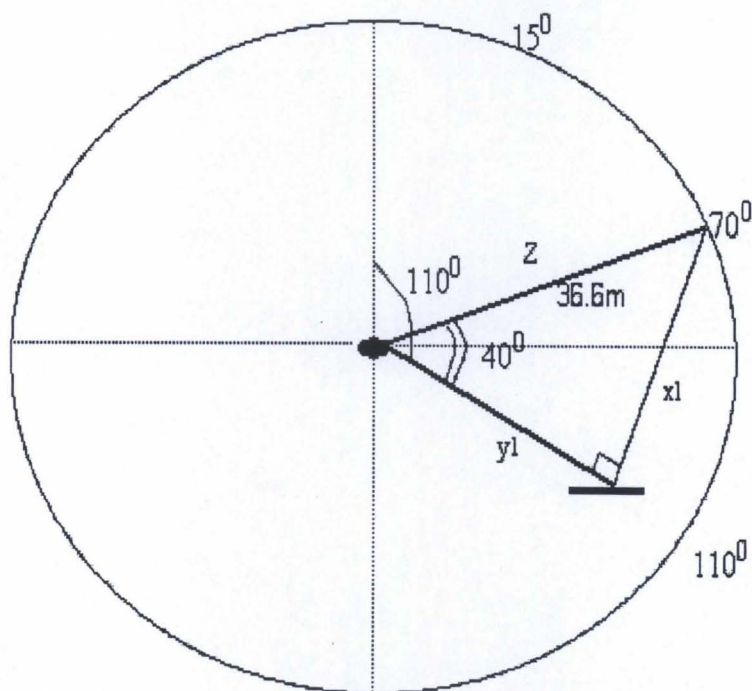


Figure A.11: Multipath 2

Similarly for the path 2

$$x_1 = Z \sin 40^\circ = 36.6 \sin 40^\circ = 23.52m \quad \text{-----(9.20)}$$

$$y_1 = Z \cos 40^\circ = 36.6 \cos 40^\circ = 28.04m \quad \text{-----(9.21)}$$

from Eq (9.20) and (9.21):

$$\text{Total distance} = 23.52 + 28.04 = 51.56m$$

$$\text{Difference} = 51.56 - 36.6 = 14.96m$$

$$\text{Delay of path2} = \frac{14.96}{3 \times 10^8} = 19.867 \mu\text{sec} \quad \text{-----(9.22)}$$