

## Declaration

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#### Abstract

In a rapidly evolving technological and industrialised society, automation is a current and growing trend. The concept is typically applied to uneconomical processes and extends from the automation of highly complex processes to those that are less complex. This dissertation discusses the automation of a previously mundane, manual, time-consuming and inefficient task using an embedded controller with dual enhanced microcontrollers as its core. Spoornet recognised the need to automate this and other processes hence a drive was initiated by Spoornet's Engineering and Technology department into the study of automation principles and techniques that can be used as a basis for the automation of workshops and test centers. This research stems from the above mentioned drive.


The Volt-Drop Test was the process that was used as a model to investigate the considerations, boundaries, design concepts and the hardware and software development that is inherent in the automation of a process. The design of the controller that facilitates the automation of the Volt-Drop Test was completed after research into embedded systems, embedded microcontrollers, programming languages and techniques, digital electronics, analogue electronics, digital system design concepts and techniques, analogue system design concepts and techniques, and the latest available electronic components.

A Graphic User Interface (GUI) was developed to interface with the controller to set up test parameters, display the present test status, perform calculations on the data received from the controller and display faults in the armature under test. Further, the GUI has the functionality to save all test data in a predefined and secure location to be retrieved and viewed as historical data or used for trending. A Remote Graphic User Interface (RGUI) was also developed. This interface is used solely to view test data (retrieved from the saved history files), from any geographic location provided that the user has been granted access to the secure location in which this data is saved.

In the testing phase, all tests were carried out using high quality, high accuracy and recently calibrated instrumentation. The test results obtained largely reflected what was expected from the system when compared to simulations that were carried out on the controller and the GUI during their development. With regard to the automation process, the system follows the procedure as it was designed with respect to correct switching sequences, response to system errors, timing of events and correct and efficient communication between the controller and the GUI. In terms of the data acquisition aspects the system captures, converts, calculates, analyses and logs data, within the expected input range with a level of accuracy that is considered to be high (a maximum percentage error of $0.75 \%$ - expressed as a percentage of the injected test supply) for this type of application when compared to the accuracy of present test methods.

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## Chapter 1

## Introduction

### 1.1 General Background

Automation [1], [6] in the industrial arena was the evolutionary step from mechanisation. Mechanisation sought to use machinery to accomplish physical tasks that were previously undertaken by humans or animals, through the use of mechanical engineering concepts in order to complete tasks in a shorter timeframe and with less effort. The machinery was still fully controlled by humans that were required to use their senses to monitor, their brain to compute progress, decisions, outcomes or assessments and their limbs (actuated by muscles), voice or physical actions to provide an appropriate output.

Automation involves the use of sensors/transducers, controllers and actuators to control a machine carrying out a task or a process consisting of multiple operating machines. Sensors [1], [7], [8] are used to sense the value/condition/progress/status of a parameter or task in the real world. They convert real world parameter values for temperature, pressure etc. to electrical signals. Controllers read these electrical signals and convert them to meaningful values that are used as variables in the controller logic to determine an appropriate output. If a physical output is required, the controller may itself or via the use of sub-controllers control actuators [1], [7], [8] that perform the real-world action required. Tasks within a process can be precisely controlled as there can be constant communication between controllers or process coordination via a master controller (master) to which individual task controllers (slaves) report.

From a controller perspective, the automation of industrial processes and machinery (leading into the realm of robotics) can be accomplished using the wealth of controllers and controller architectures available off the shelf, and by the design of embedded controllers which are used for dedicated or specialised applications. An automation project begins with the study of an existing process or machine. If the process or machine is not in existence then a theoretical or academic analysis of the
process is undertaken to determine how the process can be best automated and what machinery is required to carry out the task or tasks. As part of the machine or process design the inputs to the system needs to be determined. This leads to the choice of the appropriate transducer to convert the real world parameter values to electrical signals e.g. distance, temperature, pressure, acceleration, speed, flow rate etc. Also part of the machine or process design is the identification of the required outputs from the system.

Actuators are chosen based on what the machine or process is required to physically control or output. Actuators convert the electrical signals from the control system to real world physical outputs. Audio, visual, data etc. may also be required as outputs. These are implemented using audio system, display units and communication modules/ports/buses. The automated machine may be a standalone device or part of a process or network. If the latter is true then communication between devices is critical. The communication protocol is dependant on the choice of the control device, i.e. PLC [1], [6], [8] embedded controller or industrialised mother board. Also to be determined is whether a human-machine interface (HMI) or graphic user interface (GUI) is required.

Some tasks or processes may require an output or end result with no need for human intervention. In this instance, all that is required from the controller is data or physical real world outputs. Where human intervention is required, a HMI or GUI will give the operator control of the machine or process when required. As important is the HMI or GUI which provides insight into the status of the tasks presently undertaken as well as graphically displaying required data. The choice of HMI or GUI is also dependant on the choice of controller. For example where PLCs are used, Supervisory Control and Data Acquisition (SCADA) [6] software (e.g. Wonderware) is most commonly used. In the case of embedded controllers and industrialised mother boards, HMIs or GUIs can be developed in Visual Basic [3], [4], C Sharp etc.

PLCs have proven to be the most popular controller choice for industrial automation. They are considered as a generic solution for automation tasks that do not require specialised processing and control. Single, standalone PLCs can be used for the control of a machine or multiple networked PLCs, distributed throughout a plant, can


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control multi-loop processes aided by communication over Ethernet and using protocols such as Modbus, Profibus etc. System architecture may vary from central control where a single PLC controls multiple remote Input/Output (I/O) modules, to a distributed system architecture where PLCs are networked and communicate with each other or via a master controller that coordinates tasks and the flow of data. In the first instance, the PLC is the core of the system and performs all the processing (logic and mathematical operations) and issuing of instructions. The PLC communicates with remote I/Os to acquire data or instruct an output. The processing capability of an $\mathrm{I} / \mathrm{O}$ module is determined by the application. In the case of a distributed architecture each PLC is assigned the control of a task, machine, or component. Data is transmitted between PLCs or to a master PLC. The HMI resides on a host PC or microprocessor based display unit that communicates with the master PLC via the serial port, Ethernet etc. This system is defined as a SCADA system and its configuration is similar in functionality and architecture to a formally defined Distributed Control System (DCS) [6].


A DCS is typically a large control system that consists of a number of distributed microprocessor/microcontroller based controllers situated near or on the device it controls. I/O devices can be directly coupled to the controller or they can be located remotely and connected to the controller via the chosen industrial network. Also integral in a DCS are PCs or microprocessor based display units that run HMIs etc. All these subcomponents are supplied by single vendor that custom designs and configures a complete system for the process(s) to be controlled. This differs from a SCADA system where controllers, I/O devices, HMI software, display units etc. may all be off the shelf and originate from different vendors. In the past, SCADA systems were considered to be supervisory in nature with its primary function being data acquisition and display, and to provide the primary control system with calculated parameter values. DCS were considered as the primary control system. With the introduction of PLCs and the advanced communication technologies now used in SCADA systems, the line between DCS and SCADA systems have been blurred.

A PLC can be programmed in five programming languages as defined by IEC 611313. These are: Ladder Logic (LD) [8], Structured Text (ST), Instruction List (IL), Functional Block Diagram (FBD) and Sequential Function Chart (SFC). With the
evolution of PLCs came the evolution of HMIs. SCADA software has proven to be the most popular. Tags or points are assigned to each input or output controlled by the PLC. The SCADA software interface addresses tags or points when data has to be read from an input or an output has to be controlled. Points are referred to either as "hard" or "soft" with "hard" referring to actual data and "soft" referring to values that are the result of mathematic or logic expressions using "hard" point values. All data can be displayed numerically or graphically using the SCADA HMI graphic building blocks to represent components, equipment or processes. Data can also be stored in a data base for historical trending or auditing. Alarms and warnings can be defined to alert the operator of undesirable or dangerous conditions so that the operator can take the appropriate action using the interface to control the outputs of the PLC.

Embedded controllers are designed for specialised needs that are dedicated to specific tasks where generic PLCs may offer inferior performance. Microcontrollers [9] or Digital Signal Processors are usually the core of an embedded system with interfacing circuitry comprising digital and analogue electronic subsystems that condition signals to the input of the core and provide outputs from the core to the outside world. In most instances the core is a self contained device comprising of all the modules that are found on a standard PC. Microcontrollers for example contain a central processing unit (CPU), input/outputs ports, onboard Flash memory, RAM and communication ports (serial, USB, Ethernet). On specialised microcontrollers, analogue to digital converters (ADCs), comparators, PWM generators etc. can be found. Microcontrollers are manufactured by a number of companies each with various families that range from 4-bit to 64-bit and are chosen based on the processing power required. Microcontrollers are programmed in Assembler, C etc. using development environments that are provided by the manufacturer of the device e.g. Atmel, Microchip etc. or by developers that specialise in developing embedded development tools e.g. Keil C, Acebus [2] etc. The code that resides on an embedded controller is referred to as firmware.

Embedded controllers may operate in isolation as in the case of a dedicated controller for a machine or component or as part of a DCS. In the case of DCSs, each embedded system is a dedicated controller and communication between controllers via Ethernet, serial port, CAN bus etc. can be accomplished using protocols such as Controller

Area Network (CAN) [13], [14], [15], [16], etc. Systems communicate with each other or via a master controller (master) with slave controllers (slaves) reporting to and taking instructions from the master. The degree of pre-processing and control by slaves vary based on the system needs. This will impact on the choice of slave processor. In the CAN architecture, CAN transceivers embedded on each controller are responsible for communication via the CAN bus. A CAN master controls the flow of data on the CAN bus as well as providing data to a host PC which interprets, processors, stores or displays the data on a HMI or GUI. The HMI resides on the PC and communication with the CAN master is via the serial port, Ethernet etc. Due to the flexibility inherent in the design of an embedded controller (cost factor aside) controllers can be designed for various operating conditions, tasks, inputs, outputs and processing requirements.

A step taken to make embedded controller design more accessible to programmers as opposed to specialised engineering disciplines was the introduction of the industrialised mother board. This motherboard is essentially a standard PC motherboard that has been designed to operate in harsh environments, i.e. extreme temperatures, EMI [5] conditions etc. Boards vary depending on the type of processor, memory, input/output ports etc. that are required. Processors only differ from standard PC processors with regard to temperature specification due to the environments in which they operate. Any standard operating system (OS) can be loaded onto these processors, however for efficiency and improved processing speeds embedded OSs such as Embedded Windows XP are used with only the drivers required for the incorporated peripherals installed. Touch screens and LCDs that display the HMI or GUI are easily incorporated. HMIs and GUI can be written in almost any language for execution on the controller. The industrialised motherboard controller interfaces with off the shelf I/Os, specialised designed I/Os and other controllers via the onboard communication ports, hence they can operate within a network or as a standalone controller.

Controllers are most widely used for the execution of predefined tasks and error handling procedures based on predefined conditions or events. This is accomplished by hard coding logical steps or mathematical algorithms that provide outputs based on the inputs received. Decisions are presented as a choice of possible hard coded
outcomes. Using this methodology or approach, every possible outcome, event or occurrence must be known before coding can begin. This approach works very well when a complete system analysis has been carried out and every possibility or occurrence in the system is taken into account. In systems where every possible event or outcome is not known or where the system is expected to adapt or "learn" from basic building blocks in the decision making process, or make decisions that do not exist as hard coded instructions, Artificial Intelligence (AI) [10], [11], principals are introduced to bridge the divide. Concepts such as Fuzzy Logic [8], [10], [11], Neural Networks [10], [11], etc. are applied to make decisions based on inputs that are not discrete or expected or use past "experiences" that are based on human experience or historical data and outcomes acquired by the controller. In the realm of automation AI is most prevalent in robotics with AI concepts being applied to motion control, balance, sight based on image recognition and image processing etc. With the growth in processing power in most controllers, AI will become a more prevalent feature as knowledge and trust in the field grows.

### 1.2 Overview

Given the advancement of technology, the need be efficient in order to drive financial gains and the need to be competitive, Spoornet acknowledged the necessity to streamline their processes and methods of operation in order to improve their efficiency, reduce cost and increase profit. One way of achieving this is through the automation of processes that require skilled staff to perform simple and time consuming tasks. The objective of this research project was to design an embedded controller and GUI that will automate the Volt-Drop Test process.

The successful design principles, techniques and findings from this research and design process will be used to automate other such tests and processes in workshops and test centers. The reason for the design approach as opposed to the purchasing of controllers is based on Spoornet having a wealth of recourses in terms of equipment, facilities, funding and engineers, all of which have been used successfully to design, build and install embedded systems onboard locomotives. It was therefore a natural extension to use these resources to design controllers to automate processes in workshops and test centers.

This research and design was undertaken according to the mandate given by Spoornet to design an embedded controller and GUI for the automation of the Volt-Drop test. All software and firmware development is entirely the original work of the author. Where mathematic equations were encoded to form the computation algorithms for the GUI, the sources were quoted. The sources are purely mathematic books, which only provided equations, the coding of the equation as a function in the GUI was the work of the author. The circuit design is also entirely the original work of the author, except for the standard circuitry that is stipulated by the manufacturer for the setting up of the 555 Timer, the AT89S51, the MAX 701, the MAX 4622, the MAX 232 and the MAX 1166. This standard circuitry includes quartz crystals, capacitors and resistors that are stipulated by the component manufacturer in the component datasheet for the correct operation of the component.

In certain instances the suggested values were changed to suit the application for which the component was used. Other than the standard manufacturer component setup circuitry, all designs, component choices and calculations were undertaken by the author. This includes all circuit designs, schematic designs, component choices, PCB layout and design, protection circuitry that was required, EMI protection and software and firmware development. This work is also based on the experience that the author has gained during the design of controllers which operate on locomotives, especially in highly electrically noisy environments. One such design was that of a Weak-field controller for a pneumatic Weak-field switch array on the 6 E class of electric locomotives.

Given the mandate, the first phase of the research into embedded controllers and embedded system design involved research into microcontrollers. Once the basic principals were understood, more complex concepts such as Interrupts and Interrupt Service Routines, as well as Serial Communications were tackled, as these are key features that the controller would require for effective operation. The next phase in this project involved devising a practical concept for the automation of the Volt-Drop Test. From this phase, the author was able to decipher the number and types of transducers that would be required to monitor the system and provide the relevant feedback, as well as gauge the number and types of outputs that would be required by
the Drives and Drivers of the associated actuators (off-the-shelf Drives are used for motor control and off-the-shelf Drivers are used for IGBT switching). With knowledge of the number of inputs and outputs that the embedded system would require, as well as the expected input and required output, electrical signals that would enter and leave the system, an interfacing Digital and Analogue System was designed. These networks form the interface between the signals being received from sensors and transmitted to Drives and Drivers, and the microcontroller core.

The digital system involves level shifting, signal conditioning and logic manipulations. Also part of the digital system is the Analogue to Digital Converter (ADC) [8]. The ADC is controlled by the Communications Microcontroller, which also reads the data made available on ADC's eight-bit parallel output bus. The ADC's analogue input is the last stage in an analogue network that is responsible for the rejection of any signals that are out of the ADC Analogue input range. Considerable time was also spent in researching components such as ADCs, instrumentation amplifiers, semiconductor based analogue switches, optical sensors, proximity switches, motor drives, IGBT drivers etc.

The development of the GUI was carried out in parallel to the design of the controller. For the GUI development, the principals and techniques of object orientated programming had to be understood before the interface was designed and coded. A critical aspect during this phase was the establishment of a serial communication link between the GUI and the controller. During development however, the controller was not available to test the GUI's response to prompts and data transmitted from the controller. It was for this reason that a simulation interface was designed to mimic data that was transmitted by the controller.

Using the simulator, the author was able to monitor the GUI's response to prompts and ascertain the accuracy of the calculations carried out by the GUI. The GUI was not only designed as an interface to the automated system. Along with data analysis, test results are automatically saved in files that bear the same name as the serial number of the armature under test in a predefined destination that is specified using the GUI. This is done in order to create a test history of each armature tested. At the end of a test, the user also has the option of printing an official test report that reflects
the name of the user, the type of armature under test, the date of the test, armature winding faults that were logged during the test, as well as an undertaking, that has to be signed by the user, to remedy these faults.

Once the two entities, these being the controller and the GUI, were fully developed, additional features were integrated into the system before the testing phase of this project began. Two of these features ensure a greater level of accuracy during data acquisition and analysis. The first is the ability of the system to capture one hundred consecutive readings on a single pair of bars and record these readings on an Excel spreadsheet, which is also automatically saved along with the Fault Logged results. Presently, the average of the one hundred readings is used in calculations and is displayed on the GUI. However, any other filtering or statistical methods algorithm can replace the averaging algorithm in order to group the most relevant readings, and use an average of those grouped readings in the calculation algorithm.

The second feature is the addition of a calibration screen. At this point, the calibration screen is used by the administrator to capture readings and compare them to injected values, thus aiding the administrator to "tune" the controller in order to gain more accurate values. It is however envisaged that this calibration screen will in the near future be used to apply software calibration techniques in order to calibrate the system.

Tests were carried out on the controller to verify that the physical automation process operated as was required and designed to operate. Data accuracy and computation algorithms that formed the basis of the GUI were also tested.

The reader will be lead from the present Volt-Drop Test process to the overall design concept of the automated process and then to the more specific machine, software and electronic hardware design concepts. This finally leads to the discussion on the actual hardware, software and machine design that encompassed the specific considerations and factors that needed to be taken into account in order to implement the project practically. Each phase is discussed with reference to technical explanations, reasoning and decisions so that the reader may follow the entire design process from conceptualisation to testing.

This chapter illustrates the process to be automated. The theory of the Volt-Drop Test is briefly discussed along with the present test processes and the shortcomings thereof.

### 1.3 Background of the Volt-Drop test

The Volt-Drop test is carried out on armatures in order to test the integrity of the windings. This test is conducted on locomotive traction motors that have failed during operation and have been brought in for repairs. The Volt-Drop test is one of the first tests conducted after the motor has been stripped and cleaned. This test is also conducted prior to the armature being passed for assembly into the traction motor. The stator of the traction motor undergoes a different test and repair procedure.

The Volt-Drop test is a simple yet effective test. The effectiveness of the test however, depends on the accuracy of the test equipment. Very basically, the test entails the injection of a high current, via probes, to the commutator of the armature under test. The volt-drop across each pair of bars, hence across the winding that the bars are connected to, is measured and is compared to a reference value. The reference value is usually the volt-drop measured across the first pair of bars that were tested. If this comparison depicts a large percentage variation from the reference reading, the armature winding that is connected to that pair of bars, is either damaged, open circuited or short circuited.

The distinction between these three conditions is made evident by the value of the reading acquired for that pair of bars. Short circuited windings will be reflected by a potential difference reading that is very nearly zero volts whilst open circuited windings will be reflected as a potential difference reading that is equal to the potential of the supply test current (+15VDC maximum). Damaged windings will be reflected as a percentage variance from the reference reading. Typically any variance larger than $5 \%$ is considered by depot engineers as a reflection of a damaged winding. One should however note that if there are constant faults being recorded for each pair of bars after the pair on which the reference reading was taken, it is highly probable that the winding on the reference pair of bars itself was damaged. In this case, a new
reference reading is recorded on a different pair of bars. More detail into the present test process follows in the section below.

### 1.4 Present test program and short-comings

Presently, a trained technician carries out the volt-drop test. The author has observed two different test techniques at two test bays situated in different parts of the country. The first technique that was observed is as follows: The armature under test is placed on rollers and a test current of 350 Amps (max), is available to the commutator of the armature under test, via two current probes mounted roughly $30^{\circ}$ apart, on a semicircular frame. This current is applied to the commutator when a footswitch is pressed. At this point the technician holds two probes, one on each consecutive bar, and measures the potential difference or volt-drop between them. The variance from the reference reading, which is usually the first reading, if large, reflects a short circuit, open circuit or a damaged armature winding. The test instrument that measures the volt-drop variation is zeroed on the first pair of bars.


FIGURE 1-1: PRESENT TEST INSTRUMENT

This is now the reference value. On either side of the zero mark percentage variance markings are present. If the needle deflection on a pair of bars is within a chosen percentage variance, the pair is passed and the next pair is tested. If the needle deflection falls outside a chosen range that pair of bars is marked for further attention.

After the reading has been taken, the test current to the armature is switched of by releasing the footswitch, and the technician rotates the armature by hand to the next pair of consecutive bars. The process is then repeated until the voltage drops between all bars have been taken.

The second technique is similar to the first with the difference being that the test current probes are held onto an armature (also roughly $30^{\circ}$ apart) by means of a weighted band. This is a non-conductive band that is 3 cm wide with weights on either end. Once slung over the commutator the weights on the ends of the band allow for the current probes to be held firmly between the commutator and the band.

The current is switched on once and the readings are taken bar-to-bar using the same instrument mentioned above. The current is not switched off, the supply probes are simply moved from section to section until the entire commutator has been tested. This method is not recommended and is discouraged by company policies and safety regulations due to the possibility of electric shock if the supply current probes are not handled with care. The only reason the author can deduce for adopting this practice is that this method is considered easier to implement and is far less time consuming.

The figures that follow will give the reader a better understanding of the present test setup. Please note that the Commutator End Bearing and Front End Bearing are separate units which are fixed onto the armature shaft in order to enable rotation on the test stand. These bearings are not part of the armature and its motor assembly.


FIGURE 1-2: PRESENT TEST SET-UP


FIGURE 1-3: COMMUTATOR - TOP VIEW

In Figure 1-3, the reader will notice the distinct grooves between the commutator bars. This is due to a process called Undercutting. Not all commutators are undercut
before the volt-drop test, some commutators are simply turned in a lathe leaving the Epoxy Resin between the commutator bars. This makes no difference to the actual test however it is an important issue that has to be considered when choosing a sensor to detect the bars.


FIGURE 1-4: COMMUTATOR - FRONT VIEW

The shortcomings of these test methods become apparent when one considers the fact that some faults on the windings pass through undetected. There are two reasons for this. The first relating to the accuracy of the test instrument being used and the other is the manner in which the test is carried out by the technician. Due to a lack of test evidence, the tests are sometimes conducted in a haphazard manner. A further shortcoming of the present test is that there is no record created, soft or hard copy. A test history can therefore not be created. Further, this task is repetitive, uncomplicated, time consuming and leads to inefficient use of skilled staff.

## Chapter 2

## Project Concept and Overview

### 2.1 Design Objectives

The objective of the design of the controller for the Automated Volt-Drop Tester is twofold. The first aim is addressed by automating the test. This introduces cost effectiveness and reliability into the armature refurbishing process. The second aim is addressed through the capturing and storing of digital test data. Using this data, a history of an armature can be created and test technicians can be held accountable for overlooking the detected faults as the recorded test results, which reflects the name of the technician, serves as evidence. The overall accuracy of the system is also improved by the introduction of an electronic means of capturing volt-drop readings.

### 2.2 Project Scope

This project entailed the design of an Embedded Controller and a Graphic User Interface that controls the motion, inputs and outputs of a mechanical structure which enables the automation of a Volt-Drop Test as well as taking voltage readings that can be analysed, displayed and stored. The aforementioned controller consists of an embedded core i.e. a pair of microcontrollers, which analyse input data from the system and then prompts the appropriate output devices.

The interface between the system to be controlled and the embedded core is a digital system. This digital system was designed to condition signals before they are input to the microcontrollers. The digital system also provides the appropriate signals and voltage levels as inputs to drivers, drives and other output modules.

An analogue signal-conditioning module was also designed. The purpose of this module is to provide the input to the ADC with a volt-drop reading that is within its input range.
A Graphic User Interface (GUI) was designed to provide the controller with the required information, provide the user with a tool to monitor the system and test the
progress as well as a means to save data collected during tests. Visual Basic 6 was used to develop this GUI.

A Remote Graphic User Interface (RGUI) was also developed using Visual Basic 6.
The RGUI is installed on the desktops and laptops of authorised persons based anywhere in the country with access to the network. The GUI updates and creates records on the network. The RGUI enables a remote user to view records from any network position at any time.

The aim of this project was not to "redesign the wheel". Where components and modules are commercially available there is no need to design or develop them. These devices have been researched, designed, built and tested by leaders in the specific field. Their reliability has been proven in industry. It is therefore logical and costeffective to incorporate these modules into the system as it will add to the reliability of the system and reduce cost as time and money would have to be invested in the research, design, building and testing of these modules.

The control of motors, in terms of speed and soft-starting, is not within the scope of this project and will be accomplished by drives that are readily available as off-theshelf units. The design of drivers for IGBTs is also not within the scope of this project. IGBT drivers are commercially available and are recommended for, or matched with, specific IGBTs based on the device rating and application.

### 2.3 Design Concept

The design concept will be discussed under two more specific headings, namely, the Automation and Machine Design Concept and the Data Acquisition Concept.

### 2.3.1 Automation and Machine Design Concept



FIGURE 2-1: SYSTEM BLOCK DIAGRAM

In order to design an efficient machine and controller that carries out all the operations required to perform the test, time had to be spent in the test bay observing and conducting tests. It was noted that in terms of basic operation, the armature under test had to be rotated, the commutator bars had to be detected, the test probes had to be lowered and raised, the test current supply had to be switched and the reading analysed. For the design of the automated system, which includes the test machine (physical test station) and controller, each of these tasks had to be accomplished using transducers, actuators, electronic hardware systems or software.

In this system a PC or Laptop that interfaces with the controller runs software that provides a Graphic User Interface (GUI) to the system. The test and test machine can be controlled via the interface. The interface displays the test status, faults logged and system errors when they occur. The GUI also performs analysis and storage of data. Analysis and storage of data will be discussed under the heading Data Acquisition Concept. The figures that follow are aimed to aid the reader in the understanding of the mechanical design concept for the Physical Test Station. These figures do not reflect the final design as different, more economical and robust approaches were
taken by the manufacturer, however, the concept remains the same. These are the original sketches that were presented to mechanical engineering companies in order to describe the system that was required.

The mechanical system is designed to operate as follows under the control of the embedded controller and GUI. A test has to be set-up by the test technician. The technician ensures that the armature to be tested is lowered into the correct position using an overhead crane. Once the armature is in position the test technician lowers the Test Current Probes onto the surface of the armature ensuring that the Test Current Probes are roughly $30^{\circ}$ apart. See Figure 2-5 for a front view sketch of the Test Current Probes.

The Test Current Probes are the probes from which the Test Current is injected though the armature under test via an IGBT. The IGBT is used to switch the Test Current. The Test Current Probes are lowered onto the commutator and are fixed into place at the start of the test and are in no way attached to the Detection Unit. These probes are never raised off the surface of the commutator at any time during the test. Once the Test Current Probes are fixed into place, the technician must position the Detection Unit such that two consecutive bars are detected. See Figure 2-6C and Figure 2-6D. The detection of the bars on the commutator is accomplished through the use of an optical detection sensor unit.

The optical sensor operates on the principal of emission and reflection. A laser beam is emitted onto a surface by the unit and the reflection is detected by an optical sensor on the same unit. These optical sensors, together with the spring mounted test probes (see Figure 2-6A) form the Probe and Sensor Unit as shown in Figure 2-6B. The Detection Unit Head comprises of one fixed Probe and Sensor Unit and one sliding Probe and Sensor Unit as shown in Figure 2-6C. The Detection Unit is set up such that two consecutive bars are detected by lowering the unit to the surface of the bars, typically between 50 mm and 70 mm above the surface of the bars, and ensuring that the fixed Probe and Sensor Unit detects a bar. This is indicated by the green LED on the optical sensor switching on. This is a built-in feature on the optical unit. Once this occurs the sliding Probe and Sensor Unit is slid into position above the immediate next bar until the green LED on that optical sensor is also switched on. Once this has
occurred the sliding Probe and Sensor Unit is fixed into position using the wing-nut as shown in Figure 2-6C and Figure 2-6D. The Detection Unit Head is then raised to its original position by the test technician.

Once the set-up has been completed the technician begins the test using the GUI. The armature under test is then rotated by the Armature Drive Motor via a gear drive system until the next pair of bars has been detected. See Figure 2-2. When a pair of bars has been detected, the Armature Drive Motor is stopped and the armature is locked into place using a solenoid in the gear drive unit. The signal to the solenoid driver that allows for the energising and de-energising of the solenoid is the same as the signal used to stop and start the Armature Drive Motor via the Armature Drive Motor drive. Note that this gear drive unit is to be designed by the mechanical engineering company that was awarded the tender to design the mechanical system.

Once the armature under test has been locked into place the test current is switched on via an IGBT and the Detection Unit Head is lowered onto the surface of the commutator bars via the Detection Unit Drive Motor and the Mechanical Linear Setup which incorporates a mechanical power thread/screw [13] system much like that used in a mechanical press as shown in Figure 2-3 and Figure 2-4. The Detection Unit Drive Motor rotates, lowering the Detection Unit Head until both the spring mounted Test Probes are on the surface of the bars with sufficient pressure. This is indicated by the mechanical switches that are "Made" when the test probes are on the bars. See Figure 2-6A. Once this is signaled, the Detection Unit Drive Motor is stopped and the Detection Unit Head is held in position by the mechanical power thread which is designed not to allow movement unless it is being rotated.

Test readings can now be taken on this pair of bars. Once the reading has been completed, as signaled by the GUI, the Detection Unit is raised by rotating the Detection Unit Drive Motor in the opposite direction. The Detection Unit is raised to its original position, which is signaled by the mechanical switches on the Mechanical Linear Setup as shown in Figure 2-3 and Figure 2-4, and the Test Current is switched off. This marks the end of one test cycle. To begin the next test cycle on the next pair of bars the controller waits for a prompt from the GUI. Upon receiving this prompt the solenoid in the gear drive unit is de-energised thus unlocking the armature under
test and the armature is rotated by the Armature Drive Motor until the next pair of bars has been detected. This continues until the last pair of bars has been tested. Note that future references to the stopping of the Armature Drive Motor will imply both the signal to stop the Armature Drive Motor and the locking of the armature under test. Future references to the starting, prompting or rotating of the Armature Drive Motor will imply both the signal to start the Armature Drive Motor and the unlocking of the armature under test.

Initially mechanical switches were to be used on the Mechanical Linear Setup and on the spring mounted Test Probes to indicate position of the Detection Unit Head and the state of the Test Probes respectively. However, seeing as these applications entail a high number of repetitive on-off transitions when monitoring the position of the Test Probes and the initial position of the Detection Unit, the mechanical switches were replaced by non-contact inductive proximity switches. This was done because mechanical switches entail the physical "making" and "breaking" of metal alloy contacts and due to the high number of transitions, these contacts will wear after short periods thereby reducing the lifetime of the mechanical switch to much lower than that of non-contact switches. This is discussed further in Section 5.1.4 and Section 5.1.5. Due to the cost of the inductive proximity switches, one switch instead of the two depicted in Figure 2-3 is used to detect when the Detection Unit has returned to its initial position. Although the type of switch has been changed from those reflected in the sketches provided, the principle purpose and positioning of the switches remain the same.


FIGURE 2-2: SKETCH OF TEST SETUP [LEFT VIEW]


FIGURE 2-3: SKETCH OF MECHANICAL LINEAR SETUP [FRONT VIEW]


FIGURE 2-4: SKETCH OF MECHANICAL LINEAR SETUP [LEFT VIEW]

The switches shown in Figure 2-3 and Figure 2-4 indicate when the Detection Unit Head has been returned (is raised) to its original position. The switch shown in Figure 2-6A indicates when the Test Probes are resting on the pair of bars under test with adequate pressure as supplied by the compressed spring.


FIGURE 2-5: SKETCH OF TEST CURRENT PROBES [FRONT VIEW]


FIGURE 2-6A: SKETCH OF SPRING LOADED TEST PROBES [LEFT VIEW]


FIGURE 2-6B: SKETCH OF PROBE \& SENSOR UNIT [FRONT VIEW]


FIGURE 2-6C: SKETCH OF THE COMPLETE DETECTION UNIT HEAD [TOP VIEW]


FIGURE 2-6D: SKETCH OF THE COMPLETE DETECTION UNIT HEAD (ABOVE A PAIR OF COPPER BARS) [TOP VIEW]

Given that this machine has to perform specific tasks at certain times, an algorithm was developed to facilitate smooth and accurate task execution. The said tasks are based on information received from three sources: the machine itself, the controller and the Graphic User Interface. In order to better understand the above-mentioned algorithm, the discussion that follows will describe the Graphic User Interface and controller and their roles in the system.

The controller core consists of a pair of embedded microcontrollers that interface with a digital system and an analogue system. Each of these two microcontrollers has a specific role. One microcontroller is tasked with the automation procedures and is aptly named the Automation Microcontroller (AM) whilst the other is tasked with data acquisition and communication with the GUI, and is called the Communications Microcontroller (CM). These two microcontrollers communicate with each other via a port-to-port parallel bus.

The CM communicates with the GUI via a serial link, where the UART of microcontroller is interfaced with the serial port of a PC or Laptop. The test technician completes the GUI data fields. Using this information, the GUI analyses the input data and calculates and displays the test status. The relevant information is then transmitted to the CM, which in turn communicates with the AM. Information is also transmitted in the opposite direction, from the AM to the CM to the GUI. The system is designed to operate in one of two modes: Automated or Manual.

In Automated mode, the mechanical system is controlled by the controller via the AM. In Manual mode, the automation functionality is disabled and the CM and GUI are used to capture, analyse and record readings. The operation of the GUI and the controller is discussed in detail in Chapters 3 and 4 respectively. Figure 2-7 presents the flow chart that describes the basic operation of the test machine.



FIGURE 2-7: BASIC SYSTEM FLOW CHART

Errors 1, 2, 3 and 4 are the result of undesired events occurring in the system during operation. When any one of these errors occurs the AM enters the relevant subroutine and informs the CM which then also enters its relevant subroutine. The CM in turn informs the GUI of the error so that it is reflected on the interface.

Errorl occurs when a pair of bars is not detected by the optical sensors within a specified time. This time is calculated by recalling the time taken for the detection of the previous pair of bars and adding an additional twenty percent of this previously recorded time.

Error2 occurs when the test probes are not present on the surface of the commutator within a pre-selected default time. This occurs when the switches shown in Figure 26A and Figure 2-6B are not "made" within the default time.

Error3 occurs when the test current is not switched off before a pre-selected default time has expired. If the period of time measured from the instant that the microcontroller pulses the IGBT driver to switch on the Test Current, till the instant that the microcontroller pulses the IGBT driver to switch off the Test Current, is greater than the default time, Error3 will be signaled. This condition is monitored by the Test Current On-Time Timing Module which is discussed in Chapter 5.

Error4 occurs when the test probes are not raised to their original position within a specified time. This time is calculated by recalling the time taken to lower the test probes onto the surface of the commutator and adding an additional twenty percent of this previously recorded time. The switches shown in Figure 2-3 and Figure 2-4 indicate when the Detection Unit has returned (is raised) to its original position

### 2.3.2 Data Acquisition Concept

The input module that measures the volt-drop across each pair of bars is made up of three distinctive sub-modules. These are the Input Instrumentation Amplifier, Signal conditioning and the Analogue to Digital Conversion. The Analogue to Digital Converter that was chosen has a resolution of sixteen bits and an eight bit parallel output bus that interfaces with an eight bit input port on the CM. The sixteen-bit word is saved as two bytes (high byte and low byte) in allocated registers in the CM. These two bytes are then transmitted to the GUI where it is analysed. Analysis comprises the conversion of the received data into the correct data type and then using this value, the actual volt-drop reading is calculated. This calculated volt-drop reading is then compared to the reference value and if the variation is greater than the pre-selected percentage variance on the GUI, a fault is recorded. Based on the results of the analysis, the GUI either records the reading as a fault or signals the AM via the CM to continue to the next pair of bars. The GUI allows the user to set the following properties before a test can commence

- Select the type of armature to be tested
- The allowable percentage variance from the reference value and
- The destination on the hard drive, or network where the recorded data is to be saved.

The RGUI allows for authorised persons to view records from remote locations, provided that there is access to the network. The capturing of data and the analysis thereof is covered in detail in Chapters 3, 4 and 5.

### 2.4 System Advantages and Features

This system will address the problem of inaccurate readings and the lack of recorded data and armature test history. The fact that the system is automated allows for skilled staff to be deployed in critical areas while the tests are being conducted. Looking ahead, if multiple units are built and placed in test bays, more than one test can be carried out at the same time with one member of staff overseeing the entire process.

Below the reader will find a list of the system's main features.

- User name and password
- Administrator name and password
- Lockout
- Armature serial number (Job number)
- Time and date of test
- Duration of test
- Automated operation - Motion, bar detection, test current switching and data acquisition are governed by the controller
- Manual operation - Physical motion, bar detection and test current switching are controlled by the test technician. Data is acquired automatically when prompted by the test technician
- Error indication
- Printout of all recorded faults
- Addition of new armatures settings (only administrator)
- Addition of new percentage variance settings (only administrator)
- Set new destination for data files (only administrator)
- Emergency stop
- Test history for armatures (Save and View test files)
- Bar under test
- Number of bars remaining
- Number of faults logged
- Delete files (only administrator)
- Record reference value
- Data analysis and processing
- Fault display
- Test status
- Reference value reset
- Test status reset on reference value reset.
- Remote Graphic User Interface (RGUI) to view records from remote locations.
- Additional Features
- The ability to automatically take repetitive readings on a single pair of bars
- Automatically record each reading and the average of all the readings for a pair of bars on an Excel Spreadsheet. Also automatically save Excel Spreadsheets at the end of tests.
- Calibration of the system using the GUI.
- Multiple, unique user names and passwords
- SuperUser name and password


## Chapter 3

## Graphic User Interface (GUI) Development

The GUI provides a means to control the automated machine as well as a means to capture, analyse and store data. See Appendix A for a screen capture of the GUI and Appendix C for the complete GUI source code. Also see Appendix P for a detailed discussion including flow diagrams and code extracts. In order to perform the above two functions, reliable communication between the GUI and the Controller is imperative. As previously mentioned, the GUI communicates directly with the Communication Microcontroller (CM) which then in turn communicates with the Automation Microcontroller (AM).


FIGURE 3-1: SYSTEM BLOCK DIAGRAM

In order to understand the function of the GUI, the communication between GUI and the CM has to first be discussed.

The GUI and the CM communicate serially using their respective serial ports which are setup to interact as required. In this chapter the author will discuss how data is processed from the point at which it is present in the GUI serial buffer and the prompts transmitted by the GUI to the controller, more specifically, the CM.

The interface between the GUI and the serial port (RS232) of a PC or Laptop using the Visual Basic 6 development environment is the MSComm component. Once enabled the properties of the MSComm component have to be set so that they mirror the settings for the CM serial port.

### 3.1 A walk through the GUI

The aim of this walk through is to lead the reader through the features, functions and code behind the Graphic User Interface. Screen captures will help the reader to understand how the GUI responds to user prompts and data that is received. See Appendix A for a true representation of the GUI and Appendix O for a GUI PowerPoint Presentation. The GUI is divided into two separate parts, one being the Test Setup Fields and the other being the Test In Progress Fields. Each of these will be discussed individually in the sections that follow.

### 3.1. Test Setup Fields

### 3.1.1.1 User Identification Frame

The input fields in this section are used to setup the system for the specific armature that is to be tested. The User Identification frame is the location in which the details of the staff member performing the test are entered.


FIGURE 3-2: INITIAL TEST SCREEN


FIGURE 3-3: USER IDENTIFICATION FRAME ON THE INITIAL TEST SCREEN

Initially, except for the New Test button encircled in Figure 3-2, all the buttons and text input boxes are disabled. On clicking the New Test button in the Password frame the Enter button is enabled and replaces the New Test button. See Figure 3-4.


FIGURE 3-4: INITIATE TEST SCREEN


FIGURE 3-5: USER IDENTIFICATION FRAME ON THE INITIATE TEST SCREEN
At this stage, except for the Enter button, all other control buttons are disabled and except for the Password text input box all the text input boxes are still disabled. To enable the GUI the correct user password has to be entered. This password was originally a generic password that was assigned to the system. Any staff member that was assigned to use this system was to use this password. This has subsequently been changed such that each user has a unique username and password that is chosen by
the individual. The username and password is stored in a file on the PC or laptop hard-drive and is accessed and/or edited via the GUI whenever need be.

The login system requires that the password is entered in order to use the system. If the password is one that exists in the Username and Password file, the username that is associated with the entered password is displayed in the Name text box. This method is used to ensure accountability as the username displayed in the Name text box is the name that is printed in the test report and saved in the test history file. The username and password feature is discussed in detail in Chapter 6 under the heading, Multiple User Names and Passwords.

On entering the incorrect password GUI informs the user that the password is incorrect as well as the number of attempts that remain. See Figure 3-6A and Figure 3-6B.


FIGURE 3-6A: GUI REPRESENTATION WHEN AN INCORRECT PASSWORD HAD BEEN ENTERED


## FIGURE 3-6B: MESSAGE BOX INFORMING THE USER OF THE NUMBER OF TRIES THAT REMAIN

If, on the third attempt, an incorrect password is entered the message box depicted in Figure 3-7A appears informing the user that he/she is about to be locked out by the system.


FIGURE 3-7A: MESSAGE BOX INFORMING THE USER THAT HE/SHE HAS BEEN LOCKED OUT

On acknowledgement of this message (by clicking on the OK button) the Lock Out frame is activated. The Lock Out frame hides every input and output function of the GUI, except for the Administrator Password functionality. See Figure 3-7B. The administrator password is used by a member of staff that is responsible for the supervision of the tests as well as the test technicians. This password allows the administrator to access and edit properties such as the Armature Properties, Test Parameters, Directory path and Unlocking. A user with a basic user password does not have the ability to edit these properties. Note that only the administrator can unlock the system once it has been locked.


FIGURE 3-7B: LOCK OUT SCREEN

### 3.1.1.2 Armature Properties Frame

It is here that the user selects the armature type that is to be tested. See Figure 3-7C.


FIGURE 3-7C: ARMATURE PROPERTIES FRAME

The list of armatures is created by completing the New Armature Name and Number of Commutator Bars field and then clicking on the Add New Armature button. As mentioned previously, this functionality is only available to the administrator, therefore upon clicking the above mentioned button, the user is asked for the
administrator password before the new armature is added, see Figure 3-8 and Figure 3-9. If an incorrect password is entered the new armature will not be added. For the removal of armatures from the list the Click To Remove Highlighted Armature functionality is used and is a functionality only available to the administrator. The reason for limiting access to these property fields is to exercise control over the test system. The user may only use the system and may not define any test limits and conditions other than those available to him/her.


FIGURE 3-8: ADMINISTRATOR'S PASSWORD PROMPT


FIGURE 3-9: GUI DISPLAYING THE ADMINISTRATOR'S PASSWORD PROMPT

All armatures that appear on the list are stored in a sequential file. This sequential file is accessed and/or edited when creating the list of armatures that are to be tested, adding a new armature to an existing list or deleting an armature from the list.

The destination to which this file is saved is determined by Default Path. This path is specified in the Directory Path frame which will be discussed later in this chapter. The name of the file is Arm.

### 3.1.1.3 Job Number Property Frame



FIGURE 3-10: JOB NUMBER PROPERTY INPUT FRAME

It is in this input box that the armature serial number is entered. This serial number is reflected in the test report printout and it is also used as a file name under which the test results are saved. As will be discussed later in this chapter, tests are saved in files bearing the serial numbers of armatures as filenames in order to generate a test history for each armature. When a test is carried out on an armature with a file name (serial number) which does not appear in the file containing the list of armatures that were previously tested, that armature is added to the saved list, i.e. its serial number is added to a sequential file named 'Saved_List'.

A sequential file bearing the name of the serial number of the armature is also created and it is here that the test results are saved. When saving a test for an armature with a serial number that already exists the content of the Job Number Property frame is compared with the list of serial numbers in the 'Saved_List' file. When a match is found that file is opened and the present test details are added to it. If no match is found then a new file is created and the name of the file is added to the 'Saved_List' file.

### 3.1.1.4 Test Option Property Frame



FIGURE 3-11: TEST OPTION PROPERTY FRAME

This property frame allows the user to choose between Automated and Manual modes by selecting the appropriate option. Once a selection is made it is reflected in the Test Status property frame, as show on Figure 3-12 below.


FIGURE 3-12: TEST STATUS PROPERTY FRAME

In Automated mode the entire system is enabled. This means that the controller, more specifically the Automation Microcontroller (AM), controls the mechanical system according to the commands from the GUI and the Communication Microcontroller (CM). In Manual mode, the automated control functionality of the system is disabled and the AM enters power-down mode. Only the data acquisition, analysis and storage functionalities of the system are available to the user. In this mode, the test technician is responsible for placing the test probes on the commutator bars and switching the test current using a footswitch.

### 3.1.1.5 Test Parameter Property Frame



FIGURE 3-13: TEST PARAMETER PROPERTY FRAME

The Parameter Property Frame is where the user stipulates the allowable percentage variance (i.e. percentage difference) of present reading from the reference reading. This value is then stored in variable Percentage to be used in the Calculation subprogram. Different ranges can be added and removed from the available options by the administrator in exactly the same was way as the Armature Properties Frame. The operation of this frame is identical to that of Armature Properties Frame therefore the author will not enter into a discussion on the operation of this frame.

### 3.1.1.6 The Date and Time Frames



FIGURE 3-14: DATE AND TIME PROPERTY FRAME

These output fields reflect the date and duration of the test. On starting the test, by clicking the Start button, the date and the current time (Test Started) is uploaded from the PC's internal clock.

When a test ends, either naturally (when all the bars have been tested) or unnaturally (when an emergency stop has been invoked), the end time of the test (Test Ended) is uploaded from the PC's internal clock.

### 3.1.2 Test In Progress Fields

### 3.1.2.1 Fault Log List

The Fault Log list is a list that displays each reading that falls outside the specified percentage variance range. It is also the screen that is used to display all relevant test information and test history that is retrieved from stored files.


FIGURE 3-15A: THE FAULT LOG SCREEN DISPLAYING PRESENT TEST FAULTS

Figure 3-15A depicts a typical test fault log. This is what the user will see during the test as faults are recorded. Figure 3-15B illustrates the same test results that have been recalled from a stored file.
Job Number: Test Results
ercentage Variance: 5\%
Date: 2006/04/12
Recorded Faults
Fault on Bar: 3. Percentage Variance $=19.28123$. Bar Reading: 0.1626973 V . Reference: 0.136398 V
Fault on Bar: 5, Percentage Variance $=10.88503$, Bar Reading: 0.1215511 V. Reference: 0.136398 V
Fault on Bar: 7. Percentage Variance $=10.3879$, Bar Reading: 0.1505669 V , Reference: 0.136398 V
Fault on Bar: 8, Volt-Drop Reading Is Zero ( 0 V ) . Indicating A Possible Short Circuit
Fault on Bar: 9, Volt-Drop Reading Is Out Of Range, Indicating A Possible Open Circuit
Emergency Stop on Bar 10
End Of Recorded Results

FIGURE 3-15B: THE FAULT LOG SCREEN DISPLAYING RETRIEVED FILE DATA

Figure 3-15B depicts a saved test that has been recalled in order to view the stored results. Critical information such as the job (serial) number, the operators name, the type of armature (the armature name and the number of bars on the commutator), the allowable percentage variance and the date of the test are displayed.

Under 'Recorded Faults', each fault is recorded with the following information: the number of the pair of bars on which the fault was recorded, the percentage variance from the reference reading, the actual volt-drop reading across the present two bars, the actual reference reading and, in the event of an emergency stop, the pair of bars on which such a stop was initiated.

### 3.1.3 The Control Commands

The control commands are used to prompt the controller, and where necessary the automated machine, to react to a user initiated event. There are three controls that may be used under normal test conditions when none of the system errors have occurred. These are the Load/Start, End and the Emergency Stop controls as shown in Figure 316.


FIGURE 3-16: CONTROLS FOR NORMAL TEST CONDITIONS
In the event of an error, the two controls to be used are the Continue After Error Pause and the Manual Reading as shown in Figure 3-17A and Figure 3-17B. On an error that requires a manual reading to be taken, i.e. Error1 and Error2, the Manual Reading Control is enabled and the Reading Prompt turns green. A red Reading Prompt alerts the user that the system is not ready to take a manual reading whilst a green setting indicates to the user that the system has been prepared for a manual reading procedure. The user clicks on the Manual Reading button on the GUI when the reading is about to be taken. Thereafter the user presses a Manual Reading switch situated on the automated machine after the test current is switched on and the test probes are set in place. The volt-drop reading is then captured and processed.


FIGURE 3-17A: DISABLED MANUAL READING CONTROL


FIGURE 3-17B: ENABLED MANUAL READING CONTROL

Referring to Figure 3-16, the reader will notice that the first button in the Controls frame is the Load button and all other control buttons are disabled. This is to ensure that all the data required for a test has been entered correctly in the Test Setup Fields as discussed earlier.

Once all the data has been entered the Load button is clicked to upload the applicable information to the controller (more specifically the Communications Microcontroller). All the input data fields on the GUI are disabled when the Load button is clicked in order to ensure that the input setting can not be altered during a test. If any input data fields have not been completed when the Load button is clicked a message box or an input box appears prompting the user to enter the required data. See Appendix $P$ the flow diagram relating to this process. Once the CM has received the information it acknowledges having done so by transmitting the ASCII code for the letter 'd' back to the GUI.

On receiving this, the Load button is replaced by the Start Button and the Emergency Stop Button is enabled as depicted in Figure 3-18B. When the user is ready to begin the test the Start button is clicked and ' A ' is transmitted to the controller to begin. When the Start button is clicked it turns green, as shown in Figure 3-18C, and the mouse pointer changes to a pointer and hourglass signifying that the test is in progress.


FIGURE 3-18B: START AND EMERGENCY STOP CONTROL ENABLED


FIGURE 3-18C: START CONTROL BUTTON CLICKED TO BEGIN TEST

After the last pair of bars has been tested the End control button is highlighted in blue as shown in Figure 3-19A below. This alerts the user that the test is complete. The user must acknowledge this alert by clicking on the End button. The End control is also enabled and highlighted when an Emergency Stop is initiated. This is further discussed below.


FIGURE 3-19A: END CONTROL HIGHLIGHTED BLUE TO ALERT USER

When the End control button is clicked, ' B ' is transmitted to the controller and the End button is highlighted in green to signify the completion of the test. This signifies that the controller has entered powerdown mode and that the data is ready to be printed and saved or only saved. Referring to Figure 3-19B, the reader will notice that the Print and Save options are now enabled. All the output fields in the Test Status Frame and all the input fields in the Test Setup Frame are cleared. Further, all control and input buttons, except for the password Enter Button, are disabled. This allows the user to begin the next test once a valid password has been entered.


FIGURE 3-19B: END CONTROL HIGHLIGHTED GREEN AFTER ALERT IS ACKNOWLEDGED

When the detection unit, containing the test probes and optical sensor, is not raised to its initial position within the allocated time Error 4 is invoked and the Continue After Error Pause control, The Emergency Stop control as well as the Error 4 status display are enabled and highlighted as depicted in Figure 3-20.

The GUI is made aware of this error when the ASCII code for the letter ' $L$ ' is received. When this error occurs the user has to assess the problem and if the fault is not serious enough to abandon the test, the user will physically raise the unit to its initial position. Once this is done and the user is confident that the error was not due to an event that may be recurring, the user will click on the Continue After Error Pause control for the test to progress as usual. Once clicked all the control buttons and displays that were highlighted and enabled due to the error are disabled and are no longer highlighted. If the fault is deemed to be serious and possibly recurring in nature the user will then click on the highlighted Emergency Stop control to immediately stop the test.


FIGURE 3-20: CONTINUE AFTER ERROR PAUSE CONTROL ENABLED FOR ERROR 4

The last control featured in the Controls frame is the Emergency Stop button. This functionality is enabled as soon as the test is started and remains enabled throughout the test. If at any point during the test, the user decides that it is unsafe to continue with the test, an emergency stop can be evoked by clicking on the Emergency Stop control button. When clicked, the Emergency Stop control is highlighted in red, the End button is enabled and the ASCII code for the Letter ' F ' is transmitted from the GUI to the CM. The CM then Sets (1) P0.5, which is connected to the AM P1.5 and P3.2 (External Interrupt 0). When the AM is interrupted due to External Interrupt 0 being triggered and P1.5 is High (1), the AM immediately initiates an emergency stop. The AM immediately halts the task that was being carried out, switches off the Test Current by Clearing (0) P2.7 and safely shuts the system down before entering Powerdown mode. The GUI reflects the fact that an Emergency Stop was evoked in the Fault Log and waits for the user to click the End button in order to end the present test.


## FIGURE 3-21: EMERGENCY STOP EVOKED

### 3.1.4 Error Status Frame

The Error Status Frame is where errors are reflected as or when they occur. When no errors have occurred, the frame looks like Figure 3-22, with each error status display being disabled.


FIGURE 3-22: ERROR STATUS FRAME

When an error does occur the appropriate display is highlighted red and is enabled. Once the user clicks on the error a display message box pops up informing the user of the type of error, the cause and possible steps to follow. Only once the error has been corrected and the controller communicates this to the GUI, will the highlighted display be disabled. Each error and flow chart depicting the steps taken when they occur will be discussed in detail in Chapter 4 and Appendix Q. For the purposes of this discussion, the author will only concentrate on those events which trigger these errors and the manner in which the GUI reflects them.

Error 1 occurs when a pair of bars is not detected within an allocated time. The controller is responsible for the timing of this process and if the allocated time has
elapsed before the next pair of bars are detected, the controller transmits the ASCII code for the letter ' J ' to the GUI. When the GUI receives a ' J ' it immediately enables and highlights the Error 1 display as well as the Manual reading control. As mentioned earlier, a detailed discussion concerning this and all the other errors will follow in Chapter 4. See Figure 3-23A for a representation of the Error 1 display. When the Error 1 display is clicked the following message appears in a message box:
"The next pair of bars has not been detected within the allowable period. A Manual Reading must now be taken"


FIGURE 3-23A: ERROR 1 DISPLAY
Error 2 occurs when the detection unit has not been lowered onto the surface of the commutator within the allowable time. Here again the controller is responsible for the timing of this process and if the allocated time has elapsed before the detection unit has been lowered the controller transmits the ASCII code for the letter ' $m$ ' to the GUI. On receiving this character the GUI highlights Error 2 and enables the Manual reading control.


FIGURE 3-23B: ERROR 2 DISPLAY

When the Error 2 display is clicked the following message appears in a message box:
"The Test Probes have not been lowered within the allowable period. A Manual Reading must now be taken"

Error 3 occurs when the test current is switched on for a period longer than the predetermined allowable time. In this case the controller transmits the ASCII code for the letter 'L' to the GUI. Unlike the previous two errors, Error 3 initiates an immediate Emergency Stop (by transmitting the ASCII code for the letter ' $F$ ' to the controller) and enables the End control function. The GUI still however highlights Error 3 in order to inform the user that the Emergency Stop was initiated as a result of the occurrence of Error 3. On clicking the Error 3 display the following message appears in a message box:
"The Test Current has been switched on for too long, and as a safety measure an Emergency Stop has been invoked. Please Click End, check the device and Restart the Test"


FIGURE 3-23C: ERROR 3 DISPLAY AND INVOKED EMERGENCY STOP

Error 4 was discussed in the explanation pertaining to the Continue After Error Pause Control, however for completeness it has been discussed briefly below.

Error 4 occurs when the detection unit has not been raised to its initial position within the allowable time. When this occurs the controller transmits the ASCII code for the letter 'Q' to the GUI. On receiving this the GUI highlights and enables the Error 4 display as well as the Continue After Error Pause and Emergency Stop controls as shown in Figure 3-20 and Figure 3-24. The user then assesses the fault and elects to either continue with the test by clicking on the Continue After Error Pause button or stopping the test by clicking on the Emergency Stop button.


FIGURE 3-24: CONTINUE AFTER ERROR PAUSE CONTROL ENABLED FOR ERROR 4

### 3.1.5 Test Status Display

The Status Display is responsible for the summary of the present test at any point during the test. As can be seen from Figure 3-25, the information displayed includes the number of the pair of bars (i.e. first pair, second pair etc) that is currently under test, the number of pairs of bars that remains to be tested, the number of faults that were logged, the mode that the system is operating in (i.e. manual or automated) and the task that the system is presently performing (i.e. either searching for the next pair of bars or taking a reading).


FIGURE 3-25: TEST STATUS DISPLAY

### 3.1.6 Recorded Test Data Option

The user has four options relating to the handling of recorded test data. These are the print, save, open and delete options. Each will be discussed individually in the subsections that follow. Below is a representation of the options available at different stages of the process.

Figure 3-26A depicts the options available after the correct password is entered but before a test has started. Figure 3-26B depicts the options available while a test is in progress and Figure 3-26C depicts the options available at the end of a test.


FIGURE 3-26: TEST DATA OPTIONS

### 3.1.6.1 Print Option

A printed test report is useful for three reasons. Firstly, a hard copy of a specific test or a test history of an individual armature can be made available. The second reason is that a written record travels with the armature after this test so that staff involved at the next stage of the process will have access to the results. The third use of a printed test report is that it aids in accountability, i.e. the technician that performs the test can be held accountable for the test and the results since his/her name appears on the test report as well as his/her signature acknowledging the faults.

The user may view and print saved test records by opening a specified file using the Open button. It is for this reason that the print option is made available to the user after the correct password is entered but before a test is started. When Print is clicked, all the data contained in the opened file is printed in the format shown in Appendix D. If a file was not opened, thus implying that no data is displayed when Print is clicked, the following message appears:
"No Data Available To Print"
Once a test is in progress the print option is disabled until the end of the test. Here, when Print is clicked, only the data recorded during the test which was just completed is printed in the format shown in Appendix E. One of the main features of this new system is the fact that test data can be printed and stored. It is for this reason that when the user prints the present test the data is also automatically saved in the appropriate file.

### 3.1.6.2 Save Option

As mentioned above, when a completed test is printed it is also automatically saved therefore there is no need to click on the Save button. The Save button is useful when the user wishes to only save the present test data without printing a copy.

A dual sequential file system is used to save a test record. The first sequential file is the one used to store the names or serial numbers of the armatures that have been tested and saved, in order to generate a list when required. This file is named

DefaultPath \& 'Saved_List.TXT"'. DefaultPath is the specified location of the file named Saved_List. The above-mentioned list is available when the user clicks on the Open or Delete buttons.

The second sequential file is the one in which the test data is saved. The file name is the serial number of the armature under test. Each record added to this file has the following fields: the serial number of the armature, the name of the test technician, the type of armature, the allowable percentage variance specified for the test, the date of the test and recorded faults (if any) read by incrementing the index number of the Fault Log list and the actual fault logged on that pair of bars. In other words, each fault recorded on the Fault Log list is saved in the file with the test parameters and identification data fields preceding it. A typical record in the file is found below,
"matadin","sun 04/05","Armature Name: f Number of Bars: 50","Percentage Variance: 20\%","2005/05/04","Emergency Stop on Bar 0"

Once the last item from the Fault Log has been saved, a record containing 'xxx' in the user name, armature name and allowable percentage variance fields together with the serial number field is saved to indicate the end of a test record.

> "End","xxx","xxx","xxx","2005/05/04","End Of Recorded Results"

### 3.1.6.3 Open option

This option is only available to the user once a valid password has been entered. By clicking on Open, the user may view any and all saved tests. When clicked an input box, as shown in Figure 3-27, appears prompting the user to enter the serial number of the armature for which the test data is to be viewed. When this number has been entered all the recorded tests for that serial number i.e. the armature test history, are displayed on the Fault Log display.


FIGURE 3-27: INPUT PROMPT WHEN 'OPEN’ IS CLICKED

In order to refine the search, for example if a test on a specific date is required, the user enters 'Find' in the input box. A list of armature serial numbers appears as shown in Figure 3-28. This list is generated by reading the 'Save_List' file mentioned above.


FIGURE 3-28: LIST OF SAVED SERIAL NUMBERS
By clicking on a serial number from this list a search is initiated. This search entails the opening of the file with the name matching the selected serial number, in this case matadin, reading through each record and displaying the dates on which tests were carried out on the selected armature. All these dates along with a 'View All' option are displayed in a list box as depicted in Figure 3-29.

By selecting a specific date, the user may view the data recorded during the test (or tests) carried out on that armature on the specified date. By clicking on the 'View All' option a test history containing all tests recorded and saved under the specified serial
number is displayed. The user clicks on the Exit button provided to exit from the Open procedure at any time.


FIGURE 3-29: LIST OF TEST DATES FOR A SPECIFIED ARMATURE SERIAL NUMBER

### 3.1.6.4 Delete Option

The delete option allows a user with administrative rights to delete a file with a specified serial number. When an armature is discarded it may be decided that the history of that armature is no longer relevant however, the opposite may also be true. The relevance of the history of a discarded armature can only be decided by the workshop management and maintenance engineers.

The Delete option works in the same way as the Open option. All the records with the specified serial number are located when that serial number is entered into the input box prompt or a list containing all the saved serial numbers is generated when "Find" is entered into the input box as depicted in Figure 3-30. The difference is when the Delete button is clicked - the GUI requests the Administrator's password. If the password is entered correctly and a serial number is selected the GUI will ensure that the user is sure of his decision by prompting a response using a pop up box as shown in Figure 3-31.


FIGURE 3-30: LIST OF SERIAL NUMBERS GENERATED ON THE DELETE CLICK EVENT


FIGURE 3-31: POP UP PROMPT ON SELECTING AN ITEM TO BE DELETED

If Yes is selected by the user the deletion process is initiated. This process entails the removal of the selected serial number from the sequential file that generates the list of saved serial numbers, i.e. 'Saved_List.TXT", as well as removing the file that contains the test history saved under the name of the selected serial number. Removing the selected item from the "Saved_List.TXT" file is accomplished by reading this file and copying all items except the one selected into another file, in this case "Saved_List_Del". At the end of this process, "Saved_List.TXT" is deleted and 'Saved_List_Del" is renamed as 'Saved_List.TXT"'.

To delete the file containing the test history the following statement:

Kill (DefaultPath \& Save_Test)
is used to remove the file with the name stored in Save_Test (which is the serial number of the selected item) using DefaultPath to locate it.

### 3.1.7 Directory Path Specification

The Directory Path specifies the location where all files generated and accessed by the GUI are saved. This location is copied into the variable DefaultPath which precedes the file name. Using DefaultPath files can be saved on the local hard drive, written to removable data storage devices or by mapping a network drive, files can be stored in allocated locations on the network.

The Directory Path settings can be viewed and reset via the Directory Path frame. The Directory Path frame is made visible by clicking on the View Setting button found on the View/Change Directory Path Settings Frame. The user can return to the View/Change Directory Path Settings Frame from the Directory Path Frame by clicking on the Exit Settings button. See Figure 3-32 and Figure 3-33.

View/Change Directory Path Settings
View Settings

View User Profile Setup
View User Profile

FIGURE 3-32: DIRECTORY PATH SPECIFICATION


## FIGURE 3-33: DIRECTORY PATH SPECIFICATION

The Default Path can only be set or changed by an administrator. A directory path is selected using the drive, directory and file input boxes. The administrator then clicks on 'View Selected Path' to verify that this is the correct selected destination. Once satisfied with the selected path, the administrator clicks on Change Default Path. An input box which prompts the administrator for the administrator's password appears and if the correct password is entered the selected path is saved as the new default directory path.

The default path can also be viewed by clicking on the 'View Default Path' button. The Default Path setting is dynamic (i.e. it can be changed when required and is not hard-coded) and points to the location in memory in which data can be saved. The Default Path itself also has to be saved in a file so that it can be referred to whenever the default path is required. The location of this file is static i.e. it is hard-coded and cannot be changed by the user or the administrator.

The name and location of this file is SavePath and "C:\Program Files\SavePath" respectively. When the GUI is loaded for use each time it is initiated, the Form_Load procedure opens the SavePath file and copies its contents into the Default Path variable. This is carried out on the onset of a test so that the Default Path variable can be accessed whenever the path is required instead of opening, reading and closing a sequential file each time it is required.

### 3.1.8 Exit Command

The exit command allows the user to exit from the GUI before a test is started or once the test has ended. The Exit functionality is disabled during a test.


## FIGURE 3-34: EXIT COMMAND CLICK

### 3.2 Percentage Variance Calculation.

All the literature in this chapter thus far has concentrated on the activities of the GUI when being prompted by a user or the controller and the output commands or signals that are transmitted by the GUI to the controller based on the data received and calculations carried out by the GUI. One such calculation is carried out when the GUI receives the test data from the Analogue-to-Digital converter (ADC) via the CM. This is the calculation of the percentage variance of the present reading from the stored reference reading. This is arguably the most critical calculation as the need for the entire project has evolved around it.


Calculate the \% variance of the present reading from the reference reading


Is the
variance? i.e. is
Current_Variance >
Percentage?

A (pp. 63)


FIGURE 3-35: FLOW DIAGRAM FOR THE CALCULATION SUBPROGRAM

This subprogram has two objectives; the first is to calculate the percentage variance of a present reading from the reference reading whilst the second objective is centered on the reference reading itself. Consider this, what if the reference reading is in fact a fault reading, i.e. what if the reference reading is the reading across an open or short circuit or a damaged winding on the armature? The first step would be to check whether the first reading recorded is very close or equal to zero volts.

This would indicate a short circuit and this value will therefore not be stored as a reference value. A true open circuit would be indicated by a reading that is very close to or equal to the supply voltage. But the supply voltage and current is not the same for every type of armature tested due to the armature characteristics as well as the arc length between the test current supply probes on the commutator. Also considering that damaged and potentially problematic windings also have to be detected. There is no clear cut value that can be used to reject a reference reading (that is other than the reading for a short circuit). In order to detect that the reference value being used is
indeed a value that was recorded on a fault winding; the GUI performs a check after the first five readings taken, subsequent to the reference reading.

This essentially means that this check is carried out on the sixth reading captured. Variable Initial Count keeps track of the number of readings taken and by recalling an earlier discussion regarding the Test Status display, the reader will remember that the number of faults recorded is displayed in a text box (Text8). Noting this, in the event that the value in Initial Count is six and the value of Text8 is five,

$$
\text { If }(\text { Initial_Count }=6) \text { And }(\text { Val }(\text { Text8.Text })=5) \text { Then }
$$

this event will indicate that five (5) faults have been logged immediately after the reference value was set.

If such an event occurs, the GUI will conclude that based on the last five captured readings, the reference value was set on a fault or damaged winding reading. The reference value is then reset to that of the value recorded on the present bar (which will be the sixth bar). The values in the Test Status display as well as the variables that hold the values which reflect the number of bars that remain to be tested and the bar presently under test, are also adjusted appropriately to reflect this change. The test is reset on the sixth bar and continues as normal from that point forward.

For all of the above to occur the data transmitted from the controller has to be converted, manipulated and passed through mathematical formulae in order to obtain usable values that can be compared, displayed and stored. The following discussion will cover the manner in which this is done. Recall, that ASCII codes are transmitted by the controller. These ASCII codes are then converted into their associated numerical values in the OnComm procedure using the Visual Basic Asc function, as shown below,
Low_Byte = Asc(Serln)
and,
High_Byte = Asc(Serln)

When the calculation subprogram is called by the OnComm procedure, the Low_Byte and High_Byte variables already contain the required numerical values. The first step in the calculation subprogram is to convert these two bytes of data into the original sixteen (16) bit word that was present in the ADC register before its transmission as two separate bytes to the CM. This is accomplished using:
StnBit_WD = ((High_Byte * 256) + Low_Byte)

Once the sixteen-bit word has been realised, it is then necessary to calculate the actual voltage that this word represents. This is accomplished by dividing the ADC reference value (which is also the maximum input ADC voltage) by the sixteen-bit word when each bit is equal to 1 (i.e. 1111111111111111 which equals 65536 ). By doing this, the voltage-per-bit value or the resolution in volts (stored in variable ActVolReadRes) is obtained. With an ADC internal $\mathrm{V}_{\text {Ref }}$ of 4.096 V and sixteen bit resolution, the smallest voltage increment that the input signal can broken down into is:

$$
\text { Resolution in Volts }=4.096 / 65536=62.5 \mu \mathrm{~V}
$$

This value is then multiplied by the value of the sixteen-bit word that was captured (StnBit_WD) to produce the actual voltage associated with the sixteen bit word. This actual voltage is then stored in variable, ActVolRead. Furthermore, the actual voltage is divided by the analogue gain to obtain the true voltage reading that is present on the bars before the analogue gain. Note that the variable named "Gain" holds the value of the analogue gain as set using the Instrumentation Amplifiers external gain resistor $\mathrm{R}_{\mathrm{G}}$.

```
Let ActVoIReadRes = (4.096 / 65536)
Let ActVolRead = (StnBit_WD * ActVolReadRes)
Let mVActVoIRead = (ActVoIRead / Gain)
```

For the calculation of the percentage variance however, these actual voltage values are not used. The percentage variance is calculated using the numerical value of the sixteen bit words that are stored in variable StnBit_WD (which holds the value of present reading) and that stored in variable Reference (which holds the value of the reference reading). This is done in order to use values as close to the original recorded
values as possible and to decrease the probability of any errors that may arise by using values that have been rounded off. The equation below is responsible for the calculation of the percentage variance of the present reading from the reference reading.

$$
\text { Current Variance }=(((\text { Abs(StnBit_WD }- \text { Reference })) / \text { Reference }) * 100)
$$


#### Abstract

Abs is a Visual Basic function that produces the absolute value of a mathematical calculation. Here it is used to provide the absolute value for the difference between the present reading value (StnBit_WD) and the reference reading value (Reference) as either value may be greater than the other for any reading taken. This value is then divided by the reference value and multiplied by a hundred to obtain the percentage variance.


The next step is to compare the percentage variance value (Current Variance) to the allowable or pre-selected percentage variance that was selected by the user. Recall that this pre-selected percentage variance is stored in variable, Percentage.

```
If (Current_Variance > Percentage) Then
List1.Addltem "Fault on Bar:" & Text6.Text & ", Percentage Variance = " &
    "Current_Variance & ", Segment Reading: " & ActVolRead & "V" &
    ", Reference Reading: " & ActReference & "V"
Let Text8.Text = Val(Text8.Text) + 1
End If
```

The statements above show the comparison between the two values. In the instance where Current Variance is greater than Percentage, a fault will be recorded in the Fault Log display.

Another subprogram that is executed on every bar is the calculation of the number of bars that remain to be tested. The Bar_count subprogram decrements the number of bars that remain to be tested (stored in variable No_of_Bars) by one each time the controller transmits an increment prompt (ASCII code for the letter 'I'). This increment prompt is transmitted by the controller before the rotation of the armature under test is initiated hence the total number of bars is decremented before the very first rotation.

With this in mind, the reader will follow that when the increment signal is transmitted by the controller before the last pair of bars is tested, the decremented value in Bar_count will be zero. After the last pair of bars has been tested and when the controller next sends an ' I ' the decremented value will be less than one. It is at this point that the GUI signals to the controller that the last bar has been tested and that the test must now end.

The prompt to the CM which signals that the last bar has been tested is the ASCII code for the letter ' P '. For every increment signal received by the GUI before the last one, the ASCII code for the letter ' p ' is transmitted to the controller to indicate the last bar has not been tested and that rotation should be initiated.

### 3.3 The Remote Graphic User Interface (RGUI)

The Remote Graphic User Interface is used by authorised users in remote locations to view test records via the network, see Appendix F for a true representation of the RGUI and Appendix G for a printout of the associated code. The RGUI can only access information when the test station GUI stores data in a location on the network by mapping the network as a drive. The Default Path that is set on the RGUI must be the same as that of the GUI on the workshop floor. The RGUI only allows users to read and print information from saved files. Note that the format in which test data is displayed is exactly the same as the format in which the GUI displays retrieved file data as shown in Figure 3-37A and Figure 3-37B.

The user cannot edit, replace or delete files from a remote location. The RGUI contains three fields, namely the Search Information field, Data Display field and Directory path field. The inputs and button prompts are much the same as those on the test station GUI. They carry out the same functions and operate in the exact same way. The only variation from the test station GUI is the File Names and Refined Search - Dates display lists. The File Names list and contents is the same as the list that appears on the test station GUI when the Open button is clicked. In the RGUI this list box is permanently displayed.

The Refined Search - Dates list and contents is the same as the list that appears when a serial number is clicked on in the serial number list on the GUI. Here as well, the difference is that this list box is permanently displayed on the RGUI. As in the GUI, when Open is clicked, an input box appears prompting the user to enter a serial number. If a valid serial number is entered all test results for that serial number will be displayed in the Data Display screen. If 'Find' is entered into the input box the serial numbers of all tested armatures are displayed on the RGUI in the File Names list.

Upon selecting an item from this list, all dates on which tests were carried out on the selected armature as well as a 'View All' option appears in the Refined Search Dates list. By selecting a specific date the results of test(s) carried out on that date will be displayed in the Data Display screen. If 'View All' is selected, results of all tests carried out on the selected armature are displayed. All other functionalities that are available on the RGUI operate in the same manner as those on the GUI.


FIGURE 3-36: REMOTE GRAPHIC USER INTERFACE (RGUI)


## FIGURE 3-37A: REMOTE GRAPHIC USER INTERFACE (RGUI) DATA DISPLAY

Job Number: Test Results 1
Operator's Name: Sunveer Matadin
Armature Name: B Number of Bars. 10
Percentage Variance: 5\%
Date: 20106/04/12
Recorded Faults
Fault on Bar: 2. Percentage Variance $=4.370112 \mathrm{E}-\mathrm{02}$. Segment Reading: 0.1372522 . Fieference Reading: 0.1373122 y
Fault on Bar: 3. Percentage Variance $=18.39481$. Segment Feading: 0.1625705 V . Fieference Fieading: 0.1373122 y
Fault on Bar: 4. Percentage Variance $=0.5904046$, Seqment Reading: 0.1365015 V , Reference Reading: 0.1373122 V
Fault on Bar: 5. Percentage 'Variane = 10.91533 . Seqment Reading: 0.1223241 V . Fieference Feading: 0.1373122 y
Fault on Bar: G. Percentaqe Variance $=0.4614717$. Seqment Reading: [0.1366786v, Reference Reading: 0.1373122 V
Fault on Bar: 7. Percentage Variance $=10.28797$, Segment Reading: 0.1514309y, Reference Reading: 0.1373122 y
Fault on Bar: B. Volt-Drop Readingls Zero [DV]. Indicating A Possible Short Circuit
Fault on Bar: 9 . Volt-Drop Readingls Dut Dif Range. Indicating A Possible Dpen Cirouit
Fault on Bar: 10. Volt-Drop Reading Is Zero [CV']. IndicatingA. Possible Short Circuit
End DF Recorded Results

FIGURE 3-37B: REMOTE GRAPHIC USER INTERFACE (RGUI) DISPLAY

## FORMAT

## Chapter 4

## Microcontrollers and Embedded Programming

In this chapter the core of the controller will be discussed. This core comprises a pair of microcontrollers that communicate with each other via their port pins in order to perform the appropriate physical tasks, at the precise time, based on information received from the GUI and transducers on the automated machine i.e. the Physical Test Station. Both are AT89S51 microcontrollers and are enhanced derivatives of the 8051 [9] family. These microcontrollers were chosen on the basis of them having the following essential features: four eight pin input/output ports, 4 K bytes of Flash memory, two external interrupts, two sixteen bit timers and a full duplex UART serial channel. For further information on this microcontroller, see Appendix H for a comprehensive datasheet.

A microcontroller is the bridge between software instructions (commands) and electrical hardware. Programs written in C, Assembly [9] or any other compiler compatible language are compiled and assembled, and stored in the microcontroller memory which is most likely to be EEPROM technology. The speed at which these programs are stepped through (or executed) is dependent on the length of time that one machine cycle takes to execute and the number of machine cycles that are required for each instruction to execute. Depending on the instruction, data is either processed or input and output ports are addressed to either read signals or produce signals to or from interfacing electrical hardware.

The length of time that one machine cycle takes to execute depends on the frequency of the oscillator that provides the clocking source for the microcontroller. This design is not time critical which means that commands based on processed information did not have to execute at a very rapid rate. It is for this reason that a 12 MHz quartz crystal was chosen to drive the on-chip oscillator resulting in a machine cycle of one microsecond $(1 \mu \mathrm{~s})$ duration. The tasks performed by these microcontrollers do not involve complex mathematical calculations or algorithms. It is for this reason that code was written in assembly language as opposed to a higher level programming
language. The advantages that assembly language has over higher level languages for these types of applications (bit manipulation, logic operations and input/output port interaction) are execution speed and the efficient use of program memory space. The Acebus development environment was used to develop and simulate the code for both microcontrollers. This tool allows the developer to write, assemble, simulate and debug code written in assembly language. In the simulation environment, code can be stepped through line-by-line and the changes in the respective registers, special function registers, input/output ports etc. are reflected accordingly. See Figure 4-1A and Figure $4-1 \mathrm{bB}$ for screen captures of the Acebus development environment and Appendix I for a labeled representation of the development environment.


FIGURE 4-1A: SCREEN CAPTURE OF THE ACEBUS DEVELOPMENT ENVIRONMENT


FIGURE 4-1B: SCREEN CAPTURE OF THE ACEBUS DEVELOPMENT ENVIRONMENT IN SIMULATION MODE

Each microcontroller has a specific function, one being communication and acquisition of data as performed by the Communication Microcontroller (CM) and the other being the control of the automation tasks as performed by the Automation Microcontroller (AM).

### 4.1 The Communication Microcontroller

The Communication Microcontroller communicates with the GUI via its onboard serial port and with the Automation Microcontroller and the Analogue-to-Digital Converter (ADC) via its input/output pins (I/O pins). See Appendix Q for a detailed discussion including flow diagrams and code extracts.


FIGURE 4-2: SYSTEM BLOCK DIAGRAM

The function of the CM includes the transmission and reception of prompts to and from the GUI, the control of the ADC, the capture of data (high and low bytes) and storage thereof in two registers in its memory and the transmission of this data to the GUI for analysis. When the analysis is complete the GUI prompts the CM which in turn signals the AM to continue with the test.

While the AM is in control it communicates with the CM in the event of any system errors. If no errors occur, the AM will hand over control to the CM in order for the CM to take the volt-drop readings after the test current has been switched on and the test probes have been lowered onto the bars of the commutator. These readings are then transmitted to the GUI and so the process continues until the last pair of bars has been tested. See Figure 4-3 for the flow diagram of the CM. A discussion follows thereafter.


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## FIGURE 4-3: FLOW DIAGRAM FOR THE COMMUNICATIONS MICROCONTROLLER

On power up the CM initialises the ADC (i.e. the MAX 1166). With reference to the MAX 1166 datasheet, included as Appendix J, the ADC manufacturer's application information found on page 9 suggests that a 'dummy' conversion should be run in order to put the ADC in a known state after powering up from shut down. The CM then waits for the GUI to transmit a "Status: Ready" prompt, i.e. the ASCII code for the letter ' A '. When this has been received the CM transmits ' $b$ ' to the GUI to request the mode of operation in which the test is to be run. If a ' $G$ ' is received then the test is to be run in manual mode, the CM then informs the AM of this by Clearing (0) the CM P0.6 so that the AM can enter Powerdown mode.

The CM notes that the test is being run in manual mode by setting flag 04H in the bit addressable ram. This flag is tested in the CM Reading Subroutine in order to establish whether communication with the AM should be attempted. Recalling that AM is in Powerdown mode during a manual test any attempt by the CM to communicate with the AM will be futile and will ultimately leave the CM in a continuous wait loop as it will be waiting for communication signals from the AM that will never arrive. When flag 04H is tested in the Reading Subroutine and is found
to be Set (1), the CM will not attempt to communicate with the AM as the test is being run in manual mode. However, if this flag is tested and is found to be Low (0) the CM will establish communication with the AM as the test will be running in automated mode. If a ' g ' is received, the test will be run in the automated mode. The AM will be informed of this by Setting (1) the CM P0.6. Once the CM captures the mode of operation it transmits a ' $d$ ' to the GUI to indicate that it is ready to begin the test. As mentioned previously in the discussion relating to the GUI Start control, it is once the ' $d$ ' is received that the Start Button is enabled. On clicking the Start button an ' A ' is transmitted by the GUI. On receipt of this prompt ('A') the controller begins the test.

For the first pair of bars to be tested the CM transmits an increment prompt to the GUI, which is the ASCII code for the letter 'I', without waiting for an increment signal from the AM. However, after the first pair of bars has been tested, the CM will wait for the increment signal from the AM before transmitting the ' I ' prompt to the GUI. The increment signal from the AM is signaled by setting its output P0.0, High (logic level 1). See Appendix K for a complete list of Input/Output port utilisations for both microcontrollers.

The input P2.3 of the CM which is directly connected to P 0.0 of the AM is then also read as a High. This High state on the CM input pin is recognised as an increment signal from the AM. This signal from the AM serves to inform the GUI, via the CM, that the system is ready to test the next pair of bars. When the increment prompt is transmitted to the GUI, the Bar_count subroutine is called in order to ascertain whether the last pair of bars has been tested. If it has been tested, the GUI transmits a ' P ' to the CM to acknowledge that the test has been completed. On receiving this prompt the CM in turn informs the AM that the test is over and that Powerdown mode should be entered into. After verifying that the AM has received the command to enter Powerdown the CM itself enters Powerdown.

Note that in manual mode, the CM does not read an increment pulse from the AM as the AM is in Powerdown mode. An increment signal is generated by the user pressing on a switch that is connected to P3.6 which sends the increment prompt to the GUI.

The end of a test is signaled by the receipt of a ' B ' prompt from the GUI. This prompt is transmitted when the END control button is clicked on the GUI. The prompt ' B ' is transmitted regardless of the mode in which the test has been run. However in the automated mode the CM does not wait for the receipt of this prompt to enter Powerdown as it is already aware of the end of the test due to the AM increment signal and the GUI Bar_count subroutine.

If the last pair of bars has not yet been tested, the GUI transmits ' p '. When the CM receives this signal it instructs the AM to begin the rotation of the armature under test by setting P0.0 High. The CM waits for the AM to detect the next pair of bars, stop the armature rotation, switch on the test current and lower the test probes onto the detected bars. Once the AM receives a signal from the detection unit, indicating that the test probes are on the commutator, it signals the CM to take a reading. When the CM reads P2.2 as a High it calls the subroutine that captures the volt-drop reading for the pair of bars under test. This subroutine will be discussed in detail later in this chapter. The captured data is stored as a High Byte and Low Byte in two registers in the CM memory (RAM). The CM then transmits each byte to the GUI where it is analysed. Upon completion of the calculation and the analysis process by the GUI, the GUI transmits an ASCII ' E ' to the CM. This prompt serves to inform the CM that the data has been analysed and that the GUI is ready to proceed to the next pair of bars.

It should be noted that as an additional feature, one hundred consecutive readings are captured at $1000 \mu$ s intervals and averaged for each pair of bars. The CM and GUI Reading Subroutines were therefore modified to enable this functionality. The details and discussion offered in this chapter are aimed at providing an understanding of the basic features and concepts before the more complex additional features are discussed in Chapter 6.

On receipt of this prompt, the CM informs the AM that it too is ready to proceed to the next pair of bars by setting its P0.7 High (1). On receiving a High on P1.7, the AM confirms that it is ready to proceed to the next pair of bars by setting its P0.1 High (1) which is the increment signal that the CM reads on its P2.3. When P2.3 is read as a High (1) the CM transmits the increment prompt ('I') to the GUI.

The CM follows this process until the last pair of bars has been tested or until any one of the four possible system errors interrupts the process flow. When such an interrupt is encountered there is a branch from the main program flow to an interrupt handling procedure (an ISR) that caters specifically for the encountered error. Once the error has been 'handled' control is handed back to the main program. These Interrupts, their associated Interrupt Service Routines (ISRs) and critical subroutines will be discussed in the sections that follow. See Appendix L for the source code for both the Communication and Automation microcontrollers.

### 4.1.1.1 External Interrupts

The CM makes use of External Interrupt 0 by enabling and disabling it on demand and initialising it with a low-level interrupt priority and negative-edge activation. The function of this interrupt is to indicate and service system errors if or when they occur and to inform the GUI (by transmitting a 'O') when a manual Emergency Stop has been initiated by pressing on the Emergency Stop switch (on P3.2) on the Test Station or by the activation of a safety interlock. Once the GUI has been informed of an Emergency Stop, the CM enters Powerdown mode.

Error1 occurs when a pair of bars is not detected within a specified time, Error2 occurs when the test probes are not present on the surface of the commutator within a pre-selected default time, Error3 occurs when the test current is not switched off after a pre-selected default time and Error4 occurs when the test probes are not raised to their original position within a specified time. The AM is the first to recognise any errors should they occur as system monitoring signals produced by proximity switches and other transducers are input to the AM via the interfacing digital system. The AM then sets High (1) output pins that correspond to the error that has occurred. See Appendix K and Table 4-5.

| Automation Microcontroller (AM) - Automation Control |  |  |
| :--- | :--- | :--- |
| P2.6 | $(27)$ | $\mathbf{O}$ - Error 4 - Test Probes Not Raised. |
| P3.5 | $(15)$ | $\mathbf{O}$ - Error 1 - Pair Not Detected. |
| P3.6 | $(16)$ | O - Error 2 - Test Probes Not Lowered. |
| P3.7 | $(17)$ | O - Error 3 - Current On-Time Exceeded. |

TABLE 4-1: TABLE OF THE AM ERROR OUTPUT INDICATION PINS

These output pins are connected to individual input pins on the CM as well as the External 0 interrupt as depicted in Appendix K and Table 4-6.

| Communications Microcontroller (CM) - Communication \& Signalling |  |  |  |
| :--- | :--- | :--- | :---: |
| P2.4 | $(25)$ | I - Error 1 - Pair Not Detected. |  |
| P2.5 | $(26)$ | I - Error 2 - Test Probes Not Lowered. |  |
| P2.6 | $(27)$ | I - Error 3 - Current On-Time Exceeded. |  |
| P3.2 | $(12)$ | I - External Interrupt 0 - All Error Inputs Connected here as well. |  |
| P3.4 | $(14)$ | I - Error 4 - Test Probes Not Raised. |  |

TABLE 4-2: TABLE OF THE CM ERROR INPUT INDICATION PINS

When a system error occurs, the AM signals the CM by setting the associated pin High (1). When any one of the error lines go High (1) the interfacing digital system also triggers External Interrupt 0.


FIGURE 4-4: FLOW DIAGRAM FOR EXTERNAL INTERRUPT 0 - CM

When the interrupt is triggered the External Interrupt 0 ISR is initiated. Once in the ISR, each input error pin is tested for a High (1) status and when an error pin is identified the associated subroutine is called to handle it.

### 4.1.1.2 The Reading Subroutine

The Reading Subroutine is responsible for communication with the Reading subroutine in the AM, controlling the ADC via the ADC control lines, capturing the recorded data from the ADC and transmitting this data to the GUI.


FIGURE 4-5: SYSTEM BLOCK DIAGRAM



FIGURE 4-6: READING SUBROUTINE FLOW DIAGRAM

Once called the first operation undertaken by this subroutine is to verify whether flag 04 H has been set. Flag 04H is set when the system is to be operated in Manual mode. When running in Manual mode the AM is in Powerdown and will therefore not respond to any communication signals from the CM . When operating in the Automated mode there is constant communication between the AM and the CM in order to maintain synchronisation.

Whilst operating in Manual mode this communication is fruitless as the CM will be waiting for signals from the AM which will never be transmitted. The CM will therefore be caught in an endless waiting loop. The reason for the testing of the 04 H flag is to ensure that the CM knows if it should communicate with the AM (whilst in Automated mode) or if all its communication instructions should be skipped, whilst in Manual mode as discussed earlier in this chapter. Flag 05H is used to indicate that 100 successive readings are to be taken. This is an additional feature and will be discussed in Chapter 6.

If the system is in Automated mode, P 2.2 is tested in order to verify that the AM has called and is presently executing its Reading subroutine and to ensure that it is ready to take a reading. The CM then confirms having received this signal by setting its P0.7 pin. As mentioned above, these steps are skipped when in Manual mode. Next, P0.2 is tested in order to verify that the reading about to be taken is within the maximum input range of the ADC and other interfacing circuitry. The exact mechanics behind this process will be discussed in detail in Chapter 5. However in order to facilitate a better understanding, the author will briefly discuss the principle and concept used.

Although the test is setup by the technician to record values within a particular range, 200 mV to 350 mV , the possibility exists that a volt-drop equal to the potential of the Test Supply can be recorded across a pair of bars. This will occur when the pair of bars being tested is connected to an open circuited winding. According to tests carried out by the author, the typical Test Supply potential when setting the aforementioned range is between ten and fifteen volts ( 10 V to 15 V ) depending on the type and rating of the armature under test. As will be explained in chapter five the first stage in the input circuitry is more than capable of handling these values as well as negative input
potentials, as in the case when the polarity of the Test Supply Current or the orientation of the input test probes is reversed. The ADC input stage cannot handle such potentials. The ADC absolute maximum rating for the input pin is positive 6 volts to negative $0.3 \mathrm{~V}(+6 \mathrm{~V}$ to $-0.3 \mathrm{~V})$. It is for this reason that an Analogue Switch (MAX 4622) is placed on the ADC input line. This switch is only switched on by the CM when the interfacing analogue circuitry confirms that the potential on the ADC input line is safely within its operating range. This circuitry is explained in Chapter 5, Section 5.3.

If the CM P0.2 is High (1), the Analogue Switch is off due to the input value being out-of-range. In this case 11111111 (binary code) is transmitted as the High Byte and 11111110 (binary code) is transmitted as the Low Byte to the GUI as the reading for the pair presently under test. Upon receiving this value the GUI immediately recognises the out-of-range reading and displays a possible open circuit on this pair of bars. After this transmission the CM sits in a wait loop, waiting for the GUI to transmit the Continue Test prompt, i.e. 'E'. Note that in order to facilitate the 100 reading additional feature, a second prompt is used to verify that all 100 readings have been captured. This prompt is the ASCII code for the character ' S '. Further details on this additional feature will be provided in Chapter 6.

If P0.2 is low, the Analogue Switch is and the ADC can read the input potential. The ADC control pins are then prompted and read by the CM in order to capture a reading. The High Byte is stored in the CM register 5, R5 and the Low Byte is stored in the CM register 3, R3. See Appendix K for a list of the registers used for both the AM and CM .

The next step is to check if R5 holds 11111111 and R3 holds 1111 1110. This is the previously mentioned out-of-range default value. If the default value has been recorded, the value held in R3 is changed to 1111 1111. This new value and the out-of-range default value should normally not be recorded on a non-fault bar. As discussed in Chapter 3, the ASCII code for the letter ' $z$ ' is transmitted to the GUI before the High Byte (the value held in R5) of the captured reading is transmitted to the GUI. The ASCII code for the letter ' y ' is transmitted to the GUI before the Low Byte (the value held in R3) of the captured reading is transmitted to the GUI. The CM
then waits for the GUI to process the transmitted data and informs the CM that it is ready to continue by transmitting an ' E ' (the Continue Test prompt).

On receiving this prompt the CM again tests if flag 04H is set High (1). If it is not set High, then using P0.7 and P2.2 as described above, the CM communicates with the AM to inform it that the reading has been successfully captured, transmitted and analysed and that it should ready itself to proceed with the next task in the process. If the flag 04 H is set, then this communication process is skipped as mentioned earlier. The CM then switches off the analogue switch on the ADC input line in order to protect the ADC in the event of an out-of-range input value on the next pair of bars. The subroutine is then exited and control is returned to the calling program at the statement immediately following the CALL instruction.

### 4.1.2 ADC Control

The ADC control pins and the associated connection pins on the CM are listed below. The $\overline{C S}$, Convert Start ADC input pin, is connected to the CM P3.5 pin which is configured as an output pin. The $\mathrm{R} / \bar{C}, \mathrm{Read} / \overline{\text { Convert }}$ ADC input pin is connected to the CM P2.0 pin which is configured as an output pin. The $\overline{E O C}$, End Of Conversion ADC output pin, is connected to the CM P2.1 pin which is configured as an input pin.

And finally, the HBEN, High-Byte Enable ADC input pin is connected to the CM P3.3 pin which is configured as an output pin. Figure 4-7 depicts the flow diagram that describes the process that is followed when the ADC captures a reading. Figure 4-8 depicts the flow diagram that shows the steps taken by the CM to implement the process followed in Figure 4-7. Figure 4-9 depicts the timing diagram for the ADC control process. See Appendix J to view the ADC (MAX 1166) datasheet.



FIGURE 4-7: FLOW DIAGRAM FOR THE ADC CONTROL PROCESS



FIGURE 4-8: FLOW DIAGRAM OF STEPS TAKEN BY THE CM TO IMPLEMENT THE ADC CONTROL PROCESS


FIGURE 4-9: TIMING DIAGRAM FOR ADC CONTROL PROCESS

### 4.2 Automation Microcontroller

The Automation Microcontroller (AM) controls the Physical Test Station based on input signals received from the Physical Test Station itself, as well as commands and prompts received from the CM and the GUI via the CM .


FIGURE 4-10: SYSTEM BLOCK DIAGRAM

This section will describe the tasks undertaken by the AM and the manner in which these tasks are executed. See Appendix Q for a detailed discussion including flow diagrams and code extracts. The previous section provided detailed explanations on all the relevant microcontroller functionalities, such as Timers, Interrupts, Subroutines etc. This section will concentrate solely on discussing the AM's use of these functionalities to efficiently complete specific tasks. In order to provide an overview of the AM's process flow a diagrammatic depiction is presented in the form of a flow diagram in Figure 4-12.

### 4.2.1 Explanation of functions, tasks and flow process

The program for the AM was developed using three control levels based on interrupts and interrupt priorities. The first level is the base level where the Main program has control. Here the required initialisations are carried out as well as the control and timing of the Armature Drive Motor and the calling of Error 1 subroutine, should Error 1 occur. When a pair of bars is detected, External Interrupt 1 is triggered and the External Interrupt 1 Interrupt service routine assumes control thereby entering the
second control level. The EX1 ISR is responsible for stopping the Armature Drive Motor, the lowering and raising of the Detection Unit, switching of the Test Current, communication with the CM in order to capture the volt-drop readings and calling of error subroutines should the associated errors occur. The third level is the domain of the External Interrupt 0 (EX0) ISR. EX0 is assigned a higher priority than EX1 and can therefore interrupt the EX1 ISR as in the case when the test probes have reached the surface of the detected bars. In fact this is the function of EX0, i.e. to ascertain the status of the Detection Unit. When the test probes reach the surface of the bars EX0 is triggered, the Detection Unit Drive Motor is stopped and the time taken for the probes to be lowered to the surface of the bars is recorded in the EX0 ISR. EX0 is also triggered when the test probes have been raised to their initial position.

In summary, the base level allows for initialisations and also prompts the Armature Drive Motor to begin the rotation of the armature under test. When a pair of bars is detected EX1 is triggered and EX1s ISR is initiated as the second control level and assumes control from the base level. In the EX1 ISR, the Armature Drive Motor is stopped, the Detection Unit Drive Motor is prompted to lower the Detection Unit and the Test Current is switched on. The time taken for the test probes to reach the bars allows the test current to settle. Once the test probes on the Detection Unit reach the surface of the bars EX0 is triggered, the EX1 ISR is interrupted and the EX0 ISR executes initiating control level three and assuming control from the EX1 ISR. When the EX0 ISR has stopped the Detection Unit Drive Motor and has completed recording the relevant times, the ISR is exited and control is handed back to the EX1 ISR hence control level two.

The EX1 ISR then proceeds to communicate with the CM and a volt-drop reading is taken after which the Detection Unit Drive Motor is prompted to raise the Detection Unit. When the Detection Unit Drive Motor reaches its initial position EX0 is again triggered thereby initiating control level three and assuming control from the EX1 ISR and control level two. The EX0 ISR stops the Detection Unit Drive Motor and exits handing control back to EX1 ISR and control level two. EX1 ISR is then also exited and control is handed to the base control level and the Main program. Based on the commands from the GUI via the CM, the cycle is repeated until the last bar is tested. See Figure 4-11 for a diagrammatic representation of the above discussion. A more
detailed explanation of the Automation Microcontrollers process flow follows after Figure 4-12.


FIGURE 4-11: DIAGRAMMATIC REPRESENTATION OF THE THREE LEVEL CONTROL SYSTEM


A (pp. 96) B (pp. 96)



FIGURE 4-12: FLOW DIAGRAM FOR THE AUTOMATION MICROCONTROLLER

The AM first executes an initialisation process in which all the timers, interrupts and input/output ports that will be utilised for the duration of a test are initialised. Thereafter the AM waits for the start pulse from the CM on P1.0. Upon receiving this pulse, the AM tests P1.6 to ascertain whether the test will be run in the Automated or Manual mode. If P1.6 is High (1) then the Manual mode has been selected and the AM initiates Powerdown mode. If P1.6 is Low (0) then the Automated mode has been selected and the AM Sets (1) and Clears (0) P0.1, which is responsible for signaling 'Increment The Number Of Bars'.

The AM then waits for the GUI to inform it, via the CM, whether or not the last pair of bars has been tested. If P3.0 is Low (0), then the last pair of bars has been tested and the AM waits for the End command from the GUI via the CM. Once this is
received, the AM enters Powerdown mode. If P3.0 is High (1), then the last pair has not been tested and the command is given to the Armature Drive Motor to initiate the rotation of the armature under test by setting P0.4 High (1). The AM then waits for the next pair of bars to be detected while timing the period between the initiation command and moment when the pair of bars has been detected. Detection of a pair of bars triggers External Interrupt 1 (EX1). If EX1 is not triggered before the maximum allowable time for detection is exceeded, Error 1 has occurred and the associated subroutine is called. Recall that Error 1 occurs when a pair of bars has not been detected within the maximum allowable time. The maximum allowable time for detection for each of the first three pairs is a preset value of 10 seconds.

The time duration recorded on the third pair of bars is stored to be used to calculate a tolerance or the maximum allowable time for the detection of a pair of bars after initiating the rotation of the armature under test. This new maximum allowable time will be the Detection Reference Time for the duration of the test. The time recorded on the third pair plus twenty percent is used as the reference value, i.e.

## Detection Reference Time $=$ Third Pair Time Recording $\times 1.2$

From the fourth pair of bars onwards, if EX1 is not triggered before the Detection Reference Time has expired, Error 1 subroutine is called. The use of the Detection Reference Time allows for greater control of the system as the unique reference value that is used for the duration of the test is based on the bar widths and spaces between the bars of the particular armature under test. In this way an error is detected sooner than if a preset value that catered for all armatures was used, hence the possibility of excessive damage to the system and the armature under test due to a system error is reduced. The reason that the Detection Reference Time is calculated based on the time recorded for the third pair of bars is simply because the system is given time to settle during the first and second cycles.

The question that now arises is what happens if a detection error occurs on the third pair of bars, i.e. when the time is being recorded to calculate the Detection Reference Time? The answer is that if Error 1 was called before External Interrupt 1 was triggered, then a time period will not be recoded as all time recordings is done by the

External Interrupt 1 interrupt service routine (ISR). The Error 1 subroutine does not have the capability to perform any time interval recording. Hence the value that will be used to calculate the Detection Reference Time will now be recorded on the next detection cycle, i.e. on the fourth pair of bars. However, to introduce redundancy, the Error 1 subroutine also takes appropriate measures when this event occurs. Note that the use of timers to record time, set preset intervals and introduce delays is discussed in Section 4.1.4.

When a pair of bars has been detected before the Detection Reference Time has exceeded, hence triggering EX1, the rotation of the armature under test is immediately stopped by Clearing (0) P0.4. The rest of the process from this point forward is executed in the External Interrupt 1 ISR. From this ISR, the signal to the Detection Unit Drive Motor to begin lowering the Detection Unit is given. The Test Current is also switched on by Setting (1) P2.7. The Test Current is switched on before the Test Probes on the Detection Unit reach the bars as opposed to when they are already on the bars. This is done to prevent large voltage spikes due to the switching of the large test current to the inductive load (i.e. the inductance ( L ) of the armature under test), from damaging the input circuitry.

The Test Probes must not be confused with the Test Current Probes. The Test Current Probes are the probes from which the Test Current is injected though the armature under test via an IGBT. The Test Current Probes are lowered onto the commutator and are fixed into place at the start of the test and are in no way attached to the Detection Unit. These probes are not raised off or lowered onto the commutator as in the case of the Test Probes on the Detection unit. The Test Current is switched on when a reading is to be taken and is switched off when a reading is complete and the Test Probes have been raised off the surface of the commutator.

The Test Current probes are never raised off the surface of the commutator at any time during the test. When the IGBT is switched off, the collapsing magnetic energy that is stored in the armature is dissipated via an onboard fly-back diode. Fly-back diodes are a standard feature on most modern IGBT units and are built into the semiconductor structure of the IGBT to provide onboard protection in a single unit. The Test Current is switched on between 2 and 4 seconds after it was last switched off
depending on the speed of rotation and the spacing of the commutator bars. The low switching frequency allows for sufficient time for the stored magnetic energy to be dissipated via the onboard fly-back diode hence there is no arcing.

The spring mounted Test Probes are fixed onto the Detection Unit. These probes are lowered and raised when a reading is to be taken. A minute current flows through these test probes due to the extremely high input impedance of the Data Acquisition Module, more specifically the input impedance of the precision Instrumentation Amplifier, the INA 118, as discussed in Section 5.3. It is due to this high input impedance and the low Test Supply Voltage of typically +15VDC maximum that arcing does not occur when the test probes are raised off and lowered onto the commutator when the Test Current is flowing through the armature. Tests on the Data Acquisition Module proved that no arcing takes place when the test probes are raised off and lowered onto the commutator while a Test Current was allowed to flow through the armature.

The only undesirable electrical effect that would have to be catered for is the bouncing of the input signal due to the mechanical bounce created when spring loaded test probes make contact with the surface of the bars. This bounce will create oscillations in the input signal however, the amplitude of these oscillations should not exceed the amplitude of the input signal when it has settled. This means that although there will be oscillations due to the bounce, there will be no voltage spikes as created when switching the Inductive load. In order to cater for the above-mentioned oscillations, the ADC is instructed to perform acquisition and conversion only after a delay period has been enforced.

If the test probes on the detection unit do not reach the surface of the bars within a preset time then Error 2 occurs and the associated subroutine is called. When the test probes reach the surface of the bars within the allocated time, the Detection Unit outputs a signal which triggers External Interrupt 0 (EX0). As mentioned previously, EX0 is assigned a higher priority than EX1. Error 2 will be initiated when the preset allowable time of ten seconds, for reaching the surface of the bars, expires before EX0 is triggered. If EX0 is triggered before the aforementioned time expires, the EX0 ISR is initiated. The EX0 ISR stops the Detection Unit Drive Motor and stores the time
that was taken for the test probes to reach the surface of the bars by copying the values held in the timer registers. Once on the surface of the bars, the AM signals the CM that a volt-drop reading can now be taken be Setting (1), P0.0. The AM then waits for one of two signals from the CM. The first is the signal received on P1.7, which informs the AM that the reading has been successfully taken by the CM, transmitted to the GUI, analysed and stored. Now both the GUI and the CM are ready to proceed.

The second signal is received on P 3.1 which informs the AM that the maximum allowable time that the Test Current can be switched on for an individual volt-drop reading has been exceeded. The timing of the Test Current on-time is carried out by external interfacing circuitry and is discussed in Section 5.1.6. If P3.1 is Set (1) before P1.7, Error 3 has occurred. The Error 3 subroutine is then called and due to the severity of the effects of such high currents being applied to the armature under test for a prolonged period of time, an Emergency Stop is automatically initiated and the AM immediately halts the task that was being carried out, switches off the Test Current by Clearing (0) P2.7 and safely shuts the system down before entering Powerdown mode. If however, P1.7 is Set (1) before P3.1 then the volt-drop reading will be captured with no system irregularities and the process flow continues as normal.

The next step is to prompt the Detection Unit Drive Motor to begin raising the test probes off the surface of the bars. Here again EX0 is triggered when the Detection Unit reaches its initial position. If, however, EX0 is not triggered before the maximum allowable time has elapsed Error 4 occurs and the associated subroutine is called. This maximum allowable predetermined time for this process is called the Unit Raising Reference Time. This period is derived by adding twenty percent of the time taken for test probes to reach the surface of the bars (during lowering) to the recorded time itself, i.e.

## Unit Raising Reference Time $=$ Recorded Test Probe Lowering Time x 1.2

When EX0 is triggered before the Unit Raising Reference Time expires, the Detection Unit Drive Motor is stopped and control is returned to the EX1 ISR, which in turn
returns control to the Main program. The Main program then transmits an Increment signal to the GUI via the CM and waits for the response. This cycle continues until each pair of bars on the commutator of the armature under test has been tested.

### 4.2.1.1 External Interrupt 1 and External Interrupt 1 ISR

External Interrupt 1 is triggered when the optical sensors on the detection unit detects a pair of bars and signals this event via a D flip-flop and an interfacing digital network. On triggering this interrupt, the program is immediately paused and the program vectors off to the location in memory that is allocated to the EX1 ISR $(0013 \mathrm{H})$. Due to its size, eight bytes is too little space to hold the entire ISR. The ISR has to therefore be located elsewhere in memory and identified by a label. Once at the vectored address, i.e. 0013 H , a long jump is initiated to the ISR using the label EX1ISR to identify the ISR's location in memory. The label is the starting point of the ISR and once identified, the ISR executes and returns control to the interrupted program i.e. the Main program in this case using the Return Form Interrupt (RETI) statement. Figure 4-13 depicts the flow diagram for the EX1 ISR.



## FIGURE 4-13: EXTERNAL INTERRUPT 1 ISR FLOW DIAGRAM

On entering the ISR, the first task carried out is to stop the rotation of the Armature Drive Motor by Clearing (0) P0.4 and also stopping the Timers by Clearing (0) TR1 and TR0. The next task is to Clear (0) the D flip-flops that produce the triggering pulse. This is accomplished by setting port pin P0.5 High (1) for a short period before clearing it again. This is done to ensure that the D flip-flops are in a known state for the next detection cycle. The operation of the input detection circuitry will be discussed in Chapter 5. Next, the EX1 flag, 04H, is set. This indicates to the Main program that External Interrupt 1 was triggered and that EX1 ISR did execute.

Following this, the ISR checks whether the pair of bars that were detected are the third pair. If it is the third pair, then the values that are stored in the timer registers are copied into registers R4 (high byte) and R5 (low byte). Further, the value stored in register R3 (Timer 1 overflow count) is copied into register R6 in Register Bank 0, see Appendix K. These values are used in the calculation of the Detection Reference Time.

The Detection Unit Drive Motor is prompted to begin lowering the unit and the test probes onto the surface of the commutator by calling the RUN_DWNX subroutine. Once the test probes are on the surface of the bars the READING subroutine is called. This subroutine communicates with the CM READING subroutine in order to capture a volt-drop reading for that pair of bars. When the process reading is complete the

RUN_UP subroutine is called to raise the bars to its initial position. Note that all subroutines will be discussed in the section entitled Subroutines.

Finally, prior to exiting the ISR and returning control to the Main program, the timer registers and the Timer 1 overflow count register, R 3 , is reloaded with values that will force an almost immediate timer overflow thereby forcing the maximum allowable time to be exceeded, as discussed earlier. Control is then returned to the Main program.

### 4.2.1.2 External Interrupt 0 and External Interrupt 0 ISR

External Interrupt 0 is triggered when the test probes on the Detection Unit has reached the bars under test (when the unit is being lowered), the test probes have been raised to their initial position (when the unit is being raised), when an Emergency stop has been initiated (by pressing the Emergency Stop switch on the Test Station) or if one of the systems Safety Interlocks are triggered. When triggered the program vectors off to 0003 H where it is redirected using a jump statement to the location in memory where the label EXOISR resides. The location of this label is the beginning point of the EX0 ISR code.



FIGURE 4-14: EX0 ISR FLOW DIAGRAM

The first task undertaken by the interrupt service routine is to test port pin P1.5. If this pin is High (1) then EX0 was triggered by the initiation of an emergency stop or one of the systems Safety Interlocks was triggered. The ISR then jumps to the End label where the input/output ports are cleared and Powerdown mode is entered into. If P1.5 was Low (1) then the interrupt was triggered by the test probes reaching the surface of bars when being lowered or its initial position when being raised.

However, the ISR has to further ascertain if the interrupt was triggered while the ERROR READING PROCEDURE Subroutine was being executed by testing flag 0EH. This flag is Set (1) by the ERROR READING PROCEDURE Subroutine when a manual reading has to be taken due to an error and when it is Set (1), the EX0 ISR is to ignore the interrupt and exit the ISR. The ERROR READING PROCEDURE Subroutine will be further discussed later in this chapter. When flag 0EH is tested and found to be Low (0), the interrupt was not triggered during the execution of the ERROR READING PROCEDURE Subroutine. Both the raising and lowering motion is then stopped by Clearing ( 0 ) the port pins responsible for prompting the action, i.e. P 0.2 and P 0.3 respectively. Thereafter, the Timers are stopped by Clearing (0) TR1
and TR0. Following this, flag 0CH is tested. This flag is set by the RUN_UP subroutine to indicate that the Detection Unit was in the process of being raised at the moment of the interrupt.

If $0 C H$ is set, i.e. High (1), the Detection Unit was being raised before the ISR, which means that a reading was already completed and the test probes are off the surface of the bars and at its initial position when this interrupt was triggered. It is then required that the Test Current is switched off and this is accomplished by Clearing P2.7. If flag 0 CH was not set, i.e. Low (0), then the interrupt was triggered when the test probes reached the surface of the bars in order to take a volt-drop reading. The Test Current is therefore left on. After this process a delay is enforced by calling the DELAYLOOP subroutine.

The EX0 flag, 08 H , is then set to indicate that this interrupt has been triggered and that the associated ISR has executed. Next, flag 0CH is retested. In this case if the flag is not set (which implies that the interrupt was triggered when the Detection Unit was being lowered) the values in the timer registers are stored in Register Bank 1, register R1 (high byte) and R2 (low byte).

The Timer 1 overflow value that is stored in register R3 is copied into register R7 in Register Bank 0, see Appendix K. These values are recalled and used to calculate the Unit Raising Reference Time.

Prior to exiting and returning control to EX1 ISR the timer registers and the Timer 1 overflow count register, R3, are reloaded to force an almost immediate timer overflow hence forcing the maximum allowable time to be exceeded, as discussed earlier. Control is then handed back to the EX1 ISR by executing the RETI statement.

## Chapter 5

## Hardware Design

This chapter discusses the hardware design that enables the software that is executing within the embedded mirocontrollers and the GUI to be transformed into physical pulses and signals that control actuators that initiate the motion of objects in the physical world. Hardware also converts, conditions and monitors signals that are produced by transducers, which monitor the external environment, into signals and pulses that are decipherable and understood by the embedded microcontrollers.

This enables the system to respond to various inputs by executing the appropriate blocks of code in response to specific events. The author used the Protel Design Environment to draw schematics and develop the layout and routing of the PCB (Printed Circuit Board). The controller circuit was drawn in modules that link to each other using Netlables (this is a functionality that is available in the Protel Development Environment). The "Bottom-Up" design approach was used to develop this schematic. This approach involves drawing modules on independent sheets and using a Master Sheet (Entitled "Master" in this design) to facilitate linking between all schematic sheets using the above-mentioned Netlables.

Drawing schematics in modules that link to each other makes the circuit easy to understand and modify if need be, as it is uncluttered and easy to isolate a problem area. Each module will be discussed independently however; the reader will be informed as to how the module being discussed is connected to interfacing modules. The complete circuit schematic which includes all the modules discussed can be found in Appendix M, all datasheets can be found in Appendix J, and all test results are presented in Chapter 7. Also see Appendix R for a more detailed discussion covering all hardware modules.

### 5.1 Digital System Design

The digital system includes all digital circuitry, from the embedded controllers to the logic gates and drivers that are used in signal conditioning and level shifting respectively. The first modules to be discussed will be the Automation Microcontroller module and the Communication Microcontroller module. In both cases the 40 pin AT89S51 microcontroller was used.

### 5.1.1 The Communication Microcontroller Module

The Communication Micrcontroller module interfaces and communicates with the ADC by pulsing and reading the ADC control pins, HBEN, $\overline{C S}, \overline{E O C}$ and $\mathrm{R} / \bar{C}$ as well as receiving the 8 bit output from the ADC parallel output bus. This module also communicates with the Automation Microcontroller, reads the status on the Manual Reading switch and reacts to a forced emergency stop whether it was initiated by pressing the Emergency Stop switch or by the activation of any one of the four safety interlocks. See Figure 5-1 for a representation of the Communication Microcontroller Module and Appendix M for the complete circuit schematic.


FIGURE 5-1: THE COMMUNICATION MICROCONTROLLER MODULE.

The on-chip oscillator is driven by a quartz crystal X1 with the aid of two stabilising capacitors ( C 1 and C 2 ). Using a 12 MHz crystal and noting that each machine cycle is 12 oscillator periods, each machine cycle is calculated to be $1 \mu \mathrm{~s}$ in duration, as shown below.

$$
\begin{gathered}
\mathrm{T}=\frac{1}{12 \mathrm{MHz}}=83.33333 \times 10^{-9} \\
\mathrm{~T}_{\text {Machine Cycle }}=83.33333 \times 10^{-9} \times 12 \text { periods }=1 \mu \mathrm{~s}
\end{gathered}
$$

The reset pin (9) of the microcontroller is connected to the Reset pin of MAX 701 (see Appendix $\mathbf{J}$ for a complete datasheet for the MAX 701). The MAX 701 is a
supervisory circuit that monitors the supply to the microcontroller in order to detect Brown-out conditions. A Brown-out ${ }^{5}$ occurs when the supply falls to a level that is appreciably lower than the normal supply level for a prolonged amount of time. This will cause components that are powered by this supply to behave erratically and unpredictably. In the event of a Brown-out, which in the case of the MAX 701 is anything equal to or less than 4.65 V , the Reset pin of the MAX 701 goes High $(4.65 \mathrm{~V}$ or the present available positive logic High voltage) and is held at this level until the supply returns to its normal rating.

This procedure effectively holds the microcontroller in a Reset state until the supply is within its normal operating range. Note that holding the Reset pin (9) of the AT89S51 high (1) for at least two machine cycles effectively resets the microcontroller. The MAX 701 also provides a Reset-On-Power-up pulse to the microcontroller. This ensures that the microcontroller is in a known state on power-up i.e. all its input/output ports, internal registers, special function registers, program counter etc. are loaded with the default reset values reflected on Page 6 of the AT89S51 datasheet found in Appendix J.

The author originally used the RC network to provide the reset pulse on power-up but the author's experience has shown that this network behaves erratically and is therefore unreliable in environments where EMI (Electromagnetic Interference) is a factor.

The MAX 701 solved the EMI related problems, specifically relating to Reset-On-Power-up. There were various other methods adopted to negate the effects of EMI on the circuit as a whole. Some of these include, but are not limited to, proper PCB layout and design, which involved, amongst other things, placing the microcontrollers in the center of the board and the quartz crystals as close to the microcontroller oscillator pins (XTAL1 and XTAL2) as possible.

[^0]Reduced track lengths, avoiding $90^{\circ}$ bends in tracks, routing power and signal tracks away from each other, designing multilayer PCBs with paired power and ground planes, placing $0.1 \mu \mathrm{~F}$ capacitors across all ICs with the addition of a $4.7 \mu \mathrm{~F}$ capacitor directly across the microcontrollers. Along with these, the circuit was kept compact and a common grounded guard ring was routed around the edge of the PCB.

The first line of defense against EMI is the metal enclosure in which the circuit is housed. Keeping the size of the holes on the enclosure as small as possible and ensuring that the lid makes proper electrical contact with the rest of the enclosure, results in the metal enclosure forming a Faraday Cage around the circuit. To further reduce the impact of EMI via conductors from the external environment, shielded cables were used.

The interconnections between the Automation and Communications microcontrollers are summarised in the respective Microcontroller Port Utilisation tables found in Appendix K. The connections from the Communications Microcontroller to other devices are also summarised in the Communications Microcontroller Port Utilisation table found in Appendix K. Note that the $\overline{E A}$ (External Access) pin is connected to VCC. When the $\overline{E A}$ pin is held low (0) the microcontroller executes programs from external ROM. Holding the pin high (1) forces the microcontroller to execute programs from internal ROM.

The input to External Interrupt 0, P3.2, is an OR and NOR gate network which allows any of the system errors (Error 1, 2, 3 or 4) or an Emergency Stop, labeled "EmgcyStop_SW\&Intlks", (initiated by pressing the Emergency Stop switch or triggering a Safety Interlock) to trigger the interrupt. The Emergency Stop signal is an input to both microcontrollers that enforces a complete system stop by interrupting both microcontrollers and forcing them to enter a safe shutdown procedure before entering power-down themselves. This Emergency Stop is initiated by the triggering of switches (push-button and interlock) on the physical system and should not be confused with the Emergency Stop that is initiated by clicking on the Emergency Stop button on the GUI, although both events yield the same end result. Including

Emergency Stop triggers from various sources makes the entire system safer in the occurrence of an undesirable or dangerous event. The Emergency Stop is generated by an independent network which will be discussed later in this chapter.

### 5.1.2 The Automation Microcontroller Module

The Automation Microcontroller module is responsible for the control of the system's actuators which include the Armature Drive Motor and the Detection Unit Drive Motor as well as the switching of the Test Current Supply via an IGBT. It also receives input signals from the physical system to indicate the system status and the occurrence of events whether desirable or undesirable.

These input signals include the signal indicating the detection of a pair of bars, labeled "u2_EX1_Bar_Dect", the signal that indicates that the Detection Unit has reached its initial position, labeled "Detect_Unit_Switches", as well as Emergency Stop signals, labeled "EmgcyStop_gui" and "EmgcyStop_SW\&Intlks". All of the above mention signals, except "EmgcyStop_gui", are generated by independent networks which will be discussed later in this chapter. The "EmgcyStop_gui" signal is generated by the Communication Microcontroller to inform the Automation Microcontroller that an Emergency Stop has been initiated via the GUI. See Figure 52 for a representation of the Automation Microcontroller Module and Appendix M for the complete circuit schematic.


FIGURE 5-2: THE AUTOMATION MICROCONTROLLER MODULE

The Automation Microcontroller is set up in exactly the same way as the Communications Microcontroller. The interconnections between the Automation and Communications microcontrollers are summarised in the respective Microcontroller Port Utilisation tables in Appendix K. The connections from the Automation Microcontroller to other devices are also summarised in the Automation Microcontroller Port Utilisation table in Appendix K.

The input to External Interrupt 0, P3.2, is an OR and NOR gate network which triggers the interrupt in the occurrence of any of the two Emergency Stop events ("EmgcyStop_gui" and "EmgcyStop_SW\&Intlks") or the occurrence of the bar detection event ("Detect_Unit_Switches"). The input to port pin P1.5 is also an OR gate with "EmgcyStop_gui" and "EmgcyStop_SW\&Intlks" as input signals. The reason for this becomes apparent when the reader recalls the discussion in Chapter 4 concerning the External Interrupt 0 ISR for the Automation Microcontroller.

The first task undertaken by the interrupt service routine is to test port pin P1.5. If this pin is High (1) then EXO was triggered by the initiation of an emergency stop".

As soon as External Interrupt 0 (EX0) is triggered, the associated ISR first checks if P1.5 is High (1), indicating that any one of the Emergency Stop sources had been triggered. If this is the case, the system shut down and controller power-down procedures are entered into. If this not the case and P1.5 is Low (0) then the interrupt was triggered due to the detection of a pair of bars, i.e. the"Detect_Unit_Switches" signal. Hence this port pin is only used to decipher whether an interrupt was initiated due to an emergency stop or the detection of a pair of bars.

### 5.1.3 The Bar Detection Module

The Bar Detection module is responsible for alerting the Automation Microcontroller when a pair of bars has been detected. The actual detection of each copper bar on the commutator of the armature under test is undertaken using optical sensors that detect the reflection of an emitted laser beam. The Omron E3X-NA11 amplification unit together with the Omron E32-DC200 fiber optic unit (with reflective sensors) was used to carry out this task. See Appendix J for complete datasheets. The combination of these two units allow for the accurate detection of a copper bar from a distance of between 50 mm and 70 mm above the surface of the commutator. See Figure 5-3 and Figure 5-6 for images of the commutator and the copper bars that are to be detected.


FIGURE 5-3: TYPICAL COMMUTATOR OF AN ARMATURE UNDER TEST


FIGURE 5-4: COPPER BARS ON A COMMUTATOR
The above images depict a typical commutator, however in this case, the reader will notice that there are grooves present between each copper bar. Grooves are created by a process called Undercutting which entails the use of a motorised, revolving, circular saw blade typically 20 mm in diameter. These grooves are not present in all commutators that are to be tested. In some instances the armature that is to be tested still has an epoxy resin (from the VIP stage of the armature refurbishing process) between the bars. Due to the Turning stage (using a lathe) in the armature refurbishing process the surface of the commutator is smooth, with the copper bars and the epoxy resin being exactly the same level. It is for this reason that a high accuracy proximity sensor was abandoned. After testing various sensors, the optical sensor produced the best results and proved to be the most reliable means of detecting the copper bars.

The sensor is set on Light On mode. In this mode, an open collector NPN transistor, which is the output of the Omron E3X-NA11, is switched on when a reflected beam is detected by the reflective sensor.

The optical sensors are supplied with +15 V and the outputs from these sensors provide a clock pulse to respective positive-edge-triggered D flip-flops. The output of the D flip-flops provide the two inputs to the NAND gate which in-turn triggers the External Interrupt 1 pin on the Automation Microcontroller when driven low (0). This signal, "u2_EX1_Bar_Dect", must go low (0) only when a pair of bars has been detected. It must return to high (1) when the D flip-flops are cleared by the Automation Microcontroller and go low (0) again when the next pair or bars are detected. The network shown in Figure 5-5 fulfils the above triggering requirements. See Figure 5-7 for a timing diagram for the bar detection network.


FIGURE 5-5: BAR DETECTION NETWORK

The voltage divider resistor-network ensures that 5 V is present at the output when the transistor is off (implying that no bars have been detected) and $0 \mathrm{~V}\left(\mathrm{~V}_{\mathrm{CE}}\right.$ to be exact) is present at the output when the transistor is on (implying that a bar has been detected). A 6.2 V zener diode, with a very low response time, or a Tranzorb, depending on the operating environment, is placed in parallel with the output resistor for protection purposes to ensure that the output of the voltage divider resistor-network will not exceed 6.2 V .

Initially, the network that was used as a level shifter to provide a TTL level input to the digital interface from the optical sensor output of 0 V to 15 V was a simple series resistor and zener diode network as depicted in the figure below.


FIGURE 5-6: INITIAL LEVEL SHIFTER NETWORK

It may seem like an adequate solution, however, when one considerers the fact that the zener diode has response time, although very small, one will become aware of a potential problem that may arise when using this series network. The instant that the NPN transistor in the output circuit of the optical sensor is switched off, the zener diode is still essentially "off" as it does not respond instantaneously to the applied source. Ideally, the zener diode will be seen as an open circuit to the rest of the network for this period of time.

This being the case, the output of this series network, which is the input to the NOT gate, will for all intents and purposes, be pulled up to +15 V by the series resistor which acts as a pull-up resistor for the period before the zener diode responds or "switches on". This +15 V input is well above the absolute maximum rating for the IC and will ultimately damage it. The author used the word ultimately because, due to the very small response time of the zener diode, the IC will only be exposed to +15 V for a very short period. The IC may therefore not be damaged instantly however, repeated exposure to such high input potentials will damage the IC over time.

It is for the above reason that the voltage divider comprising of a $1 \mathrm{k} \Omega$ and $2 \mathrm{k} \Omega$ with adequate protection was used. This network produces a 5 V drop across the $1 \mathrm{~K} \Omega$ resistor when a +15 V source is applied.

$$
\mathrm{V}_{\mathrm{R} 1 \mathrm{~K}}=\frac{1 K}{1 K+2 K} \times 15 \mathrm{~V}=5 \mathrm{~V}
$$

This network ensures that the input to the NOT gate is exposed to a maximum of 6.2 V which is within recommended operating range for the IC.

The output of the resistor-zener network enters a NOT gate which inverts the signal producing an output high (1) when a bar has been detected and a low (0) when no bars have been detected. The output of this NOT gate clocks a positive-edge-triggered D flip-flop whenever a bar has been detected. Because the D input of the flip-flop is tied high (Vcc) when clocked, the output of the flip-flop, Q, goes high. The output of the D flip-flop provides the input to the NAND gate which triggers the external interrupt pin on the Automation Microcontroller. The microcontroller clears both D flip-flops in order to put them in a known state, as soon as it enters the Interrupt Service Routine (ISR) that it vectored to when a pair of bars have been detected.


FIGURE 5-7: TIMING DIAGRAM FOR THE DETECTION NETWORK

The discussion that follows is with reference to Figure 5-7 and Figure 5-5 and describes the operation of the Bar Detection module. Assume that the commutator is rotating slowly and Sensor 1 detects a bar, the output of the NOT gate [point A] is
high (1). The low-to-high transition (positive edge) clocks the D flip-flop producing an output [at point F] that is also high (1). If, at this point, Sensor 2 has not yet detected a bar the output of the NAND gate remains high (1). The commutator will continue slowly rotating with Sensor 1 directly over it's bar until Sensor 2 detects a bar. For the purposes of this explanation, assume that Sensor 2 has also detected a bar at the same time that Sensor 1 has detected a bar (Ideal situation with an ideal commutator) the output of the NOT gate [point B], is high (1). The low-to-high transition (positive edge) clocks the D flip-flop producing an output [at point E ] that is high (1). With both the inputs to the NAND gate being high (1), the output [at point G] goes low (0).

This high-to-low transition (negative edge) triggers External Interrupt 1 of the Automation Microcontroller. The microcontroller clears both flip-flops in the associated ISR. When rotation resumes, control is handed back to the Bar Detection module. At this point both sensors indicate that they detect a bar. This is because the Armature Rotation Drive Motor was stopped as soon as both bars were detected. The outputs of the NOT gates at both point $A$ and point $B$ are now high (1). These high outputs however, do not clock the D flip-flops as they are positive edge triggered. Since the clock did not go low (0) before going high (1), the outputs of the flip-flops remain cleared (0) implying that the output of the NAND gate remains high (1). As the commutator rotates the sensors will pass over the groove (or epoxy resin gap) between a pair of consecutive bars.

This causes the output of the sensors to produce a low (0), via the NOT gates. On the detection of the next bar, a low-to-high transition will be created and this positive edge will again trigger the D flip-flops. It is thus clear that the Bar Detection module only detects the NEXT pair of bars to be tested by using positive edge triggered flipflops to reject the high (1) signal from the sensors when they are still over the pair of bars that were previously detected. Note that although theoretically both bars should be detected at the exact same time by their respective optical sensors, this is not the case practically. There are two reasons for this, one being that when the commutator is undercut, some of the copper is also cut into producing bars and gaps of varying widths. The other reason is dirt, spots or marks on a bar that do not allow for the reflection of the laser. If the bars and the gaps between bars were the exact same
width throughout the circumference of the commutator and the commutator was clean, as in the case of a new commutator, both bars will be detected at the exact same time.

### 5.2 The Data Acquisition Module

The Data Acquisition module is responsible for measuring the difference in potential between two successive bars, signal conditioning to reject any inputs outside the expected input range and converting the input analogue signal to a sixteen-bit word that is to be transmitted to the Graphic User Interface (GUI) via the Communications Microcontroller. See Figure 5-8 and Figure 5-9 for the block diagram describing this module.


FIGURE 5-8: BLOCK DIAGRAM FOR THE DATA ACQUISITION MODULE


FIGURE 5-9: DETAILED BLOCK DIAGRAM FOR THE DATA ACQUISITION MODULE

Before discussing this module any further it is important for the reader to know the type and magnitude of the input signal that is to be measured. The test supply is a maximum of $+15 \mathrm{~V} / 400 \mathrm{~A}$. The typical potential difference (or volt drop) expected to
be measured between a pair of successive bars, on any armature that is to be tested, is in the range of between 100 mV and 350 mV for a healthy winding. Before the test begins the test technician will verify that readings within this range are produced by measuring the volt drop across the first pair of bars and, if need be, varying the magnitude of the test supply or varying the arc length of the test supply probes or both to ensure that the reading produced is within the stipulated range.

The technician will thereafter measure the volt drop across at least five other successive pairs of bars that lie within the arc length of the test supply probes in order to verify the range. If the readings on these bars fall outside the range that was set on the first pair of bars the implication is that the windings of first pair of bars are unhealthy or damaged. In this case the input range must be set and verified on one of the other five measured pairs of bars.

The expected input range discussed above only applies to healthy windings, i.e. windings that are not open circuited, shot circuited or damaged. If a winding is open circuited the volt drop across the connected pair of bars will be equal to the supply potential. If a winding is short circuited the volt drop across the pair of connected bars will be zero volts. If a winding is damaged the volt-drop across the connected pair of bars will fall outside the preset variance (or tolerance) from the reference reading specified at the beginning of the test. The input signals are DC with no expected AC components. Any AC components encountered are regarded as noise and will be rejected and/or filtered.

A precision Instrumentation Amplifier, the INA 118 is used to acquire the potential difference (or volt drop) between two successive bars. See Appendix J for the complete datasheet for the INA 118. This amplifier features amongst other things, a high Common Mode Rejection (CMR) of 110dB (at a gain of 10) and input protection of up to $\pm 40 \mathrm{~V}$. It also offers a non-linearity of typically $\pm 0.0005 \%$ of the full-scale range (at a gain of 10). Some of the specifications mentioned above are stipulated at a gain of 10 . This is because a gain of 10 is set (using the external resistor, $\mathrm{R}_{\mathrm{G}}$ - see datasheet) to amplify the input signal from the hundreds of millivolts to the volt range. Hence, an input of 350 mV will be amplified to 3.5 V . This is done in order to utilise the full input range of the sixteen-bit Analogue-to-Digital Converter hence
maximising the 16 -bit resolution and reducing the effects of any conversion errors should they occur.

A sixteen-bit, successive approximation, Analogue-to-Digital Converter, the MAX 1166 , with an input range of between -0.3 V and $\mathrm{V}_{\text {Ref }}(4.096 \mathrm{~V})$ is used to convert the input signal to a sixteen-bit word (2 eight-bit wide, parallel output words). See Appendix J for the complete datasheet for the MAX 1166. The operation of the ADC was discussed in detail in Chapter 4, under the section entitled ADC Control. The ADC was set-up to make use of the internal reference voltage as prescribed in the datasheet and shown in Figure 5-10.


FIGURE 5-10: ANALOGUE-TO-DIGITAL CONVERTER NETWORK

The ADC features, amongst other things, sixteen-bit resolution, a high speed sampling rate, an eight-bit wide parallel output and an accuracy of $\pm 2$ LSB (Least Significant Bit). With an internal $\mathrm{V}_{\text {Ref }}$ of 4.096 V and sixteen bit resolution, the smallest voltage increment that the input signal can broken down into is:

$$
\text { Resolution in Volts }=4.096 / 65536=62.5 \mu \mathrm{~V}
$$

i.e. each digital bit is equal to an analogue step of $62.5 \mu \mathrm{~V}$.

As mentioned earlier, the input signal is amplified by a factor of 10 , the true analogue step size (after being scaled down in software) is $6.25 \mu \mathrm{~V}$. Similarly, the true input voltage range after being scaled down by software will be 0 to 350 mV . This implies that a variance of

$$
\text { Variance }(\%)=\frac{6.25 \mu \mathrm{~V}}{350 \mathrm{mV}} \times 100=1.786 \times 10^{-3} \%
$$

can theoretically/ideally be detected by the system. This value has two important connotations, the first being the fact that the smallest input change that can be detected is well below $1 \%$, hence the percentage variance from the reference reading can be calculated with a great degree of accuracy. The second connotation is that the ADC error of $\pm 2$ LSB will be almost negligible when considering the percentage variance from the reference value.

Recalling that the input range for the ADC is between -0.3 V and $\mathrm{V}_{\text {Ref }}(4.096 \mathrm{~V})$, the ADC has to be protected from any inputs outside this range as they will potentially damage the ADC. Out of range input signals can be produced in two ways, the first being due to an open circuit. In this case, the potential difference across the pair of bars that are connected to an open circuited winding will equal to the potential of the test supply current (which may be as high as 15 V ). The second way an out of range reading can be produced is by the reversal of the orientation of the test probes with respect to the test supply probes.

This means that when the test current positive probe is to the right of the negative probe and the positive test probe is to the left of the negative test probe (or versa-visa) a negative reading of equal magnitude to the positive reading will be produced. This situation can arise when the test technician setting up the test reverses the polarity of the test supply or when the test technician is taking a manual reading and uses an independent (unauthorised) set of test probes to take a manual reading and unknowingly reverses the orientation of the polarity of the inputs with respect to the potential of the test supply probes. Although this situation should not occur, protection has to be designed into the system to prevent any hardware damage should
this situation somehow occur. The reader may ask why an ADC with an equal positive and negative input range (e.g. $\pm 5 \mathrm{~V}$ ) is not used.

The answer to this is - the expected input range is between 0 and 3.5 V (after amplification). And with a sixteen-bit ADC that has a positive input range (eg. +5 V ), all sixteen bits are dedicated to conversions within this positive range. If a sixteen-bit ADC with an equal positive and negative range was to be used, eight bits will be dedicated to the positive range, 0 to +5 V , and the other eight bits will be dedicated to the negative range, 0 to -5 V . Hence only an eight bit resolution can be expected for the readings of importance i.e. those within the 0 to 5 V range. The eight bits dedicated to the conversion of negative values will only be used in events of unwanted or undesirable readings that are produced by an incorrect system set up or use. In the author's opinion, the eight bit resolution used for the negative range of inputs is wasted. The author has hence elected to use a sixteen-bit ADC with only a positive input range and has devised a method of rejecting all unwanted and potentially damaging input signals. This method will be discussed in the paragraphs that follow.

With reference to Sheet 4 of the circuit schematic found in Appendix M, the first stage of the data acquisition module is the INA 118 instrumentation amplifier. This stage is followed by a filtering stage that comprises capacitors of various values which facilitates more efficient filtering over a range of frequencies. Seeing as the output of the instrumentation amplifier is expected (and required) to be purely DC in nature, any AC components found on this signal must be filtered before the signal progresses to the next phase of the system. It is for this reason that capacitors were used as low-pass filters instead of low-pass high order passive or active filters with cut-off frequencies set very low (almost zero Hertz, in this case).

In the phase that follows, three Voltage Followers (or Buffers) makes three identical copies of the original signal. A Voltage Follower is simply an Op-Amp (LM 741 in this case) with its output fed directly into its inverting input. The non-inverting input is the input pin for the signal. This network produces an output with zero gain, i.e. an output that is equal to the input. A fourth Voltage Follower is placed at the input to the ADC .

Note that all the Op-Amp and Comparator ICs that are used make provision for a potentiometer that is used to nullify the output offset voltage. These potentiometers are also used for "tuning" purposes to ensure that the signal which is the input to the $A D C$ is equal to the signal at the input end of the data acquisition module provided that the magnitude of the signal is within the allowable ADC input range.

Three identical copies of the input signal are made purely to maintain the integrity of the input signal to the ADC. Two comparator stages are required to determine whether the input signal is outside the ADC input range. These two stages are in parallel implying that they each require a perfect copy of the original input signal. The third copy of the input signal flows directly to the ADC input via an analogue switch. If only one signal was used in each of the comparison stages before being input to the ADC, the integrity of that one signal would be compromised, i.e. the ADC input signal will vary from the original input signal to the data acquisition module.

Recalling that the input of the ADC must be within the -0.3 V to 4.096 V range, a comparison must be done in order to reject all inputs outside this range. This comparison is done in two parallel stages. The first stage determines if the input signal is less than the ADC reference voltage, $\mathrm{V}_{\text {Ref }}$, which is equal to 4.096 V . In order to do this a comparator (the LM 311) is used with the input signal connected to the comparator's inverting input and a reference voltage connected to the non-inverting input pin. The reference voltage is set up using a voltage divider network that comprises a $2 \mathrm{k} \Omega$ and a $9 \mathrm{k} \Omega$ resistor both with a $1 \%$ tolerance. With these values the expected reference at zero percent variance is:

$$
\mathrm{V}_{\mathrm{Ref}}=\frac{9 k \Omega}{9 k \Omega+2 k \Omega} \times 5 \mathrm{~V}=4.091 \mathrm{~V}
$$

with $\mathrm{a} \pm 1 \% \mathrm{~V}_{\text {Ref }}$ variance of the range between 4.076 V and 4.105 V .

The output of LM 311 is open-collector, with pin 7 being the collector end and pin 1 being the emitter end of the output transistor. Connecting the collector (pin 7) via a pull-up resistor to the +5 V supply and connecting the emitter (pin 1) to ground, the comparator outputs a High (1), i.e. +5 V , when the non-inverting input is greater than the inverting input and a Low ( 0 ), 0 V (or $\mathrm{V}_{\mathrm{ce}}$ ) when the inverting input is greater than
the non-inverting input. The output of this comparison stage is connected to the first of two inputs of an AND gate.

The second comparison stage is tasked to ensure that all negative input signals are rejected. Here the input signal is connected to the non-inverting input pin of the comparator (LM 311) and the reference is connected to the inverting input. The reverence voltage, $\mathrm{V}_{\text {Ref, }}$ is set to 0 V by connecting the inverting input directly to ground. However, the reader should note that a voltage divider network which is set up between -15 V and ground (Gnd) is provided in the event that a slightly negative reference is required due to the operating environment. To set a 0 V reference using this network the resistor to ground is replaced with a physical jumper and the resistor to the negative supply is not inserted. The output of this comparison stage is connected to the second of the two inputs to the AND gate.

When the input signal is within range the first comparator stage will produce a High input signal to the AND gate because the potential at the inverting pin will be greater than that at the non-inverting pin. The second comparator stage will also produce a High input signal to the AND gate for the same reason. The output of the AND gate is hence High. The output of the AND gate ("V_RangeDetect") provides the input to the Communication Microcontroller's P0.2. Before a reading can be taken this input port (i.e. P0.2) is tested to verify if it is High (1).

If this is the case, the Analogue Switch (MAX 4622) is switched on by the Communication Microcontroller port pin P0.0, allowing the signal to pass through to the ADC input pin. See Appendix J for a complete datasheet for the MAX 4622. If this port pin is Low, the analogue switch is left off, connecting the ADC input pin to ground. The MAX 4622 analogue switch has a low on-resistance, with a normally open, normally closed and a common pin. It can be operated from a bipolar supply of $\pm 18 \mathrm{~V}$, although in this case the operating supply is $\pm 15 \mathrm{~V}$. This allows the analogue switch to control any input within this range without any damage which makes it perfect for this application. When the input pin of this device is low, as in the case where the input signal is found to be outside the allowable range, the common pin is "connected" to the normally closed pin which in this case is connected to ground. When the input pin of this device is High, as in the case where the input signal is
found to be within the allowable range, the common pin is "connected" to the normally open pin which in this case is connected to output pin of the first voltage follower stage which represents the input signal to the data acquisition unit.

For completeness, if the input signal is higher than the preset reference, $\mathrm{V}_{\text {Ref }}$, of the first comparison stage as in the case where an open circuit is detected on a winding connected to the pair of bars under test, the output of the comparison stage will be Low. This is because the inverting input will be at a higher potential than the noninverting input. The output of the AND gate will therefore be Low hence ensuring that the Communication Microcontroller keeps the analogue switch off. This in turn ensures that the ADC input remains connected to ground, i.e. 0 V , and not to the out-of-range input signal.

If the input signal is lower than the preset reference, 0 V , of the second comparison stage, as in the case where the orientation of the test probes is reversed with respect to that of the Test Supply probes, the output of the comparison stage will be Low. This is because the inverting input will be at a higher potential than the non-inverting input. The output of the AND gate will be Low ensuring that the Communication Microcontroller keeps the analogue switch off. This in turn ensures that the ADC input remains connected to ground, i.e. 0 V , and not to the out-of-range input signal. It is in this way that all out-of-range inputs are rejected by the data acquisition module.

This method was not the first approach that was tried. After much research and experimentation with adaptive (variable) gain Op-Amp networks, arithmetic using a number of Op-Amp stages, scaling and using various switching devices such as relays, BJTs and FETs, this approach was found to be the simplest, most effective and most accurate method of rejecting out-of-range input signals while still maintaining the integrity of the original input signal.

## Chapter 6

## Additional Features

In order to gain a greater level of accuracy and provide engineers and technicians with more valuable data, three additional features were added to the basic system. These include:

- The ability to automatically take repetitive readings on a single pair of bars
- Automatically record each reading and the average of all the readings for a pair of bars on an Excel Spreadsheet. Also automatically saving Excel Spreadsheets at the end of tests.
- Calibration of the system using the GUI Calibration Tool.


### 6.1 Automatic Repetitive Readings

The system has now been setup to take one hundred (100) consecutive readings in roughly $1000 \mu$ s intervals. This implies that the duration for one complete, one hundred reading recordings is roughly 100 ms . This is achieved by introducing a variable called "MultiReading" in the Calculation Subroutine of the GUI. This variable is loaded with a value of one hundred and decremented each time the Calculation Subroutine is called. As long as the value held in variable "MultiReading" is not equal to zero, the ASCII code for the character "E" is transmitted to the Communication Microcontroller. When "MultiReading" holds zero, the ASCII code for the character " S " is transmitted.

Additions for each reading, as well as the average of the 100 readings for each bar are to be recorded in an Excel Spreadsheet. This Spreadsheet is created as an object, when the Load button is.

The author has setup the Spreadsheet such that each row from column 1 to 100, holds "raw" readings as they are acquired. Column 102 of each row will contain the average for that row. Further, the reference reading raw data and the average calculated is represented in bold font.

After all 100 readings have been recorded the average is calculated using a For Loop to read the data from each column in the current row and adding it to the sum of the previous readings in that row. The sum of all 100 readings is recorded in variable SumBarReading which is divided by 100 to acquire the average. This average is stored in variable AvgBarReading and is recorded in column 102 in the current row.

The Excel Spreadsheet containing all the data recorded for a test is automatically saved in the same default location as the Test Fault Log files under the Name, Date and Time of the test when the Save or Print button is clicked.

Using these Spreadsheets data can be further analysed by makingthrough the use of graphs and other mathematical tools.

Also included as an additional feature is the systems ability to indicate a possible Open or Short Circuit. A Short circuit is identified when the system records a value of zero for more than 50 repetitive readings on the same pair of bars. This count takes place in variable "ZeroIn". It should be noted that the ADC represents zero volts by 011110000111 1000. The decimal representation of this code, broken into a High and Low byte is 120120 . This is exactly the condition that is tested in order to increment variable, "ZeroIn".

If ZeroIn is greater than 50 , the Spreadsheet recordings for each cell of this 100 cycle reading will be changed to "Adjusted" and the average reading held in column 102 of
that row will be changed to 0 . The value held in variable "AvgBarReading" is also changed to 0 .

In the case of an Open Circuit, the reader will recall that the Input Analogue Circuitry alerts the Communication Microcontroller when the reading is out of range. The Communication Microcontroller then transmits 1111111111111110 to the GUI. Note that this is a unique code that is only transmitted on the occurrence of an out of range reading. Recall that if ever this code is encountered during a normal reading acquisition, the Communication Microcontroller converts the acquired code to 1111 111111111111 before transmitting it to the GUI. Also, note that the port pin on the Communication Microcontroller i.e. P0.2 is set high by the input analogue circuitry to indicate that the orientation of the system input test probed is revered with respect to the polarity of the Test Supply Current probes.

This condition will however never occur during the automated process provided that the test was set up correctly by the test technician. This implies that whenever 1111 111111111110 is encountered during a reading acquisition cycle, it can only indicate that an Open Circuit has been detected. When this value is encountered by the Calculation Subroutine as decimal 65534, variable/flag "StnBit_WDflg" is set to true.

### 6.2 The Calibration Tool

The ideology behind the GUI Calibration Tool is to facilitate calibration by the system administrator whenever necessary. This tool aids the calibration process which has to be carried out by specially trained personnel. Presently, the Calibration Tool is used to simply acquire and record the system readings for a respective known injected value. The author is experimenting with software calibration techniques and in the future will implement algorithms based on these techniques to enable software calibration of the system.

This will imply that the user can account for any offsets and variations that may occur over time in software as opposed to hardware tuning. To demonstrate the ability and possibilities of the Calibration Tool, the author has included an algorithm based on the nullification of errors using two linear Best-Fit curves. A true size representation of the calibration screen can be found in Appendix N and a screen capture of the calibration screen is shown in Figure 6-2.


FIGURE 6-2: SCREEN CAPTURE OF THE CALIBRATION SCREEN

The Calibration Screen is a separate form that is called by clicking on the Calibration Setup button on the main GUI. The user is then prompted for the Administrator's Password. The Calibration Screen is only made visible if the correct password is entered.

As shown, there are two Text Boxes, one Check Box and one Button for each of the forty readings that are to be taken. An injection value is specified for each reading with an allowable variance of $\pm 1 \mathrm{mV}$. The voltage value being injected into the controller's data acquisition module is to be entered into the first Text Box before the button is clicked.

When the button is clicked, the value that the data acquisition system acquires for the voltage that is being injected is recorded in an Excel Spreadsheet along with the injection value that was entered in the first Text Box. The acquired value is also displayed in the second Text Box for the present reading. Note that an average of 100 readings is also used here however, only the average is recorded in the Spreadsheet. The CalibrationSub subroutine is responsible for this process. See Appendix C for the subroutine coding.

After a reading has been taken the button is disabled and the Check Box is checked to indicate completion. Readings can be retaken by the Re-Take Reading button. After all forty readings have been taken the Calculate And Save button is clicked to perform the relevant calculations and save the calibration factor in a specified file.

The calculation carried out here is completed in three phases. The first phase involves the calculation of the gradient and the Y-intercept of the best-fit linear plot for the injection values that were entered in the first Text Box. The second phase entails the calculation of the gradient and the Y-intercept of the best-fit linear plot for the values acquired by the data acquisition system which were displayed in the second Text Box. These plots are obtained by using the Least Squares Approximation technique. The following equations were used to calculate the gradient and the Y-intercept respectively, for each plot.

$$
\begin{align*}
& \text { Gradient }=\frac{\mathrm{n} \times\left(\text { sum of } x_{i} \times y_{i}\right)-\left(\operatorname{sum} \text { of } x_{i}\right) \times\left(\operatorname{sum} \text { of } y_{i}\right)}{\mathrm{n} \times\left(\operatorname{sum} \text { of } x_{i} \times x_{i}\right)-\left(\operatorname{sum} \text { of } x_{i}\right)^{2}} \\
& \quad \text { Y-intercept }=\left(\left(\text { sum of } y_{i}\right)-\text { Gradient } \times\left(\operatorname{sum} \text { of } x_{i}\right)\right) / \mathrm{n}
\end{align*}
$$

Where, $\mathrm{n}=$ total number of points or samples
$i=$ point or sample index
$x=\mathrm{x}$ coordinate of a point or sample
$y=y$ coordinate of a point or sample

## Source: Calculus and Analytic Geometry ( $9^{\text {th }}$ Edition) [17]

Once the gradient and Y-intercepts for each best-fit linear plot has been calculated, a straight line equation for each is derived with the value of $y$ being the same for both and representing the point or reading number.

$$
\begin{array}{rlr}
\mathrm{y}_{\text {Injection }} & =\mathrm{m}_{\text {Injection }} \mathrm{X}_{\text {Injection }}+\mathrm{c}_{\text {Injection }} & 6-3 \\
\mathrm{y}_{\text {Acquired }} & =\mathrm{m}_{\text {Acquired }} \mathrm{x}_{\text {Acquired }}+\mathrm{c}_{\text {Acquired }} & 6-4
\end{array}
$$

Now, $\mathrm{x}_{\text {Injection }}$, represents a value on the best-fit linear plot for the injected voltage for a given reading, point or sample as represented by the $y$-coordinate $y_{\text {Injection }}$, for that point. For example, the coordinate for point $(1,0.25)$ means reading number 1 , with a value of $0,25 \mathrm{~V}$ as represented by ( $\mathrm{y}_{\text {Injection }}, \mathrm{X}_{\text {Injection }}$ ). The same applies to the acquired readings and plots. See Figure 6-3 for a diagrammatic representation of the above paragraph.


FIGURE 6-3: DIAGRAMMATIC REPRESENTATION OF THE LEAST SQUARED APPROXIMATION METHOD

Phase three of the calculation entailed equating both of the above equations ( $\mathrm{y}_{\text {Injection }}=$ $y_{\text {Acquired }}=$ point number) and calculating the calibration factor as follows:

$$
\begin{array}{rlr}
\mathrm{m}_{\text {Injection }} \mathrm{X}_{\text {Injection }}+\mathrm{c}_{\text {Injection }} & =\mathrm{m}_{\text {Acquired }} \mathrm{X}_{\text {Acquired }}+\mathrm{c}_{\text {Acquired }} & 6-5 \\
\mathrm{~m}_{\text {Injection }} \mathrm{X}_{\text {Injection }} & =\mathrm{m}_{\text {Acquired }} \mathrm{X}_{\text {Acquired }}+\mathrm{c}_{\text {Acquired }}-\mathrm{c}_{\text {Injection }} & 6-6 \\
\mathrm{X}_{\text {Injection }} & =\left(\mathrm{m}_{\text {Acquired }} \mathrm{X}_{\text {Acquired }}+\mathrm{c}_{\text {Acquired }}-\mathrm{c}_{\text {Injection }}\right) / \mathrm{m}_{\text {Injection }} & 6-7
\end{array}
$$

Rearranging,

$$
\mathrm{x}_{\text {Injection }}=\mathrm{x}_{\text {Acquired }} \times\left(\mathrm{m}_{\text {Acquired }} / \mathrm{m}_{\text {Injection }}\right)+\left(\left(\mathrm{c}_{\text {Acquired }}-\mathrm{c}_{\text {Injection }}\right) / \mathrm{m}_{\text {Injection }}\right)
$$

The calibration factor therefore aims to get the best-fit Injection plot as close to the best-fit acquisition plot as possible for the entire range of input values. This is accomplished by manipulating the acquired value, $\mathrm{x}_{\text {Acquired }}$, such that it is equal to the injected value $\mathrm{x}_{\text {Injection }}$, for that specific reading number. This manipulation is carried out in the Calculation Subroutine by implementing Equation 6-8 as follows:

$$
\mathrm{x}_{\text {Calibrated }}=\mathrm{x}_{\text {Acquired }} \times\left(\mathrm{m}_{\text {Acquired }} / \mathrm{m}_{\text {Injection }}\right)+\left(\left(\mathrm{c}_{\text {Acquired }}-\mathrm{c}_{\text {Injection }}\right) / \mathrm{m}_{\text {Injection }}\right)
$$

Where,
$\mathrm{x}_{\text {Calibrated }}$ is the true value calculated from the system acquired value, $\mathrm{x}_{\text {Acquired. }}$

This calibration factor is then saved along with the date of the calibration procedure in a file entitled Calibration1 which is located in a specially created folder named Calibration ${ }^{6}$ in the Program files folder on the C drive. Each time the Load button on the GUI is clicked this file is opened and the calibration factor is loaded into variables "gradient" and "intercept" which are used in the Calculation subroutine. If on first use the system has not been calibrated or the calibration file has been erased, a default value of 1 is loaded into "gradient" and 0 into "intercept". The user is also made aware that the system needs to be calibrated by means of a message box.

Each time the system is calibrated, the previous calibration factor and date are replaced by the new ones. In order to facilitate this calibration functionality, the Communication Microcontroller has to be made aware that it should only take a reading when it is prompted and not communicate with the Automation Microcontroller or any of the sensor or transducer modules. This is accomplished by transmitting the ASCII code for the letter " H " when any one of the forty calibration buttons on the calibration screen are clicked. Also, when one of these buttons are clicked the CalibFlagClear flag is set to "False". This is done so that when this flag is tested at the beginning of the Calculation subroutine and is found to be false the Calibration subroutine is called to handle the incoming data. When this flag is set to "True", indicating that a test is in progress the Calculation Subroutine handles all incoming data.

[^1]
### 6.3 Multiple User Names And Passwords

Access to this functionality is obtained through clicking on the View User Profile button on the GUI. The user will then be prompted to enter the Administrator's Password before proceeding. The Administrator can then allow a user to enter his name and personal unique password. Once all entries have been made, the Administrator clicks on the Enter New User button. This opens (or creates if not in existence) a file named "B_2_B_Pwd" in the Calibration folder which is found in the Program files folder on the C drive. The new user details are then added to this file.

Note that if the Password and Confirm Password entries do not match the user is asked to reenter a password. The Administrator also has the option of deleting a user's records from this file, thus effectively revoking his/her rights to access the system. When a user intends on using the system, he/she enters a password and clicks on the GUI Enter button. This action opens the password file "B_2_B_Pwd" and verifies if the password exists. If it does exist, the User Name associated with that password is automatically displayed in the Name Text Box on the GUI. See Figure 64 for a screen capture of this functionality.


FIGURE 6-4: MULTIPLE USER NAMES AND PASSWORDS SETUP FRAME

### 6.4 GUI Special Function (Simulator) Controls

The GUI Special Function Controls have no bearing on the GUI functionality. These controls are made available to a SuperUser, in this case only the author, who has a unique user name and password. The Special Function Controls allows the SuperUser to simulate inputs from the Controller. It is thus in essence a Graphic User Interface Simulator. As the GUI and the controller were developed in parallel there was no means of assessing the GUI when it became necessary to test it in terms of its responses to input prompts and data, as well as the outputs it generated based on its calculations.

A simulator had to therefore be developed to mimic the controller and the data that it transmitted. The simulator functionality is useful in the event of a system failure or malfunction where the author can determine if the GUI or the controller or both is at fault by testing them independently. These controls are also useful for de-bugging purposes in the event of future modifications and additional functionalities. In order to display the simulator screen (or frame) the Super User first clicks on the View Controls button that is found in the GUI Special Function Controls frame depicted in the Figure 6-5.


FIGURE 6-5: GUI SPECIAL FUNCTION CONTROLS FRAME

Upon clicking this button an identification frame appears prompting the Super User for a username and password, as shown in Figure 6-6.


FIGURE 6-6: SUPERUSER IDENTIFICATION FRAME
When the correct user username and password is entered, the Simulator is made available to the SuperUser as shown in the figure below. The Super User simply clicks on the Exit button to exit from this frame and returns to the default frame that is depicted in Figure 6-5.


## FIGURE 6-7: GUI SIMULATOR THAT SIMULATES CONTROLLER TRANSMISSION

Recall that the OnComm procedure is developed such that it is initiated when received data is present in the serial port buffer. This data is then copied from the buffer into the variable, SerIn,
Let Serln = MSComm1.Input
before the Select Case routine is invoked.
In order to mimic the controller, the data must be received in much the same way as when data is being received from the controller. The problem however arises when
one considers that there will be no data present in the serial port buffer. This means that the OnComm procedure will never be initiated. The simulator has to therefore input data (mimicked received data) to the very first storage facility after the serial port buffer. This facility is the variable, Serln.

The simulator therefore writes all data that was entered into the "Mscom In Sim" input box to this variable and since the Select Case routine is not initiated automatically as in the case of the OnComm procedure it has to be manually initiated using the Case Select button. The GUI transmitted output may also be read in the "Out" text box provided that the code simulated writes to the original serial port as well as the Out text box. Code Extract 6-5 shows the source code for the Case Select button.

Note that the code is exactly the same as that of the OnComm procedure except for the fact that the mimicked data is being read from Text Box 17 and is copied directly into Serln.

## Chapter 7

## Test Results

Various tests were conducted with results recorded to measure the system's performance and verify the system process flow and event sequencing. Tests were carried out in two phases. The first phase was aimed at quantifying the Data Acquisition accuracy, repeatability and all round performance. The second phase was aimed at verifying the automated flow process and to ensure that the correct sequence of events was followed as programmed.

For the first phase of tests, forty voltage values were injected at intervals of $10 \mathrm{mV} \pm$ 1 mV and the GUI Calibration Tool was used to acquire and record the forty respective system readings. The readings are taken in exactly the same manner as it would be in a normal test, i.e. 100 successive readings which will be averaged to produce the final value for the respective injected voltage value.

The first test carried out in this phase was aimed at determining the repeatability of the system, i.e. to quantify the variation between the maximum and minimum readings acquired by the system for the same injected voltage value. Note that the results of this test are influenced by the Test Supply which was measured to have a worst case ripple of $\pm 1 \mathrm{mV}$.

The complete results of this test, comprising 100 readings for each acquisition cycle, can be found on the disc included as Appendix O. The spreadsheet entitled "Repeatability Test As Recorded" is an unedited spreadsheet that depicts the manner in which readings are recorded by the system. The spreadsheet entitled "Repeatability Test with Highlights" has been edited by the author to present the recorded data to the reader in a manner that is easier to analyse. With reference to Column CX the maximum average acquired was 0.187902 V and the minimum average acquired was 0.187048 V producing a variance range of 0.000854 V .

The second test in this phase was aimed at quantifying the variances of the acquired values from the true, injected values, determining the output linearity of the system and ascertaining the relationship between the input injected values and the system output recorded values. The complete results of this test, comprising 100 readings for each acquisition cycle, can be found on the disc included as Appendix O.

The Spreadsheet entitled "System Evaluation" shows the data that was acquired and recorded during this test. Columns A to CX are the original data columns and depict the data that was recorded during each reading cycle. Column CY represents the voltage that was injected into the system in order to produce the respective system reading and recording. Column CZ shows the absolute value of the difference between the injected and recorded values, i.e. the system error, and Column DA represents the reading number. It should be noted here again that the results of this test depends on the ripple of the Test Supply.

The author noted that the system's acquired values vary more from the true injected values for the lower range of injected values, i.e. for injected values less than 0.08 V . As the input voltage (injected voltage) increases the variation from the true value reduces. Recalling that the expected input range for any test that is to be carried out by this system is within the range of 100 mV to 350 mV , these variances for the lower input values are tolerable, as it will have little bearing on actual test results due to the decreasing error as the input voltage increases to within the typical 100 mV to 350 mV input range. If need be, more time and resources can be spent on reducing this variation when the system is installed. For the expected input range of 100 mV to 350 mV , the maximum error that was measured during this test was 0.00112 V which when calculated as a percentage of the injected voltage (i.e. 0.15 V ) for that measurement is:

$$
\begin{aligned}
\text { Maximum Percentage Error }= & \frac{0.00112 \mathrm{~V}}{0.15 \mathrm{~V}} \times 100 \\
& =0.75 \%
\end{aligned}
$$

The graphs shown in Figures 7-1 to 7-6 summarises the results of this test. The input (injected value) curves and best-fit input linear curves are plotted and compared with
the output (acquired values) curves and best-fit output linear curves. This is done in order to compare the variation of the output from the input injection values throughout the range of the Data Aquisation System. As can be seen from these graphs and the best fit linear graph equations, the variation between the injected values and the system acquired values is minimal therefore implying an almost straight line, $y=x$ relationship between the system input and recorded output values, as depicted in Figure 7-6.

When plotting the Output Vs Input curve and deriving the associated straight-line equation, i.e. $y=1.004 x-0.0012$, it is clear the deviation from the ideal, $y=x$, curve is minimal. In simple terms this means that whatever potential is present at the system input is acquired and recorded by the system with very little deviation from the original input value.


FIGURE 7-1: INPUT LINEARITY CURVE


FIGURE 7-2: LINEAR BEST-FIT INPUT LINEARITY CURVE


FIGURE 7-3: OUTPUT LINEARITY CURVE


FIGURE 7-4: LINEAR BEST-FIT OUTPUT LINEARITY CURVE


FIGURE 7-5: PLOT OF OUTPUT (ACQUIRED) READINGS VS INPUT (INJECTED) VALUES


## FIGURE 7-6: LINEAR BEST-FIT PLOT OF OUTPUT (ACQUIRED) READINGS VS INPUT (INJECTED) VALUES

Test three in this phase concentrated on the analysis of the data. As mentioned previously, if the potential difference across a pair of bars varies from the reference reading by a percentage that is larger than the percentage variance selected by the technician at the beginning of the test, a fault containing all the necessary details must be logged. At the end of the test, a test report containing all the faults as well as the test details and selected parameters must be printed. This information is also saved as a soft copy, as an update to the file that is associated with the armature under test by the component's serial number.

For this test, a simple series resistor and potentiometer network was set up on a test bench. All the resistor values were identical, $10 \mathrm{k} \Omega$, and were to represent/simulate bars that were healthy, i.e. bearing no faults. The resistor represented/simulated bars 1,2, 4 and 6 . Bars 3, 5 and 7 were represented/simulated by potentiometers that were set such that the potential difference across them varied from the reference value $(0.13594 \mathrm{~V})$ by a percentage that was greater the pre-selected $5 \%$ variance. The test report for this test can be found in Appendix E and the data recorded during this test
can found on the disc provided as Appendix O under the file named "001 Test Results 2006-4-12 14H16M31". Note that the name of the file represents the serial number that was entered, i.e. 001 Test Results, and the date and time of the test.

With reference to Appendix E and O the reader will note all the recorded faults. The simulated short circuit fault that was logged on Bar 8 was created by simply shorting the system's input probes. As discussed in the previous chapter and with reference to Appendix O, each cell in this row holds "Adjusted" except for column 102 of this row which holds 0 . In the case of an Open Circuit, the binary word (1111 11111111 1110) that was transmitted by the Communication Microcontroller upon encountering this condition alerts the Calculation Subprogram that an Open Circuit has been detected. The value here is not important, all that matters is that a fault was logged on this bar indicating an Open Circuit. However, for completeness the value of 0.411646 is calculated using an algorithm in the Calculation subroutine in the GUI. Note that this algorithm contains the variable "Gain" which the reader will recall was set to 9.95 , the outcome when 1111111111111110 is received by the GUI is:

Let ActVolReadRes $=(4.096 / 65536)$
Let ActVolRead = (StnBit_WD *ActVolReadRes)
Let mVActVolRead = ActVolRead / Gain
i.e.

Let ActVolReadRes $=4.096 / 65536=0.0000625$
Let ActVoIRead $=65534 \times 0.0000625=4.095875$
Let mVActVolRead $=4.095875 / 9.95=0.411646$
And finally, on the tenth pair of bars, an Emergency Stop was initiated.

The second phase of tests involved the testing of the automation processes. For these tests a digital oscilloscope that is capable of handling sixteen digital inputs was used to record the sequence of events as a test was carried out. The first test that was carried out was aimed at confirming the timing and the process flow of the system. See Figure 7-7 for the results from this test.


FIGURE 7-7: SYSTEM TIMING DIAGRAM

Where,

| Signal 0 | Represents the output of the first optical sensor |
| :---: | :--- |
| Signal 1 | Represents the output of the second optical sensor |
| Signal 2 | Represents the output of the D flip-flop to which the first optical <br> sensor is connected |
| Signal 3 | Represents the output of the D flip-flop to which the Second optical <br> sensor is connected |
| Signal 4 | Represents the input to the External Interrupt 1 pin of the <br> Automation Microcontroller |
| Signal 5 | Represents the output signal that controls the Armature Drive Motor |
| Signal 6 | Represents input to the External Interrupt 0 pin of the Automation <br> Microcontroller |
| Signal 7 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the lowering motion |
| Signal 8 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the raising motion |
| Signal 9 | Represents the output signal that controls the Test Supply Current |

Every test cycle begins by pulsing the Armature Drive Motor to begin rotating the armature under test, as signal 5 depicts. While rotating the armature optical sensors 1 and 2 detect the copper bars on the commutator. Upon detecting a bar, the respective
optical sensor output goes high, clocking the gate of the D flip-flop that it is connected to causing its output to also go high. This is depicted by signals 0 and 2, and signals 1 and 3. As soon as both D flip-flop outputs are high, External Interrupt 1 is triggered via a NAND Gate as depicted by signal 4. The External Interrupt 1 ISR is then initiated. The Armature Drive Motor is stopped immediately, (Signal 5). Following this, the D flip-flops are "Cleared" (output $=0$ ). This is evident when one looks at the point when External Interrupt 1 is triggered. After a few microseconds, the Armature Drive Motor signal goes Low followed by the outputs of the D flip-flops (Signals 1 and 3) both going low.

Note that for this test the optical sensors were manually triggered, hence the output returns low after the triggering source is removed. Ordinarily, the outputs of the optical sensors will only return low when the gap between the bars have been detected. Signals 0 and 1 going High indicates that a copper bar has been detected, and returning to Low indicated that the gap between the bars have been detected. This is shown in the figure below.


FIGURE 7-8: TIMING DIAGRAM FOR A TYPICAL BAR DETECTION CYCLE
Where,

| Signal 0 | Represents the output of the first optical sensor |
| :---: | :--- |
| Signal 1 | Represents the output of the second optical sensor |
| Signal 2 | Represents the output of the D flip-flop to which the First optical <br> sensor is connected |
| Signal 3 | Represents the output of the D flip-flop to which the Second optical <br> sensor is connected |
| Signal 4 | Represents the input to the External Interrupt 1 pin of the <br> Automation Microcontroller |
| Signal 5 | Represents the P0.5 on the Automation Microcontroller which <br> provided the input signal to a Nand gate in order to clear the D flip- <br> flops |
| Signal 6 | Represents the output of the above-mentioned Nand Gate, which <br> triggers External Interrupt 1. |

Continuing with reference to Figure 7-7, shortly after the Armature Drive Motor has been stopped and the flip-flops cleared, the Detection Unit is lowered by pulsing the Detection Unit Drive Motor (Signal 7). At this point the Test Current is also switched on (Signal 9) for the reasons discussed in Chapter 4. When the test probes have reached the surface of the commutator as signaled by the inductive proximity switch on the Detection Unit, External Interrupt 0 is triggered as depicted by Signal 6. The External Interrupt 0 ISR immediately stops the lowering process.

The 100 cycle successive reading process then begins. Once this process is completed the Detection Unit is raised by pulsing the Detection Unit Drive Motor (Signal 8). Once raised to its initial position, as signaled by the inductive proximity switch on the physical test unit frame, External Interrupt 0 is again triggered. This time the ISR ends the raising process. The Test Supply Current is also switched off at this point. This is one complete automation cycle. The very same process is carried out for the next pair of bars. The control of the system's main components such as the Armature Drive Motor, Detection Unit Drive Motor and the IGBT, via their respective electronic drives and drivers is depicted in Figure 7-9.


FIGURE 7-9: TIMING DIAGRAM FOR MAIN COMPONENT SWITCHING

Where,

| Signal 0 | Represents the output signal that controls the Armature Drive Motor |
| :---: | :--- |
| Signal 1 | Represents the input to the External Interrupt 1 pin of the <br> Automation Microcontroller |
| Signal 2 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the lowering motion |
| Signal 3 | Represents input to the External Interrupt 0 pin of the Automation <br> Microcontroller |
| Signal 4 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the raising motion |
| Signal 5 | Represents the output signal that controls the Test Supply Current |

The next two tests were concerned with the verification of the accuracy of the maximum allowable time that is reloaded into the timer registers for the detection process i.e. Detection Reference Time and for the raising of the detection unit, i.e.
Unit Raising Reference Time. As discussed in Chapter 4 under the heading Automation Microcontroller, the same subroutine is used by both procedures therefore, if the calculation and reloading algorithm is correct for one, it will also hold true for the other.

With this in mind, the author chose to verify the Detection Reference Time. Note that unlike the Unit Raising Reference Time, the Detection Reference Time for the first three bars is a preset 10s. This is because the recorded time from which the Detection Reference Time is calculated is only taken on the third pair of bars for the reason discussed in Chapter 4. Recall from Chapter 4, "The reason that the Detection Reference Time is calculated based on the time recorded for the third pair of bars is simply because the system is given time to settle during the first and second cycles." This means that Error 1 should occur if a pair of bars is not detected within 10s of the Armature Drive Motor being started, for the first three pairs of bars.


FIGURE 7-10: ERROR 1 INITIATION AFTER A 10S+1S, PREDEFINED, ALLOWABLE PERIOD HAS LAPSED

Where,

| Signal 0 | Represents the output signal that controls the Armature Drive Motor |
| :---: | :--- |
| Signal 1 | Represents the input to the External Interrupt 1 pin of the <br> Automation Microcontroller |
| Signal 2 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the lowering motion |


| Signal 3 | Represents input to the External Interrupt 0 pin of the Automation <br> Microcontroller |
| :---: | :--- |
| Signal 4 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the raising motion |
| Signal 5 | Represents the output signal that controls the Test Supply Current |

Figure 7-10 shows the first complete automation cycle for the first pair of bars but for the second automation cycle a pair of bars has not been detected, as shown by the External Interrupt 1 (Signal1) not being initiated, hence allowing the Armature Drive Motor to continue running until the 10 s preset time has elapsed. This initiates the Error1 subroutine. The reader will notice that the Armature Drive Motor, Signal 0, was left to run for 11s. This is because of the 1s delay loop that was called immediately after initiating the Armature Drive Motor P0.4 to cater for real time switching delays.

```
SETB PO.4
CALL DELAYLOOP
```

The effect of this is that 11 s will elapse due to the 10 s predetermined allowable time only being counted after the 1 s delay loop.

As shown in the next test's results, see Figure 7-11, the 1s delay loop has no effect on the calculated Detection Reference Time. This reference time is equal to the time recorded for the detection process on the third pair of bars plus an additional $20 \%$ of this recorded time.

## Detection Reference Time $=$ Third Pair Time Recording x 1.2

The reason that the 1s delay loop does not have any effect on this calculation is because the recording of this time was stopped after a 1s delay loop which was called immediately after the Armature Drive Motor was stopped. In other words, the time recording process was started 1s after the Armature Drive Motor was started and stopped 1s after the Armature Drive Motor was stopped, the net result being that the precise duration for which the Armature Drive Motor ran, was recorded. The exact same procedure was followed in recording the Test Probe Lowering Time which is used to calculate the Unit Raising Reference Time.

Unit Raising Reference Time $=$ Recorded Test Probe Lowering Time x 1.2

The reference time recorded on the third pair of bars was 6 seconds and as can be seen in the figure below the maximum allowable time for a pair of bars to be detected, i.e. Detection Reference Time, is 7.2 seconds.


FIGURE 7-11: ERROR 1 INITIATED AFTER THE PRE-CALCULATED TIME OF 6S X 1.2 = 7.2S HAS LAPSED
Where,

| Signal 0 | Represents the output signal that controls the Armature Drive Motor |
| :---: | :--- |
| Signal 1 | Represents the input to the External Interrupt 1 pin of the <br> Automation Microcontroller |
| Signal 2 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the lowering motion |
| Signal 3 | Represents input to the External Interrupt 0 pin of the Automation <br> Microcontroller |
| Signal 4 | Represents the output signal that controls the Detection Unit Drive <br> Motor for the raising motion |
| Signal 5 | Represents the output signal that controls the Test Supply Current |

The last test in this phase focused on the ADC control inputs and outputs. Although the fact that 100 volt-drop readings are acquired for each reading cycle, see Appendix

O , is proof that the ADC is operating as it should, the author thought that the following results should be included for completeness.
Figure 7-12 and Figure 7-13 depict the transitions that each of the ADC control pins undergo for each of the 100 readings taken. The time scale on which these results were recorded was $50 \mu \mathrm{~s} /$ division.


FIGURE 7-12: TIMING DIAGRAM FOR THE ADC INPUT AND OUTPUT CONTROL PINS

Where,

| Signal 0 | Represents the ADC input pin, $R / \bar{C}$ |
| :--- | :--- |
| Signal 1 | Represents the ADC output pin, $\overline{E O C}$ |
| Signal 2 | Represents the ADC input pin, HBEN |
| Signal 3 | Represents the ADC input pin, $\overline{C S}$ |

FIGURE 7-13: ANNOTATED TIMING DIAGRAM FOR THE ADC INPUT AND OUTPUT CONTROL PINS

Where,

| Signal 0 | Represents the ADC input pin, $R / \bar{C}$ |
| :--- | :--- |
| Signal 1 | Represents the ADC output pin, $\overline{E O C}$ |
| Signal 2 | Represents the ADC input pin, HBEN |
| Signal 3 | Represents the ADC input pin, $\overline{C S}$ |

As presented in Chapter 4, the ADC control pins follow the same input and output sequence as specified in the datasheet. With reference to Figure 7-13, the reader will see that the first red marker, labelled 1 , denotes the first $\overline{C S}$ falling edge. Holding $R / \bar{C}$ low during this transition puts the ADC into acquisition mode. The second red marker denotes the second $\overline{C S}$ falling edge. This initiates the start of a conversion. Holding $R / \bar{C}$ low during this transition puts the ADC into Standby Mode, i.e. the reference and buffer remain powered up after a conversion. Shortly after the second $\overline{C S}$ falling edge, the $\overline{E O C}$ line goes low signalling the end of a conversion to the Communications Microcontroller. Upon receiving this signal the Communications

Microcontroller sets the HBEN pin Low, in order to ensure that the low-byte (i.e. the least significant data byte) of the converted ADC data is available on the output data bus on the $\overline{C S}$ third falling edge. The $\overline{C S}$ third falling edge is then initiated, as denoted by red marker labelled 3. This action loads the ADC data onto the eight-bit output bus. The HBEN pin is then toggled so that the high-byte (i.e. the most significant data byte) of the ADC conversion is available on the output data bus. Following this, the first $\overline{C S}$ raising edge after the third falling edge, as denoted by the pink marker labelled 4, puts the ADC output bus back into a high impedance state, as well as forcing the $\overline{E O C}$ line High. The next $\overline{C S}$ falling edge will begin the next conversion cycle.

## Conclusion

The research, design and development that was required for the controller used in the Automated Volt-Drop Test process was centred largely on the design of embedded systems for automation applications. Microcontroller based embedded systems offers the designer the flexibility to design any controller or system based on specific application requirements.

However with flexibility comes the requirement for a deeper level of design detail in which case the designer has to cater for every task, function and outcome using software, firmware and hardware. From the provision of responses to inputs from the external environment to achieving communication between the modules that make up the controller or system and the building of a product that can operate optimally in the environment that it is designed to, the designer has to conceptualise, design, build and test each module. The same applies to the development of a GUI. With design of a controller, one can tailor a GUI that suits the application using existing programming packages with very little cost. However this entails a deeper level of programming to achieve the required outcomes.

The designed controller, GUI and RGUI fulfil the requirements of the set-out objective, i.e. the design of an embedded controller and GUI for the automation of the armature Volt-Drop Test. This was confirmed by the automation phase test results and the data acquisition and computation test results which revealed a maximum percentage error of $0.75 \%$. When compared to the present test methods this controller and GUI will introduce a higher degree of accuracy in terms of the actual volt-drop readings and greater efficiency in terms of ensuring that every winding is tested and that skilled staff are not under utilised by performing these tests. Further, this new process ensures that test records are automatically saved on file to build a history of the armatures tested and to verify the competency of the test technician and armature repair staff.

Although embedded controller designs are recommended for specialised or smaller controllers, with regard to larger scale process automation, off the shelf controllers
and GUI packages are recommended. From the authors experience, embedded controllers prove to be more cost effective and robust in on-board locomotive applications especially when considering the older locomotives where relays, resistors and heavy current contacts switches are used instead of microprocessor control and power electronic components such as IGBTs. Custom designed embedded controllers are recommended as the controllers that are installed in these locomotives as part of modifications have to withstand the unusually high electrical noise, EMI, vibration, dust and temperature environment along with very irregular and electrically noisy power supplies. Off the shelf controllers often fail in this environment, hence controllers have to be designed and built to operate optimally in this environment. For common industrial environments, off the shelf controllers are sufficiently rugged to cope with the operating environment.

Off the shelf controllers, which include PLCs, may offer less flexibility and may require the purchase of a controller that incorporates features, functionality, input and output ports etc. that may be considered over-kill for smaller controller applications, however, they do offer built-in features, functionality and plug-and-play options for the interconnection of additional modules and GUI packages that will require minimal programming and hardware design. Built-in software functions and hardware operation have been tested in industry and have a proven record by the specific manufacturer.

An off the shelf GUI environment, SCADA for example, which will be used with PLCs offer a large array of functionalities that can easily be used with minimum programming required as compared to a tailored GUI but has the associated downside of the cost.

In summary, the design of an embedded controller, GUI and RGUI for the automation of the Volt-Drop Test was a task that involved detail design and testing along each phase of the project. For future automation projects in Spoornet workshops and test centres, it is recommended that the use of a off the shelf controller be investigated along with the design of embedded controllers.

The trade off that has to be considered in terms of embedded controller design is the flexibility to design a controller that is perfectly suited to the application and environment vs. the time and cost required for design and testing. The trade off to be considered in using off the shelf controllers is the ease of use and reduced time of implementation due to proven product history vs. the cost of purchasing these products and the possibility of unreliable performance in the operational environment.

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## Appendices

GUI Screen Captures :Appendix A<br>List of ASCII prompts :Appendix B GUI Source Code :Appendix C Printout From A Saved File :Appendix D<br>Test Report Printout :Appendix E<br>Remote GUI (RGUI) Screen Capture :Appendix F<br>Remote GUI (RGUI) Source Code :Appendix G<br>The AT89S51 Microcontroller Datasheet :Appendix H<br>Acebus Development Environment :Appendix I<br>For Microcontroller Embedded programming<br>Component Datasheets :Appendix J<br>Automation Microcontroller Port Utilisations :Appendix K<br>Communications Microcontroller Port Utilisations<br>Automation Microcontroller Register Utilisations<br>Communications Microcontroller Register Utilisations<br>Automation Microcontroller Bit Addressable Ram Used For Flags<br>Communications Microcontroller Bit Addressable Ram Used For Flags<br>Automation Microcontroller Source Code :Appendix L<br>Communications Microcontroller Source Code<br>Controller Circuit Schematic :Appendix M<br>Screen Capture For The Calibration Screen :Appendix $\mathbf{N}$<br>Disc Containing Recorded Test Results \& :Appendix O<br>A GUI PowerPoint Presentation<br>Detailed Discussion on Graphic User Interface (GUI) Development :Appendix P (Includes Flow Diagrams and Code Extracts)<br>Detailed Discussion on Microcontrollers and Embedded Programming :Appendix Q (Includes Flow Diagrams and Code Extracts)<br>Detailed Discussion on Hardware Design :Appendix R

# Appendix A <br> GUI Screen Captures 

## Appendix B

## List of ASCII prompts

## Appendix C GUI Source Code

# Appendix D 

Printout From A Saved File

# Appendix E 

Test Report Printout

## Appendix F <br> Remote GUI (RGUI) Screen Capture

# Appendix G 

Remote GUI (RGUI) Source Code

# Appendix H 

The AT89S51 Microcontroller Datasheet

## Appendix I

Acebus Development Environment For Microcontroller Embedded Programming

## Appendix J

Component Datasheets

# Appendix K 

Automation Microcontroller Port Utilisations Communications Microcontroller Port Utilisations
Automation Microcontroller Register Utilisations
Communications Microcontroller Register Utilisations
Automation Microcontroller Bit Addressable Ram Used For Flags Communications Microcontroller Bit Addressable Ram Used For Flags

# Appendix L 

Automation Microcontroller Source Code Communications Microcontroller Source Code

# Appendix L 

Communications Microcontroller Source Code

# Appendix L 

## Automation Microcontroller Source Code

# Appendix M 

Controller Circuit Schematic

# Appendix N 

Screen Capture For The Calibration Screen

# Appendix O 

Disc Containing Recorded Test Results \& A GUI PowerPoint Presentation

# Appendix P 

Detailed Discussion on Graphic User Interface (GUI) Development (Includes Flow Diagrams and Code Extracts)

# Appendix Q 

Detailed Discussion on Microcontrollers and Embedded Programming (Includes Flow Diagrams and Code Extracts)

## Appendix R

Detailed Discussion on Hardware Design


Test $\ln$ Progress Fields



Test $\ln$ Progress Fields



Test $\ln$ Progress Fields



Test $\ln$ Progress Fields


- View User Profile Setup

View User Profile


Test $\ln$ Progress Fields


| View/Change Directory Path Settings |
| :---: |
| View Settings |

- View User Profile Setup

View User Profile


Test $\ln$ Progress Fields


| View/Change Directory Path Seltings: |
| :---: |
| View Settings |

- View User Profile Setup

View User Profile



| View/Change Directory Path Settings |
| :---: |
| View Settings |

View User Profile Setup
View User Profile


Test $\ln$ Progress Fields


- View User Profile Setup

View User Profile


- Test In Progress Fields -


| View/Change Directory Path Settings |
| :---: |
| View Settings |

- View User Profile Setup

View User Profile


Test $\ln$ Progress Fields



Test In Progress Fields -

-Manual Reading Controls

-GUI Special Fuction Controls
View Controls

- Directory Path



Test $\ln$ Progress Fields

-GUI Special Fuction Controls View Controls

View/Change Directory Path Settings

-View User Profile Setup
View User Profile
$-\mid \underline{a} x$

LOCKED OUT


Test $\ln$ Progress Fields



## Test In Progress Fields

## Fault Log

Fault on Bar: 3, Percentage Variance $=19.28123$, Bar Reading: 0.1626973 V , Reference: 0.136398 V Fault on Bar: 5. Percentage Variance $=10.88503$, Bar Reading: 0.1215511 V. Reference: 0.136398 V Fault on Bar: 7. Percentage Variance $=10.3879$, Bar Reading: 0.1505669 V , Reference: 0.136398 V
Fault on Bar: 8, Volt-Drop Reading Is Zero ( $0 V$ ), Indicating A Possible Short Circuit
Fault on Bar: 9, Volt-Drop Reading Is Out Of Range, Indicating A Possible Open Circuit
Emergency Stop on Bar 10
Test Print Complete


| Armature Properties |
| :--- |
| Armature Name: b Number of Bars: 10  <br>  New Armature Name <br>  Add Nevs <br>   <br> Number Of Commutator Bars  <br> Circk To Fiemove Highlighted Amature  |

## Job Number

 001 Test Results
## Test $\ln$ Progress Fields

## -Fault Log

Fault on Bar: 3. Percentage Variance $=19.45295$, Bar Reading: 0.1623932 V . Reference: 0.1359474 V Fault on Bar: 5, Percentage Variance $=10.68346$, Bar Reading: 0.1214235 V , Reference: 0.1359474 V Fault on Bar: 7. Percentage Variance $=11.05382$, Bar Reading: 0.1509748 V , Reference: 0.1359474 V
Fault on Bar: 8, Volt-Drop Reading Is Zero ( 0 V ) Indicating A Possible Short Circuit
Fault on Bar: 9, Volt-Drop Reading Is Out Of Range, Indicating A Possible Open Circuit
Emergency Stop on Bar 10
Test Print Complete


## Communications Microcontroller $\Leftrightarrow$ Notebook Protocols Serial Communication

| Variable | $\mu_{1}$ (In) | $\mu_{1}$ (Out) | NB (In) | NB (Out) | Protocol |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Ask for Man/Auto |  | x | x |  | b |
| Volt Drop Reading |  | x | x |  | Data |
| Ready to begin test |  | x | x |  | d |
| Start (click) | x |  |  | X | A |
| End (click) | x |  |  | x | B |
| Continue After Error (click) | x |  |  | x | C |
| Take reading - Manual (signal) | x |  |  | x | D |
| Continue test (signal) | x |  |  | x | E |
| Emergency Stop (click) | x |  |  | x | F |
| Auto/Man Toggle (signal) Manual | X |  |  | x | G |
| Auto/Man Toggle (signal) Automatic | x |  |  | x | g |
| Manual Emergency Stop (Press -Switch on the frame) |  | $\mathbf{x}$ | $\mathbf{x}$ |  | 0 |
| Last Bar Reached (signal) | x |  |  | x | P |
| Last Bar Not Reached (signal) | x |  |  | x | p |
| Increment \# of bars (signal) |  | x | x |  | I |
| Error 1 - Bars Not Detected (signal) |  | x | x |  | J |
| Error 2 - Probes not lowered (signal) |  | x | x |  | m |
| Error 3 - Current Time Exceeded (signal) |  | x | x |  | L |
| Error 4 - Probed not Raised (signal) |  | x | x |  | Q |
| Alert NB of incoming Test reading data (High Byte) |  | $x$ | $x$ |  | z |
| Alert NB of incoming Test Reading data (Low Byte) |  | $x$ | $x$ |  | y |

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| End of 100 count reading <br> continue signal | $x$ |  |  | $x$ | S |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Perform Calibration <br> Procedure | $x$ |  |  | $x$ | H |

    '******For arm sel Eile \(* * * * * * *\)
    'num -> no. of bars
    'nam -> name of arm
    'ont -> record number
    '****End For arm sel File *****
    ************** save Directory path **************
    Dim DefaultPath As String
    '************* save Directory path ***************
    "*******Printing*****************
    Dim Print flag As Boolean ' for deleting file while print
    '*******End Printing*************
    '*******Open \& Del Eiles*********
    'aa is the Job No field
    'bb is the Operators Name field
    'cc is the Armature Selection field
    'dd is the Percentange Variance field
    'ee is the Date field
    'ff is the Recorded Faults field
    Dim Save Test As String ' file name of amature with specific job no
    Dim Deletex As String
    Dim Test Date As String ' date of test for specific armature
    '*****En \(\bar{d}\) Open \& Del Files*******
    '*********Calculation***********
    Dim ActVolReadRes As Single ' holds resolution ie, ref voltage devided by 16 bit levels (4.096/
    65535)
    Dim ActVolRead As Single ' holds actual voltage level of the current reading
    Dim mVActVolRead As Single 'holds actual voltage level of the current reading in millivolts
    Dim ActReference As Single 'holds actual reference level
    Dim mVActReference As Single 'holds actual reference level in millivolts
    Dim StnBit WD As Long ' holds the 16 bit word
    Dim StnBit_WDflg As Boolean
    Dim Current_Variance As Single ' holds the variance of current reading fron ref
    Dim Initial_Count As Integer ' counts the first 5 readings
    Dim Initial_Error As Boolean ' flag to signal that the first (ref reading) was on an fault bar
    Dim Reference As Long
    Dim Bin2Dec As String
    Dim AvgRefReading As Single ' average reference reading calculated after 100 cycles
    '*********End Calculation********
    '********Serial In*************
    Dim SerIn As String
    Dim High Byte As String * 8
    Dim Low Byte As String * 8
    Dim Incomming HighB Flag As Boolean
    Dim Incomming LowB \(\bar{F} l a g\) As Boolean
    1********End Serial In \(* * * * * * * * * * * *\)
    '*******Time calc*********
    Dim timef As Integer
Dim timed As Integer
Dim timee As Integer
Dim timea As Integer
Dim timeb As Integer
Dim timec As Integer
1*******End Time Calc*********
-*******100 READING COUNT***********************
Dim MultiReading As Integer
Dim RowCount As Integer
Dim ExcelSheet As Object
Dim Savetime As String
Dim SaveDate As String
'*******END 100 READING COUNT*******************

Dim TimerFlag As Boolean


Jim Gain As Single
'***************End specify hardware gain****************

Dim CalibElag As Boolean
Dim ReadingBoxIndex As Integer
Dim CalibRefIn As Single
Dim gradient As Single
Dim intercept As Single


Public AddNewArm As Boolean
Public RemoveArm As Boolean
Fublic AddNewVal As Boolean
Public RemoveVal As Boolean
Public Calpassw As Boolean
Public PathPassW As Boolean
Public Delfile As Boolean
Public UsrProf As Boolean


Dim ZeroIn As Integer
Dim HighBCount As Integer
Dim HighBCountl As Integer
Dim HighBCount2 As Integer
Dim HighBCount3 As Integer
Dim HighBCount 4 As Integer
Dim HighBCount5 As Integer
Dim SndEntry As Integer
Lower range value adjust*********************
Dim Auto Man As String ' automatic / manual select
Dim No_of_Bars As Long ' global variable for num of bars
Dim Percentage As Single ' global variable for \& variance
Dim Pswd As String ' 3 password tries
Dim PasswdFlag As Boolean ' flag to signal correct password
Dim Emergency As Boolean
Dim pa As Integer
Dim a As Integer
Private Sub Combol_Click()
Dim dp As Integer
Let $d p=$ Combo1. ListIndex
Let $d p=d p+1$
Open DefaultPath \& "Per.TX'T" For Input As \#3
Do While Not EOF (3)
Input \#3, per, vlu If $v l u=d p$ Then Let Percentage $=$ Val $($ per $)$ End If
Loop
Close \#3
End Sub
Private Sub Combo2 Click()
Dim d As Integer
Let $d=$ Combo2.ListIndex
Let $d=d+1$
Open DefaultPath \& "Arm.TXT" For Input As \#1
Do While Not EOF(1)
Input \#1, nam, num, cnt If cnt $=d$ Then
Let Text 7. Text $=$ num
Let Text6.Text $=0$
Let Text 8. Text $=0$
Let No_of Bars = Val(num)
End If
Loop
Close \#1
End Sub
Private Sub Commandl Click()
-et AddNewArm = True
Form3.Visible $=$ True
'Eorm3. Show 1
Form3.Text1.Text = ""
?orm3.TextI.SetEocus

End Sub
Private Sub Commandi GotFocus()
If Form3.AdminPasswordelag = True Then
Let Eorm3.AdminPasswordFlag = False If (Text3.Text <> "") Then Combo1.AddItem "Percentage Variance: " \& Text3.Text \& "\%" Let $\mathrm{pa}=$ Combol. Listcount , used as a record number, lst item starts at 1 Open DefaultPath \& "Per.TXT" For Append As \#3
Write \#3, Text3.Text, pa Let Text 3. Text $=$ "" Close \#3
Else
MsgBox "Enter new Percentage Variance", vbokonly, "Enter Percentage Variance" End If
'Else
'MsgBox " You are Not Authorised to use this fuctionality"
End If
End Sub
Private Sub Commandio Click()
MsgBox " The next pair of bars has not been detected within the allowable period. A Manual Read ing must now be taken", vbokonly, "Detection Error"
End Sub
Private Sub Commandll Click()
MsgBox " The Test Probes have not been lowered within the allowable period. A Manual Reading mu st now be taken", vbOKOnly, "Detection Unit Lowering Error"
End Sub
Private Sub Commandi2_Click()
MsgBox " The Test Current has been Switched on for too long, and as a safety measure an Emergen cy Stop has been invoked. Please Click End, check the device and Restart the Test", vbokonly, " Test Current On-Time Exceeded"
End Sub
Private Sub Command13_Click()
MsgBox " The Test Probes have not been raised within the allowable time. Check the device and $c$ lick Continue After Error Pause OR Click Emerengcy Stop!", vbokonly, "Detection Unit Raising Er ror"
End Sub
Private Sub Command14_Click()
Command15.Enabled $=$ Fālse
Command14.Enabled = Ealse
If Listl.List (0) <> "" Then
If Left(List1.List (0), 11) = "Job Number:" Then
Let Deletex = Eopen
Printer. NewPage
Let Print Save_i=0
Do While Print_Save i $<=$ (Listl.ListCount - I)
Printer. Print Listl.List(Print Save_i)
Print_Save_i = Print_Save_i + $\overline{1}$
Loop
Listl.AddItem "Test Print Complete"
Printer.EndDoc

```
    ***Print in Pic Box for Simulation
    TTmerl.Enabled = True
    '*****************End Print in Pic Box for Simulation ***************************
    Else
    '*****************Print in Pic Box for Simulation ******************************
    Timerl.Enabled = True
    *****************End Print in Pic Box for Simulation **************************
    Let Save Test = Text9.Text
    Call FsaveSub
    Printer.NewPage
    Printer.FontBold = True
    Printer.FontSize = 9
    Printer.Print "
```

Printer. FontBold $=$ False
Printer.FontSize $=8$
Printer. Print ""
Printer. Print Spc(49); "Automated Volt-Drop Test Report"
Printer. EontBold $=$ True
Printer.Eontsize $=9$
Printer.Print "
Printer. Print ""
Printer. Print Spc(5); "Job/Serial Number: " \& Text9.Text
Printer. Print Spc(5); "Operator's Name: " \& Text2. Text
Printer. Print Spc(5); Combo2. List (Combo2. ListIndex)
Printer. Print Spc (5); Combol.List (Combol. ListIndex)
Printer. Print Spc(5); "Date: " \& LTrim(Textll.Text)
Printer.Print " $"$ L Limimextil.

Printer.Print ""
Printer. Fontsize $=12$
Printer. Print Spc(4); "Recorded Faults "
Printer. FontBold $=$ False
Printer. Fontsize $=8$
Printer.Print ""

Let Print current $i=0$
Do While Print_current_i $<=$ (Listl.ListCount - 1)
Printer. Print $\overline{S p c}(5)$; Listl. List(Print current i)
Print current_i $=$ Print_current_i +1
Loop
Printer. FontBold $=$ False
Printer.Print ""
Printer. FontSize $=9$
Printer. Print Spc (5); "I, " \& Text2.Text \& " acknowledge the above results and pledge to in vestigate and/or remedy the"

Printer.Print $\operatorname{Spc}(5)$; "above recorded faults (if any)."
Printer.Print ""
Printer. Print Spe(5); "Signature, " \& Text2.Text \& "
Printer. Print ""
Printer. Print ""
Listl.AddItem "Test Print Complete"
Printer. EontBold $=$ True
Printer.Print "

Printer. EndDoc
End If
Else
MsgBox "No Data Available To Print", vbokOnly, "Print Error"
Command14. Enabled = True
End If

End Sub

Private Sub Commandl5_Click()
Dim Add Elag As Booleān
Command14.Enabled $=$ False
Command15. Enabled $=$ False
Let Add_Elag = Ealse
Let Save Test $=$ Text 9. Text
$1 * * * * * * * * * * * * * * * * * * * * * *$ Save Excel Data $* * * * * * * * * * * * * * * * * * * * * * * * *$
'objExcel. Application. Save "Sun"
'objExcel.Application.Quit
ExcelSheet.SaveAs DefaultPath \& Text9. Text \& Space(2) \& SaveDate \& Space(2) \& Savetime ExcelSheet. Application. Quit
Set ExcelSheet $=$ Nothing
$1 * * * * * * * * * * * * * * * * * * * *$ End Save Excel Data $* * * * * * * * * * * * * * * * * * * * * * * * *$
If Dir(DefaultPath \& "Saved List.TXT") <> "" Then
Open DefaultPath \& "Saved_List.TXT" Eor Input As \#7 'file for the list of all jobs saved
Do While Not EOE(7)

```
        Input #7, Add_list
            If Add list = Save Test Then
                        Let Add_Flag = True
            End If
        Loop
    Close #7
        If Add Flag = False Then
            Let Add Flag = Ealse ' redundant
            Open DefaultPath & "Saved List.TXT" For Append As #7
            Write #7, Save Test
            Close #7
                End If
```

Else
Open Defaultpath \& "Saved_List.TXT" Eor Append As \#7
Write \#7, Save Test
Close \#7
End If
Open DefaultPath \& Save_Test For Append As \#5
Let $\mathrm{i}=0$
Do While $i<=$ (Listl.ListCount - 1)
Write \#5, Text9.Text, Text2.Text, Combo2.List(Combo2.ListIndex), Combol.List(Combol.Lis
tIndex), LTrim(TextI1.Text), Listl.List(i)
Let $i=i+1$
Loop
Write \#5, "End", "xxx", "xxx", "xxx", LTrim(Text11.Text), "End Of Recorded Results"
Close \#5

End Sub
Private Sub Commandl6 Click()
End
End Sub
Private Sub Command17 Click()
Frame37.Visible $=$ True
Command46.Visible $=$ True
Text20.Text $=$ ""
Text21.Text = ""
Text22.Text = ""
Pswd = Pswd - 1
If Textl.Text <> "" Then
If Dir("C:\Program Files\Calibration\" \& "B_2 B_Pwd") <> "" Then
Open "C:\Program Files \Calibration\" \& "B_2_B-Pwd" For Input As \#1 Do While Not EOE (1)
Input \#1, UserName, UserPassword If UserPassword $=$ Textl.Text Then
'If Text1.Text = "AutoSun6" Then
Let PasswdFlag = True
Let Text2.Text = UserName

## End If

Loop
Close \#1

If PasswdFlag = True Then
Text1.Text $="$ "
Textl.Locked $=$ True
Let Emergency = False
Let Text2.Text $=$ UserName
Let Text2.Locked $=$ True
Let Text9.Locked $=$ False
Let Text2.Text $=$ ""
Let Text 9. Text $="$ "

Combo2.Text = "Armature Select"
Combol.Text = "Percentage Variance"
Optionl = False
Option2 = False
Let Command5. Caption $=$ "Load"
Let Command14.Enabled = Ealse ' print
Let Command15. Enabled = False ' save
Let Command36.Enabled $=$ True ' change default path

```
Let Text3.Locked = False
Let Text4.Locked = Ealse
Let Text5.Locked = False
Let Text9.Locked = Ealse
Let Command30.Enabled = True 'For delete and open
Let Command32.Enabled = True
'Let Erame30.Enabled = True '
'Let Frame31.Enabled = True '
Command14.Enabled = True ' print
    Let Text3.Text = ""
    Let Text4.Text = ""
    Let Text5.Text = ""
    Let Command6.Enabled = False
    Let Command6. BackColor = & 48000000F
    Let Commandl.Enabled = True
    Let Command2. Enabled = True
    Let Command3.Enabled = True
    Let Command4.Enabled = True
    Let Command5.Enabled = True ' enabled for LOAD, then disabled and then enabled
    for START after mscomm says micro is ready
            Let Command9.Enabled = True
    Let Combol.Enabled = True
    Let Combo2.Enabled = True
    Let Option1.Enabled = True
    Let Option2.Enabled = True
    Let Command17.Enabled = False
    Let Commandl8.Enabled = False ' Lock out password
    Let Textl0.Locked = True ' Lock out password
    'clearing flags and resetting variabled for calculation
    Let StnBit WD = 0
    Let Current Variance = 0
    Let Initial Count =0
    Let Initial_Error = False
    Let Reference = 0
    '**************************************************************
```

                '*******Initilize Serial Comm port \(1 * * * * * * *\)
                ' new code \(20 / 11\) to re-initilze the sp and Clear the Out(transmit) buffer
                'Rec data
                MSComm1. PortOpen = False
            MSComml.RThreshold \(=1\)
            MSComm1. InputLen \(=1\)
            MSComm1.DTREnable = False
                MSComm1.Settings \(=\) "2400, N, 8,1"
                MSComm1. CommPort \(=1\)
                MSComm1. PortOpen \(=\) True
                'Trans data
                MSComm1.OutBufferCount \(=0\)
            '**** End Initilize Serial Comm port 1***** \(^{*}\)
        Else
            If Pswd > 0 Then
                            MsgBox "Incorrect Password, Tries left: " \& Pswd \& "", vbokOnly, "Incorrect Pa
            Let Text1.Text \(=\) " \("\)
            Text1.SetFocus
            Else
            MsgBox " You DO NOT have the authority to use this equipment. You have been LoC
    KED OUT", vbokOnly, "Lock Out"
Let Textl.Text $=" "$
Erame27.Visible $=$ True
Text 10. Visible $=$ True
Command18.Visible $=$ True
End If
End If

Else
MsgBox "A User Profile List Has Not Been Created", vbokonly, "User Profile Error" Texti.Text $=$ "" End If
Else
MsgBox "Please Enter A Password In the Space Provided", vbokonly, "Enter Password" Text1.SetFocus
End If
End Sub

Private Sub Command18_Click()
If Textl0.Text = "AdminAutoSun6" Then
Frame27.Visible = False
Text10.Text $=$ "
Let Commandi8.Visible = False
Let Textlo.Visible = False
Let Pswd = 3
End If
Textlo. Text $=$ "
End Sub
Private Sub Command19 Click()
Command5. BackColor $=\& H 8000000 \mathrm{~F}$ 'simulator
Let Command5.Caption $=$ "Start"
Command5.Enabled $=$ True
Let Command8. Enabled $=$ True
Screen. MousePointer $=$ vbArrow
End Sub
Private Sub Command2 Click()
Let AddNewArm = True
Form3.Visible $=$ True
'Form3.Show 1
Form3.Textl.Text = ""
Form3.Text1.SetFocus

End Sub

Private Sub Command2_GotFocus()
If Eorm3.AdminPassworaFlag = True Then
Let Form3.AdminPasswordFlag = False
If MsgBox("Are You Sure That You Want to Delete The Selected Item?", vbYesNo, "Confirm Dele te") = vbYes Then

Dim pc As Integer
Let $\mathrm{pb}=$ Combol. ListIndex ' note: first item in box is at 0 therefore 1 must be added $t$ listcount valne the record is saved under






t 1
 Combol.AddItem "Percentage Variance: " \& per \& " " Let $p c=$ Combol.Listcount Write \#4, per, pc End If

## Loop

Close \#3
Close \#4
Kill DefaultPath \& "Per.TXT"
Name "Del2" As DefaultPath \& "Per.TXT"
Else: MsgBox "No Percentage Variance Values Found", vbokonly, "Percentage Variance Erro
End If
End If
'Else
'MsgBox " You are Not Authorised to use this fuctionality"
End If

Forml - 8
End Sub
Private Sub Command20 Click()
Command47.Visible = True
Text23.Visible $=$ True
Text24.Visible $=$ True
Command49.Visible $=$ True
Label14.Visible $=$ True
Label18.Visible $=$ True
End Sub
Private Sub Command2l Click(
Text15.Text $=$ Auto Man
End Sub
Private Sub Command22_Click()
Call Bar count
End Sub
Private Sub Command23 Click()
Let Commandio. Enabled $=$ True , errorl
Commandlo.BackColor $=$ QBColor(12)
Framel4.Forecolor $=$ QBColor(12)
Frame14.FontSize $=10$
Frame14.FontBold $=$ True
Command9. Enabled $=$ True
Frame20. ForeColor $=$ QBColor (10) ' enables man reading but and dsply
Picture5. BackColor $=$ QBColor (10) '
Frame21.ForeColor = QBColor(10) '
Command9.BackColor $=$ QBColor (9)
End Sub
Private Sub Command24_Click()
Let Command11.Enabled $=$ 'True ' error2
Commandll. BackColor $=$ QBColor(12)
Frame16.ForeColor = QBColor(12)
Framel6.FontSize $=10$
Eramel6.FontBold $=$ True
Frame20. ForeColor = QBColor(10) ' enables man reading but and dsply
Picture5.BackColor = QBColor(10)
Frame21. ForeColor $=$ QBColor (10) '
Command9. BackColor $=$ QBColor (9)
End Sub
Private Sub Command25 Click()
Let Command12. Enabled $=$ True 'error3 is enabled and is disabled when Cont after pause or emgncy stop is clicked

Command12. BackColor $=$ QBColor (12)
Frame17.ForeColor $=$ QBColor(12)
Framel7.FontSize $=10$
Frame17. FontBold $=$ True
Command7.Enabled = True
Command7. BackColor $=$ \&HFF8080
Command8. BackColor $=\$ H E F 8080$
Command8.Enabled $=$ True
End Sub
Private Sub Command26 Click()
Let Commandl3.Enabled = True 'error4 is enabled and is disabled when Cont after pause or emgncy stop is clicked

Commandi3.BackColor $=\mathrm{QBColor}(12)$
Frame15.ForeColor $=$ QBColor(12)
Erame15. FontSize $=10$
Frame15. FontBold = True
Command7.Enabled $=$ True
Command7. BackColor $=$ \&HFF8080
Command8. BackColor $=\&$ HFF8080
Command8.Enabled $=$ True
End Sub
Private Sub Command27 Click()
figh_Byte = SerIn
ind $\bar{S} u b$

If Incomming LowB Flag = True Then Low Byte = SerIn Picturel. Print Low Byte Let Incomming LowB Flag = False Let Incomming High $\bar{B}$ Elag $=$ False ' redundant Call Calculation ElseIf Incomming HighB Elag = True Then High_Byte $=$ SerIn Picturel. Print High Byte Let Incomming_HighB Flag = False Else Select Case SerIn
Case "a"
Call Trans_Arm_Type
Case "b"
Text15.Text $=$ Auto_Man
Case "d"
Command5. BackColor $=\& H 8000000 \mathrm{~F}$
Let Command5.Caption = "Start"
Command5.Enabled $=$ True
Let Command8. Enabled $=$ True
Screen. MousePointer $=$ vbArrow
Case "O" 'Emergency Stop prompt when the Emergenct stop switch on the test station is press

```
Command8.BackColor = QBColor(12)
```

Command7. BackColor $=\propto \mathrm{H} 8000000 \mathrm{~F}$
Let Command6.Enabled = True
Let Command6. BackColor $=\&$ HFF8080
Let Picture6.BackColor $=\& H 8000000 \mathrm{~F}$
Call TestEnd_States
Let Emergency $=$ True
Command8.Enabled $=$ Ealse
Listl. FontBold $=$ True
List1.AddItem "Emergency Stop on Bar " \& Text6. Text
List1.FontBold $=$ Ealse
Case "I"
Call Bar count

Case "J"
Let Commandio.Enabled $=$ True ' error 1
Commandlo. BackColor $=$ QBColor(12)
Frame14.ForeColor $=$ QBColor(12)
Frame14.FontSize $=10$
Framel4. FontBold = True
Command9.Enabled $=$ True
Erame20. ForeColor = QBColor(10) ' enables man reading but and dsply
Picture5.BackColor $=$ QBColor(10) '
Erame21. ForeColor $=$ QBColor(10) '
Command9.BackColor $=\& \mathrm{HEF} 8080$
Case "m"
Let Command11.Enabled $=$ True ' error2
Commandil. BackColor $=$ QBColor (12)
Framel6.EoreColor $=$ QBColor(12)
Frame16.FontSize $=10$
Eramel6.FontBold = True
Frame20. ForeColor $=$ QBColor (10) ' enables man reading but and dsply
Picture5.BackColor $=$ QBColor(10)
Erame2I.ForeColor = QBColor(10) '
Conmand9. BackColor $=$ \&HFF8080
Case "L"
Frame17. ForeColor $=$ QBColor(12)
Eramel7. Fontsize $=10$
Erame17. FontBold = True
Command8. Enabled $=$ True Command7.Enabled $=$ True Command7. BackColor $=\&$ HFF8080
Command8. BackColor $=\&$ HFF8080

```
            ' Emergnct stop is automatically entered into hence the code below is a copy of the "Em
rgency Stop" button
            Command8.BackColor = QBColor(12)
            Command7.BackColor = &H8000000F
            Let Command6.Enabled = True
            Let Command6. BackColor = &HFF8080
            Let Picture6. BackColor = & H8000000F
            Call TestEnd States
            Let Emergency = True
            Command8.Enabled = False
            List1.FontBold = True
            List1.AddItem "Emergency Stop on Bar " & Text6.Text
                    Listl.FontBold = False
                            Let Commandl2.Enabled = True 'error3 is enabled and is disabled when Cont after pause c
                            Commandl2.BackColor = QBColor(12)
    Case "Q"
                            Let Commandl3. Enabled = True 'error4 is enabled and is disabled when Cont after pause c
r emgncy stop is clicked
            Command13.BackColor = QBColor(12)
            Frame15.ForeColor = QBColor(12)
            Frame15.FontSize = 10
            Erame15.FontBold = True
            Command8.Enabled = True
            Command7.Enabled = True
            Command7.BackColor = &HFF8080
            Command8.BackColor = &HFF8080
    Case "z"
            Let Incomming_HighB_Flag = True
            Picture8.BackColor = QBColor(4)
            Picture9.BackColor = & H8000000F
    Case "y"
    Let Incomming LowB Flag = True
    End Select
    End If
```

End Sub

```
Private Sub Command3 Click()
```

Let AddNewArm = True
Form3.Visible $=$ True
'Form3. Show 1
Form3.Text1. Text $=$ ""
Form3.Text1.SetFocus
End Sub
Private Sub Command3 GotFocus()
If Form3.AdminPasswordFlag $=$ True Then
Let Eorm3.AdminPasswordElag = Ealse
If (Text4.Text <> "") And (Text5.Text <> "") Then
Combo2.AddItem "Armature Name: " \& Text4.Text \& " Number of Bars: " \& Text5.Text
Let $a=$ Combo2.Listcount ' used as a record number, 1 st item starts at 1
Open DefaultPath \& "Arm.TXT" For Append As \#1
Write \#1, Text4.Text, Val(Text5.Text), (a)
Let Text4.Text $=$ ""
Let Text5.Text $=" "$
Close \#1
Else
MsgBox "Enter new Armature Name and Number of Bars", vbokonly, "Enter Data"
End If
'Else
'MsgBox " You are Not Authorised to use this fuctionality"
End If
Ind Sub
Private Sub Command30 Click()
Jim $X$ As String
Jim j As Boolean
Yommand14.Enabled = True
Save Test = InputBox("Enter Job Number", "Enter The Job Number Of the Test You Wish To Open")
If Sāve Test <> "" Then

```
If Save Test <> "Find" Then
        If Dir(DefaultPath & Save_Test) <> "" Then
        List1.Clear
        Open DefaultPath & Save Test For Input As #5
                        Let j = False
                Do While Not EOF(5)
                        Input #5, aa, bb, cc, dd, ee, ff
                        If j = False Then
                        List1.AddItem "Job Number: " & aa
                        List1.AddItem "Operator's Name: " & bb
                        List1.AddItem cc
                        ListI.AddItem dd
                                ListI.AddItem "Date: " & LTrim(ee)
                                ListI.AddItem ""
                                List1.AddItem "Recorded Faults "
                                List1.AddItem ""
                                List].AddItem ff
                                Let j = True
                                    Else
                                    List1.AddItem ff
                                    If aa = "End" Then
                                    Let j = False
                                    Listl.AddItem ""
                                    Listl.AddItem ""
                                    GoTo Next Rec
                                    End If
```

                                    End If
    Next_Rec:
Loop
Close \#5
Else: MsgBox "The Requested Job Number Does Not Exist", vbokonly, "Request Error"
End If
Else
If Dir(DefaultPath \& "Saved_List.TXT") <> "" Then
Open DefaultPath \& "Saved_List. TXT" For Input As \#7
List2.Clear
Let Open Hold = ""
Do While Not EOF (7)
Input \#7, job
If Open Hold <> job Then
List2.AddItem job
Let Open Hold $=$ job
End If
Loop
If List2.ListCount $<>0$ Then
List2.Visible $=$ True
Command33.Visible $=$ True
Else
MsgBox "There Are No Tests To View", vbokOnly, "Data Error"
End If
Close \#7
Else: MsgBox "There Are No Tests To View", vbokOnly, "Data Error"
End If
End If
Else: MsgBox "Job Number Was Not Entered", vboKOnly, "Enter Data"
End If

End Sub

```
Private Sub Command31 Click()
Let Text18.Text = ""
Text18.Text = Dir1.Path
If Right(Dirl.Path, 1) <> "\" Then
    Text18.Text = Text18.Text & "\"
End If
End Sub
?rivate Sub Command32 Click()
set DelFile = True
'Form3.Visible = True
Porm3.Show 1
```

    Eorm3.Text1.Text = ""
    'Eorm3.Text1.SetEocus
    End Sub
    Private Sub Command32 GotFocus()
    If Form3.AdminPasswordFlag = True Then
    Let Form3.AdminPasswordFlag = Ealse
    Save_Test \(=\) InputBox("Enter File Name", "Delete file")
        If Save Test <> "" Then
            If Save_Test \(<>\) "Find" Then
                If Dir(DefaultPath \& Save Test) <> "" Then
                        Open DefaultPath \& Save Test For Input As \#5
                If MsgBox("Are You Sure That You Want to Delete The Selected Item?", vbYest
                ) vbyes Then
                        Call Delete
                        End If
                Close \#5
                Else: MsgBox " Eile Does Not Exist", vbokonly, "Data Error"
                End If
        Else
        If Dir(DefaultPath \& "Saved List.TXT") <> "" Then
        Open DefaultPath \& "Saved_Iİst.TXT" For Input As \#7
        List3.Clear
            Let Del_Hold = ""
                Do While Not EOF(7)
                Input \#7, Delx
                        If Del_Hold <> Delx Then
                        List \(3 . \bar{A} d d I t e m\) Delx
                        Let Del_Hold = Delx
                        End If
                Loop
                        If List3.ListCount <> 0 Then
                        List3. Visible \(=\) True
                        Command34.Visible \(=\) True
                        Else
                        MsgBox "There Are No Tests To View", vbokOnly, "Data Error"
                    End If
                Close \#7
        Else: MsgBox "There Are No Tests To View", vbokonly, "Data Error"
        End If
        End If
    Else: MsgBox "Job Number Not Entered", vbokonly, "Enter Data"
    End If
    'Else
'MsgBox " You are Not Authorised to use this fuctionality"
End If
End Sub
Private Sub Command33_Click()
List2.Visible $=$ False
Command33.Visible $=$ False
List2.Clear
List 4. Visible $=$ False
List4. Clear
End Sub
Private Sub Command34 Click()
List $3 . V i s i b l e=$ False
Command34.Visible $=$ Ealse
List 3. Clear
End Sub
Private Sub Command35 Click()
Erame 37.Visible $=$ Trué
Command46.Visible $=$ True
Pext20.Text =="
Pext21.Text $=" "$
「ext22.Text $=" "$
Yommand35. Visible $=$ False
Let Command36. Enabled $=$ True
ind Sub
Private Sub Command36 Click()
Let Text18.Text = ""
Text18.Text $=$ Dir1.Path
If Right (Dirl. Path, 1) <> " $\$ " Then
Text18.Text $=$ Text18.Text \& "\"
End If
If Text18.Text <> "" Then
Let AddNewArm = True
Form3.Visible $=$ True
'Eorm3. Show 1
Eorm3.Textl.Text = ""
Form3.TextI.SetEocus
Else
MsgBox "No Path Specified", vboKOnly, "Data Path Error"
End If
End Sub
Private Sub Command36 GotFocus()
If Eorm3.AdminPasswordFlag $=$ True Then
Let Form3.AdminPasswordFlag = False
If Dir("C:\Program Files \SavePath") <> "" Then
Open "C:\Program Files \SavePath" For Input As \#10' to save the default path
Open "Temp" For Output As \#11
Write \#11, Text18.Text
Close \#11
Close \#10
Kill ("C:\Program Files \SavePath")
Name "Temp" As "C:\Program Files \SavePath"
Command17. Enabled $=$ True
Else
Open "C: $\backslash$ Program Files $\backslash$ SavePath" For Output As \#10
Write \#10, Text18. Text
Close \#10
Command17.Enabled $=$ True
End If
Let DefaultPath $=$ Text18. Text
'Else
'MsgBox " You are Not Authorised to use this fuctionality"
End If
End Sub
Private Sub Command37 Click()
If Dir("C:\Program Files\SavePath") <> "" Then
Open "C:\Program Eiles SavePath" For Input As \#10
Input \#10, DefaultPath ' holds the path to the saved files
Let Text18.Text $=$ DefaultPath
Close \#10
Else
MsgBox "Default Path is Not Valid due to an Unauthorized change", vbokonly, "Data Path Erro
r"
End If
End Sub
Private Sub Command38_Click()
Picture2.Cls
Picture2.Visible $=$ False
End Sub
Private Sub Command39_Click()
ExcelSheet.Application.Visible $=$ True
End Sub
Private Sub Command4 Click()
Let AddNewArm = True
Form3.Visible $=$ True
'Eorm3. Show 1
Eorm3.Text1.Text $=$ " "
Eorm3.Text1. SetFocus
Private Sub Command4 GotFocus()
If Eorm3.AdminPasswordFlag $=$ True Then
Let Eorm3.AdminPasswordFlag = False
' When removing an item the listindex value is used to find the record using the
' record number it was stored under using the listcount prop. The problem is that the
' using listcount, the first item is at 1 , and for the listindex prop, the lst item in
' the combo box is at 0 . Therefore 1 is added to listindex value in order to match the
' stored record value using listcount.
If MsgBox("Are You Sure That You Want to Delete The Selected Item?", vbYesNo, "Confirm
Delete") = vbYes Then
Dim c As Integer
Let $\mathrm{b}=$ Combo2.Listindex ' note: first item in box is at 0 therefore 1 must be adde
$d$ to $=$ the listcount valne the record is saved under
Combo2.Clear
If Dir(DefaultPath \& "Arm.TXT") <> "" Then
Open DefaultPath \& "Arm.TXT" For Input As \#1
Open "Del" For Output As \#2
Do While Not EOF(1)
Input \#1, nam, num, cnt ' cnt is the record num saved when adding and start
$s$ at 1
$s$ at 1
If cnt $<>(b+I)$ Then $\quad \cos$ listindex begins at 0 and listcount start
Combo2. AddItem "Armature Name: $\quad \| \&$ nam \& " Number of Bars: $\|$ n
um

```
                                    Let c = Combo2.ListCount
```

                                    Write \#2, nam, num, c
                                    End If
                                    Loop
                Close \#1
                Close \#2
                Kill DefaultPath \& "Arm.TXT"
                Name "Del" As DefaultPath \& "Arm.TXT"
            Else: MsgBox "No Armature Properties Found", vboKOnly, "Data Error"
            End If
            End If
    - Else
    'MsgBox " You are Not Authorised to use this fuctionality"
    End If
    End Sub
Private Sub Command40 Click()
Command41.Visible $=$ True
Frame34.Visible $=$ True
End Sub
Private Sub Command41 Click()
Command4I.Visible =Ealse
Frame34.Visible = False
End Sub
Private Sub Command42_Click()
Let CalPassW = True
Form3.Visible $=$ True
' Form3. Show 1
Eorm3.Text1.Text $=$ " "
Form3.Text1.SetFocus
End Sub
Private Sub Command43_Click()
If Text20.Text 《 "" And Text21.Text 《 "" And Text22.Text <> "" Then
If Text 21. Text $=$ Text 22. Text Then
If Dir("C:\Program Files\Calibration)" \& "B 2 B Pwd") < " " Then
Open "C:\Program Files\Calibration\" \& "B_B_Pwd" For Append As \#1
Write \#1, Text 20. Text, Text 21. Text
Close \#1
Else
Open "C:\Program Files \Calibration " \& "B_2_B_Pwd" For Output As \#1
Write \#1, Text20.Text, Text21.Text
Close \#1

Else
MsgBox " The two Passwords that were entered Do Not match", vbokOnly, "Password Error"
Text21. Text $=$ ""
Text22.Text $=" "$
End If
Else
MsgBox "Please Enter All The Requested Information Before Proceeding", vbokonly, "Input Data Es ror"
End If
End Sub

Private Sub Command44_Click()
Erame37.Visible $=$ Truē
Command46.Visible $=$ True
Text20.Text = ""
Text21.Text $=$ ""
Text22.Text $=$ " "
End Sub
Private Sub Command42 GotFocus()
If Eorm3.AdminPasswordFlag = True Then
Let Eorm3.AdminPasswordFlag = False
Form2.Visible $=$ True
Let CalibFlag = True
'***********multiple reading initialization*************
Let MultiReading $=0$
Let RowCount $=0$

Set ExcelSheet = CreateObject("Excel.Sheet")
'*********End multiple reading initialization***********
'for test
If Dir("C:\Program Files\Calibration\" \& "Calibrationl.txt") <> "" Then
Open "C:\Program Files Calibration\" \& "Calibrationl.txt" For Input As \#1
Input \#1, gradient, intercept, ddate
Close \#1
Else
MsgBox "The system has not been Calibrated or the Calibtation Factor File does not exist. The $T$ est will, however, still continue", vboKOnly, "No Calibration Warning"
Let gradient $=1$
Let intercept $=0$
End If
'for test
'*******************specify hardware gain****************
Let Gain $=9.95$
'****************End specify hardware gain*****************
'Else
'MsgBox " You are Not Authorised to use this fuctionality"
End If
End Sub
Private Sub Command45 Click()
If Text20.Text <> "" Then
If Dix("C:\Program Eiles\Calibration\" \& "B 2 B Pwd") <> "" Then
Open "C:\Program Files\Calibration " \& "B_2-BWd" For Input As \#1
Open "C:\Program Eiles\Calibration " \& "B_B-Pwd2" For Output As \# 2
Do While Not EOE(1)
Input \#1, UserName, UserPassword
If UserName <> Text20. Text Then Write \#2, UserName, UserPassword End If
Loop
Close \#1
Close \#2
Kill "C:\Program Files\Calibration\" \& "B 2 B Pwd"
Name "C:\Program Files Calibration\" \& "B_2_B_Pwd2" As "C:\Program Files\Calibrationl" \& "B

```
    Text20.Text = ""
    Text21.Text = ""
    Text22.Text = ""
    Else
    MsgBox "A User Profile List Has Not Been Created", vbokonly, "Data Error"
    End If
Else
MsgBox "Please Enter User Name", vboKOnly, "Enter Data"
End If
End Sub
Private Sub Command46 Click()
Let UsrProf = True
Form3.Visible = True
'Form3.Show 1
Form3.Text1.Text = ""
Eorm3.Text1.SetFocus
```

End Sub
Private Sub Command46 GotFocus()
If Eorm3.AdminPasswordFlag = True Then
Let Eorm3.AdminPasswordFlag = False
Frame37.Visible $=$ False
Command46.Visible $=$ False
End If
End Sub
Private Sub Command47_Click()
If Text23.Text $=$ SuperUser \& Text24.Text $=$ SuperAutoSun 6 Then
Frame38.Visible = False
Else
MsgBox " You are Not Authorised to use this fuctionality", vbokonly, "Unauthorized Action"
Command47.Visible $=$ False
Text23.Visible = False
Text24.Visible $=$ False
End If
End Sub
Private Sub Command48_Click()
Frame38.Visible $=$ True
Command47.Visible = False
Text23.Text = ""
Text24.Text $=$ ""
Text23.Visible = False
Text24.Visible $=$ False
Label14.Visible = False
Labell8.Visible = False
End Sub
Private Sub Command49 Click()
Command47.Visible $=$ False
Text23.Visible $=$ False
Text24.Visible $=$ Ealse
Command49.Visible $=$ False
Label14.Visible $=$ False
Labell8.Visible $=$ False
End Sub
Private Sub Command5_Click()
If Command5.Caption $=$ "Start" Then
Picture9. BackColor $=$ QBColor (10) 'search highlighted on first count
Set ExcelSheet = CreateObject("Excel.Sheet")
Zommand16.Enabled = False
and If
Yommand42.Enabled = Ealse
'***********multiple reading initialization*************
Let MultiReading $=0$
set RowCount $=0$
Set ExcelSheet $=$ Createobject ("Excel. Sheet")
*End multiple reading initialization***********

Let Gain $=9.95$
'****************End specify hardware gain***********************)
'*************open Calibration factor file****************************)
If Dir("C:\Program Eiles\Calibration " $\dot{\alpha}$ "Calibration1.txt") <> "" Then
Open "C:\Program Files\Calibration\" \& "Calibrationl.txt" For Input As \#1
Input \#1, gradient, intercept, ddate
Close \#1
Else
MsgBox "The system has not been Calibrated or the Calibtation Factor file does not exist. The 7 est will, however, still continue", vbOKOnly, "No Calibration Warning"
Let gradient $=1$
Let intercept $=0$
End If
'Let Text9.Text $=$ gradient 'for test
'Let Text2.Text $=$ intercept ' for test

' Dim ADList As Integer
'Let Check = ""
'Let ADList $=0$
'If Dir("DefaultPath \& Save_Test") <> "" Then
', Open "DefaultPath \& Save_Test" For Input As \#5
' Do While (Not EOF(5))
' Input \#5, aa, bb, cc, dd, ee, ff
If Check <> aa Then
Let ADList $=$ ADList +1
Let Check = aa
End If
Loop Close \#5

- End If
'If ADList $<=25$ Then '***********log number of bars************* If Combo2.Text <> "" And Combo2.Text <> "Armature Select" Then
'**********log $\frac{9}{8}$ variance ${ }^{* * * * * * * * * * * * * ~}$
If Combol.Text <> "" And Combol.Text <> "Percentage Variance" Then

```
                If Option1 = True Or Option2 = True Then
```

```
Do While Text2.Text = ""
                    Text2.Text = InputBox("Enter User Name", "User Name Not Entered")
                    Loop
                        Do While Text9.Text = ""
                        Text9.Text = InputBox("Enter Job Number", "Job Number Not Entered")
                    Loop
                            Screen.MousePointer = vbArrowHourglass ' change mouse icon when test is running
                            l********** load begin time and date********
                Let Text11.Text = Space(30) & Date
                Let SaveDate = Year(Date) & "-" & Month(Date) & "-" & Day(Date)
                Let Text12.Text = Space(20) & Time
                timed = Second(Time)
                timee = Minute(Time)
                timef = Hour(Time)
                Let Savetime = Hour(Time) & "H" & Minute(Time) & "M" & Second(Time)
```

                        '********Enable Control Buttons***********
                            'Let Command6. Enabled = True' only enabled after last bar is reached, or test
                                    Let Command7. Enabled \(=\) False 'only enabled when error 3 or 4 occurs
                                    1********End Enable Control Buttons***********
    $* * * * * * * * * * * * * * * *$ Disable fields when started***********
Let Command30. Enabled = False 'For delete and open
Let Command32.Enabled = Eaise '
Let Frame30.Enabled = False $\quad$,

```
            'Let Frame31.Enabled = False '
            Let Fopen = ""
            Let Deletex = ""
                List1.Clear
                List2.Visible = Ealse
                    List2.Clear
                    List3.Visible = Ealse
                    List3.Clear
                List4.Visible = False
                List4.Clear
                Command33.Visible = Ealse
                Command34.Visible = False
                Let Print_flag= False ' for deleting file while print
                    Let Command1.Enabled = False
                    Let Command2.Enabled = False
                    Let Command3.Enabled = False
                    Let Command4.Enabled = Ealse
                    Let Command5.Enabled = False
                    Let Command9.Enabled = False
                    Let Command14.Enabled = Ealse 'print
                    Let Commandl5.Enabled = False 'save
                    Let Combol.Enabled = False
                    Let Combo2.Enabled = False
                    Let Optionl.Enabled = False
                    Let Option2.Enabled = Ealse
                    Let Command17.Enabled = False
                    Let Text1.Locked = True
                    Let Text2.Locked == True
                    Let Text3.Text = ""
                    Let Text3.Locked = True
                    Let Text4.Text = ""
                    Let Text4.Locked = True
                    Let Text5.Text = ""
                    Let Text5.Locked = True
                    Let Text9.Locked = True
                    '********End Disable fields when started************
                    MSComm1.Output = "A"
                    '**************For simulation Only***********************
                    Text15.Text = "A"
                    '**********End For simulation Only**********************
                    Command5.BackColor = QBColor(10)
                    Command5.Enabled = False
```

Else
MsgBox " Select Automated Or Manual Opperation", vbokOnly, "Select Operation Mode"
End If
Else
MsgBox "No Percentage Variance Value Selected", vbokonly, "Select Percentage Variance"
End If
'********End $\log$ 號 variance************
Else
MsgBox "Armature Not Selected", vbokonly, "Select Armature"
End If
'********End log number of bars***********
'Else
' MsgBox "The File in which the Test Files are saved contains 50 Items and if Full, Delete I
tems before proceding."
' Command30.Enabled = False
'Command32. Enabled $=$ True
'Listl. Clear 'list boxes and commands for open and delete and listl
' List2.Visible = False
' List2.Clear
' List3.Visible $=$ False
'List2.Clear
Command33. Visible = False
'Command34.Visible = False
'End If
End Sub

```
MSComm1.Output = "B"
```

    Command16.Enabled = True
    '*************EOr simulation Only********************
    Text15.Text \(=\) "B"
    '***********End For simulation Only \(\mathrm{y}^{* * * * * * * * * * * * * * * * * * * ~}\)
    Command6. BackColor \(=\) QBColor (10)
    Let Text6.Text \(=" "\)
    Let Text7.Text \(=" "\)
    Let Text8.Text \(=" "\)
    Let Pswd = 3
    Let PasswdFlag = False
    Let Command18.Enabled \(=\) True ' Lock out password
    Let Text1.Locked = Ealse ' Lock out password
    Let Command17. Enabled = True ' password
    Let Command14. Enabled \(=\) True 'print
    Let Command15.Enabled \(=\) True 'save
    Let Text1. Locked = False ' Lock out password
    Let Command17. Enabled \(=\) True ' password
    Let Command8. Enabled \(=\) False
    Command8. BackColor \(=\$ H 8000000 \mathrm{~F}\)
    Call TestEnd_States
    Command6.Enā̄led = False
    Command35. Visible \(=\) True 'new test button
    If Initial Error = True Then ' if initial bar was a Fault bar
    List1. Font $\bar{B}$ old $=$ True
List1. AddItem "Note: Reference Value Error Occured, Bar 5 has be recorded as the Bar 1 ( First
Bar )"
List1. FontBold $=$ False
MsgBox "Note: Reference Value Error Occured", vbokonly, "Reference Value Error"
End If
End Sub
Private Sub Command7_Click()
MSComm1.Output $=" \mathrm{C}$ "

Text15.Text $=$ "C"
$1 * * * * * * * * * *$ End For simulation Only*******************
Command7. BackColor $=\& H 8000000 \mathrm{~F}$
Command7.Enabled $=$ Ealse
Command8. BackColor $=\& \mathrm{H} 8000000 \mathrm{~F}$
Let Command12.Enabled $=$ Ealse 'error 3
Command12. BackColor $=\$ \mathrm{H} 8000000 \mathrm{~F}$
Frame17. ForeColor $=\& 480000012$
Eramel7.FontSize $=8$
Framel7.FontBold $=$ False

```
Let Command13.Enabled = False 'error4
Command13.BackColor = &H80000000F
Frame15.ForeColor = &H80000012
Frame15.FontSize = 8
Frame15.FontBold = False
```

End Sub
Private Sub Command8 Click()
MSComm1. Output $=$ "F"

Text 15. Text $=$ "F"
'***********End For simulation Only ${ }^{* * * * * * * * * * * * * * * * * * * ~}$
Command8. BackColor = QBColor(12)
Command7. BackColor $=\$ \mathrm{H} 8000000 \mathrm{~F}$
Let Command6. Enabled = True
Let Command6. BackColor $=\& H F F 8080$
Let Picture6. BackColor $=\& H 8000000 \mathrm{~F}$
all TestEnd States
jet Emergency = True

Command8.Enabled $=$ Ealse
List1. FontBold $=$ True
List1.AddItem "Emergency Stop on Bar " \& Text6.Text
Listl.FontBold $=$ False
End Sub

Private Sub Command9 Click()
MSComm1. Output $=$ "D"' send signal to ready the switch to take man reading

Text15.Text = "D"
'**********End For simulation Only*******************
'Command9.BackColor $=\{48000000 \mathrm{~F}$
'Command9. Enabled = Ealse
Command9. Enabled $=$ False 'disables man reading but and dsply
Frame20.ForeColor $=\& H 8000000 \mathrm{~F}$,
Picture5.BackColor $=$ QBColor(12) '
Frame21.ForeColor $=\& 48000000 \mathrm{~F}$
Let Commandio.Enabled = False 'error4
Command10.BackColor $=\& H 8000000 \mathrm{~F}$
Erame14.ForeColor $=\& \mathrm{H} 80000012$
Framel4.FontSize $=8$
Framel4.FontBold $=$ False
Let Commandll.Enabled $=$ False 'error 4
Command11. BackColor $=\& H 8000000 \mathrm{~F}$
Frame16.ForeColor $=\& H 80000012$
Framel6.FontSize $=8$
Framel6.FontBold = False
'Command8.Enabled $=$ True
'***below code is just to test \& is not prog code****
'To delete a File
'Dim Arm As ArmData
'Close \#1
'Kill DefaultPath \& "Arm.TXT"
'Texti.Enabled $=$ True
'Text1.Text = "Works"
'Text1. Enabled = False
''Picture10. FontSize $=13$
''Picturelo.Print "a"
'Command11.Enabled $=$ True
'Command11.BackColor = QBColor(12)
'Framel4. ForeColor = QBColor(12)
'Erame14.EontSize $=10$
'Framel4. FontBold = True
'Command12.Enabled = True
'Commandi2.BackColor $=$ QBColor (12)
'Frame15. ForeColor $=$ QBColor (12)
'Frame15.FontSize $=10$
'Framel5. FontBold $=$ True
'Command13. Enabled $=$ True
'Command13. BackColor $=$ QBColor(12)
'Framel6.ForeColor = QBColor(12)
'Erame16. Eontsize $=10$
'Frame16. FontBold = True
Commandlo.Enabled $=$ True
Commandio. BackColor $=$ QBColor (12)
Frame17. ForeColor $=$ QBColor (12)
Frame17.EontSize $=10$
Frame17. EontBold = True
Private Sub Dirl Change()
Let Filel. Path $=$ Dirl. Path
End Sub
Private Sub Drivel Change()
Let Dirl.Path = Drivel. Drive
End Sub
Private Sub Form Load()
Let Pswd = 3
Let PasswdFlag = False
Let Emergency $=$ False
Frame27.Visible = Ealse
'****************Calibration****************
Let Form2.Visible = False
Let Form2. CalibFlagClear = True
Let CalibFlag = False
'*************End Calibration****************
List8. AddItem Form2.CalibFlagClear 'for test

If Dir("C:\Program Files\SavePath") <> "" Then
Open "C:\Program Files \SavePath" For Input As \#10
Input \#10, DefaultPath ' holds the path to the saved files
Close \#10
Else
MsgBox "Default Path is Not Valid due to an Unauthorized change", vbokOnly, "Data Path Erro
r"
'Let DefaultPath = "xxx"
Command17.Enabled $=$ False
End If
'************** End Load default path from c:program files***************
'******* Load Percentage Selection *************************************)
'cnt is used as a record number and is the listcount value.
'ont starts at 1 but when items are loaded into the combo box, the 1 st item is at 0
If Dir(DefaultPath \& "Per.TXT") <> "" Then
Open DefaultPath \& "Per.TXT" Eor Input As \#3
Do While (Not EOF(3))
Input \#3, per, vlu
Combol.AddItem "Percentage Variance: " \& per \& "o"
Loop
Close \#3
End If


'cnt is used as a record number and is the listcount value.
' cnt starts at 1 but when items are loaded into the combo box, the 1st item is at 0
If Dir(DefaultPath \& "Arm.TXT") <> "" Then
Open DefaultPath \& "Arm. TXT" For Input As \#1
Do While (Not EOF(1))
Input \#1, nam, num, cnt
Combo2.AddItem "Armature Name: "\& nam \& " Number of Bars: " \& num
Loop
Close \#1
End If
1******* End Load Armature Selection
'*******Initilize Serial Comm port $1 * * * * * * *$
'Rec data
MSComml. RThreshold $=1$
YSComml. InputLen $=1$
4SComml. DTREnable $=$ False
4SComm1.Settings $=" 2400, N, 8,1 "$
ASComm1. CommPort $=1$
1SComm1. PortOpen $=$ True

Form1 - 22
'Trans data
MSComml. OutBufferCount $=0$
'**** End Initilize Serial Comm port 1 *****
'Text10.Locked = True

```
Let Text2.Locked = True
Let Text3.Locked = True
Let Text4.Locked = True
Let Text5.Locked = True
Let Text9.Locked = True
```

End Sub
Private Sub List2 Click()
Let Save_Test $=$ List2.Text
List1.Clear
Let Dspl_Date = ""
List4.Clear
List4.AddItem "View All"
Open DefaultPath \& Save_Test For Input As \#5
Do While Not EOF(5)
Input \#5, aa, bb, cc, dd, ee, ff
If (Dspl_Date <> ee) And (bb <> "xxx") Then List $\overline{4}$.AddItem LTrim(ee) Let Dspl_Date $=$ ee

## End If

Loop
If List4.ListCount $=1$ Then
MsgBox "There are no items to View", vbokonly, "Data Error"
List4.Clear
Else
List4.Visible = True
End If
Close \#5
Call FopenSub
'List2.Visible $=$ False
'Command33.Visible = False
End Sub
Private Sub List3 Click()
Let Save_Test $=$ List3.Text
If MsgBox/"Are You Sure That You Want to Delete The Selected Item?", vbYesNo, "Confirm Dele
te") = vbYes Then
Call Delete
End If
List3.Visible = False
Command34.Visible $=$ False
End Sub
Private Sub List4 Click()
Listl.Clear
Let Test Date $=$ List4.Text
Call Fopensub
List2.Visible $=$ False
List4.Visible $=$ False
Command33.Visible $=$ False
End Sub

Private Sub MSComm1 OnComm()
If MSCommi. Cormevent = ComEvReceive Then
Let SerIn $=$ MSComm1.Input
' after emergency stop, the micro goes into powerdowm mode and "" is sent to the pc, this value crashes the program
' b4 power down P3 is loaded with 00000011B, keeping the serial pins 1 , this should prevent a "
" value from being sent
' this code is kept here in the event an unexpected "" is sent, and thus prevent the program fr om crashing
If SerIn = "" Then
Set SerIn = "x"
and If
eet Text19. Text $=$ SerIn ' for tests only
ist5.AddItem SerIn ' for tests only

```
    If Incomming LowB Flag = True Then
    Low Byte == Asc(Se\overline{rIn})
    List6.AddItem Low_Byte
    ' for tests only
    Let Incomming_LowB Flag = False
    Let Incomming_High\overline{B}Elag = False ' redundant
    Call Calculation
    ElseIf Incomming_HighB_Flag = True Then
    High Byte = Asc(SerIn)
    List7.AddItem High Byte ' for tests only
    Let Incomming_High\overline{B}_Flag = False
    Else
    Select Case SerIn
    'Case "a" ' bar count done in the nb therefore no need to transmit this data.
    ' Call Trans_Arm_Type
    Case "b"
        MSComm1.Output = Auto Man
    Case "d"
        Command5. BackColor = &H8000000E
        Let Command5.Caption = "Start"
        Command5.Enabled = True
        Let Command8. Enabled = True
        Screen.MousePointer = vbArrow
    Case "O" 'Emergency Stop prompt when the Emergenct Stop switch on the test station is press
```

        ed
        Command8. BackColor \(=\) QBColor (12)
        Command7. BackColor \(=\& H 8000000 \mathrm{~F}\)
        Let Command6. Enabled \(=\) True
        Let Command6. BackColor \(=\& \mathrm{HFF} 8080\)
        Let Picture6. BackColor \(=\& H 8000000 \mathrm{~F}\)
        Call TestEnd States
        Let Emergency = True
        Command8.Enabled = False
        Listi. FontBold \(=\) True
        List1.AddItem "Emergency Stop on Bar " \& Text6.Text
        Listl. FontBold \(=\) Ealse
    Case "I"
        Call Bar_count
    Case "J"
Let Command10.Enabled = True ' error1
Commandlo. BackColor $=$ QBColor (12)
Frame14.ForeColor $=$ QBColor(12)
Erame14.EontSize $=10$
Framel4.FontBold $=$ True
Command9.Enabled $=$ True
Frame20. ForeColor $=$ QBColor (10) ' enables man reading but and dsply
Picture5. BackColor $=$ QBColor (10) '
Frame21. ForeColor = QBColor (10) ,
Command9. BackColor $=\&$ HEF8080
Case "m"
Let Command11.Enabled $=$ True ' error2
Commandll. BackColor $=$ QBColor (12)
Frame16. ForeColor $=$ QBColor(12)
Erame16. FontSize $=10$
Eramel6.FontBold = True
Command9.Enabled $=$ True
Command8. Enabled = Ealse
Frame20. ForeColor $=$ QBColor (10) ' enables man reading but and dsply
Picture5. BackColor $=Q B C o l o r(10)$ '
Frame21.ForeColor = QBColor(10) '
Command9. BackColor $=\&$ HFF8080
Case "N"
MsgBox "A Negative Potential has been detected. Correct the fault and Click Continue or
Click Emenengcy Stop", vbokonly, "Error: Negative Input Value Detected"
Case "L"
Let Command12.Enabled = True 'error3 is enabled emgncy stop is automatic as the system
is alxeady shut down on error3
Command12. BackColor $=$ QBColor(12)
Erame17. ForeColor = QBColor (12)
Frame17. FontSize $=10$
Erame17. FontBold = True
Command8. Enabled $=$ True
Command7.Enabled $=$ True
Command7. BackColor $=\& H F F 8080$

Command8. BackColor $=\& H F F 8080$
rgency stop" 'Egnct stop is automatically entered into hence the code below is a copy of the "Eme
Command8.BackColor $=$ QBColor (12)
Command7. BackColor $=\& H 8000000 \mathrm{E}$
Let Command6.Enabled = True
Let Command6. BackColor $=\& H F F 8080$
Let Picture6.BackColor $=\& 48000000 \mathrm{E}$
Call TestEnd_States
Let Emergency $=$ True
Command8.Enabled = False
Listl. FontBold = True
List1.AddItem "Emergency Stop on Bar " \& Text6.Text
Listi.FontBold $=$ False
Let Command12. Enabled = True 'error3 is enabled emgncy stop is automatic as the system is already shut down on error3 Command12. BackColor $=$ QBColor (12)

Case "Q"
Let Commandl3.Enabled $=$ True 'error4 is enabled and is disabled when Cont after pause o r emgncy stop is clicked

Command13. BackColor $=$ QBColor (12)
Frame15.ForeColor $=Q B C o l o r(12)$
Erame15.FontSize $=10$
Frame15.FontBold $=$ True
Command8.Enabled $=$ True
Command7. Enabled $=$ True Command7. BackColor $=\& H E F 8080$ Command8. BackColor $=\&$ HFF8080
Case "z"
Let Incomming_HighB Flag = True
Picture8. BackColor $=$ QBColor (4)
Picture9. BackColor $=\& H 8000000 \mathrm{~F}$
Case "y"
Let Incomming_LowB_Flag = True
End Select
End If
End If
End Sub
Private Sub Optionl Click()
Picture6.BackColor $\overline{=}$ QBColor(10)
Picture7.BackColor $=\& \mathrm{H} 8000000 \mathrm{~F}$
Let Auto Man = "G"
End Sub
Private Sub Option2 Click()
Picture7.BackColor $=$ QBColor (10)
Picture6.BackColor $=\$ \mathrm{H} 8000000 \mathrm{~F}$
Let Auto_Man = "g"
End Sub
Private Sub Text 15 Change ()
xa: If Text15. Text $=$ "E" Then
Call Calculation
GoTo xa
End If
End Sub
Private Sub Timer1_Timer()
'Let Form2.Text6 $=$ "xxx"
'Timerl.Enabled $=$ Ealse
' For i = 1 To 102
'Let ExcelSheet.Application.Cells((RowCount + 1), i).Value $=$ " "
'Let ExcelSheet. Application.Cells(RowCount, i).Value $=$ " "
' Next i
'Let MultiReading $=0$
'Let RowCount $=$ RowCount -1
'MSComml. Output $=$ "H"
'If Form2. CalibflagClear = Ealse Then

```
    Form1 - 25
    'Call CalibrationSub
    Else
    Call Calculation
    'Let Form2.Text6 = "xxxyyy"
    'End If
    'Picture2.Cls
    *****************Print in Pic Box for Simulation *******************************
, Picture2.Visible = True
' Picture2.Print "Job Number: " & Text9.Text
, Picture2.Print "Operator's Name: " & Text2.Text
' Picture2.Print Combo2.List(Combo2.ListIndex)
' Picture2.Print Combol.List(Combol.ListIndex)
' Picture2.Print "Date: " & LTrim(Text11.Text)
' Picture2.Print ""
' Picture2.Print "Recorded Faults "
' Picture2.Print ""
'******************End Print in Pic Box for Simulation **************************
'******************Print in Pic Box for Simulation ******************************
    Let Print current i = 0
        Do While Print current i <= (ListI.ListCount - 1)
        Picture2.Print List1.List(Print current i)
        Print_current_i = ((Print_curreñt_i) + (1))
        Loop
'*****************End Print in Pic Box for Simulation ***************************
    '******************Print in Pic Box for Simulation
        Picture2.Print ""
ate and/or remedy the"
, Picture2.Print "above recorded faults (if any)."
' Picture2.Frint "Signature, " & Text2.Text & "
    Picture2.Print ""
    '*****************End Print in Pic Box for Simulation
```


## End Sub

Public Sub TestEnd States()
Let Command18.Enabled $=$ True ' Lock out password

Let Picture6. BackColor $=\& H 8000000 \mathrm{~F}$
Let Picture7.BackColor $=\& 48000000 \mathrm{~F}$
Let Picture8.BackColor $=\& H 8000000 \mathrm{~F}$
Let Picture9. BackColor $=\& 48000000 \mathrm{~F}$

Let Text10.Locked = False ' password
Screen. MousePointer $=$ vbArrow ' change mouse icon when test is NOT running
Command5. BackColor $=\& H 8000000 \mathrm{~F}$
Command5.Enabled $=$ Ealse
Let Command7.Enabled = False
Command7. BackColor $=\& \mathrm{H} 8000000 \mathrm{~F}$
Let Command9.Enabled = False
Picture5.BackColor $=$ QBColor (12)
Frame20.Enabled = False
Erame21.Enabled = Ealse
Let Command10.Enabled $=$ False ' errorl
Command10.BackColor $=\& H 8000000 \mathrm{~F}$
Frame14.ForeColor $=\& 480000012$
Framel4.Fontsize $=8$
Framel4. FontBold $=$ False
Let Commandll.Enabled $=$ False ' error2
Command11. BackColor $=\$ \mathrm{H} 8000000 \mathrm{~F}$
Framel6.ForeColor $=\& H 80000012$
Framel6.Fontsize $=8$
Erame16. FontBold $=$ False
Let Commandi2.Enabled $=$ Ealse 'error 3
Zommand12.BackColor $=\& H 8000000 \mathrm{~F}$
Erame17.ForeColor $=\& H 80000012$

```
'**************** Time&Date ****************************
If Emergency = False Then
Let Text13.Text = Space(20) & Time
    timed = Second(Time) - timed
    If timed < 0 Then
    timed = 60 + timed
    timee = timee + 1
    End If
    timee = Minute(Time) - timee
    If timee < 0 Then
    timee = 60 + timee
    timef = timef + 1
    End If
    timef = Hour(Time) - timef
    If timef < 0 Then
    timed = 24 + timef
    End If
    Let Text14.Text = Space(20) & timef & ":" & Space(1) & timee & ":" & Space(1) & timed
End If
l*************** End Time&Date *****************************
```

End Sub
Public Sub Trans_Arm_Type() ' might not be needed as the bar count is done in the nb.
Let HB bars $=$ No-of Bars / 256
Let LB bars $=$ No_of Bars Mod 256
MSComm 1 . Output $={ }^{-}$Ch $\bar{r}($ HB_bars $)$ ' transmit High byte
MSComm1.Output $=$ Chr(LB_bars) ' transmit Low byte

```
'***************For simulation Only*
Text15.Text = Chr(HB bars)' transmit High byte
Text18.Text = Chr(LB_bars) ' transmit Low byte
'************End For simulation Only*********************
End Sub
Public Sub Bar_count()
Let No of Bars}\mp@subsup{}{}{-}=\mathrm{ No of Bars - I
If No_of_Bars < O Then }\mp@subsup{}{}{-1}<0\mathrm{ cos for the last bar this variable =0
MSComm1.\overline{Output = "P"}
Command6. BackColor = QBColor(9)
Command5.BackColor = & H8000000F
Command6. Enabled = True
'***************Eor simulation Only**********************
TextI5.Text = "P"
'************End For simulation Only*********************
Else
MSComm1.Output = "p"
'***************For simulation Only**********************
Text15.Text = "p"
'***********End For simulation Only**********************
Let Text7.Text = No of Bars
Let Text6.Text = Val(Text6.Text) + 1
End If
End Sub
?ublic Sub Calculation()
' List8.AddItem "enter" 'for test
************************Calibration*****************************
If Eorm2.CalibFlagClear = True Then
LEt CalibFlag = False
```

Eorm1 - 27
'Else
If Eorm2.CalibFlagClear = False Then
Let CalibElag = True
'End If
'List8. AddItem CalibFlag 'for test
'If CalibFlag = True Then
Call Calibrationsub
'GoTo EndReading
' End If

List8.AddItem "enterI" 'for test
Dim AvgBarReading As Single
Dim SumBarReading As Single
'**************for multiple readings*************************)
If MultiReading $=0$ Then
Let MultiReading $=100$
'Let TimerFlag $=$ True
Let Timerl.Enabled $=$ True
End If
Let MultiReading = MultiReading - 1
If MultiReading $=99$ Then
Let RowCount = RowCount +1
Let Zeroln $=0$
Let HighBCount $=0$
Let HighBCount $1=0$
Let HighBCount2 $=0$
Let HighBCount $3=0$
Let HighBCount $4=0$
Let HighBCount5 $=0$
Let SndEntry $=0$
Let StnBit_WDflg = Ealse
End If
Let ColumnCount $=100$ - MultiReading
'************End for multiple readings****************
Picture8.BackColor $=$ QBColor (4)
Picture9.BackColor $=\$ H 8000000 \mathrm{~F}$
' convert to 16 bit word
Let Bin2Dec $=$ High Byte
'Call Binary2Decimā̄
'High_Byte = Bin2Dec

'Picturel. Print Bin2Dec
'**********End For simulation Only*******************
'Let Bin2Dec = Low Byte
-Call Binary2Decimál
'Let Low Byte $=$ Bin2Dec

'Picturel.Print Bin2Dec
'**********End For simulation Only
StnBit WD $=$ ( (High_Byte * 256) + Low_Byte)
'*************For simulation Only**************************)
Picturel. Print StnBit WD


If StnBit WD $=65534$ Then Let StnBit_WDflg = True
End If


If High Byte And Low Byte $=120$ Then
Let ZeroIn = ZeroIn +1
End If
If High Byte $=120$ Then
Let HighBCount $=$ HighBCount +1
End If
If High Byte $=1$ Then

```
    Let HighBCount1 = HighBCount1 + 1
    End If
    If High Byte = 2 Then
    Let HighBCount2 = HighBCount2 + 1
    End If
    If High_Byte = 3 Then
    Let HighBCount3 = HighBCount3 + 1
    End If
    If High Byte = 4 Then
        Let HighBCount4 = HighBCount4 + 1
    End If
        If High Byte = 5 Then
    Let HighBCount5 = HighBCount5 + 1
    End If
    '**************Lower Range Value Adjust*********************
    **********************Actual Voltage Reading********************
        Let ActVolReadRes = (4.096 / 65536)
        Let ActVolRead == (StnBit WD * ActVolReadRes)
    Let mVActVolRead = ActVolRead / Gain
    Let mVActVolRead = ((gradient * (ActVolRead / Gain)) + intercept) ' actual voltage with ca
libtation factor.
    'objExcel.Application.Cells(RowCount, ColumnCount) = mVActVolRead
    ExcelSheet.Application.Cells(RowCount, ColumnCount).Value = mVActVolRead
    If High_Byte <> 120 Then
        ExCelSheet.Application.Cells((RowCount + I), ColumnCount).Value = mVActVolRead
        Let SndEntry = SndEntry + 1
    End If
```

    \(\underset{f}{\text { 'ListI.AddItem mVActVolRead \& " , " \& StnBit_WD \& " , " \& Low_Byte \& " , " \& High_Byt }}\)
    List8.AddItem RowCount 'for test
    List8. AddItern ColumnCount 'for test
    List8. AddItem mVActVolRead 'for test
    If MultiReading > 0 Then
MSComm1.Output $=$ "E" ' to microcontroller ' 07-02-06

Text15.Text $=$ "E"
'***********End For simulation Only*******************
Go'To EndReading
End If
If MultiReading $=0$ Then
Let SumBarReading $=0$
For col = 1 To 100
Let SumBarReading $=$ SumBarReading + ExcelSheet.Application.Cells (RowCount, col). Value
Next col
Let AvgBarReading $=$ SumBarReading / 100 ' $100=$ no of readings
'objExcel.Application.Cells(RowCount, 102) = AvgBarReading' put the average of this row in
col 102
ExcelSheet.Application.Cells(RowCount, 102).Value $=$ AvgBarReading
End If
'********************End Actual Voltage reagings*****************

If Zeroln > 50 Then
For adj $=1$ To 100
ExcelSheet.Application.Cells(RowCount, adj).Value $=$ "Adjusted"
Next adj
ExcelSheet.Application.Cells(RowCount, 102).Value $=" 0 "$
Let AvgBarReading $=0$
End If
'List1.AddItem HighBCount \& " $"$ " \& HighBCount1 \& " ' " \& HighBCount2 \& " , " \& HighBCount3
\& " ' " \& HighBCount4 \& " $"$ \& HighBCOunt5
'If (HighBCount1 > 10 Or HighBCount $2>10$ Or HighBCount $3>10$ Or HighBCount $4>10$ Or HighBC
ount5 > 10) Then
, For adj $=1$ To 100
' If ExcelSheet.Application. Cells((RowCount +1$)$, adj). Value $=$ " "Then
' Let ExcelSheet.Application.Cells ((RowCount +1 ), adj).Value $=" 0$ " Then
Let Exce
Next adj

```
    , Let SumBarReading = 0
    , For col = I To 100
    ' Let SumBarReading = SumBarReading + ExcelSheet.Application.Cells(RowCount + 1, col).Ve
lue
    Next col
    , Let AvgBarReading = SumBarReading / SndEntry
    , Eor adj = 1 To 100
    ' ExcelSheet.Application.Cells(RowCount, adj).Value = ExcelSheet.Application.Cells((Row(
ount + 1), adj).Value
    ', Let ExcelSheet.Application.Cells((RowCount + 1), adj).Value = ""
    , Next adj
    ', ExcelSheet.Application.Cells(RowCount, 102).Value = AvgBarReading
    ExcelSheet.Application.Cells(RowCount, 102). Font.Bold = True
    'End If
        'For adj = 1 To 100
        'Let ExcelSheet.Application.Cells((RowCount + 1), adj).Value = ""
        'Next adj
```

    '**************set Reference value on first reading*************
        If Initial Count \(=0\) Then
        'Let Reference \(=\) StnBit \(W D\)
        'Let ActReference = (Reference * ActVolReadRes)
        'Let mVActReference \(=\) (ActReference / Gain)
        'objExcel.Application.Cells(RowCount, ColumnCount) = mVActReference
        For Acol =1 To 100
        ExcelSheet. Application.Cells(RowCount, Acol). Font. Bold \(=\) True
        Next Acol
                Let AvgRefReading = AvgBarReading
                ExcelSheet.Application.Cells(RowCount, 102).Font. Bold \(=\) True
    End If
    Let Initial_Count $=$ Initial_Count +1
$1 * * * * * * * * * * *$ End set Reference value on first reading************

If AvgRefReading $<>0$ Then ' checking if reference value $=0$
' calc variance of current reading
If Initial_Count $>0$ Then
'Current Vāriance $=\left(\left(\left(\operatorname{Abs}\left(S t n B i t \_W D-\text { Reference }\right)\right) / \text { Reference }\right) * 100\right)^{\prime} 07-03-06$
Current Variance $=(((\operatorname{Abs}($ AvgBarRēading - AvgRefReading $)) /$ AvgRefReading $) * 100)$
$\prime * * * * * * * * * * * * * * * * * * * *$ Check For Open cct, Short cct And Comparisons With Refrence $\begin{gathered}\text { O } \\ \text { Ot************ }\end{gathered}$
'If a value less than 20 is recorded, the CM is Indicating a possible SC and should be disp layed as such.
' Circuit If StnBit_WD $>20$ Then ' the min value of 20 may be change depending on the typical short Circuit reading
' If 65534 is recorded, the $C M$ is Indicating an out of range reading. This should be dis played as a possible OC.

If StnBit WDflg $=$ True Then
Listl. AddItem "Eault on Bar: " \& Text6. Text \& ", Volt-Drop Reading Is Out of Range, Indicating A Possible Open Circuit"

Let Text8.Text $=\operatorname{Val}($ Text 8. Text $)+1$
ElseIf AvgBarReading $=0$ Then
List1.AddItem "Fault on Bar: " \& Text6.Text \& ", Volt-Drop Reading Is Zero (0V), In
dicating A Possible Short Circuit"
Let Text8. Text $=$ Val $($ Text 8. Text $)+1$
Else
' compare to selected ${ }^{5}$ variance and log if a fault
If (Current Variance $>$ Percentage) Then
Listl.AddItem "Fault on Bar: " \& Text6.Text \& ", Percentage Variance $=" \&$ Zurrent Variance \& ", Bar Reading: " \& AvgBarReading \& "V" \& ", Reference: " \& AvgRefRead

Let Text8.Text $=$ Val $($ Text 8. Text $)+1$
End If
'end current reading and comparison
End If
'end possible OC check

Else
ListI.AddItem "Fault on Bar: " \& Text6.Text \& ",
Equal to Zero, Indicating A Possible Short Circuit"
End If
'end possible SC check


```
Command9.Enabled = Ealse 'disables man reading but and dsply
Erame20.Enabled = False
Picture5.BackColor = QBColor(12) ,
Frame21.Enabled = False
Let Commandl0.Enabled = False ' errorl
Commandl0.BackColor = &H8000000F
Frame14.EoreColor =&H80000012
Frame14.FontSize = 8
Framel4.FontBold = False
Let Command11. Enabled = False ' error2
Commandll.BackColor }=$H8000000\textrm{F
Frame16.ForeColor = & %80000012
Frame16.FontSize = 8
Framel6.FontBold = False
```

    ' checking the 1 st 5 readings to see if the ref reading is from a fault bar.
    Let Initial_Count = Initial_Count +1
        If (Initial_Count \(=6\) ) And (Val(Text8.Text) \(=5\) ) Then
    'Let Refereñce = StnBit_WD
    'Let ActReference \(=\) (Reference * ActVolReadRes)
    'Let mVActReference \(=(\) ActReference \(/ 1000)\)
        Let AvgRefReading = AvgBarReading
        Let Text8.Text \(=\) " "
        Let No of Bars \(=((\operatorname{Val}(\) Text \(6 . T e x t)+\operatorname{Val}(T e x t 7 . T e x t))-1)\)
        Let Text7. Text \(=\) No_of_Bars
        Let Text6. Text \(=1\)
        Let Initial_Error = True ' flag to indicate Ref value error.
        Listi. FontBold \(=\) True
        Listl.AddItem "Test Restarted, Bar 5 is reset as the Initial (Fjrst) Bar!"
        Listl. FontBold = False
        End If
    ```
            MSComm1.Output = "S" ' to microcontroller ' 07-02-06
            Picture8.BackColor = &H8000000F
            Picture9.BackColor = QBColor(10)
            '***************For simulation Only***********************
            Text15.Text = "S"
            '***********End For simulation Only**********************
```

        Else
        MsgBox " The Recorded reference value is 0 Volts \& is therefore not Valid. Please Restart this
        Test", vbokonly, "Invalid Reference Value"
        MSComml. Output \(=\) "S" ' to microcontroller ' 07-02-06
        Picture8.Backcolor \(=\$ 48000000 \mathrm{~F}\)
        Picture9.BackColor \(=\) QBColor (10)
    
Text15.Text $=" S "$
***********End For simulation Only*******************
End If
indReading:
End Sub
?ublic Sub Binary2Decimal()
yim B2D_flag As Boolean
jim $B 2 D^{-}$a As String
)im $B 2 D^{-} b$ As Integer

Dim B2D d As Integer
Dim B2D_total As Integer
Let B2D_a = ""
Let B2D_a $=$ Bin2Dec
Let $B 2 D^{-} 1=1$
Let $B 2 D_{-}$flag = False
Let $B 2 D_{-} b=\operatorname{Len}\left(B 2 D_{-} a\right)$
Do While B2D flag = False
Let $B 2 D_{\_}=$InStr $\left(B 2 D_{1} 1, B 2 D \_a, ~ " 1 ", 0\right)$
If $B 2 D$ $C<>0$ Then
Let $B 2 \bar{D}$ total $=B 2 D$ total $+2 \wedge\left(B 2 D_{1} b-B 2 D \_c\right)$
Let $B 2 D^{-1}=B 2 D-C+{ }^{-} 1$
Else
Let B2D_flag = True
End If
Loop
Let $\operatorname{Bin} 2 \mathrm{Dec}=\mathrm{B} 2 \mathrm{D}$ _total
End Sub
Public Sub FopenSub()

```
If Test_Date = "View All" Then
        Open DefaultPath & Save_Test For Input As #5
            Let j = False
            Do While Not EOF(5)
                Input #5, aa, bb, cc, dd, ee, ff
                If j = False Then
                List1.AddItem "Job Number: " & aa
                List1.AddItem "Operator's Name: " & bb
                List1.AddItem cc
                List1.AddItem dd
                List1.AddItem "Date: " & LTrim(ee)
                List1.AddItem ""
                List1.AddItem "Recorded Faults "
                List1.AddItem ""
                List1.AddItem ff
                Let j = True
                Else
                        List1.AddItem ff
                            If aa = "End" Then
                            Let j = False
                                    List1.AddItem ""
                                    List1.AddItem ""
                                    End If
                End If
            Loop
            Close #5
Else
        Open DefaultPath & Save_Test For Input As #5
            Let j = False
            Do While Not EOE(5)
                Input #5, aa, bb, cc, dd, ee, ff
                    If (Test Date == LTrim(ee)) Then
                    If j = False Then
                            Listl.AddItem "Job Number: " & aa
                            List1.AddItem "Operator's Name: " & bb
                            ListI.AddItem cc
                            List1.AddItem dd
                            ListI.AddItem "Date: " & LTrim(ee)
                            ListI.AddItem ""
                            List1.AddItem "Recorded Eaults "
                        List1.AddItem ""
                        Listl.AddItem ff
                        Let j = True
                            'End If
                    Else
                            List1.AddItem ff
                            If aa = "End" Then 'xxx (or End) signals end of a test and
all the fields for the next test has to be printed
                                    Let j = False
                                    List1.AddItem "
```


## List1.AddItem ""

End If
End If
End If
Loop
Close \#5
End If
'aa is the Job No field
'bb is the Operators Name field
'cc is the Armature Selection field
'dd is the Percentange Variance field
'ee is the Date field
'ff is the Recorded Raults field
End Sub
Public Sub Delete()
If Dir(DefaultPath \& "Saved List.TXT") <> "" Then
Open DefaultPath \& "Saved_List.TXT" For Input As \#7
Open "Saved_List_Del" Eor Output As \#8
Do While Not EOF(7)
Input \#7, look
If Save Test <> look Then
Write \#8, look
End If
Loop
Close \#7
Close \#8
Kill DefaultPath \& "Saved_List.TXT"
Name "Saved_List_Del" As DefaultPath \& "Saved_List.TXT"
Else: MsgBox "File Does Not Exist", vbokonly, "Data Errō"
End If
close \#5
If Dir(DefaultPath \& Save_Test) <> "" Then
Kill (DefaultPath \& Save_Test)
List1.Clear
End If
End Sub
Public Sub FsaveSub()

'objExcel.Application.Save (Text9.Text \& Text11.Text)
'objExcel.Application.Quit
ExcelSheet.SaveAs DefaultPath \& Text9.Text \& Space(2) \& SaveDate \& Space (2) \& Savetime ExcelSheet.Application.Quit Set ExcelSheet $=$ Nothing

```
End Save Excel Data****************************
```

Dim Add Flagx As Boolean
Let Add Flagx = False
Let Save Test $=$ Text9.Text ' redundant
If Dir(DefaultPath \& "Saved_List.TXT") <> "" Then
Open DefaultPath \& "Saved_List.TXT" For Input As \#7 'file for the list of all jobs saved
Do While Not EOE (7)
Input \#7, Add list If Add list $=$ Save Test Then Lé Add Flagx $\equiv$ True
End If
Loop

Close \#7
If Add_Flagx = False Then
Let Add Flagx = Ealse ' redundant
Open Defaultpath \& "Saved List.TXT" For Append As \#7
Write \#7, Save_Test
Close \#7
End If
Else
Open DefaultPath \& "Saved List.TXT" Eor Append As \#7
Write \#7, Save Test
Close \#7

End If
Open DefaultPath \& Save Test For Append As \#5
Let $i=0$
Do While $i<=$ (List1.ListCount - 1)
Write \#5, Text9.Text, Text2.Text, Combo2.List(Combo2.ListIndex), Combol.List(Combol.Lis
tIndex), LTrim(TextII.Text), List1.List(i)
Let $i=i+1$
Loop
Write \#5, "End", "xxx", "xxx", "xxx", LTrim(Text11.Text), "End Of Recorded Results" Close \#5
End Sub
Public Sub CalibrationSub()
Let Form2.Text6 $=$ "xxxyyysun"
Dim AvgBarReading As Single
Dim SumBarReading As Single

```
****************for multiple readings*******************
If MultiReading = 0 Then
Let MultiReading = 100
Let TimerFlag = True
Let Timerl.Enabled = True
Let Form2.Text5.Text = Timerl.Interval
End If
Let MultiReading = MultiReading - 1
If MultiReading = 99 Then
Let RowCount = RowCount + 1
Let ZeroIn = 0
Let HighBCount = 0
Let HighBCount1 = 0
Let HighBCount2 = 0
Let HighBCount3 = 0
Let HighBCount 4 = 0
Let HighBCount5 = 0
Let SndEntry = 0
End If
Let ColumnCount = 100 - MultiReading
'**************End for multiple readings******************
```

StnBit_WD $=(($ High_Byte * 256) + Low_Byte)
' $\star * * * * \bar{*} * * * * * * *$ For simulation Only $\mathrm{y}^{* * *} \bar{*} * * * * * * * * * * * * * * * *$
Picture1. Print StnBit WD


If High_Byte And Low Byte $=120$ Then
Let ZeroIn $=$ ZeroIn $\mp 1$
End If
If High Byte $=120$ Then
Let HighBCount $=$ HighBCount +1
End If
If High Byte $=1$ Then
Let HighBCount $1=$ HighBCount $1+1$
End If
If High Byte $=2$ Then
Let HighBCount2 $=$ HighBCount2 +1
End If
If High Byte $=3$ Then
Let HighBCount $3=$ HighBCount $3+1$
End If
If High_Byte $=4$ Then
Let HighBCount $4=$ HighBCount $4+1$
End If
If High Byte $=5$ Then
Let HighBCount $5=$ HighBCount5 +1
End If

```
                                    *Actual Voltage Reading********************
    Let ActVolReadRes = (4.096 / 65536)
    Let ActVolRead = (StnBit WD * ActVolReadRes)
    Let mVActVolRead = ((ActVolRead) / Gain) '[ removed for test ]
    ExcelSheet.Application.Cells(RowCount, ColumnCount).Value = mVActVolRead
    If High_Byte <> 120 Then
    ExcelSheet.Application.Cells((RowCount + 1), ColumnCount).Value = mVActVolRead
    Let SndEntry = SndEntry + 1
    End If
    Eorm2.List1.AddItem mVActVolRead & " , "& StnBit_WD & " , " & Low_Byte & " , "& Hiç
If MultiReading > 0 Then
    MSComml.Output = "E" ' to microcontroller ' 07-02-06
    GoTo EndReading2
End If
If MuItiReading = 0 Then
'****************Reading Timer*******************************
Let TimerFlag = False
Let Timerl.Enabled = False
'****************Reading Timer*******************************
    Let SumBarReading = 0
    For Col = 1 To 100
    Let SumBarReading = SumBarReading + ExcelSheet.Application.Cells(RowCount, col).Value
    Next col
    'For col = 1 To 100
    'Let ExcelSheet.Application.Cells(RowCount, col).VaIue = ""
    'Next col
    Let AvgBarReading = SumBarReading / 100 '100= no of readings
    'objExcel.Application.Cells(RowCount, 102) = AvgBarReading ' put the average of this row in
col 102
    ExcelSheet.Application.Cells(RowCount, 102).Value = AvgBarReading
    ExcelSheet.Application.Cells(RowCount, 102). Font.Bold = True
    'Eor i = 0 To 39
    'If Form2.Command1(i).Value = True Then
    Let i = Form2.ReadingBoxIndex
    Let Text25.Text = i
    Let Form2.Text2(i).Text = AvgBarReading
    Let CalibRefIn = Val(Form2.Textl(i).Text)
    'ExcelSheet.Application.Cells(RowCount, 3).Value = CalibRefIn
    'ExcelSheet.Application.Cells(RowCount, 1).Value = RowCount
    Let Eorm2.Commandl(i).Enabled ExcelSheet.Application.Cells(RowCount, 2).Value = CalibRefIn
= False
    'End If
    'Next i
'*************Lower Range Value Adjust*********************
    If ZeroIn > 50 Then
        For adj = 1 To 100
        ExcelSheet.Application.Cells(RowCount, adj).Value = "Adjusted"
        Next adj
        ExcelSheet.Application.Cells(RowCount, 102).Value = "0"
        Let Form2.Text2(i).Text = "0"
    End If
    Let Eorm2.Text6 = HighBCount & " ' " & HighBCount1 & " ' " & HighBCount2 & " ' " & HighBCou
nt3 & " ' " & HighBCount4 & " ' " & HighBCount5
    If (HighBCount1 > 10 Or HighBCount2 > 10 Or HighBCount3 > 10 Or HighBCount4 > 10 Or HighBCo
ant5 > 10) Then
        For adj = 1 To 100
            If ExcelSheet.Application.Cells((RowCount + 1), adj).Value = "" Then
            Let ExcelSheet.Application.Cells((RowCount + 1), adj).Value = "0"
```

Let SumBarReading $=0$
For col $=1$ To 100
Let SumBarReading $=$ SumBarReading + ExcelSheet.Application.Cells(RowCount +1 , col).Va:
Next col
Let AvgBarReading = SumBarReading / SndEntry
For $\mathrm{adj}=1$ To 100
ExcelSheet.Application.Cells(RowCount, adj).Value = ExcelSheet.Application.Cells(/RowCc
), adj).Value
Let ExcelSheet.Application.Cells((RowCount +1$)$, adj).Value $=$ "
Next adj
ExcelSheet.Application. Cells(RowCount, 102).Value $=$ AvgBarReading
ExcelSheet.Application.Cells(RowCount, 102). Font. Bold $=$ True
Let $i=$ Form2.ReadingBoxIndex
Let Text25.Text $=1$
Let Form2. Text2 (i). Text =AvgBarReading
Let CalibRefIn = Val(Form2.TextI(i).Text)
End If
'If HighBCountl > 0 Then
'ExcelSheet.Application.Cells(RowCount, adj).Value = "Adjusted"
'Next adj
'ExcelSheet.Application.Cells(RowCount, 102).Value = "0.0016"
'Let Form2.Text2(i).Text $=$ "0.0016"
'End If
'
'If HighBCount2 $>0$ Then
'For adj = 1 To 100
'ExcelSheet.Application.Cells(RowCount, adj).Value $=$ "Adjusted"
'Next adj
'ExcelSheet.Application.Cells(RowCount, 102).Value $=$ "0.0032"
'Let Form2.Text2(i).Text $=0.0032 "$
'End If
'If HighBCount $1>0$ Then
'For adj = 1 To 100
'ExcelSheet.Application.Cells(RowCount, adj).Value $=$ "Adjusted"
'Next adj
'ExcelSheet.Application.Cells(RowCount, 102).Value $=$ "0.0048"
'Let Form2.Text2(i).Text $=\mathbf{= 0 . 0 0 4 8 "}$
'End If
'If HighBCountl > 0 Then
' For adj $=1$ To 100
'ExcelSheet.Application.Cells(RowCount, adj).Value = "Adjusted"
'Next adj
'ExcelSheet.Application.Cells(RowCount, 102).Value $=0.0064 "$
'Let Form2.Text2(i).Text $=\mathbf{" 0 . 0 0 6 4 "}$
' End If
'If HighBCount1 > 0 Then
'For adj $=1$ To 100
'ExcelSheet.Application.Cells(RowCount, adj).Value $=$ "Adjusted"
'Next adj
'ExcelSheet. Application.Cells(RowCount, 102).Value $=$ "0.008"
'Let Form2.Text2(i).Text $=$ "0.008"
'End If
For adj $=1$ To 100
Let ExcelSheet.Application.Cells((RowCount +1$)$, adj). Value $=$ " $"$
Next adj
End If

'End If
'*******************End Actual Voltage reagings*******************)
MSComm1.Output $=$ "S" ' to microcontroller ' 07-02-06
'*************For simulation Only********************
Text15.Text $=$ "S"
$1 \star * * * * * * * * *$ End For simulation Only*******************
'Else
'MsgBox " The Recorded reference value is O Volts \& is therefore not Valid. Please Restart this Test" 'MSComml.Output $=$ "S" ' to microcontroller ' 07-02-06
$1 \star * * * * * * * * * * * *$ Eor simulation Only $\begin{gathered}* * * * * * * * * * * * * * * * * * * ~\end{gathered}$
'Text15. Text $=$ "S"
$1 * * * * * * * * * *$ End For simulation Only*******************
'End If
EndReading2:
End Sub

Dim cSum Of Prod xy As Double
Dim cSum_x Ās Single
Dim cSum y As Single
Dim cGrad As Single
Dim cIntcpt As Single
Dim CProd $x$ As Single
Dim cSum_Prod_x As Single
Dim aSum Of Prod xy As Single
Dim asum-x Ās Single
Dim aSum y As Single
Dim aGrad As Single
Dim aIntcpt As Single
Dim aprod $x$ As Single
Dim aSum Prod_x As Single
Dim Adj_m As Single
Dim Adj_c As Single
Public ReadingBoxIndex As Integer
Public CalibFlagClear As Boolean
Dim ExcelSheet As Object

Private Sub Commandl Click(Index As Integer)
Let CalibFlagClear = False
For $i=0$ To 39
If Commandl(i). Value $=$ True Then
Let ReadingBoxIndex = i
Let Text3.Text $=$ ReadingBoxIndex
Let Checkl(i).Value = 1
Let Commandl(i).Enabled = False
End If
Next i
Form1.MSComm1. Output $=$ "H"
'*******for test*******************
Let Text3.Text $=$ ReadingBoxIndex
'If Form1.CalibFlag = True Then
Let Text4.Text = "True"
'Else
Let Text4.Text = "false"
'End If
'*******for test*******************
End Sub
Private Sub Command2 Click()
Form2.Visible = False
Let CalibflagClear = True
ExcelSheet.Application.Quit
Set ExcelSheet = Nothing
End Sub
Private Sub Command3 Click()
For $i=0$ To 39
Let Commandl(i).Enabled $=$ True
Let Checkl(i).Value $=0$
Next i
End Sub
Private Sub Form2_Load()
End Sub

Private Sub Command4 Click()
ExcelSheet.Application.Visible $=$ True
End Sub
Private Sub Command5 Click()
'Dim Incomp As Integēr
'Let Incomp = 0
'For $\mathrm{i}=0$ To 39
'If Textl(i).Text = "" Or Textl(i).Text = "" Then
'Let Incomp $=$ Incomp +1
'End If

Form2-2
'Next i
'If Incomp $=0$ Then

```
    Let cProd xy = 0
    Let cSum Of Prod xy = 0
    Let csum x = 0
    Let csum}\mp@subsup{}{}{-}y=
    Let cGrad = 0
    Let cIntcpt = 0
    Let cProd x = 0
    Let cSum_Prod_x = 0
    Let aProd xy = 0
    Let aSum \overline{Of Prod xy = 0}00
    Let aSum-}x\equiv
    Let aSum_y = 0
    Let aGra\overline{d}=0
    Let aIntcpt = 0
    Let aProd x = 0
    Let aSum_\overline{Prod_x = 0}
```

    For i \(=0\) To 39
    Let cProd xy \(=(\) Val \((\) Textl(i).Text) * \((i+1))\)
    Let cSum_Of Prod_xy = cSum_Of_Prod_xy + cProd_xy
    Let cSum_x \(=\operatorname{cSum} x+\operatorname{Val}(\overline{T e x t} 1(i)\). Text)
    Let cSum_y \(=\) cSum_y \(+(1+i)\)
    Let cProd_x = ((Val(Textl(i).Text)) * Val((Textl(i).Text)))
    Let cSum_Prod_x = cSum Prod_x + cProd \(x\)
    Let \(\operatorname{aProd} x y=(\operatorname{Val}(\) Text2(i).Text) \(*(i+1))\)
    Let aSum_Of_Prod_xy = aSum_Of_Prod_xy + aProd_xy
    Let aSum_x = aSum \(x+\operatorname{Val}(\) Text2(i).Text)
    Let \(\operatorname{aSum}^{-} y=\operatorname{aSum}^{-} y+(1+i)\)
    Let \(\mathrm{aProd}_{\mathrm{x}}=((\operatorname{Val}(T e x t 2(i) . T e x t))\) * Val((Text2(i).Text)))
    Let aSum_Erod_x = aSum_Prod_x + aProd x
Next i
Let cGrad $=\left((40 *\right.$ cSum_Of_Prod_xy $\left.)-\left(\operatorname{cSum} x * \operatorname{cSum}_{-} y\right)\right) /((40 *$ cSum_Prod_x) $-((\operatorname{cSum} \quad x)$

* (cSum x)) )
Let ${ }^{-}$cIntcpt $=(($cSum_y $)-($cGrad * CSum_x) $) / 40$

Let aIntcpt $=((\operatorname{aSum} y)-(\operatorname{aGrad} * \operatorname{aSum} \mathrm{x})) / 40$
*******************for test**************************)
Let Text 3. Text $=$ cGrad
Let Text 4. Text $=$ cIntcpt
Let Text5.Text $=$ aGrad
Let Text6. Text $=$ a Intcpt
'using $y l=m l x l+c l$ for the best fit calibrated injected linear plot
'and
'using $y^{2}=m 2 \times 2+c 2$ for the best fit actual system reading linear plot
'we get
'mlx1 $+\mathrm{c} 1=\mathrm{m} 2 \times 2+\mathrm{c} 2, \quad(\mathrm{y} 1=\mathrm{y} 2)$
'therefore, $\mathrm{x} 1=\mathrm{x} 2 *[\mathrm{~m} 2 / \mathrm{m} 1]+[(\mathrm{c} 2-\mathrm{c} 1) / \mathrm{ml}]$
' $x 1$ is the true, real or adjusted reading, given the untrue reading, $x 2$.
Let Adj m = Text3.Text 'aGrad / cGrad
Let Adj c = Text4.Text '(aIntcpt - cIntcpt) / cGrad
Let Adj_m = aGrad / cGrad
Let Adj_c = (aIntcpt - cIntcpt) / cGrad
Open "C:\Program Files\Calibration\" \& "Calibration2" For Output As \#2
Write \#2, Adj m, Adj c, Date
Close \#2
If Dir("C:\Program Files\Calibration\" \& "Calibrationl.txt") <> "" Then
Kill "C:\Program Files\Calibration\" \& "Calibrationl.txt"
Else
Open "C:\Program Files\Calibration\" \& "Calibrationl.txt" For Output As \#1

Close \#1
Kill "C:\Program Files Calibration\" \& "Calibrationl.txt"
End If
Name "C:\Program Eiles Calibration\" \& "Calibration2" As "C:\Program Files Calibration\" \& "Calibrationl.txt"

- Else
' MsgBox "Input Fields Incomplete. Please Complete all Recordings before continuing"
- End If

End Sub

Private Sub Command6_Click()
End Sub
Private Sub Form Load()
Set ExcelSheet = CreateObject("Excel.Sheet")
End Sub

Public AdminFasswordFlag As Boolean
Private Sub Command Click()
If Text1. Text $=$ "AdminAutosun6" Then
Let AdminPasswordFlag $=$ True
If Form1.AddNewArm = True Then
Forml. Command3.SetFocus
End If
If Formi.RemoveArm = True Then
Forml. Command4. SetFocus
End If
If Forml.AddNewVal = True Then
Forml.Commandl. SetEocus
End If
If Formi.RemoveVal $=$ True Then
Forml. Command2. Set Focus
End If
If Form1.CalPassW $=$ True Then
'Eorm1.Command42.SetFocus
End If
If Form1.PathPassW $=$ True Then
Form1. Command36. Set Eocus
End If
If Forml.DelFile $=$ True Then
Form1.Command32.SetFocus
End If
If Forml.UsrProf $=$ True Then
Form1. Command46. Set Focus
End If
Else
MsgBox "You are NOT Authorized to perform this action"
End If
Form3.Visible = Ealse
Let Formi.AddNewArm = False
Let Form1.AddNewVal = False
Let Form1. RemoveArm = False
Let Formi. RemoveVal $=$ False
Let Eorml.CalPassW = Ealse
Let Form1. PathPassW = False
Let Forml. UsrProf = False
Let Form1.DelFile = False
End Sub
Private Sub Form LostFocus()
Form3.Visible $=$ False
End Sub

Recorded Faults

## Emergency Stop on Bar 0

End Of Recorded Results

Job Number: matadin
Operator's Name: ccccccc
Armature Name: h Number of Bars: 200
Percentage Variance: 15\%
Date: 2005/05/05
Recorded Faults
Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: $Z \times Z \times Z \times Z \times Z \times Z z \times Z \times Z$
Armature Name: e Number of Bars: 25
Percentage Variance: $25 \%$
Date: 2005/05/05
Recorded Faults
Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: vvwvvvv
Armature Name: c Number of Bars: 15
Percentage Variance: $25 \%$
Date: 2005/05/05
Recorded Faults

Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin Operator's Name: v1v1v1v1v1v1
Armature Name: c Number of Bars: 15
Percentage Variance: 5\%
Date: 2005/05/05
Recorded Faults

Emergency Stop on Bar 0
End Of Recorded Results
lob Number: matadin
jperator's Name: matadin 05/05/05
trmature Name: d Number of Bars: 20
'ercentage variance: $20 \%$
late: 2005/05/05
ecorded Faults

## mergency Stop on Bar 0

nd Of Recorded Results

## Job Number: matadin

## Operator's Name: matadin2 05/05/05

Armature Name: c Number of Bars: 15
Percentage Variance: 30\%
Date: 2005/05/05

Recorded Faults

Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: 09-05
Armature Name: e Number of Bars: 25
Percentage Variance: 15\%
Date: 2005/05/09
Recorded Faults
Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: sun 09-05
Armature Name: d Number of Bars: 20
Percentage Variance: 25\%
Date: 2005/05/09
Recorded Faults
Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: sun2 09-05
Armature Name: e Number of Bars: 25
Percentage Variance: 35\%
Date: 2005/05/09
Recorded Faults

Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: sun3 09-05
Armature Name: d Number of Bars: 20
Percentage Variance: 15\%
Date: 2005/05/09
रecorded Faults

Emergency Stop on Bar 0
:nd Of Recorded Results
ob Number: matadin iperator's Name: sun4 09-05
irmature Name: f Number of Bars: 50
'ercentage Variance: 35\%
late: 2005/05/09

## Emergency Stop on Bar 0

 End Of Recorded ResultsJob Number: matadin
Operator's Name: sun5 09-05
Armature Name: e Number of Bars: 25
Percentage Variance: 20\%
Date: 2005/05/09
Recorded Faults
Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: sunveer
Armature Name: d Number of Bars: 20
Percentage Variance: 20\%
Date: 2005/05/09
Recorded Faults
Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: sunveer2
Armature Name: a Number of Bars: 5
Percentage Variance: 15\%
Date: 2005/05/09
Recorded Faults
Emergency Stop on Bar 0
End Of Recorded Results

Job Number: matadin
Operator's Name: sunny 09-05
Armature Name: f Number of Bars: 50
Percentage Variance: $40 \%$
Jate: 2005/05/09
Recorded Faults
:mergency Stop on Bar 0
:nd Of Recorded Results
ob Number: matadin
iperator's Name: matadin 09-05
rmature Name: c Number of Bars: 15
ercentage Variance: $25 \%$
ate: 2005/05/09
ecorded Faults
nergency Stop on Bar 0
1d Of Recorded Results
ib Number: matadin
jerator's Name: matadin 09-05
mature Name: c Number of Bars: 15
rcentage Variance: $10 \%$

## Date: 2005/05/09

Recorded Faults
Emergency Stop on Bar 0 End Of Recorded Results

# Job/Serial Number: 001 Test Results <br> Operator's Name: Sunveer Matadin <br> Armature Name: b Number of Bars: 10 <br> Percentage Variance: 5\% <br> Date: 2006/04/12 

## Recorded Faults

Fault on Bar: 3, Percentage Variance $=19.45295$, Bar Reading: 0.1623932 V , Reference: 0.1359474 V
Fault on Bar: 5, Percentage Variance $=10.68346$, Bar Reading: 0.1214235 V , Reference: 0.1359474 V
Fault on Bar: 7, Percentage Variance $=11.05382$, Bar Reading: 0.1509748 V , Reference: 0.1359474 V
Fault on Bar: 8, Volt-Drop Reading is Zero ( OV ), Indicating A Possible Short circuit
Fault on Bar: 9, Volt-Drop Reading is Out Of Range, Indicating A Possible Open Circuit
Emergency Stop on Bar 10
I, Sunveer Matadin acknowledge the above results and pledge to investigate and/or remedy the above recorded faults (if any).

Signature, Sunveer Matadin $\qquad$

## Automated Volt-Drop Test Report

## Job/Serial Number: Test Results

## Operator's Name: Sunveer Matadin

Armature Name: b Number of Bars: 10

## Percentage Variance: 5\%

Date: 2006/04/12

## Recorded Faults

Fault on Bar: 3, Percentage Variance $=19.28123$, Bar Reading: 0.1626973V, Reference: 0.136398 V
Fault on Bar: 5, Percentage Variance $=10.88503$, Bar Reading: 0.1215511V, Reference: 0.136398 V
Fault on Bar: 7, Percentage Variance $=10.3879$, Bar Reading: 0.1505669 V , Reference: 0.136398 V
Fault on Bar: 8, Volt-Drop Reading Is Zero ( 0 V ), Indicating A Possible Short Circuit
Fault on Bar: 9, Volt-Drop Reading Is Out Of Range, Indicating A Possible Open Circuit
Emergency Stop on Bar 10
I, Sunveer Matadin acknowledge the above results and pledge to investigate and/or remedy the above recorded faults (if any).

Signature, Sunveer Matadin $\qquad$


| Print Displayed Data |
| :--- |
| Print |

-Open File


File Names


Refined Search - Dates


Exit Program

Display Data


## Directory Path

-Path Propeties
View Default Path

View Selected Path Change Default Path -Drive / Network Path
宝f:[Ntrac\cky370\$]
$\rightarrow$
-Folders
Ef: - backup 22.12.05
-IGBT
$\square$ Weakfield

Files
05SysArchDesign.pdf
DataloggerDraft Functional Description v0.doc LCMS Project Charter v3_chris Saniiv_Final_2 Specification for Logger_VerF3.doc

## Horml - 1

Dim DefaultPath As String
Dim Pswd As Integer
Dim PasswdFlag As Boolean
Dim Test_Date As String
Dim Save_Test As String
'Dim Savè Test As String

Private Sub Command Click()
Dim X As String
Dim $j$ As Boolean
Save Test = InputBox("Enter Job Number", "Enter The Job Number Of the Test You Wish To Open")
If Save Test <>" Then If Save Test <> "Find" Then If Dir (DefaultPath \& Save Test) <> "" Then List1.Clear Open DefaultPath \& Save Test For Input As \#5 Let $j=$ Falsé Do While Not EOF(5)

Input \#5, aa, bb, cc, dd, ee, ff If $j=$ Ealse Then List1.AddItem "Job Number: " \& aa Listl.AddItem "Operator's Name: " \& bb Listl. AddItem cc List1.AddItem dd List1.AddItem "Date: " \& LTrim(ee) List1.AddItem "" List1.AddItem "Recorded Faults " Listl.AddItem "" List1.AddItem ff Let $j=$ True

List1.AddItem ff
If aa $=$ "End" Then
Let $\mathrm{j}=$ False
Listi.AddItem ""
Listl.AddItem ""
GoTo Next Rec End If

## Next_Rec:

End If
Nex__rec:

## Loop

Close \#5
Else: MsgBox "The Requested Job Number Does Not Exist"
End If
Else
If Dir(DefaultPath \& "Saved List.TXT") <> "" Then Open DefaultPath \& "Saved_List.TXT" For Input As \#7 List2. Clear

Let Open Hold $=$ "" Do While Not EOF(7)
Input \#7, job
If Open Hold $<>$ job Then
List2.AddItem job Let Open_Hold $=$ job End If
Loop
If List2.ListCount $<>0$ Then
List2.Visible $=$ True
'Command33. Visible = True
Else
MsgBox "There Are No Tests To View"
End If
Close \#7
Else: MsgBox "There Are No Tests To View"
End If
End If
Else: MsgBox "Job Number Was Not Entered"
End If
nd Sub
rivate Sub Command2_Click()
swd $=$ Pswd - 1

## torms - 2

```
    If Textl.Text = "AutoSun6" Then
        Let PasswdFlag = True
        Textl.Text = ""
        Textl.Locked = True
        Commandl.Enabled = True
        Command2.Enabled = False
        Command4.Enabled = True
Else
    If Pswd > 0 Then
    MsgBox " Incorrect Password, Tries left: " & Pswd & ""
    Let TextI.Text = "'
    Else
    MsgBox " You DO NOT have the authority to use this equipment. You have been LOCKED OUT"
    Framel.Visible = True
    'Textlo.Visible = True
    Commandl8.Visible = True
    End If
    End If
    End Sub
```

    Private Sub Command3_Click()
    End
    End Sub
    Private Sub Command4 Click()
    If Listl.List(0) <> "" Then
        If Left(List1.List(0), 11) \(=\) "Job Number:" Then
        Let Deletex = Fopen
        Printer. NewPage
        Let Print Save_i \(=0\)
            Do While Print_Save_i \(<=\) (List1.ListCount - 1)
            Printer. Print Listl.List(Print_Save_i)
            Picturel. Print List1. List (Print Save_i)
            Print_Save_i \(=\) Print_Save_i +1
            Loop
        List1.AddItem "Test Print Complete"
        Printer.EndDoc
        End If
    Else
MsgBox "No Data Available To Print"
End If
End Sub
Private Sub Dir2_Change()
End Sub
Private Sub Command5_Click()
Let Text2.Text = ""
Text2. Text $=$ Dirl. Path
If Right (Dir1. Path, 1) <> " $\backslash$ " Then
Text2.Text $=$ Text 2. Text \& " $\backslash$ "
End If
End Sub
Private Sub Command 6 Click()
Let Text2.Text = ""
rext2.Text $=$ Dir1.Path
[f Right(Dirl. Path, 1) <> " $\backslash$ " Then
Text2.Text $=$ Text2. Text \& " $\backslash "$
ind If
f Text2.Text 《> " Then
If InputBox ("Enter Password", "Enter Administrator's Password") = "AdminAutoSun6" Then
If Dir("C:\Program Files \SavePath") <> "" Then
Open "C:\Program Eiles SavePath" For Input As \#1 ' to save the default path
Open "Temp" For Output As \#2
Write \#2, Text2. Text
Close \#2
Close \#1
Kill ("C:\Program Eiles SavePath")

## Horml - 3

```
Name "Temp" As "C:\Program Files\SavePath"
Open "C:\Program Files\SavePath" For Output As #1
Write #l, Text2.Text
Close #1
End If
```

    Let DefaultPath \(=\) Text 2 .Text
    Else
    MsgBox "You are NOT Authorised to perform this task"
    End If
    Else
    MsgBox "No Path Specified"
    End If
    End Sub
    Private Sub Command7 Click()
    If Dir("C: \Program Fíles SavePath") <> "" Then
        Open "C: \Program Files \SavePath" For Input As \#1
        Input \#1, DefaultPath ' holds the path to the saved files
        Let Text2.Text \(=\) DefaultPath
        Close \#1
    Else
        MsgBox "Default Path is Not Valid, it has been changed"
    End If
    End Sub
    Private Sub Dirl_Change()
    Let File1.Path \(=\)-Dir1. Path
    End Sub
    Private Sub Drive1_Change()
    Let Dirl.Path \(=\) Drivel. Drive
    End Sub
    Private Sub Form Load()
    Let Fswd = 3
    Let PasswdFlag = False
Let Commandl.Enabled $=$ False
Let Command4.Enabled $=$ False
Frame1.Visible $=$ False
If Dir("C:\Program Files \SavePath") <> "" Then
Open "C:\Program Files \SavePath" For Input As \#I
Input \#1, DefaultPath ' holds the path to the saved files
Close \#1
Else
MsgBox "Default Path is Not Valid, it has been changed"
'Let DefaultPath $=$ "xxx"
End If
End Sub
Private Sub List2 Click()
Let Save_Test $=$ Līst2.Text
List1.Clear
Let Dspl Date $=$ ""
List4.Clear
List4.AddItem "View All"
Open DefaultPath \& Save_Test For Input As \#5
Do While Not EOF (5)
Input \#5, $a \mathrm{a}, \mathrm{bb}, \mathrm{cc}, \mathrm{dd}$, ee, ff
If (Dspl Date <> ee) And (bb <> "xxx") Then
List 4 .AddItem LTrim(ee)
Let Dspl Date $=$ ee
End If
Loop
If List4.ListCount $=1$ Then
MsgBox "There are no items to View"
List4.Clear
Else
List4.Visible $=$ True
End If
lose \#5
nd Sub
Private Sub List4_Click()
List1.Clear
Let Test Date $=$ List4.Text
Call Fopensub
'List2.Visible = False
'List4.Visible $=$ False
'Command33.Visible $=$ False
End Sub
Public Sub FopenSub()
If Test Date $=$ "View All" Then
Open DefaultPath \& Save Test For Input As \#5
Let $j=$ False
Do While Not EOF(5)
Input \#5, $a a, b b, c c, d d, ~ e e, ~ f f$
If $j=$ False Then
List1.AddItem "Job Number: " \& aa
Listl.AddItem "Operator's Name: " \& bb
List1.AddItem co
List1.AddItem dd
List1.AddItem "Date: " \& LTrim(ee)
Listi.AddItem ""
Listi.AddItem "Recorded Faults "
Listi.AddItem ""
List1.AddItem ff
Let $j=$ True
Else
List1.AddItem ff
If aa = "End" Then
Let $j=$ False
Listl.AddItem ""
List1.AddItem ""
End If
End If
Loop
Close \#5
Else
Open DefaultPath \& Save_Test For Input As \#5
Let $j=$ False
Do While Not EOF(5)
Input \#5, aa, bb, cc, dd, ee, ff
If (Test Date $=\operatorname{LTrim}(e e))$ Then
If $j=$ False Then
List1.AddItem "Job Number: " \& aa
List1.AddItem "Operator's Name: " \& bb
Listi. AddItem cc
List1. AddItem dd
List1.AddItem "Date: " \& LTrim(ee)
List1.AddItem ""
List1.AddItem "Recorded Faults "
Listl.AddItem ""
List1. AddItem ff
Let $j=$ True
End If
Else
Listi. AddItem ff
If $a \mathrm{a}=$ "End" Then 'xxx (or End) signals end of a test and
all the fields for the next test has to be printed
Let $j=$ Ealse
List1.AddItem
List].AddItem ""
End If
End If
End If
LOOp
Close \#5
End If
'ad is the Job No field
bb is the Operators Name field
cc is the Armature Selection field
dd is the Percentange Variance field
'ff is the Recorded Faults field
End Sub

## Features

- Compatible with MCS ${ }^{\oplus}-51$ Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
- Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5 V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)


## Description

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the indus-try-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.
The AT89S51 provides the following standard features: 4 K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a fivevector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

## Pin Configurations

| PDIP |  |  |  |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| P1.0 | 1 | 40 | $\square \mathrm{VCC}$ |
| P1.1 | 2 | 39 | $\square \mathrm{P} 0.0$ (ADO) |
| P1.2 | 3 | 38 | $\square \mathrm{P} 0.1$ (AD1) |
| P1.3 | 4 | 37 | $\square \mathrm{P} 0.2$ (AD2) |
| P1.4 | 5 | 36 | $\square \mathrm{P} 0.3$ (AD3) |
| (MOSI) P1.5 $\square$ | 6 | 35 | $\square \mathrm{P} 0.4$ (AD4) |
| (MISO) P1.6 | 7 | 34 | $\square \mathrm{P} 0.5$ (AD5) |
| (SCK) P1.7 $\square$ | 8 | 33 | $\square \mathrm{P} 0.6$ (AD6) |
| RST $\square$ | 9 | 32 | $\square \mathrm{P} 0.7$ (AD7) |
| (RXD) P3.0 $\square$ | 10 | 31 | $\square \overline{\mathrm{EA}} / \mathrm{VPP}$ |
| (TXD) P3.1 $\square$ | 11 | 30 | $\square \mathrm{ALE} / \overline{\mathrm{PROG}}$ |
| (INT0) P3.2 $\square$ | 12 | 29 | $\square \overline{\text { PSEN }}$ |
| (INT1) P3.3 | 13 | 28 | $\square \mathrm{P} 2.7$ (A15) |
| (T0) P3.4 $\square$ | 14 | 27 | $\square \mathrm{P} 2.6$ (A14) |
| (T1) P3.5 | 15 | 26 | $\square \mathrm{P} 2.5$ (A13) |
| ( $\overline{\mathrm{WR}})$ P3.6 | 16 | 25 | $\square \mathrm{P} 2.4$ (A12) |
| ( $\overline{\mathrm{RD}}) \mathrm{P} 3.7 \square$ | 17 | 24 | $\square \mathrm{P} 2.3$ (A11) |
| XTAL2 | 18 | 23 | $\square \mathrm{P} 2.2$ (A10) |
| XTAL1 | 19 | 22 | $\square \mathrm{P} 2.1$ (A9) |
| GND | 20 | 21 | $\square \mathrm{P} 2.0$ (A8) |




| PDIP |  |  |  |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| RST - | 1 | 42 | $\square \mathrm{P} 1.7$ (SCK) |
| (RXD) P3.0 | 2 | 41 | $\square \mathrm{P} 1.6$ (MISO) |
| (TXD) P3.1 | 3 | 40 | $\square \mathrm{P} 1.5$ (MOSI) |
| (INTO) P3.2 | 4 | 39 | P1.4 |
| (INT1) P3.3 | 5 | 38 | P1.3 |
| (T0) P3.4 | 6 | 37 | $\square \mathrm{P} 1.2$ |
| (T1) P3.5 | 7 | 36 | $\square \mathrm{P} 1.1$ |
| ( $\overline{\mathrm{WR}}) \mathrm{P} 3.6$ | 8 | 35 | P1.0 |
| ( $\overline{\mathrm{RD}}) \mathrm{P} 3.7$ | 9 | 34 | $\checkmark$ VDD |
| XTAL2 | 10 | 33 | $\square$ PWRVDD |
| XTAL1 | 11 | 32 | $\square \mathrm{P} 0.0$ (ADO) |
| GND | 12 | 31 | $\square \mathrm{P} 0.1$ (AD1) |
| PWRGND | 13 | 30 | $\square \mathrm{P} 0.2$ (AD2) |
| (A8) P2.0 | 14 | 29 | P0.3 (AD3) |
| (A9) P2.1 | 15 | 28 | $\square \mathrm{P} 0.4$ (AD4) |
| (A10) P2.2 | 16 | 27 | P0.5 (AD5) |
| (A11) P2.3 | 17 | 26 | P0.6 (AD6) |
| (A12) P2.4 | 18 | 25 | P0.7 (AD7) |
| (A13) P2.5 | 19 | 24 | $\square \overline{E A} / \mathrm{VPP}$ |
| (A14) P2.6 | 20 | 23 | $\square \mathrm{ALE} / \overline{\mathrm{PROG}}$ |
| (A15) P2.7 | 21 | 22 | PSEN |

## Block Diagram



## Pin Description

VCC

GND

Supply voltage (all packages except 42-PDIP).

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board MUST connect both VDD and PWRVDD to the board supply voltage.

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board MUST connect both GND and PWRGND to the board ground.

Port 0 is an 8 -bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1 s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 is an 8 -bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1 s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ( $I_{L}$ ) because of the internal pull-ups.
Port 1 also receives the low-order address bytes during Flash programming and verification.

| Port Pin | Alternate Functions |
| :--- | :--- |
| P1.5 | MOSI (used for In-System Programming) |
| P1.6 | MISO (used for In-System Programming) |
| P1.7 | SCK (used for In-System Programming) |

Port 2 is an 8 -bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1 s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current $\left(l_{L}\right)$ because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

## Port 3

## ALE/PROG

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
External Access Enable. $\overline{\mathrm{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000 H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.
$\overline{E A}$ should be strapped to $\mathrm{V}_{\mathrm{CC}}$ for internal program executions.
This pin also receives the 12 -volt programming enable voltage ( $\mathrm{V}_{\mathrm{PP}}$ ) during Flash programming.

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

| 0F8H |  |  |  |  |  |  |  |  | 0FFH |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0FOH | $\begin{gathered} \text { B } \\ 00000000 \end{gathered}$ |  |  |  |  |  |  |  | 0F7H |
| 0E8H |  |  |  |  |  |  |  |  | 0EFH |
| OEOH | $\begin{gathered} \text { ACC } \\ 00000000 \end{gathered}$ |  |  |  |  |  |  |  | 0E7H |
| 0D8H |  |  |  |  |  |  |  |  | ODFH |
| 0DOH | $\begin{gathered} \text { PSW } \\ 00000000 \end{gathered}$ |  |  |  |  |  |  |  | 0D7H |
| 0 C 8 H |  |  |  |  |  |  |  |  | OCFH |
| OCOH |  |  |  |  |  |  |  |  | 0C7H |
| 0B8H | $\begin{gathered} \text { IP } \\ \times \times 000000 \end{gathered}$ |  |  |  |  |  |  |  | OBFH |
| 0B0H | $\begin{gathered} \text { P3 } \\ 11111111 \end{gathered}$ |  |  |  |  |  |  |  | 0B7H |
| 0A8H | $\begin{gathered} \text { IE } \\ 0 \times 000000 \end{gathered}$ |  |  |  |  |  |  |  | OAFH |
| OAOH | $\begin{gathered} \text { P2 } \\ 11111111 \end{gathered}$ |  | $\begin{gathered} \text { AUXR1 } \\ \text { XXXXXX0 } \end{gathered}$ |  |  |  | WDTRST XXXXXXXX |  | 0A7H |
| 98H | $\begin{gathered} \text { SCON } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { SBUF } \\ \text { XXXXXXXX } \end{gathered}$ |  |  |  |  |  |  | 9FH |
| 90H | $\begin{gathered} \text { P1 } \\ 11111111 \end{gathered}$ |  |  |  |  |  |  |  | 97H |
| 88H | $\begin{gathered} \text { TCON } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TMOD } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TLO } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TL1 } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TH0 } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TH1 } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { AUXR } \\ \text { XXX00XX0 } \end{gathered}$ |  | 8FH |
| 80H | $\begin{gathered} \text { P0 } \\ 11111111 \end{gathered}$ | $\begin{gathered} \text { SP } \\ 00000111 \end{gathered}$ | $\begin{gathered} \text { DPOL } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { DPOH } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { DP1L } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { DP1H } \\ 00000000 \end{gathered}$ |  | $\begin{gathered} \text { PCON } \\ 0 X X X 0000 \end{gathered}$ | 87H |

User software should not write 1 s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0 .

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register


Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16 -bit Data Pointer Registers are provided: DP0 at SFR address locations $82 \mathrm{H}-$ 83 H and DP1 at $84 \mathrm{H}-85 \mathrm{H}$. Bit DPS $=0$ in SFR AUXR1 selects DP0 and DPS $=1$ selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to " 1 " during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1


## Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64 K bytes each of external Program and Data Memory can be addressed.

If the $\overline{E A}$ pin is connected to GND, all program fetches are directed to external memory.
On the AT89S51, if $\overline{E A}$ is connected to $\mathrm{V}_{\mathrm{CC}}$, program fetches to addresses 0000 H through FFFH are directed to internal memory and fetches to addresses 1000 H through FFFFH are directed to external memory.

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location OA6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location OA6H). When the WDT is enabled, the user needs to service it by writing 01EH and OE1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $98 \times$ TOSC, where TOSC $=1 /$ FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

## UART

## Timer 0 and 1

## Interrupts

In Power-down mode the oscillator stops, which means the WDT also stops. While in Powerdown mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0 ) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.
With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe ${ }^{\circledR}$ Acrobat ${ }^{\circledR}$ file "AT89 Series Hardware Description".

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe Acrobat file "AT89 Series Hardware Description".

The AT89S51 has a total of five interrupt vectors: two external interrupts (INT0 and INT1), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.
Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.
Note that Table 4 shows that bit positions IE. 6 and IE. 5 are unimplemented. User software should not write 1 s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 4. Interrupt Enable (IE) Register
(MSB)

| EA | - | - | ES | ET1 | EX1 | ET0 | EX0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables the interrupt.

| Symbol | Position | Function |
| :--- | :--- | :--- |
| EA | IE. 7 | Disables all interrupts. If EA $=0$, no interrupt is <br> acknowledged. If EA $=1$, each interrupt source is <br> individually enabled or disabled by setting or clearing <br> its enable bit. |
| - | IE.6 | Reserved |
| - | IE. 5 | Reserved |
| ES | IE.4 | Serial Port interrupt enable bit |
| ET1 | IE.3 | Timer 1 interrupt enable bit |
| EX1 | IE. 2 | External interrupt 1 enable bit |
| ET0 | IE.0 | Timer 0 interrupt enable bit |
| EX0 | External interrupt 0 enable bit |  |
| User software should never write 1s to reserved bits, because they may be used in future AT89 <br> products. |  |  |

Figure 1. Interrupt Sources

$\mathrm{TFO} \longrightarrow$


TF1 $\longrightarrow$


## Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections


Note: $\quad \mathrm{C} 1, \mathrm{C} 2=30 \mathrm{pF} \pm 10 \mathrm{pF}$ for Crystals
$=40 \mathrm{pF} \pm 10 \mathrm{pF}$ for Ceramic Resonators
Figure 3. External Clock Drive Configuration


In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.
Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Powerdown is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt (INTO or INT1). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $\mathrm{V}_{\mathrm{CC}}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize. morn

## Power-down Mode

## Idle Mode

Table 5. Status of External Pins During Idle and Power-down Modes

| Mode | Program Memory | ALE | $\overline{\text { PSEN }}$ | PORT0 | PORT1 | PORT2 | PORT3 |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power-down | External | 0 | 0 | Float | Data | Data | Data |

## Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed $(P)$ to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

| Program Lock Bits |  |  |  | Protection Type |
| :---: | :---: | :---: | :---: | :---: |
|  | LB1 | LB2 | LB3 |  |
| 1 | U | U | U | No program lock features |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{\mathrm{EA}}$ is sampled and latched on reset, and further programming of the Flash memory is disabled |
| 3 | P | P | U | Same as mode 2, but verify is also disabled |
| 4 | P | P | P | Same as mode 3, but external execution is also disabled |

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of EA must agree with the current logic level at that pin in order for the device to function properly.

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.
Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 7) and Figures 4 and 5 . To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{E A} / V_{P P}$ to 12 V .
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The bytewrite cycle is self-timed and typically takes no more than $50 \mu \mathrm{~s}$. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.
 During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{\text { Data }}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/ $\overline{\operatorname{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations $000 \mathrm{H}, 100 \mathrm{H}$, and 200 H , except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.
$(000 \mathrm{H})=1 \mathrm{EH}$ indicates manufactured by Atmel
$(100 \mathrm{H})=51 \mathrm{H}$ indicates AT89S51
$(200 \mathrm{H})=06 \mathrm{H}$
Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/PROG low for a duration of 200 ns 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms .

During chip erase, a serial read from any address location will return 00 H at the data output.

> Programming the Flash Serial Mode

## Serial <br> Programming Algorithm

The Code memory array can be programmed using the serial ISP interface while RST is pulled to $\mathrm{V}_{\mathrm{cc}}$. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.
The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than $1 / 16$ of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz .

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

Apply power between VCC and GND pins.
Set RST pin to " H ".
If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5 V .
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):
Set XTAL1 to "L" (if a crystal is not used).
Set RST to "L".
Turn $\mathrm{V}_{\mathrm{Cc}}$ power off.
Data Polling: The $\overline{\text { Data }}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

## Serial <br> Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8.

## Programming Interface Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

| Mode | $\mathrm{V}_{\mathrm{cc}}$ | RST | PSEN | $\frac{\text { ALE/ }}{\text { PROG }}$ | $\begin{aligned} & \overline{E A} / \\ & \mathrm{V}_{\mathrm{PP}} \end{aligned}$ | P2.6 | P2.7 | P3.3 | P3.6 | P3.7 | $\begin{aligned} & \text { P0.7-0 } \\ & \text { Data } \end{aligned}$ | P2.3-0 | P1.7-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  | Address |  |
| Write Code Data | 5 V | H | L | $\sim^{(2)}$ | 12 V | L | H | H | H | H | $\mathrm{D}_{\text {IN }}$ | A11-8 | A7-0 |
| Read Code Data | 5V | H | L | H | H | L | L | L | H | H | $\mathrm{D}_{\text {OUt }}$ | A11-8 | A7-0 |
| Write Lock Bit 1 | 5 V | H | L | $\sim^{(3)}$ | 12 V | H | H | H | H | H | X | X | X |
| Write Lock Bit 2 | 5 V | H | L | $\sim^{(3)}$ | 12 V | H | H | H | L | L | X | X | X |
| Write Lock Bit 3 | 5 V | H | L | $\sim^{(3)}$ | 12 V | H | L | H | H | L | X | X | X |
| Read Lock Bits $1,2,3$ | 5 V | H | L | H | H | H | H | L | H | L | $\begin{aligned} & \text { P0.2, } \\ & \text { P0.3, } \\ & \text { P0. } \end{aligned}$ | X | X |
| Chip Erase | 5 V | H | L | $\sim{ }^{(1)}$ | 12 V | H | L | H | L | L | X | X | X |
| Read Atmel ID | 5 V | H | L | H | H | L | L | L | L | L | 1 EH | 0000 | 00H |
| Read Device ID | 5 V | H | L | H | H | L | L | L | L | L | 51H | 0001 | OOH |
| Read Device ID | 5 V | H | L | H | H | L | L | L | L | L | 06H | 0010 | OOH |

Notes: 1. Each PROG pulse is $200 \mathrm{~ns}-500 \mathrm{~ns}$ for Chip Erase.
2. Each $\overline{\text { PROG }}$ pulse is $200 \mathrm{~ns}-500 \mathrm{~ns}$ for Write Code Data.
3. Each PROG pulse is $200 \mathrm{~ns}-500 \mathrm{~ns}$ for Write Lock Bits.
4. RDY/ $\overline{\mathrm{BSY}}$ signal is output on P3.0 during programming.
5. $\mathrm{X}=$ don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)


Figure 5. Verifying the Flash Memory (Parallel Mode)


Flash Programming and Verification Characteristics (Parallel Mode)
$\mathrm{T}_{\mathrm{A}}=20^{\circ} \mathrm{C}$ to $30^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=4.5$ to 5.5 V

| Symbol | Parameter | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {PP }}$ | Programming Supply Voltage | 11.5 | 12.5 | V |
| $\mathrm{I}_{\mathrm{PP}}$ | Programming Supply Current |  | 10 | mA |
| $\mathrm{I}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}$ Supply Current |  | 30 | mA |
| 1/t ${ }_{\text {CLCL }}$ | Oscillator Frequency | 3 | 33 | MHz |
| $t_{\text {AVGL }}$ | Address Setup to $\overline{\text { PROG Low }}$ | $48 \mathrm{t}_{\text {CLCL }}$ |  |  |
| $\mathrm{t}_{\text {GHAX }}$ | Address Hold After PROG | $48 \mathrm{t}_{\mathrm{CLCL}}$ |  |  |
| $\mathrm{t}_{\text {DVGL }}$ | Data Setup to $\overline{\text { PROG }}$ Low | $48 \mathrm{t}_{\text {CLCL }}$ |  |  |
| $\mathrm{t}_{\text {GHDX }}$ | Data Hold After $\overline{\text { PROG }}$ | $48 \mathrm{t}_{\text {CLCL }}$ |  |  |
| $\mathrm{t}_{\text {EHSH }}$ | P2.7 ( $\overline{\text { ENABLE }}$ ) High to $\mathrm{V}_{\mathrm{PP}}$ | $48 \mathrm{t}_{\mathrm{CLCL}}$ |  |  |
| $\mathrm{t}_{\text {SHGL }}$ | $\mathrm{V}_{\text {PP }}$ Setup to $\overline{\text { PROG }}$ Low | 10 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {GHSL }}$ | $V_{\text {PP }}$ Hold After $\overline{\text { PROG }}$ | 10 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {GLGH }}$ | $\overline{\text { PROG Width }}$ | 0.2 | 1 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {AVQV }}$ | Address to Data Valid |  | $48 \mathrm{t}_{\text {CLCL }}$ |  |
| $t_{\text {ELQV }}$ | ENABLE Low to Data Valid |  | $48 \mathrm{t}_{\text {CLCL }}$ |  |
| $\mathrm{t}_{\text {EHQZ }}$ | Data Float After ENABLE | 0 | $48 \mathrm{t}_{\text {CLCL }}$ |  |
| $\mathrm{t}_{\text {GHBL }}$ | $\overline{\text { PROG }}$ High to $\overline{\text { BUSY }}$ Low |  | 1.0 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {wc }}$ | Byte Write Cycle Time |  | 50 | $\mu \mathrm{s}$ |

Figure 6. Flash Programming and Verification Waveforms - Parallel Mode


Figure 7. Flash Memory Serial Downloading


## Flash Programming and Verification Waveforms - Serial Mode

Figure 8. Serial Programming Waveforms


Table 8. Serial Programming Instruction Set

| Instruction | Instruction <br> Format |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
|  | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Operation |

Note: 1. B1 $=0, \mathrm{~B} 2=0 \rightarrow$ Mode 1, no lock protection $\mathrm{B} 1=0, \mathrm{~B} 2=1 \rightarrow$ Mode 2, lock bit 1 activated $B 1=1, B 2=0 \rightarrow$ Mode 3, lock bit 2 activated $B 1=1, B 2=1 \rightarrow$ Mode 4, lock bit 3 activated

Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than $1 / 16$ of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255 . After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

## Serial Programming Characteristics

Figure 9. Serial Programming Timing


Table 9. Serial Programming Characteristics, $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=4.0-5.5 \mathrm{~V}$ (Unless Otherwise Noted)

| Symbol | Parameter | Min | Typ | Max | Units |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $1 / t_{\text {CLCL }}$ | Oscillator Frequency | 3 |  | 33 | MHz |
| $\mathrm{t}_{\mathrm{CLCL}}$ | Oscillator Period | 30 |  |  | ns |
| $\mathrm{t}_{\text {SHSL }}$ | SCK Pulse Width High | $8 \mathrm{t}_{\mathrm{CLCL}}$ |  |  | ns |
| $\mathrm{t}_{\mathrm{SLSH}}$ | SCK Pulse Width Low | $8 \mathrm{t}_{\mathrm{CLCL}}$ |  | ns |  |
| $\mathrm{t}_{\mathrm{OVSH}}$ | MOSI Setup to SCK High | $\mathrm{t}_{\mathrm{CLCL}}$ |  |  | ns |
| $\mathrm{t}_{\text {SHOX }}$ | MOSI Hold after SCK High | $2 \mathrm{t}_{\mathrm{CLCL}}$ |  |  | ns |
| $\mathrm{t}_{\text {SLIV }}$ | SCK Low to MISO Valid | 10 |  | 16 | 32 |
| $\mathrm{t}_{\text {ERASE }}$ | Chip Erase Instruction Cycle Time |  |  | 500 | ns |
| $\mathrm{t}_{\text {SWC }}$ | Serial Byte Write Cycle Time |  |  | $64 \mathrm{t}_{\mathrm{CLCL}}+400$ | $\mu \mathrm{~s}$ |

## Absolute Maximum Ratings*

| Operating Temperature ............................... $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :--- |
| Storage Temperature ................................ $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Voltage on Any Pin |
| with Respect to Ground .................................. -1.0 V to +7.0 V |
| Maximum Operating Voltage ........................................... 6.6 V |
| DC Output Current...................................................... 15.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

The values shown in this table are valid for $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}$ to 5.5 V , unless otherwise noted.

| Symbol | Parameter | Condition | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Input Low Voltage | (Except EA) | -0.5 | $0.2 \mathrm{~V}_{\mathrm{CC}}-0.1$ | V |
| $\mathrm{V}_{\text {IL1 }}$ | Input Low Voltage ( $\overline{\mathrm{EA}}$ ) |  | -0.5 | $0.2 \mathrm{~V}_{\mathrm{CC}}-0.3$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input High Voltage | (Except XTAL1, RST) | $0.2 \mathrm{~V}_{\mathrm{CC}}+0.9$ | $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{V}_{\mathrm{IH} 1}$ | Input High Voltage | (XTAL1, RST) | $0.7 \mathrm{~V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Output Low Voltage ${ }^{(1)}$ (Ports 1,2,3) | $\mathrm{I}_{\mathrm{OL}}=1.6 \mathrm{~mA}$ |  | 0.45 | V |
| $\mathrm{V}_{\text {OL1 }}$ | Output Low Voltage ${ }^{(1)}$ (Port 0, ALE, PSEN) | $\mathrm{I}_{\mathrm{OL}}=3.2 \mathrm{~mA}$ |  | 0.45 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage <br> (Ports 1,2,3, ALE, PSEN) | $\mathrm{I}_{\mathrm{OH}}=-60 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%$ | 2.4 |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-25 \mu \mathrm{~A}$ | $0.75 \mathrm{~V}_{\mathrm{Cc}}$ |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-10 \mu \mathrm{~A}$ | $0.9 \mathrm{~V}_{\mathrm{CC}}$ |  | V |
| $\mathrm{V}_{\mathrm{OH} 1}$ | Output High Voltage <br> (Port 0 in External Bus Mode) | $\mathrm{I}_{\mathrm{OH}}=-800 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%$ | 2.4 |  | V |
|  |  | $\mathrm{I}_{\text {OH }}=-300 \mu \mathrm{~A}$ | $0.75 \mathrm{~V}_{\mathrm{CC}}$ |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-80 \mu \mathrm{~A}$ | $0.9 \mathrm{~V}_{\mathrm{CC}}$ |  | V |
| $\mathrm{I}_{\text {IL }}$ | Logical 0 Input Current (Ports 1,2,3) | $\mathrm{V}_{\mathrm{IN}}=0.45 \mathrm{~V}$ |  | -50 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{TL}}$ | Logical 1 to 0 Transition Current (Ports 1,2,3) | $\mathrm{V}_{\text {IN }}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%$ |  | -650 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{LI}}$ | Input Leakage Current (Port 0, $\overline{\mathrm{EA}}$ ) | $0.45<\mathrm{V}_{\text {IN }}<\mathrm{V}_{\mathrm{CC}}$ |  | $\pm 10$ | $\mu \mathrm{A}$ |
| RRST | Reset Pulldown Resistor |  | 50 | 300 | $\mathrm{K} \Omega$ |
| $\mathrm{C}_{10}$ | Pin Capacitance | Test Freq. $=1 \mathrm{MHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 10 | pF |
| $\mathrm{I}_{\mathrm{CC}}$ | Power Supply Current | Active Mode, 12 MHz |  | 25 | mA |
|  |  | Idle Mode, 12 MHz |  | 6.5 | mA |
|  | Power-down Mode ${ }^{(2)}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ |  | 50 | $\mu \mathrm{A}$ |

Notes: 1. Under steady state (non-transient) conditions, $\mathrm{I}_{\mathrm{OL}}$ must be externally limited as follows:
Maximum Iol per port pin: 10 mA
Maximum I $\mathrm{I}_{\mathrm{OL}}$ per 8-bit port:
Port 0: $26 \mathrm{~mA} \quad$ Ports 1, 2, 3: 15 mA
Maximum total $\mathrm{I}_{\mathrm{OL}}$ for all output pins: 71 mA
If $\mathrm{I}_{\mathrm{OL}}$ exceeds the test condition, $\mathrm{V}_{\mathrm{OL}}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum $\mathrm{V}_{\mathrm{CC}}$ for Power-down is 2 V .

## AC Characteristics

Under operating conditions, load capacitance for Port $0, A L E / \overline{\text { PROG }}$, and $\overline{\text { PSEN }}=100 \mathrm{pF}$; load capacitance for all other outputs $=80 \mathrm{pF}$.

## External Program and Data Memory Characteristics

| Symbol | Parameter | 12 MHz Oscillator |  | Variable Oscillator |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max |  |
| 1/t ${ }_{\text {CLCL }}$ | Oscillator Frequency |  |  | 0 | 33 | MHz |
| $t_{\text {LHLL }}$ | ALE Pulse Width | 127 |  | $2 \mathrm{t}_{\mathrm{CLCL}}-40$ |  | ns |
| $t_{\text {AVLL }}$ | Address Valid to ALE Low | 43 |  | $\mathrm{t}_{\text {CLCL- }}-25$ |  | ns |
| $\mathrm{t}_{\text {LLAX }}$ | Address Hold After ALE Low | 48 |  | $\mathrm{t}_{\text {CLCL- }} 25$ |  | ns |
| $\mathrm{t}_{\text {LLIV }}$ | ALE Low to Valid Instruction In |  | 233 |  | $4 t_{\text {CLCL }}-65$ | ns |
| tLLPL | ALE Low to $\overline{\text { PSEN }}$ Low | 43 |  | $\mathrm{t}_{\text {CLCL- }}-25$ |  | ns |
| $t_{\text {PLPH }}$ | $\overline{\text { PSEN Pulse Width }}$ | 205 |  | $3 \mathrm{t}_{\mathrm{CLCL}}-45$ |  | ns |
| $\mathrm{t}_{\text {PLIV }}$ | $\overline{\text { PSEN Low to Valid Instruction In }}$ |  | 145 |  | $3 \mathrm{t}_{\text {CLCL- }}-60$ | ns |
| $\mathrm{t}_{\text {PXIX }}$ | Input Instruction Hold After $\overline{\text { PSEN }}$ | 0 |  | 0 |  | ns |
| $\mathrm{t}_{\text {PXIZ }}$ | Input Instruction Float After $\overline{\text { PSEN }}$ |  | 59 |  | $\mathrm{t}_{\mathrm{CLCL}}-25$ | ns |
| $\mathrm{t}_{\text {PXAV }}$ | $\overline{\text { PSEN }}$ to Address Valid | 75 |  | $\mathrm{t}_{\mathrm{CLCL}}{ }^{-8}$ |  | ns |
| $\mathrm{t}_{\text {AVIV }}$ | Address to Valid Instruction In |  | 312 |  | $5 \mathrm{t}_{\mathrm{CLCL}}-80$ | ns |
| $t_{\text {PLAZ }}$ | $\overline{\text { PSEN Low to Address Float }}$ |  | 10 |  | 10 | ns |
| $\mathrm{t}_{\text {RLRH }}$ | $\overline{\mathrm{RD}}$ Pulse Width | 400 |  | $6 \mathrm{t}_{\mathrm{CLCL}}-100$ |  | ns |
| $t_{\text {WLWH }}$ | $\overline{\text { WR Pulse Width }}$ | 400 |  | $6 \mathrm{t}_{\text {CLCLL }}{ }^{-100}$ |  | ns |
| $\mathrm{t}_{\text {RLDV }}$ | $\overline{\mathrm{RD}}$ Low to Valid Data In |  | 252 |  | $5 \mathrm{t}_{\text {CLCL }}-90$ | ns |
| $\mathrm{t}_{\text {RHDX }}$ | Data Hold After $\overline{\mathrm{RD}}$ | 0 |  | 0 |  | ns |
| $\mathrm{t}_{\text {RHDZ }}$ | Data Float After $\overline{\mathrm{RD}}$ |  | 97 |  | $2 \mathrm{t}_{\mathrm{CLCL}}-28$ | ns |
| tLLDV | ALE Low to Valid Data In |  | 517 |  | $8 \mathrm{t}_{\mathrm{CLCL}}-150$ | ns |
| $\mathrm{t}_{\text {AVDV }}$ | Address to Valid Data In |  | 585 |  | $9 \mathrm{t}_{\text {CLCL }}-165$ | ns |
| $\mathrm{t}_{\text {LLWL }}$ | ALE Low to $\overline{\mathrm{RD}}$ or $\overline{\mathrm{WR}}$ Low | 200 | 300 | $3 \mathrm{t}_{\mathrm{CLCL}}-50$ | $3 \mathrm{t}_{\mathrm{CLCL}}+50$ | ns |
| $t_{\text {AVWL }}$ | Address to $\overline{\mathrm{RD}}$ or WR Low | 203 |  | $4 \mathrm{t}_{\text {CLCLL }}-75$ |  | ns |
| $\mathrm{t}_{\text {QVwX }}$ | Data Valid to $\overline{\mathrm{WR}}$ Transition | 23 |  | $\mathrm{t}_{\text {CLCL }}$-30 |  | ns |
| $\mathrm{t}_{\text {QVWH }}$ | Data Valid to $\overline{W R}$ High | 433 |  | $7 \mathrm{t}_{\text {CLCL }}-130$ |  | ns |
| $\mathrm{t}_{\text {WHQX }}$ | Data Hold After $\overline{W R}$ | 33 |  | $\mathrm{t}_{\text {CLCL- }}$-25 |  | ns |
| $\mathrm{t}_{\text {RLAZ }}$ | $\overline{\mathrm{RD}}$ Low to Address Float |  | 0 |  | 0 | ns |
| $\mathrm{t}_{\text {WHLH }}$ | $\overline{\mathrm{RD}}$ or $\overline{\mathrm{WR}}$ High to ALE High | 43 | 123 | $\mathrm{t}_{\mathrm{CLCL}}-25$ | $\mathrm{t}_{\mathrm{CLCL}}+25$ | ns |

## External Program Memory Read Cycle



## External Data Memory Read Cycle



## External Data Memory Write Cycle



## External Clock Drive Waveforms



## External Clock Drive

| Symbol | Parameter | Min | Max | Units |
| :--- | :--- | :---: | :---: | :---: |
| $1 / t_{\text {CLCL }}$ | Oscillator Frequency | 0 | 33 | MHz |
| $\mathrm{t}_{\mathrm{CLCL}}$ | Clock Period | 30 |  | ns |
| $\mathrm{t}_{\mathrm{CHCX}}$ | High Time | 12 |  | ns |
| $\mathrm{t}_{\mathrm{CLCX}}$ | Low Time | 12 |  | ns |
| $\mathrm{t}_{\mathrm{CLCH}}$ | Rise Time |  | 5 | ns |
| $\mathrm{t}_{\mathrm{CHCL}}$ | Fall Time | 5 | ns |  |

## Serial Port Timing: Shift Register Mode Test Conditions

The values in this table are valid for $\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}$ to 5.5 V and Load Capacitance $=80 \mathrm{pF}$.

| Symbol | Parameter | 12 MHz Osc |  | Variable Oscillator |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max |  |
| $\mathrm{t}_{\text {XLXL }}$ | Serial Port Clock Cycle Time | 1.0 |  | $12 \mathrm{t}_{\text {CLCL }}$ |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {QVXH }}$ | Output Data Setup to Clock Rising Edge | 700 |  | $10 \mathrm{CLLCL}^{-133}$ |  | ns |
| $\mathrm{t}_{\mathrm{XHQX}}$ | Output Data Hold After Clock Rising Edge | 50 |  | $2 \mathrm{t}_{\text {CLCL }}-80$ |  | ns |
| $\mathrm{t}_{\text {XHDX }}$ | Input Data Hold After Clock Rising Edge | 0 |  | 0 |  | ns |
| $\mathrm{t}_{\text {XHDV }}$ | Clock Rising Edge to Input Data Valid |  | 700 |  | $10 \mathrm{t}_{\text {CLCL }}-133$ | ns |

## Shift Register Mode Timing Waveforms



## AC Testing Input/Output Waveforms ${ }^{(1)}$



Note: 1. AC Inputs during testing are driven at $\mathrm{V}_{\mathrm{CC}}-0.5 \mathrm{~V}$ for a logic 1 and 0.45 V for a logic 0 . Timing measurements are made at $\mathrm{V}_{\mathrm{IH}}$ min . for a logic 1 and $\mathrm{V}_{\mathrm{IL}}$ max. for a logic 0 .

## Float Waveforms ${ }^{(1)}$



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded $\mathrm{V}_{\mathrm{OH}} / \mathrm{V}_{\mathrm{OL}}$ level occurs.

## Ordering Information

| Speed <br> (MHz) | Power Supply | Ordering Code | Package | Operation Range |
| :---: | :---: | :---: | :---: | :---: |
| 24 | 4.0 V to 5.5V | $\begin{aligned} & \text { AT89S51-24AC } \\ & \text { AT89S51-24JC } \\ & \text { AT89S51-24PC } \\ & \text { AT89S51-24SC } \end{aligned}$ | $\begin{aligned} & \hline 44 \mathrm{~A} \\ & 44 \mathrm{~J} \\ & 40 \mathrm{P} 6 \\ & 42 \mathrm{PS} 6 \end{aligned}$ | $\begin{aligned} & \text { Commercial } \\ & \left(0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C}\right) \end{aligned}$ |
|  |  | AT89S51-24AI <br> AT89S51-24JI <br> AT89S51-24PI <br> AT89S51-24SI | 44A <br> 44J <br> 40P6 <br> 42PS6 | $\begin{gathered} \text { Industrial } \\ \left(-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right) \end{gathered}$ |
| 33 | 4.5 V to 5.5 V | AT89S51-33AC <br> AT89S51-33JC <br> AT89S51-33PC <br> AT89S51-33SC | $\begin{aligned} & \hline 44 \mathrm{~A} \\ & 44 \mathrm{~J} \\ & 40 \mathrm{P} 6 \\ & 42 \mathrm{PS} 6 \end{aligned}$ | Commercial $\left(0^{\circ} \mathrm{C}\right.$ to $70^{\circ} \mathrm{C}$ ) |


| Package Type |  |
| :--- | :--- |
| 44A | 44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP) |
| 44J | 44-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 40P6 | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 42PS6 | 42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |

## Packaging Information

## 44A - TQFP



## 44J - PLCC



Notes: 1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion.

Allowable protrusion is $.010 "(0.254 \mathrm{~mm})$ per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is $0.004^{\prime \prime}(0.102 \mathrm{~mm})$ maximum.

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
DRAWING NO. REV.

40P6 - PDIP



Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure $=\mathrm{mm}$ )

| SYMBOL | MIN | NOM | MAX | NOTE |
| :---: | :---: | :---: | :---: | :---: |
| A | - | - | 4.83 |  |
| A1 | 0.51 | - | - |  |
| D | 36.70 | - | 36.96 | Note 2 |
| E | 15.24 | - | 15.88 |  |
| E1 | 13.46 | - | 13.97 | Note 2 |
| B | 0.38 | - | 0.56 |  |
| B1 | 0.76 | - | 1.27 |  |
| L | 3.05 | - | 3.43 |  |
| C | 0.20 | - | 0.30 |  |
| eB | - | - | 18.55 |  |
| e | 1.78 TYP |  |  |  |

## Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

## Regional Headquarters

Europe<br>Atmel Sarl<br>Route des Arsenaux 41<br>Case Postale 80<br>CH-1705 Fribourg<br>Switzerland<br>Tel: (41) 26-426-5555<br>Fax: (41) 26-426-5500<br>Asia<br>Room 1219<br>Chinachem Golden Plaza<br>77 Mody Road Tsimshatsui<br>East Kowloon<br>Hong Kong<br>Tel: (852) 2721-9778<br>Fax: (852) 2722-1369<br>Japan<br>9F, Tonetsu Shinkawa Bldg.<br>1-24-8 Shinkawa<br>Chuo-ku, Tokyo 104-0033<br>Japan<br>Tel: (81) 3-3523-3551<br>Fax: (81) 3-3523-7581

## Atmel Operations

Memory<br>2325 Orchard Parkway<br>San Jose, CA 95131, USA<br>Tel: 1(408) 441-0311<br>Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60
ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759
Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G750QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

## RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

## Biometrics/Imaging/Hi-Rel MPU/

High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Operating Free Air Temperature Range
DM54LS and 54LS
DM74LS
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS00 |  |  | DM74LS00 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\text {CC }}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {l }}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{lOL}^{\text {l }}$ | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & V_{C C}=M a x \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 0.8 | 1.6 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 2.4 | 4.4 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 3 | 10 | 4 | 15 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 10 | 4 | 15 | ns |
| Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$. |  |  |  |  |  |  |





Physical Dimensions inches (millimeters) (Continued)


14-Lead Ceramic Flat Package (W) Order Number 54LS00FMQB or DM54LS00W NS Package Number W14B

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| :---: | :---: | :---: | :---: |

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\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{FRIRPHILD} \& \& \multicolumn{2}{|r|}{May 1986} \\
\hline \multicolumn{6}{|l|}{SEMICONDபСTロRTM} \\
\hline \multicolumn{6}{|l|}{DM74LS02} \\
\hline \multicolumn{6}{|l|}{Quad 2-Input NOR Gate} \\
\hline \multicolumn{6}{|l|}{General Description} \\
\hline \multicolumn{6}{|l|}{This device contains four independent gates each of which performs the logic NOR function.} \\
\hline \multicolumn{6}{|l|}{Ordering Code:} \\
\hline Order Number \& Package Number \& \multicolumn{4}{|c|}{Package Description} \\
\hline DM74LS02M \& M14A \& \multicolumn{4}{|l|}{14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow} \\
\hline DM74LS02SJ \& M14D \& \multicolumn{4}{|l|}{14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide} \\
\hline DM74LS02N \& N14A \& \multicolumn{4}{|l|}{14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide} \\
\hline \begin{tabular}{l}
Devices also available \\
Connectio
\end{tabular} \& \begin{tabular}{l}
in Tape and Reel. Specify \\
n Diagram
\end{tabular} \& by appending the suffix \&  \& ¢

B
L
H
L

H \& | Output |
| :---: |
| $\mathbf{Y}$ |
| H |
| L |
| L |
| L | <br>

\hline
\end{tabular}

Absolute Maximum Ratings(Note 1)

| Supply Voltage | 7 V |
| :--- | ---: |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note 1: The "Absolute Maximum Ratings" are those values beyond which he safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrica Characteristics tables are not guaranteed at the absolute maximum ratings The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.75 | 5 | 5.25 | V |
| $\mathrm{~V}_{\mathrm{IH}}$ | HIGH Level Input Voltage | 2 |  |  | V |
| $\mathrm{~V}_{\mathrm{IL}}$ | LOW Level Input Voltage |  |  | 0.8 | V |
| $\mathrm{I}_{\mathrm{OH}}$ | HIGH Level Output Current |  |  | -0.4 | mA |
| $\mathrm{I}_{\mathrm{OL}}$ | LOW Level Output Current |  |  | 8 | mA |
| $\mathrm{~T}_{\mathrm{A}}$ | Free Air Operating Temperature | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics

| Symbol | Parameter | Conditions | Min |  | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | 2.7 | 3.4 |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ |  | 0.35 | 0.5 | V |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  | 0.1 | mA |
| IIH | HIGH Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | LOW Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.40 | mA |
| l OS | Short Circuit Output Current | $\mathrm{V}_{\text {CC }}=\operatorname{Max}$ (Note 3) | -20 |  | -100 | mA |
| ${ }^{\text {CCH }}$ | Supply Current with Outputs HIGH | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  | 1.6 | 3.2 | mA |
| $\mathrm{I}_{\mathrm{CCL}}$ | Supply Current with Outputs LOW | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  | 2.8 | 5.4 | mA |

Note 2: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics

at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=\mathbf{2} \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $\mathrm{t}_{\text {PLH }}$ | Propagation Delay Time LOW-to-HIGH Level Output |  | 13 |  | 18 | ns |
| $\overline{t_{\text {PHL }}}$ | Propagation Delay Time HIGH-to-LOW Level Output |  | 10 |  | 15 | ns |

Physical Dimensions inches (millimeters) unless otherwise noted



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
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## - Dependable Texas Instruments Quality and Reliability <br> description

These devices contain six independent inverters.

SN5404 . . J J PACKAGE
SN54LS04, SN54S04 . . J OR W PACKAGE SN7404 . . D, N, OR NS PACKAGE SN74LS04... D, DB, N, OR NS PACKAGE SN74S04...D OR N PACKAGE (TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE (TOP VIEW)


NC - No internal connection

ORDERING INFORMATION

| $\mathrm{T}_{\mathbf{A}}$ | PACKAGE $\dagger$ |  | ORDERABLE <br> PART NUMBER | TOP-SIDE MARKING |
| :---: | :---: | :---: | :---: | :---: |
| $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | PDIP - N | Tube | SN7404N | SN7404N |
|  |  | Tube | SN74LS04N | SN74LS04N |
|  |  | Tube | SN74S04N | SN74S04N |
|  | SOIC - D | Tube | SN7404D | 7404 |
|  |  | Tube | SN74LS04D | LS04 |
|  |  | Tape and reel | SN74LS04DR |  |
|  |  | Tube | SN74S04D | S04 |
|  |  | Tape and reel | SN74S04DR |  |
|  | SOP - NS | Tape and reel | SN7404NSR | SN7404 |
|  |  | Tape and reel | SN74LS04NSR | 74LS04 |
|  | SSOP - DB | Tape and reel | SN74LS04DBR | LS04 |
| $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | CDIP - J | Tube | SN5404J | SN5404J |
|  |  | Tube | SNJ5404J | SNJ5404J |
|  |  | Tube | SN54LS04J | SN54LS04J |
|  |  | Tube | SN54S04J | SN54S04J |
|  |  | Tube | SNJ54LS04J | SNJ54LS04J |
|  |  | Tube | SNJ54S04J | SNJ54S04J |
|  | CFP - W | Tube | SNJ5404W | SNJ5404W |
|  |  | Tube | SNJ54LS04W | SNJ54LS04W |
|  |  | Tube | SNJ54S04W | SNJ54S04W |
|  | LCCC - FK | Tube | SNJ54LS04FK | SNJ54LS04FK |
|  |  | Tube | SNJ54S04FK | SNJ54S04FK |

$\dagger$ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)

| INPUT <br> $\mathbf{A}$ | OUTPUT <br> $\mathbf{Y}$ |
| :---: | :---: |
| $H$ | $L$ |
| $L$ | $H$ |

logic diagram (positive logic)


INSTRUMENTS
schematics (each gate)


Resistor values shown are nominal.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $\dagger$

```
Supply voltage, VCC (see Note 1)
                                7V
Input voltage, 採: '04, 'S04 ...................................................................... 5.5 V
    'LS04 ............................................................................................
```



```
    DB package .......................................96
    N package ............................................. 800}\textrm{C}/\textrm{W
    NS package .....................................76
Storage temperature range, T}\mp@subsup{T}{\mathrm{ stg}}{
    -65*}\textrm{C}\mathrm{ to }15\mp@subsup{0}{}{\circ}\textrm{C
\(\dagger\) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
```

recommended operating conditions

|  |  | SN5404 |  |  | SN7404 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  | 0.8 |  |  | 0.8 | V |
| ${ }^{\text {I OH }}$ | High-level output current |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{I}^{\text {I }}$ | Low-level output current |  |  | 16 |  |  | 16 | mA |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS $\ddagger$ |  |  | SN5404 |  |  | SN7404 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MIN | TYP§ | MAX | MIN | TYP§ | MAX |  |
| $\mathrm{V}_{\text {IK }}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{I}=-12 \mathrm{~mA}$ |  |  |  | -1.5 |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{V}_{\text {IL }}=0.8 \mathrm{~V}$, | $\mathrm{I} \mathrm{OH}=-0.4 \mathrm{~mA}$ | 2.4 | 3.4 |  | 2.4 | 3.4 |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}$, | $\mathrm{IOL}=16 \mathrm{~mA}$ |  | 0.2 | 0.4 |  | 0.2 | 0.4 | V |
| 1 | $V_{C C}=$ MAX, | $\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ |  |  |  | 1 |  |  | 1 | mA |
| IIH | $V_{C C}=$ MAX, | $\mathrm{V}_{\mathrm{I}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |  | 40 | $\mu \mathrm{A}$ |
| ILL | $V_{C C}=$ MAX, | $\mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ |  |  |  | -1.6 |  |  | -1.6 | mA |
| Ios ${ }^{1}$ | $V_{C C}=$ MAX |  |  | -20 |  | -55 | -18 |  | -55 | mA |
| ICCH | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$, | $\mathrm{V}_{\mathrm{I}}=0 \mathrm{~V}$ |  |  | 6 | 12 |  | 6 | 12 | mA |
| $\mathrm{I}_{\mathrm{CCL}}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$, | $\mathrm{V}_{\mathrm{I}}=4.5 \mathrm{~V}$ |  |  | 18 | 33 |  | 18 | 33 | mA |

$\ddagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
I Not more than one output should be shorted at a time.
switching characteristics, $\mathrm{V}_{\mathbf{C C}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$ (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS |  | $\begin{aligned} & \hline \text { SN5404 } \\ & \text { SN7404 } \end{aligned}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | MIN | TYP | MAX |  |
| tPLH | A | Y | $\mathrm{R}_{\mathrm{L}}=400 \Omega$, | $C_{L}=15 \mathrm{pF}$ |  | 12 | 22 | ns |
| tPHL |  |  |  |  |  | 8 | 15 |  |

SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS
SDLS029B - DECEMBER 1983 - REVISED FEBRUARY 2002
recommended operating conditions

|  |  | SN54LS04 |  |  | SN74LS04 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {I }}$ | High-level output current |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{I}_{\mathrm{OL}}$ | Low-level output current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS $\dagger$ |  |  | SN54LS04 |  |  | SN74LS04 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MIN | TYP\# | MAX | MIN | TYPキ | MAX |  |
| $\mathrm{V}_{\mathrm{IK}}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{I}=-18 \mathrm{~mA}$ |  |  |  | -1.5 |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{V}_{\mathrm{IL}}=\mathrm{MAX}$, | $\mathrm{IOH}=-0.4 \mathrm{~mA}$ | 2.5 | 3.4 |  | 2.7 | 3.4 |  | V |
| VOL | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}$ | $\mathrm{IOL}=4 \mathrm{~mA}$ |  | 0.25 | 0.4 |  |  | 0.4 | V |
|  |  |  | $\mathrm{IOL}=8 \mathrm{~mA}$ |  |  |  |  | 0.25 | 0.5 |  |
| 1 | $V_{C C}=$ MAX, | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  | 0.1 |  |  | 0.1 | mA |
| IIH | $V_{C C}=M A X$, | $\mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  |  | 20 |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | $V_{C C}=M A X$, | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.4 |  |  | -0.4 | mA |
| IOS§ | $V_{C C}=$ MAX |  |  | -20 |  | -100 | -20 |  | -100 | mA |
| ICCH | $V_{C C}=\mathrm{MAX}$, | $\mathrm{V}_{1}=0 \mathrm{~V}$ |  |  | 1.2 | 2.4 |  | 1.2 | 2.4 | mA |
| ICCL | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$, | $\mathrm{V}_{\mathrm{I}}=4.5 \mathrm{~V}$ |  |  | 3.6 | 6.6 |  | 3.6 | 6.6 | mA |

$\dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
$\ddagger$ All typical values are at $\mathrm{V}_{\mathrm{C}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
switching characteristics, $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathbf{2 5}^{\circ} \mathrm{C}$ (see Figure 2)

| PARAMETER | FROM (INPUT) | $\begin{gathered} \text { TO } \\ \text { (OUTPUT) } \end{gathered}$ | TEST CONDITIONS |  | $\begin{aligned} & \hline \text { SN54LS04 } \\ & \text { SN74LS04 } \end{aligned}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | MIN | TYP | MAX |  |
| tPLH | A | Y | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$, | $C_{L}=15 \mathrm{pF}$ |  | 9 | 15 | ns |
| tPHL |  |  |  |  |  | 10 | 15 |  |

recommended operating conditions

|  |  | SN54S04 |  |  | SN74S04 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage |  |  | 0.8 |  |  | 0.8 | V |
| $\mathrm{IOH}^{2}$ | High-level output current |  |  | -1 |  |  | -1 | mA |
| IOL | Low-level output current |  |  | 20 |  |  | 20 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS $\dagger$ |  |  | SN54S04 |  |  | SN74S04 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MIN | TYP\# | MAX | MIN | TYP¥ | MAX |  |
| VIK | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  | -1.2 |  |  | -1.2 |  |  | V |
| $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}$, | $\mathrm{IOH}=-1 \mathrm{~mA}$ | 2.5 | 3.4 |  | 2.7 | 3.4 |  | V |
| V OL | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | $\mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}$, | $\mathrm{IOL}=20 \mathrm{~mA}$ | 0.5 |  |  | 0.5 |  |  | V |
| 1 | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$, | $\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ |  |  |  | 1 |  |  | 1 | mA |
| 1 IH | $V_{C C}=$ MAX, | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 50 |  |  | 50 | $\mu \mathrm{A}$ |
| ILL | $V_{C C}=$ MAX, | $\mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}$ |  |  |  | -2 |  |  | -2 | mA |
| Ios§ | $V_{C C}=$ MAX |  |  | -40 |  | -100 | -40 |  | -100 | mA |
| ICCH | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$, | $\mathrm{V}_{1}=0 \mathrm{~V}$ |  |  | 15 | 24 |  | 15 | 24 | mA |
| ICCL | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$, | $\mathrm{V}_{\text {I }}=4.5 \mathrm{~V}$ |  |  | 30 | 54 |  | 30 | 54 | mA |

$\dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
$\ddagger$ All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
switching characteristics, $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS |  | $\begin{aligned} & \hline \text { SN54S04 } \\ & \text { SN74S04 } \end{aligned}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | MIN | TYP | MAX |  |
| tPLH | A | Y | $R_{L}=280 \Omega$, | $C_{L}=15 \mathrm{pF}$ |  | 3 | 4.5 | ns |
| tPHL |  |  |  |  |  | 3 | 5 |  |
| tPLH | A | Y | $R_{L}=280 \Omega$, | $C_{L}=50 \mathrm{pF}$ |  | 4.5 |  | ns |
| tPHL |  |  |  |  |  | 5 |  |  |

## PARAMETER MEASUREMENT INFORMATION SERIES 54/74 AND 54S/74S DEVICES





VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tpZL.
E. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{O}} \approx 50 \Omega$; $\mathrm{t}_{\mathrm{r}}$ and $\mathrm{t}_{\mathrm{f}} \leq 7 \mathrm{~ns}$ for Series $54 / 74$ devices and $\mathrm{t}_{\mathrm{r}}$ and $\mathrm{t}_{\mathrm{f}} \leq 2.5 \mathrm{~ns}$ for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES




VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1 N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tPZL.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{O}} \approx 50 \Omega, \mathrm{t}_{\mathrm{r}} \leq 1.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 2.6 \mathrm{~ns}$.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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## - PIN ARRANGEMENT



## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings | Unit |
| :--- | :--- | :---: | :---: |
| Supply voltage | $V C C$ | 7.0 | V |
| Input voltage | VIN | 7.0 | V |
| Output voltage | Vout | 30 | V |
| Operating temperature range | Topr | $-20 \sim+75$ | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | Tstg | $-65 \sim+150$ | ${ }^{\circ} \mathrm{C}$ |

## - RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | $\min$ | typ | $\max$ | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Supply voltage | $V C C$ | 4.75 | 5.00 | 5.25 | V |
| High level output voltage | $V O H$ | - | - | 30 | V |
| Low level output current | $I O L$ | - | - | 48 | mA |
| Operating temperature range | Topr | -20 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS (Ta $=-20 \sim+75^{\circ} \mathrm{C}$ )

| Item | Symbol | Test Conditions |  |  | min | typ* | max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input voltage | VIH |  |  |  | 2.0 | - | - | V |
|  | VIL |  |  |  | - | - | 0.8 | V |
| Output voltage | VoL | $V C C=4.75 \mathrm{~V}$, | $V / H=2 \mathrm{~V}$ | $1 O L=24 \mathrm{~mA}$ | - | - | 0.4 | V |
|  |  |  |  | $I O L=48 \mathrm{~mA}$ | - | - | 0.5 | V |
| Input current | $\overline{I H}$ | $V C C=5.25 \mathrm{~V}$ | $V I=2.7 \mathrm{~V}$ |  | - | - | 20 | $\mu \mathrm{A}$ |
|  | ILL | $V C C=5.25 \mathrm{~V}$, | $V=0.4 \mathrm{~V}$ |  | - | - | -0.4 | mA |
|  | II | $V C C=5.25 \mathrm{~V}$, | $V I=7 \mathrm{~V}$ |  | - | - | 0.1 | mA |
| Output current | IOH | $V C C=4.75 \mathrm{~V}$, | $V / L=0.8 \mathrm{~V}$, | $\mathrm{VOH}=30 \mathrm{~V}$ | - | - | 250 | $\mu \mathrm{A}$ |
| Supply current | ICCH | $V C C=5.25 \mathrm{~V}$ |  |  | - | 23 | 48 | mA |
|  | ICCL | $V C C=5.25 \mathrm{~V}$ |  |  | - | 21 | 51 | mA |
| Input clamp voltage | $V I K$ | $V C C=4.75 \mathrm{~V}$ | IIN $=-18 \mathrm{~mA}$ |  | - | - | -1.5 | V |

*VCC $=5 \mathrm{~V}, T a=25^{\circ} \mathrm{C}$

SWITCHING CHARACTERISTICS (VCC $=5 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$ )

| Item | Symbol | Test Conditions | min | typ | max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation delay time | $t_{P L H}$ | $C_{L=15 \mathrm{pF}, R L=110 \Omega}$ | $t_{P H L}$ |  | - | 10 |
|  |  |  | - | 15 | 23 | ns |

## ■ TESTING METHOD

Test Circuit


Waveform


Notes) 1. Input puise: $P R R=1 \mathrm{MHz}$, duty cycle $50 \%$, Zout $=50 \Omega$, ttLH $\leq 15 \mathrm{~ns}$. tTHL $\leq 6 \mathrm{~ns}$
2. CL includes probe and jig capacitance.
3. All diodes are $1 \mathrm{~S} 2074(\mathrm{H})$


| Hitachi Code | DP-14 |
| :--- | :--- |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.97 g |



| Hitachi Code | FP-14DA |
| :--- | :--- |
| JEDEC | - |
| EIAJ | Conforms |
| Weight (reference value) | 0.23 g |



| Hitachi Code | FP-14DN |
| :--- | :--- |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 0.13 g |

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## HITACHI

## Hitachi, Ltd.

Semiconductor \& Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109
URL NorthAmerica : http:semiconductor.hitachi.com/

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## For further information write to:

Hitachi Semiconductor
America) Inc.
179 East Tasman Drive, San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group Dornacher Stra§e 3
D-85622 Feldkirchen, Munich Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9293000
Hitachi Europe Ltd Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd. 16 Collyer Quay \#20-00 Hitachi Tower Singapore 049318
Tel: 535-2100
Fax: 535-1533
Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

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| Absolute Maximum Ratings (Note) |
| :--- |
| If Military/Aerospace specified devices are required, |
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| Supply Voltage |
| Input Voltage |
| Operating Free Air Temperature Range |
| DM54LS and 54 LS |
| DM74LS |
| Storage Temperature Range |
| Te |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS08 |  |  | DM74LS08 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\text {l }}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| IOL | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | $\begin{gathered} \text { Typ } \\ \text { (Note 1) } \end{gathered}$ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{IOL}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {IL }}$ | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & (\text { Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICCH | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 2.4 | 4.8 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 4.4 | 8.8 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 4 | 13 | 6 | 18 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 11 | 5 | 18 | ns |
| Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$. |  |  |  |  |  |  |




Physical Dimensions inches (millimeters) (Continued)

14-Lead Ceramic Flat Package (W) Order Number 54LS08FMQB or DM54LS08W NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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| :---: | :---: | :---: | :---: |



Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage | 7 V |
| :--- | ---: |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range |  |
| DM54LS and 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS32 |  |  | DM74LS32 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\prime}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{IOL}^{\text {l }}$ | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min} \end{aligned}$ | DM54 | 2.5 | 3.4 |  | V |
|  |  |  | DM74 | 2.7 | 3.4 |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}$ | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.36 | mA |
| los | Short Circuit Output Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\ & \text { (Note 2) } \end{aligned}$ | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ${ }^{\text {ICCH }}$ | Supply Current with Outputs High | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 3.1 | 6.2 | mA |
| $\mathrm{I}_{\text {CCL }}$ | Supply Current with Outputs Low | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ |  |  | 4.9 | 9.8 | mA |

Switching Characteristics at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega$ |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ |  |  |
|  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | 3 | 11 | 4 | 15 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | 3 | 11 | 4 | 15 | ns |
| Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$. <br> Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. |  |  |  |  |  |  |




54LS32/DM54LS32/DM74LS32 Quad 2-Input OR Gates
Physical Dimensions inches (millimeters) (Continued)

14-Lead Ceramic Flat Package (W) Order Number 54LS32FMQB or DM54LS32W NS Package Number W14B

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| :---: | :---: | :---: | :---: |



Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage | 7 V |
| :--- | ---: |
| Input Voltage | 7 V |
| Operating Free Air Temperature Range |  |
| DM54LS and 54LS | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| DM74LS | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | DM54LS279 |  |  | DM74LS279 |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\text {IH }}$ | High Level Input Voltage | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\mathrm{IL}}$ | Low Level Input Voltage |  |  | 0.7 |  |  | 0.8 | V |
| $\mathrm{IOH}^{\prime}$ | High Level Output Current |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{IOL}^{\text {l }}$ | Low Level Output Current |  |  | 4 |  |  | 8 | mA |
| $\mathrm{T}_{\text {A }}$ | Free Air Operating Temperature | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions |  | Min | Typ <br> (Note 1) | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{1}$ | Input Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 | 2.5 | 3.5 |  | V |
|  |  |  | DM74 | 2.7 | 3.5 |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low Level Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min} \end{aligned}$ | DM54 |  | 0.25 | 0.4 | V |
|  |  |  | DM74 |  | 0.35 | 0.5 |  |
|  |  | $\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}$, | DM74 |  | 0.25 | 0.4 |  |
| 1 | Input Current @ Max Input Voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  |  | 0.1 | mA |
| IIH | High Level Input Current | $V_{C C}=\operatorname{Max}, \mathrm{V}_{\mathrm{l}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IIL | Low Level Input Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V}$ |  |  |  | -0.4 | mA |
| los | Short Circuit Output Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ <br> (Note 2) | DM54 | -20 |  | -100 | mA |
|  |  |  | DM74 | -20 |  | -100 |  |
| ICC | Supply Current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}$ (Note 3) |  |  | 3.8 | 7 | mA |

Note 1: All typicals are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all $\overline{\mathrm{R}}$ inputs grounded, all $\overline{\mathrm{S}}$ inputs at 4.5 V and all outputs open.

| Symbol | Parameter | From (Input) <br> To (Output) | $\mathbf{R}_{\mathrm{L}}=\mathbf{2 k} \mathbf{~}$, |  |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |
|  |  |  | Min | Max | Min | Max |  |
| $t_{\text {PLH }}$ | Propagation Delay Time Low to High Level Output | $\begin{gathered} \overline{\mathrm{S}} \text { to } \\ \mathrm{Q} \end{gathered}$ |  | 22 |  | 25 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\overline{\mathrm{S}}$ to Q |  | 15 |  | 23 | ns |
| $t_{\text {PHL }}$ | Propagation Delay Time High to Low Level Output | $\overline{\mathrm{R}}$ to Q |  | 27 |  | 33 | ns |



Physical Dimensions inches (millimeters) (Continued)


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| :---: | :---: | :---: | :---: |

## Features

- Compatible with MCS ${ }^{\oplus}-51$ Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
- Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5 V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)


## Description

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the indus-try-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.
The AT89S51 provides the following standard features: 4 K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a fivevector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

## Pin Configurations

| PDIP |  |  |  |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| P1.0 | 1 | 40 | $\square \mathrm{VCC}$ |
| P1.1 | 2 | 39 | $\square \mathrm{P} 0.0$ (ADO) |
| P1.2 | 3 | 38 | $\square \mathrm{P} 0.1$ (AD1) |
| P1.3 | 4 | 37 | $\square \mathrm{P} 0.2$ (AD2) |
| P1.4 | 5 | 36 | $\square \mathrm{P} 0.3$ (AD3) |
| (MOSI) P1.5 $\square$ | 6 | 35 | $\square \mathrm{P} 0.4$ (AD4) |
| (MISO) P1.6 | 7 | 34 | $\square \mathrm{P} 0.5$ (AD5) |
| (SCK) P1.7 $\square$ | 8 | 33 | $\square \mathrm{P} 0.6$ (AD6) |
| RST $\square$ | 9 | 32 | $\square \mathrm{P} 0.7$ (AD7) |
| (RXD) P3.0 $\square$ | 10 | 31 | $\square \overline{\mathrm{EA}} / \mathrm{VPP}$ |
| (TXD) P3.1 $\square$ | 11 | 30 | $\square \mathrm{ALE} / \overline{\mathrm{PROG}}$ |
| (INT0) P3.2 $\square$ | 12 | 29 | $\square \overline{\text { PSEN }}$ |
| (INT1) P3.3 | 13 | 28 | $\square \mathrm{P} 2.7$ (A15) |
| (T0) P3.4 $\square$ | 14 | 27 | $\square \mathrm{P} 2.6$ (A14) |
| (T1) P3.5 | 15 | 26 | $\square \mathrm{P} 2.5$ (A13) |
| ( $\overline{\mathrm{WR}})$ P3.6 | 16 | 25 | $\square \mathrm{P} 2.4$ (A12) |
| ( $\overline{\mathrm{RD}}) \mathrm{P} 3.7 \square$ | 17 | 24 | $\square \mathrm{P} 2.3$ (A11) |
| XTAL2 | 18 | 23 | $\square \mathrm{P} 2.2$ (A10) |
| XTAL1 | 19 | 22 | $\square \mathrm{P} 2.1$ (A9) |
| GND | 20 | 21 | $\square \mathrm{P} 2.0$ (A8) |




| PDIP |  |  |  |
| :---: | :---: | :---: | :---: |
|  |  |  |  |
| RST - | 1 | 42 | $\square \mathrm{P} 1.7$ (SCK) |
| (RXD) P3.0 | 2 | 41 | $\square \mathrm{P} 1.6$ (MISO) |
| (TXD) P3.1 | 3 | 40 | $\square \mathrm{P} 1.5$ (MOSI) |
| (INTO) P3.2 | 4 | 39 | P1.4 |
| (INT1) P3.3 | 5 | 38 | P1.3 |
| (T0) P3.4 | 6 | 37 | $\square \mathrm{P} 1.2$ |
| (T1) P3.5 | 7 | 36 | $\square \mathrm{P} 1.1$ |
| ( $\overline{\mathrm{WR}}) \mathrm{P} 3.6$ | 8 | 35 | P1.0 |
| ( $\overline{\mathrm{RD}}) \mathrm{P} 3.7$ | 9 | 34 | $\checkmark$ VDD |
| XTAL2 | 10 | 33 | $\square$ PWRVDD |
| XTAL1 | 11 | 32 | $\square \mathrm{P} 0.0$ (ADO) |
| GND | 12 | 31 | $\square \mathrm{P} 0.1$ (AD1) |
| PWRGND | 13 | 30 | $\square \mathrm{P} 0.2$ (AD2) |
| (A8) P2.0 | 14 | 29 | P0.3 (AD3) |
| (A9) P2.1 | 15 | 28 | $\square \mathrm{P} 0.4$ (AD4) |
| (A10) P2.2 | 16 | 27 | P0.5 (AD5) |
| (A11) P2.3 | 17 | 26 | P0.6 (AD6) |
| (A12) P2.4 | 18 | 25 | P0.7 (AD7) |
| (A13) P2.5 | 19 | 24 | $\square \overline{E A} / \mathrm{VPP}$ |
| (A14) P2.6 | 20 | 23 | $\square \mathrm{ALE} / \overline{\mathrm{PROG}}$ |
| (A15) P2.7 | 21 | 22 | PSEN |

## Block Diagram



## Pin Description

VCC

GND

Supply voltage (all packages except 42-PDIP).

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board MUST connect both VDD and PWRVDD to the board supply voltage.

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board MUST connect both GND and PWRGND to the board ground.

Port 0 is an 8 -bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1 s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 is an 8 -bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1 s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ( $I_{L}$ ) because of the internal pull-ups.
Port 1 also receives the low-order address bytes during Flash programming and verification.

| Port Pin | Alternate Functions |
| :--- | :--- |
| P1.5 | MOSI (used for In-System Programming) |
| P1.6 | MISO (used for In-System Programming) |
| P1.7 | SCK (used for In-System Programming) |

Port 2 is an 8 -bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1 s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current $\left(l_{L}\right)$ because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

## Port 3

## ALE/PROG

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
External Access Enable. $\overline{\mathrm{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000 H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.
$\overline{E A}$ should be strapped to $\mathrm{V}_{\mathrm{CC}}$ for internal program executions.
This pin also receives the 12 -volt programming enable voltage ( $\mathrm{V}_{\mathrm{PP}}$ ) during Flash programming.

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

| 0F8H |  |  |  |  |  |  |  |  | 0FFH |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0FOH | $\begin{gathered} \text { B } \\ 00000000 \end{gathered}$ |  |  |  |  |  |  |  | 0F7H |
| 0E8H |  |  |  |  |  |  |  |  | 0EFH |
| OEOH | $\begin{gathered} \text { ACC } \\ 00000000 \end{gathered}$ |  |  |  |  |  |  |  | 0E7H |
| 0D8H |  |  |  |  |  |  |  |  | ODFH |
| 0DOH | $\begin{gathered} \text { PSW } \\ 00000000 \end{gathered}$ |  |  |  |  |  |  |  | 0D7H |
| 0 C 8 H |  |  |  |  |  |  |  |  | OCFH |
| OCOH |  |  |  |  |  |  |  |  | 0C7H |
| 0B8H | $\begin{gathered} \text { IP } \\ \times \times 000000 \end{gathered}$ |  |  |  |  |  |  |  | OBFH |
| 0B0H | $\begin{gathered} \text { P3 } \\ 11111111 \end{gathered}$ |  |  |  |  |  |  |  | 0B7H |
| 0A8H | $\begin{gathered} \text { IE } \\ 0 \times 000000 \end{gathered}$ |  |  |  |  |  |  |  | OAFH |
| OAOH | $\begin{gathered} \text { P2 } \\ 11111111 \end{gathered}$ |  | $\begin{gathered} \text { AUXR1 } \\ \text { XXXXXX0 } \end{gathered}$ |  |  |  | WDTRST XXXXXXXX |  | 0A7H |
| 98H | $\begin{gathered} \text { SCON } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { SBUF } \\ \text { XXXXXXXX } \end{gathered}$ |  |  |  |  |  |  | 9FH |
| 90H | $\begin{gathered} \text { P1 } \\ 11111111 \end{gathered}$ |  |  |  |  |  |  |  | 97H |
| 88H | $\begin{gathered} \text { TCON } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TMOD } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TLO } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TL1 } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TH0 } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { TH1 } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { AUXR } \\ \text { XXX00XX0 } \end{gathered}$ |  | 8FH |
| 80H | $\begin{gathered} \text { P0 } \\ 11111111 \end{gathered}$ | $\begin{gathered} \text { SP } \\ 00000111 \end{gathered}$ | $\begin{gathered} \text { DPOL } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { DPOH } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { DP1L } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { DP1H } \\ 00000000 \end{gathered}$ |  | $\begin{gathered} \text { PCON } \\ 0 X X X 0000 \end{gathered}$ | 87H |

User software should not write 1 s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0 .

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register


Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16 -bit Data Pointer Registers are provided: DP0 at SFR address locations $82 \mathrm{H}-$ 83 H and DP1 at $84 \mathrm{H}-85 \mathrm{H}$. Bit DPS $=0$ in SFR AUXR1 selects DP0 and DPS $=1$ selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to " 1 " during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1


## Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64 K bytes each of external Program and Data Memory can be addressed.

If the $\overline{E A}$ pin is connected to GND, all program fetches are directed to external memory.
On the AT89S51, if $\overline{E A}$ is connected to $\mathrm{V}_{\mathrm{CC}}$, program fetches to addresses 0000 H through FFFH are directed to internal memory and fetches to addresses 1000 H through FFFFH are directed to external memory.

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location OA6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location OA6H). When the WDT is enabled, the user needs to service it by writing 01EH and OE1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is $98 \times$ TOSC, where TOSC $=1 /$ FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

## UART

## Timer 0 and 1

## Interrupts

In Power-down mode the oscillator stops, which means the WDT also stops. While in Powerdown mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0 ) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.
With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe ${ }^{\circledR}$ Acrobat ${ }^{\circledR}$ file "AT89 Series Hardware Description".

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe Acrobat file "AT89 Series Hardware Description".

The AT89S51 has a total of five interrupt vectors: two external interrupts (INT0 and INT1), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.
Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.
Note that Table 4 shows that bit positions IE. 6 and IE. 5 are unimplemented. User software should not write 1 s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 4. Interrupt Enable (IE) Register
(MSB)

| EA | - | - | ES | ET1 | EX1 | ET0 | EX0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables the interrupt.

| Symbol | Position | Function |
| :--- | :--- | :--- |
| EA | IE. 7 | Disables all interrupts. If EA $=0$, no interrupt is <br> acknowledged. If EA $=1$, each interrupt source is <br> individually enabled or disabled by setting or clearing <br> its enable bit. |
| - | IE.6 | Reserved |
| - | IE. 5 | Reserved |
| ES | IE.4 | Serial Port interrupt enable bit |
| ET1 | IE.3 | Timer 1 interrupt enable bit |
| EX1 | IE. 2 | External interrupt 1 enable bit |
| ET0 | IE.0 | Timer 0 interrupt enable bit |
| EX0 | External interrupt 0 enable bit |  |
| User software should never write 1s to reserved bits, because they may be used in future AT89 <br> products. |  |  |

Figure 1. Interrupt Sources

$\mathrm{TFO} \longrightarrow$


TF1 $\longrightarrow$


## Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections


Note: $\quad \mathrm{C} 1, \mathrm{C} 2=30 \mathrm{pF} \pm 10 \mathrm{pF}$ for Crystals
$=40 \mathrm{pF} \pm 10 \mathrm{pF}$ for Ceramic Resonators
Figure 3. External Clock Drive Configuration


In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.
Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Powerdown is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt (INTO or INT1). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $\mathrm{V}_{\mathrm{CC}}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize. morn

## Power-down Mode

## Idle Mode

Table 5. Status of External Pins During Idle and Power-down Modes

| Mode | Program Memory | ALE | $\overline{\text { PSEN }}$ | PORT0 | PORT1 | PORT2 | PORT3 |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power-down | External | 0 | 0 | Float | Data | Data | Data |

## Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed $(P)$ to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

| Program Lock Bits |  |  |  | Protection Type |
| :---: | :---: | :---: | :---: | :---: |
|  | LB1 | LB2 | LB3 |  |
| 1 | U | U | U | No program lock features |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{\mathrm{EA}}$ is sampled and latched on reset, and further programming of the Flash memory is disabled |
| 3 | P | P | U | Same as mode 2, but verify is also disabled |
| 4 | P | P | P | Same as mode 3, but external execution is also disabled |

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of EA must agree with the current logic level at that pin in order for the device to function properly.

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.
Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 7) and Figures 4 and 5 . To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{E A} / V_{P P}$ to 12 V .
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The bytewrite cycle is self-timed and typically takes no more than $50 \mu \mathrm{~s}$. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.
 During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{\text { Data }}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/ $\overline{\operatorname{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations $000 \mathrm{H}, 100 \mathrm{H}$, and 200 H , except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.
$(000 \mathrm{H})=1 \mathrm{EH}$ indicates manufactured by Atmel
$(100 \mathrm{H})=51 \mathrm{H}$ indicates AT89S51
$(200 \mathrm{H})=06 \mathrm{H}$
Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/PROG low for a duration of 200 ns 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms .

During chip erase, a serial read from any address location will return 00 H at the data output.

> Programming the Flash Serial Mode

## Serial <br> Programming Algorithm

The Code memory array can be programmed using the serial ISP interface while RST is pulled to $\mathrm{V}_{\mathrm{cc}}$. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.
The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than $1 / 16$ of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz .

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

Apply power between VCC and GND pins.
Set RST pin to " H ".
If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5 V .
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):
Set XTAL1 to "L" (if a crystal is not used).
Set RST to "L".
Turn $\mathrm{V}_{\mathrm{Cc}}$ power off.
Data Polling: The $\overline{\text { Data }}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

## Serial <br> Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8.

## Programming Interface Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

| Mode | $\mathrm{V}_{\mathrm{cc}}$ | RST | PSEN | $\frac{\text { ALE/ }}{\text { PROG }}$ | $\begin{aligned} & \overline{E A} / \\ & \mathrm{V}_{\mathrm{PP}} \end{aligned}$ | P2.6 | P2.7 | P3.3 | P3.6 | P3.7 | $\begin{aligned} & \text { P0.7-0 } \\ & \text { Data } \end{aligned}$ | P2.3-0 | P1.7-0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  | Address |  |
| Write Code Data | 5 V | H | L | $\sim^{(2)}$ | 12 V | L | H | H | H | H | $\mathrm{D}_{\text {IN }}$ | A11-8 | A7-0 |
| Read Code Data | 5V | H | L | H | H | L | L | L | H | H | $\mathrm{D}_{\text {OUt }}$ | A11-8 | A7-0 |
| Write Lock Bit 1 | 5 V | H | L | $\sim^{(3)}$ | 12 V | H | H | H | H | H | X | X | X |
| Write Lock Bit 2 | 5 V | H | L | $\sim^{(3)}$ | 12 V | H | H | H | L | L | X | X | X |
| Write Lock Bit 3 | 5 V | H | L | $\sim^{(3)}$ | 12 V | H | L | H | H | L | X | X | X |
| Read Lock Bits $1,2,3$ | 5 V | H | L | H | H | H | H | L | H | L | $\begin{aligned} & \text { P0.2, } \\ & \text { P0.3, } \\ & \text { P0. } \end{aligned}$ | X | X |
| Chip Erase | 5 V | H | L | $\sim{ }^{(1)}$ | 12 V | H | L | H | L | L | X | X | X |
| Read Atmel ID | 5 V | H | L | H | H | L | L | L | L | L | 1 EH | 0000 | 00H |
| Read Device ID | 5 V | H | L | H | H | L | L | L | L | L | 51H | 0001 | OOH |
| Read Device ID | 5 V | H | L | H | H | L | L | L | L | L | 06H | 0010 | OOH |

Notes: 1. Each PROG pulse is $200 \mathrm{~ns}-500 \mathrm{~ns}$ for Chip Erase.
2. Each $\overline{\text { PROG }}$ pulse is $200 \mathrm{~ns}-500 \mathrm{~ns}$ for Write Code Data.
3. Each PROG pulse is $200 \mathrm{~ns}-500 \mathrm{~ns}$ for Write Lock Bits.
4. RDY/ $\overline{\mathrm{BSY}}$ signal is output on P3.0 during programming.
5. $\mathrm{X}=$ don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)


Figure 5. Verifying the Flash Memory (Parallel Mode)


Flash Programming and Verification Characteristics (Parallel Mode)
$\mathrm{T}_{\mathrm{A}}=20^{\circ} \mathrm{C}$ to $30^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=4.5$ to 5.5 V

| Symbol | Parameter | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {PP }}$ | Programming Supply Voltage | 11.5 | 12.5 | V |
| $\mathrm{I}_{\mathrm{PP}}$ | Programming Supply Current |  | 10 | mA |
| $\mathrm{I}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}$ Supply Current |  | 30 | mA |
| 1/t ${ }_{\text {CLCL }}$ | Oscillator Frequency | 3 | 33 | MHz |
| $t_{\text {AVGL }}$ | Address Setup to $\overline{\text { PROG Low }}$ | $48 \mathrm{t}_{\text {CLCL }}$ |  |  |
| $\mathrm{t}_{\text {GHAX }}$ | Address Hold After PROG | $48 \mathrm{t}_{\mathrm{CLCL}}$ |  |  |
| $\mathrm{t}_{\text {DVGL }}$ | Data Setup to $\overline{\text { PROG }}$ Low | $48 \mathrm{t}_{\text {CLCL }}$ |  |  |
| $\mathrm{t}_{\text {GHDX }}$ | Data Hold After $\overline{\text { PROG }}$ | $48 \mathrm{t}_{\text {CLCL }}$ |  |  |
| $\mathrm{t}_{\text {EHSH }}$ | P2.7 ( $\overline{\text { ENABLE }}$ ) High to $\mathrm{V}_{\mathrm{PP}}$ | $48 \mathrm{t}_{\mathrm{CLCL}}$ |  |  |
| $\mathrm{t}_{\text {SHGL }}$ | $\mathrm{V}_{\text {PP }}$ Setup to $\overline{\text { PROG }}$ Low | 10 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {GHSL }}$ | $V_{\text {PP }}$ Hold After $\overline{\text { PROG }}$ | 10 |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {GLGH }}$ | $\overline{\text { PROG Width }}$ | 0.2 | 1 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {AVQV }}$ | Address to Data Valid |  | $48 \mathrm{t}_{\text {CLCL }}$ |  |
| $t_{\text {ELQV }}$ | ENABLE Low to Data Valid |  | $48 \mathrm{t}_{\text {CLCL }}$ |  |
| $\mathrm{t}_{\text {EHQZ }}$ | Data Float After ENABLE | 0 | $48 \mathrm{t}_{\text {CLCL }}$ |  |
| $\mathrm{t}_{\text {GHBL }}$ | $\overline{\text { PROG }}$ High to $\overline{\text { BUSY }}$ Low |  | 1.0 | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {wc }}$ | Byte Write Cycle Time |  | 50 | $\mu \mathrm{s}$ |

Figure 6. Flash Programming and Verification Waveforms - Parallel Mode


Figure 7. Flash Memory Serial Downloading


## Flash Programming and Verification Waveforms - Serial Mode

Figure 8. Serial Programming Waveforms


Table 8. Serial Programming Instruction Set

| Instruction | Instruction <br> Format |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
|  | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Operation |

Note: 1. B1 $=0, \mathrm{~B} 2=0 \rightarrow$ Mode 1, no lock protection $\mathrm{B} 1=0, \mathrm{~B} 2=1 \rightarrow$ Mode 2, lock bit 1 activated $B 1=1, B 2=0 \rightarrow$ Mode 3, lock bit 2 activated $B 1=1, B 2=1 \rightarrow$ Mode 4, lock bit 3 activated

Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than $1 / 16$ of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255 . After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

## Serial Programming Characteristics

Figure 9. Serial Programming Timing


Table 9. Serial Programming Characteristics, $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=4.0-5.5 \mathrm{~V}$ (Unless Otherwise Noted)

| Symbol | Parameter | Min | Typ | Max | Units |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $1 / t_{\text {CLCL }}$ | Oscillator Frequency | 3 |  | 33 | MHz |
| $\mathrm{t}_{\mathrm{CLCL}}$ | Oscillator Period | 30 |  |  | ns |
| $\mathrm{t}_{\text {SHSL }}$ | SCK Pulse Width High | $8 \mathrm{t}_{\mathrm{CLCL}}$ |  |  | ns |
| $\mathrm{t}_{\mathrm{SLSH}}$ | SCK Pulse Width Low | $8 \mathrm{t}_{\mathrm{CLCL}}$ |  | ns |  |
| $\mathrm{t}_{\mathrm{OVSH}}$ | MOSI Setup to SCK High | $\mathrm{t}_{\mathrm{CLCL}}$ |  |  | ns |
| $\mathrm{t}_{\text {SHOX }}$ | MOSI Hold after SCK High | $2 \mathrm{t}_{\mathrm{CLCL}}$ |  |  | ns |
| $\mathrm{t}_{\text {SLIV }}$ | SCK Low to MISO Valid | 10 |  | 16 | 32 |
| $\mathrm{t}_{\text {ERASE }}$ | Chip Erase Instruction Cycle Time |  |  | 500 | ns |
| $\mathrm{t}_{\text {SWC }}$ | Serial Byte Write Cycle Time |  |  | $64 \mathrm{t}_{\mathrm{CLCL}}+400$ | $\mu \mathrm{~s}$ |

## Absolute Maximum Ratings*

| Operating Temperature ............................... $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| :--- |
| Storage Temperature ................................ $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Voltage on Any Pin |
| with Respect to Ground .................................. -1.0 V to +7.0 V |
| Maximum Operating Voltage ........................................... 6.6 V |
| DC Output Current...................................................... 15.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

The values shown in this table are valid for $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}$ to 5.5 V , unless otherwise noted.

| Symbol | Parameter | Condition | Min | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Input Low Voltage | (Except EA) | -0.5 | $0.2 \mathrm{~V}_{\mathrm{CC}}-0.1$ | V |
| $\mathrm{V}_{\text {IL1 }}$ | Input Low Voltage ( $\overline{\mathrm{EA}}$ ) |  | -0.5 | $0.2 \mathrm{~V}_{\mathrm{CC}}-0.3$ | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input High Voltage | (Except XTAL1, RST) | $0.2 \mathrm{~V}_{\mathrm{CC}}+0.9$ | $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{V}_{\mathrm{IH} 1}$ | Input High Voltage | (XTAL1, RST) | $0.7 \mathrm{~V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}+0.5$ | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Output Low Voltage ${ }^{(1)}$ (Ports 1,2,3) | $\mathrm{I}_{\mathrm{OL}}=1.6 \mathrm{~mA}$ |  | 0.45 | V |
| $\mathrm{V}_{\text {OL1 }}$ | Output Low Voltage ${ }^{(1)}$ (Port 0, ALE, PSEN) | $\mathrm{I}_{\mathrm{OL}}=3.2 \mathrm{~mA}$ |  | 0.45 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | Output High Voltage <br> (Ports 1,2,3, ALE, PSEN) | $\mathrm{I}_{\mathrm{OH}}=-60 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%$ | 2.4 |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-25 \mu \mathrm{~A}$ | $0.75 \mathrm{~V}_{\mathrm{Cc}}$ |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-10 \mu \mathrm{~A}$ | $0.9 \mathrm{~V}_{\mathrm{CC}}$ |  | V |
| $\mathrm{V}_{\mathrm{OH} 1}$ | Output High Voltage <br> (Port 0 in External Bus Mode) | $\mathrm{I}_{\mathrm{OH}}=-800 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%$ | 2.4 |  | V |
|  |  | $\mathrm{I}_{\text {OH }}=-300 \mu \mathrm{~A}$ | $0.75 \mathrm{~V}_{\mathrm{CC}}$ |  | V |
|  |  | $\mathrm{I}_{\mathrm{OH}}=-80 \mu \mathrm{~A}$ | $0.9 \mathrm{~V}_{\mathrm{CC}}$ |  | V |
| $\mathrm{I}_{\text {IL }}$ | Logical 0 Input Current (Ports 1,2,3) | $\mathrm{V}_{\mathrm{IN}}=0.45 \mathrm{~V}$ |  | -50 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{TL}}$ | Logical 1 to 0 Transition Current (Ports 1,2,3) | $\mathrm{V}_{\text {IN }}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%$ |  | -650 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{LI}}$ | Input Leakage Current (Port 0, $\overline{\mathrm{EA}}$ ) | $0.45<\mathrm{V}_{\text {IN }}<\mathrm{V}_{\mathrm{CC}}$ |  | $\pm 10$ | $\mu \mathrm{A}$ |
| RRST | Reset Pulldown Resistor |  | 50 | 300 | $\mathrm{K} \Omega$ |
| $\mathrm{C}_{10}$ | Pin Capacitance | Test Freq. $=1 \mathrm{MHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 10 | pF |
| $\mathrm{I}_{\mathrm{CC}}$ | Power Supply Current | Active Mode, 12 MHz |  | 25 | mA |
|  |  | Idle Mode, 12 MHz |  | 6.5 | mA |
|  | Power-down Mode ${ }^{(2)}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ |  | 50 | $\mu \mathrm{A}$ |

Notes: 1. Under steady state (non-transient) conditions, $\mathrm{I}_{\mathrm{OL}}$ must be externally limited as follows:
Maximum Iol per port pin: 10 mA
Maximum I $\mathrm{I}_{\mathrm{OL}}$ per 8-bit port:
Port 0: $26 \mathrm{~mA} \quad$ Ports 1, 2, 3: 15 mA
Maximum total $\mathrm{I}_{\mathrm{OL}}$ for all output pins: 71 mA
If $\mathrm{I}_{\mathrm{OL}}$ exceeds the test condition, $\mathrm{V}_{\mathrm{OL}}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum $\mathrm{V}_{\mathrm{CC}}$ for Power-down is 2 V .

## AC Characteristics

Under operating conditions, load capacitance for Port $0, A L E / \overline{\text { PROG }}$, and $\overline{\text { PSEN }}=100 \mathrm{pF}$; load capacitance for all other outputs $=80 \mathrm{pF}$.

## External Program and Data Memory Characteristics

| Symbol | Parameter | 12 MHz Oscillator |  | Variable Oscillator |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max |  |
| 1/t ${ }_{\text {CLCL }}$ | Oscillator Frequency |  |  | 0 | 33 | MHz |
| $t_{\text {LHLL }}$ | ALE Pulse Width | 127 |  | $2 \mathrm{t}_{\mathrm{CLCL}}-40$ |  | ns |
| $t_{\text {AVLL }}$ | Address Valid to ALE Low | 43 |  | $\mathrm{t}_{\text {CLCL- }}-25$ |  | ns |
| $\mathrm{t}_{\text {LLAX }}$ | Address Hold After ALE Low | 48 |  | $\mathrm{t}_{\text {CLCL- }} 25$ |  | ns |
| $\mathrm{t}_{\text {LLIV }}$ | ALE Low to Valid Instruction In |  | 233 |  | $4 t_{\text {CLCL }}-65$ | ns |
| tLLPL | ALE Low to $\overline{\text { PSEN }}$ Low | 43 |  | $\mathrm{t}_{\text {CLCL- }}-25$ |  | ns |
| $t_{\text {PLPH }}$ | $\overline{\text { PSEN Pulse Width }}$ | 205 |  | $3 \mathrm{t}_{\mathrm{CLCL}}-45$ |  | ns |
| $\mathrm{t}_{\text {PLIV }}$ | $\overline{\text { PSEN Low to Valid Instruction In }}$ |  | 145 |  | $3 \mathrm{t}_{\text {CLCL- }}-60$ | ns |
| $\mathrm{t}_{\text {PXIX }}$ | Input Instruction Hold After $\overline{\text { PSEN }}$ | 0 |  | 0 |  | ns |
| $\mathrm{t}_{\text {PXIZ }}$ | Input Instruction Float After $\overline{\text { PSEN }}$ |  | 59 |  | $\mathrm{t}_{\mathrm{CLCL}}-25$ | ns |
| $\mathrm{t}_{\text {PXAV }}$ | $\overline{\text { PSEN }}$ to Address Valid | 75 |  | $\mathrm{t}_{\mathrm{CLCL}}{ }^{-8}$ |  | ns |
| $\mathrm{t}_{\text {AVIV }}$ | Address to Valid Instruction In |  | 312 |  | $5 \mathrm{t}_{\mathrm{CLCL}}-80$ | ns |
| $t_{\text {PLAZ }}$ | $\overline{\text { PSEN Low to Address Float }}$ |  | 10 |  | 10 | ns |
| $\mathrm{t}_{\text {RLRH }}$ | $\overline{\mathrm{RD}}$ Pulse Width | 400 |  | $6 \mathrm{t}_{\mathrm{CLCL}}-100$ |  | ns |
| $t_{\text {WLWH }}$ | $\overline{\text { WR Pulse Width }}$ | 400 |  | $6 \mathrm{t}_{\text {CLCLL }}{ }^{-100}$ |  | ns |
| $\mathrm{t}_{\text {RLDV }}$ | $\overline{\mathrm{RD}}$ Low to Valid Data In |  | 252 |  | $5 \mathrm{t}_{\text {CLCL }}-90$ | ns |
| $\mathrm{t}_{\text {RHDX }}$ | Data Hold After $\overline{\mathrm{RD}}$ | 0 |  | 0 |  | ns |
| $\mathrm{t}_{\text {RHDZ }}$ | Data Float After $\overline{\mathrm{RD}}$ |  | 97 |  | $2 \mathrm{t}_{\mathrm{CLCL}}-28$ | ns |
| tLLDV | ALE Low to Valid Data In |  | 517 |  | $8 \mathrm{t}_{\mathrm{CLCL}}-150$ | ns |
| $\mathrm{t}_{\text {AVDV }}$ | Address to Valid Data In |  | 585 |  | $9 \mathrm{t}_{\text {CLCL }}-165$ | ns |
| $\mathrm{t}_{\text {LLWL }}$ | ALE Low to $\overline{\mathrm{RD}}$ or $\overline{\mathrm{WR}}$ Low | 200 | 300 | $3 \mathrm{t}_{\mathrm{CLCL}}-50$ | $3 \mathrm{t}_{\mathrm{CLCL}}+50$ | ns |
| $t_{\text {AVWL }}$ | Address to $\overline{\mathrm{RD}}$ or WR Low | 203 |  | $4 \mathrm{t}_{\text {CLCLL }}-75$ |  | ns |
| $\mathrm{t}_{\text {QVwX }}$ | Data Valid to $\overline{\mathrm{WR}}$ Transition | 23 |  | $\mathrm{t}_{\text {CLCL }}$-30 |  | ns |
| $\mathrm{t}_{\text {QVWH }}$ | Data Valid to $\overline{W R}$ High | 433 |  | $7 \mathrm{t}_{\text {CLCL }}-130$ |  | ns |
| $\mathrm{t}_{\text {WHQX }}$ | Data Hold After $\overline{W R}$ | 33 |  | $\mathrm{t}_{\text {CLCL- }}$-25 |  | ns |
| $\mathrm{t}_{\text {RLAZ }}$ | $\overline{\mathrm{RD}}$ Low to Address Float |  | 0 |  | 0 | ns |
| $\mathrm{t}_{\text {WHLH }}$ | $\overline{\mathrm{RD}}$ or $\overline{\mathrm{WR}}$ High to ALE High | 43 | 123 | $\mathrm{t}_{\mathrm{CLCL}}-25$ | $\mathrm{t}_{\mathrm{CLCL}}+25$ | ns |

## External Program Memory Read Cycle



## External Data Memory Read Cycle



## External Data Memory Write Cycle



## External Clock Drive Waveforms



## External Clock Drive

| Symbol | Parameter | Min | Max | Units |
| :--- | :--- | :---: | :---: | :---: |
| $1 / t_{\text {CLCL }}$ | Oscillator Frequency | 0 | 33 | MHz |
| $\mathrm{t}_{\mathrm{CLCL}}$ | Clock Period | 30 |  | ns |
| $\mathrm{t}_{\mathrm{CHCX}}$ | High Time | 12 |  | ns |
| $\mathrm{t}_{\mathrm{CLCX}}$ | Low Time | 12 |  | ns |
| $\mathrm{t}_{\mathrm{CLCH}}$ | Rise Time |  | 5 | ns |
| $\mathrm{t}_{\mathrm{CHCL}}$ | Fall Time | 5 | ns |  |

## Serial Port Timing: Shift Register Mode Test Conditions

The values in this table are valid for $\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}$ to 5.5 V and Load Capacitance $=80 \mathrm{pF}$.

| Symbol | Parameter | 12 MHz Osc |  | Variable Oscillator |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max |  |
| $\mathrm{t}_{\text {XLXL }}$ | Serial Port Clock Cycle Time | 1.0 |  | $12 \mathrm{t}_{\text {CLCL }}$ |  | $\mu \mathrm{s}$ |
| $\mathrm{t}_{\text {QVXH }}$ | Output Data Setup to Clock Rising Edge | 700 |  | $10 \mathrm{CLLCL}^{-133}$ |  | ns |
| $\mathrm{t}_{\mathrm{XHQX}}$ | Output Data Hold After Clock Rising Edge | 50 |  | $2 \mathrm{t}_{\text {CLCL }}-80$ |  | ns |
| $\mathrm{t}_{\text {XHDX }}$ | Input Data Hold After Clock Rising Edge | 0 |  | 0 |  | ns |
| $\mathrm{t}_{\text {XHDV }}$ | Clock Rising Edge to Input Data Valid |  | 700 |  | $10 \mathrm{t}_{\text {CLCL }}-133$ | ns |

## Shift Register Mode Timing Waveforms



## AC Testing Input/Output Waveforms ${ }^{(1)}$



Note: 1. AC Inputs during testing are driven at $\mathrm{V}_{\mathrm{CC}}-0.5 \mathrm{~V}$ for a logic 1 and 0.45 V for a logic 0 . Timing measurements are made at $\mathrm{V}_{\mathrm{IH}}$ min . for a logic 1 and $\mathrm{V}_{\mathrm{IL}}$ max. for a logic 0 .

## Float Waveforms ${ }^{(1)}$



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded $\mathrm{V}_{\mathrm{OH}} / \mathrm{V}_{\mathrm{OL}}$ level occurs.

## Ordering Information

| Speed <br> (MHz) | Power Supply | Ordering Code | Package | Operation Range |
| :---: | :---: | :---: | :---: | :---: |
| 24 | 4.0 V to 5.5V | $\begin{aligned} & \text { AT89S51-24AC } \\ & \text { AT89S51-24JC } \\ & \text { AT89S51-24PC } \\ & \text { AT89S51-24SC } \end{aligned}$ | $\begin{aligned} & \hline 44 \mathrm{~A} \\ & 44 \mathrm{~J} \\ & 40 \mathrm{P} 6 \\ & 42 \mathrm{PS} 6 \end{aligned}$ | $\begin{aligned} & \text { Commercial } \\ & \left(0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C}\right) \end{aligned}$ |
|  |  | AT89S51-24AI <br> AT89S51-24JI <br> AT89S51-24PI <br> AT89S51-24SI | 44A <br> 44J <br> 40P6 <br> 42PS6 | $\begin{gathered} \text { Industrial } \\ \left(-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right) \end{gathered}$ |
| 33 | 4.5 V to 5.5 V | AT89S51-33AC <br> AT89S51-33JC <br> AT89S51-33PC <br> AT89S51-33SC | $\begin{aligned} & \hline 44 \mathrm{~A} \\ & 44 \mathrm{~J} \\ & 40 \mathrm{P} 6 \\ & 42 \mathrm{PS} 6 \end{aligned}$ | Commercial $\left(0^{\circ} \mathrm{C}\right.$ to $70^{\circ} \mathrm{C}$ ) |


| Package Type |  |
| :--- | :--- |
| 44A | 44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP) |
| 44J | 44-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 40P6 | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 42PS6 | 42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |

## Packaging Information

## 44A - TQFP



## 44J - PLCC



Notes: 1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion.

Allowable protrusion is $.010 "(0.254 \mathrm{~mm})$ per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is $0.004^{\prime \prime}(0.102 \mathrm{~mm})$ maximum.

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
DRAWING NO. REV.

40P6 - PDIP



Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure $=\mathrm{mm}$ )

| SYMBOL | MIN | NOM | MAX | NOTE |
| :---: | :---: | :---: | :---: | :---: |
| A | - | - | 4.83 |  |
| A1 | 0.51 | - | - |  |
| D | 36.70 | - | 36.96 | Note 2 |
| E | 15.24 | - | 15.88 |  |
| E1 | 13.46 | - | 13.97 | Note 2 |
| B | 0.38 | - | 0.56 |  |
| B1 | 0.76 | - | 1.27 |  |
| L | 3.05 | - | 3.43 |  |
| C | 0.20 | - | 0.30 |  |
| eB | - | - | 18.55 |  |
| e | 1.78 TYP |  |  |  |

## Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

## Regional Headquarters

Europe<br>Atmel Sarl<br>Route des Arsenaux 41<br>Case Postale 80<br>CH-1705 Fribourg<br>Switzerland<br>Tel: (41) 26-426-5555<br>Fax: (41) 26-426-5500<br>Asia<br>Room 1219<br>Chinachem Golden Plaza<br>77 Mody Road Tsimshatsui<br>East Kowloon<br>Hong Kong<br>Tel: (852) 2721-9778<br>Fax: (852) 2722-1369<br>Japan<br>9F, Tonetsu Shinkawa Bldg.<br>1-24-8 Shinkawa<br>Chuo-ku, Tokyo 104-0033<br>Japan<br>Tel: (81) 3-3523-3551<br>Fax: (81) 3-3523-7581

## Atmel Operations

Memory<br>2325 Orchard Parkway<br>San Jose, CA 95131, USA<br>Tel: 1(408) 441-0311<br>Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60
ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759
Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G750QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

## RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

## Biometrics/Imaging/Hi-Rel MPU/

High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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## Absolute Maximum Ratings

| If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. |  | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| :---: | :---: | :---: | :---: |
|  |  | Soldering Information |  |
|  |  | Dual-In-Line Package |  |
| Supply Voltage | $+18 \mathrm{~V}$ | Soldering (10 Seconds) | $260^{\circ} \mathrm{C}$ |
| Power Dissipation (Note 1) |  | Small Outline Package |  |
| LM555H, LM555CH | 760 mW | Vapor Phase (60 Seconds) | $215^{\circ} \mathrm{C}$ |
| LM555, LM555CN | 1180 mW | Infrared (15 Seconds) | $220^{\circ} \mathrm{C}$ |
| Operating Temperature Ranges |  | See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. |  |
| LM555C | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |  |  |  |
| LM555 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |

## Electrical Characteristics $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}\right.$ to +15 V , unless othewise specified)




## Typical Performance Characteristics



## Applications Information

## monostable operation

In this mode of operation, the timer functions as a one-shot (Figure 1). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than $1 / 3 \mathrm{~V}_{\mathrm{CC}}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.


## FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t=1.1 R_{A} C$, at the end of which time the voltage equals $2 / 3 V_{C C}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 2 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

$V_{C C}=5 \mathrm{~V}$
TIME $=0.1 \mathrm{~ms} / \mathrm{DIV}$.
$\mathrm{R}_{\mathrm{A}}=9.1 \mathrm{k} \Omega$
Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.
FIGURE 2. Monostable Waveforms
During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least $10 \mu \mathrm{~s}$ before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to $\mathrm{V}_{\mathrm{CC}}$ to avoid any possibility of false triggering.
Figure 3 is a nomograph for easy determination of R, C values for various time delays.
NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.


TL/H/7851-7
FIGURE 3. Time Delay

## ASTABLE OPERATION

If the circuit is connected as shown in Figure 4 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_{A}+R_{B}$ and discharges through $\mathrm{R}_{\mathrm{B}}$. Thus the duty cycle may be precisely set by the ratio of these two resistors.


TL/H/7851-8
FIGURE 4. Astable
In this mode of operation, the capacitor charges and discharges between $1 / 3 \mathrm{~V}_{\mathrm{CC}}$ and $2 / 3 \mathrm{~V}_{\mathrm{CC}}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

## Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.


TL/H/7851-9

## $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ <br> Top Trace: Output 5V/Div. <br> TIME $=20 \mu \mathrm{~s} /$ DIV. Bottom Trace: Capacitor Voltage 1V/Div.

$\mathrm{R}_{\mathrm{A}}=3.9 \mathrm{k} \Omega$
$\mathrm{R}_{\mathrm{B}}=3 \mathrm{k} \Omega$
$\mathrm{C}=0.01 \mu \mathrm{~F}$
FIGURE 5. Astable Waveforms
The charge time (output high) is given by:

$$
t_{1}=0.693\left(R_{A}+R_{B}\right) C
$$

And the discharge time (output low) by:

$$
\mathrm{t}_{2}=0.693\left(\mathrm{R}_{\mathrm{B}}\right) \mathrm{C}
$$

Thus the total period is:

$$
\mathrm{T}=\mathrm{t}_{1}+\mathrm{t}_{2}=0.693\left(\mathrm{R}_{\mathrm{A}}+2 \mathrm{R}_{\mathrm{B}}\right) \mathrm{C}
$$

The frequency of oscillation is:

$$
f=\frac{1}{T}=\frac{1.44}{\left(R_{A}+2 R_{B}\right) C}
$$

Figure 6 may be used for quick determination of these RC values.
The duty cycle is: $\quad D=\frac{R_{B}}{R_{A}+2 R_{B}}$


FIGURE 6. Free Running Frequency

## FREQUENCY DIVIDER

The monostable circuit of Figure 1 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 7 shows the waveforms generated in a divide by three circuit.

$\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$
Top Trace: Input 4V/Div.
TIME $=20 \mu \mathrm{~s} /$ DIV. Middle Trace: Output 2V/Div.
$\mathrm{R}_{\mathrm{A}}=9.1 \mathrm{k} \Omega \quad$ Bottom Trace: Capacitor 2V/Div.
$\mathrm{C}=0.01 \mu \mathrm{~F}$

## FIGURE 7. Frequency Divider

## PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5 . Figure 8 shows the circuit, and in Figure 9 are some waveform examples.


TL/H/7851-12
FIGURE 8. Pulse Width Modulator


TL/H/7851-13
$\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$
Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.
$\mathrm{TIME}=0.2 \mathrm{~ms}$
$\mathrm{R}_{\mathrm{A}}=9.1 \mathrm{k} \Omega$
$R_{\mathrm{A}}=9.1 \mathrm{k} \Omega$
$\mathrm{C}=0.01 \mu \mathrm{~F}$
FIGURE 9. Pulse Width Modulator

## PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 10, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 11 shows the waveforms generated for a triangle wave modulation signal.

Applications Information (Continued)


TL/H/7851-14
FIGURE 10. Pulse Position Modulator


TL/H/7851-15
$\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$
TIME $=0.1 \mathrm{~ms} /$ DIV .
$\mathrm{R}_{\mathrm{A}}=3.9 \mathrm{k} \Omega$
$\mathrm{R}_{\mathrm{B}}=3 \mathrm{k} \Omega$
$\mathrm{R}=0.01 \mu \mathrm{~F}$
FIGURE 11. Pulse Position Modulator

## LINEAR RAMP

When the pullup resistor, $R_{A}$, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 12 shows a circuit configuration that will perform this function.


FIGURE 12
Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$
\begin{gathered}
T=\frac{2 / 3 V_{C C} R_{E}\left(R_{1}+R_{2}\right) C}{R_{1} V_{C C}-V_{B E}\left(R_{1}+R_{2}\right)} \\
V_{B E} \cong 0.6 V
\end{gathered}
$$


$\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$
Top Trace: Input 3V/Div.
TIME $=20 \mu \mathrm{~s} /$ DIV. Middle Trace: Output 5V/Div.
$\mathrm{R}_{1}=47 \mathrm{k} \Omega \quad$ Bottom Trace: Capacitor Voltage 1V/Div.
$\mathrm{R}_{2}=100 \mathrm{k} \Omega$
$\mathrm{R}_{\mathrm{E}}=2.7 \mathrm{k} \Omega$
$\mathrm{C}=0.01 \mu \mathrm{~F}$
FIGURE 13. Linear Ramp
50\% DUTY CYCLE OSCILLATOR
For a $50 \%$ duty cycle, the resistors $R_{A}$ and $R_{B}$ may be connected as in Figure 14. The time period for the out-

Applications Information (Continued)
put high is the same as previous, $t_{1}=0.693 R_{A} C$. For the output low it is $\mathrm{t}_{2}=$

$$
\left[\left(R_{A} R_{B}\right) /\left(R_{A}+R_{B}\right)\right] C \ln \left[\frac{R_{B}-2 R_{A}}{2 R_{B}-R_{A}}\right]
$$

Thus the frequency of oscillation is $f=\frac{1}{t_{1}+t_{2}}$


TL/H/7851-18
FIGURE 14. 50\% Duty Cycle Oscillator
Physical Dimensions inches (millimeters)


Metal Can Package (H)
Order Number LM555H or LM555CH
NS Package Number H08C



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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
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| :---: | :---: | :---: | :---: |

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Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
$7 V$
Operating Free Air Temperature Range
DM54LS and 54LS
DM74LS
Storage Temperature Range
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter |  | DM54LS74A |  |  | DM74LS74A |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Nom | Max | Min | Nom | Max |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High Level Input Voltage |  | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low Level Input Voltage |  |  |  | 0.7 |  |  | 0.8 | V |
| IOH | High Level Output Current |  |  |  | -0.4 |  |  | -0.4 | mA |
| $\mathrm{l}_{\mathrm{OL}}$ | Low Level Output Current |  |  |  | 4 |  |  | 8 | mA |
| $\mathrm{f}_{\text {CLK }}$ | Clock Frequency (Note 2) |  | 0 |  | 25 | 0 |  | 25 | MHz |
| $\mathrm{f}_{\mathrm{CLK}}$ | Clock Frequency (Note 3) |  | 0 |  | 20 | 0 |  | 20 | MHz |
| $t_{W}$ | Pulse Width (Note 2) | Clock High | 18 |  |  | 18 |  |  | ns |
|  |  | Preset Low | 15 |  |  | 15 |  |  |  |
|  |  | Clear Low | 15 |  |  | 15 |  |  |  |
| $t_{W}$ | Pulse Width (Note 3) | Clock High | 25 |  |  | 25 |  |  | ns |
|  |  | Preset Low | 20 |  |  | 20 |  |  |  |
|  |  | Clear Low | 20 |  |  | 20 |  |  |  |
| tsu | Setup Time (Notes 1 and 2) |  | $20 \uparrow$ |  |  | $20 \uparrow$ |  |  | ns |
| tsu | Setup Time (Notes 1 and 3) |  | $25 \uparrow$ |  |  | $25 \uparrow$ |  |  | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time (Note 1 and 4) |  | $0 \uparrow$ |  |  | $0 \uparrow$ |  |  | ns |
| $\mathrm{T}_{\mathrm{A}}$ | Free Air Operating Temperature |  | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

Note 1: The symbol ( $\uparrow$ ) indicates the rising edge of the clock pulse is used for reference.
Note 2: $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 3: $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.
Note 4: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$.



54LS74/DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered
Physical Dimensions inches (millimeters) (Continued)

-Lead Ceramic Flat Package (W)
Order Number 54LS74FMQB or DM54LS74AW
NS Package Number W14B

## LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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| :---: | :---: | :---: | :---: |

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## Simple and Easy

- Easy operation.
- LED display for incident level.
- Long sensing distance ( 200 mm with reflective models) - double that of standard E3X-NA models.
- High resolution - 7 times that of previous models (e.g., E3X-NA11).
- "Easy wiring" connector.
- Same design as E3X-DA-N Digital Fiber Amplifier.


## Ordering Information: Amplifier Units, Connectors and Accessories

## Amplifier Units

## Amplifier Units with Cables



## Amplifier Units with Connectors

| Item | Appearance | Applicable Connector (order separately) |  | Control output | Model |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | NPN output | PNP output |
| Standard models |  | Master | E3X-CN11 |  | ON/OFF output | E3X-NA6 | E3X-NA8 |
|  |  | Slave | E3X-CN12 |  |  |  |
| Water-resistant models (M8 connectors) |  | $\begin{aligned} & \text { XS3F-M } \\ & \text { XS3F-M } \end{aligned}$ | $\begin{aligned} & 0 \square-A \\ & 0 \square-A \end{aligned}$ | E3X-NA14V |  | E3X-NA44V |

## Amplifier Unit Connectors (Order Separately)

Note Stickers for Connectors are included as accessories.

| Item | Appearance | Cable length | No. of conductors | Model |
| :--- | :---: | :--- | :--- | :--- |
| Master Connector | 2 m | 3 | E3X-CN11 |  |
|  | Slave Connector |  | 1 | E3X-CN12 |

## Combining Amplifier Units and Connectors

Refer to the following tables when placing an order. Basically, Amplifier Units and Connectors are sold separately.

| Amplifier Units |  |  |
| :---: | :---: | :---: |
| Type | NPN | PNP |
| Standard models | E3X-NA6 | E3X-NA8 |$+$| Applicable Connectors (Order Separately) |  |
| :--- | :--- | :--- |
| Master Connector | Slave Connector |
| E3X-CN11 (3-wire) | E3X-CN12 (1-wire) |



## Sensor I/O Connectors (Order Separately)

| Size | Cable specifications | Appearance | Cable type |  | Model |
| :---: | :---: | :---: | :---: | :---: | :---: |
| M8 | Standard cable | Straight connector | 2 m | Four-core cable | XS3F-M421-402-A |
|  |  |  | 5 m |  | XS3F-M421-405-A |
|  |  | L-shaped connector | 2 m |  | XS3F-M422-402-A |
|  |  |  | 5 m |  | XS3F-M422-405-A |

## Accessories (Order Separately)

## Mounting Brackets

| Appearance | Applicable <br> models | Model | Quantity |
| :---: | :--- | :--- | :--- |
|  | E3X-NA $\square$ <br> E3X-NA $\square$ <br> E3X-NAG $\square$ | E39-L143 | 1 |
|  |  | E3X-NA $\square \mathrm{V}$ | E39-L148 |

## End Plate

| Appearance | Model | Quantity |
| :--- | :--- | :--- |
|  | PFP-M | 1 |

## Specifications: Amplifier Units

Ratings/Characteristics

| Item |  | Amplifier Units with Cables |  |  |  | Amplifier Units with Connectors |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Standard models | High-speed detection models | Mark-detecting models | Water-resistant models | Standard models | Water-resistant models (M8 connectors) |
| Output type | NPN output | E3X-NA11 | E3X-NA11F | E3X-NAG11 | E3X-NA11V | E3X-NA6 | E3X-NA14V |
|  | PNP output | E3X-NA41 | E3X-NA41F | E3X-NAG41 | E3X-NA41V | E3X-NA8 | E3X-NA44V |
| Light source (wavelength) |  | Red LED (680 nm) |  | $\begin{aligned} & \text { Green LED } \\ & (520 \mathrm{~nm}) \end{aligned}$ | Red LED (680 nm) |  |  |
| Supply voltage |  | 12 to 24 VDC $\pm 10 \%$, ripple (p-p): $10 \%$ max. |  |  |  |  |  |
| Current consumption |  | 35 mA max. | 35 mA max. (for 24-VDC power supply) | 35 mA max. |  |  |  |
| Control output |  | NPN/PNP (depends on model) open collector; load current: 50 mA max.; residual voltage: 1 V max.; Light ON/Dark ON mode selector |  |  |  |  |  |
| Response time |  | $200 \mu \mathrm{~s}$ max. for operation <br> and reset respectively <br> (See note.) Operation: <br> $20 \mu \mathrm{~s}$ max. <br> Reset: <br> $30 \mu \mathrm{~s}$ max. |  | $200 \mu \mathrm{~s}$ max. for operation and reset respectively (See note.) |  |  |  |
| Sensitivity adjustment |  | 8-turn sensitivity adjuster (with indicator) |  |  |  |  |  |
| Circuit protection |  | Reverse polarity, output <br> short-circuit, mutual inter- <br> ference prevention (opti- <br> cally synchronized) Reverse polari- <br> ty, output short- <br> circuit |  | Reverse polarity, output short-circuit, mutual interference prevention (optically synchronized) |  |  |  |
| Timer function |  | OFF-delay timer: 40 ms (fixed) |  |  |  |  |  |
| Ambient illumination (receiver side) |  | Incandescent lamp:10,000 lux max.Sunlight: $\quad 20,000$ lux max. |  |  |  |  |  |
| Ambient temperature |  |  |  |  |  |  |  |
| Ambient humidity |  | Operating and storage: $35 \%$ to $85 \%$ (with no condensation) |  |  |  |  |  |
| Insulation resistance |  | $20 \mathrm{M} \Omega$ min. (at 500 VDC ) |  |  |  |  |  |
| Dielectric strength (destruction) |  | $1,000 \mathrm{VAC}$ at $50 / 60 \mathrm{~Hz}$ for 1 minute |  |  |  |  | 500 VAC at $50 / 60 \mathrm{~Hz}$ for 1 minute |
| Vibration resistance (destruction) |  | 10 to 55 Hz with a 1.5-mm double amplitude for 2 hrs each in $\mathrm{X}, \mathrm{Y}$ and Z directions |  |  |  |  |  |
| Shock resistance (destruction) |  | $500 \mathrm{~m} / \mathrm{s}^{2}$, for 3 times each in $\mathrm{X}, \mathrm{Y}$ and Z directions |  |  |  |  |  |
| Enclosure rating |  | IEC60529 IP50 (with Protective Cover attached) |  |  | IEC60529 IP66 (with Protective Cover attached) | IEC60529 IP50 (with Protective Cover attached) | IEC60529 IP66 (with Protective Cover attached) |
| Connection method |  | Pre-wired (standard cable length: 2 m ) |  |  |  | Connector | M8 connector |
| Weight (packed state) |  | Approx. 100 g |  |  | Approx. 110 g | Approx. 55 g | Approx. 65 g |
| Material | Case | Polybutylene terephthalate (PBT) |  |  |  |  |  |
|  | Cover | Polycarbonate |  |  | Polyethersulfone (PES) | Polycarbonate | Polyethersulfone (PES) |
| Accessories |  | Instruction Sheet |  |  |  |  |  |

Note When there are 8 or more Units mounted side-by-side, the response time will be $350 \mu \mathrm{~s}$ max.
Amplifier Unit Connectors

| Item | E3X-CN11 | E3X-CN12 |
| :--- | :--- | :--- |
| Rated current | 2.5 A |  |
| Rated voltage | 50 V | $20 \mathrm{~m} \Omega$ max. (20 mVDC max., 100 mA max.) <br> (The above figure is for connection to the Amplifier Unit and the adjacent Connector. It does not include the con- <br> ductor resistance of the cable.) |
| Contact resistance | 50 times (for connection to the Amplifier Unit and the adjacent Connector) |  |
| Number of insertions <br> (destruction) | Housing | Polybutylene terephthalate (PBT) |
| Material | Contact | Phosphor bronze/gold-plated nickel |
| Weight (packed state) | Approx. 55 g | Approx. 25 g |

## Ordering Information: Fiber Units

## Through-beam Fiber Units

Refer to the end of the following table for notes and precautions.
rree-cur Indicates models that allow free cutting. Models without this mark do not allow free cutting.
: Red light $\square$ : Green light

| Application | Features | Appearance | Applicable Amplifier Unit | Sensing distance (mm) (Values in parentheses: when using the E39-F1 Lens Unit) | Standard object <br> (see notes) <br> (min. sensing <br> object: opaque) <br> 1 | Model | Permissible bending radius |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Long distance | M4 Free-cut |  | E3X-NA $\square$ (V) | $700(2,000)$ | $\begin{aligned} & \hline \text { 1.4-mm dia. } \\ & \text { (0.03-mm dia.) } \end{aligned}$ | E32-T11L | 25 mm |
|  |  |  | E3X-NAG $\square$ | $\square 130(370)$ |  |  |  |
|  |  |  | E3X-NA $\square$ F | $\begin{aligned} & 1 \\ & 1 \\ & 1 \end{aligned}$ | $1.4-\mathrm{mm}$ dia. (0.5-mm dia.) |  |  |
|  | 3-mm dia. | $\underset{3-\mathrm{mm} \text { dia. }}{+i} \rightarrow \infty$ | E3X-NA $\square$ (V) | $700$ | $\begin{aligned} & \text { 1.4-mm dia. } \\ & \text { (0.03-mm dia.) } \end{aligned}$ | E32-T12L |  |
|  |  |  | E3X-NAG $\square$ | $\square 130^{\circ}$ |  |  |  |
|  |  |  | E3X-NA $\square$ F | 210 | $\begin{aligned} & \text { 1.4-mm dia. } \\ & \text { ( } 0.5-\mathrm{mm} \text { dia.) } \\ & \hline \end{aligned}$ |  |  |
|  | M3 | $\begin{gathered} \text { M3 screw } \end{gathered}$ | E3X-NA $\square$ (V) | $200$ | $\begin{aligned} & 0.9-\mathrm{mm} \text { dia. } \\ & \text { (0.03-mm dia.) } \end{aligned}$ | E32-T21L | 10 mm |
|  |  |  | E3X-NAG $\square$ | P40 : |  |  |  |
|  |  |  | E3X-NA $\square$ F | $$ | $\begin{aligned} & \text { 0.9-mm dia. } \\ & \text { (0.2-mm dia.) } \\ & \hline \end{aligned}$ |  |  |
|  | 2-mm dia.; small diameter | $\frac{-\frac{1}{4} \rightarrow \square}{2-\mathrm{mm} \text { dia. }}$ | E3X-NA $\square$ (V) | ${ }_{1}^{200}$ | $\begin{aligned} & 0.9-\mathrm{mm} \text { dia. } \\ & \text { (0.03-mm dia.) } \end{aligned}$ | E32-T22L |  |
|  |  |  | E3X-NAG $\square$ | $\square 40:$ |  |  |  |
|  |  |  | E3X-NA $\square$ F | 60 : | $\begin{array}{\|l\|} \hline \text { 0.9-mm dia. } \\ \text { (0.2-mm dia.) } \\ \hline \end{array}$ |  |  |
|  | M14; with lens; ideal for explo-sion-proof applications |  | E3X-NA $\square$ (V) | C 14,000 | $\begin{aligned} & \hline \text { 10-mm dia. } \\ & \text { (0.1-mm dia.) } \\ & \hline \end{aligned}$ | E32-T17L | 25 mm |
|  |  |  | E3X-NA $\square$ F | $4,200$ | $\begin{aligned} & \text { 10-mm dia. } \\ & \text { (1.5-mm dia.) } \end{aligned}$ |  |  |
| Generalpurpose | M4 Free-cut |  | E3X-NA $\square$ (V) | $400(3,000)$ | $\begin{aligned} & \text { 1.0-mm dia. } \\ & \text { (0.03-mm dia.) } \end{aligned}$ | E32-TC200 | 25 mm |
|  |  |  | E3X-NAG $\square$ | $\begin{array}{llll} \hline & 75 \text { (550) } & \vdots & \vdots \\ & 1 & 1 \end{array}$ |  |  |  |
|  |  |  | E3X-NA $\square$ F | 120 (900) ' ' | $\begin{aligned} & \text { 1.0-mm dia. } \\ & \text { (0.2-mm dia.) } \end{aligned}$ |  |  |
|  | M4 |  | E3X-NA $\square$ (V) | - 280 (2,100) | $\begin{aligned} & \text { 1.0-mm dia. } \\ & \text { ( } 0.03-\mathrm{mm} \text { dia.) } \end{aligned}$ | E32-T11R | 1 mm |
|  |  |  | E3X-NAG $\square$ | 50 (375) ! |  |  |  |
|  |  |  | E3X-NA $\square$ F | 80 (600) ! | $1.0-\mathrm{mm}$ dia. (0.2-mm dia.) |  |  |
|  | 3-mm dia. Free-cut | $\xrightarrow[3-\mathrm{mm} \text { dia. }]{\stackrel{i}{4}} \rightarrow \infty$ | E3X-NA $\square$ (V) | $280!$ | $\begin{aligned} & \text { 1.0-mm dia. } \\ & \text { (0.03-mm dia.) } \end{aligned}$ | E32-T12R |  |
|  |  |  | E3X-NAG $\square$ | $50:$ |  |  |  |
|  |  |  | E3X-NA $\square$ F | $80!$ | $\begin{aligned} & 1.0-\mathrm{mm} \text { dia. } \\ & \text { (0.2-mm dia.) } \end{aligned}$ |  |  |
|  | M3; possible to mount the reflective side-view conversion attachment E39-F5 |  | E3X-NA $\square$ (V) | 360 | $\begin{aligned} & \hline \text { 1.0-mm dia. } \\ & \text { (0.03-mm dia.) } \end{aligned}$ | E32-TC200A | 25 mm |
|  |  |  | E3X-NAG $\square$ | $\sqsupset 65$ |  |  |  |
|  |  |  | E3X-NA $\square$ F | 100 | $\begin{aligned} & 1.0-\mathrm{mm} \text { dia. } \\ & \text { (0.2-mm dia.) } \\ & \hline \end{aligned}$ |  |  |
|  | M3; for detecting minute sensing objects | $\begin{aligned} & \text { M3 screw } \rightarrow \text { dibl} \\ & \text { M } \end{aligned}$ | E3X-NA $\square$ (V) | 100 | $\begin{aligned} & \hline 0.5-\mathrm{mm} \text { dia. } \\ & (0.03-\mathrm{mm} \text { dia. }) \end{aligned}$ | E32-TC200E | 10 mm |
|  |  |  | E3X-NAG■ | 20 : |  |  |  |
|  |  |  | E3X-NA $\square$ F | 130 | $\begin{array}{\|l\|} \hline 0.5-\mathrm{mm} \text { dia. } \\ \text { (0.1-mm dia.) } \end{array}$ |  |  |
|  | M3; small diameter |  | E3X-NA $\square$ (V) | 160 , | $\begin{aligned} & \hline 0.5-\mathrm{mm} \text { dia. } \\ & (0.03-\mathrm{mm} \text { dia.) } \end{aligned}$ | E32-T21R | 1 mm |
|  |  | $\begin{aligned} & \text { M3 screw } \end{aligned}$ | E3X-NAG $\square$ | 12 |  |  |  |
|  |  |  | E3X-NA $\square$ F | 118 | $\begin{array}{\|l\|} \hline \text { 1.0-mm dia. } \\ \text { (0.1-mm dia.) } \\ \hline \end{array}$ |  |  |




| Application | Features | Appearance | Applicable Amplifier Unit | Sensing distance (mm) (Values in parentheses: when using the E39-F1 Lens Unit) | Standard object (mine notes) (mensing object: : opaque) | Model | Permissible bending radius |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{\|l\|} \hline \begin{array}{l} \text { Area } \\ \text { sensing } \end{array} \\ \hline \end{array}$ | Multi-point detection (4-head) |  | E3X-NA $\square$ (V) <br> E3X-NA $\square \mathrm{F}$ | 300 <br> 90 | $2.0-\mathrm{mm}$ dia. <br> (0.03-mm dia.) <br> $2.0-\mathrm{mm}$ dia. <br> ( $0.3-\mathrm{mm}$ dia.) <br> $(0.5-\mathrm{m}$ dia.) | E32-M21 | 25 mm |
|  | Detects in a 30-mm area |  | E3X-NA $\square$ (V) <br> E3X-NAG $\square$ <br> E3X-NA $\square \mathrm{F}$ |  920  <br> $\square 170$   <br>  270  <br>    | $\begin{aligned} & \hline(0.5-\mathrm{mm} \text { dia.) } \\ & * 4 \end{aligned}$ | E32-T16W | 10 mm |
|  | Detects in a 30-mm area |  | E3X-NA $\square$ (V) <br> E3X-NA $\square \mathrm{F}$ | $\prime$ $'$ $\vdots$ <br> $\vdots$ $\vdots$ $\vdots$ <br> 1 $\vdots$ $\vdots$ <br> 200 1 1 |  | E32-T16WR | 1 mm |
|  | Side-view; suitable for applications with limited spatial depth |  | E3X-NA $\square$ (V) <br> E3X-NAG $\square$ <br> E3X-NA $\square \mathrm{F}$ |  | $\begin{aligned} & (0.3-\mathrm{mm} \text { dia.) } \\ & { }_{4} 4 \end{aligned}$ | E32-T16J | 10 mm |
|  | Side-view; suitable for applications with limited spatial depth |  | E3X-NA $\square$ (V) <br> E3X-NA $\square \mathrm{F}$ |  390 <br> 110 $\vdots$ | $\begin{array}{\|l} \hline(0.3-\mathrm{mm} \text { dia. }) \\ { }^{*} 4 \\ \hline \begin{array}{l} (2.0-\mathrm{mm} \text { dia. }) \\ { }^{2} 4 \end{array} \\ \hline \end{array}$ | E32-T16JR | 1 mm |
|  | Suitable for detecting over a $10-\mathrm{mm}$ area; long distance |  | E3X-NA $\square$ (V) <br> E3X-NAG $\square$ <br> E3X-NA $\square$ F |  | $\begin{aligned} & \text { (0.9-mm dia.) } \\ & { }_{*} 4 \end{aligned}$ | E32-T16 | 25 mm |
|  | Stable for detecting minute sensing objects in a wide area; degree of protection: IEC 60529 IP50 |  | E3X-NA $\square$ (V) <br> E3X-NAG $\square$ <br> E3X-NA $\square \mathrm{F}$ |  | $\begin{aligned} & \hline \text { (0.3-mm dia.) } \\ & { }_{* 4} \end{aligned}$ | E32-T16P | 10 mm |
|  | Stable for detecting minute sensing objects in a wide area; degree of protection: IEC60529 IP50 |  | E3X-NA $\square$ (V) <br> E3X-NA $\square F$ | 1 450 <br> 1 $\vdots$ <br> 130 1 | $\begin{array}{\|l\|} \hline \begin{array}{l} \text { (0.3-m dia.) } \\ * 4 \end{array} \\ \hline \begin{array}{l} \text { (2.0-m dia.) } \\ \hline \end{array} \\ \hline \end{array}$ | E32-T16PR | 1 mm |

*1 Teflon is a registered trademark of the Dupont Company and the Mitsui Dupont Chemical Company for their fluoride resin.
*2 For continuous operation, use the products within a temperature range of $-40^{\circ} \mathrm{C}$ to $130^{\circ} \mathrm{C}$.
*3 Indicates the heat-resistant temperature at the fiber tip.
*4 These figures are for a sensing distance of 100 mm . (Diameters of sensing objects are ones at a stationary state.)
Note: 1. The size of standard sensing object is the same as the fiber core diameter (lens diameter for models with lens).
2. The values of the minimum sensing object for E3X-NA $\square(V)$ and E3X-NAG $\square$ through-beam models indicate those obtained where the sensing distance and sensitivity are set to optimum values.
3. The value of the minimum sensing object for E3X-NA $\square \mathrm{F}$ through-beam models indicates that obtained at the rated sensing distance with the sensitivity set to the optimum value.

■ Fiber Units with Reflective Sensors
Refer to the end of the following table for notes and precautions.
Free-cur Indicates models that allow free cutting. Models without this mark do not allow free cutting.
: Red light
$\square$
: Green light


| Application | Features | Appearance | Applicable Amplifier Unit | Sensi | sing distance (mm) *1 | Standard object (see note) (min. sensing object: Gold wire) | Model | Permis- sible bending radius |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Thin fiber | 2.5-mm dia.; with sleeve |  | E3X-NA $\square$ (V) | 150 |  | $\begin{aligned} & \hline 200 \times 200 \\ & (0.01-\mathrm{mm} \text { dia. }) \end{aligned}$ | $\begin{aligned} & \text { E32-DC200B } \\ & \text { E32-DC200B4 } \end{aligned}$ | 25 mm |
|  |  |  | E3X-NAG $\square$ | $\square 25$ ! |  | $\begin{aligned} & 50 \times 50 \\ & (0.1-\mathrm{mm} \text { dia.) } \end{aligned}$ |  |  |
|  |  |  | E3X-NA $\square \mathrm{F}$ | $\square 50$ ' | $\begin{array}{ll} 1 \\ \vdots & \vdots \\ 1 \end{array}$ | $\begin{aligned} & 75 \times 75 \\ & \text { (0.015-mm dia.) } \end{aligned}$ |  |  |
|  | 1.2-mm dia.; with sleeve |  | E3X-NA $\square$ (V) | $\square 36$ ' | ' | $\begin{aligned} & 50 \times 50 \\ & (0.01-\mathrm{mm} \text { dia. }) \end{aligned}$ | $\begin{aligned} & \text { E32-DC200F } \\ & \text { E32-DC200F4 } \end{aligned}$ | 10 mm |
|  |  |  | E3X-NAG $\square$ | 6 1 |  | $\begin{aligned} & \hline 25 \times 25 \\ & (0.1-\mathrm{mm} \text { dia.) } \end{aligned}$ |  |  |
|  |  |  | E3X-NA $\square \mathrm{F}$ | 12 | $\vdots$ | $\begin{aligned} & 25 \times 25 \\ & (0.02-\mathrm{mm} \text { dia. }) \end{aligned}$ |  |  |
|  | 0.8-mm dia.; for detecting minute sensing objects |  | E3X-NA $\square$ (V) | - 10 |  | $\begin{aligned} & \hline 25 \times 25 \\ & (0.01-\mathrm{mm} \text { dia. }) \end{aligned}$ | E32-D33 | 4 mm |
|  |  |  | E3X-NA $\square \mathrm{F}$ | 13.3 |  | $\begin{aligned} & 25 \times 25 \\ & \text { ( } 0.03-\mathrm{mm} \text { dia.) } \end{aligned}$ |  |  |
|  | 0.5-mm dia.; for detecting minute sensing objects |  | E3X-NA $\square$ | 1.5 | ! ' | $\begin{aligned} & 25 \times 25 \\ & (0.01-\mathrm{mm} \text { dia. }) \end{aligned}$ | E32-D331 | 4 mm |
|  |  |  | E3X-NA $\square \mathrm{F}$ | 10.5 |  | $\begin{aligned} & \hline 25 \times 25 \\ & (0.05-\mathrm{mm} \text { dia. }) \end{aligned}$ |  |  |
| Flexible (resists breaking) (R4) | Ideal for mounting on moving sections (R4) | M6 screw | E3X-NA $\square$ (V) | 90 | ! | $\begin{aligned} & \hline 150 \times 150 \\ & (0.01-\mathrm{mm} \text { dia.) } \end{aligned}$ | E32-D11 | 4 mm |
|  |  |  | E3X-NAG $\square$ | ¢ 15 | $\vdots$ | $\begin{aligned} & 25 \times 25 \\ & (0.1-\mathrm{mm} \text { dia.) } \end{aligned}$ |  |  |
|  |  |  | E3X-NA $\square \mathrm{F}$ | 130 ! |  | $\begin{aligned} & 50 \times 50 \\ & (0.015-\mathrm{mm} \text { dia.) } \end{aligned}$ |  |  |
|  |  | M3 screw | E3X-NA $\square$ (V) | 15 : | : | $\begin{aligned} & 25 \times 25 \\ & (0.01-\mathrm{mm} \text { dia. }) \end{aligned}$ | E32-D21 |  |
|  |  |  | E3X-NA $\square \mathrm{F}$ | 15 ! | : | $\begin{aligned} & 25 \times 25 \\ & (0.02-\mathrm{mm} \text { dia. }) \end{aligned}$ |  |  |
|  |  | $\begin{aligned} & =1 \text { fib } \\ & \text { M4 screw } \end{aligned}$ | E3X-NA $\square$ (V) | 15 | ! | $\begin{aligned} & 25 \times 25 \\ & (0.01-\mathrm{mm} \text { dia. }) \end{aligned}$ | E32-D21B |  |
|  |  |  | E3X-NAG $\square$ | 2.4 |  | $\begin{aligned} & 25 \times 25 \\ & (0.1-\mathrm{mm} \text { dia. }) \end{aligned}$ |  |  |
|  |  |  | E3X-NA $\square \mathrm{F}$ | 15 |  | $\begin{aligned} & \hline 25 \times 25 \\ & (0.02-\mathrm{mm} \text { dia. }) \end{aligned}$ |  |  |
|  |  | $\xlongequal[1.5-\mathrm{mm}^{\frac{1}{m}}]{\stackrel{1}{2}}$ | E3X-NA $\square$ (V) | 7 | 1 $\vdots$ $\vdots$ | $\begin{aligned} & 25 \times 25 \\ & (0.01-\mathrm{mm} \text { dia. }) \end{aligned}$ | E32-D22B |  |
|  |  |  | E3X-NA $\square \mathrm{F}$ | 12.3 | $\vdots$ | $\begin{aligned} & 25 \times 25 \\ & (0.02-\mathrm{mm} \text { dia. }) \end{aligned}$ |  |  |



*1 Sensing distance indicates values for white paper.
*2 For continuous operation, use the products within a temperature range of $-40^{\circ} \mathrm{C}$ to $130^{\circ} \mathrm{C}$.
*3 Teflon is a registered trademark of the Dupont Company and the Mitsui Dupont Chemical Company for their fluoride resin.
*4 Indicates the heat-resistant temperature at the fiber tip.
Note The values of the minimum sensing object indicate those obtained at a distance where the smallest object can be sensed with the Reflective Fiber Unit.

## Output Circuits

| Output | Model | Mode selector | Timing chart | State of output transistor | Output circuit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NPN | E3X-NA11 E3XAK E3X-NAG11 E3X-NA11F E3X-NA11V E3X-NA14V | LIGHT ON (L/ON) |  | Light ON | M8 Connector Pin Arrangement <br> Note <br> Pin 2 is not used. |
| PNP | E3X-NA41 E3XXA8 E3X-NAG41 E3X-NA41F E3X-NA41V E3X-NA44V |  |  | Light ON | M8 Connector Pin Arrangement <br> Note <br> Pin 2 is not used. |

## Connectors (Sensor I/O Connectors)



| Classification | Color of cable <br> conductors | Connection <br> pin number | Application |
| :--- | :--- | :--- | :--- |
| DC | Brown | 1 | Power supply <br> $(+$ V) |
|  | White | 2 | --- |
|  | Blue | 3 | Power supply <br> $(0 \mathrm{~V})$ |
|  | Black | 4 | Output |

Note Pin 2 is not used.

## Engineering Data (Typical)

## Parallel Operating Range

At max. sensitivity. (Use for optical axis adjustment at installation.)


## Operating Range

With standard sensing object at max. sensitivity. (Use for the positioning of the object and Sensor.)

E32-DC200


E32-D11L


E32-D11R/D12R


E32-DC200E


E32-D33


E32-L25L


## E3X-NA

Number of Turns of Sensitivity Adjuster vs. Sensing Distance

E32-T11L


E32-D11L


## Sensing Distance vs. Hysteresis

E32-T11L


E32-D11L


## Application

## ■ Wiring Precautions

Read the following before using the Amplifier Unit and Sensor to ensure safety.

## Power Supply Voltage

Do not impose any voltage exceeding the rated voltage on the E3XNA. Do not impose AC power ( 100 VAC) on models that operate with DC. In both cases, the E3X-NA may rupture or burn.

## Load Short-circuits

Do not short-circuit the load connected to the E3X-NA, otherwise the E3X-NA may rupture or burn.

## Polarity

When supplying power to the E3X-NA, make sure that the polarity of the power is correct, otherwise the E3X-NA may rupture or burn.

## Amplifier Units

## Nomenclature



## Installation

## Turning Power ON

The Sensor is ready to operate within 100 ms after the power supply is turned ON. If the Sensor and load are connected to power supplies separately, be sure to turn ON the power supply to the Sensor first.

## Turning Power OFF

Pulses may be output when the power is turned OFF. Always turn OFF the power to the load or the load line first.

## Power Supply Type

A full or half-wave rectifying power supply without a smoothing circuit cannot be used.

## Communications Hole

The hole on the side of the Amplifier Unit is a communications hole for preventing mutual interference when Amplifier Units are mounted side-by-side. The E3X-MC11 Mobile Console (sold separately) cannot be used.
If an excessive amount of light is received via the Sensor, the mutual interference prevention function may not work. In this case, make the appropriate adjustments using the sensitivity adjuster.
The mutual interference prevention function will not operate when the E3X-NA is used side-by-side with E3X-DA-N models.

## No-load Operation

A load must be connected to the E3X-NA during operation, otherwise internal elements may rupture or burn. Always wire through a load.

## Operating Environment

- Do not use the Amplifier Unit or Sensor in places with flammable or explosive gas.
- Do not use the Amplifier Unit or Sensor underwater.
- Do not disassemble, repair, or modify the Amplifier Unit or Sensor.


## Wiring

## Cable

The cable can be extended, provided that the extension wire applied is at least $0.3 \mathrm{~mm}^{2}$ thick and the total distance no more than 100 m . Do not pull the cable with a force exceeding 30N.

## Separation from Power or High-tension Lines

Do not wire power lines or high-tension lines alongside the lines of the Amplifier Unit in the same conduit, otherwise the Amplifier Unit may be damaged or malfunction due to induction. Be sure to wire the lines of the Amplifier Unit separated as far as possible from power lines or high-tension lines or laid in an exclusive, shielded conduit.


## Power Supply

If a standard switching regulator is used as a power supply, the frame ground (FG) terminal and the ground (G) terminal must be grounded, otherwise faulty operation may result from the switching noise of the power supply.

## M8 Metal Connectors (Water-resistant Models)

Turn OFF the power before inserting or removing the connector. Hold the connector cover when inserting or removing the connector. Tighten the fixing screws by hand. Using tools such as pliers may cause damage.
The applicable tightening torque range is 0.3 to $0.4 \mathrm{~N} \cdot \mathrm{~m}$. If tightening is insufficient, the enclosure rating may not be maintained, and vibrations may cause the connector to come loose.

## Mounting

## Joining Amplifier Units

1. Mount the Amplifier Units one at a time onto the DIN track.

2. Slide the Amplifier Units together, line up the clips, and press the Amplifier Units together until they click into place.


## Separating Amplifier Units

Slide Amplifier Units away from each other, and remove from the DIN track one at a time. (Do not attempt to remove Amplifier Units from the DIN track without separating them first.)
Note: 1. The specifications for ambient temperature will vary according to the number of Amplifier Units used together. For details, refer to Ratings/Characteristics.
2. Always turn OFF the power supply before joining or separating Amplifier Units.

## Mounting

1. Mount the front part on the mounting bracket (ordered separately) or a DIN track.
2. Press the back part onto the mounting bracket or the DIN track.

Note Do not mount the back of the Amplifier Unit onto the mounting bracket or the DIN track first, otherwise the mounting strength of the Amplifier Unit may be reduced. Always mount the front of the Amplifier Unit first.


## Dismounting

By pressing the Amplifier Unit in direction (3) and lifting the fiber insertion part in direction (4) as shown in the following diagram, the Amplifier Unit can be dismounted with ease.


When side-mounting using a mounting bracket, secure the mounting bracket to the Amplifier Unit and then mount using M3 screws. Use plain washers of diameter 6 mm or less when mounting


## Adjustment

## Indicators

In addition to an operation indicator (orange), the E3X-NA also has incident level indicators (4 green and 1 red). Use these indicators for optical axis adjustments and maintenance.

| Status of indicators <br> (in L/ON mode) | Operation <br> indicator <br> (in L/ON <br> mode) | Incident level |
| :--- | :--- | :--- | :--- |
| Operation indicator Incident level indicators |  | Approx. <br> 80\% max. of op- <br> erating level |
| Not lit |  |  |

Note The rightmost indicator will be lit even if the incident level is 0 .

## Operating Environment

## Ambient Conditions

If dust or dirt adhere to the hole for optical communications, it may prevent normal communications. Be sure to remove any dust or dirt before using the Units.

## Miscellaneous

## Ratings and Specifications

The ratings and performance specifications for items such as the minimum sensing object and characteristics are based on products taken at random from certain production lots. Use this data as reference only.

## Protective Cover

Be sure to mount the Protective Cover before use.

## Fiber Unit

## Mounting

## Tightening Force

The tightening force applied to the Fiber Unit should be as follows:

## Screw-mounting Model



| Fiber Units | Clamping torque |
| :---: | :---: |
| M3/M4 screw | 0.78 N-m max. |
| M6 screw/ 6-mm dia. cylinder | $0.98 \mathrm{~N} \cdot \mathrm{~m}$ max. |
| 1.5-mm dia. cylinder | 0.2 N-m max. |
| 2-mm dia./3-mm dia. cylinder | 0.29 N•m max. |
| E32-T12F 5-mm dia. Teflon model | 0.78 N.m max |
| E32-D12F 6-mm dia. Teflon model | 0.78 N.m max. |
| E32-T16 | $0.49 \mathrm{~N} \cdot \mathrm{~m}$ max. |
| E32-R21 | 0.59 N•m max. |
| E32-M21 | Up to 5 mm to the tip: $0.49 \mathrm{~N} \cdot \mathrm{~m}$ max. More than 5 mm from the tip: $0.78 \mathrm{~N} \cdot \mathrm{~m}$ max. |
| E32-L25A | 0.78 N•m max. |
| E32-T16P E32-T16PR E32-T24S E32-L24L E32-L25L E32-T16J E32-T16JR | 0.29 N•m max. |
| $\begin{aligned} & \hline \text { E32-T16W } \\ & \text { E32-T16WR } \end{aligned}$ | 0.3 N•m max. |

Use a proper-sized wrench.


## Fiber Connection and Disconnection

The E3X Amplifier Unit has a lock button. Connect or disconnect the fibers to or from the E3X Amplifier Unit using the following procedures:

1. Connection

Open the protective cover, insert the fibers according to the fiber insertion marks on the side of the Amplifier Unit, and lower the lock button.

2. Disconnection

Remove the protective cover and raise the lock button to pull out the fiber.


Note To maintain the fiber properties, confirm that the lock is released before removing the fiber.
3. Precautions for Fiber Connection/Disconnection

Be sure to lock or unlock the lock button within an ambient temperature range between $-10^{\circ} \mathrm{C}$ and $40^{\circ} \mathrm{C}$.

## Cutting Fiber

Insert a fiber into the Fiber Cutter and determine the length of the fiber to be cut.

Press down the Fiber Cutter in a single stroke to cut the fiber.
The cutting holes cannot be used twice. If the same hole is used twice, the cutting face of the fiber will be rough and the sensing distance will be reduced. Always use an unused hole.
Cut a thin fiber as follows:

1. An attachment is temporarily fitted to a thin fiber before shipment.

2. Secure the attachment after adjusting the position of it in the direction indicated by the arrow.

3. Insert the fiber to be cut into the E39-F4.

4. Finished state (proper cutting state)


Note Insert the fiber in the direction indicated by the arrow.

## Connection

Do not pull or press the Fiber Units. The Fiber Units have a withstand force of 9.8 N or 29.4 N maximum (pay utmost attention because the fibers are thin).
Do not bend the Fiber Unit beyond the permissible bending radius given under Specifications: Amplifier Units on page 3.
Do not bend the edge of the Fiber Units (excluding the E32-T $\square$ R and E32-D $\square R$ ).


Do not apply excess force on the Fiber Units.

## Correct



Incorrect


The Fiber Head could be broken by excessive vibration. To prevent this, the following is effective:

## Amplifier Units with Connectors

## Mounting

## Mounting Connectors

1. Insert the Master or Slave Connector into the Amplifier Unit until it clicks into place.

2. Join Amplifier Units together as required after all the Master and Slave Connectors have been inserted.
3. Attach the stickers (provided as accessories) to the sides of Master and Slave Connectors that are not connected to other Connectors.


Note Attach the stickers to the sides with grooves.


## Bending Radius

## E39-F11 Sleeve Bender

The bending radius of the stainless steel tube should be as large as possible. The smaller the bending radius becomes, the shorter the sensing distance will be.
Insert the tip of the stainless steel tube to the Sleeve Bender and bend the stainless steel tube slowly along the curve of the Sleeve Bender (refer to the figure).


## Removing Connectors

1. Slide the slave Amplifier Unit for which the Connector is to be removed away from the rest of the group.
2. After the Amplifier Unit has been separated, press down on the lever on the Connector and remove it. (Do not attempt to remove Connectors without separating them from other Amplifier Units first.)


## Mounting End Plate (PFP-M)

Depending on how it is mounted, an Amplifier Unit may move during operation. In this case, use an End Plate.
Before mounting an End Plate, remove the clip from the master Amplifier Unit using a nipper or similar tool.


The clip can also be removed using the following mechanism, which is incorporated in the construction of the section underneath the clip.

1. Insert the clip to be removed into the slit underneath the clip on another Amplifier Unit.

2. Remove the clip by rotating the Amplifier Unit.


Pull Strengths for Connectors (Including Cables)
E3X-CN11: 30 N max.
E3X-CN12: 12 N max.

## Reflector

## Use of E39-R3 Reflector

Use detergent, etc., to remove any dust or oil from the surfaces where tape is applied. Adhesive tape will not be attached properly if oil or dust remains on the surface.
The E39-R3 cannot be used in places where it is exposed to oil or chemicals.

## E39-F32 $\square$ Protective Spiral Tubes

Insert a fiber to the Protective Spiral Tube from the head connector side (screwed) of the tube.


Push the fiber into the Protective Spiral Tube. The tube should be straight so that the fiber is not twisted when inserted. Then turn the end cap of the spiral tube.


Secure the Protective Spiral Tube on a suitable place with the attached nut.


Use the attached saddle to secure the end cap of the Protective Spiral Tube. To secure the Protective Spiral Tube at a position other than the end cap, apply tape to the tube so that the portion becomes thicker in diameter.


End cap

## E39-F10 Fiber Connector

Mount the Fiber Connector as shown in the following illustrations.


The Fiber Units should be as close as possible when they are connected.
Sensing distance will be reduced by approximately $25 \%$ when fibers are connected.
Only 2.2-mm-dia. fibers can be connected.

## Dimensions

Note All units are in millimeters unless otherwise indicated.

## Amplifier Units

## Amplifier Units with Cables (with Mounting Bracket Attached)



Note: 1. The mounting bracket can also be used on side $A$
2. With these models, a 4-dia., 3-conductor, vinyl-insulated round cable (conductor cross-sectional area: $0.2 \mathrm{~mm}^{2}$; insulation diameter: 1.1 mm ) is used
Standard length: 2 m .
3. The hole for optical communications is for preventing mutual interference. There is no hole for E3X-NA $\square \mathrm{F}$ models.

## Amplifier Units with Cables, Water-resistant Models (with Mounting Bracket Attached)



Note: 1. The mounting bracket can also be used on side $A$.
2. With these models, a 4-dia., 3-conductor, vinyl-insulated round cable (conductor cross-sectional area: $0.2 \mathrm{~mm}^{2}$; in sulation diameter: 1.1 mm ) is used. Standard length: 2 m .

## Amplifier Units with Connectors



Dimensions with Master Connector Connected


Dimensions with Slave Connector Connected


Amplifier Units with Connectors, Water-resistant Models (with Mounting Bracket Attached)


## E3X-NA

## - Amplifier Unit Connectors

## Master Connectors

E3X-CN11


Note: A 4-dia., 3-conductor, vinyl-insulated round cable (conductor cross-sectional area: $0.2 \mathrm{~mm}^{2}$; insulation diameter: 1.1 mm ) is used.

## Slave Connectors

 E3X-CN12

Note: A 2.6-dia., single-conductor, vinyl-insulated round cable (conductor cross-sectional area: $0.2 \mathrm{~mm}^{2}$; insulation diameter: 1.1 mm ) is used.

## Sensor I/O Connectors

Straight Connector (at One End of Cable)
XS3F-M421-402-A (L=2 m)
XS3F-M421-405-A (L=5 m)


L-shaped Connector (at One End of Cable)
XS3F-M422-402-A (L=2 m)
XS3F-M422-405-A (L=5 m)


## Accessories (Order Separately)

## Mounting Bracket for E3X-NA $\square$, E3X-NA $\square$ F, and E3X-NAG $\square$ Models

## E39-L143



Mounting Holes


## Mounting Bracket for E3X-NA $\square$ V Models

E39-L148


Material: Stainless steel (SUS 304)


Mounting Holes
Two, M3


## End Plate



M4 spring washer


## OMRON Corporation

Industrial Automation Company

Application Sensors Division
Sensing Devices and Components Division H.Q.
Shiokoji Horikawa, Shimogyo-ku,
Kyoto, 600-8530 Japan
Printed in Japan
Tel: (81)75-344-7068/Fax: (81)75-344-7107

# omron 

Sense Different,
Make Difference!

## Simple to Use

Just Open It!


You don't need a manual anymore.
Super Manual Fiber Amplifiers
The E3X-NA Series

# The E3X-NA debut! Following on from our best-seller E3X-A/F Amplifiers, OMRON now presents the ultimate in ease and simplicity. 



We were highly praised for the simplicity of the E3X-A/F Fiber Amplifiers when they were released in the ' 90 's. Now, at the beginning of 21st century, we present the E3X-NA Series of Super Manual Fiber Amplifiers. Based on the concept that anyone should be able to use the amplifiers without an instruction manual, we pursued the bare essentials required of manual fiber amplifiers. Removing all unnecessary functions, we achieved simplicity in an amplifier that could be used immediately by anyone. The Millennium Sensor.

## Instinctively Simple

1. Instinctive LED Bar Displays of Light Levels

E3X-NA:
LED Bar Display
The vertical movement of the LED light level and operation display shows


## Previous Manual Amplifier:

Stability and Light Reception Indicators
This method makes the light level far less obvious.

2. The Same "Save-wiring" Connector as the E3X-DA-N

Gang-mount up to 16 Amplifiers

Reduced Wiring and Space Requirements for Power Lines

Example for 5 Amplifiers
E3X-NA Series


Installation work, costs, and space not required for relay connectors.

3. Same Sensing Distance as Previous Long-distance Models (200-mm Reflective Models)

4. Approximately Seven Times the Detection Accuracy

Applied Fiber: E32-T16P (screen fiber) set at 100 mm .

5. Optical Communications to Prevent Mutual Interference for Up to 5 Amplifiers

6. Dimensions and Designs Inherited from the E3X-DA-N Digital Fiber Amplifier


## Selecting State-of-the-Art Fiber Amplifiers

Select the E3X-NA Series of Super Manual Fiber Amplifiers for the Ultimate in Simplicity.


(Representative model: E3X-NA6)

(Representative model: E3X-NAG11)

(Representative model: E3X-NA11F)


- Water-resistant Models (M8 connectors)
(Representative model: E3X-NA14V)

For Complete Functionality, select the E3X-DA-N Series of Digital Fiber Amplifiers


O Water-resistant Models (M8 connectors)
(Representative model: E3X-DA14V)

## A New Series Addition:

## E3X-DA $\square \square$ TW

- Twin Output Models with Two Threshold Settings

- Twin Output Models
- Supports zone outputs with OK/NG judgements


# The E3X-NA Series - a new lineup of Fiber Amplifiers that enable simple manual operation. <br> <br> Ordering Information 

 <br> <br> Ordering Information}

## $\square$ Amplifier Units

Amplifier Units with Cables

| Item | Appearance | Control output | Model |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | NPN output | PNP output |
| Standard models |  | ON/OFF output | E3X-NA11 | E3X-NA41 |
| High-speed detection models |  |  | E3X-NA11F | E3X-NA41F |
| Mark-detecting models |  |  | E3X-NAG11 | E3X-NAG41 |
| Water-resistant models |  |  | E3X-NA11V | E3X-NA41V |

Amplifier Units with Connectors

| Item | Appearance | Applicable Connector (order separately) |  | Control output | Model |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | NPN output | PNP output |
| Standard models |  | Master | E3X-CN11 |  | ON/OFF output | E3X-NA6 | E3X-NA8 |
|  |  | Slave | E3X-CN12 |  |  |  |  |
| Water-resistant models (M8 connectors) |  | $\begin{aligned} & \text { XS3F-N } \\ & \text { XS3F-M } \end{aligned}$ | $\begin{aligned} & 421-40 \square-\mathrm{A} \\ & 422-40 \square-\mathrm{A} \end{aligned}$ | E3X-NA14V |  | E3X-NA44V |  |

Amplifier Unit Connectors (Order Separately)

Sensor I/O Connectors (Order Separately)

| Item | Appearance | Cable length | No. of conductors | Model | Cable specifications | Appearance | Type of cable |  | Model |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Master |  | 2 m | 3 | E3X-CN11 | Standard cable | Straight | 2 m | Four-core cable | XS3F-M421-402-A |
| Connector |  |  |  |  |  |  | 5 m |  | XS3F-M421-405-A |
| Slave |  |  | 1 | E3X-CN12 |  | L-shape | 2 m |  | XS3F-M422-402-A |
| Connector |  |  |  |  |  |  | 5 m |  | XS3F-M422-405-A |

## Combining Amplifier Units and Connectors

When ordering Connector-type Amplifier Units, refer to the following tables. Basically, Amplifier Units and Connectors are sold separately.

| Amplifier Units |  |  |
| :---: | :---: | :---: |
| Type | NPN | PNP |
| Standard models | E3X-NA6 | E3X-NA8 |

$+$

| Applicable Connectors (Order Separately) |  |
| :---: | :---: |
| Master Connector | Slave Connector |
| E3X-CN11 (3-wire) | E3X-CN21 (1-wire) |

When Using 5 Amplifier Units
Amplifier Units (5 Units)
$+\quad 1$ Master Connector +4 Slave Connectors

[^2]
## OmROn

## Photoelectric Sensor with Built-in Amplifier

- Photoelectric Sensor with built-in amplifier is applicable to a wide variety of lines and ensures a longer sensing distance than any other model.
- User-friendly Sensor takes all installation and on-site conditions into consideration.
- Eliminates the influence of installation and on-site conditions, thus increasing the reliability of the line.
- OMRON has been making efforts towards environmental protection by adopting user and environment-friendly measures.
- Greatly saves energy and resources. The economy-oriented age has evolved into the ecology-oriented age.
- Meets a variety of international standards, thus allowing use in any country.

( $\epsilon$


## Ordering Information

## ■ List of Models

| Sensing method | Appearance | Connection method | Sensing distance | Model |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | NPN output | PNP output |
| Through-beam | $\theta \rightarrow \downarrow$ | Pre-wired (see note 3) |  | E3Z-T61 | E3Z-T81 |
|  |  | Connector | $\square 15 \mathrm{~m}$ | E3Z-T66 | E3Z-T86 |
| Retroreflective (with MSR function) | $\square \stackrel{(\text { see note 1) }}{\leftrightarrows}$ | Pre-wired (see note 3) | $4 \mathrm{~m}$ | E3Z-R61 | E3Z-R81 |
|  |  | Connector | 100 mm ) <br> (see note 2) | E3Z-R66 | E3Z-R86 |
| Diffuse-reflective | $\Delta] \leftrightarrows$ | Pre-wired (see note 3) | 5 to 100 mm (wide view) | E3Z-D61 | E3Z-D81 |
|  |  | Connector |  | E3Z-D66 | E3Z-D86 |
|  |  | Pre-wired (see note 3) | , | E3Z-D62 | E3Z-D82 |
|  |  | Connector | $\begin{array}{c:c}1 \mathrm{~m} & \\ & \\ \end{array}$ | E3Z-D67 | E3Z-D87 |

Note: 1. The Reflector is sold separately. Select the Reflector model most suited to the application.
2. The sensing distance specified is possible when the E39-R1S used. Figure in parentheses indicate the minimum required distance between the Sensor and Reflector.
3. Models provided with a $0.5-\mathrm{m}$ cable are available. When ordering, specify the cable length by adding the code " 0.5 M " to the model number (e.g., E3Z-T61 0.5M).

## ■ Nomenclature

## Through-beam Models <br> E3Z-T6 $\square$ Receiver

Retroreflective Models E3Z-R6■

Diffuse-reflective Models E3Z-D6


## ■ Accessories (Order Separately)

## Slit for Through-beam Models

| Slit width | Sensing distance <br> (typical) | Minimum sensing <br> object (typical) | Model | Quantity required | Remarks |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0.5 mm dia. | 50 mm | 0.5 mm dia. | E39-S65A | One each for the <br> emitter and receiver. | These Slits are <br> available for the <br> E3Z-T $\square$ <br> 1 mm dia. |
| 2 mm dia. | 200 mm | 1 mm dia. | E39-S65B |  |  |
| $0.5 \times 10 \mathrm{~mm}$ | 800 mm | 2 mm dia. | E39-S65C |  |  |
| $1 \times 10 \mathrm{~mm}$ | 1 m | 0.7 mm dia. | E39-S65D |  |  |
| $2 \times 10 \mathrm{~mm}$ | 2.2 m | 1.2 mm dia. | E39-S65E |  |  |

## Reflectors for Retroreflective Models

| Name | Sensing distance (typical) | Model | Remarks |
| :---: | :---: | :---: | :---: |
| Reflector | $3 \mathrm{~m}(100 \mathrm{~mm})$ | E39-R1 | Retroreflective models are not provided with Reflectors. <br> The MSR function is available. |
|  | $4 \mathrm{~m}(100 \mathrm{~mm})$ | E39-R1S |  |
|  | $5 \mathrm{~m}(100 \mathrm{~mm})$ (see note 2) | E39-R2 |  |
| Miniature Reflector | $1.5 \mathrm{~m}(50 \mathrm{~mm})$ (see note 2) | E39-R3 |  |
| Tape Reflector | 700 mm (150 mm) (see note 2) | E39-RS1 |  |
|  | $1.1 \mathrm{~m}(150 \mathrm{~mm})$ (see note 2) | E39-RS2 |  |
|  | 1.4 m (150 mm) (see note 2) | E39-RS3 |  |

Note: 1. Figure in parentheses indicates the minimum required distance between the Sensor and Reflector.
2. The actual sensing distance may be reduced to approximately $70 \%$ of the typical sensing distance when using a Reflector other than E39-R1 or E39-R1S.

## Mounting Brackets

| Appearance | Model |
| :--- | :--- |
|  | E39-L104 |
|  | E39-L43 |


| Appearance | Model | Remarks |
| :--- | :--- | :--- |
|  | For Sensor adjustment use. <br> Mounted to the aluminum <br> frame rails of conveyors <br> and adjustable with ease. |  |

Note: If a through-beam model is used, order two Mounting Brackets for the emitter and receiver respectively.

## Sensor I/O Connectors



## Specifications

## ■ Ratings/Characteristics

| Item | Sensing method | Through-beam | Retroreflective with MSR function | Diffuse-reflective |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | NPN output PNP output (see note 3) | E3Z-T61/T66 | E3Z-R61/R66 | E3Z-D61/D66 | E3Z-D62/D67 |
|  |  | E3Z-T81/T86 | E3Z-R81/R86 | E3Z-D81/D86 | E3Z-D82/D87 |
| Sensing distance |  | 15 m | $\begin{aligned} & \hline 4 \mathrm{~m}(100 \mathrm{~mm})^{\star} \\ & \text { (when using E39-R1S) } \\ & 3 \mathrm{~m}(100 \mathrm{~mm})^{*} \\ & \text { (when using E39-R1) } \\ & \hline \end{aligned}$ | White paper $(100 \times 100 \mathrm{~mm}): 100$ mm | White paper $(300 \times 300 \mathrm{~mm})$ : 1 m |
| Standard sensing object |  | Opaque: 12-mm dia. min. | Opaque: 75-mm dia. min. | -- |  |
| Hysteresis |  | --- |  | 20\% max. of setting distance |  |
| Directional angle |  | Both emitter and receiver: 3 to $15^{\circ}$ | 2 to $10^{\circ}$ | --- |  |
| Light source (wave length) |  | Infrared LED (860 nm) | Red LED (680 nm) | Infrared LED (860 nm) |  |
| Power supply voltage |  | 12 to 24 VDC $\pm 10 \%$ including 10\% (p-p) max. ripple |  |  |  |
| Current consumption |  | Emitter: 15 mA Receiver: 20 mA | 30 mA max. |  |  |
| Control output |  | Load power supply voltage: 26.4 V max. <br> Load current: 100 mA max. (Residual voltage: 1 V max.) <br> Open collector output (NPN or PNP depending on model)  <br> L-ON/D-ON selectable  |  |  |  |
| Circuit protection |  | Protection from load short-circuit and reversed power supply connection | Protection from reversed power supply connection, output short-circuit, and mutual interference protection |  |  |
| Response time |  | Operation or reset: 1 ms max . |  |  |  |
| Sensitivity adjustment |  | One-turn adjuster |  |  |  |
| Ambient illumination (receiver side) |  | Incandescent lamp: 3,000 $\ell \times \max$.Sunlight: $\quad 10,000$ ex max. |  |  |  |
| Ambient temperature |  | Operating: $-25^{\circ} \mathrm{C}$ to $55^{\circ} \mathrm{C} /$ Storage: $-40^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ (with no icing or condensation) |  |  |  |
| Ambient humidity |  | Operating: 35\% to 85\%/Storage: 35\% to 95\% (with no condensation) |  |  |  |
| Insulation resistance |  | $20 \mathrm{M} \Omega \mathrm{min}$. at 500 VDC |  |  |  |
| Dielectric strength |  | 1,000 VAC, $50 / 60 \mathrm{~Hz}$ for 1 min |  |  |  |
| Vibration resistance |  | 10 to 55 Hz , 1.5-mm double amplitude or $300 \mathrm{~m} / \mathrm{s}^{2}$ for 2 hours each in $\mathrm{X}, \mathrm{Y}$, and Z directions |  |  |  |
| Shock resistance |  | Destruction: $500 \mathrm{~m} / \mathrm{s}^{2} 3$ times each in $\mathrm{X}, \mathrm{Y}$, and Z directions |  |  |  |
| Degree of protection |  | IP67 (IEC60529) |  |  |  |
| Connection method |  | 500-mm-thick pre-wired cable (standard length: 2 m ) with M8 connector |  |  |  |
| Indicator |  | Operation indicator (orange) <br> Stability indicator (green) <br> Emitter has power indicator (orange) only. |  |  |  |
| Weight (packed state) | Pre-wired cable (2 m) | Approx. 120 g | Approx. 65 g |  |  |
|  | Connector | Approx. 30 g | Approx. 20 g |  |  |
| Material | Case | PBT (polybutylene terephthalate) |  |  |  |
|  | Lens | Methacrylate resin |  |  |  |
| Accessories |  | Instruction manual (The Reflector or Mounting Bracket is not provided with any of the above models.) |  |  |  |

Note: *Figures in parentheses indicate the minimum required distances between the Sensors and Reflectors.

## Engineering Data

## - Parallel Operating Range (Typical)

Through-beam Models
E3Z-T $\square 1$ (T $\square 6)$


Through-beam Models
E3Z-T $\square 1$ (T $\square 6$ ) and Slit


Retroreflective Models E3Z-R $\square \mathbf{1}$ (R $\square 6$ ) and Reflector


## - Operating Range (Typical)



## ■ Excess Gain Ratio vs. Distance (Typical)

## Through-beam Models

E3Z-T $\square 1$ (T $\square 6)$


Retroreflective Models
E3Z-R $\square 1$ (R $\square 6$ ) and Reflector


Diffuse-reflective Models E3Z-D $\square 1$ (D $\square 6)$


Diffuse-reflective Model
E3Z-D $\square 2$ (D $\square 7$ )


## ■ Sensing Object Size vs. Sensing Distance (Typical)

## Diffuse-reflective Models

E3Z-D $\square 1$ (D $\square 6$ )


Diffuse-reflective Models
E3Z-D $\square \mathbf{2}$ (D $\square 7$ )


INA118

## Precision, Low Power INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: $50 \mu \mathrm{~V}$ max
- LOW DRIFT: $0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO $\pm 40 \mathrm{~V}$
- WIDE SUPPLY RANGE: $\pm 1.35$ to $\pm 18 \mathrm{~V}$
- LOW QUIESCENT CURRENT: $350 \mu \mathrm{~A}$
- 8-PIN PLASTIC DIP, SO-8


## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION


## DESCRIPTION

The INA118 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain ( 70 kHz at $\mathrm{G}=100$ ).
A single external resistor sets any gain from 1 to 10,000 . Internal input protection can withstand up to $\pm 40 \mathrm{~V}$ without damage.
The INA118 is laser trimmed for very low offset voltage $(50 \mu \mathrm{~V})$, drift $\left(0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)$ and high common-mode rejection $(110 \mathrm{~dB}$ at $\mathrm{G}=1000)$. It operates with power supplies as low as $\pm 1.35 \mathrm{~V}$, and quiescent current is only $350 \mu \mathrm{~A}$-ideal for battery operated systems.
The INA118 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ temperature range.


## SPECIFICATIONS

## ELECTRICAL

At $T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ unless otherwise noted.

| PARAMETER | CONDITIONS | INA118PB, UB |  |  | INA118P, U |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| INPUT <br> Offset Voltage, RTI Initial vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode Linear Input Voltage Range <br> Safe Input Voltage Common-Mode Rejection | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }} \text { to } \mathrm{T}_{\text {MAX }} \\ \mathrm{V}_{\mathrm{S}}= \pm 1.35 \mathrm{~V} \text { to } \pm 18 \mathrm{~V} \end{gathered}$ $\begin{gathered} V_{\mathrm{CM}}= \pm 10 \mathrm{~V}, \Delta \mathrm{R}_{\mathrm{S}}=1 \mathrm{k} \Omega \\ \mathrm{G}=1 \\ \mathrm{G}=10 \\ \mathrm{G}=100 \\ \mathrm{G}=1000 \end{gathered}$ | $\begin{gathered} (\mathrm{V}+)-1 \\ (\mathrm{~V}-)+1.1 \\ \\ 80 \\ 97 \\ 107 \\ 110 \end{gathered}$ | $\begin{gathered} \pm 10 \pm 50 / \mathrm{G} \\ \pm 0.2 \pm 2 / \mathrm{G} \\ \pm 1 \pm 10 / \mathrm{G} \\ \pm 0.4 \pm 5 / \mathrm{G} \\ 10^{10} \\| 1 \\ 10^{10} \\| 4 \\ (\mathrm{~V}+)-0.65 \\ (\mathrm{~V}-)+0.95 \end{gathered}$ $\begin{gathered} 90 \\ 110 \\ 120 \\ 125 \end{gathered}$ | $\begin{gathered} \pm 50 \pm 500 / \mathrm{G} \\ \pm 0.5 \pm 20 / \mathrm{G} \\ \pm 5 \pm 100 / \mathrm{G} \end{gathered}$ $\pm 40$ | $\begin{gathered} * \\ * \\ \\ \\ 73 \\ 89 \\ 98 \\ 100 \\ \hline \end{gathered}$ | $\begin{gathered} \pm 25 \pm 100 / \mathrm{G} \\ \pm 0.2 \pm 5 / \mathrm{G} \\ * \\ * \\ * \\ * \\ * \\ * \\ \\ * \\ * \\ * \\ * \end{gathered}$ | $\begin{gathered} \pm 125 \pm 1000 / \mathrm{G} \\ \pm 1 \pm 20 / \mathrm{G} \\ \pm 10 \pm 100 / \mathrm{G} \end{gathered}$ | $\begin{gathered} \mu \mathrm{V} \\ \mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\ \mu \mathrm{~V} / \mathrm{V} \\ \mu \mathrm{~V} / \mathrm{mo} \\ \Omega \\| \mathrm{pF} \\ \Omega \\| \mathrm{pF} \\ \mathrm{~V} \\ \mathrm{~V} \\ \mathrm{~V} \\ \\ \mathrm{~dB} \\ \mathrm{~dB} \\ \mathrm{~dB} \\ \mathrm{~dB} \\ \hline \end{gathered}$ |
| BIAS CURRENT vs Temperature |  |  | $\begin{gathered} \pm 1 \\ \pm 40 \end{gathered}$ | $\pm 5$ |  | $\begin{aligned} & * \\ & * \\ & * \end{aligned}$ | $\pm 10$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{pA} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| OFFSET CURRENT vs Temperature |  |  | $\begin{gathered} \pm 1 \\ \pm 40 \end{gathered}$ | $\pm 5$ |  | $\begin{aligned} & * \\ & * \\ & * \end{aligned}$ | $\pm 10$ | $\begin{gathered} \mathrm{nA} \\ \mathrm{pA} /{ }^{\prime} \mathrm{C} \end{gathered}$ |
| NOISE VOLTAGE, RTI $\begin{aligned} & f=10 \mathrm{~Hz} \\ & f=100 \mathrm{~Hz} \\ & f=1 \mathrm{kHz} \\ & f_{B}=0.1 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz} \end{aligned}$ <br> Noise Current $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{f}_{\mathrm{B}}=0.1 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz} \\ & \hline \end{aligned}$ | $\mathrm{G}=1000, \mathrm{R}_{\mathrm{S}}=0 \Omega$ |  | $\begin{gathered} 11 \\ 10 \\ 10 \\ 0.28 \\ \\ 2.0 \\ 0.3 \\ 80 \\ \hline \end{gathered}$ |  |  | $\begin{gathered} * \\ * \\ * \\ * \\ * \\ * \\ * \\ * \\ \hline \end{gathered}$ |  | $n V / \sqrt{\mathrm{Hz}}$ <br> $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ <br> $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ <br> $\mu \vee p-p$ <br> $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ <br> $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ <br> pAp-p |
| GAIN <br> Gain Equation <br> Range of Gain <br> Gain Error <br> Gain vs Temperature $50 \mathrm{k} \Omega$ Resistance ${ }^{(1)}$ Nonlinearity | $\begin{gathered} G=1 \\ G=10 \\ G=100 \\ G=1000 \\ G=1 \\ G=1 \\ G=10 \\ G=100 \\ G=1000 \end{gathered}$ | 1 | $\begin{gathered} 1+\left(50 \mathrm{k} \Omega / \mathrm{R}_{\mathrm{G}}\right) \\ \pm 0.01 \\ \pm 0.02 \\ \pm 0.05 \\ \pm 0.5 \\ \pm 1 \\ \pm 25 \\ \pm 0.0003 \\ \pm 0.0005 \\ \pm 0.0005 \\ \pm 0.002 \end{gathered}$ | $\begin{gathered} 10000 \\ \pm 0.024 \\ \pm 0.4 \\ \pm 0.5 \\ \pm 1 \\ \pm 10 \\ \pm 100 \\ \pm 0.001 \\ \pm 0.002 \\ \pm 0.002 \\ \pm 0.01 \end{gathered}$ | * | * <br> * <br> * <br> * <br> * <br> * <br> * <br> * <br> * <br> * <br> * | $\begin{gathered} * \\ \pm 0.1 \\ \pm 0.5 \\ \pm 0.7 \\ \pm 2 \\ \pm 10 \\ * \\ \pm 0.002 \\ \pm 0.004 \\ \pm 0.004 \\ \pm 0.02 \end{gathered}$ | V/V <br> V/V <br> \% <br> \% <br> \% <br> \% <br> $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ <br> $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ <br> \% of FSR <br> \% of FSR <br> \% of FSR <br> \% of FSR |
| OUTPUT Voltage: Positive Negative Single Supply High Single Supply Low Load Capacitance Stability Short Circuit Current | $\begin{gathered} \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ \mathrm{~V}_{\mathrm{S}}=+2.7 \mathrm{~V} / 0 \mathrm{~V}(2), \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ \mathrm{~V}_{\mathrm{S}}=+2.7 \mathrm{~V} / 0 \mathrm{~V}(2), \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{gathered}$ | $\begin{gathered} (\mathrm{V}+)-1 \\ (\mathrm{~V}-)+0.35 \\ 1.8 \\ 60 \end{gathered}$ | $\begin{gathered} (\mathrm{V}+)-0.8 \\ (\mathrm{~V}-)+0.2 \\ 2.0 \\ 35 \\ 1000 \\ +5 /-12 \end{gathered}$ |  | $\begin{aligned} & * \\ & * \\ & * \\ & * \end{aligned}$ | $\begin{aligned} & * \\ & * \\ & * \\ & * \\ & * \\ & * \\ & * \end{aligned}$ |  | V <br> V <br> V <br> mV pF <br> mA |
| FREQUENCY RESPONSE <br> Bandwidth, -3 dB <br> Slew Rate Settling Time, 0.01\% <br> Overload Recovery | $\begin{gathered} \mathrm{G}=1 \\ \mathrm{G}=10 \\ \mathrm{G}=100 \\ \mathrm{G}=1000 \\ \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{G}=10 \\ \mathrm{G}=1 \\ \mathrm{G}=10 \\ \mathrm{G}=100 \\ \mathrm{G}=1000 \\ 50 \% \text { Overdrive } \end{gathered}$ |  | 800 500 70 7 0.9 15 15 21 210 20 |  |  | $\begin{aligned} & * \\ & * \\ & * \\ & * \\ & * \\ & * \\ & * \\ & * \\ & * \\ & * \\ & * \end{aligned}$ |  | kHz <br> kHz <br> kHz <br> kHz <br> $\mathrm{V} / \mu \mathrm{s}$ <br> $\mu \mathrm{s}$ <br> $\mu \mathrm{S}$ <br> $\mu \mathrm{s}$ <br> $\mu \mathrm{s}$ <br> $\mu \mathrm{s}$ |
| POWER SUPPLY <br> Voltage Range Current | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ | $\pm 1.35$ | $\begin{gathered} \pm 15 \\ \pm 350 \end{gathered}$ | $\begin{gathered} \pm 18 \\ \pm 385 \end{gathered}$ | * | * | * | $\begin{gathered} \mathrm{V} \\ \mu \mathrm{~A} \end{gathered}$ |
| TEMPERATURE RANGE <br> Specification <br> Operating <br> $\theta_{\mathrm{JA}}$ |  | $\begin{aligned} & -40 \\ & -40 \end{aligned}$ | 80 | $\begin{gathered} 85 \\ 125 \end{gathered}$ | $\begin{aligned} & * \\ & * \end{aligned}$ | * | $\begin{aligned} & * \\ & * \end{aligned}$ | $\begin{gathered} { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |

* Specification same as INA118PB, UB.

NOTE: (1) Temperature coefficient of the " $50 \mathrm{k} \Omega$ " term in the gain equation. (2) Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

PIN CONFIGURATION

8-Pin DIP and SO-8


## ABSOLUTE MAXIMUM RATINGS

| Supply Voltage | $\pm 18 \mathrm{~V}$ |
| :---: | :---: |
| Analog Input Voltage Range | $\pm 40 \mathrm{~V}$ |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage Temperature | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Junction Temperature | $\ldots . .+150^{\circ} \mathrm{C}$ |
| Lead Temperature (soldering, 10s) | .. $+300^{\circ} \mathrm{C}$ |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE <br> DRAWING <br> NUMBER(1) | TEMPERATURE <br> RANGE |
| :--- | :---: | :---: | :---: |
| INA118P | 8-Pin Plastic DIP | 006 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| INA118PB | 8-Pin Plastic DIP | 006 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| INA118U | SO-8 Surface-Mount | 182 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| INA118UB | SO-8 Surface-Mount | 182 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

[^3]
## TYPICAL PERFORMANCE CURVES

At $T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, unless otherwise noted.








를

## TYPICAL PERFORMANCE CURVES (CONT)

At $T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, unless otherwise noted.







## TYPICAL PERFORMANCE CURVES (CONT)

At $T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, unless otherwise noted.



INPUT BIAS AND OFFSET CURRENT






## 를

## TYPICAL PERFORMANCE CURVES (CONT)

At $T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}$, unless otherwise noted.



10 $\mu \mathrm{s} / \mathrm{div}$

INPUT-REFERRED NOISE, 0.1 Hz to 10 Hz

$0.1 \mu \mathrm{~V} / \mathrm{div}$

$100 \mu \mathrm{~s} / \mathrm{div}$


## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.
The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of $12 \Omega$ in series with the Ref pin will cause a typical device to degrade to approximately 80 dB CMR $(\mathrm{G}=1)$.

## SETTING THE GAIN

Gain of the INA118 is set by connecting a single external resistor, $\mathrm{R}_{\mathrm{G}}$, connected between pins 1 and 8 :

$$
\begin{equation*}
\mathrm{G}=1+\frac{50 \mathrm{k} \Omega}{\mathrm{R}_{\mathrm{G}}} \tag{1}
\end{equation*}
$$

Commonly used gains and resistor values are shown in Figure 1.
The $50 \mathrm{k} \Omega$ term in Equation 1 comes from the sum of the two internal feedback resistors of $\mathrm{A}_{1}$ and $\mathrm{A}_{2}$. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, $\mathrm{R}_{\mathrm{G}}$, also affects gain. $\mathrm{R}_{\mathrm{G}}$ 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

## DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.
The INA118 exhibits approximately 3 dB peaking at 500 kHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable $+6 \mathrm{~dB} /$ octave due to a response zero. A simple pole at 300 kHz or lower will produce a flat passband unity gain response.

| DESIRED <br> GAIN | $\mathbf{R}_{\mathbf{G}}$ <br> $(\Omega)$ | NEAREST $\mathbf{1 \%} \mathbf{R}_{\mathbf{G}}$ <br> $(\Omega)$ |
| :---: | :---: | :---: |
| 1 | NC | NC |
| 2 | 50.00 k | 49.9 k |
| 5 | 12.50 k | 12.4 k |
| 10 | 5.556 k | 5.62 k |
| 20 | 2.632 k | 2.61 k |
| 50 | 1.02 k | 1.02 k |
| 100 | 505.1 | 511 |
| 200 | 251.3 | 249 |
| 500 | 100.2 | 100 |
| 1000 | 50.05 | 49.9 |
| 2000 | 25.01 | 24.9 |
| 5000 | 10.00 | 10 |
| 10000 | 5.001 | 4.99 |

NC: No Connection.


Also drawn in simplified form:


FIGURE 1. Basic Connections.

## NOISE PERFORMANCE

The INA118 provides very low noise in most applications. For differential source impedances less than $1 \mathrm{k} \Omega$, the INA103 may provide lower noise. For source impedances greater than $50 \mathrm{k} \Omega$, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.
Low frequency noise of the INA118 is approximately $0.28 \mu \mathrm{~V} p-\mathrm{p}$ measured from 0.1 to $10 \mathrm{~Hz}(\mathrm{G} \geq 100)$. This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

## OFFSET TRIMMING

The INA118 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good commonmode rejection.


FIGURE 2. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA118 is extremely highapproximately $10^{10} \Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately $\pm 5 \mathrm{nA}$. High input impedance means that this input bias current changes very little with varying input voltage.
Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the commonmode range of the INA118 and the input amplifiers will saturate.
If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.


FIGURE 3. Providing an Input Common-Mode Current Path.

## INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA118 is from approximately 0.6 V below the positive supply voltage to 1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of amplifiers $\mathrm{A}_{1}$ and $\mathrm{A}_{2}$. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage-see performance curves "Input Common-Mode Range vs Output Voltage".

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA118 will be near 0V even though both inputs are overloaded.

## LOW VOLTAGE OPERATION

The INA118 can be operated on power supplies as low as $\pm 1.35 \mathrm{~V}$. Performance of the INA118 remains excellent with power supplies ranging from $\pm 1.35 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$. Most parameters vary only slightly throughout this supply voltage rangesee typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input commonmode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for a various supply voltages and gains.

## SINGLE SUPPLY OPERATION

The INA118 can be used on single power supplies of +2.7 V to +36 V . Figure 5 shows a basic single supply circuit. The output Ref terminal is connected to ground. Zero differential input voltage will demand an output voltage of 0 V (ground). Actual output voltage swing is limited to approximately 35 mV above ground, when the load is referred to ground as shown. The typical performance curve "Output Voltage vs Output Current" shows how the output voltage swing varies with output current.
With single supply operation, $\mathrm{V}_{\text {IN }}^{+}$and $\mathrm{V}_{\text {IN }}^{-}$must both be 0.98 V above ground for linear operation. You cannot, for instance, connect the inverting input to ground and measure a voltage connected to the non-inverting input.
To illustrate the issues affecting low voltage operation, consider the circuit in Figure 5. It shows the INA118, operating from a single 3 V supply. A resistor in series with the low side of the bridge assures that the bridge output
voltage is within the common-mode range of the amplifier's inputs. Refer to the typical performance curve "Input Com-mon-Mode Range vs Output Voltage" for 3V single supply operation.

## INPUT PROTECTION

The inputs of the INA118 are individually protected for voltages up to $\pm 40 \mathrm{~V}$. For example, a condition of -40 V on one input and +40 V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5 mA . The typical performance curve "Input Bias Current vs Input Overload Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

## INSIDE THE INA118

Figure 1 shows a simplified representation of the INA118. The more detailed diagram shown here provides additional insight into its operation.
Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 1.5 to 5 mA .

The differential input voltage is buffered by $Q_{1}$ and $Q_{2}$ and impressed across $R_{G}$, causing a signal current to flow through $\mathrm{R}_{\mathrm{G}}, \mathrm{R}_{1}$ and $\mathrm{R}_{2}$. The output difference amp, $\mathrm{A}_{3}$, removes the common-mode component of the input signal and refers the output signal to the Ref terminal.

Equations in the figure describe the output voltages of $\mathrm{A}_{1}$ and $\mathrm{A}_{2}$. The $\mathrm{V}_{\mathrm{BE}}$ and IR drop across $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ produce output voltages on $A_{1}$ and $A_{2}$ that are approximately 1 V lower than the input voltages.
$\mathrm{A}_{1}$ Out $=\mathrm{V}_{\mathrm{CM}}-\mathrm{V}_{\mathrm{BE}}-(10 \mu \mathrm{~A} \cdot 25 \mathrm{k} \Omega)-\mathrm{V}_{\mathrm{O}} / 2$
$A_{2}$ Out $=V_{C M}-V_{B E}-(10 \mu A \cdot 25 k \Omega)+V_{\mathrm{O}} / 2$
Output Swing Range $\mathrm{A}_{1}, \mathrm{~A}_{2} ;(\mathrm{V}+)-0.65 \mathrm{~V}$ to $(\mathrm{V}-)+0.06 \mathrm{~V}$
Amplifier Linear Input Range: $(\mathrm{V}+)-0.65 \mathrm{~V}$ to $(\mathrm{V}-)+0.98 \mathrm{~V}$


FIGURE 4. INA118 Simplified Circuit Diagram.


FIGURE 5. Single-Supply Bridge Amplifier.


FIGURE 6. AC-Coupled Instrumentation Amplifier.


FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.


FIGURE 8. Differential Voltage to Current Converter.


FIGURE 9. ECG Amplifier With Right-Leg Drive.

## International IsR Rectifier

- Surface Mount (IRLR120N)
- Straight Lead (IRLU120N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated


## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for throughhole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

IRLR/U120N HEXFET ${ }^{\circledR}$ Power MOSFET


## Absolute Maximum Ratings

|  | Parameter | Max. | Units |
| :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{D}} @ \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ | Continuous Drain Current, $\mathrm{V}_{\mathrm{GS}}$ @ 10V | 10 | A |
| $\mathrm{I}_{\mathrm{D}} @ \mathrm{~T}_{\mathrm{C}}=100^{\circ} \mathrm{C}$ | Continuous Drain Current, $\mathrm{V}_{\mathrm{GS}}$ @ 10V | 7.0 |  |
| $\mathrm{I}_{\text {DM }}$ | Pulsed Drain Current (1) © | 35 |  |
| $\mathrm{P}_{\mathrm{D}} @ \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ | Power Dissipation | 48 | W |
|  | Linear Derating Factor | 0.32 | W/ ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{GS}}$ | Gate-to-Source Voltage | $\pm 16$ | V |
| $\mathrm{E}_{\text {AS }}$ | Single Pulse Avalanche Energy (2) (6) | 85 | mJ |
| $\mathrm{I}_{\text {AR }}$ | Avalanche Current(1) © | 6.0 | A |
| $\mathrm{E}_{\text {AR }}$ | Repetitive Avalanche Energy (1) © | 4.8 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (3) | 5.0 | V/ns |
| $\begin{aligned} & \hline \mathrm{T}_{\mathrm{J}} \\ & \mathrm{~T}_{\mathrm{STG}} \end{aligned}$ | Operating Junction and Storage Temperature Range | -55 to +175 | ${ }^{\circ} \mathrm{C}$ |
|  | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) |  |

Thermal Resistance

|  | Parameter | Typ. | Max. | Units |
| :--- | :--- | :---: | :---: | :---: |
| $R_{\theta J C}$ | Junction-to-Case | - | 3.1 |  |
| $R_{\theta J A}$ | Junction-to-Ambient (PCB mount) ${ }^{* *}$ | - | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\theta \mathrm{JA}}$ | Junction-to-Ambient | - | 110 |  |

Electrical Characteristics $@ \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ (unless otherwise specified)

|  | Parameter | Min. | Typ. | Max. | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {(BR) }{ }^{\text {dss }}}$ | Drain-to-Source Breakdown Voltage | 100 | - | - | V | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=250 \mu \mathrm{~A}$ |
| $\Delta \mathrm{V}_{\text {(BR) }{ }^{\text {dss }} / \Delta \mathrm{T}_{\mathrm{J}}}$ | Breakdown Voltage Temp. Coefficient | - | 0.12 | - | V/ ${ }^{\circ} \mathrm{C}$ | Reference to $25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA}$ |
| $\mathrm{R}_{\text {DS(on) }}$ | Static Drain-to-Source On-Resistance | - | - | 0.185 | W | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A}$ (4) |
|  |  | - | - | 0.225 |  | $\mathrm{V}_{\mathrm{GS}}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A} \oplus$ |
|  |  | - | - | 0.265 |  | $\mathrm{V}_{\mathrm{GS}}=4.0 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=5.0 \mathrm{~A} \mathrm{©}$ |
| $\mathrm{V}_{\mathrm{GS} \text { (th) }}$ | Gate Threshold Voltage | 1.0 | - | 2.0 | V | $\mathrm{V}_{\mathrm{DS}}=\mathrm{V}_{\mathrm{GS}}, \mathrm{I}_{\mathrm{D}}=250 \mu \mathrm{~A}$ |
| $\mathrm{gfs}^{\text {f }}$ | Forward Transconductance | 3.1 | - | - | S | $\mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A}$ © |
| ldss | Drain-to-Source Leakage Current | - | - | 25 | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{DS}}=100 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}$ |
|  |  | - | - | 250 |  | $\mathrm{V}_{\mathrm{DS}}=80 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{~T}_{J}=150^{\circ} \mathrm{C}$ |
| IGSs | Gate-to-Source Forward Leakage | - | - | 100 | nA | $\mathrm{V}_{\mathrm{GS}}=16 \mathrm{~V}$ |
|  | Gate-to-Source Reverse Leakage | - | - | -100 |  | $\mathrm{V}_{\mathrm{GS}}=-16 \mathrm{~V}$ |
| $\mathrm{Q}_{\mathrm{g}}$ | Total Gate Charge | - | - | 20 | nC | $\mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A}$ |
| $\mathrm{Q}_{\mathrm{gs}}$ | Gate-to-Source Charge | - | - | 4.6 |  | $V_{\text {DS }}=80 \mathrm{~V}$ |
| $\mathrm{Q}_{\mathrm{gd}}$ | Gate-to-Drain ("Miller") Charge | - | - | 10 |  | $\mathrm{V}_{\mathrm{GS}}=5.0 \mathrm{~V}$, See Fig. 6 and 13 (4) © |
| $\mathrm{t}_{\text {d(on) }}$ | Turn-On Delay Time | - | 4.0 | - | ns | $\begin{aligned} & \mathrm{V}_{\mathrm{DD}}=50 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A} \\ & \mathrm{R}_{\mathrm{G}}=11 \Omega, \mathrm{~V}_{\mathrm{GS}}=5.0 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{D}}=8.2 \Omega \text {, See Fig. } 10 \text { (4)(6) } \end{aligned}$ |
| $\mathrm{tr}_{\mathrm{r}}$ | Rise Time | - | 35 | - |  |  |
| $\mathrm{t}_{\mathrm{d} \text { (off) }}$ | Turn-Off Delay Time | - | 23 | - |  |  |
| $\mathrm{t}_{\mathrm{f}}$ | Fall Time |  | 22 |  |  |  |
| $L_{D}$ | Internal Drain Inductance | - | 4.5 | - | nH | Between lead, <br> 6 mm (0.25in.) <br> from package <br> and center of die contact(5) |
| Ls | Internal Source Inductance | - | 7.5 | - |  |  |
| $\mathrm{C}_{\text {iss }}$ | Input Capacitance | - | 440 | - | pF | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{DS}}=25 \mathrm{~V} \\ & f=1.0 \mathrm{MHz} \text {, See Fig. } 5 \odot \end{aligned}$ |
| $\mathrm{C}_{\text {oss }}$ | Output Capacitance | - | 97 | - |  |  |
| $\mathrm{C}_{\text {rss }}$ | Reverse Transfer Capacitance | - | 50 | - |  |  |

Source-Drain Ratings and Characteristics

|  | Parameter | Min. | Typ. | Max. | Units | Conditions |
| :--- | :--- | :---: | :---: | :---: | :---: | :--- |
| $I_{\mathrm{S}}$ | Continuous Source Current <br> (Body Diode) | - | - | 10 |  | MOSFET symbol <br> showing the <br> integral reverse <br> $p-n$ <br> $j u n c t i o n ~ d i o d e . ~$ |

## Notes:

(1) Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11)
(2) $\mathrm{V}_{\mathrm{DD}}=25 \mathrm{~V}$, starting $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{L}=4.7 \mathrm{mH}$ $\mathrm{R}_{\mathrm{G}}=25 \Omega$, $\mathrm{I}_{\mathrm{AS}}=6.0 \mathrm{~A}$. (See Figure 12)
(3) $\mathrm{I}_{\mathrm{SD}} \leq 6.0 \mathrm{~A}, \mathrm{di} / \mathrm{dt} \leq 340 \mathrm{~A} / \mu \mathrm{s}, \mathrm{V}_{\mathrm{DD}} \leq \mathrm{V}_{(\mathrm{BR}) \mathrm{DSS}}$, (6) Uses IRL520N data and test conditions. $\mathrm{T}_{\mathrm{J}} \leq 175^{\circ} \mathrm{C}$
** When mounted on 1 " square PCB (FR-4 or G-10 Material ) .
For recommended footprint and soldering techniques refer to application note \#AN-994 2


Fig 1. Typical Output Characteristics


Fig 3. Typical Transfer Characteristics


Fig 2. Typical Output Characteristics


Fig 4. Normalized On-Resistance
Vs. Temperature


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage


Fig 8. Maximum Safe Operating Area

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Fig 9. Maximum Drain Current Vs. Case Temperature


Fig 10a. Switching Time Test Circuit


Fig 10b. Switching Time Waveforms


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit


Fig 12b. Unclamped Inductive Waveforms


Fig 13a. Basic Gate Charge Waveform


Fig 12c. Maximum Avalanche Energy Vs. Drain Current


Fig 13b. Gate Charge Test Circuit
www.irf.com


Fig 14. For N-Channel HEXFETS

## IRLR/U120N

International IER Rectifier

## Package Outline

## TO-252AA Outline

Dimensions are shown in millimeters (inches)


Part Marking Information TO-252AA (D-PARK)

```
EXAMPLE: THIS IS AN IRFR120
        WITH ASSEMBLY
        LOT CODE 9U1P
```



## Package Outline

## TO-251AA Outline

Dimensions are shown in millimeters (inches)


## Part Marking Information <br> TO-251AA (I-PARK)

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY LOT CODE 9U1P
INTERNATIONAL
RECTIFIER
LOGO

## Tape \& Reel Information

## TO-252AA



NOTES

1. OUTLINE CONFORMS TO EIA-481.

# International <br> ISR Rectifier 

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 3223331 EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 441883732020

IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T 3Z2, Tel: (905) 4532200 IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49617296590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39114510111
IR FAR EAST: 171 (K\&H Bldg.) 30-4 Nishi-ikebukuro 3-chome, Toshima-ku, Tokyo Japan Tel: 81339830086 IR SOUTHEAST ASIA: 315 Outram Road, \#10-02 Tan Boon Liat Building, Singapore 16907 Tel: 652218371

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## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

## (Note 5)

Supply Voltage
Power Dissipation (Note 1)
Differential Input Voltage
Input Voltage (Note 2)
Output Short Circuit Duration
Operating Temperature Range
Storage Temperature Range
Junction Temperature
Soldering Information
N-Package (10 seconds)
J- or H-Package (10 seconds)
M-Package
Vapor Phase (60 seconds)
Infrared (15 seconds)
LM741A
$\pm 22 \mathrm{~V}$
500 mW
$\pm 30 \mathrm{~V}$
$\pm 15 \mathrm{~V}$
Continuous
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
$150^{\circ} \mathrm{C}$

$260^{\circ} \mathrm{C}$
$300^{\circ} \mathrm{C}$

$215^{\circ} \mathrm{C}$
$215^{\circ} \mathrm{C}$
LM741E
$\pm 22 \mathrm{~V}$
500 mW
$\pm 30 \mathrm{~V}$
$\pm 15 \mathrm{~V}$
Continuous
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
$100^{\circ} \mathrm{C}$

$260^{\circ} \mathrm{C}$
$300^{\circ} \mathrm{C}$

$215^{\circ} \mathrm{C}$
$215^{\circ} \mathrm{C}$

| LM741 | LM741C |
| :---: | :---: |
| $\pm 22 \mathrm{~V}$ | $\pm 18 \mathrm{~V}$ |
| 500 mW | 500 mW |
| $\pm 30 \mathrm{~V}$ | $\pm 30 \mathrm{~V}$ |
| $\pm 15 \mathrm{~V}$ | $\pm 15 \mathrm{~V}$ |
| Continuous | Continuous |
| $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| $150^{\circ} \mathrm{C}$ | $100^{\circ} \mathrm{C}$ |
|  |  |
| $260^{\circ} \mathrm{C}$ | $260^{\circ} \mathrm{C}$ |
| $300^{\circ} \mathrm{C}$ | $300^{\circ} \mathrm{C}$ |
|  |  |
| $215^{\circ} \mathrm{C}$ | $215^{\circ} \mathrm{C}$ |
| $215^{\circ} \mathrm{C}$ | $215^{\circ} \mathrm{C}$ |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.
ESD Tolerance (Note 6)
400 V
400 V
400 V
400 V

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM741A/LM741E |  |  | LM741 |  |  | LM741C |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{S}} \leq 50 \Omega \\ & \hline \end{aligned}$ |  | 0.8 | 3.0 |  | 1.0 | 5.0 |  | 2.0 | 6.0 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
|  | $\begin{aligned} & \mathrm{T}_{\mathrm{AMIN}} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{AMAX}} \\ & \mathrm{R}_{\mathrm{S}} \leq 50 \Omega \\ & \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\ & \hline \end{aligned}$ |  |  | 4.0 |  |  | 6.0 |  |  | 7.5 | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Average Input Offset Voltage Drift |  |  |  | 15 |  |  |  |  |  |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Offset Voltage Adjustment Range | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}$ | $\pm 10$ |  |  |  | $\pm 15$ |  |  | $\pm 15$ |  | mV |
| Input Offset Current | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 3.0 | 30 |  | 20 | 200 |  | 20 | 200 | nA |
|  | $\mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }}$ |  |  | 70 |  | 85 | 500 |  |  | 300 | nA |
| Average Input Offset Current Drift |  |  |  | 0.5 |  |  |  |  |  |  | $n A /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 30 | 80 |  | 80 | 500 |  | 80 | 500 | nA |
|  | $\mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }}$ |  |  | 0.210 |  |  | 1.5 |  |  | 0.8 | $\mu \mathrm{A}$ |
| Input Resistance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}$ | 1.0 | 6.0 |  | 0.3 | 2.0 |  | 0.3 | 2.0 |  | $\mathrm{M} \Omega$ |
|  | $\begin{aligned} & \mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }} \\ & \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V} \end{aligned}$ | 0.5 |  |  |  |  |  |  |  |  | $\mathrm{M} \Omega$ |
| Input Voltage Range | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  |  |  |  |  | $\pm 12$ | $\pm 13$ |  | V |
|  | $\mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }}$ |  |  |  | $\pm 12$ | $\pm 13$ |  |  |  |  | V |
| Large Signal Voltage Gain | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{S}}= \pm 20 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 15 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \end{aligned}$ | 50 |  |  | 50 | 200 |  | 20 | 200 |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |
|  | $\begin{aligned} & \mathrm{T}_{\mathrm{AMIN}} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{AMAX}}, \\ & \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \\ & \mathrm{~V}_{\mathrm{S}}= \pm 20 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 15 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{S}}= \pm 5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 2 \mathrm{~V} \\ & \hline \end{aligned}$ | $\begin{aligned} & 32 \\ & 10 \\ & \hline \end{aligned}$ |  |  | 25 |  |  | 15 |  |  | $\begin{aligned} & \mathrm{V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \\ & \mathrm{~V} / \mathrm{mV} \end{aligned}$ |




## Physical Dimensions inches (millimeters)



Physical Dimensions inches (millimeters) (Continued)


Physical Dimensions inches (millimeters) (Continued)


## LIFE SUPPORT POLICY

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## LM211, LM311

## Single Comparators

The ability to operate from a single power supply of 5.0 V to 30 V or $\pm 15 \mathrm{~V}$ split supplies, as commonly used with operational amplifiers, makes the LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the $\mathrm{V}_{\mathrm{CC}}$ or the $\mathrm{V}_{\mathrm{EE}}$ supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 V at currents to 50 mA , therefore, the LM211/LM311 can be used to drive relays, lamps or solenoids.

## Features

- $\mathrm{Pb}-$ Free Packages are Available


Single Supply
Split Power Supply with Offset Balance


Input polarity is reversed when GND pin is used as an output.

Ground-Referred Load


Input polarity is reversed when GND pin is used as an output.

Load Referred to Negative Supply


Strobe Capability

Figure 1. Typical Comparator Design Configurations


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## http://onsemi.com



PDIP-8 N SUFFIX CASE 626

SOIC-8
D SUFFIX
CASE 751

PIN CONNECTIONS


## ORDERING \& DEVICE MARKING INFORMATION

See detailed ordering and shipping information and marking information in the package dimensions section on pag 7 of this data sheet.

## LM211, LM311

MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | LM211 | LM311 | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Total Supply Voltage | $\mathrm{V}_{\mathrm{CC}}+\mathrm{V}_{\mathrm{EE}} \mid$ | 36 | 36 | Vdc |
| Output to Negative Supply Voltage | $\mathrm{V}_{\mathrm{O}}-\mathrm{V}_{\mathrm{EE}}$ | 50 | 40 | Vdc |
| Ground to Negative Supply Voltage | $\mathrm{V}_{\mathrm{EE}}$ | 30 | 30 | Vdc |
| Input Differential Voltage | $\mathrm{V}_{\text {ID }}$ | $\pm 30$ | $\pm 30$ | Vdc |
| Input Voltage (Note 2) | $V_{\text {in }}$ | $\pm 15$ | $\pm 15$ | Vdc |
| Voltage at Strobe Pin | - | $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{CC}}-5$ | $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{CC}}-5$ | Vdc |
| Power Dissipation and Thermal Characteristics Plastic DIP <br> Derate Above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\text {日JA }} \\ \hline \end{gathered}$ | $\begin{aligned} & 625 \\ & 5.0 \end{aligned}$ |  | $\begin{gathered} \mathrm{mW} \\ \mathrm{~mW} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -25 to +85 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J} \text { (max) }}$ | +150 | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted) Note 1

| Characteristic | Symbol | LM211 |  |  | LM311 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Input Offset Voltage (Note 3) } \\ & R_{S} \leq 50 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & R_{S} \leq 50 \mathrm{k} \Omega, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \end{aligned}$ | $\mathrm{V}_{10}$ | - | $0.7$ | $\begin{aligned} & 3.0 \\ & 4.0 \end{aligned}$ |  |  | $\begin{gathered} 7.5 \\ 10 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Input Offset Current (Note 3) } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \end{aligned}$ | 10 | - | $1.7$ | $\begin{aligned} & 10 \\ & 20 \end{aligned}$ | - | $1.7$ | $\begin{aligned} & 50 \\ & 70 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Bias Current } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \end{aligned}$ | $I_{\text {IB }}$ | - | $45$ | $\begin{aligned} & 100 \\ & 150 \end{aligned}$ | - |  | $\begin{aligned} & 250 \\ & 300 \end{aligned}$ | nA |
| Voltage Gain | $\mathrm{A}_{V}$ | 40 | 200 | - | 40 | 200 | - | V/mV |
| Response Time (Note 4) |  | - | 200 | - | - | 200 | - | ns |
| Saturation Voltage $\begin{aligned} & \mathrm{V}_{I D} \leq-5.0 \mathrm{mV}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{I D} \leq-10 \mathrm{mV}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}} \geq 4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \\ & \mathrm{~V}_{I D}<\leq 6.0 \mathrm{mV}, \mathrm{I}_{\text {sink }} \leq 8.0 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{ID}}<\leq 10 \mathrm{mV}, \mathrm{I}_{\text {sink }} \leq 8.0 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | $\begin{gathered} 0.75 \\ - \\ 0.23 \end{gathered}$ | $\begin{gathered} 1.5 \\ - \\ 0.4 \end{gathered}$ | - | $\begin{gathered} - \\ 0.75 \\ - \\ 0.23 \end{gathered}$ | $\begin{gathered} - \\ 1.5 \\ - \\ 0.4 \end{gathered}$ | V |
| Strobe "On" Current (Note 5) | Is | - | 3.0 | - | - | 3.0 | - | mA |
| $\begin{aligned} & \text { Output Leakage Current } \\ & \mathrm{V}_{I D} \geq 5.0 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {strobe }}=3.0 \mathrm{~mA} \\ & \mathrm{~V}_{I D} \geq 10 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {strobe }}=3.0 \mathrm{~mA} \\ & \mathrm{~V}_{\text {ID }} \geq 5.0 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \\ & \hline \end{aligned}$ |  | - | $\begin{gathered} 0.2 \\ - \\ 0.1 \end{gathered}$ | $\begin{gathered} 10 \\ - \\ 0.5 \end{gathered}$ | - | $-\overline{-}$ | $\frac{-}{50}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input Voltage Range ( $\mathrm{T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*}$ ) | VICR | -14.5 | $\begin{gathered} -14.7 \\ \text { to } \\ 13.8 \end{gathered}$ | +13.0 | -14.5 | $\begin{gathered} -14.7 \\ \text { to } \\ 13.8 \end{gathered}$ | +13.0 | V |
| Positive Supply Current | Icc | - | +2.4 | +6.0 | - | +2.4 | +7.5 | mA |
| Negative Supply Current | $\mathrm{I}_{\text {EE }}$ | - | -1.3 | -5.0 | - | -1.3 | -5.0 | mA |

*LM211: $\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$ LM311: $T_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$

1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 V supply up to $\pm 15 \mathrm{~V}$ supplies.
2. This rating applies for $\pm 15 \mathrm{~V}$ supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 mA to 5.0 mA .

## LM211, LM311



Figure 2. Circuit Schematic


Figure 3. Input Bias Current versus Temperature


Figure 5. Input Bias Current versus Differential Input Voltage


Figure 4. Input Offset Current versus Temperature


Figure 6. Common Mode Limits versus Temperature


Figure 7. Response Time for Various Input Overdrives


Figure 9. Response Time for Various Input Overdrives


Figure 8. Response Time for Various Input Overdrives


Figure 10. Response Time for Various Input Overdrives


Figure 12. Output Saturation Voltage versus Output Current


Figure 13. Output Leakage Current versus Temperature


Figure 14. Power Supply Current versus Supply Voltage


Figure 15. Power Supply Current versus Temperature

## APPLICATIONS INFORMATION



Figure 16. Improved Method of Adding Hysteresis Without Applying Positive

Feedback to the Inputs


Figure 17. Conventional Technique for Adding Hysteresis

## TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high speed comparator such as the LM211 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with $0.1 \mu \mathrm{~F}$ disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high $(1.0 \mathrm{k} \Omega$ to $100 \mathrm{k} \Omega$ ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM211 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 16.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a $0.01 \mu \mathrm{~F}$ capacitor ( C 1 ) between Pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 16. For the fastest response time, tie both balance pins to $\mathrm{V}_{\mathrm{CC}}$.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor ( C 2 ) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R 2 of the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = $10 \mathrm{k} \Omega$, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM211 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM211, and a $0.01 \mu \mathrm{~F}$ capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM211.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 17, the feedback resistor of $510 \mathrm{k} \Omega$ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than $100 \Omega$, such as $50 \mathrm{k} \Omega$, it would not be practical to simply increase the value of the positive feedback resistor proportionally above $510 \mathrm{k} \Omega$ to maintain the same amount of hysteresis.
When both inputs of the LM211 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM211 so that positive feedback would be disruptive, the circuit of Figure 16 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 mV to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz . The positive-feedback signal across the $82 \Omega$ resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the $5.0 \mathrm{k} \Omega$ pot and $3.0 \mathrm{k} \Omega$ resistor as shown.

## LM211, LM311



Figure 18. Zero-Crossing Detector Driving CMOS Logic


Figure 19. Relay Driver with Strobe Capability

ORDERING INFORMATION

| Device | Package | Shipping ${ }^{\dagger}$ |
| :---: | :---: | :---: |
| LM211D | SOIC-8 | 98 Units / Rail |
| LM211DR2 | SOIC-8 |  |
| LM211DR2G | $\begin{gathered} \text { SOIC-8 } \\ \text { (Pb-Free) } \end{gathered}$ |  |
| LM311D | SOIC-8 | 2500 Units / Reel |
| LM311DG | $\begin{gathered} \hline \text { SOIC-8 } \\ \text { (Pb-Free) } \end{gathered}$ | 98 Units / Rail |
| LM311DR2 | SOIC-8 | 2500 Units / Reel |
| LM311DR2G | $\begin{gathered} \text { SOIC-8 } \\ \text { (Pb-Free) } \end{gathered}$ |  |
| LM311N | PDIP-8 | 50 Units / Rail |
| LM311NG | $\begin{gathered} \hline \text { PDIP-8 } \\ \text { (Pb-Free) } \end{gathered}$ |  |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS


$x \quad=2$ or 3
A = Assembly Location
WL, L = Wafer Lot
YY, $Y=$ Year
WW, W = Work Week

## LM211, LM311

## PACKAGE DIMENSIONS

PDIP-8
N SUFFIX
CASE 626-05
ISSUE L


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)
3. DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982.

| DIM | MILLII | TERS |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC |  | 0.300 BSC |  |
| M | --- | $10^{\circ}$ | --- | $10^{\circ}$ |
| N | 0.76 | 1.01 | 0.030 | 0.040 |

## LM211, LM311

SOIC-8
D SUFFIX
CASE 751-07
ISSUE AC


## SOLDERING FOOTPRINT*


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Datasheets for electronics components.

## MC78XX/LM78XX/MC78XXA 3-Terminal 1A Positive Voltage Regulator

## Features

- Output Current up to 1 A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection


## Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.


## Internal Block Digram



Rev. 1.0.1

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage (for $\mathrm{VO}=5 \mathrm{~V}$ to 18 V ) <br> (for $\mathrm{VO}=24 \mathrm{~V}$ ) | $\mathrm{VI}_{\mathrm{I}}$ | 35 | V |
| Thermal Resistance Junction-Cases (TO-220) | $\mathrm{V}_{\mathrm{I}}$ | 40 | V |
| Thermal Resistance Junction-Air (TO-220) | $\mathrm{R}_{\theta \mathrm{JC}}$ | 5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature Range | $\mathrm{R}_{\theta \mathrm{JA}}$ | 65 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | TOPR | $0 \sim+125$ | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=10 \mathrm{~V}, \mathrm{CI}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7805/LM7805 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 4.8 | 5.0 | 5.2 | V |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{Io} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V}_{\mathrm{I}}=7 \mathrm{~V} \text { to } 20 \mathrm{~V} \end{aligned}$ |  | 4.75 | 5.0 | 5.25 |  |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VO}=7 \mathrm{~V}$ to 25 V | - | 4.0 | 100 | mV |
|  |  |  | $\mathrm{VI}=8 \mathrm{~V}$ to 12 V | - | 1.6 | 50 |  |
| Load Regulation (Note1) | Regload | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{IO}=5.0 \mathrm{~mA}$ to 1.5 A | - | 9 | 100 | mV |
|  |  |  | $\begin{aligned} & \mathrm{IO}=250 \mathrm{~mA} \text { to } \\ & 750 \mathrm{~mA} \end{aligned}$ | - | 4 | 50 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0A |  | - | 0.03 | 0.5 | mA |
|  |  | V I $=7 \mathrm{~V}$ to 25 V |  | - | 0.3 | 1.3 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}^{\text {a }}+25^{\circ} \mathrm{C}$ |  | - | 42 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{VO}=8 \mathrm{~V} \text { to } 18 \mathrm{~V} \end{aligned}$ |  | 62 | 73 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 15 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | V I $=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 230 | - | mA |
| Peak Current | IPK | $\mathrm{T}_{\mathrm{J}=+25^{\circ} \mathrm{C}}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{o}}$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7806)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=11 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7806 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | 5.75 | 6.0 | 6.25 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V}=8.0 \mathrm{~V} \text { to } 21 \mathrm{~V} \end{aligned}$ |  | 5.7 | 6.0 | 6.3 | V |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=8 \mathrm{~V}$ to 25 V | - | 5 | 120 | mV |
|  |  |  | $\mathrm{VI}=9 \mathrm{~V}$ to 13 V | - | 1.5 | 60 |  |
| Load Regulation (Note1) | Regload | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.5 A | - | 9 | 120 | mV |
|  |  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 A | - | 3 | 60 |  |
| Quiescent Current | IQ | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l} Q$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1 A |  | - | - | 0.5 | mA |
|  |  | $\mathrm{VI}=8 \mathrm{~V}$ to 25 V |  | - | - | 1.3 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 45 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{VI}=9 \mathrm{~V} \text { to } 19 \mathrm{~V} \end{aligned}$ |  | 59 | 75 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 19 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7808)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=14 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7808 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 7.7 | 8.0 | 8.3 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V}_{\mathrm{I}}=10.5 \mathrm{~V} \text { to } 23 \mathrm{~V} \end{aligned}$ |  | 7.6 | 8.0 | 8.4 | V |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=10.5 \mathrm{~V}$ to 25 V | - | 5.0 | 160 | mV |
|  |  |  | $\mathrm{VI}=11.5 \mathrm{~V}$ to 17 V | - | 2.0 | 80 |  |
| Load Regulation (Note1) | Regload | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ | $\mathrm{IO}=5.0 \mathrm{~mA}$ to 1.5 A | - | 10 | 160 | mV |
|  |  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA | - | 5.0 | 80 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 0.05 | 0.5 | mA |
|  |  | $\mathrm{VI}=10.5 \mathrm{~A}$ to 25 V |  | - | 0.5 | 1.0 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | $\mathrm{V} N$ | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 52 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{~V}$ I $=11.5 \mathrm{~V}$ to 21.5 V |  | 56 | 73 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 17 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 230 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7809)

(Refer to test circuit $, 0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=15 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7809 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 8.65 | 9 | 9.35 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V}=11.5 \mathrm{~V} \text { to } 24 \mathrm{~V} \end{aligned}$ |  | 8.6 | 9 | 9.4 | V |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=11.5 \mathrm{~V}$ to 25 V | - | 6 | 180 | mV |
|  |  |  | $\mathrm{V}=12 \mathrm{~V}$ to 17 V | - | 2 | 90 |  |
| Load Regulation (Note1) | Regload | $\mathrm{T}=+25^{\circ} \mathrm{C}$ | $\mathrm{lO}=5 \mathrm{~mA}$ to 1.5A | - | 12 | 180 | mV |
|  |  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA | - | 4 | 90 |  |
| Quiescent Current | IQ | $\mathrm{T}_{\mathrm{J}=+25^{\circ} \mathrm{C}}$ |  | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l} \mathrm{Q}$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0A |  | - | - | 0.5 | mA |
|  |  | $\mathrm{VI}=11.5 \mathrm{~V}$ to 26 V |  | - | - | 1.3 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 58 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{VI}=13 \mathrm{~V} \text { to } 23 \mathrm{~V} \end{aligned}$ |  | 56 | 71 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 17 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7810)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=16 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7810 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 9.6 | 10 | 10.4 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}_{\mathrm{I}}=12.5 \mathrm{~V} \text { to } 25 \mathrm{~V} \end{aligned}$ |  | 9.5 | 10 | 10.5 | V |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{V}=12.5 \mathrm{~V}$ to 25 V | - | 10 | 200 | mV |
|  |  |  | $\mathrm{VI}=13 \mathrm{~V}$ to 25 V | - | 3 | 100 |  |
| Load Regulation (Note1) | Regload | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{lO}=5 \mathrm{~mA}$ to 1.5 A | - | 12 | 200 | mV |
|  |  |  | $1 \mathrm{O}=250 \mathrm{~mA}$ to 750 mA | - | 4 | 400 |  |
| Quiescent Current | IQ | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 5.1 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | - | 0.5 | mA |
|  |  | $\mathrm{VI}=12.5 \mathrm{~V}$ to 29 V |  | - | - | 1.0 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 58 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{VI}=13 \mathrm{~V} \text { to } 23 \mathrm{~V} \end{aligned}$ |  | 56 | 71 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 17 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7812)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{~V}=19 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7812 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 11.5 | 12 | 12.5 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V} I=14.5 \mathrm{~V} \text { to } 27 \mathrm{~V} \end{aligned}$ |  | 11.4 | 12 | 12.6 | V |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=14.5 \mathrm{~V}$ to 30 V | - | 10 | 240 | mV |
|  |  |  | V I $=16 \mathrm{~V}$ to 22 V | - | 3.0 | 120 |  |
| Load Regulation (Note1) | Regload | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.5 A | - | 11 | 240 | mV |
|  |  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA | - | 5.0 | 120 |  |
| Quiescent Current | IQ | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 5.1 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 0.1 | 0.5 | mA |
|  |  | $\mathrm{VI}=14.5 \mathrm{~V}$ to 30 V |  | - | 0.5 | 1.0 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 76 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{VI}=15 \mathrm{~V} \text { to } 25 \mathrm{~V} \end{aligned}$ |  | 55 | 71 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 18 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | - | 230 | - | mA |
| Peak Current | IPK | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7815)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=23 \mathrm{~V}, \mathrm{CI}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7815 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 14.4 | 15 | 15.6 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V}_{\mathrm{I}}=17.5 \mathrm{~V} \text { to } 30 \mathrm{~V} \end{aligned}$ |  | 14.25 | 15 | 15.75 | V |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=17.5 \mathrm{~V}$ to 30 V | - | 11 | 300 | mV |
|  |  |  | V = $=20 \mathrm{~V}$ to 26 V | - | 3 | 150 |  |
| Load Regulation (Note1) | Regload | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.5 A | - | 12 | 300 | mV |
|  |  |  | $\begin{aligned} & \mathrm{IO}=250 \mathrm{~mA} \text { to } \\ & 750 \mathrm{~mA} \end{aligned}$ | - | 4 | 150 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.2 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0A |  | - | - | 0.5 | mA |
|  |  | V I $=17.5 \mathrm{~V}$ to 30 V |  | - | - | 1.0 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | $\mathrm{V}_{\mathrm{N}}$ | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | - | 90 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & f=120 \mathrm{~Hz} \\ & V_{I}=18.5 \mathrm{~V} \text { to } 28.5 \mathrm{~V} \end{aligned}$ |  | 54 | 70 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 19 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | V I $=35 \mathrm{~V}, \mathrm{~T}_{\text {A }}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7818)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{~V}=27 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7818 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | 17.3 | 18 | 18.7 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V}=21 \mathrm{~V} \text { to } 33 \mathrm{~V} \end{aligned}$ |  | 17.1 | 18 | 18.9 | V |
| Line Regulation (Note1) | Regline | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=21 \mathrm{~V}$ to 33 V | - | 15 | 360 | mV |
|  |  |  | $\mathrm{VI}=24 \mathrm{~V}$ to 30 V | - | 5 | 180 |  |
| Load Regulation (Note1) | Regload | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{lO}=5 \mathrm{~mA}$ to 1.5 A | - | 15 | 360 | mV |
|  |  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA | - | 5.0 | 180 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.2 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{lO}=5 \mathrm{~mA}$ to 1.0A |  | - | - | 0.5 | mA |
|  |  | $\mathrm{VI}=21 \mathrm{~V}$ to 33 V |  | - | - | 1 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | V N | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 110 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{VI}=22 \mathrm{~V} \text { to } 32 \mathrm{~V} \end{aligned}$ |  | 53 | 69 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 22 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{~T} A=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7824)

(Refer to test circuit , $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{~V}=33 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | MC7824 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min. | Typ. | Max. |  |
| Output Voltage | Vo | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | 23 | 24 | 25 |  |
|  |  | $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=27 \mathrm{~V} \text { to } 38 \mathrm{~V} \end{aligned}$ |  | 22.8 | 24 | 25.25 | V |
| Line Regulation (Note1) | Regline | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=27 \mathrm{~V}$ to 38 V | - | 17 | 480 | mV |
|  |  |  | $\mathrm{VI}=30 \mathrm{~V}$ to 36V | - | 6 | 240 |  |
| Load Regulation (Note1) | Regload | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{lO}=5 \mathrm{~mA}$ to 1.5 A | - | 15 | 480 | mV |
|  |  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA | - | 5.0 | 240 |  |
| Quiescent Current | IQ | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 5.2 | 8.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 0.1 | 0.5 | mA |
|  |  | $\mathrm{V}=27 \mathrm{~V}$ to 38 V |  | - | 0.5 | 1 |  |
| Output Voltage Drift | $\Delta \mathrm{VO} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1.5 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\mathrm{f}=10 \mathrm{~Hz}$ to $100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 60 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{VI}=28 \mathrm{~V} \text { to } 38 \mathrm{~V} \end{aligned}$ |  | 50 | 67 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 28 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 230 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7805A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=10 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}$ |  | 4.9 | 5 | 5.1 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=7.5 \mathrm{~V} \text { to } 20 \mathrm{~V} \end{aligned}$ |  | 4.8 | 5 | 5.2 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \mathrm{V} \mathrm{I}=7.5 \mathrm{~V} \text { to } 25 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 5 | 50 | mV |
|  |  | $\mathrm{VI}=8 \mathrm{~V}$ to 12 V |  | - | 3 | 50 |  |
|  |  | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{V}=7.3 \mathrm{~V}$ to 20V | - | 5 | 50 |  |
|  |  |  | $\mathrm{V}=8 \mathrm{~V}$ to 12 V | - | 1.5 | 25 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{lO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 9 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1 A |  | - | 9 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 4 | 50 |  |
| Quiescent Current | IQ | $\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}$ |  | - | 5.0 | 6 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1 A |  | - | - | 0.5 | mA |
|  |  | V I $=8 \mathrm{~V}$ to $25 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{V}_{\mathrm{I}}=7.5 \mathrm{~V}$ to $20 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.8 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{lo}=5 \mathrm{~mA}$ |  | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | V N | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=8 \mathrm{~V} \text { to } 18 \mathrm{~V} \end{aligned}$ |  | - | 68 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 17 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7806A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{~V} \mathrm{I}=11 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 5.58 | 6 | 6.12 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=8.6 \mathrm{~V} \text { to } 21 \mathrm{~V} \end{aligned}$ |  | 5.76 | 6 | 6.24 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \hline \mathrm{V}=8.6 \mathrm{~V} \text { to } 25 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 5 | 60 | mV |
|  |  | $\mathrm{V}=9 \mathrm{~V}$ to 13 V |  | - | 3 | 60 |  |
|  |  | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ | V I $=8.3 \mathrm{~V}$ to 21V | - | 5 | 60 |  |
|  |  |  | $\mathrm{V}=9 \mathrm{~V}$ to 13 V | - | 1.5 | 30 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 9 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1 A |  | - | 4 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 5.0 | 50 |  |
| Quiescent Current | IQ | $\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}$ |  | - | 4.3 | 6 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{IO}=5 \mathrm{~mA}$ to 1 A |  | - | - | 0.5 | mA |
|  |  | $\mathrm{VI}=9 \mathrm{~V}$ to $25 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{V}=8.5 \mathrm{~V}$ to $21 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.8 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=9 \mathrm{~V} \text { to } 19 \mathrm{~V} \end{aligned}$ |  | - | 65 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 17 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7808A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{~V} \mathrm{I}=14 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 7.84 | 8 | 8.16 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=10.6 \mathrm{~V} \text { to } 23 \mathrm{~V} \end{aligned}$ |  | 7.7 | 8 | 8.3 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \mathrm{V}=10.6 \mathrm{~V} \text { to } 25 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 6 | 80 | mV |
|  |  | V I $=11 \mathrm{~V}$ to 17 V |  | - | 3 | 80 |  |
|  |  | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=10.4 \mathrm{~V}$ to 23 V | - | 6 | 80 |  |
|  |  |  | V I $=11 \mathrm{~V}$ to 17 V | - | 2 | 40 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 12 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1 A |  | - | 12 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 5 | 50 |  |
| Quiescent Current | IQ | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 5.0 | 6 | mA |
| Quiescent Current Change | ${ }^{\Delta} \mathrm{Q}$ | $\mathrm{IO}=5 \mathrm{~mA}$ to 1 A |  | - | - | 0.5 | mA |
|  |  | $\mathrm{V}_{\mathrm{I}}=11 \mathrm{~V}$ to 25V, $\mathrm{IO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{V} /=10.6 \mathrm{~V}$ to $23 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.8 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\begin{aligned} & f=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=11.5 \mathrm{~V} \text { to } 21.5 \mathrm{~V} \end{aligned}$ |  | - | 62 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 18 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7809A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=15 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 8.82 | 9.0 | 9.18 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{~V}=11.2 \mathrm{~V} \text { to } 24 \mathrm{~V} \end{aligned}$ |  | 8.65 | 9.0 | 9.35 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \hline \mathrm{V}=11.7 \mathrm{~V} \text { to } 25 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 6 | 90 | mV |
|  |  | $\mathrm{V}=12.5 \mathrm{~V}$ to 19 V |  | - | 4 | 45 |  |
|  |  | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{V}=11.5 \mathrm{~V}$ to 24 V | - | 6 | 90 |  |
|  |  |  | $\mathrm{V}=12.5 \mathrm{~V}$ to 19 V | - | 2 | 45 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.0 \mathrm{~A} \end{aligned}$ |  | - | 12 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 12 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 5 | 50 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.0 | 6.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ | $\mathrm{V}_{\mathrm{I}}=11.7 \mathrm{~V}$ to $25 \mathrm{~V}, \mathrm{~T} \mathrm{~J}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.8 | mA |
|  |  | $\mathrm{VI}=12 \mathrm{~V}$ to $25 \mathrm{~V}, \mathrm{lO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | - | 0.5 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | $\mathrm{V}_{\mathrm{N}}$ | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=12 \mathrm{~V} \text { to } 22 \mathrm{~V} \end{aligned}$ |  | - | 62 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.0 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 17 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant, junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7810A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=16 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 9.8 | 10 | 10.2 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=12.8 \mathrm{~V} \text { to } 25 \mathrm{~V} \end{aligned}$ |  | 9.6 | 10 | 10.4 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \hline \mathrm{V}=12.8 \mathrm{~V} \text { to } 26 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 8 | 100 | mV |
|  |  | $\mathrm{V}=13 \mathrm{~V}$ to 20V |  | - | 4 | 50 |  |
|  |  | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=12.5 \mathrm{~V}$ to 25 V | - | 8 | 100 |  |
|  |  |  | V I $=13 \mathrm{~V}$ to 20V | - | 3 | 50 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 12 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 12 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 5 | 50 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.0 | 6.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{VI}=13 \mathrm{~V}$ to $26 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.5 | mA |
|  |  | $\mathrm{VI}=12.8 \mathrm{~V}$ to 25 V , $\mathrm{IO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | - | 0.5 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{lO}=5 \mathrm{~mA}$ |  | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | $\mathrm{V} N$ | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=14 \mathrm{~V} \text { to } 24 \mathrm{~V} \end{aligned}$ |  | - | 62 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.0 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 17 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{VI}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25{ }^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7812A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=19 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 11.75 | 12 | 12.25 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=14.8 \mathrm{~V} \text { to } 27 \mathrm{~V} \end{aligned}$ |  | 11.5 | 12 | 12.5 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \mathrm{V} \mathrm{I}=14.8 \mathrm{~V} \text { to } 30 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 10 | 120 | mV |
|  |  | V I $=16 \mathrm{~V}$ to 22V |  | - | 4 | 120 |  |
|  |  | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | V I $=14.5 \mathrm{~V}$ to 27 V | - | 10 | 120 |  |
|  |  |  | V I $=16 \mathrm{~V}$ to 22 V | - | 3 | 60 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 12 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 12 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 5 | 50 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.1 | 6.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{VI}=15 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - |  | 0.8 | mA |
|  |  | $\mathrm{VI}=14 \mathrm{~V}$ to $27 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}$ |  | - |  | 0.8 |  |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - |  | 0.5 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{lO}=5 \mathrm{~mA}$ |  | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=14 \mathrm{~V} \text { to } 24 \mathrm{~V} \end{aligned}$ |  | - | 60 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.0 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 18 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{~T} A=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7815A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=23 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 14.7 | 15 | 15.3 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=17.7 \mathrm{~V} \text { to } 30 \mathrm{~V} \end{aligned}$ |  | 14.4 | 15 | 15.6 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \mathrm{V} \mathrm{I}=17.9 \mathrm{~V} \text { to } 30 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 10 | 150 | mV |
|  |  | V I $=20 \mathrm{~V}$ to 26 V |  | - | 5 | 150 |  |
|  |  | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{V}=17.5 \mathrm{~V}$ to 30 V | - | 11 | 150 |  |
|  |  |  | V I $=20 \mathrm{~V}$ to 26 V | - | 3 | 75 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{lO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 12 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 12 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 5 | 50 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.2 | 6.0 | mA |
| Quiescent Current Change | ${ }^{\text {d }} \mathrm{Q}$ | $\mathrm{VI}=17.5 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.8 | mA |
|  |  | $\mathrm{V}=17.5 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | - | 0.5 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{lO}=5 \mathrm{~mA}$ |  | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | VN | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=18.5 \mathrm{~V} \text { to } 28.5 \mathrm{~V} \end{aligned}$ |  | - | 58 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.0 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 19 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7818A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=27 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | 17.64 | 18 | 18.36 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=21 \mathrm{~V} \text { to } 33 \mathrm{~V} \end{aligned}$ |  | 17.3 | 18 | 18.7 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \mathrm{V} \mathrm{I}=21 \mathrm{~V} \text { to } 33 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 15 | 180 | mV |
|  |  | $\mathrm{V}=21 \mathrm{~V}$ to 33V |  | - | 5 | 180 |  |
|  |  | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ | $\mathrm{V}=20.6 \mathrm{~V}$ to 33 V | - | 15 | 180 |  |
|  |  |  | $\mathrm{V}=24 \mathrm{~V}$ to 30V | - | 5 | 90 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 15 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 15 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 7 | 50 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25{ }^{\circ} \mathrm{C}$ |  | - | 5.2 | 6.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ | $\mathrm{VI}=21 \mathrm{~V}$ to $33 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.8 | mA |
|  |  | $\mathrm{VI}=21 \mathrm{~V}$ to 33 V , $\mathrm{IO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | - | 0.5 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{IO}=5 \mathrm{~mA}$ |  | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | V N | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}=+25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=22 \mathrm{~V} \text { to } 32 \mathrm{~V} \end{aligned}$ |  | - | 57 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.0 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 19 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{VI}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7824A)

(Refer to the test circuits. $0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=33 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}$, unless otherwise specified)

| Parameter | Symbol | Conditions |  | Min. | Typ. | Max. | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage | Vo | $\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}$ |  | 23.5 | 24 | 24.5 | V |
|  |  | $\begin{aligned} & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\ & \mathrm{VI}=27.3 \mathrm{~V} \text { to } 38 \mathrm{~V} \end{aligned}$ |  | 23 | 24 | 25 |  |
| Line Regulation (Note1) | Regline | $\begin{aligned} & \mathrm{VI}=27 \mathrm{~V} \text { to } 38 \mathrm{~V} \\ & \mathrm{IO}=500 \mathrm{~mA} \end{aligned}$ |  | - | 18 | 240 | mV |
|  |  | $\mathrm{V}=21 \mathrm{~V}$ to 33V |  | - | 6 | 240 |  |
|  |  | $\mathrm{T} J=+25^{\circ} \mathrm{C}$ | $\mathrm{VI}=26.7 \mathrm{~V}$ to 38 V | - | 18 | 240 |  |
|  |  |  | $\mathrm{V}=30 \mathrm{~V}$ to 36V | - | 6 | 120 |  |
| Load Regulation (Note1) | Regload | $\begin{aligned} & \mathrm{TJ}=+25^{\circ} \mathrm{C} \\ & \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A} \end{aligned}$ |  | - | 15 | 100 | mV |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | 15 | 100 |  |
|  |  | $\mathrm{IO}=250 \mathrm{~mA}$ to 750 mA |  | - | 7 | 50 |  |
| Quiescent Current | IQ | $\mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 5.2 | 6.0 | mA |
| Quiescent Current Change | $\Delta \mathrm{l}$ Q | $\mathrm{VI}=27.3 \mathrm{~V}$ to $38 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | - | 0.8 | mA |
|  |  | $\mathrm{VI}=27.3 \mathrm{~V}$ to $38 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}$ |  | - | - | 0.8 |  |
|  |  | $\mathrm{IO}=5 \mathrm{~mA}$ to 1.0 A |  | - | - | 0.5 |  |
| Output Voltage Drift | $\Delta \mathrm{V} / \Delta \mathrm{T}$ | $\mathrm{lO}=5 \mathrm{~mA}$ |  | - | -1.5 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Output Noise Voltage | $\mathrm{V} N$ | $\begin{aligned} & \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\ & \mathrm{TA}=25^{\circ} \mathrm{C} \end{aligned}$ |  | - | 10 | - | $\mu \mathrm{V} / \mathrm{Vo}$ |
| Ripple Rejection | RR | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\ & \mathrm{VI}=28 \mathrm{~V} \text { to } 38 \mathrm{~V} \end{aligned}$ |  | - | 54 | - | dB |
| Dropout Voltage | VDrop | $\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}$ |  | - | 2.0 | - | V |
| Output Resistance | ro | $\mathrm{f}=1 \mathrm{KHz}$ |  | - | 20 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current | ISC | $\mathrm{VI}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}$ |  | - | 250 | - | mA |
| Peak Current | IPK | $\mathrm{T} J=+25{ }^{\circ} \mathrm{C}$ |  | - | 2.2 | - | A |

## Note:

1. Load and line regulation are specified at constant junction temperature. Change in VO due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Typical Perfomance Characteristics



Figure 1. Quiescent Current


Figure 3. Output Voltage


Figure 2. Peak Output Current


Figure 4. Quiescent Current

## Typical Applications



Figure 5. DC Parameters


Figure 6. Load Regulation


Figure 7. Ripple Rejection


Figure 8. Fixed Output Regulator


$$
l_{0}=\frac{V x x}{R_{1}}+l_{0}
$$

Figure 9. Constant Current Regulator

## Notes:

(1) To specify an output voltage. substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.
(2) $\mathrm{C}_{\boldsymbol{l}}$ is required if regulator is located an appreciable distance from power Supply filter.
(3) Co improves stability and transient response.


$$
\begin{gathered}
\mathrm{I}_{\mathrm{RI}} \geq 5 \mathrm{IQ} \\
\mathrm{VO}=\mathrm{VXX}_{\mathrm{XI}}\left(1+\mathrm{R}_{2} / \mathrm{R}_{1}\right)+\mathrm{I}_{\mathrm{QR}}^{2}
\end{gathered}
$$

Figure 10. Circuit for Increasing Output Voltage

$\mathrm{IRI} \geq 5 \mathrm{lQ}$
$\mathrm{VO}_{\mathrm{O}}=\mathrm{VXX}_{\mathrm{X}}\left(1+\mathrm{R}_{2} / \mathrm{R}_{1}\right)+\mathrm{IQR}_{2}$
Figure 11. Adjustable Output Regulator (7 to 30V)


Figure 12. High Current Voltage Regulator


Figure 13. High Output Current with Short Circuit Protection


Figure 14. Tracking Voltage Regulator


Figure 15. Split Power Supply ( $\pm 15 \mathrm{~V}-1 \mathrm{~A}$ )


Figure 16. Negative Output Voltage Circuit


Figure 17. Switching Regulator

## Mechanical Dimensions

## Package



## Mechancal Dimensions (Continued)

## Package

## D-PAK



Ordering Information

| Product Number | Output Voltage Tolerance | Package | Operating Temperature |
| :---: | :---: | :---: | :---: |
| LM7805CT | $\pm 4 \%$ | TO-220 | $0 \sim+125^{\circ} \mathrm{C}$ |


| Product Number | Output Voltage Tolerance | Package | Operating Temperature |
| :---: | :---: | :---: | :---: |
| MC7805CT | $\pm 4 \%$ | TO-220 | $0 \sim+125^{\circ} \mathrm{C}$ |
| MC7806CT |  |  |  |
| MC7808CT |  |  |  |
| MC7809CT |  |  |  |
| MC7810CT |  |  |  |
| MC7812CT |  |  |  |
| MC7815CT |  |  |  |
| MC7818CT |  |  |  |
| MC7824CT |  |  |  |
| MC7805CDT |  |  |  |
| MC7806CDT |  |  |  |
| MC7808CDT |  |  |  |
| MC7809CDT |  | D-PAK |  |
| MC7810CDT |  |  |  |
| MC7812CDT |  |  |  |
| MC7805ACT | $\pm 2 \%$ | TO-220 |  |
| MC7806ACT |  |  |  |
| MC7808ACT |  |  |  |
| MC7809ACT |  |  |  |
| MC7810ACT |  |  |  |
| MC7812ACT |  |  |  |
| MC7815ACT |  |  |  |
| MC7818ACT |  |  |  |
| MC7824ACT |  |  |  |

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## LM79XX Series <br> 3-Terminal Negative Regulators

## General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of $-5 \mathrm{~V},-12 \mathrm{~V}$, and -15 V . These devices need only one external component-a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.
These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.
Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a
resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.
For applications requiring other voltages, see LM137 datasheet.

## Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5 A output current
- $4 \%$ tolerance on preset output voltage


## Connection Diagrams



Front View
Order Number LM7905CT, LM7912CT or LM7915CT See NS Package Number TO3B

## Typical Applications


*Required if regulator is separated from filter capacitor by more than $3^{\prime \prime}$. For value given, capacitor must be solid tantalum. $25 \mu \mathrm{~F}$ aluminum electrolytic may be substituted.
tRequired for stability. For value given, capacitor must be solid tantalum. $25 \mu \mathrm{~F}$ aluminum electrolytic may be substituted. Values given may be increased without limit.
For output capacitance in excess of $100 \mu \mathrm{~F}$, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage
$\begin{array}{ll}\left(\mathrm{V}_{\mathrm{o}}=-5 \mathrm{~V}\right) & -25 \mathrm{~V} \\ \left(\mathrm{~V}_{\mathrm{o}}=-12 \mathrm{~V} \text { and }-15 \mathrm{~V}\right) & -35 \mathrm{~V}\end{array}$

Input-Output Differential

$$
\begin{array}{lr}
\qquad\left(\mathrm{V}_{\mathrm{o}}=-5 \mathrm{~V}\right) & 25 \mathrm{~V} \\
\left(\mathrm{~V}_{\mathrm{o}}=-12 \mathrm{~V} \text { and }-15 \mathrm{~V}\right) & 30 \mathrm{~V} \\
\text { Power Dissipation (Note 2) } & \text { Internally Limited } \\
\text { Operating Junction Temperature Range } & 0^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
\text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \\
\text { Lead Temperature (Soldering, 10 sec.) } & 230^{\circ} \mathrm{C}
\end{array}
$$

## Electrical Characteristics

Conditions unless otherwise noted: $\mathrm{I}_{\text {OUT }}=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$, Power Dissipation $\leq 1.5 \mathrm{~W}$.


Electrical Characteristics
Conditions unless otherwise noted: $\mathrm{I}_{\text {OUT }}=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$, Power Dissipation $\leq 1.5 \mathrm{~W}$.

| Part Number |  |  | LM7912C | LM7915C | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage |  |  | -12V | -15V |  |
|  | Input Voltage (un | erwise specified) | -19V | -23V |  |
| Symbol | Parameter | Conditions | Min ${ }^{\text {T }}$ Typ ${ }^{\text {a }}$ Max |  |  |
| $\mathrm{V}^{\circ}$ | Output Voltage | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & 5 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 1 \mathrm{~A}, \\ & \mathrm{P} \leq 15 \mathrm{~W} \end{aligned}$ | -11.5 -12.0 -12.5 <br> -11.4  -12.6 <br> $\left(-27 \leq \mathrm{V}_{\mathrm{IN}} \leq\right.$ $-14.5)$  | -14.4 -15.0 -15.6 <br> -14.25  -15.75 <br> $\left(-30 \leq V_{\text {IN }} \leq\right.$ $-17.5)$  | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| $\Delta \mathrm{V}_{\mathrm{O}}$ | Line Regulation | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, (Note 3) | $\begin{array}{rr} \hline 5 & 80 \\ \left(-30 \leq \mathrm{V}_{\mathrm{IN}} \leq-14.5\right) \\ 3 & 30 \\ \left(-22 \leq \mathrm{V}_{\mathrm{IN}} \leq-16\right) \\ \hline \end{array}$ | $\begin{gathered} 5 \\ \left(-30 \leq \mathrm{V}_{\text {IN }} \leq\right. \\ 3 \quad 100 \\ 3 \\ \left(-26 \leq \mathrm{V}_{\mathrm{IN}} \leq-20\right) \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{mV} \\ \mathrm{~V} \\ \mathrm{mV} \\ \mathrm{~V} \end{gathered}$ |
| $\Delta \mathrm{V}$ | Load Regulation | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, (Note 3) |  |  |  |

Electrical Characteristics
(Continued)
Conditions unless otherwise noted: $\mathrm{I}_{\mathrm{OUT}}=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$, Power Dissipation $\leq 1.5 \mathrm{~W}$.


Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee Specific Performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Refer to Typical Performance Characteristics and Design Considerations for details.
Note 3: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

## Design Considerations

The LM79XX fixed voltage regulator series has thermal overload protection from excessive power dissipation, internal short circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.
Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature $\left(125^{\circ} \mathrm{C}\right)$ in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

| Package | Typ <br> $\theta_{\text {JC }}$ <br>  <br>  <br>  <br>  <br> $\mathbf{C} / \mathbf{W}$ | Max <br> $\theta_{\text {JC }}$ <br> ${ }^{\circ} \mathbf{C} / \mathbf{W}$ | Typ <br> $\theta_{\text {JA }}$ <br> ${ }^{\circ} \mathbf{C} / \mathbf{W}$ | Max <br> $\theta_{\text {JA }}$ <br> ${ }^{\circ} \mathbf{C} / \mathbf{W}$ |
| :--- | :---: | :---: | :---: | :---: |
|  | 3.0 | 5.0 | 60 | 40 |

$$
\begin{aligned}
& P_{D M A X}=\frac{T_{J M a X}-T_{A}}{\theta_{J C}+\theta_{C A}} \text { or } \frac{T_{J M a x} T_{A}}{\theta_{J A}} \\
& \theta_{C A}=\theta_{C S}+\theta_{S A} \text { (without heat sink) }
\end{aligned}
$$

Solving for $T_{J}$ :
$T_{J}=T_{A}+P_{D}\left(\theta_{J C}+\theta_{C A}\right)$ or
$=T_{A}+P_{D} \theta_{J A}$ (without heat sink)
Where:
$\mathrm{T}_{\mathrm{J}}=$ Junction Temperature
$\mathrm{T}_{\mathrm{A}}=$ Ambient Temperature
$P_{D}=$ Power Dissipation
$\theta_{\mathrm{JA}}=$ Junction-to-Ambient Thermal Resistance
$\theta_{\mathrm{JC}}=$ Junction-to-Case Thermal Resistance
$\theta_{\mathrm{CA}}=$ Case-to-Ambient Thermal Resistance
$\theta_{\mathrm{CS}}=$ Case-to-Heat Sink Thermal Resistance
$\theta_{\mathrm{SA}}=$ Heat Sink-to-Ambient Thermal Resistance

## Typical Applications

Bypass capacitors are necessary for stable operation of the LM79XX series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response by the regulator.
The bypass capacitors, $(2.2 \mu \mathrm{~F}$ on the input, $1.0 \mu \mathrm{~F}$ on the output) should be ceramic or solid tantalum which have good
high frequency characteristics. If aluminum electrolytics are used, their values should be $10 \mu \mathrm{~F}$ or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.


Load and line regulation $<0.01 \%$ temperature stability $\leq 0.2 \%$
†Determine Zener current
$\dagger \dagger$ Solid tantalum
*Select resistors to set output voltage. $2 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ tracking suggested

${ }^{*}$ IOUT $=1 \mathrm{~mA}+\frac{5 \mathrm{~V}}{\mathrm{R}_{1}}$

Typical Applications (Continued)

*Lamp brightness increase until $\mathrm{i}_{\mathrm{I}}=\mathrm{i}_{\mathrm{Q}}(\approx 1 \mathrm{~mA})+5 \mathrm{~V} / \mathrm{R} 1$.
†Necessary only if raw supply filter capacitor is more that $2^{\prime \prime}$ from LM7905CT

*Lamp brightness increases until $\mathrm{i}_{\mathrm{i}}=5 \mathrm{~V} / \mathrm{R} 1$ ( $\mathrm{l}_{\mathrm{i}}$ can be set as low as $1 \mu \mathrm{~A}$ )
†Necessary only if raw supply filter capacitor is more that 2 " from LM7905

*Improves transient response and ripple rejection. Do not increase beyond $50 \mu \mathrm{~F}$.
$\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SET }}\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 2}\right)$
Select R2 as follows:
LM7905CT $300 \Omega$
LM7912CT $750 \Omega$
LM7915CT 1k

Typical Applications (Continued)


|  | (-15) | $\mathbf{( + 1 5 )}$ |
| :--- | :--- | :--- |
| Load Regulation at $\Delta \mathrm{I}_{\mathrm{L}}=1 \mathrm{~A}$ | 40 mV | 2 mV |
| Output Ripple, $\mathrm{C}_{\mathrm{IN}}=3000 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~A}$ | $100 \mu \mathrm{Vms}$ | $100 \mu \mathrm{Vms}$ |
| Temperature Stability | 50 mV | 50 mV |
| Output Noise $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | $150 \mu \mathrm{Vms}$ | $150 \mu \mathrm{Vms}$ |

*Resistor tolerance of R4 and R5 determine matching of ( + ) and ( - ) outputs.
**Necessary only if raw supply filter capacitors are more than 3 " from regulators.

## Dual Trimmed Supply



Schematic Diagrams



Physical Dimensions inches (millimeters) unless othervise noted


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| :---: | :---: | :---: | :---: |

- Meet or Exceed TIA/EIA-232-F and ITU Recommendation V. 28
- Operate With Single 5-V Power Supply
- Operate Up to 120 kbit/s
- Two Drivers and Two Receivers
- $\pm 30$-V Input Levels
- Low Supply Current . . . 8 mA Typical
- Designed to be Interchangeable With Maxim MAX232
- ESD Protection Exceeds JESD 22
- 2000-V Human-Body Model (A114-A)
- Applications

TIA/EIA-232-F
Battery-Powered Systems
Terminals
Modems
Computers

## description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V , and can accept $\pm 30-\mathrm{V}$ inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASICTM library.

ORDERING INFORMATION

| $\mathrm{T}_{\mathrm{A}}$ | PACKAGE $\dagger$ |  | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
| :---: | :---: | :---: | :---: | :---: |
| $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | PDIP (N) | Tube | MAX232N | MAX232N |
|  | SOIC (D) | Tube | MAX232D | MAX232 |
|  |  | Tape and reel | MAX232DR |  |
|  | SOIC (DW) | Tube | MAX232DW | MAX232 |
|  |  | Tape and reel | MAX232DWR |  |
|  | SOP (NS) | Tape and reel | MAX232NSR | MAX232 |
| $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | PDIP (N) | Tube | MAX232IN | MAX232IN |
|  | SOIC (D) | Tube | MAX232ID | MAX2321 |
|  |  | Tape and reel | MAX232IDR |  |
|  | SOIC (DW) | Tube | MAX232IDW | MAX2321 |
|  |  | Tape and reel | MAX232IDWR |  |

$\dagger$ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## Function Tables

EACH DRIVER

| INPUT <br> TIN | OUTPUT <br> TOUT |
| :---: | :---: |
| L | H |
| H | L |

H = high level, $\mathrm{L}=$ low
level

logic diagram (positive logic)


## absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $\dagger$

| Input supply voltage range, $\mathrm{V}_{\mathrm{CC}}$ (see Note 1) | -0.3 V to 6 V |
| :---: | :---: |
| Positive output supply voltage range, $\mathrm{V}_{\mathrm{S}_{+}}$ | $\mathrm{V}_{\mathrm{CC}}-0.3 \mathrm{~V}$ to 15 V |
| Negative output supply voltage range, $\mathrm{V}_{\mathrm{S}}$ | -0.3 V to -15 V |
| Input voltage range, $\mathrm{V}_{\mathrm{l}}$ : Driver | -0.3 V to $\mathrm{V}_{\mathrm{CC}}+0.3 \mathrm{~V}$ |
| Receiver | $\pm 30 \mathrm{~V}$ |
| Output voltage range, $\mathrm{V}_{\mathrm{O}}$ : T1OUT, T2OUT R1OUT, R2OUT | $\begin{aligned} & \mathrm{V}_{\mathrm{S}_{-}-}-0.3 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{S}_{+}}+0.3 \mathrm{~V} \\ & \ldots . .0 .3 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{cc}}+0.3 \mathrm{~V} \end{aligned}$ |
| Short-circuit duration: T1OUT, T2OUT | Unlimited |
| Package thermal impedance, $\theta_{\text {JA }}$ (see Note 2): D package | $73^{\circ} \mathrm{C} / \mathrm{W}$ |
| DW package | $57^{\circ} \mathrm{C} / \mathrm{W}$ |
| N package | $67^{\circ} \mathrm{C} / \mathrm{W}$ |
| NS package | $64^{\circ} \mathrm{C} / \mathrm{W}$ |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | $260^{\circ} \mathrm{C}$ |
| Storage temperature range, $\mathrm{T}_{\text {stg }}$ | $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ |

$\dagger$ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
recommended operating conditions

|  |  |  | MIN | NOM | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage (T1IN,T2IN) |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage (T1IN, T2IN) |  |  |  | 0.8 | V |
| R1IN, R2IN | Receiver input voltage |  |  |  | $\pm 30$ | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature | MAX232 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |
|  |  | MAX2321 | -40 |  | 85 |  |

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figure 4)

|  | PARAMETER | TEST CONDITIONS | MIN | TYP $\ddagger$ |
| :---: | :---: | :---: | :---: | :---: |
| ICC MAX | UNIT |  |  |  |
| Supply current | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \quad$ All outputs open, <br> $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 8 | 10 | mA |

$\ddagger$ All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
NOTE 3: Test conditions are $\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}$ at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}$.

## DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

| PARAMETER |  |  | TEST CONDITIONS | MIN | TYP $\dagger$ |
| :--- | :--- | :--- | ---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | T1OUT, T2OUT | $\mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega$ to GND | UNIT |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage $\ddagger$ | $\mathrm{T} 1 \mathrm{OUT}, \mathrm{T} 2 \mathrm{OUT}$ | $\mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega$ to GND | 5 | 7 |
| $\mathrm{r}_{\mathrm{O}}$ | Output resistance | T1OUT, T2OUT | $\mathrm{V}_{\mathrm{S}_{+}}=\mathrm{V}_{\mathrm{S}-}=0, \quad \mathrm{~V}_{\mathrm{O}}= \pm 2 \mathrm{~V}$ | 300 | -7 |
| $\mathrm{I}_{\mathrm{OS}} \S$ | Short-circuit output current | T1OUT, T2OUT | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \quad \mathrm{~V}_{\mathrm{O}}=0$ | V | V |
| $\mathrm{I}_{\mathrm{IS}}$ | Short-circuit input current | $\mathrm{T} 1 \mathrm{IN}, \mathrm{T} 2 \mathrm{IN}$ | $\mathrm{V}_{\mathrm{I}}=0$ |  | $\pm 10$ |

$\dagger$ All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
$\ddagger$ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at a time.
NOTE 3: Test conditions are $\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}$ at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}$.
switching characteristics, $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (see Note 3)

| PARAMETER |  | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SR | Driver slew rate | $\mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega \text { to } 7 \mathrm{k} \Omega \text {, }$ See Figure 2 |  |  | 30 | $\mathrm{V} / \mu \mathrm{s}$ |
| SR(t) | Driver transition region slew rate | See Figure 3 |  | 3 |  | $\mathrm{V} / \mu \mathrm{s}$ |
|  | Data rate | One TOUT switching |  | 120 |  | kbit/s |

NOTE 3: Test conditions are $\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}$ at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}$.

## RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

| PARAMETER |  |  | TEST CONDITIONS |  | MIN | TYP† | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | R10UT, R2OUT | $\mathrm{I}^{\mathrm{OH}}=-1 \mathrm{~mA}$ |  | 3.5 |  |  | V |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage $\ddagger$ | R1OUT, R2OUT | $\mathrm{IOL}=3.2 \mathrm{~m}$ |  |  |  | 0.4 | V |
| $\mathrm{V}_{\text {IT }}+$ | Receiver positive-going input threshold voltage | R1IN, R2IN | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$, | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.7 | 2.4 | V |
| VIT- | Receiver negative-going input threshold voltage | R1IN, R2IN | $\mathrm{V}_{C C}=5 \mathrm{~V}$, | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 0.8 | 1.2 |  | V |
| Vhys | Input hysteresis voltage | R1IN, R2IN | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ |  | 0.2 | 0.5 | 1 | V |
| $\mathrm{r}_{\mathrm{i}}$ | Receiver input resistance | R1IN, R2IN | $\mathrm{V}_{\mathrm{CC}}=5$, | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 3 | 5 | 7 | k $\Omega$ |

$\dagger$ All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
$\ddagger$ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
NOTE 3: Test conditions are $\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}$ at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}$.
switching characteristics, $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (see Note 3 and Figure 1)

|  | PARAMETER | TYP | UNIT |
| :---: | :--- | :---: | :---: |
| $\operatorname{tPLH}(\mathrm{R})$ | Receiver propagation delay time, low- to high-level output | 500 | ns |
| $\operatorname{tPHL}(\mathrm{R})$ | Receiver propagation delay time, high- to low-level output | 500 | ns |

NOTE 3: Test conditions are $\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}$ at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}$.

PARAMETER MEASUREMENT INFORMATION


NOTES: A. The pulse generator has the following characteristics: $Z_{O}=50 \Omega$, duty cycle $\leq 50 \%$.
B. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.
C. All diodes are 1 N3064 or equivalent.

Figure 1. Receiver Test Circuit and Waveforms for $\mathrm{t}_{\text {PHL }}$ and $\mathrm{t}_{\text {PLH }}$ Measurements


NOTES: A. The pulse generator has the following characteristics: $Z_{O}=50 \Omega$, duty cycle $\leq 50 \%$.
B. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for $\mathrm{t}_{\text {PHL }}$ and $\mathrm{t}_{\text {PLH }}$ Measurements ( $5-\mu \mathrm{s}$ Input)


TEST CIRCUIT


WAVEFORMS
NOTE A: The pulse generator has the following characteristics: $Z_{O}=50 \Omega$, duty cycle $\leq 50 \%$.
Figure 3. Test Circuit and Waveforms for $\mathrm{t}_{\mathrm{THL}}$ and $\mathrm{t}_{\mathrm{TLH}}$ Measurements ( $20-\mu \mathrm{s}$ Input)

## APPLICATION INFORMATION



Figure 4. Typical Operating Circuit

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## General Description

The MAX700／701／702 are supervisory circuits used to monitor the power supplies in $\mu \mathrm{P}$ and digital systems．The RESET／RESET outputs of the MAX700／701／702 are guar－ anteed to be in the correct state for VCC voltages down to +1 V （Figure 4）．They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5 V powered circuits．
The MAX702 is the simplest part in the family．When VCC falls to 4.65 V ，RESET goes low．The MAX702 also pro－ vides a debounced manual reset input．The MAX701 performs the same functions but has both RESET and RESET outputs．Their primary function is to provide a system reset．Accordingly，an active reset signal is supplied for low supply voltages and for at least 200 ms after the supply voltage reaches its operating value．
In addition to the features of the MAX701 and MAX702， the MAX700 provides preset or adjustable voltage de－ tection so thresholds other than 4.65 V can be selected， and adjustable hysteresis．All parts are supplied in 8－pin Plastic DIP and Narrow SO packages in commercial and extended temperature ranges．

Applications
Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical $\mu$ P Power Monitoring
－Min 200ms RESET Pulse on Power－Up， Power－Down，and During Low－Voltage Conditions
－Reset Threshold Factory Trimmed for +5 V Systems
－No External Components or Adjustments With +5 V Powered Circuits
－Debounced Manual Reset Input
－Preset or Adjustable Voltage Detection（MAX700）
－Adjustable Hysteresis（MAX700）
－8－Pin Plastic DIP and Narrow SO Packages
Ordering Information

| PART | TEMP．RANGE | PIN－PACKAGE |
| :--- | :---: | :--- |
| MAX700CPA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX700CSA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Narrow SO |
| MAX700C／D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice |
| MAX700EPA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX700ESA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Narrow SO |
| MAX701CPA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX701CSA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Narrow SO |
| MAX701C／D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice |
| MAX701EPA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX701ESA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Narrow SO |
| MAX702CPA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX702CSA | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 8 Narrow SO |
| MAX702C／D | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Dice |
| MAX702EPA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Plastic DIP |
| MAX702ESA | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8 Narrow SO |

Pin Configurations


VIノメIルV
Call toll free 1－800－998－8800 for free samples or literature．

## Power-Supply Monitor with Reset

ABSOLUTE MAXIMUM RATINGS
VCC . . . ..................................... 3 V to +15.5 V
Voltage (with respect to GND) at RESET, RESET, HYST,
CTL, SENSE
Operating Temperature Range
MAX70_C
MAX70-E
-0.3 V to Vcc
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
$-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

| Rate of Rise | 100V/ $/ \mathrm{s}$ |
| :---: | :---: |
| Power Dissipation, any package | 380 mW |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 sec .) | $300^{\circ}$ |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability

## ELECTRICAL CHARACTERISTICS

$\left(T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{CTL}=\mathrm{GND}\right.$ on MAX700, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VCC Monitor Voltage Range MAX700 Only | $\begin{aligned} & \text { TA }_{A}=T_{\text {MIN to }} \text { TMAX } \\ & \text { CTL }=\text { VCC } \end{aligned}$ | 3 |  | 15 | V |
| Min VCC For Valid Reset Output, Declining Supply | $\mathrm{T}_{A}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ $\overline{\text { RESET }} \leq 0.4 \mathrm{~V}$ when sinking 1 mA | 1.5 | 1 |  | V |
| Supply Current |  |  | 100 | 200 | $\mu \mathrm{A}$ |
| Reset Threshold Power-up Power-down | $T_{A}=T_{\text {MIN }}$ to $T_{\text {MAX }}$ | $\begin{aligned} & 4.5 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 4.65 \\ & 4.62 \end{aligned}$ | $\begin{aligned} & 4.75 \\ & 4.75 \end{aligned}$ | V |
| Internal Hysteresis | HYST not connected |  | 30 |  | mV |
| Reset Output Pulse Width |  | 200 | 350 | 500 | ms |
| RESET Fall Time | MAX700/701 Only, CLOAD $=100 \mathrm{pF}$ |  | 200 |  | ns |
| VCC Pulse Duration Guaranteeing No Reset Reset | 5 V to 4V Vcc Pulse | 100 | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | 1 | $\mu \mathrm{s}$ |
| MR Input Threshold |  |  | 0.7 |  | $V$ |
| MR Pullup Current |  |  | -5 | -30 | $\mu \mathrm{A}$ |
| MAX700 |  |  |  |  |  |
| RESET Output Low <br> RESET Output High | $\begin{aligned} & \text { ISINK }=3.2 \mathrm{~mA}, V C C=5 \mathrm{~V} \\ & \text { ISINK }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\ & \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\ & \text { ISOURCE }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\ & \text { ISOURCE }=0.5 \mathrm{~mA}, V C C=1.5 \mathrm{~V} \end{aligned}$ | VCC-0. 4 <br> VCC-0. 4 <br> VCC-0. 4 |  | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | V |
| RESET Output Low <br> $\overline{\text { RESET Output High }}$ | $\begin{aligned} & \text { ISINK }=16 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\ & \text { ISINK }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\ & \text { ISINK }=0.4 \mathrm{~mA}, V C C=1.5 \mathrm{~V} \\ & \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=5 \mathrm{~V} \\ & \text { ISOURCE }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \end{aligned}$ | Vcc-0.4 <br> VCC-0.4 |  | $\begin{aligned} & 0.4 \\ & 0.4 \\ & 0.4 \end{aligned}$ | V |
| MAX701 |  |  |  |  |  |
| RESET Output Low RESET Output High | $\begin{aligned} & I \text { SINK }=16 \mathrm{~mA}, V C C=5 \mathrm{~V} \\ & \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\ & \text { ISOURCE }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\ & \text { ISOURCE }=0.5 \mathrm{~mA}, V C C=1.5 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{CC}}-0.4$ <br> $V_{C C}-0.4$ <br> VCC-0.4 |  | 0.4 | V |
| RESET Output Low <br> RESET Output High | ISINK $=3.2 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=4.25 \mathrm{~V}$ <br> ISINK $=1.6 \mathrm{~mA}, V_{C C}=3 \mathrm{~V}$ <br> ISINK $=0.4 \mathrm{~mA}, V_{C C}=1.5 \mathrm{~V}$ <br> ISOURCE $=3.2 \mathrm{~mA}, \mathrm{VCC}=5 \mathrm{~V}$ | Vcc-0.4 |  | $\begin{aligned} & 0.4 \\ & 0.4 \\ & 0.4 \end{aligned}$ | V |

$\qquad$

# Power－Supply Monitor with Reset 

## ELECTRICAL CHARACTERISTICS（continued）

$\left(T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{CTL}=\mathrm{GND}\right.$ on MAX700，unless otherwise noted．）

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MAX702 |  |  |  |  |  |
| RESET Output Low <br> RESET Output High | $\begin{aligned} & \text { ISINK }=3.2 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\ & \text { ISINK }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\ & \text { ISINK }=0.4 \mathrm{~mA}, V C C=1.5 \mathrm{~V} \\ & \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=5 \mathrm{~V} \end{aligned}$ | Vcc－0．4 |  | $\begin{aligned} & 0.4 \\ & 0.4 \\ & 0.4 \end{aligned}$ | V |
| MAX700 ONLY（CTL＝Vcc，unless otherwise noted．） |  |  |  |  |  |
| SENSE Input Threshold | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {min }}$ to $\mathrm{Tmax}^{\text {ma }}$ | 1.25 | 1.29 | 1.35 | $V$ |
| SENSE Input Current |  |  | 0.1 |  | nA |
| HYST Input On Resistance |  |  | 0.5 |  | k $\Omega$ |
| CTL Input Threshold |  |  | 2 |  | $\checkmark$ |
| CTL Pulldown Current |  |  | 30 | 100 | $\mu \mathrm{A}$ |

Pin Description

| NAME | FUNCTION |
| :---: | :---: |
| VCC | Chip power and +5 V sensing input（when CTL ＝GND on MAX700） |
| GND | Ground |
| RESET | Goes low when VCC falls below 4.65 V ，or when $C T L=V C C$ on the MAX700 goes low when SENSE falls below 1.9 V ． |
| RESET | MAX700， 701 only－Inverted Version of $\overline{\text { RESET }}$ ． |
| MR | Input for manual push button reset．Has inter－ nal $5 \mu \mathrm{~A}$ pull up．Low input activates the RESET／RESET outputs． |
| CTL | MAX700 only－When CTL＝GND．VCC is moni－ tored by the reset circuit．When CTL $=\mathrm{VCC}_{C}, ~ \mathrm{VCC}$ is ignored and SENSE is monitored，allowing the threshold to be set with external resistors． |
| HYST | MAX700 only－Normally NOT used when volt－ age is monitored through VCC（CTL＝GND）． When monitoring through SENSE（CTL＝VCC）， HYST allows hysteresis to be added，reducing noise and spurious reset activity（Figure 3）．HYST turns on $5 \mu$ s before the RESET／RESET outputs are activated，and its on resistance to GND is typi－ cally $1 \mathrm{k} \Omega$ ． |
| SENSE | MAX700 only－The voltage sense input when $C T L=V C C$ ．Its threshold is 1.29 V ．Sense al－ ways remains connected to the internal compa－ rator．So，when VCC is being monitored internally（CTL＝GND），SENSE should be left open circuit． |

## Power－Supply Monitor with Reset



Figure 1．MAX700 Block Diagram


Figure 3．MAX700 Connected for External Sense and Hysteresis


Figure 2．MAX700 Typical Connection Diagram


Figure 4．Typical MAX700／701／702 $\overline{\text { RESET }}$ Output vs．VCC

Figure 4 shows the $\overline{\operatorname{RE} \overline{S E T}}$ output of the MAX700／701／702 in the correct state for VCC voltages down to OV．Note the effect of the built－in hysteresis on the trigger level of RESET．

## Low-Power, 16-Bit Analog-to-Digital Converters with Parallel Interface


#### Abstract

General Description


The MAX1165/MAX1166 16-bit, low-power, successiveapproximation analog-to-digital converters (ADCs) feature automatic power-down, factory-trimmed internal clock, and a 16-bit wide (MAX1165) or byte wide (MAX1166) parallel interface. The devices operate from a single +4.75 V to +5.25 V analog supply and $\mathrm{a}+2.7 \mathrm{~V}$ to +5.25 V digital supply.
The MAX1165/MAX1166 use an internal 4.096V reference or an external reference. The MAX1165/MAX1166 consume only 1.8 mA at a sampling rate of 165 ksps with external reference and 2.7 mA with internal reference. AutoShutdown ${ }^{\top 1}$ reduces supply current to 0.1 mA at 10ksps.
The MAX1165/MAX1166 are ideal for high-performance, battery-powered, data-acquisition applications. Excellent dynamic performance and low power consumption in a small package make the MAX1165/ MAX1166 ideal for circuits with demanding power consumption and space requirements.
The 16 -bit wide MAX1165 is available in a 28 -pin TSSOP package and the byte wide MAX1166 is available in a 20-pin TSSOP package. Both devices are available in either the $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ commercial, or the $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ extended temperature range.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

## Applications

Temperature Sensor/Monitor Industrial Process Control
I/O Boards
Data-Acquisition Systems
Cable/Harness Tester
Accelerometer Measurements
Digital Signal Processing

Pin Configurations appear at end of data sheet. Functional Diagram appears at end of data sheet.

Features

- 16-Bit Wide (MAX1165) and Byte Wide (MAX1166) Parallel Interface
- High Speed: 165ksps Sample Rate
- Accurate: $\pm 2$ LSB INL, 16 Bit No Missing Codes
- 4.096V, 35ppm/ ${ }^{\circ} \mathrm{C}$ Internal Reference
- External Reference Range: +3.8V to +5.25V
- Single +4.75V to +5.25V Analog Supply Voltage
- +2.7V to +5.25V Digital Supply Voltage
- Low Supply Current
1.8mA (External Reference)
2.7mA (Internal Reference)
$0.1 \mu \mathrm{~A}$ (10ksps, External Reference)
- Small Footprint

28-Pin TSSOP Package (16-Bit Wide)
20-Pin TSSOP Package (Byte Wide)
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | INL |
| :--- | ---: | :--- | :---: |
| MAX1165ACUI | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 28 TSSOP | $\pm 2$ |
| MAX1165BCUI | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 28 TSSOP | $\pm 2$ |
| MAX1165CCUI | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 28 TSSOP | $\pm 4$ |
| MAX1165AEUI* | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 28 TSSOP | $\pm 2$ |
| MAX1165BEUI | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 28 TSSOP | $\pm 2$ |
| MAX1165CEUI ${ }^{\star}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 28 TSSOP | $\pm 4$ |

*Future product-contact factory for availability.

Ordering Information continued at end of data sheet.
Typical Operating Circuit


## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface

## ABSOLUTE MAXIMUM RATINGS

| AVDD to AGND | -0.3V to +6V |
| :---: | :---: |
| DV ${ }_{\text {D }}$ to DGND | 0.3V to ( $\mathrm{AV}_{\text {DD }}+0.3 \mathrm{~V}$ ) |
| AGND to DGND. | -0.3V to +0.3V |
| AIN, REF, REFADJ to AGND | .-0.3V to ( $\mathrm{AV} \mathrm{V}_{\text {D }}+0.3 \mathrm{~V}$ ) |
| $\overline{\mathrm{CS}}, \mathrm{HBEN}, \mathrm{R} / \overline{\mathrm{C}}, \mathrm{RESET}$ to DGND | -0.3V to +6V |
| Digital Output (D15-D0, $\overline{\mathrm{EOC}}$ ) to DGND | .-0.3V to (DVDD +0.3 V ) |
| Maximum Continuous Current | . 50 mA |

Continuous Power Dissipation ( $\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}$ )
20-Pin TSSOP (derate $10.9 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+70^{\circ} \mathrm{C}$ ) ........ 879 mW 28-Pin TSSOP (derate $12.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+70^{\circ} \mathrm{C}$ ) ..... 1026 mW Operating Temperature Ranges
MAX116_ _CU_ _................................................................ $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
MAX116_ EU_

Storage Temperature Range ............................. $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Junction Temperature ...................................................... $150^{\circ} \mathrm{C}$
Lead Temperature (soldering, 10s) ................................. $300^{\circ} \mathrm{C}$
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $A V_{D D}=D_{D D}=+5 \mathrm{~V}$, external reference $=+4.096 \mathrm{~V}, C_{R E F}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\text {REFADJ }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)


## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface

## ELECTRICAL CHARACTERISTICS (continued)

$\left(A V_{D D}=D V_{D D}=+5 V\right.$, external reference $=+4.096 \mathrm{~V}, C_{R E F}=4.7 \mu F, C_{R E F A D J}=0.1 \mu F, T_{A}=T_{M I N}$ to $T_{M A X}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| INTERNAL REFERENCE |  |  |  |  |  |  |  |
| REF Output Voltage | VREF |  |  | 4.056 | 4.096 | 4.136 | V |
| REF Output Tempco | TCREF |  |  |  | $\pm 25$ |  | ppm $/{ }^{\circ} \mathrm{C}$ |
| REF Short-Circuit Current | IREFSC |  |  |  | $\pm 10$ |  | mA |
| Capacitive Bypass at REFADJ | Crefadj |  |  | 0.1 |  |  | $\mu \mathrm{F}$ |
| Capacitive Bypass at REF | CreF |  |  | 1 |  |  | $\mu \mathrm{F}$ |
| REFADJ Input Leakage Current | IREFADJ |  |  |  | 20 |  | $\mu \mathrm{A}$ |
| EXTERNAL REFERENCE |  |  |  |  |  |  |  |
| REFADJ Buffer Disable Threshold |  | To power down the internal reference |  | $\begin{gathered} \text { AVDD } \\ 0.4 \end{gathered}$ |  | $\begin{gathered} A V_{D D}- \\ 0.1 \end{gathered}$ | V |
| REF Input Voltage Range |  | Internal reference disabled |  | 3.8 |  | AVDD | V |
| REF Input Current | IREF | $\mathrm{V}_{\text {REF }}=+4.096 \mathrm{~V}$, fSAMPLE $=165 \mathrm{ksps}$ |  |  | 50 | 120 | $\mu \mathrm{A}$ |
|  |  | Shutdown mode |  | $\pm 0.1$ |  |  |  |
| DIGITAL INPUTS/OUTPUTS |  |  |  |  |  |  |  |
| Input High Voltage | $\mathrm{V}_{\mathrm{IH}}$ |  |  | $\begin{gathered} 0.7 \times \\ D V_{D D} \end{gathered}$ |  |  | V |
| Input Low Voltage | VIL |  |  |  |  | $\begin{aligned} & 0.3 \times \\ & D V_{D D} \end{aligned}$ | V |
| Input Leakage Current | IIN | $\mathrm{V}_{\mathrm{IH}}=0$ or $\mathrm{V}_{\text {DD }}$ |  |  | $\pm 0.1$ | $\pm 1$ | $\mu \mathrm{A}$ |
| Input Hysteresis | $\mathrm{V}_{\text {HYST }}$ |  |  |  | 0.1 |  | V |
| Input Capacitance | CIN |  |  |  | 15 |  | pF |
| Output High Voltage | VOH | $\begin{aligned} & \text { ISOURCE }=0.5 \mathrm{~mA}, \\ & \mathrm{AV}_{\mathrm{DD}}=+5.25 \mathrm{~V} \end{aligned}$ | $\mathrm{o}+5.25 \mathrm{~V}$ | $\begin{gathered} \text { DVDD - } \\ 0.4 \end{gathered}$ |  |  | V |
| Output Low Voltage | Vol | $\begin{aligned} & I_{S I N K}=1.6 \mathrm{~mA}, D V_{I} \\ & A V_{D D}=+5.25 \mathrm{~V} \end{aligned}$ | $5.25 \mathrm{~V},$ |  |  | 0.4 | V |
| Three-State Leakage Current | IOZ | D0-D15 |  |  | $\pm 0.1$ | $\pm 10$ | $\mu \mathrm{A}$ |
| Three-State Output Capacitance | Coz |  |  |  | 15 |  | pF |
| POWER REQUIREMENTS |  |  |  |  |  |  |  |
| Analog Supply Voltage | AVDD |  |  | 4.75 |  | 5.25 | V |
| Digital Supply | DVDD |  |  | 2.7 |  | AVDD | V |
| Analog Supply Current | IAVDD | Internal reference | 165ksps |  | 2.7 | 3.2 | mA |
|  |  |  | 100ksps |  | 2.0 |  |  |
|  |  |  | 10ksps |  | 1.0 |  |  |
|  |  |  | 1ksps |  | 1.0 |  |  |
|  |  | External reference | 165ksps |  | 1.8 | 2.3 |  |
|  |  |  | 100ksps |  | 1.1 |  |  |
|  |  |  | 10ksps |  | 0.1 |  |  |
|  |  |  | 1ksps |  | 0.01 |  |  |

## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface

## ELECTRICAL CHARACTERISTICS (continued)

$\left(A V_{D D}=D_{D D}=+5 V\right.$, external reference $=+4.096 \mathrm{~V}, C_{R E F}=4.7 \mu F, C_{R E F A D J}=0.1 \mu F, T_{A}=T_{\text {MIN }}$ to $T_{M A X}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Digital Supply Current | IDVDD | D0-D15 = all zeros | 165ksps | 0.5 | 0.7 | mA |
|  |  |  | 100ksps | 0.3 |  |  |
|  |  |  | 10ksps | 0.03 |  |  |
|  |  |  | 1ksps | 0.003 |  |  |
| Shutdown Supply Current | ISHDN | Full power-down | IAVDD | 0.5 | 5 | $\mu \mathrm{A}$ |
|  |  |  | IDVDD | 0.5 | 5 |  |
|  |  | REF and REF buffer enabled (standby mode) | IAVDD | 1.0 | 1.2 | mA |
|  |  |  | IDVDD <br> (Note 3) | 0.5 | 5 | $\mu \mathrm{A}$ |
| Power-Supply Rejection Ratio | PSRR | $\mathrm{AV} \mathrm{V}_{\mathrm{DD}}=+5 \mathrm{~V} \pm 5 \%$, full-scale input (Note 4) |  | 68 |  | dB |

## TIMING CHARACTERISTICS (Figures 1 and 2)

$\left(\mathrm{AV}_{\mathrm{DD}}=+4.75 \mathrm{~V}\right.$ to $+5.25 \mathrm{~V}, \mathrm{DV}$ DD $=+2.7 \mathrm{~V}$ to $\mathrm{AV}_{\mathrm{DD}}$, external reference $=+4.096 \mathrm{~V}, \mathrm{CREF}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REFAD}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{LOAD}}=20 \mathrm{pF}$, $T_{A}=T_{\text {MIN }}$ to $T_{M A X}$, unless otherwise noted. Typical values are at $T_{A}=+25^{\circ} \mathrm{C}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Acquisition Time | tacQ |  | 1.1 |  | $\mu \mathrm{s}$ |
| Conversion Time | tconv |  |  | 4.7 |  |
| $\overline{\mathrm{CS}}$ Pulse Width High | tCSH | (Note 5) | 40 |  | ns |
| $\overline{\mathrm{CS}}$ Pulse Width Low (Note 5) | tCSL | $\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}$ to 5.25 V | 40 |  | ns |
|  |  | V ${ }_{\text {DVDD }}=2.7 \mathrm{~V}$ to 5.25 V | 60 |  |  |
|  | tDS |  | 0 |  | ns |
| $\mathrm{R} / \overline{\mathrm{C}}$ to $\overline{\mathrm{CS}}$ Fall Hold Time | tD | $\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}$ to 5.25 V | 40 |  | ns |
|  |  | V ${ }_{\text {DVDD }}=2.7 \mathrm{~V}$ to 5.25 V | 60 |  |  |
| $\overline{\mathrm{CS}}$ to Output Data Valid | tDO | $\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}$ to 5.25 V |  | 40 | ns |
|  |  | $\mathrm{V}_{\text {DVDD }}=2.7 \mathrm{~V}$ to 5.25 V |  | 80 |  |
| HBEN Transition to Output Data Valid (MAX1166 Only) | tDO1 | $\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}$ to 5.25 V |  | 40 | ns |
|  |  | V ${ }_{\text {DVDD }}=2.7 \mathrm{~V}$ to 5.25 V |  | 80 |  |
| $\overline{\text { EOC }}$ Fall to $\overline{\mathrm{CS}}$ Fall | tDV |  | 0 |  | ns |
| $\overline{\mathrm{CS}}$ Rise to $\overline{\mathrm{EOC}}$ Rise | teoc | V ${ }_{\text {DVDD }}=4.75 \mathrm{~V}$ to 5.25 V |  | 40 | ns |
|  |  | $\mathrm{V}_{\text {DVDD }}=2.7 \mathrm{~V}$ to 5.25 V |  | 80 |  |
| Bus Relinquish Time (Note 5) | tBR | $\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}$ to 5.25 V |  | 40 | ns |
|  |  | V ${ }_{\text {DVDD }}=2.7 \mathrm{~V}$ to 5.25 V |  | 80 |  |

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after offset and gain errors have been removed.
Note 2: Offset nulled.
Note 3: Shutdown supply currents are typically $0.5 \mu \mathrm{~A}$, maximum specification is limited by automated test equipment.
Note 4: Defined as the change in positive full scale caused by a $\pm 5 \%$ variation in the nominal supply.
Note 5: To ensure best performance, finish reading the data and wait tBR before starting a new acquisition.

## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface

Typical Operating Characteristics
$\left(A V_{D D}=D_{D D}=+5 \mathrm{~V}\right.$, external reference $=+4.096 \mathrm{~V}, \mathrm{CREF}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\text {REFAD }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted..$)$



OFFSET ERROR
vs. TEMPERATURE


DNL vs. OUTPUT CODE


IAVDD + IDVDD SHUTDOWN CURRENT vs. TEMPERATURE


GAIN ERROR
vs. TEMPERATURE


IAVDD + IDVDD SUPPLY CURRENT
vs. SAMPLE RATE


INTERNAL REFERENCE
vs. TEMPERATURE


SINAD vs. FREQUENCY


## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface

$\left(A V_{D D}=D V_{D D}=+5 \mathrm{~V}\right.$, external reference $=+4.096 \mathrm{~V}, \mathrm{CREF}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\text {REFADJ }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted. $)$





# Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface 

Pin Description

| PIN |  | NAME |  | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| MAX1165 | MAX1166 | MAX1165 | MAX1166 |  |
| 1 | 1 | D8 | D4/D12 | Three-State Digital Data Output |
| 2 | 2 | D9 | D5/D13 | Three-State Digital Data Output |
| 3 | 3 | D10 | D6/D14 | Three-State Digital Data Output |
| 4 | 4 | D11 | D7/D15 | Three-State Digital Data Output. D15 is the MSB. |
| 5 | - | D12 | - | Three-State Digital Data Output |
| 6 | - | D13 | - | Three-State Digital Data Output |
| 7 | - | D14 | - | Three-State Digital Data Output |
| 8 | - | D15 | - | Three-State Digital Data Output (MSB) |
| 9 | 5 | $\mathrm{R} /$ |  | Read/Convert Input. Power up and put the MAX1165/MAX1166 in acquisition mode by holding $\mathrm{R} / \overline{\mathrm{C}}$ low during the first falling edge of $\overline{\mathrm{CS}}$. During the second falling edge of $\overline{C S}$, the level on $R / \bar{C}$ determines whether the reference and reference buffer power down or remain on after conversion. Set R/C high during the second falling edge of $\overline{\mathrm{CS}}$ to power down the reference and buffer, or set $\mathrm{R} / \overline{\mathrm{C}}$ low to leave the reference and buffer powered up. Set R/C high during the third falling edge of $\overline{\mathrm{CS}}$ to put valid data on the bus. |
| 10 | 6 | $\overline{\mathrm{EO}}$ |  | End of Conversion. $\overline{\mathrm{EOC}}$ drives low when conversion is complete. |
| 11 | 7 | AV |  | Analog Supply Input. Bypass with a $0.1 \mu \mathrm{~F}$ capacitor to AGND. |
| 12 | 8 | AGN |  | Analog Ground. Primary analog ground (star ground). |
| 13 | 9 | AIN |  | Analog Input |
| 14 | 10 | AGN |  | Analog Ground. Connect pin 14 to pin 12 (MAX1165). Connect pin 10 to pin 8 (MAX1166). |
| 15 | 11 | REFA | ADJ | Reference Buffer Output. Bypass REFADJ with a $0.1 \mu \mathrm{~F}$ capacitor to AGND for internal reference mode. Connect REFADJ to AVDD to select external reference mode. |
| 16 | 12 | RE |  | Reference Input/Output. Bypass REF with a $4.7 \mu \mathrm{~F}$ capacitor to AGND for internal reference mode. External reference input when in external reference mode. |
| 17 | - | RES |  | Reset Input. Logic high resets the device. |
| - | 13 | HBE |  | High-Byte Enable Input. Used to multiplex the 14-bit conversion result: <br> 1: Most significant byte available on the data bus. <br> 0: Least significant byte available on the data bus. |
| 18 | 14 | $\overline{C S}$ |  | Convert Start. The first falling edge of $\overline{\mathrm{CS}}$ powers up the device and enables acquire mode when $R / \bar{C}$ is low. The second falling edge of $\overline{C S}$ starts conversion. The third falling edge of $\overline{\mathrm{CS}}$ loads the result onto the bus when $\mathrm{R} / \overline{\mathrm{C}}$ is high. |
| 19 | 15 | DGN |  | Digital Ground |
| 20 | 16 | DV |  | Digital Supply Voltage. Bypass with a $0.1 \mu$ F capacitor to DGND. |
| 21 | 17 | D0 | D0/D8 | Three-State Digital Data Output |
| 22 | 18 | D1 | D1/D9 | Three-State Digital Data Output |
| 23 | 19 | D2 | D2/D10 | Three-State Digital Data Output |
| 24 | 20 | D3 | D3/D11 | Three-State Digital Data Output |
| 25 | - | D4 | - | Three-State Digital Data Output |
| 26 | - | D5 | - | Three-State Digital Data Output |
| 27 | - | D6 | - | Three-State Digital Data Output |
| 28 | - | D7 | - | Three-State Digital Data Output |

## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface



Figure 1. Load Circuits

## Detailed Description

Converter Operation
The MAX1165/MAX1166 use a successive-approximation (SAR) conversion technique with an inherent track-and-hold (T/H) stage to convert an analog input into a 16-bit digital output. Parallel outputs provide a highspeed interface to most microprocessors ( $\mu \mathrm{Ps}$ ). The Functional Diagram shows a simplified internal architecture of the MAX1165/MAX1166. Figure 3 shows a typical application circuit for the MAX1166.

## Analog Input

The equivalent input circuit is shown in Figure 4. A switched capacitor digital-to-analog converter (DAC) provides an inherent T/H function. The single-ended input is connected between AIN and AGND.

## Input Bandwidth

The ADC's input-tracking circuitry has a 4 MHz smallsignal bandwidth, so it is possible to digitize highspeed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, use anti-alias filtering.

## Analog Input Protection

Internal protection diodes, which clamp the analog input to AVDD and/or AGND, allow the input to swing from $A G N D-0.3 V$ to $A V D D+0.3 V$, without damaging the device.
If the analog input exceeds 300 mV beyond the supplies, limit the input current to 10 mA .


Figure 2. MAX1165/MAX1166 Timing Diagram

## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface



Figure 3. Typical Application Circuit for the MAX1166
Track and Hold (T/H)
In track mode, the analog signal is acquired on the internal hold capacitor. In hold mode, the T/H switches open and the capacitive DAC samples the analog input.
During the acquisition, the analog input (AIN) charges capacitor CDAC. The acquisition ends on the second falling edge of CS. At this instant, the T/H switches open. The retained charge on CDAC represents a sample of the input.
In hold mode, the capacitive DAC adjusts during the remainder of the conversion time to restore node ZERO to zero within the limits of 16-bit resolution. Force $\overline{\mathrm{CS}}$ low to put valid data on the bus at the end of the conversion.
The time required for the $\mathrm{T} / \mathrm{H}$ to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time ( $\mathrm{t}_{\mathrm{ACQ}}$ ) is the maximum time the device takes to acquire the signal. Use the following formula to calculate acquisition time:

$$
t_{A C Q}=11\left(R_{S}+R_{I N}\right) \times 35 p F
$$

where $\mathrm{RIN}_{\mathrm{IN}}=800 \Omega$, RS $=$ the input signal's source impedance, and taCQ is never less than $1.1 \mu \mathrm{~s}$. A source impedance less than $1 \mathrm{k} \Omega$ does not significantly affect the ADC's performance.
To improve the input signal bandwidth under AC conditions, drive AIN with a wideband buffer ( $>4 \mathrm{MHz}$ ) that can drive the ADC's input capacitance and settle quickly.


Figure 4. Equivalent Input Circuit
Power-Down Modes
Select standby mode or shutdown mode with the R/C bit during the second falling edge of $\overline{\mathrm{CS}}$ (see the Selecting Standby or Shutdown Mode section). The MAX1165/MAX1166 automatically enter either standby mode (reference and buffer on) or shutdown (reference and buffer off) after each conversion depending on the status of $\mathrm{R} / \overline{\mathrm{C}}$ during the second falling edge of $\overline{\mathrm{CS}}$.

## Internal Clock

The MAX1165/MAX1166 generate an internal conversion clock. This frees the microprocessor from the burden of running the SAR conversion clock. Total conversion time after entering hold mode (second falling edge of $\overline{\mathrm{CS}}$ ) to end of conversion ( $\overline{\mathrm{EOC}}$ ) falling is $4.7 \mu \mathrm{~s}$ (max).

## Applications Information

## Starting a Conversion

$\overline{\mathrm{CS}}$ and $\mathrm{R} / \overline{\mathrm{C}}$ control acquisition and conversion in the MAX1165/MAX1166 (Figure 2). The first falling edge of $\overline{\mathrm{CS}}$ powers up the device and puts it in acquire mode if $R / \bar{C}$ is low. The convert start is ignored if $R / \bar{C}$ is high. The MAX1165/MAX1166 need at least 10 ms (CREFADJ $=0.1 \mu \mathrm{~F}$, CREF $=4.7 \mu \mathrm{~F}$ ) for the internal reference to wake up and settle before starting the conversion if powering up from shutdown. The ADC can wake up, from shutdown, to an unknown state. Put the ADC in a known state by completing one "dummy" conversion. The MAX1165/MAX1166 are in a known state, ready for actual data acquisition, after the completion of the dummy conversion. A dummy conversion consists of one full conversion cycle.
The MAX1165 provides an alternative reset function to reset the device (see the RESET section).

## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface



Figure 5. Selecting Standby Mode

## Selecting Standby or Shutdown Mode

The MAX1165/MAX1166 have a selectable standby or low-power shutdown mode. In standby mode, the ADC's internal reference and reference buffer do not power down between conversions, eliminating the need to wait for the reference to power up before performing the next conversion. Shutdown mode powers down the reference and reference buffer after completing a conversion. The reference and reference buffer require a minimum of $10 \mathrm{~ms}($ CREFADJ $=0.1 \mu \mathrm{~F}, \mathrm{CREF}=4.7 \mu \mathrm{~F})$ to power up and settle from shutdown.
The state of $R / \bar{C}$ at the second falling edge of $\overline{C S}$ selects which power-down mode the MAX1165/ MAX1166 enter upon conversion completion. Holding R/C low causes the MAX1165/MAX1166 to enter standby mode. The reference and buffer are left on after the conversion completes. R/C high causes the MAX1165/ MAX1166 to enter shutdown mode and shut down the reference and buffer after conversion (Figures 5 and 6). When using an external reference, set the REF powerdown bit high for lowest current operation.

## Standby Mode

While in standby mode, the supply current is reduced to less than 1mA (typ). The next falling edge of $\overline{C S}$ with R/C low causes the MAX1165/MAX1166 to exit standby mode and begin acquisition. The reference and reference buffer remain active to allow quick turn-on time. Standby mode allows significant power savings while running at the maximum sample rate.

Shutdown Mode
In shutdown mode, the reference and reference buffer are shut down between conversions. Shutdown mode reduces supply current to $0.5 \mu \mathrm{~A}$ (typ) immediately after the conversion. The falling edge of $\overline{C S}$ with $R / \bar{C}$ low


Figure 6. Selecting Shutdown Mode
causes the reference and buffer to wake up and enter acquisition mode. To achieve 16-bit accuracy, allow $10 \mathrm{~ms}($ CREFADJ $=0.1 \mu \mathrm{~F}, \mathrm{CREF}=4.7 \mu \mathrm{~F})$ for the internal reference to wake up.

## Internal and External Reference

Internal Reference
The internal reference of the MAX1165/MAX1166 is internally buffered to provide +4.096 V output at REF. Bypass REF to AGND and REFADJ to AGND with $4.7 \mu \mathrm{~F}$ and $0.1 \mu \mathrm{~F}$, respectively.
Fine adjustments can be made to the internal reference voltage by sinking or sourcing current at REFADJ. The input impedance of REFADJ is nominally $5 \mathrm{k} \Omega$. The internal reference voltage is adjustable to $\pm 1.5 \%$ with the circuit of Figure 7.


Figure 7. MAX1165/MAX1166 Reference Adjust Circuit

## External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1165/ MAX1166s' internal buffer amplifier. When connecting an

## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface

external reference to REFADJ, the input impedance is typically $5 \mathrm{k} \Omega$. Using the buffered REFADJ input makes buffering the external reference unnecessary; however, the internal buffer output must be bypassed at REF with a $1 \mu \mathrm{~F}$ capacitor.
Connect REFADJ to AVDD to disable the internal buffer. Directly drive REF using an external reference. During conversion the external reference must be able to drive $100 \mu \mathrm{~A}$ of DC load current and have an output impedance of $10 \Omega$ or less. REFADJ's impedance is typically $5 k \Omega$. The DC input impedance of REF is a minimum $40 \mathrm{k} \Omega$.
For optimal performance, buffer the reference through an op amp and bypass REF with a $1 \mu \mathrm{~F}$ capacitor. Consider the MAX1165/MAX1166s' equivalent input noise $\left(38 \mu V_{\mathrm{RMS}}\right)$ when choosing a reference.

## Reading a Conversion Result

$\overline{\mathrm{EOC}}$ is provided to flag the microprocessor when a conversion is complete. The falling edge of $\overline{\mathrm{EOC}}$ signals that the data is valid and ready to be output to the bus.
D0-D15 are the parallel outputs of the MAX1165/ MAX1166. These three-state outputs allow for direct connection to a microcontroller I/O bus. The outputs remain high-impedance during acquisition and conversion. Data is loaded onto the bus with the third falling edge of $\overline{C S}$ with $R / \bar{C}$ high after tDO. Bringing $\overline{C S}$ high forces the output bus back to high impedance. The MAX1165/MAX1166 then wait for the next falling edge of $\overline{\mathrm{CS}}$ to start the next conversion cycle (Figure 2).
The MAX1165 loads the conversion result onto a 16-bit wide data bus while the MAX1166 has a byte-wide output format. HBEN toggles the output between the most/least significant byte. The least significant byte is loaded onto the output bus when HBEN is low and the most significant byte is on the bus when HBEN is high (Figure 2).

RESET
Toggle RESET with $\overline{\mathrm{CS}}$ high. The next falling edge of $\overline{\mathrm{CS}}$ begins acquisition. This reset is an alternative to the dummy conversion explained in the Starting a Conversion section.

## Transfer Function

Figure 8 shows the MAX1165/MAX1166 output transfer function. The output is coded in standard binary.

## Input Buffer

Most applications require an input buffer amplifier to achieve 16 -bit accuracy. If the input signal is multi-


Figure 8. MAX1165/MAX1166 Transfer Function
plexed, the input channel should be switched immediately after acquisition, rather than near the end of or after a conversion. This allows more time for the input buffer amplifier to respond to a large step change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change before the beginning of the acquisition time. At the beginning of acquisition, the internal sampling capacitor array connects to AIN (the amplifier output), causing some output disturbance. Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the internal sampling capacitor with very little ripple. However, for AC use, AIN must be driven by a wideband buffer (at least 10 MHz ), which must be stable with the ADC's capacitive load (in parallel with any AIN bypass capacitor used) and also settle quickly. An example of this circuit using the MAX4434 is given in Figure 9.


Figure 9. MAX1165/MAX1166 Fast Settling Input Buffer

# Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface 


#### Abstract

Layout, Grounding, and Bypassing For best performance, use printed circuit boards. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital ground planes with only one point connecting the two ground systems (analog and digital) as close to the device as possible. Route digital signals far away from sensitive analog and reference inputs. If digital lines must cross analog lines, do so at right angles to minimize coupling digital noise onto the analog lines. If the analog and digital sections share the same supply, then isolate the digital and analog supply by connecting them with a low-value (10 resistor or ferrite bead. The ADC is sensitive to high-frequency noise on the AVDD supply. Bypass AVDD to AGND with a $0.1 \mu \mathrm{~F}$ capacitor in parallel with a $1 \mu \mathrm{~F}$ to $10 \mu \mathrm{~F}$ low-ESR capacitor with the smallest capacitor closest to the device. Keep capacitor leads short to minimize stray inductance.


## Definitions

## Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1165/MAX1166 are measured using the end-point method.

## Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of $\pm 1$ LSB guarantees no missing codes and a monotonic transfer function.

## Aperture Jitter and Delay

Aperture jitter is the sample-to-sample variation in the time between samples. Aperture delay is the time between the rising edge of the sampling clock and the instant when the actual sample is taken.

## Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization
noise error only and results directly from the ADC's resolution (N bits):

$$
\text { SNR }=(6.02 \times N+1.76) \mathrm{dB}
$$

where $\mathrm{N}=16$ bits.
In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$
\text { SINAD }(\mathrm{dB})=20 \times \log \left[\frac{\text { Signal }_{\text {RMS }}}{(\text { Noise }+ \text { Distortion })_{\mathrm{RMS}}}\right]
$$

Effective Number of Bits Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the fullscale range of the ADC, calculate the effective number of bits as follows:

$$
\mathrm{ENOB}=\frac{\mathrm{SINAD}-1.76}{6.02}
$$

## Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$
\mathrm{THD}=20 \times \log \left[\frac{\left(\sqrt{V_{2}^{2}+V_{3}^{2}+V_{4}^{2}+V_{5}^{2}}\right)}{V_{1}}\right]
$$

where $\mathrm{V}_{1}$ is the fundamental amplitude and $\mathrm{V}_{2}$ through $V_{5}$ are the 2nd- through 5th-order harmonics.

## Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component.

# Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface 

Functional Diagram


Ordering Information (continued)

| PART | TEMP RANGE | PIN-PACKAGE | INL |
| :--- | ---: | :--- | :---: |
| MAX1166ACUP | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 TSSOP | $\pm 2$ |
| MAX1166BCUP | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 TSSOP | $\pm 2$ |
| MAX1166CCUP | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 20 TSSOP | $\pm 4$ |
| MAX1166AEUP | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 TSSOP | $\pm 2$ |
| MAX1166BEUP ${ }^{\star}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 TSSOP | $\pm 2$ |
| MAX1166CEUP ${ }^{*}$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 20 TSSOP | $\pm 4$ |

*Future product-contact factory for availability

TRANSISTOR COUNT: 15,140
PROCESS: BiCMOS

Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface


## Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)


This datasheet has been download from:
www.datasheetcatalog.com
Datasheets for electronics components.

# Dual, $5 \Omega$ Analog Switches 

## General Description

The MAX4621/MAX4622/MAX4623 are precision, dual, high-speed analog switches. The single-pole/singlethrow (SPST) MAX4621 and double-pole/single-throw (DPST) MAX4623 dual switches are normally open (NO). The single-pole/double-throw (SPDT) MAX4622 has two normally closed (NC) and two NO poles. All three parts offer low $5 \Omega$ on-resistance guaranteed to match to within $0.5 \Omega$ between channels and to remain flat over the full analog signal range ( $\Delta 0.5 \Omega$ max). They also offer low leakage ( $<500$ pA at $+25^{\circ} \mathrm{C}, \angle 5 n A$ at $+85^{\circ} \mathrm{C}$ ) and fast switching times (turn-on time $<250 \mathrm{~ns}$, turn-off time <200ns).
These analog switches are ideal in low-distortion applications and are the preferred solution over mechanical relays in automatic test equipment or applications where current switching is required. They have low power requirements, use less board space, and are more reliable than mechanical relays.
The MAX4621/MAX4622/MAX4623 are pin-compatible replacements for the DG401/DG403/DG405, respectively , offering improved overall performance. These monolithic switches operate from a single positive supply $(+4.5 \mathrm{~V}$ to +36 V ) or with bipolar supplies ( $\pm 4.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$ ) while retaining CMOS-logic input compatibility.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Features

- Low On-Resistance: $3 \Omega$ (typ), $5 \Omega$ (max)
- Guaranteed Ron Match Between Channels ( $0.5 \Omega$ max)
- Guaranteed Break-Before-Make Operation (MAX4622)
- Guaranteed Off-Channel Leakage $<5 n A$ at $+85^{\circ} \mathrm{C}$
- Single-Supply Operation ( +4.5 V to +36 V )

Bipolar-Supply Operation ( $\pm 4.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$ )

- TTL/CMOS-Logic Compatible
- Rail-to-Rail ${ }^{\circledR}$ Analog Signal Handling Capability
- Pin Compatible with DG401/DG403/DG405

|  | Applications |
| :--- | :--- |
| Reed Relay Replacement | Military Radios |
| Test Equipment | PBX, PABX Systems |
| Communication Systems | Audio-Signal Routing |
| Data-Acquisition Systems | Avionics |

Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
| :--- | :--- | :--- |
| MAX4621CSE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 Narrow SO |
| MAX4621CPE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 16 Plastic DIP |

Ordering Information continued at end of data sheet.


For free samples \& the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 1-800-835-8769.

## Dual, $5 \Omega$ Analog Switches

```
ABSOLUTE MAXIMUM RATINGS
```

(Voltages Referenced to GND)


Continuous Power Dissipation ( $\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}$ )
Narrow SO (derate $8.70 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+70^{\circ} \mathrm{C}$ ) ............. 696 mW Narrow DIP (derate $10.53 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $+70^{\circ} \mathrm{C}$ ) .......... 842 mW Operating Temperature Ranges
MAX462_C $\qquad$ $.0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
MAX462 E $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
Storage Temperature Range $\qquad$ $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Lead Temperature (soldering, 10sec) $\qquad$ $+300^{\circ} \mathrm{C}$

Note 1: Signals on NO_, NC_, or COM_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Dual Supplies

$\left(\mathrm{V}+=+15 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{L}}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{~V}_{\mathrm{INH}}=+2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{I} L \mathrm{~L}}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |
| Input Voltage Range (Note 3) | VCOM_ VNO_, $\mathrm{VNC}_{-}$ |  |  | V- |  | V+ | V |
| On-Resistance | Ron | $\begin{aligned} & \mathrm{ICOM}_{-}=10 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}_{-}}= \pm 10 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 3 | 5 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 7 |  |
| On-Resistance Match Between Channels (Notes 3, 4) | $\Delta \mathrm{RoN}$ | $\begin{aligned} & \mathrm{ICOM}_{-}=10 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}}^{-} \end{aligned}= \pm 10 \mathrm{~V} .$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 0.25 | 0.5 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to TMAX |  |  | 0.7 |  |
| On-Resistance Flatness <br> (Notes 3, 5) | RFLAT(ON) | $\begin{aligned} & \mathrm{ICOM}_{-}=10 \mathrm{~mA} ; \\ & \mathrm{V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}_{-}}=-5 \mathrm{~V} \text {, } \\ & 0,5 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 0.2 | 0.5 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 0.7 |  |
| Off-Leakage Current (NO_ or NC_) (Note 6) | ${ }^{\prime} \mathrm{NO}_{-}, \mathrm{INC}^{\prime}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{NO}_{-} \text {or }} \mathrm{V}_{\mathrm{NC}_{-}}= \pm 10 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{COM}}=\mp 10 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.01 | 0.5 | nA |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -5 |  | 5 |  |
| COM_ Off-Leakage Current (Note 6) | ICOM_(OFF) | $\begin{aligned} & \mathrm{V}_{C O M}= \pm 10 \mathrm{~V} \\ & \mathrm{~V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=\mp 10 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.01 | 0.5 | nA |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -5 |  | 5 |  |
| COM_ On-Leakage Current (Note 6) | ICOM_(ON) | $\begin{aligned} & \mathrm{VCOM}_{\mathrm{CO}}= \pm 10 \mathrm{~V}, \\ & \mathrm{~V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=\mp 10 \mathrm{~V} \end{aligned}$or floating | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 | 0.02 | 1 | nA |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to TMAX | -10 |  | 10 |  |
| LOGIC INPUT |  |  |  |  |  |  |  |
| Input Current with Input Voltage High | IINH | VIN_ $=2.4 \mathrm{~V}$ |  | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
| Input Current with Input Voltage Low | IINL | $\mathrm{V}_{1} \mathrm{~N}_{-}=0.8 \mathrm{~V}$ |  | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
| Logic Input Voltage High | VINH |  |  | 2.4 |  |  | V |
| Logic Input Voltage Low | VINL |  |  |  |  | 0.8 | V |

## Dual, $5 \Omega$ Analog Switches

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

$\left(\mathrm{V}+=+15 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V}, \mathrm{VL}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{~V} \operatorname{INH}=+2.4 \mathrm{~V}, \mathrm{~V} \operatorname{INL}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| POWER SUPPLY |  |  |  |  |  |  |  |
| Power-Supply Range |  |  |  | $\pm 4.5$ |  | $\pm 20.0$ | V |
| Positive Supply Current | I+ | $\mathrm{V}_{1} \mathrm{~N}_{-}=0$ or 5 V | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -5 |  | 5 |  |
| Negative Supply Current | I- | $\mathrm{V} \mathrm{IN}_{-}=0$ or 5 V | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to TMAX | -5 |  | 5 |  |
| Logic Supply Current | IL | VIN_ $=0$ or 5 V | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -5 |  | 5 |  |
| Ground Current | IGND | $\mathrm{V} \mathrm{N}_{-}=0$ or 5 V | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to TMAX | -5 |  | 5 |  |
| SWITCH DYNAMIC CHARACTERISTICS |  |  |  |  |  |  |  |
| Turn-On Time | ton | $V_{C O M}= \pm 10 \mathrm{~V},$ <br> Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 120 | 250 | ns |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 325 |  |
| Turn-Off Time | toff | $V_{C O M}= \pm 10 \mathrm{~V},$ <br> Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 90 | 200 | ns |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 275 |  |
| Break-Before-Make Time Delay (MAX4622 only) | tD | $\mathrm{VCOM}_{-}= \pm 10 \mathrm{~V}$, Figure $3, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 5 | 25 |  | ns |
| Charge Injection | Q | $\begin{aligned} & C_{L}=1.0 n F, V_{G E N}=0, \text { RGEN }=0 \text {, Figure } 4, \\ & T_{A}=+25^{\circ} \mathrm{C} \end{aligned}$ |  |  | 480 |  | pC |
| Off-Isolation (Note 7) | VISO | $\mathrm{RL}_{\mathrm{L}}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}$, Figure $5, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | -62 |  | dB |
| Crosstalk (Note 8) | $\mathrm{V}_{\text {CT }}$ | $R \mathrm{~L}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}$, Figure 6, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | -60 |  | dB |
| NC_ or NO_ Capacitance | Coff | $\mathrm{f}=1 \mathrm{MHz}$, Figure 7, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 34 |  | pF |
| COM_ Off-Capacitance | Ссом | $\mathrm{f}=1 \mathrm{MHz}$, Figure 7, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 34 |  | pF |
| On-Capacitance | Ccom | $\mathrm{f}=1 \mathrm{MHz}$, Figure $8, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  | 150 |  | pF |

## Dual, $5 \Omega$ Analog Switches

## ELECTRICAL CHARACTERISTICS—Single Supply

$\left(\mathrm{V}+=+12 \mathrm{~V}, \mathrm{~V}-=0, \mathrm{VL}_{\mathrm{L}}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{VINH}=+2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ANALOG SWITCH |  |  |  |  |  |  |  |
| Input Voltage Range (Note 3) | VCOM_ VNO_, $\mathrm{V}_{\mathrm{NC}}$ |  |  | GND |  | V+ | V |
| On-Resistance | Ron | $\begin{aligned} & \mathrm{ICOM}_{-}=10 \mathrm{~mA}, \\ & \mathrm{~V}_{\mathrm{NO}}^{2} \\ & \text { or } \mathrm{V}_{\mathrm{NC}}^{-} \end{aligned}=10 \mathrm{~V} .$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 5.5 | 8 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\text {A }}=$ TMIN to $\mathrm{T}_{\text {MAX }}$ |  |  | 10 |  |
| On-Resistance Match Between Channels (Notes 3, 4) | $\Delta \mathrm{RoN}$ | $\begin{aligned} & \mathrm{ICOM}_{-}=10 \mathrm{~mA}, \mathrm{~V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}_{-}}=10 \mathrm{~V} \text {, } \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ |  |  | 0.2 | 0.5 | $\Omega$ |
| On-Resistance Flatness (Notes 3, 5) | RFLAT(ON) | $\begin{aligned} & \text { ICOM_ }=10 \mathrm{~mA} ; \mathrm{V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}_{-}}=3 \mathrm{~V}, 6 \mathrm{~V}, 9 \mathrm{~V} \text {; } \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ |  |  | 0.9 | 1.3 | $\Omega$ |
| NO_ or NC_ Off-Leakage Current (Notes 6, 9) | INO_(OFF), <br> INC_(OFF) | $\begin{aligned} & \mathrm{VCOM}_{-}=1 \mathrm{~V}, 10 \mathrm{~V} ; \\ & \mathrm{V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=10 \mathrm{~V}, 1 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.01 | 0.5 | nA |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -5 |  | 5 |  |
| COM_ Off-Leakage Current (Notes 6, 9) | ICOM_(OFF) | $\begin{aligned} & V_{C O M}^{-}=10 \mathrm{~V}, 1 \mathrm{~V} \\ & \mathrm{~V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=1 \mathrm{~V}, 10 \mathrm{~V} \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.01 | 0.5 | nA |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -5 |  | 5 |  |
| COM_ On-Leakage Current (Notes 6, 9) | ICOM_(ON) | $\begin{aligned} & V_{C O M}=10 \mathrm{~V}, 1 \mathrm{~V} ; \\ & \mathrm{V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=10 \mathrm{~V}, \\ & 1 \mathrm{~V} \text {, or floating } \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -1 | 0.02 | 1 | nA |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -10 |  | 10 |  |
| LOGIC INPUT |  |  |  |  |  |  |  |
| Input Current with Input Voltage High | IINH | $\mathrm{V}_{1} \mathrm{~N}_{-}=2.4 \mathrm{~V}$ |  | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
| Input Current with Input Voltage Low | IINL | $\mathrm{V} \mathrm{IN}_{-}=0.8 \mathrm{~V}$ |  | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
| Logic Input Voltage High | VINH |  |  | 2.4 |  |  | V |
| Logic Input Voltage Low | VINL |  |  |  |  | 0.8 | V |
| POWER SUPPLY |  |  |  |  |  |  |  |
| Power-Supply Range |  |  |  | 4.5 |  | 36.0 | V |
| Positive Supply Current | I+ | VIN_ $=0$ or 5 V | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=$ TMIN to TMAX | -5 |  | 5 |  |
| Logic Supply Current | IL | VIN_ $=0$ or 5 V | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to TMAX | -5 |  | 5 |  |
| Ground Current | IGND | $\mathrm{V} \mathrm{N}_{-}=0$ or 5 V | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | -0.5 | 0.001 | 0.5 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ | -5 |  | 5 |  |

## Dual, $5 \Omega$ Analog Switches

## ELECTRICAL CHARACTERISTICS—Single Supply (continued)

$\left(\mathrm{V}+=+12 \mathrm{~V}, \mathrm{~V}-=0, \mathrm{~V}_{\mathrm{L}}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{~V} \operatorname{INH}=+2.4 \mathrm{~V}, \mathrm{~V} \operatorname{INL}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.$ to $\mathrm{T}_{\mathrm{MAX}}$, unless otherwise noted. Typical values are $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SWITCH DYNAMIC CHARACTERISTICS |  |  |  |  |  |  |  |
| Turn-On Time (Note 3) | ton | $\mathrm{VCOM}_{-}=10 \mathrm{~V}$, Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 200 | 350 | ns |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 475 |  |
| Turn-Off Time (Note 3) | tofF | $\mathrm{VCOM}_{-}=10 \mathrm{~V}$, Figure 2 | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 100 | 200 | ns |
|  |  |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ |  |  | 300 |  |
| Break-Before-Make Time Delay (MAX4622 only) (Note 3) | tD | $R L=100 \Omega, C L=35 p F$, Figure 3, $T_{A}=+25^{\circ} \mathrm{C}$ |  | 10 | 75 |  | ns |
| Charge Injection | Q | $\mathrm{CL}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{V}_{\mathrm{GEN}}=0$, RGEN $=0$, Figure 4 |  |  | 45 |  | pC |
| Off-Isolation (Note 7) | VISO | $\mathrm{RL}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}$, Figure 5 |  |  | -62 |  | dB |
| Crosstalk (Note 8) | $\mathrm{V}_{\mathrm{C}}$ T | $\mathrm{RL}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}$, Figure 6 |  |  | -60 |  | dB |

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: $\Delta$ RON = RON_MAX - RON_MIN.
Note 5: Flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog signal range.
Note 6: Leakage currents are $100 \%$ tested at the maximum-rated hot temperature and guaranteed by correlation at $+25^{\circ} \mathrm{C}$.

Note 8: Between any two switches.
Note 9: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

## Dual, $5 \Omega$ Analog Switches

## Typical Operating Characteristics

( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)



ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)






## Dual, $5 \Omega$ Analog Switches

Pin Description

| PIN | NAME | FUNCTION |
| :---: | :---: | :---: |
| MAX4621 |  |  |
| 1, 8 | COM1, COM2 | Switch Common Terminal |
| 2-7 | N.C. | Not internally connected |
| 9, 16 | NO2, NO1 | Switch Normally Open Terminal |
| 10, 15 | IN2, IN1 | Digital Logic Inputs |
| 11 | V+ | Positive Supply-Voltage Input |
| 12 | VL | Logic Supply-Voltage Input |
| 13 | GND | Ground |
| 14 | V- | Negative Supply Voltage Input |
| MAX4622 |  |  |
| 1, 3, 6, 8 | COM_ | Switch Common Terminal |
| 2, 7 | N.C. | Not internally connected |
| 4, 5, 9, 16 | NC_, NO_ | Switch Normally Closed/Open Terminal |
| 10, 15 | IN2, IN1 | Digital Logic Inputs |
| 11 | V+ | Positive Supply-Voltage Input |
| 12 | VL | Logic Supply-Voltage Input |
| 13 | GND | Ground |
| 14 | V- | Negative Supply Voltage Input |
| MAX4623 |  |  |
| 1, 3, 6, 8 | COM_ | Switch Common Terminal |
| 2, 7 | N.C. | Not internally connected |
| 4, 5, 9, 16 | NO_ | Switch Normally Open Terminal |
| 10, 15 | IN2, IN1 | Digital Logic Inputs |
| 11 | V+ | Positive Supply-Voltage Input |
| 12 | VL | Logic Supply-Voltage Input |
| 13 | GND | Ground |
| 14 | V- | Negative Supply Voltage |

## Applications Information

## Operation with Supply Voltages Other than $\pm 15 \mathrm{~V}$

The MAX4621/MAX4622/MAX4623 switches operate with $\pm 4.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$ bipolar supplies and $\mathrm{a}+4.5 \mathrm{~V}$ to +36 V single supply. In either case, analog signals ranging from V+ to V-can be switched. The Typical Operating Characteristics graphs show the typical on-resistance variation with analog signal and supply voltage.

## Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. It is important not to exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence $V+$ on first, followed by $V_{L}, V_{-}$, and logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with the supply pins and a Schottky diode between V+ and VL (Figure 1). Adding diodes reduces the analog signal range to 1 V below V+ and 1V above V-, but low switch resistance and low leakage characteristics are unaffected. The difference between $V+$ and $V$ - should not exceed +44 V .


Figure 1. Overvoltage Protection Using Blocking Diodes

## Dual, $5 \Omega$ Analog Switches



Figure 2. Switching-Time Test Circuit


Figure 3. MAX4622 Break-Before-Make Test Circuit

$Q=\left(\Delta V_{0}\right)\left(C_{L}\right)$

Figure 4. Charge-Injection Test Circuit

## Dual， $5 \Omega$ Analog Switches



Figure 5．Off－Isolation

| FREQUENCY <br> TESTED | SIGNAL <br> GENERATOR | ANALYZER |
| :---: | :---: | :---: |
| 1 MHz | AUTOMATIC <br> SYNTHESIZER | TRACKING SPECTRUM <br> ANALYZER |

Figure 6．Crosstalk Test Circuit


Figure 7．Channel－On Capacitance


Figure 8．Channel－Off Capacitance

## Dual, $5 \Omega$ Analog Switches

_Cordering Information (continued)
Chip Information
TRANSISTOR COUNT: 82

Package Information


## Dual, $5 \Omega$ Analog Switches

Package Information (continued)


# Dual, $5 \Omega$ Analog Switches 

## NOTES

# Flags Used from Bit Addressable Ram <br> Communications Microcontroller 

| Flag | Description |
| :---: | :--- |
| 00 H | Set after first reading is stored as a reference value |
| 01 H | Set when the last cycle, for the high register for the number of bars, <br> are to be run |
| 02 H | Indicates that the system was paused |
| 03 H | Indicates to the "Wait for reading signal" loop that an error occurred |
| 04 H | Indicates to Reading Sub that the system is in manual mode \& the <br> Communications Microcontroller must not try to communicate with <br> the Automation Microcontroller |
| 05 H | Indicates to the Reading subroutine that multiple readings are being <br> taken and therefore the Communications Microcontroller must not try <br> to communicate with the Automation Microcontroller |

## Flags Used from Bit Addressable Ram Automation Microcontroller

| Flag | Description |
| :---: | :---: |
| 00H | FOR 3 ${ }^{\text {rd }}$ BAR PROCESS |
| 01H | FOR 3 ${ }^{\text {rd }}$ BAR PROCESS |
| 02H | FOR 3 ${ }^{\text {rd }}$ BAR PROCESS |
| 03H | FOR TIMER CYCLE COMPLETE - INDICATES ERROR1 |
| 04H | FLAG - EXTERNAL INTERRUPT 1 |
| 05H | TAKE TIMER READING ON $3{ }^{\text {RD }}$ BAR IN EX1ISR |
| 06H | ON $1^{\text {ST }}$ LOWERING OF DETECTION UNIT. |
| 07H | FOR TIMER CYCLE COMPLETE - INDICATES ERROR2 |
| 08H | EXTERNAL INTERRUPT 0 |
| 09H | To Indicate Pause has been entered |
| 0AH | To indicate to the Error 4 subroutine that Error 2 has occurred |
| 0BH | To indicate to Error 2 subroutine that Error 4 has occurred |
| 0CH | To Indicate to External Interrupt 0 that Run_Up subroutine was running when interrupted, and the timer value must not be logged. |
| 0DH | To indicate that error3 occurred and if there is a Run up error (error4) It must be ignored, so that power down is entered |
| 0EH | Set in ERROR READING PROCEDURE Subroutine to indicate to EX0 that interrupt was triggered in this subroutine, and must be ignored. |

Flag 06H was used because a stored value was reloaded for both the up and down count. On the first down count there is no stored value, so this flag is not set, and the 10s default value is loaded. But now a value is stored on the down count and reloaded for the up count. The flag is therefore no longer needed.

# Input / Output Port Utilization Communications Microcontroller - Communication \& Signaling 

| Communications Microcontroller (CM) - Communication \& Signaling |  |
| :---: | :---: |
| Port Number | Utilization |
| Port 0 |  |
| P0.0 (39) | O - Start / Analogue Switch on ADC line |
| P0.1 (38) | O-End |
| P0.2 (37) | I - Over-voltage Detection on the ADC In line |
| P0.3 (36) | $\mathbf{O}$ - Take Reading (Manual) |
| P0.4 (35) | $\mathbf{O}$ - Continue After Reading (Manual) \& Communication with AM |
| P0.5 (34) | $\mathbf{O}$ - Emergency Stop from GUI |
| P0.6 (33) | $\mathbf{O}$ - Automatic / Manual Toggle To u2 $\boldsymbol{\rightarrow} 0=$ MAN, $1=$ AUTO |
| P0.7 (32) | $\mathbf{O}$ - Continue After Reading (Automatic) |
| Port 1 |  |
| P1.0 (1) | I - A to D line |
| P1.1 (2) | I - A to D line |
| P1.2 (3) | $\mathbf{I}-\mathrm{A}$ to D line |
| P1.3 (4) | I - A to D line |
| P1.4 (5) | I - A to D line |
| P1.5 (6) | I-A to D line |
| P1.6 (7) | $\mathbf{I}-\mathrm{A}$ to D line |
| P1.7 (8) | I-A to D line |
| Port 2 |  |
| P2.0 (21) | O-ADC R/C pin |
| P2.1 (22) | I - ADC Waits for Low pulse from EOC - conversion complete |
| P2.2 (23) | I - Take Reading (Automatic) \& Communication with AM |
| P2.3 (24) | I - Increment No. Of Bars |
| P2.4 (25) | I - Error 1 - Pair Not Detected. |
| P2.5 (26) | I - Error 2 - Test Probes Not Lowered. |
| P2.6 (27) | I - Error 3 - Current On-Time Exceeded. |
| P2.7 (28) | $\mathbf{O}$ - Not Last Pair |
| Port 3 |  |
| P3.0 (10) | Serial Communication |
| P3.1 (11) | Serial Communication |
| P3.2 (12) | I - External Interrupt 0 - All Error Inputs Connected here as well/ manual emergency stop \& Safety Interlocks connected to AM P1.5 as well. |
| P3.3 (13) | O-ADC HBEN pin |
| P3.4 (14) | I - Error 4 - Test Probes Not Raised |
| P3.5 (15) | O- ADC CS pin |
| P3.6 (16) | I - Take Manual Reading Switch |
| P3.7 (17) | O - Led to indicate that the system is ready after power on and ADC initialization |

## Input / Output Port Utilization Automation Microcontroller - Automation Control

| Automation Microcontroller (AM) - Automation Control |  |
| :---: | :---: |
| Port Number | Utilization |
| Port 0 |  |
| P0.0 (39) | $\mathbf{O}$ - Take Reading (Automatic) |
| P0.1 (38) | $\mathbf{O}$ - Increment No. Of Bars |
| P0.2 (37) | O - Detection Unit Motor (Up) |
| P0.3 (36) | O - Detection Unit Motor (Down) |
| P0.4 (35) | $\mathbf{O}$ - Armature Drive Motor |
| P0.5 (34) | $\mathbf{O}$ - Set to clear D-FF on test detection signal (connected to CLR) |
| P0.6 (33) |  |
| P0.7 (32) |  |
| Port 1 |  |
| P1.0 (1) | I - Start |
| P1.1 (2) | I - End |
| P1.2 (3) |  |
| P1.3 (4) | I - Take Reading (Manual) |
| P1.4 (5) | I - Continue Test (Manual) |
| P1.5 (6) | I - Emergency Stop \& Safety Interlocks (Connect to ex0 of this uC as well) |
| P1.6 (7) | I - Automatic / Manual Toggle From u1 |
| P1.7 (8) | I - Continue After Reading (Automatic) |
| Port 2 |  |
| P2.0 (21) | O - Led to indicate probes r on the com b4 the current is to be switched on |
| P2.1 (22) | O - Led to indicate probes r on the com b 4 the current is to be switched off |
| P2.2 (23) |  |
| P2.3 (24) |  |
| P2.4 (25) |  |
| P2.5 (26) |  |
| P2.6 (27) | O - Error 4 - Test Probes Not Raised. |
| P2.7 (28) | $\mathbf{O}$ - Switch Test Current |
| Port 3 |  |
| P3.0 (10) | I - Not Last Pair |
| P3.1 (11) | I - Current On-Time Exceeded |
| P3.2 (12) | I - External Interrupt 0 - Test Probe Switch (Lowered) \& Emergency Stop from CM and AM P1.5 |
| P3.3 (13) | I - External Interrupt 1 - Bar Detection |
| P3.4 (14) |  |
| P3.5 (15) | O - Error 1 - Pair Not Detected. |
| P3.6 (16) | O - Error 2 - Test Probes Not Lowered. |
| P3.7 (17) | $\mathbf{O}$ - Error 3 - Current On-Time Exceeded. |

## Register Utilization

Communications Microcontroller

| Register Bank 0 |  |
| :---: | :---: |
| Register - R0 | High byte for number of bars |
| Register - R1 | Low byte for number of bars |
| Register - R2 | Value for percentage variance from first reading |
| Register - R3 | Holds the low byte 8-bit word from the A-D converter |
| Register - R4 | Holds the reference value (i.e. the first reading) |
| Register - R5 | Holds the high byte from adc |
| Register - R6 | Holds reference value minus the specified percentage variance |
| Register - R7 |  |
| Register Bank 1 |  |
| Register - R0 | Holds P0 values when the system is paused |
| Register - R1 | Holds P1 values when the system is paused |
| Register - R2 | Holds P2 values when the system is paused |
| Register - R3 | Holds P3 values when the system is paused |
| Register - R4 | Used for > 10ms delay for ADC's internal ref to "Wake" |
| Register - R5 | Used for $>10 \mathrm{~ms}$ delay for ADC's internal ref to "Wake" |
| Register - R6 | Used along with R4 and R5 to create a 1s delay after uC1 starts. This is for the tri-state buffers |
| Register - R7 |  |

## Registers Used - Microcontroller 2-Automation

| Register Bank 0 |  |
| :---: | :---: |
| Register - R0 | DELAYLOOP, LOOP COUNT |
| Register - R1 | LOAD TIMER HIGH REGISTER, SAFETY \& RECORDING ON $3^{\text {RD }}$ BAR |
| Register - R2 | LOAD TIMER LOW REGISTER, SAFETY \& RECORDING ON $3^{\text {RD }}$ BAR |
| Register - R3 | LOOP COUNT SAFETY AND RECORDING ON $3{ }^{\text {RD }}$ BAR |
| Register - R4 | HIGH BYTE OF TIMER VALUE TAKEN ON $3^{\mathrm{RD}}$ BAR |
| Register - R5 | LOW BYTE OF TIMER VALUE TAKEN ON $3^{\mathrm{RD}}$ BAR |
| Register - R6 | LOOP COUNT FOR RECORDING ON $3{ }^{\text {RD }}$ BAR |
| Register - R7 | LOOP COUNT FOR THE DETECTION UNIT |
| Register Bank 1 |  |
| Register - R0 | LOAD TIMER HIGH REGISTER, FOR THE DETECTION UNIT |
| Register - R1 | LOAD TIMER LOW REGISTER, FOR THE DETECTION UNIT |
| Register - R2 | Holds P0 values when the system is paused |
| Register - R3 | Holds P1 values when the system is paused |
| Register - R4 | Holds P2 values when the system is paused |
| Register - R5 | Holds P3 values when the system is paused |
| Register - R6 | LOAD TIMER HIGH REGISTER, FOR THE DETECTION UNIT |
| Register - R7 | LOAD TIMER LOW REGISTER, FOR THE DETECTION UNIT |
| Register Bank 2 |  |
| Register - R0 |  |
| Register - R1 |  |
| Register-R2 |  |
| Register - R3 |  |
| Register - R4 |  |
| Register - R5 |  |
| Register - R6 |  |
| Register - R7 |  |
| Register Bank 3 |  |
| Register - R0 |  |
| Register - R1 |  |
| Register - R2 |  |
| Register - R3 |  |
| Register - R4 |  |
| Register - R5 |  |
| Register-R6 |  |
| Register-R7 |  |

```
12-04-06 Micro1 16bitADC rly cal
    ;Date Last modified : 09-01-06
    ;Date Last modified : 07-03-06
    ;Date Last modified : 08-03-06
    ;Date Last modified : 23-03-05
;Date Last modified : 21-04-06
```

| ORG | OH |
| :--- | :--- |
| LJMP | MAIN |
| ORG | $0003 H$ |
| LJMP | EXOISR |
| ORG | $0023 H$ |
| LJMP | SPISR |

ORG 0030H


SETB P3.5

|  | CLR | RS0 | ; 1S |
| :---: | :---: | :---: | :---: |
|  | SETB | RSI |  |
|  | MOV | R6,\#50 |  |
| DLY3: | mov | r5, \#100 |  |
| dly: | mov | r4,\#100 |  |
| dly2: | djnz | r4, dly 2 |  |
|  | djnz | r5,dly |  |
|  | DJNZ | R6, DLY3 |  |
|  | CLR | RSO |  |
|  | CLR | RS1 | 1S |


| CLR | 00 H | ;CLEARING FLAGS |
| :--- | :--- | :--- |
| CLR | 01 H |  |
| CLR | 02 H |  |
| CLR | 03 H |  |
| CLR | 04 H |  |
| CLR | 05 H |  |



```
    RDG_SUB_DUMMY:NOP
    CLR RS0 ;TIME 4 INTERNAL REF TO "WAKE UP" AFTER SF
    mov r5,#100
adc 2nd:mov r4,#100
adc_dly:djnz r4,adc_dly
    djnz r5,adc_2nd
    CLR RSO
    CLR RS1 ;TIME 4 INTERNAL REE TO "WAKE UP" AFTER SF
    SETB P3.5; CS
    CLR P2.0
    NOP ; EXTRA TIME BEFORE CS IS FORCED LOW, NOT REALLY N
    CLR P3.5; AQUISITAION MODE, p3,5 cleared lus after p2.0 (1mach
```

ADC_W_DUMMY: JB P2.1.ADC_W_DUMMY ;EOC'
SETB P3.5
SETB P3.7
CLR RSO ;20US
SETB RS1
MOV R6,\#20
DJNZ R6,D2
CLR RSO
CLR RS1 ;20US
$\begin{array}{lll}\text { SETB } & \text { P2.0; TO PUT DATA OUT } \\ \text { NOP } & \text { EXTRA TIME BEFORE CS IS FORCED LOW, NOT REALLY NH } \\ \text { CLR } & \text { P3.5;***(CS EALLING eDGE 3) } \\ & & \\ \text { CLR } & \text { RS0 } & \text {;20US } \\ \text { SETB } & \text { RSI } & \\ \text { MOV } & \text { R6, \#20 } & \\ \text { DJNZ } & \text { R6,D3 } & \\ \text { CLR } & \text { RS0 } & \\ \text { CLR } & \text { RS1 } & \text {;20US }\end{array}$
NOP CIR 3. WAIT FOR VALID DATA, Tdo + Tdv ( $(t d v=0)$
CLR P3.3; ;HBEN - LOW BYTE
NOP ;tdol, MAY NEED MORE TIME
NOP
SETB P3.3 ;HBEN - HIGH BYTE
NOP ;tdo1, MAT NEED MORE TIME
NOB
SETB P3.5; *** (CS 1ST RISING EDGE AFTER fALLING eDGE 3)

```
    ;*********************************************************************
    ; MAIN - SERIAL INITIALIZITION - no PARITY - IN/OUT CHAR
MAIN2: MOV SCON,#01010000B
    MOV TMOD,#2OH
    MOV TH1,#-13
    SETB TRI
    MOV IE,#10000000B
    MOV IP,#00010000B; SET SP AT HIGHER PRIORIYY THAN EXO
    SETB ITO ;NEGATIVE EDE TRIGGERED
    ; SETB TR1
    ; SETB P2.0
    SETB ES
    JMP START
CH_OUT: CLR ES
    MOV SBUF,A
    ;CLR ACC.7 ;may not need 21/11, but check
TX2: JNB TI,TX2
    CLR TI
    SETB ES ; COME BACK TO THIS
    RET
;*********************************************************************
START: Cjne A,#'A',CAL; SRL1, wait for all the data to be in the nb b.
CAL: CJNE A,#'H',START ; 4 CALIB
    CLR PO.6 ; IN MAN MODE FOR CALIBRATION
    SETB 04H
    CALL RDG_SUB
    CLR 04H
    SETB PO.6
    JMP START ; 4 CALIB
NB_AM: MOV A,#'b'; SEND PROMPT, FOR MAN/AUTO
    CALI CH_OUT
SRL2: CJNE A,#'G',X ; G->MAN
; reading is taken each time the man sw is pressed and exits when end is p:
manRsub:NOP
W_ENDx: CJNE A,#'B',TK_RDx
    LJMP EINISH
```

| TK_RDx: JNB | P3.6, manRsub; MAN SWITCH |
| :---: | :--- |
| TK_RDx2: JB | P3.6,TK_RDx2' |

X: CJNE A, \#'g',SRL2
CLR $C$; A should hold ' $g$ '
SETB PO. 6

MOV A,\#'d'; SEND PROMPT \& WAIT FOR START PULSE
CALL CH OUT
WT_STRT:CJNE A, \#'A',WT_STRT ; START PULSE TO U2
jmp fstbar
WT_U2ST: JNB P2.3,WT_U2ST ; LOOP STARTS
fstbar: JMP BARS

; DEC NO OF BARS FROM THE TOTAL IN U1 HERE
; ALSO CHECK FOR LAST BAR - IF YES, ALLERT NB
; THEN WAIT FOR THE "END"PULSE FROM NB AND JUMP TO END

GO: SETB P0.0; START TO U2 / ANA SW ON

SETB P2.7 ; NOT LAST BAR
BGN_TW: JNB P2.2,BGN_TW ; WAIT TO CHECK IF PULSE WAS RECIEVED
CLR P2.7 ; tō u2 to signal last bar
CLR PO.O, ANA SW OFF
SETB EXO
NOP
NOP
NOP
NOP
WT_RDNG: JNB P2.2,WT_RDNGE ; WAIT FOR TAKE READING PULSE
SETB PO.7; TOU2 TO CONT AFTER READING TAKEN
NOP
NOP
NOP
CLR PO.7

```
12-04-06 Microl 16bitADC rly cal
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```
    CALL RDG SUB
    JMP WT Ũ2ST; LOOP ENDS NORMALLY
WT_RDNGE:JNB 03\overline{H},WT_RDNG
    CLR 03H
    JMP WT_U2ST; LOOP ENDS AFTER ERROR 1 ND 2
```

; EXTERNAL INTERRUPT O ISR - FOR ERRORS 1 TO 4 \& Emergency Stop

READING SUBPROGRAM
RDG_SUB:NOP

| $;$ NEG_TST: JB | P3.6,NO_NEG |  |
| :--- | :--- | :--- |
| $;$ | MOV | A, \#'N'_ |
| $;$ | CALL | CH_OUT |
| ; NEG_R: | CJNE | A, \#'C',NEG_R |
| $;$ | JMP | NEG_TST |

NO_NEG: JB
04H,NO_COM

```
    12-04-06 Microl 16bitADC rly cal
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```
    ;EXTRA 1S DELAY IN UC2 (X) 4 INPUT CCTRY
    OV_CHK: JNB PO.2,DWN ; for pcb, for tst cct, jb p0.2
    DWN: LJMP OVRVVOI
    FET_ON: SETB PO.O ; ANA SW ON
        CLR P2.0
        CLR RSO ;20US
        SETB RS1
        MOV R6,#24
    D4: DJNZ R6,D4
        CLR RSO
        CLR RS1 ;20US
        CLR P3.5; AQUISITAION MODE, p3,5 cleared lus after p2.0 (1mach
        CLR RS0 ;20US
        SETB RS1
        MOV R6,#20
D5: DJNZ R6,D5
    CLR RSO
    CLR RS1 ;20US
    NOP ;Tcsl and tdh
    SETB P3.5
        CLR RS0 ;20US
        SETB RS1
        MOV R6,#24
D6: DJNZ R6,D6
    CLR RSO
    CLR RS1 ;20US
    CLR P3.5; FOR STANDBY MODE ***(CS fALLING eDGE 2)
ADC_W: JB P2.1,ADC_W ;EOC'
    SETB P3.5
    SETB P2.0; TO PUT DATA OUT
        CLR P3.3; ;HBEN - LOW BYTE nu 28/11
        NOP ; EXTRA TIME BEFORE CS IS FORCED LOW, NOT REALLY Nl
        CLR P3.5; ***(CS fALLING eDGE 3)
```



```
    CALL
    CH_OUT
    WT_NBC: CJNE A,#'E',WT_100E ; WAIT FOR CONTINUE FROM NB
WT_100E: CJNE A,#'S',WT_NBC; WAIT FOR end of 100 reading cycle FROM NB
RDG_EDS:JB 04H,NO_COM2
        JB 05H,NO-COM2
        SETB PO.7; TO U2 TO CONT AFTER READING TAKEN
        RG_EDS: JNB P2.2,RG_EDS
        CLR PO.7
        CLR PO.0 ; ANA SW OFF
NO_COM2:RET
    ERROR 1 SUB
ERI_SUB:MOV A,#'J'
E1E2: NOP CH_OUT
MAN_RDG:CJNE A,#'D',E1E2
    ;SETB P3.7
    SETB PO.3
TK_RDG2:JB P3.6,TK_RDG2
    SETB P0.4 ;TEL U2 SWITCH I ON
E1_CK1: JNB P2.2,E1_CK1
    JB P2.2,$
    CLR P0.4
E3_RDNG:JNB P2.2,E3_RDNG ; WAIT FOR TAKE READING PULSE
    SETB PO.7; TO}\mathrm{ U2 TO CONT AFTER READING TAKEN
        NOP
        NOP
        NOP
        CLR PO.7
        CALL RDG SUB
        ;CLR P3.7.7
        CLR P0.3
E_CON: CJNE A,#'C',E_CON ;29/01/06
    SETB PO.4
E1_WT: JNB P2.2.E1_WT ; CHECK IF U2 RECIEVED EXIT PULSE
    CLR P0.4
    NOP
        NOP
        RET
;******************************************************
;******************************************************
```

```
    ER2_SUB:MOV A,#'m'
    CALI CH OUT
    CALL E1E2
    RET
;*****************************************************
;*****************************************************
; ERROR 3 SUB
;*****************************************************
ER3 SUB:MOV A,#'L'
    CALL CH OUT
    JMP CRNT_E ; IN SPISR TO ENTER POWERDOWN IF CURRENT ON TIME IS
    RET
; SEE PREV VERSION FOR NOTES
;*********************************************************
;******************************************************
; ERROR 4 SUB
;*****************************************************
\begin{tabular}{rl} 
ER4_SUB:MOV & A, \#'Q' \\
CALL & CH OUT
\end{tabular}
E3E4: NOP -
WT_NBC3:CJNE A,#'C',E3E4 ; WAIT FOR CONTINUE FROM NB
E3_WT: JNB P2.2,E3_WT ; CHECK IF U2 RECIEVED EXIT PULSE
    CLR P0.4
    RET
;******************************************************
;*****************************************************
; SERIAL PORT ISR
SPISR: CLR EX0 ;? needed? 06/12
    JNB TI,REC
    ;CLR TI; cleared in ch_out
    JMP SP_OUT
REC: NOP
SLCH_IN:JNB RI,$
    CLR RI
    MOV A,SBUF
    CJNE A,#'B',SPNXT ; END
ENDD: SETB PO.1; END TO U2
SP_END: JNB P3.4,SP_END; ERROR 4 PULSE USED TO
                                ; ENSURE THAT U2 IS ABOUT TO END
    CLR PO.I
    MOV PO,#OH
    MOV P1,#OH
    MOV P2,#OH
    MOV P3,#00000011B
    MOV PCON,#O0000010B;POWER DOWN, ONLY EXIT IS RESET
    NOP
```

```
12-04-06 Microl 16bitADC rly cal
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12-04-06 Micro1 16bitADC rly cal

```
; Date Last modified : 09-01-06
;Date Last modified : 07-03-06
;Date Last modified : 08-03-06
;Date Last modified : 23-03-06
;Date Last modified : 21-04-06
```

| ORG | OH |
| :--- | :--- |
| LJMP | MAIN |
| ORG | 0003 H |
| LJMP | EXOISR |
| ORG | $0023 H$ |
| LJMP | SPISR |

ORG 0030 H


SETB P3. 5

|  | CLR | RS0 | ;1S |
| :--- | :--- | :--- | :--- |
|  | SETB | RS1 |  |
| DLY3: | MOV | R6,\#50 |  |
| mov | r5,\#100 |  |  |
| dly2: | mov | r4,\#100 |  |
|  | djnz | r4,dly2 |  |
|  | djnz | r5,dly |  |
|  | DJNZ | R6, DLY3 |  |
|  | CLR | RS0 |  |
|  | CLR | RS1 | $; 1 S$ |


| CLR | 00 H | ; CLEARING FLAGS |
| :--- | :--- | :--- |
| CLR | 01 H |  |
| CLR | 02 H |  |
| CLR | 03 H |  |
| CLR | 04 H |  |
| CLR | 05 H |  |



```
12-04-06 Microl 16bitADC rly cal
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```
RDG_SUB_DUMMY:NOP
    CLR RSO ;TIME 4 INTERNAL REF TO "WAKE UP" AFTER SF
    REIB RSI
    mov r5,#100
adc 2nd:mov r4,#100
adc_dly:djnz r4,adc dly
    djnz r5,adc-2nd
    CLR RSO
    CLR RSI ;TIME 4 INTERNAL REF TO "WAKE UP" AFTER SE
```

    SETB P3.5; CS
    CLR P2.0
    NOP ; EXTRA TIME BEFORE CS IS FORCED LOW, NOT REALLY N
    CLR P3.5; AQUISITAION MODE, p3,5 cleared 1us after p2.0 (1mach
    ADC_W_DUMMY: JB P2.1,ADC_W_DUMMY ;EOC'
$\begin{array}{ll}\text { SETB } & \text { P3.5 } \\ \text { SETB } & \text { P3.7 }\end{array}$
CLR RSO ;20US
SETB RS1
MOV R6,\#20
D2: DJNZ R6,D2
CLR RSO
CLR RSI ;20US
SETB P2.0; TO PUT DATA OUT
NOP ; EXTRA TIME BEFORE CS IS FORCED LOW, NOT REALLY NI
CLR P3.5;*** (CS EALLING eDGE 3)
CLR RSO ;20US
SETB RSI
MOV R6,\#20
D3: DJNZ R6,D3
CLR RSO
CLR RSI ;20US
NOP ; WAIT EOR VALID DATA, Tdo+Tdv (tdv = 0)
CLR P3.3; ;HBEN - LOW BYTE
NOP ;tdo1, MAY NEED MORE TIME
NOP
SETB P3.3 ; HBEN - HIGH BYTE
NOP ; tdo1, MAT NEED MORE TIME
NOP
SETB P3.5; $* * *$ (CS 1ST RISING EDGE AFTER fALLING eDGE 3)

```
    ;*****************************************************************
    MOV IE,#10000000B
    MOV IP,#00010000B; SET SP AT HIGHER PRIORIYY THAN EXO
    SETB ITO ; NEGATIVE EDE TRIGGERED
    ; SETB TRI
    ;SETB P2.0
    SETB ES
    JMP START
    CH_OUT: CLR ES
        MOV SBUF,A
        ;CLR ACC.7 ;may not need 21/11, but check
        TX2: JNB TI,TX2
        CLR TI
        SETB ES ; COME BACK TO THIS
        RET
; ********************************************************************
START: cjne A,#'A',CAL; SRL1, wait for all the data to be in the nb b.
CAL: CJNE A,#'H',START ; 4 CALIB
    CLR PO.6 ;IN MAN MODE EOR CALIBRATION
    SETB 04H
    CALI RDG_SUB
    CLR 04H
    SETB PO.6
    JMP START ; 4 CALIB
NB_AM: MOV A,#'b'; SEND PROMPT, FOR MAN/AUTO
    CALI CH_OUT
SRL2: CJNE A,#'G',X ; G->MAN
; reading is taken each time the man sw is pressed and exits when end is p:
manRsub:NOP
W_ENDx: CJNE A,#'B',TK_RDx
        LJMP FINISH
```

| TK_RDX: JNB | P3.6, manRsub ; MAN SWITCH |
| :---: | :--- |
| TK_RDx2: JB | P3.6,TK_RDx2' |


| X : | CJNE | A, \#'g', SRL2 |
| :---: | :---: | :---: |
|  | CLR | C; A should hold 'g' |
|  | SETB | P0.6 |

MOV A,\#'d'; SEND PROMPT \& WAIT FOR START PULSE CALL CH_OUT
WT_STRT:CJNE A, \#'A',WT_STRT ; START PULSE TO U2
jmp fstbar
WT U2ST:JNB P2.3,WT_U2ST ; LOOP STARTS fst̄bar: JMP BARS


```
    CALL RDG SUB
    JMP WT U}2ST; LOOP ENDS NORMALLY
WT_RDNGE:JNB 03\overline{H},WT RDNG
    CLR 03H
JMP WT_U2ST; LOOP ENDS AFTER ERROR I ND 2
```

; EXTERNAL INTERRUPT 0 ISR - FOR ERRORS 1 TO 4 \& Emergency Stop



```
;
READING SUBPROGRAM
```

RDG_SUB:NOP

| $;$ NEG_TST: JB | P3.6,NO_NEG |  |
| :--- | :--- | :--- |
| $;$ | MOV | A, \#'N' |
| $;$ | CALL | CH_OUT |
| ; NEG_R: | CJNE | A, \#'C',NEG_R |
| $;$ | JMP | NEG_TST |

NO_NEG: JB 04H,NO_COM

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12-04-06 Micro1 16bitADC rly cal
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|  | JB $05 H$, NO_COM <br> WT_RD:  <br> JNB P 2.2, WT RD ; WAIT FOR CURRENT TO BE SWITCHED BY U2 <br> SETB P0.7; TO U2 TO SIGNAL READY TO TAKE READING <br> NOP  |  |
| :--- | :--- | :--- |
| NOP | P0.7 |  |
| CLR |  |  |

; EXTRA 1 S DELAY IN Uc2 (X) 4 INPUT CCTRY


|  | CLR | P2.0 |  |
| :--- | :--- | :--- | :--- |
|  |  |  |  |
|  | CLR | RS0 |  |
|  | SETB | RS1 |  |
| D4: | MOV | R6,\#24 |  |
|  | DJNZ | R6,D4 |  |
|  | CLR | RS0 | ;20US |

CLR P3.5; AQUISITAION MODE, p3,5 cleared Ius after p2.0 (1mach
CLR RSO ;20US
SETB RSI
MOV R6,\#20
D5: DJNZ R6,D5
CLR RSO
CLR RS1 ;20US
NOP ;TCSI and tdh
SETB P3.5
CLR RSO ;20US
SETB RS1
MOV R6,\#24
D6: DJNZ R6,D6
CLR RSO
CLR RS1 ;20US
CLR P3.5; FOR STANDBY MODE *** (CS fALLING eDGE 2)

ADC_W: JB P2.1,ADC_W ;EOC ${ }^{\prime}$
SETB P3.5
SETB P2.0; TO PUT DATA OUT
CLR P3.3; ;HBEN - LOW BYTE nu 28/11
NOP ; EXTRA TIME BEFORE CS IS FORCED LOW, NOT REALLY NI
CLR P3.5; *** (CS fALLING eDGE 3)

```
12-04-06 Microl 16bitADC rly cal
```



```
    CALL
                                CH_OUT
        WT_NBC: CJNE A,#'E',WT_100E ; WAIT EOR CONTINUE FROM NB
            JMP RDG SUB
        WT_100E:CJNE A,#'S',WT_NBC; WAIT EOR end of 100 reading cycle EROM NB
        RDG_EDS:JB 04H,NO COM2
            JB 05H,NO-
            SETB PO.7; TO U2 TO CONT AFTER READING TAKEN
        RG_EDS: JNB P2.2,RG_EDS
        CLR PO.7
        CLR PO.O ; ANA SW OFF
    NO COM2:RET
; ERROR 1 SUB
ERI_SUB:MOV A,#'J'
    CALL CH_OUT
E1E2: NOP
MAN_RDG:CJNE A,#'D',E1E2
    ; SETB P3.7
    SETB P0.3
TK_RDG: JNB P3.6,TK_RDG ; MAN RDNG SWITCH, wait for switch to be pres:
TK_RDG2:JB P3.6,TK_RDG2
    SETB P0.4 ;TEL U2 SWITCH I ON
E1_CK1: JNB P2.2,E1_CK1
    JB P2.2,$
    CLR P0.4
E3_RDNG:JNB P2.2,E3_RDNG ; WAIT FOR TAKE READING PULSE
    SETB PO.7; TOU U2 TO CONT AFTER READING TAKEN
    NOP
    NOP
    NOP
    CLR P0.7
    CALL RDG SUB
    ;CLR P3.7
    CLR P0.3
E_CON: CJNE A,#'C',E_CON ;29/01/06
    SETB PO.4
E1_WT: JNB P2.2,E1_WT ; CHECK IE U2 RECIEVED EXIT PULSE
    NOP
    NOP
    RET
l
```

```
\begin{tabular}{rl} 
ER2_SUB: MOV & A, \#'m' \\
CALI & CH_OUT \\
CALI & E1E2 \\
RET &
\end{tabular}
;******************************************************
;*****************************************************
; ERROR 3 SUB
;******************************************************
ER3_SUB:MOV A,#'L'
                            CALL CH_OUT
                            JMP CRNT_E ; IN SPISR TO ENTER POWERDOWN IF CURRENT ON TIME IS
; SEE PREV VERSION FOR NOTES
;**********************************************************
;******************************************************
ER4_SUB:MOV A,#'Q'
E3E4: NOP
WT_NBC3:CJNE A,#'C',E3E4 ; WAIT FOR CONTINUE FROM NB
    SETB P0.4
E3_WT: JNB P2.2,E3_WT ; CHECK IF U2 RECIEVED EXIT PULSE
    CLR PO.4
    RET
;******************************************************
; SERIAL PORT ISR
SPISR: CLR EX0 ;? needed? 06/12
    JNB TI,REC
    ;CLR TI; cleared in ch_out
    JMP SP OUT
REC: NOP
SLCH_IN:JNB RI,$
    CLR RI
    MOV A,SBUF
    CJNE A,#'B',SPNXT ; END
ENDD: SETB PO.1; END TO U2
SP_END: JNB P3.4,SP_END; ERROR 4 PULSE USED TO
                                    ; ENSURE THAT U2 IS ABOUT TO END
    CLR PO.1
    MOV PO,#OH
    MOV P1,#0H
    MOV P2,#OH
    MOV P3,#00000011B
    MOV PCON,#O0000010B;POWER DOWN, ONLY EXIT IS RESET
```

```
12-04-06 Micro1 16bitADC rly cal
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| EINISH: | CLR | EXO |
| :--- | :--- | :--- |
|  | SETB | PO.I; END TO U2 |
|  | CLR | EA ; DISABLE INTERUPT AS THE P3.4 IS USED FOR SIGNALLING |

WX_END: JNB P3.4,WX_END; ERROR 4 PULSE USED TO
; ENSURE THAT U2 IS ABOUT TO END

| EXT: | MOV | PO, \#OH |
| :--- | :--- | :--- |
|  | MOV | PI,\#OH |
|  | MOV | P2,\#0H |
|  | MOV | P3,\#00000011B |
|  | MOV | PCON, \#00000010B; POWER DOWN, ONLY EXIT IS RESET |
| MOV | PCON,\#00000001B ;IDLE MODE, system remains in idle mode ur |  |
|  | NOP |  |

```
12-04-06 Micro2 latest
;Date Last modified : 09-01-06
;Date Last modified : 07-03-06
;
;Date Last modified : 23-03-06
; Date Last modified : 21-04-06
```


ORG OH
LJMP MAIN
ORG 0003H
LJMP EXOISR
ORG 0013H
LJMP EXIISR

| COUNT | EQU | -10000 | ; DELAY | LOOP |
| :--- | :--- | :--- | :--- | :--- |
| COUNT2 | EQU | -50000 | ; SAFTY | TIME |

    ORG 0030 H
    MAIN: MOV TMOD,\#00010001B
MOV IP,\#00000001B
MOV IE,\#00000101B

12-04-06 Micro2 latest

AUTO: | SETB | P0.5; |
| :--- | :--- |
| nop | $;$ |
| nop | $;$ |
| nop | $;$ |
| nop | ; |
| CLR | P0.5; |
| SETB | EX1 |
| SETB | EX0 |



|  | SETB | P0.1 |
| :---: | :---: | :---: |
|  | CLR | 0 CH |
|  | CALL | DELAYLOOP |
| NLBAR: | JNB | P3.0, LBAR |
|  | JMP | CONT |
| LBAR: | JNB | P1.1, NLBAR |
|  | CLR | P0.1 |
|  | LJMP | END |
| CONT: | SETB | P0. 0 |
| PW: | JNB | P3.0, PW |
|  | NOP |  |
|  | NOP |  |
|  | NOP |  |
|  | NOP |  |
|  | CLR | P0. 0 |
|  | CLR | P0. 1 |
|  | JB | 02H, LOAD; *nu |
|  | JB | OOH, ONE |
|  | SETB | 00H |
|  | JMP | LOAD |
| ONE: | JB | 01H, TWO |
|  | SETB | 01H |
|  | JMP | LOAD |
| TWO: | JB | 02H,LOAD |
|  | SETB | 02H |
|  | CLR | 00H |
|  | CLR | 01H |
|  | JMP | NTRD |
| LOAD: | JB | 02H, THIRD |
| NTRD: | MOV | R1, \#HIGH COUNT2 |
|  | MOV | R2, \#LOW COUNT2 |
|  | MOV | R3, \#200 ;* |


|  | JMP | BEGIN |
| :---: | :---: | :---: |
| THIRD: | MOV | A, R 4 |
|  | MOV | R1, A |
|  | MOV | A, R 5 |
|  | MOV | R2, A |
|  | MOV | A, R6 |
|  | MOV | R3, A |
|  | MOV | A, \#200 ; * |
|  | CALL | CALC_TIME |
|  | SETB | P0. 4 |
|  | CALL | DELAYLOOP |
| CNT_RT: | MOV | TH1, \#HIGH COUNT2 |
|  | MOV | TL1, \#LOW COUNT2 |
|  | SETB | TR1 |
| WAIT_R: | JNB | TF1, WAIT_R |
|  | clr | tri |
|  | clr | 七f1 |
|  | DJNZ | R3, CNT_RT |
|  | JB | 04H, TMR_OUT |
|  | MOV | TH1, R1 |
|  | MOV | TL1, R2 |
|  | SETB | TR1 |
| WAIT_RX: | : JNB | TF1,WAIT_RX |
|  | Clr | trl |
|  | clr | 七f1 |
|  | SETB | 03H |
|  | JMP | TMR_OUT |
| BEGIN: | SETB | P0. 4 |
|  | CALL | DELAYLOOP |
| TMR: | MOV | THO, \#OH |
|  | MOV | TLO, \#OH |
|  | MOV | TH1, R1 |
|  | MOV | TL1, R2 |
|  | SETB | TRI |
|  | SETB | TRO |
| WAIT_T1: | JNB | TE1,WAIT_T1 |
|  | clr | trl |
|  | CLR | TR0 |
|  | clr | tfl |
|  | CLR | TFO |
|  | DJNZ | R3, TMR |
|  | SETB | 03H |
|  | JMP | TMR_OUT |

CALC TIME

| CALC_TIME: | CLR | C |
| :--- | :--- | :--- |
|  | SUBB | A, R3 |
|  | MOV | R3, A |
|  | CLR | C |
|  | CLR | AC |

```
                                    CLR OV
                                    MOV A,R2
                                    CPL A
                                    ADD A,#1
                                    MOV R2,A
                    MOV A,RI
                    CPL A
                    JNC SUM
                CLR C; ;08/12
                ADD A,#1
                JNC SUM; ;08/12
                MOV A,#255; ;08/12
                MOV R1,A
                CLR C
                CLR AC
                CLR OV
\begin{tabular}{lll} 
GO1: & MOV & A, R3 \\
& MOV & B, \#5 \\
& DIV & AB \\
& ADD & A, R3 \\
& JNC & TOLL \\
& MOV & R3, \#255 \\
& CLR & C \\
& MOV & R3, A \\
& CLR & OV \\
& CLR & AC \\
& RET &
\end{tabular}
\begin{tabular}{cc} 
TMR_OUT: & CLR \\
JB & \(04 \mathrm{H}, \mathrm{NO}\) ERR1 \\
CALL & ERRORI
\end{tabular}
\begin{tabular}{|c|c|}
\hline NO_ERRI:CLR & O4H \\
\hline SETB & EX1 \\
\hline TMP & \\
\hline
\end{tabular}
```

```
;
.********* EXTERNAL INTERUPT 1 - ISR - v2
```

EXIISR: | CLR | P0. 4 |
| :--- | :--- |
| SETB | P0.5; |
| nOp | $;$ |
| nOp | $;$ |
| nOp | $;$ |
| nOp | $;$ |
| CLR | PO. $5 ;$ |
| CALL | DELAYLOOP |



CALL READING


CALL RUN UP

| EXR1OUT: MOV | TH1,\#-10 |
| ---: | :--- |
| MOV | TL1,\#-10 |
| MOV | R3,\#1 |
| SETB | TR1 |
| RETI |  |

EXOISR: jnb P1.5,no_stop
ljmp end
no_stop:JB OEH,IG
CLR PO. 2
CLR PO. 3
JNB $0 \mathrm{CH}, \mathrm{S}$
CLR P2. 7 ; CURRENT OEF
S: CLR TRI ;04/06
CLR TRO ;04/06
CALL DELAYLOOP
SETB 08H
JB 0 CH, EXROOUT
; SETB 06 H
; SETB 06H ; 06/12
MOV B,R3
MOV R7,B

| CLR | RSO | ; |  |  |
| :--- | :--- | :--- | :--- | :--- |
| SETB | RS1 | ;REG BANK 1 |  |  |
| MOV | R1,TH0 |  |  |  |
| MOV | R2,TLO |  |  |  |
| CLR | RSO | ; |  |  |
| CLR | RS1 | ;REG BANK | 0 |  |
|  |  |  |  |  |
| MOV | R3,\#1H |  |  |  |


|  | EXR0OUT: CLR | OCH |
| :--- | :--- | :--- |
|  | MOV | TH1, \#-10 |
|  | MOV | TL1, \#-10 |
|  | MOV | R3,\#1 |
|  | SETB | TR1 |
| IG: | RETI |  |

## ; DELAY LOOP

DELAYLOOP: MOV R0,\#100;1SEC = 100X10000
RPT: MOV THO, \#HIGH COUNT
MOV TLO,\#LOW COUNT
SETB TRO
DLY: JNB TEO,DLY
CLR TRO
CLR TFO
DJNZ R0,RPT
RET

$\begin{array}{cc}\text { RUN_DWNX: SETB } & \text { EXO } \\ \text { CLR } & 0 \mathrm{CH}\end{array}$
SETB P2.7; CUTTENT ON
CALL DELAYLOOP
;JB 06H,DECT 2 ; 25-08
MOV R1,\#HIGH COUNT2
MOV R2,\#LOW COUNT2
MOV R3,\#200 ;*
SETB P0. 3
CALL DELAYLOOP
TMR2: MOV THO, \#OH
MOV TLO, \#OH
MOV TH1,R1
MOV TL1,R2
SETB TR1
SETB TRO
WAIT_T2:JNB TF1,WAIT_T2
clr tri
CLR TR0
clr tfi
CLR TFO
DJNZ R3,TMR2

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| SETB | 07 H |
| :--- | :--- |
| JMP | TMR_OUT2 |


| TMR_OUT2: $\boldsymbol{C l}$ CLR | EX0 |
| :---: | :--- |
| JB | O8H,NO_ERR2 |
| CALL | ERROR2 |
| SETB | EX0 |
| JMP | EXR1OUT |


| NO_ERR2: SETB | EXO |
| :---: | :---: |
| CLR | 08 H |

    RET
    ; RUN_UP SUB - rAISE DETECTION UNIT

| RUN_UP: | SETB <br> SETB | EXO |
| :--- | :--- | :--- |
| OCH |  |  |
| DECT_3: | CLR | RSO; |
|  | SETB | RSI; $;$ |

MOV A,R1

MOV B, R2
CLR RSO;
CLR RSI; REG BANKO

MOV R1,A
MOV R2,B
MOV A,R7
MOV R3,A
MOV A,\#200 ;*
CALL CALC_TIME
SETB P0.2
CALL DELAYLOOP

| CNT_DN: | MOV | TH1, \#HIGH COUNT2 |
| ---: | :--- | :--- |
|  | MOV | TL1, \#LOW COUNT2 |
|  | SETB | TR1 |

WAIT_D: JNB TFI,WAIT_D
clr tri
clr tfi
DJNZ R3,CNT_DN
JB $08 \mathrm{H}, \mathrm{TMR}$ OUT3; EX0 OCCURED SO SKIP
MOV TH1,R1
MOV TL1,R2
SETB TR1
WAIT_DX:JNB TF1,WAIT_DX
clr tr1
clr tf1
SETB 07H

```
\begin{tabular}{ll} 
JB & O8H,NO_ERR3 \\
JB & ODH,NO_ERR3 \\
CALL & ERROR4 \\
SETB & EXO \\
JMP & OUT2
\end{tabular}
\begin{tabular}{rr} 
NO_ERR3:CLR & 08 H \\
CLR & 0 DH
\end{tabular}
\begin{tabular}{lll} 
OUT2: & SETB & EXO \\
& CLR & 0 CH \\
& CLR & 0 DH \\
& CLR & 08 H
\end{tabular}
RET
READING:SETB PO.0
RD_WT: JNB P1.7,RD_WT
CLR PO.O
; SETB P2.7
; CALI DELAYLOOP
; SETB PO. 6
NOP
NOP
CALL DELAYLOOP
SETB PO.O
RDNG0: JNB P1.7,RDNGO
CLR P0.0
CALL DELAYLOOP
RDNG: JNB P1.7,RDNGX
JMP RDNGOK
RDNGX: JB P3.1,RDNG; 555 output is high for thr preset time ofter \(t\) :
CALL ERROR3
CLR PO.O
JMP OUT2
RDNGOK: SETB P0.0
NOP
NOP
CLR PO.O
; CLR P0.6
NOP
NOP
; CLR P2.7
; CALL DELAYLOOP
JB P3.1,cnt_chk
CALL ERROR3
cnt chk: RET
;
```

ERROR1: CLR PO.4
JB 05H,Sl ;
JNB 02H,SI ;
MOV R4,\#HIGH COUNT2 ;
MOV R5,\#LOW COUNT2 ;
MOV B,\#200 ;
MOV R6,B
CLR 05H ; *nU IF ERR OCCURS ON 3RD PAIR, THEN TIME READING
CLR 02H ; "
SETB 00H ; "
SETB 01H ; ABOVE 4 ERROR ON 3RD BAR, BUT NOT REALLY REQUIREC
S1: SETB P0.5 ;
nOp ;
nop ;
nop ;
nop ;
nop ;
nop ;
nop ;
CLR P0.5 ;
SETB P3.5 ;TO MIC1
CALL ER_I_SW
CLR P3.5
RET
; ERROR 2 - TEST PROBES NOT LOWERED
ERROR2: CLR P0.3
CLR P2.7
CALL DELAYLOOP
SETB OAH
JB 08H,NO_RELD ;23-03-06 reload values for run_up
CLR TRI ;cos EX0 is not triggered on Erर̄ror 2
CLR TRO
MOV B,R3
MOV R7,B
CLR RSO ;
SETB RSI ;REG BANK I
MOV R1,THO
MOV R2,TLO
CLR RSO ;
CLR RS1 ;REG BANK 0 ;23-03-06 reload values for run_up
NO RELD:CALL RUN UP
; SEE NOTE HERE IN P\overline{REVIOUS VERSIONS OF CODE}
JB OBH,E2_OUT
SETB P3.6 ;TO MIC1
CALL ER_I_SW
CLR P3.6
E2_OUT: CLR OAH
CLR OBH
RET

```

```

    CLR P2.0
    PRBS_WT:JB P3.2,PRBS_WT
CALL DELAYLOOP
JB P3.2,PRBS_WT
;CALL DELAYLOOP
SETB P0.0
NOP
NOP
CLR PO.0
CALL READING
E1_HLD: JNB P1.4,E1_HLD
SETB PO.0
NOP
NOP
CLR PO.0
AGN2: JB P3.2,OF_I
SETB P2.1
JMP AGN2
OF_I: CALL DELAYLOOP
CLR P2.7
CLR P2.1
CALL DELAYLOOP
;SETB EXO ;? needed?06/12
CLR OEH
RET
END: MOV PO,\#OH
MOV P1,\#OH
MOV P2,\#OH
MOV P3,\#OH
SETB P2.6
MOV PCON,\#00000010B;POWER DOWN
NOP
END

```

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```

    ; Date Last modified : 09-01-06
    ; Date Last modified : 07-03-06
    ;
; Date Last modified : 23-03-06
; Date Last modified : 21-04-06

```


```

| ORG | OH |
| :--- | :--- |
| LJMP | MAIN |
| ORG | $0003 H$ |
| LJMP | EXOISR |
| ORG | $0013 H$ |
| LJMP | EXIISR |


| COUNT | EQU | -10000 ; DELAY LOOP |
| :--- | :--- | :--- |
| COUNT2 | EQU | -50000 ; SAFTY TIME |

    ORG 0030H
    MAIN: MOV TMOD,\#00010001B
MOV IP,\#00000001B
MOV IE,\#00000101B
;******************************iNTILIZE I/O PORTS ******************************
MOV PO,\#OH ; only for sim, input ports must be set to 1
MOV P1,\#11111111B ; only for sim, input ports must be set to 1
MOV P2,\#00001000H ; only for sim, input ports must be set to 1
MOV P3,\#00011111B ; only for sim, input ports must be set to 1
;*****************************iNTILIZE I/O PORTS *****************************
; clearing all flags
CLR OOH
CLR 01H
CLR 02H
CLR 03H
CLR 04H
CLR 05H
CLR 06H
CLR 07H
CLR 08H
CLR 09H
CLR OAH
CLR OBH
CLR OCH
CLR ODH
CLR OEH
SETB EA
SETB IT1
SETB ITO
AGIAN: SETB EXI; ENABLE EX INTI
START: JNB P1.0, START
JB P1.6, AUTO ; (1 = AUTO, 0 = MAN )
MOV PCON,\#00000010B ;

```
```

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```
AUTO: \begin{tabular}{lr} 
SETB & P0.5; \\
nop & \(;\) \\
nop & \(;\) \\
nop & \(;\) \\
nop & ; \\
CLR & P0.5; \\
SETB & EX1 \\
SETB & EX0
\end{tabular}

\begin{tabular}{|c|c|c|}
\hline \multirow[t]{3}{*}{} & SETB & PO. 1 \\
\hline & CLR & OCH \\
\hline & CALL & DELAYLOOP \\
\hline \multirow[t]{2}{*}{NLBAR:} & JNB & P3.0, LBAR \\
\hline & JMP & CONT \\
\hline \multirow[t]{3}{*}{LBAR:} & JNB & P1. 1, NLBAR \\
\hline & CLR & P0. 1 \\
\hline & LJMP & END \\
\hline CONT: & SETB & P0. 0 \\
\hline \multirow[t]{11}{*}{PW:} & JNB & P3.0, PW \\
\hline & NOP & \\
\hline & NOP & \\
\hline & NOP & \\
\hline & NOP & \\
\hline & CLR & P0.0 \\
\hline & CLR & PO. 1 \\
\hline & JB & 02H,LOAD; *nu \\
\hline & JB & OOH, ONE \\
\hline & SETB & OOH \\
\hline & JMP & LOAD \\
\hline \multirow[t]{3}{*}{ONE:} & JB & 01H, TWO \\
\hline & SETB & 01H \\
\hline & JMP & LOAD \\
\hline \multirow[t]{5}{*}{TWO:} & JB & 02H, LOAD \\
\hline & SETB & 02H \\
\hline & CLR & 00H \\
\hline & CLR & 01H \\
\hline & JMP & NTRD \\
\hline LOAD: & JB & 02H, THIRD \\
\hline \multirow[t]{3}{*}{NTRD:} & MOV & R1, \#HIGH COUNT2 \\
\hline & MOV & R2, \#LOW COUNT2 \\
\hline & MOV & R3, \#200 ; * \\
\hline
\end{tabular}

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```

        JMP BEGIN
    THIRD: MOV A,R4
            MOV R1,A
            MOV A,R5
            MOV R2,A
            MOV A,R6
            MOV R3,A
            MOV A,#200 ;*
            CALL CALC TIME
            SETB PO.4
            CALI DELAYLOOP
    CNT_RT: MOV TH1,\#HIGH COUNT2
MOV TL1,\#LOW COUNT2
SETB TRI
WAIT_R: JNB TF1,WAIT_R
clr trl
clr tf1
DJNZ R3,CNT RT
JB 04H,TMR OUT
MOV TH1,R1
MOV TL1,R2
SETB TR1
WAIT_RX:JNB TF1,WAIT_RX
clr trl
clr tfl
SETB 03H
JMP TMR OUT
BEGIN: SETB PO.4
CALL DELAYLOOP
TMR: MOV THO,\#OH
MOV TLO,\#OH
MOV TH1,R1
MOV TL1,R2
SETB TRI
SETB TRO
WAIT_T1:JNB TFI,WAIT_T1
clr trl
CLR TRO
clr tf1
CLR TFO
DJNZ R3,TMR
SETB 03H
JMP TMR_OUT
CALC_TIME
CALC TIME:
CLR C
SUBB A,R3
MOV R3,A
CLR C
CLR AC

```
```

GO1: MOV A,R3
MOV B,\#5
DIV AB
ADD A,R3
JNC TOLL
MOV R3,\#255
CLR C
TOLL: MOV R3,A
CLR OV
CLR AC
RET

| TMR_OUT:CLR | EX1 |
| :---: | :---: |
| JB | 04 H, | NO_ERR1

    CALL ERROR1
    NO_ERR1:CLR 04H
SETB EX1
JMP AUTO

```
```

; EXTERNAL INTERUPT 1 - ISR - v2

```

EX1ISR: CLR P0.4
SETB PO.5;
nop ;
nop ;
nop ;
nop ;
CLR PO.5;
CALL DELAYLOOP
```

12-04-06 Micro2 latest

```


CALL READING


CALL RUN_UP
\begin{tabular}{|c|c|}
\hline EXRIOUT: MOV & TH1, \#-10 \\
\hline MOV & TL1, \#-10 \\
\hline MOV & R3, \#1 \\
\hline SETB & TR1 \\
\hline RETI & \\
\hline
\end{tabular}
```

; EXTERNAL INTERUPT 0 - ISR - v2

```

EXOISR: jnb P1.5,no_stop
ljmp end
no_stop:JB OEH,IG
CLR PO.2
CLR P0.3
JNB \(\quad 0 \mathrm{CH}, \mathrm{S}\)
CLR P2.7 ; CURRENT OFF
S: CLR TRI ;04/06
CLR TRO;04/06
CALL DELAYLOOP
SETB 08H
JB OCH,EXROOUT
; SETB 06H
; SETB 06H ; 06/12
MOV B,R3
MOV R7,B
\begin{tabular}{lllll} 
CLR & RSO & ; & & \\
SETB & RS1 & ;REG BANK 1 \\
MOV & R1,THO & & & \\
MOV & R2,TLO & & & \\
CLR & RSO & ; & & \\
CLR & RS1 & ;REG BANK & 0 \\
& & MOV & R3,\#1H & \\
& & & &
\end{tabular}
\begin{tabular}{|c|c|}
\hline EXROOUT: CLR & OCH \\
\hline MOV & TH1, \#-10 \\
\hline MOV & TL1, \#-10 \\
\hline MOV & R3, \#1 \\
\hline SETB & TR1 \\
\hline IG: RETI & \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|}
\hline \multicolumn{3}{|l|}{; DELAY LOOP} \\
\hline \multicolumn{3}{|l|}{} \\
\hline \multirow[t]{4}{*}{DELAYLOOP: RPT:} & MOV & R0, \#100; 1SEC = \\
\hline & MOV & TH0, \#HIGH COUNT \\
\hline & MOV & TLO, \#LOW COUNT \\
\hline & SETB & TRO \\
\hline \multirow[t]{4}{*}{DLY:} & JNB & TEO, DLY \\
\hline & CLR & TR0 \\
\hline & CLR & TFO \\
\hline & DJNZ & R0, RPT \\
\hline
\end{tabular}

RET
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{}} \\
\hline & \\
\hline RUN_DWNX:SETB & EXO \\
\hline CLR & OCH \\
\hline SETB & P2.7; CUTTENT ON \\
\hline CALL & DELAYLOOP \\
\hline ; JB & 06H, DECT 2 ; 25-08 \\
\hline MOV & R1, \#HIGH COUNT2 \\
\hline MOV & R2, \#LOW COUNT2 \\
\hline MOV & R3, \#200 ; * \\
\hline SETB & P0. 3 \\
\hline CALL & DELAYLOOP \\
\hline TMR2: MOV & THO, \#OH \\
\hline MOV & TLO, \#OH \\
\hline MOV & TH1, R1 \\
\hline MOV & TL1,R2 \\
\hline SETB & TR1 \\
\hline SETB & TRO \\
\hline WAIT_T2:JNB & TE1,WAIT_T2 \\
\hline Clr & trl \\
\hline CLR & TRO \\
\hline clr & tfI \\
\hline CLR & TE0 \\
\hline DJNZ & R3, TMR2 \\
\hline
\end{tabular}
```

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| SETB | 07 H |
| :--- | :--- |
| JMP | TMR_OUT2 |

```
\begin{tabular}{rl} 
TMR_OUT2: \(;\) CLR & \multicolumn{1}{c}{ EXO } \\
JB & 08H,NO_ERR2 \\
CALL & ERROR2 \\
SETB & EX0 \\
JMP & EXR1OUT
\end{tabular}
NO_ERR2: SETB \(\quad\) EX0

RUN_UP: SETB EXO
SETB OCH

DECT_3: CLR RSO;
SETB RSI; REG BANKI
\begin{tabular}{ll} 
MOV & A,R1 \\
MOV & B,R2 \\
& \\
CLR & RS0; \\
CLR & RS1; REG BANK0
\end{tabular}

MOV R1,A
MOV R2,B
MOV A,R7
MOV R3,A
MOV A, \#200 ; *
CALL CALC_TIME
SETB PO.2
CALL DELAYLOOP
```

CNT_DN: MOV THI,\#HIGH COUNT2
MOV TL1,\#LOW COUNT2
SETB TRI
WAIT_D: JNB TF1,WAIT_D
clr trl
clr tf1
DJNZ R3,CNT_DN
JB 08H,TMR OUT3; EX0 OCCURED SO SKIP
MOV TH1,R1
MOV TL1,R2
SETB TR1
WAIT_DX:JNB TE1,WAIT_DX
clr trl
clr tf1
SETB 07H

```
```

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| JB | O8H,NO_ERR3 |
| :--- | :--- |
| JB | ODH, NO_ERR3 |
| CALL | ERROR4 |
| SETB | EXO |
| JMP | OUT2 |

NO_ERR3:CLR $\quad 08 \mathrm{H}$

| OUT2: | SETB | EXO |
| :--- | :--- | :--- |
|  | CLR | 0 CH |
|  | CLR | 0 DH |
|  | CLR | 08 H |

    RET
    ;***********************************
READING:SETB PO.0
RD_WT: JNB P1.7,RD_WT
CLR P0.0
;SETB P2.7
;CALL DELAYLOOP
;SETB PO.6
NOP
NOP
CALI DELAYLOOP
SETB PO.0
RDNGO: JNB P1.7,RDNGO
CLR PO.0
CALL DELAYLOOP
RDNG: JNB P1.7,RDNGX
JMP RDNGOK
RDNGX: JB P3.1,RDNG ; 555 output is high for thr preset time ofter t:
CALL ERROR3
CLR PO.O
JMP OUT2
RDNGOK: SETB PO.O
NOP
NOP
CLR PO.0
;CLR P0.6
NOP
NOP
;CLR P2.7
;CALL DELAYLOOP
JB P3.1,cnt_chk
CALL ERROR3
cnt_chk:RET

```
;
```

ERROR1: CLR PO.4
JB 05H,SI ;
JNB 02H,SI ;
MOV R4,\#HIGH COUNT2 ;
MOV R5,\#LOW COUNT2 ;
MOV B,\#200 ;
MOV R6,B
CLR 05H ; *nu IF ERR OCCURS ON 3RD PAIR, THEN TIME READING
CLR 02H ; "
SETB 00H ; "
SETB 01H ; ABOVE 4 ERROR ON 3RD BAR, BUT NOT REALLY REQUIRED
S1: SETB P0.5 ;
nop ;
nop ;
nop ;
nop ;
nop ;
nop ;
nop ;
CLR PO.5 ;
SETB P3.5 ;TO MIC1
CALL ER_I_SW
CLR P3.5
RET
; E********************************************************
ERROR2: CLR P0.3
CLR P2.7
CALL DELAYLOOP
SETB OAH
JB 08H,NO_RELD ;23-03-06 reload values for run_up
CLR TR1 ; cos EX0 is not triggered on Er\overline{ror}2
CLR TRO
MOV B,R3
MOV R7,B
CLR RSO ;
SETB RS1 ;REG BANK 1
MOV R1,TH0
MOV R2,TLO
CLR RSO ;
CLR RSI ;REG BANK 0 ;23-03-06 reload values for run_up
NO RELD:CALL RUN UP
; SEEE NOTE HERE IN P\overline{REVIOUS VERSIONS OF CODE}
JB OBH,E2 OUT
SETB P3.6 ;\overline{TO MIC1}
CALL ER_I_SW
CLR P3.6-
E2_OUT: CLR OAH
CLR OBH
RET

```


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\begin{tabular}{|c|c|c|}
\hline & CLR & P2.0 \\
\hline \multicolumn{2}{|l|}{PRBS_WT:JB} & P3.2, PRBS WT \\
\hline & CALL & DELAYLOOP \\
\hline & JB & P3.2, PRBS WT \\
\hline & ; CALL & DELAYLOOP \\
\hline & SETB & PO. 0 \\
\hline & NOP & \\
\hline & NOP & \\
\hline & CLR & P0. 0 \\
\hline & CALI & READING \\
\hline \multirow[t]{5}{*}{E1_HLD:} & JNB & P1.4, E1_HLD \\
\hline & SETB & P0.0 - \\
\hline & NOP & \\
\hline & NOP & \\
\hline & CLR & P0.0 \\
\hline \multirow[t]{3}{*}{AGN2:} & JB & P3.2,OF_I \\
\hline & SETB & P2.1 \\
\hline & JMP & AGN2 \\
\hline \multirow[t]{7}{*}{OF_I:} & CALL & DELAYLOOP \\
\hline & CLR & P2.7 \\
\hline & CLR & P2.1 \\
\hline & CALL & DELAYLOOP \\
\hline & ; SETB & EX0 ; ? needed?06/12 \\
\hline & CLR & OEH \\
\hline & RET & \\
\hline \multicolumn{3}{|l|}{} \\
\hline \multirow[t]{8}{*}{END:} & MOV & PO, \#OH \\
\hline & MOV & P1, \#OH \\
\hline & MOV & P2, \#0H \\
\hline & MOV & P3, \#0H \\
\hline & SETB & P2. 6 \\
\hline & MOV & PCON, \#OOO00010B; POWER DOWN \\
\hline & NOP & \\
\hline & END & \\
\hline
\end{tabular}

\footnotetext{

}





\(\qquad\)


Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
Operating Free Air Temperature Range
DM54LS and 54LS
DM74LS
Storage Temperature Range

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Symbol} & \multirow[t]{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS00} & \multicolumn{3}{|c|}{DM74LS00} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\text {CC }}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{lOL}^{\text {l }}\) & Low Level Output Current & & & 4 & & & 8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & DM54 & 2.5 & 3.4 & & V \\
\hline & & & DM74 & 2.7 & 3.4 & & \\
\hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
\hline & & & DM74 & & 0.35 & 0.5 & \\
\hline & & \(\mathrm{IOL}=4 \mathrm{~mA}\), & DM74 & & 0.25 & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -0.36 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C C}=M a x \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -20 & & -100 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 0.8 & 1.6 & mA \\
\hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 2.4 & 4.4 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 3 & 10 & 4 & 15 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 3 & 10 & 4 & 15 & ns \\
\hline \multicolumn{7}{|l|}{Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).} \\
\hline
\end{tabular}




Physical Dimensions inches (millimeters) (Continued)


14-Lead Ceramic Flat Package (W) Order Number 54LS00FMQB or DM54LS00W NS Package Number W14B

\section*{LIFE SUPPORT POLICY}

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
\begin{tabular}{|c|c|c|c|}
\hline \begin{tabular}{l}
National Semiconductor Corporation \\
1111 West Bardin Road \\
Arlington, TX 76017 \\
Tel: 1(800) 272-9959 \\
Fax: 1(800) 737-7018
\end{tabular} & \begin{tabular}{l}
National Semiconductor Europe \\
Fax: (+49) 0-180-530 8586 \\
Email: cnjwge@tevm2.nsc.com \\
Deutsch Tel: \((+49)\) 0-180-530 8585 \\
English Tel: \((+49)\) 0-180-532 7832 \\
Français Tel: \((+49)\) 0-180-532 9358 \\
Italiano Tel: (+49) 0-180-534 1680
\end{tabular} & \begin{tabular}{l}
National Semiconductor Hong Kong Ltd. \\
13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong \\
Tel: (852) 2737-1600 \\
Fax: (852) 2736-9960
\end{tabular} & \begin{tabular}{l}
National Semiconductor Japan Ltd. \\
Tel: 81-043-299-2309 \\
Fax: 81-043-299-2408
\end{tabular} \\
\hline
\end{tabular}

This datasheet has been download from:
www.datasheetcatalog.com
Datasheets for electronics components.
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{3}{|l|}{FRIRPHILD} & & \multicolumn{2}{|r|}{May 1986} \\
\hline \multicolumn{6}{|l|}{SEMICONDபСTロRTM} \\
\hline \multicolumn{6}{|l|}{DM74LS02} \\
\hline \multicolumn{6}{|l|}{Quad 2-Input NOR Gate} \\
\hline \multicolumn{6}{|l|}{General Description} \\
\hline \multicolumn{6}{|l|}{This device contains four independent gates each of which performs the logic NOR function.} \\
\hline \multicolumn{6}{|l|}{Ordering Code:} \\
\hline Order Number & Package Number & \multicolumn{4}{|c|}{Package Description} \\
\hline DM74LS02M & M14A & \multicolumn{4}{|l|}{14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow} \\
\hline DM74LS02SJ & M14D & \multicolumn{4}{|l|}{14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide} \\
\hline DM74LS02N & N14A & \multicolumn{4}{|l|}{14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide} \\
\hline \begin{tabular}{l}
Devices also available \\
Connectio
\end{tabular} & \begin{tabular}{l}
in Tape and Reel. Specify \\
n Diagram
\end{tabular} & by appending the suffix &  & ¢

B
L
H
L
H & \begin{tabular}{c} 
Output \\
\hline \(\mathbf{Y}\) \\
\hline H \\
L \\
L \\
L
\end{tabular} \\
\hline
\end{tabular}

Absolute Maximum Ratings(Note 1)
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 7 V \\
Operating Free Air Temperature Range & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note 1: The "Absolute Maximum Ratings" are those values beyond which he safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrica Characteristics tables are not guaranteed at the absolute maximum ratings The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{l|l|c|c|c|c}
\hline \multicolumn{1}{c|}{ Symbol } & \multicolumn{1}{|c|}{ Parameter } & Min & Nom & Max & Units \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{~V}_{\mathrm{IH}}\) & HIGH Level Input Voltage & 2 & & & V \\
\hline \(\mathrm{~V}_{\mathrm{IL}}\) & LOW Level Input Voltage & & & 0.8 & V \\
\hline \(\mathrm{I}_{\mathrm{OH}}\) & HIGH Level Output Current & & & -0.4 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & LOW Level Output Current & & & 8 & mA \\
\hline \(\mathrm{~T}_{\mathrm{A}}\) & Free Air Operating Temperature & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & Conditions & Min &  & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}\) & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & HIGH Level Output Voltage & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max}, \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\] & 2.7 & 3.4 & & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{2}{*}{LOW Level Output Voltage} & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\] & & 0.35 & 0.5 & \multirow[t]{2}{*}{V} \\
\hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & & 0.25 & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\) & & & 0.1 & mA \\
\hline IIH & HIGH Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\) & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & LOW Level Input Current & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\) & & & -0.40 & mA \\
\hline l OS & Short Circuit Output Current & \(\mathrm{V}_{\text {CC }}=\operatorname{Max}\) (Note 3) & -20 & & -100 & mA \\
\hline \({ }^{\text {CCH }}\) & Supply Current with Outputs HIGH & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 1.6 & 3.2 & mA \\
\hline \(\mathrm{I}_{\mathrm{CCL}}\) & Supply Current with Outputs LOW & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) & & 2.8 & 5.4 & mA \\
\hline
\end{tabular}

Note 2: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

\section*{Switching Characteristics}
at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=\mathbf{2} \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(\mathrm{t}_{\text {PLH }}\) & Propagation Delay Time LOW-to-HIGH Level Output & & 13 & & 18 & ns \\
\hline \(\overline{t_{\text {PHL }}}\) & Propagation Delay Time HIGH-to-LOW Level Output & & 10 & & 15 & ns \\
\hline
\end{tabular}

Physical Dimensions inches (millimeters) unless otherwise noted



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
 Fairchild reserves the right at any time without notice to change said circuitry and specifications.

\section*{LIFE SUPPORT POLICY}

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
www.fairchildsemi.com

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Datasheets for electronic components.

\section*{- Dependable Texas Instruments Quality and Reliability \\ description}

These devices contain six independent inverters.

SN5404 . . J J PACKAGE
SN54LS04, SN54S04 . . J OR W PACKAGE SN7404 . . D, N, OR NS PACKAGE SN74LS04... D, DB, N, OR NS PACKAGE SN74S04...D OR N PACKAGE (TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE (TOP VIEW)


NC - No internal connection

ORDERING INFORMATION
\begin{tabular}{|c|c|c|c|c|}
\hline \(\mathrm{T}_{\mathbf{A}}\) & \multicolumn{2}{|r|}{PACKAGE \(\dagger\)} & \begin{tabular}{l}
ORDERABLE \\
PART NUMBER
\end{tabular} & TOP-SIDE MARKING \\
\hline \multirow{11}{*}{\(0^{\circ} \mathrm{C}\) to \(70^{\circ} \mathrm{C}\)} & \multirow{3}{*}{PDIP - N} & Tube & SN7404N & SN7404N \\
\hline & & Tube & SN74LS04N & SN74LS04N \\
\hline & & Tube & SN74S04N & SN74S04N \\
\hline & \multirow{5}{*}{SOIC - D} & Tube & SN7404D & 7404 \\
\hline & & Tube & SN74LS04D & \multirow[b]{2}{*}{LS04} \\
\hline & & Tape and reel & SN74LS04DR & \\
\hline & & Tube & SN74S04D & \multirow[t]{2}{*}{S04} \\
\hline & & Tape and reel & SN74S04DR & \\
\hline & \multirow[b]{2}{*}{SOP - NS} & Tape and reel & SN7404NSR & SN7404 \\
\hline & & Tape and reel & SN74LS04NSR & 74LS04 \\
\hline & SSOP - DB & Tape and reel & SN74LS04DBR & LS04 \\
\hline \multirow{11}{*}{\(-55^{\circ} \mathrm{C}\) to \(125^{\circ} \mathrm{C}\)} & \multirow{6}{*}{CDIP - J} & Tube & SN5404J & SN5404J \\
\hline & & Tube & SNJ5404J & SNJ5404J \\
\hline & & Tube & SN54LS04J & SN54LS04J \\
\hline & & Tube & SN54S04J & SN54S04J \\
\hline & & Tube & SNJ54LS04J & SNJ54LS04J \\
\hline & & Tube & SNJ54S04J & SNJ54S04J \\
\hline & \multirow{3}{*}{CFP - W} & Tube & SNJ5404W & SNJ5404W \\
\hline & & Tube & SNJ54LS04W & SNJ54LS04W \\
\hline & & Tube & SNJ54S04W & SNJ54S04W \\
\hline & \multirow[t]{2}{*}{LCCC - FK} & Tube & SNJ54LS04FK & SNJ54LS04FK \\
\hline & & Tube & SNJ54S04FK & SNJ54S04FK \\
\hline
\end{tabular}
\(\dagger\) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each inverter)
\begin{tabular}{|c|c|}
\hline \begin{tabular}{c} 
INPUT \\
\(\mathbf{A}\)
\end{tabular} & \begin{tabular}{c} 
OUTPUT \\
\(\mathbf{Y}\)
\end{tabular} \\
\hline\(H\) & \(L\) \\
\(L\) & \(H\) \\
\hline
\end{tabular}
logic diagram (positive logic)


INSTRUMENTS
schematics (each gate)


Resistor values shown are nominal.

\section*{absolute maximum ratings over operating free-air temperature range (unless otherwise noted) \(\dagger\)}
```

Supply voltage, VCC (see Note 1)
7V
Input voltage, 採: '04, 'S04 ...................................................................... 5.5 V
'LS04 ............................................................................................

```

```

    DB package .......................................96
    N package ............................................. 800}\textrm{C}/\textrm{W
    NS package .....................................76
    Storage temperature range, T}\mp@subsup{T}{\mathrm{ stg}}{
-65*}\textrm{C}\mathrm{ to }15\mp@subsup{0}{}{\circ}\textrm{C
$\dagger$ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

```
recommended operating conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{}} & \multicolumn{3}{|c|}{SN5404} & \multicolumn{3}{|c|}{SN7404} & \multirow[b]{2}{*}{UNIT} \\
\hline & & MIN & NOM & MAX & MIN & NOM & MAX & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High-level input voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low-level input voltage & & & 0.8 & & & 0.8 & V \\
\hline \({ }^{\text {I OH }}\) & High-level output current & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{I}^{\text {I }}\) & Low-level output current & & & 16 & & & 16 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Operating free-air temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{PARAMETER} & \multicolumn{3}{|c|}{\multirow[b]{2}{*}{TEST CONDITIONS \(\ddagger\)}} & \multicolumn{3}{|c|}{SN5404} & \multicolumn{3}{|c|}{SN7404} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & & MIN & TYP§ & MAX & MIN & TYP§ & MAX & \\
\hline \(\mathrm{V}_{\text {IK }}\) & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \(\mathrm{I}=-12 \mathrm{~mA}\) & & & & -1.5 & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \(\mathrm{V}_{\text {IL }}=0.8 \mathrm{~V}\), & \(\mathrm{I} \mathrm{OH}=-0.4 \mathrm{~mA}\) & 2.4 & 3.4 & & 2.4 & 3.4 & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \(\mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}\), & \(\mathrm{IOL}=16 \mathrm{~mA}\) & & 0.2 & 0.4 & & 0.2 & 0.4 & V \\
\hline 1 & \(V_{C C}=\) MAX, & \(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\) & & & & 1 & & & 1 & mA \\
\hline IIH & \(V_{C C}=\) MAX, & \(\mathrm{V}_{\mathrm{I}}=2.4 \mathrm{~V}\) & & & & 40 & & & 40 & \(\mu \mathrm{A}\) \\
\hline ILL & \(V_{C C}=\) MAX, & \(\mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\) & & & & -1.6 & & & -1.6 & mA \\
\hline Ios \({ }^{1}\) & \(V_{C C}=\) MAX & & & -20 & & -55 & -18 & & -55 & mA \\
\hline ICCH & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\), & \(\mathrm{V}_{\mathrm{I}}=0 \mathrm{~V}\) & & & 6 & 12 & & 6 & 12 & mA \\
\hline \(\mathrm{I}_{\mathrm{CCL}}\) & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\), & \(\mathrm{V}_{\mathrm{I}}=4.5 \mathrm{~V}\) & & & 18 & 33 & & 18 & 33 & mA \\
\hline
\end{tabular}
\(\ddagger\) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
I Not more than one output should be shorted at a time.
switching characteristics, \(\mathrm{V}_{\mathbf{C C}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathbf{2 5}{ }^{\circ} \mathrm{C}\) (see Figure 1)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{PARAMETER} & \multirow[t]{2}{*}{FROM (INPUT)} & \multirow[t]{2}{*}{TO (OUTPUT)} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{TEST CONDITIONS}} & \multicolumn{3}{|c|}{\[
\begin{aligned}
& \hline \text { SN5404 } \\
& \text { SN7404 }
\end{aligned}
\]} & \multirow[t]{2}{*}{UNIT} \\
\hline & & & & & MIN & TYP & MAX & \\
\hline tPLH & \multirow[t]{2}{*}{A} & \multirow[t]{2}{*}{Y} & \multirow[t]{2}{*}{\(\mathrm{R}_{\mathrm{L}}=400 \Omega\),} & \multirow[t]{2}{*}{\(C_{L}=15 \mathrm{pF}\)} & & 12 & 22 & \multirow{2}{*}{ns} \\
\hline tPHL & & & & & & 8 & 15 & \\
\hline
\end{tabular}

SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS
SDLS029B - DECEMBER 1983 - REVISED FEBRUARY 2002
recommended operating conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{}} & \multicolumn{3}{|c|}{SN54LS04} & \multicolumn{3}{|c|}{SN74LS04} & \multirow[b]{2}{*}{UNIT} \\
\hline & & MIN & NOM & MAX & MIN & NOM & MAX & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High-level input voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low-level input voltage & & & 0.7 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {I }}\) & High-level output current & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{I}_{\mathrm{OL}}\) & Low-level output current & & & 4 & & & 8 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Operating free-air temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{PARAMETER} & \multicolumn{3}{|c|}{\multirow[b]{2}{*}{TEST CONDITIONS \(\dagger\)}} & \multicolumn{3}{|c|}{SN54LS04} & \multicolumn{3}{|c|}{SN74LS04} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & & MIN & TYP\# & MAX & MIN & TYPキ & MAX & \\
\hline \(\mathrm{V}_{\mathrm{IK}}\) & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \multicolumn{2}{|l|}{\(\mathrm{I}=-18 \mathrm{~mA}\)} & & & -1.5 & & & -1.5 & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \(\mathrm{V}_{\mathrm{IL}}=\mathrm{MAX}\), & \(\mathrm{IOH}=-0.4 \mathrm{~mA}\) & 2.5 & 3.4 & & 2.7 & 3.4 & & V \\
\hline \multirow[b]{2}{*}{VOL} & \multirow[b]{2}{*}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\),} & \multirow[b]{2}{*}{\(\mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}\)} & \(\mathrm{IOL}=4 \mathrm{~mA}\) & & 0.25 & 0.4 & & & 0.4 & \multirow[t]{2}{*}{V} \\
\hline & & & \(\mathrm{IOL}=8 \mathrm{~mA}\) & & & & & 0.25 & 0.5 & \\
\hline 1 & \(V_{C C}=\) MAX, & \multicolumn{2}{|l|}{\(\mathrm{V}_{1}=7 \mathrm{~V}\)} & & & 0.1 & & & 0.1 & mA \\
\hline IIH & \(V_{C C}=M A X\), & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\)} & & & 20 & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & \(V_{C C}=M A X\), & \multicolumn{2}{|l|}{\(\mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.4 & & & -0.4 & mA \\
\hline IOS§ & \multicolumn{3}{|l|}{\(V_{C C}=\) MAX} & -20 & & -100 & -20 & & -100 & mA \\
\hline ICCH & \(V_{C C}=\mathrm{MAX}\), & \multicolumn{2}{|l|}{\(\mathrm{V}_{1}=0 \mathrm{~V}\)} & & 1.2 & 2.4 & & 1.2 & 2.4 & mA \\
\hline ICCL & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\), & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{I}}=4.5 \mathrm{~V}\)} & & 3.6 & 6.6 & & 3.6 & 6.6 & mA \\
\hline
\end{tabular}
\(\dagger\) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
\(\ddagger\) All typical values are at \(\mathrm{V}_{\mathrm{C}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
switching characteristics, \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathbf{2 5}^{\circ} \mathrm{C}\) (see Figure 2)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{PARAMETER} & \multirow[t]{2}{*}{FROM (INPUT)} & \multirow[t]{2}{*}{\[
\begin{gathered}
\text { TO } \\
\text { (OUTPUT) }
\end{gathered}
\]} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{TEST CONDITIONS}} & \multicolumn{3}{|c|}{\[
\begin{aligned}
& \hline \text { SN54LS04 } \\
& \text { SN74LS04 }
\end{aligned}
\]} & \multirow[t]{2}{*}{UNIT} \\
\hline & & & & & MIN & TYP & MAX & \\
\hline tPLH & \multirow[t]{2}{*}{A} & \multirow[t]{2}{*}{Y} & \multirow[t]{2}{*}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\),} & \multirow[t]{2}{*}{\(C_{L}=15 \mathrm{pF}\)} & & 9 & 15 & \multirow[t]{2}{*}{ns} \\
\hline tPHL & & & & & & 10 & 15 & \\
\hline
\end{tabular}
recommended operating conditions
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{}} & \multicolumn{3}{|c|}{SN54S04} & \multicolumn{3}{|c|}{SN74S04} & \multirow[b]{2}{*}{UNIT} \\
\hline & & MIN & NOM & MAX & MIN & NOM & MAX & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High-level input voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low-level input voltage & & & 0.8 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{2}\) & High-level output current & & & -1 & & & -1 & mA \\
\hline IOL & Low-level output current & & & 20 & & & 20 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Operating free-air temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{PARAMETER} & \multicolumn{3}{|c|}{\multirow[b]{2}{*}{TEST CONDITIONS \(\dagger\)}} & \multicolumn{3}{|c|}{SN54S04} & \multicolumn{3}{|c|}{SN74S04} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & & MIN & TYP\# & MAX & MIN & TYP¥ & MAX & \\
\hline VIK & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \multicolumn{2}{|l|}{\(\mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & \multicolumn{3}{|r|}{-1.2} & \multicolumn{3}{|r|}{-1.2} & V \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}\), & \(\mathrm{IOH}=-1 \mathrm{~mA}\) & 2.5 & \multicolumn{2}{|l|}{3.4} & 2.7 & \multicolumn{2}{|l|}{3.4} & V \\
\hline V OL & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}\), & \(\mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V}\), & \(\mathrm{IOL}=20 \mathrm{~mA}\) & \multicolumn{3}{|r|}{0.5} & \multicolumn{3}{|r|}{0.5} & V \\
\hline 1 & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\), & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}\)} & & & 1 & & & 1 & mA \\
\hline 1 IH & \(V_{C C}=\) MAX, & \multicolumn{2}{|l|}{\(\mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 50 & & & 50 & \(\mu \mathrm{A}\) \\
\hline ILL & \(V_{C C}=\) MAX, & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}\)} & & & -2 & & & -2 & mA \\
\hline Ios§ & \multicolumn{3}{|l|}{\(V_{C C}=\) MAX} & -40 & & -100 & -40 & & -100 & mA \\
\hline ICCH & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\), & \multicolumn{2}{|l|}{\(\mathrm{V}_{1}=0 \mathrm{~V}\)} & & 15 & 24 & & 15 & 24 & mA \\
\hline ICCL & \(\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}\), & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {I }}=4.5 \mathrm{~V}\)} & & 30 & 54 & & 30 & 54 & mA \\
\hline
\end{tabular}
\(\dagger\) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
\(\ddagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
switching characteristics, \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (see Figure 1)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{PARAMETER} & \multirow[t]{2}{*}{FROM (INPUT)} & \multirow[t]{2}{*}{TO (OUTPUT)} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{TEST CONDITIONS}} & \multicolumn{3}{|c|}{\[
\begin{aligned}
& \hline \text { SN54S04 } \\
& \text { SN74S04 }
\end{aligned}
\]} & \multirow[t]{2}{*}{UNIT} \\
\hline & & & & & MIN & TYP & MAX & \\
\hline tPLH & \multirow[t]{2}{*}{A} & \multirow[t]{2}{*}{Y} & \multirow[b]{2}{*}{\(R_{L}=280 \Omega\),} & \multirow[b]{2}{*}{\(C_{L}=15 \mathrm{pF}\)} & & 3 & 4.5 & \multirow[b]{2}{*}{ns} \\
\hline tPHL & & & & & & 3 & 5 & \\
\hline tPLH & \multirow[t]{2}{*}{A} & \multirow[t]{2}{*}{Y} & \multirow[t]{2}{*}{\(R_{L}=280 \Omega\),} & \multirow[t]{2}{*}{\(C_{L}=50 \mathrm{pF}\)} & & 4.5 & & \multirow[t]{2}{*}{ns} \\
\hline tPHL & & & & & & 5 & & \\
\hline
\end{tabular}

\section*{PARAMETER MEASUREMENT INFORMATION SERIES 54/74 AND 54S/74S DEVICES}




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tpZL.
E. All input pulses are supplied by generators having the following characteristics: \(\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{O}} \approx 50 \Omega\); \(\mathrm{t}_{\mathrm{r}}\) and \(\mathrm{t}_{\mathrm{f}} \leq 7 \mathrm{~ns}\) for Series \(54 / 74\) devices and \(\mathrm{t}_{\mathrm{r}}\) and \(\mathrm{t}_{\mathrm{f}} \leq 2.5 \mathrm{~ns}\) for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

\section*{PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES}



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. \(C_{L}\) includes probe and jig capacitance.
B. All diodes are 1 N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tPZL.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: \(\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{O}} \approx 50 \Omega, \mathrm{t}_{\mathrm{r}} \leq 1.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}} \leq 2.6 \mathrm{~ns}\).
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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\author{
Mailing Address: \\ Texas Instruments \\ Post Office Box 655303 \\ Dallas, Texas 75265
}

\section*{- PIN ARRANGEMENT}


\section*{ABSOLUTE MAXIMUM RATINGS}
\begin{tabular}{l|l|c|c}
\hline \multicolumn{1}{c|}{ Item } & Symbol & Ratings & Unit \\
\hline \multicolumn{1}{c|}{ Supply voltage } & \(V C C\) & 7.0 & V \\
\hline Input voltage & VIN & 7.0 & V \\
\hline Output voltage & Vout & 30 & V \\
\hline Operating temperature range & Topr & \(-20 \sim+75\) & \({ }^{\circ} \mathrm{C}\) \\
\hline Storage temperature range & Tstg & \(-65 \sim+150\) & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{- RECOMMENDED OPERATING CONDITIONS}
\begin{tabular}{l|l|c|c|c:c}
\hline \multicolumn{1}{c|}{ Item } & Symbol & \(\min\) & typ & \(\max\) & Unit \\
\hline Supply voltage & \(V C C\) & 4.75 & 5.00 & 5.25 & V \\
\hline High level output voltage & \(V O H\) & - & - & 30 & V \\
\hline Low level output current & \(I O L\) & - & - & 48 & mA \\
\hline Operating temperature range & Topr & -20 & 25 & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

ELECTRICAL CHARACTERISTICS (Ta \(=-20 \sim+75^{\circ} \mathrm{C}\) )
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline Item & Symbol & \multicolumn{3}{|c|}{Test Conditions} & min & typ* & max & Unit \\
\hline \multirow[t]{2}{*}{Input voltage} & VIH & & & & 2.0 & - & - & V \\
\hline & VIL & & & & - & - & 0.8 & V \\
\hline \multirow[b]{2}{*}{Output voltage} & \multirow[b]{2}{*}{VoL} & \multirow[b]{2}{*}{\(V C C=4.75 \mathrm{~V}\),} & \multirow[b]{2}{*}{\(V / H=2 \mathrm{~V}\)} & \(1 O L=24 \mathrm{~mA}\) & - & - & 0.4 & V \\
\hline & & & & \(I O L=48 \mathrm{~mA}\) & - & - & 0.5 & V \\
\hline \multirow{3}{*}{Input current} & \(\overline{I H}\) & \(V C C=5.25 \mathrm{~V}\) & \multicolumn{2}{|l|}{\(V I=2.7 \mathrm{~V}\)} & - & - & 20 & \(\mu \mathrm{A}\) \\
\hline & ILL & \(V C C=5.25 \mathrm{~V}\), & \multicolumn{2}{|l|}{\(V=0.4 \mathrm{~V}\)} & - & - & -0.4 & mA \\
\hline & II & \(V C C=5.25 \mathrm{~V}\), & \multicolumn{2}{|l|}{\(V I=7 \mathrm{~V}\)} & - & - & 0.1 & mA \\
\hline Output current & IOH & \(V C C=4.75 \mathrm{~V}\), & \(V / L=0.8 \mathrm{~V}\), & \(\mathrm{VOH}=30 \mathrm{~V}\) & - & - & 250 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{Supply current} & ICCH & \(V C C=5.25 \mathrm{~V}\) & & & - & 23 & 48 & mA \\
\hline & ICCL & \(V C C=5.25 \mathrm{~V}\) & & & - & 21 & 51 & mA \\
\hline Input clamp voltage & \(V I K\) & \[
V C C=4.75 \mathrm{~V}
\] & \multicolumn{2}{|l|}{IIN \(=-18 \mathrm{~mA}\)} & - & - & -1.5 & V \\
\hline
\end{tabular}
*VCC \(=5 \mathrm{~V}, T a=25^{\circ} \mathrm{C}\)

SWITCHING CHARACTERISTICS (VCC \(=5 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}\) )
\begin{tabular}{c|c|c|c|c|c|c}
\hline Item & Symbol & Test Conditions & min & typ & max & Unit \\
\hline \multirow{2}{*}{ Propagation delay time } & \(t_{P L H}\) & \multirow{2}{*}{\(C_{L=15 \mathrm{pF}, R L=110 \Omega}\)} & \(t_{P H L}\) & & - & 10 \\
\cline { 2 - 6 } & & & - & 15 & 23 & ns \\
\hline
\end{tabular}

\section*{■ TESTING METHOD}

Test Circuit


Waveform


Notes) 1. Input puise: \(P R R=1 \mathrm{MHz}\), duty cycle \(50 \%\), Zout \(=50 \Omega\), ttLH \(\leq 15 \mathrm{~ns}\). tTHL \(\leq 6 \mathrm{~ns}\)
2. CL includes probe and jig capacitance.
3. All diodes are \(1 \mathrm{~S} 2074(\mathrm{H})\)

\begin{tabular}{|l|l|}
\hline Hitachi Code & DP-14 \\
\hline JEDEC & Conforms \\
\hline EIAJ & Conforms \\
\hline Weight (reference value) & 0.97 g \\
\hline
\end{tabular}

\begin{tabular}{|l|l|}
\hline Hitachi Code & FP-14DA \\
\hline JEDEC & - \\
\hline EIAJ & Conforms \\
\hline Weight (reference value) & 0.23 g \\
\hline
\end{tabular}

\begin{tabular}{|l|l|}
\hline Hitachi Code & FP-14DN \\
\hline JEDEC & Conforms \\
\hline EIAJ & Conforms \\
\hline Weight (reference value) & 0.13 g \\
\hline
\end{tabular}

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\section*{HITACHI}

\section*{Hitachi, Ltd.}

Semiconductor \& Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109
URL NorthAmerica : http:semiconductor.hitachi.com/

Asia (Singapore)
Asia (Taiwan)
Asia (HongKong) Japan
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\section*{For further information write to:}

Hitachi Semiconductor
America) Inc.
179 East Tasman Drive, San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group Dornacher Stra§e 3
D-85622 Feldkirchen, Munich Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9293000
Hitachi Europe Ltd Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd. 16 Collyer Quay \#20-00 Hitachi Tower Singapore 049318
Tel: 535-2100
Fax: 535-1533
Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

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\begin{tabular}{l} 
Absolute Maximum Ratings (Note) \\
If Military/Aerospace specified devices are required, \\
please contact the National Semiconductor Sales \\
Office/Distributors for availability and specifications. \\
Supply Voltage \\
Input Voltage \\
Operating Free Air Temperature Range \\
DM54LS and 54 LS \\
DM74LS \\
Storage Temperature Range \\
Te \\
\hline
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS08} & \multicolumn{3}{|c|}{DM74LS08} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\text {l }}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline IOL & Low Level Output Current & & & 4 & & & 8 & mA \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \[
\begin{gathered}
\text { Typ } \\
\text { (Note 1) }
\end{gathered}
\] & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & DM54 & 2.5 & 3.4 & & V \\
\hline & & & DM74 & 2.7 & 3.4 & & \\
\hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\mathrm{Max}, \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
\hline & & & DM74 & & 0.35 & 0.5 & \\
\hline & & \(\mathrm{IOL}=4 \mathrm{~mA}\), & DM74 & & 0.25 & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\text {IL }}\) & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=0.4 \mathrm{~V}\)} & & & -0.36 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& (\text { Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -20 & & -100 & \\
\hline ICCH & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 2.4 & 4.8 & mA \\
\hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 4.4 & 8.8 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 4 & 13 & 6 & 18 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 3 & 11 & 5 & 18 & ns \\
\hline \multicolumn{7}{|l|}{Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).} \\
\hline
\end{tabular}



Physical Dimensions inches (millimeters) (Continued)

14-Lead Ceramic Flat Package (W) Order Number 54LS08FMQB or DM54LS08W NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
\begin{tabular}{|c|c|c|c|}
\hline \begin{tabular}{l}
National Semiconductor Corporation \\
1111 West Bardin Road Arlington, TX 76017 \\
Tel: 1(800) 272-9959 \\
Fax: 1(800) 737-7018
\end{tabular} & \begin{tabular}{l}
National Semiconductor \\
Europe \\
Fax: (+49) 0-180-530 8586 \\
Email: cnjwge@tevm2.nsc.com \\
Deutsch Tel: \((+49)\) 0-180-530 8585 \\
English Tel: \((+49)\) 0-180-532 7832 \\
Français Tel: \((+49)\) 0-180-532 9358 \\
Italiano Tel: (+49) 0-180-534 1680
\end{tabular} & \begin{tabular}{l}
National Semiconductor Hong Kong Ltd. \\
13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong \\
Tel: (852) 2737-1600 \\
Fax: (852) 2736-9960
\end{tabular} & \begin{tabular}{l}
National Semiconductor Japan Ltd. \\
Tel: 81-043-299-2309 \\
Fax: 81-043-299-2408
\end{tabular} \\
\hline
\end{tabular}


Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 7 V \\
Operating Free Air Temperature Range & \\
DM54LS and 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS32} & \multicolumn{3}{|c|}{DM74LS32} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\prime}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{IOL}^{\text {l }}\) & Low Level Output Current & & & 4 & & & 8 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|l|}{Conditions} & Min & Typ (Note 1) & Max & Units \\
\hline \(\mathrm{V}_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OH}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IH}}=\mathrm{Min}
\end{aligned}
\]} & DM54 & 2.5 & 3.4 & & \multirow[t]{2}{*}{V} \\
\hline & & & DM74 & 2.7 & 3.4 & & \\
\hline \multirow[t]{3}{*}{\(\mathrm{V}_{\mathrm{OL}}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{IOL}_{\mathrm{OL}}=\mathrm{Max} \\
& \mathrm{~V}_{\mathrm{IL}}=\mathrm{Max}
\end{aligned}
\]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
\hline & & & DM74 & & 0.35 & 0.5 & \\
\hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{Min}\) & DM74 & & 0.25 & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
\hline \(\mathrm{IIH}^{\text {H }}\) & High Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{1}=0.4 \mathrm{~V}\)} & & & -0.36 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Max} \\
& \text { (Note 2) }
\end{aligned}
\]} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -20 & & -100 & \\
\hline \({ }^{\text {ICCH }}\) & Supply Current with Outputs High & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 3.1 & 6.2 & mA \\
\hline \(\mathrm{I}_{\text {CCL }}\) & Supply Current with Outputs Low & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\)} & & 4.9 & 9.8 & mA \\
\hline
\end{tabular}

Switching Characteristics at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (See Section 1 for Test Waveforms and Output Load)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multicolumn{4}{|c|}{\(\mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega\)} & \multirow{3}{*}{Units} \\
\hline & & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}\)} & \multicolumn{2}{|c|}{\(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}\)} & \\
\hline & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & 3 & 11 & 4 & 15 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & 3 & 11 & 4 & 15 & ns \\
\hline \multicolumn{7}{|l|}{\begin{tabular}{l}
Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\). \\
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
\end{tabular}} \\
\hline
\end{tabular}



54LS32/DM54LS32/DM74LS32 Quad 2-Input OR Gates
Physical Dimensions inches (millimeters) (Continued)

14-Lead Ceramic Flat Package (W) Order Number 54LS32FMQB or DM54LS32W NS Package Number W14B

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If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
\begin{tabular}{lr} 
Supply Voltage & 7 V \\
Input Voltage & 7 V \\
Operating Free Air Temperature Range & \\
DM54LS and 54LS & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
DM74LS & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\end{tabular}

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multirow{2}{*}{Parameter} & \multicolumn{3}{|c|}{DM54LS279} & \multicolumn{3}{|c|}{DM74LS279} & \multirow{2}{*}{Units} \\
\hline & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & Supply Voltage & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\text {IH }}\) & High Level Input Voltage & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & Low Level Input Voltage & & & 0.7 & & & 0.8 & V \\
\hline \(\mathrm{IOH}^{\prime}\) & High Level Output Current & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{IOL}^{\text {l }}\) & Low Level Output Current & & & 4 & & & 8 & mA \\
\hline \(\mathrm{T}_{\text {A }}\) & Free Air Operating Temperature & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Symbol & Parameter & \multicolumn{2}{|c|}{Conditions} & Min & \begin{tabular}{l}
Typ \\
(Note 1)
\end{tabular} & Max & Units \\
\hline \(V_{1}\) & Input Clamp Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{l}_{\mathrm{I}}=-18 \mathrm{~mA}\)} & & & -1.5 & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow[t]{2}{*}{High Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\operatorname{Min}, \mathrm{I}_{\mathrm{OH}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\operatorname{Max}, \mathrm{V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & DM54 & 2.5 & 3.5 & & V \\
\hline & & & DM74 & 2.7 & 3.5 & & \\
\hline \multirow[t]{3}{*}{\(\mathrm{V}_{\text {OL }}\)} & \multirow[t]{3}{*}{Low Level Output Voltage} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=\mathrm{Min}, \mathrm{I}_{\mathrm{OL}}=\operatorname{Max} \\
& \mathrm{V}_{\mathrm{IL}}=\mathrm{Max}, \mathrm{~V}_{\mathrm{IH}}=\operatorname{Min}
\end{aligned}
\]} & DM54 & & 0.25 & 0.4 & \multirow{3}{*}{V} \\
\hline & & & DM74 & & 0.35 & 0.5 & \\
\hline & & \(\mathrm{l}_{\mathrm{OL}}=4 \mathrm{~mA}\), & DM74 & & 0.25 & 0.4 & \\
\hline 1 & Input Current @ Max Input Voltage & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}\)} & & & 0.1 & mA \\
\hline IIH & High Level Input Current & \multicolumn{2}{|l|}{\(V_{C C}=\operatorname{Max}, \mathrm{V}_{\mathrm{l}}=2.7 \mathrm{~V}\)} & & & 20 & \(\mu \mathrm{A}\) \\
\hline IIL & Low Level Input Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}, \mathrm{V}_{\mathrm{l}}=0.4 \mathrm{~V}\)} & & & -0.4 & mA \\
\hline \multirow[t]{2}{*}{los} & \multirow[t]{2}{*}{Short Circuit Output Current} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}
\] \\
(Note 2)
\end{tabular}} & DM54 & -20 & & -100 & \multirow[t]{2}{*}{mA} \\
\hline & & & DM74 & -20 & & -100 & \\
\hline ICC & Supply Current & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{CC}}=\mathrm{Max}\) (Note 3)} & & 3.8 & 7 & mA \\
\hline
\end{tabular}

Note 1: All typicals are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
Note 3: ICC is measured with all \(\overline{\mathrm{R}}\) inputs grounded, all \(\overline{\mathrm{S}}\) inputs at 4.5 V and all outputs open.
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{3}{*}{Symbol} & \multirow{3}{*}{Parameter} & \multirow{3}{*}{\begin{tabular}{l}
From (Input) \\
To (Output)
\end{tabular}} & \multicolumn{4}{|c|}{\(\mathbf{R}_{\mathrm{L}}=\mathbf{2 k} \mathbf{~}\),} & \multirow{3}{*}{Units} \\
\hline & & & & & & & \\
\hline & & & Min & Max & Min & Max & \\
\hline \(t_{\text {PLH }}\) & Propagation Delay Time Low to High Level Output & \[
\begin{gathered}
\overline{\mathrm{S}} \text { to } \\
\mathrm{Q}
\end{gathered}
\] & & 22 & & 25 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(\overline{\mathrm{S}}\) to Q & & 15 & & 23 & ns \\
\hline \(t_{\text {PHL }}\) & Propagation Delay Time High to Low Level Output & \(\overline{\mathrm{R}}\) to Q & & 27 & & 33 & ns \\
\hline
\end{tabular}


Physical Dimensions inches (millimeters) (Continued)


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\hline
\end{tabular}

\section*{Features}
- Compatible with MCS \({ }^{\oplus}-51\) Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
- Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5 V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

\section*{Description}

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the indus-try-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.
The AT89S51 provides the following standard features: 4 K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a fivevector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

\section*{Pin Configurations}
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{4}{|c|}{PDIP} \\
\hline & & & \\
\hline P1.0 & 1 & 40 & \(\square \mathrm{VCC}\) \\
\hline P1.1 & 2 & 39 & \(\square \mathrm{P} 0.0\) (ADO) \\
\hline P1.2 & 3 & 38 & \(\square \mathrm{P} 0.1\) (AD1) \\
\hline P1.3 & 4 & 37 & \(\square \mathrm{P} 0.2\) (AD2) \\
\hline P1.4 & 5 & 36 & \(\square \mathrm{P} 0.3\) (AD3) \\
\hline (MOSI) P1.5 \(\square\) & 6 & 35 & \(\square \mathrm{P} 0.4\) (AD4) \\
\hline (MISO) P1.6 & 7 & 34 & \(\square \mathrm{P} 0.5\) (AD5) \\
\hline (SCK) P1.7 \(\square\) & 8 & 33 & \(\square \mathrm{P} 0.6\) (AD6) \\
\hline RST \(\square\) & 9 & 32 & \(\square \mathrm{P} 0.7\) (AD7) \\
\hline (RXD) P3.0 \(\square\) & 10 & 31 & \(\square \overline{\mathrm{EA}} / \mathrm{VPP}\) \\
\hline (TXD) P3.1 \(\square\) & 11 & 30 & \(\square \mathrm{ALE} / \overline{\mathrm{PROG}}\) \\
\hline (INT0) P3.2 \(\square\) & 12 & 29 & \(\square \overline{\text { PSEN }}\) \\
\hline (INT1) P3.3 & 13 & 28 & \(\square \mathrm{P} 2.7\) (A15) \\
\hline (T0) P3.4 \(\square\) & 14 & 27 & \(\square \mathrm{P} 2.6\) (A14) \\
\hline (T1) P3.5 & 15 & 26 & \(\square \mathrm{P} 2.5\) (A13) \\
\hline ( \(\overline{\mathrm{WR}})\) P3.6 & 16 & 25 & \(\square \mathrm{P} 2.4\) (A12) \\
\hline ( \(\overline{\mathrm{RD}}) \mathrm{P} 3.7 \square\) & 17 & 24 & \(\square \mathrm{P} 2.3\) (A11) \\
\hline XTAL2 & 18 & 23 & \(\square \mathrm{P} 2.2\) (A10) \\
\hline XTAL1 & 19 & 22 & \(\square \mathrm{P} 2.1\) (A9) \\
\hline GND & 20 & 21 & \(\square \mathrm{P} 2.0\) (A8) \\
\hline
\end{tabular}


\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{4}{|c|}{PDIP} \\
\hline & & & \\
\hline RST - & 1 & 42 & \(\square \mathrm{P} 1.7\) (SCK) \\
\hline (RXD) P3.0 & 2 & 41 & \(\square \mathrm{P} 1.6\) (MISO) \\
\hline (TXD) P3.1 & 3 & 40 & \(\square \mathrm{P} 1.5\) (MOSI) \\
\hline (INTO) P3.2 & 4 & 39 & P1.4 \\
\hline (INT1) P3.3 & 5 & 38 & P1.3 \\
\hline (T0) P3.4 & 6 & 37 & \(\square \mathrm{P} 1.2\) \\
\hline (T1) P3.5 & 7 & 36 & \(\square \mathrm{P} 1.1\) \\
\hline ( \(\overline{\mathrm{WR}}) \mathrm{P} 3.6\) & 8 & 35 & P1.0 \\
\hline ( \(\overline{\mathrm{RD}}) \mathrm{P} 3.7\) & 9 & 34 & \(\checkmark\) VDD \\
\hline XTAL2 & 10 & 33 & \(\square\) PWRVDD \\
\hline XTAL1 & 11 & 32 & \(\square \mathrm{P} 0.0\) (ADO) \\
\hline GND & 12 & 31 & \(\square \mathrm{P} 0.1\) (AD1) \\
\hline PWRGND & 13 & 30 & \(\square \mathrm{P} 0.2\) (AD2) \\
\hline (A8) P2.0 & 14 & 29 & P0.3 (AD3) \\
\hline (A9) P2.1 & 15 & 28 & \(\square \mathrm{P} 0.4\) (AD4) \\
\hline (A10) P2.2 & 16 & 27 & P0.5 (AD5) \\
\hline (A11) P2.3 & 17 & 26 & P0.6 (AD6) \\
\hline (A12) P2.4 & 18 & 25 & P0.7 (AD7) \\
\hline (A13) P2.5 & 19 & 24 & \(\square \overline{E A} / \mathrm{VPP}\) \\
\hline (A14) P2.6 & 20 & 23 & \(\square \mathrm{ALE} / \overline{\mathrm{PROG}}\) \\
\hline (A15) P2.7 & 21 & 22 & PSEN \\
\hline
\end{tabular}

\section*{Block Diagram}


\section*{Pin Description}

VCC

GND

Supply voltage (all packages except 42-PDIP).

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board MUST connect both VDD and PWRVDD to the board supply voltage.

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board MUST connect both GND and PWRGND to the board ground.

Port 0 is an 8 -bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1 s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 is an 8 -bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1 s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ( \(I_{L}\) ) because of the internal pull-ups.
Port 1 also receives the low-order address bytes during Flash programming and verification.
\begin{tabular}{|l|l|}
\hline Port Pin & Alternate Functions \\
\hline P1.5 & MOSI (used for In-System Programming) \\
\hline P1.6 & MISO (used for In-System Programming) \\
\hline P1.7 & SCK (used for In-System Programming) \\
\hline
\end{tabular}

Port 2 is an 8 -bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1 s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current \(\left(l_{L}\right)\) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

\section*{Port 3}

\section*{ALE/PROG}

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
External Access Enable. \(\overline{\mathrm{EA}}\) must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000 H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.
\(\overline{E A}\) should be strapped to \(\mathrm{V}_{\mathrm{CC}}\) for internal program executions.
This pin also receives the 12 -volt programming enable voltage ( \(\mathrm{V}_{\mathrm{PP}}\) ) during Flash programming.

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline 0F8H & & & & & & & & & 0FFH \\
\hline 0FOH & \[
\begin{gathered}
\text { B } \\
00000000
\end{gathered}
\] & & & & & & & & 0F7H \\
\hline 0E8H & & & & & & & & & 0EFH \\
\hline OEOH & \[
\begin{gathered}
\text { ACC } \\
00000000
\end{gathered}
\] & & & & & & & & 0E7H \\
\hline 0D8H & & & & & & & & & ODFH \\
\hline 0DOH & \[
\begin{gathered}
\text { PSW } \\
00000000
\end{gathered}
\] & & & & & & & & 0D7H \\
\hline 0 C 8 H & & & & & & & & & OCFH \\
\hline OCOH & & & & & & & & & 0C7H \\
\hline 0B8H & \[
\begin{gathered}
\text { IP } \\
\times \times 000000
\end{gathered}
\] & & & & & & & & OBFH \\
\hline 0B0H & \[
\begin{gathered}
\text { P3 } \\
11111111
\end{gathered}
\] & & & & & & & & 0B7H \\
\hline 0A8H & \[
\begin{gathered}
\text { IE } \\
0 \times 000000
\end{gathered}
\] & & & & & & & & OAFH \\
\hline OAOH & \[
\begin{gathered}
\text { P2 } \\
11111111
\end{gathered}
\] & & \[
\begin{gathered}
\text { AUXR1 } \\
\text { XXXXXX0 }
\end{gathered}
\] & & & & WDTRST XXXXXXXX & & 0A7H \\
\hline 98H & \[
\begin{gathered}
\text { SCON } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { SBUF } \\
\text { XXXXXXXX }
\end{gathered}
\] & & & & & & & 9FH \\
\hline 90H & \[
\begin{gathered}
\text { P1 } \\
11111111
\end{gathered}
\] & & & & & & & & 97H \\
\hline 88H & \[
\begin{gathered}
\text { TCON } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { TMOD } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { TLO } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { TL1 } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { TH0 } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { TH1 } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { AUXR } \\
\text { XXX00XX0 }
\end{gathered}
\] & & 8FH \\
\hline 80H & \[
\begin{gathered}
\text { P0 } \\
11111111
\end{gathered}
\] & \[
\begin{gathered}
\text { SP } \\
00000111
\end{gathered}
\] & \[
\begin{gathered}
\text { DPOL } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { DPOH } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { DP1L } \\
00000000
\end{gathered}
\] & \[
\begin{gathered}
\text { DP1H } \\
00000000
\end{gathered}
\] & & \[
\begin{gathered}
\text { PCON } \\
0 X X X 0000
\end{gathered}
\] & 87H \\
\hline
\end{tabular}

User software should not write 1 s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0 .

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register


Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16 -bit Data Pointer Registers are provided: DP0 at SFR address locations \(82 \mathrm{H}-\) 83 H and DP1 at \(84 \mathrm{H}-85 \mathrm{H}\). Bit DPS \(=0\) in SFR AUXR1 selects DP0 and DPS \(=1\) selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to " 1 " during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1


\section*{Memory Organization}

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64 K bytes each of external Program and Data Memory can be addressed.

If the \(\overline{E A}\) pin is connected to GND, all program fetches are directed to external memory.
On the AT89S51, if \(\overline{E A}\) is connected to \(\mathrm{V}_{\mathrm{CC}}\), program fetches to addresses 0000 H through FFFH are directed to internal memory and fetches to addresses 1000 H through FFFFH are directed to external memory.

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location OA6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location OA6H). When the WDT is enabled, the user needs to service it by writing 01EH and OE1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is \(98 \times\) TOSC, where TOSC \(=1 /\) FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

\author{
WDT During Power-down and Idle
}

\section*{UART}

\section*{Timer 0 and 1}

\section*{Interrupts}

In Power-down mode the oscillator stops, which means the WDT also stops. While in Powerdown mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0 ) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.
With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe \({ }^{\circledR}\) Acrobat \({ }^{\circledR}\) file "AT89 Series Hardware Description".

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe Acrobat file "AT89 Series Hardware Description".

The AT89S51 has a total of five interrupt vectors: two external interrupts (INT0 and INT1), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.
Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.
Note that Table 4 shows that bit positions IE. 6 and IE. 5 are unimplemented. User software should not write 1 s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 4. Interrupt Enable (IE) Register
(MSB)
\begin{tabular}{|l|l|l|l|l|l|l|l|}
\hline EA & - & - & ES & ET1 & EX1 & ET0 & EX0 \\
\hline
\end{tabular}

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables the interrupt.
\begin{tabular}{|l|l|l|}
\hline Symbol & Position & Function \\
\hline EA & IE. 7 & \begin{tabular}{l} 
Disables all interrupts. If EA \(=0\), no interrupt is \\
acknowledged. If EA \(=1\), each interrupt source is \\
individually enabled or disabled by setting or clearing \\
its enable bit.
\end{tabular} \\
\hline- & IE.6 & Reserved \\
\hline- & IE. 5 & Reserved \\
\hline ES & IE.4 & Serial Port interrupt enable bit \\
\hline ET1 & IE.3 & Timer 1 interrupt enable bit \\
\hline EX1 & IE. 2 & External interrupt 1 enable bit \\
\hline ET0 & IE.0 & Timer 0 interrupt enable bit \\
\hline EX0 & External interrupt 0 enable bit \\
\hline \begin{tabular}{l} 
User software should never write 1s to reserved bits, because they may be used in future AT89 \\
products.
\end{tabular} & \\
\hline
\end{tabular}

Figure 1. Interrupt Sources

\(\mathrm{TFO} \longrightarrow\)


TF1 \(\longrightarrow\)


\section*{Oscillator Characteristics}

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections


Note: \(\quad \mathrm{C} 1, \mathrm{C} 2=30 \mathrm{pF} \pm 10 \mathrm{pF}\) for Crystals
\(=40 \mathrm{pF} \pm 10 \mathrm{pF}\) for Ceramic Resonators
Figure 3. External Clock Drive Configuration


In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.
Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Powerdown is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt (INTO or INT1). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before \(\mathrm{V}_{\mathrm{CC}}\) is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize. morn

\section*{Power-down Mode}

\section*{Idle Mode}

Table 5. Status of External Pins During Idle and Power-down Modes
\begin{tabular}{|l|l|c|c|c|c|c|c|}
\hline Mode & Program Memory & ALE & \(\overline{\text { PSEN }}\) & PORT0 & PORT1 & PORT2 & PORT3 \\
\hline Idle & Internal & 1 & 1 & Data & Data & Data & Data \\
\hline Idle & External & 1 & 1 & Float & Data & Address & Data \\
\hline Power-down & Internal & 0 & 0 & Data & Data & Data & Data \\
\hline Power-down & External & 0 & 0 & Float & Data & Data & Data \\
\hline
\end{tabular}

\section*{Program Memory Lock Bits}

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed \((P)\) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{Program Lock Bits} & \multirow[b]{2}{*}{Protection Type} \\
\hline & LB1 & LB2 & LB3 & \\
\hline 1 & U & U & U & No program lock features \\
\hline 2 & P & U & U & MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, \(\overline{\mathrm{EA}}\) is sampled and latched on reset, and further programming of the Flash memory is disabled \\
\hline 3 & P & P & U & Same as mode 2, but verify is also disabled \\
\hline 4 & P & P & P & Same as mode 3, but external execution is also disabled \\
\hline
\end{tabular}

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of EA must agree with the current logic level at that pin in order for the device to function properly.

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.
Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 7) and Figures 4 and 5 . To program the AT89S51, take the following steps:
1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise \(\overline{E A} / V_{P P}\) to 12 V .
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The bytewrite cycle is self-timed and typically takes no more than \(50 \mu \mathrm{~s}\). Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.
 During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. \(\overline{\text { Data }}\) Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/ \(\overline{\operatorname{BSY}}\) output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations \(000 \mathrm{H}, 100 \mathrm{H}\), and 200 H , except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.
\((000 \mathrm{H})=1 \mathrm{EH}\) indicates manufactured by Atmel
\((100 \mathrm{H})=51 \mathrm{H}\) indicates AT89S51
\((200 \mathrm{H})=06 \mathrm{H}\)
Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/PROG low for a duration of 200 ns 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms .

During chip erase, a serial read from any address location will return 00 H at the data output.

> Programming the Flash Serial Mode

\section*{Serial \\ Programming Algorithm}

The Code memory array can be programmed using the serial ISP interface while RST is pulled to \(\mathrm{V}_{\mathrm{cc}}\). The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.
The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than \(1 / 16\) of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz .

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:
1. Power-up sequence:

Apply power between VCC and GND pins.
Set RST pin to " H ".
If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5 V .
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):
Set XTAL1 to "L" (if a crystal is not used).
Set RST to "L".
Turn \(\mathrm{V}_{\mathrm{Cc}}\) power off.
Data Polling: The \(\overline{\text { Data }}\) Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

\section*{Serial \\ Programming Instruction Set}

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8.

\section*{Programming Interface Parallel Mode}

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Mode} & \multirow[b]{2}{*}{\(\mathrm{V}_{\mathrm{cc}}\)} & \multirow[b]{2}{*}{RST} & \multirow[b]{2}{*}{PSEN} & \multirow[t]{2}{*}{\[
\frac{\text { ALE/ }}{\text { PROG }}
\]} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \overline{E A} / \\
& \mathrm{V}_{\mathrm{PP}}
\end{aligned}
\]} & \multirow[b]{2}{*}{P2.6} & \multirow[b]{2}{*}{P2.7} & \multirow[b]{2}{*}{P3.3} & \multirow[b]{2}{*}{P3.6} & \multirow[b]{2}{*}{P3.7} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \text { P0.7-0 } \\
& \text { Data }
\end{aligned}
\]} & P2.3-0 & P1.7-0 \\
\hline & & & & & & & & & & & & \multicolumn{2}{|c|}{Address} \\
\hline Write Code Data & 5 V & H & L & \[
\sim^{(2)}
\] & 12 V & L & H & H & H & H & \(\mathrm{D}_{\text {IN }}\) & A11-8 & A7-0 \\
\hline Read Code Data & 5V & H & L & H & H & L & L & L & H & H & \(\mathrm{D}_{\text {OUt }}\) & A11-8 & A7-0 \\
\hline Write Lock Bit 1 & 5 V & H & L & \[
\sim^{(3)}
\] & 12 V & H & H & H & H & H & X & X & X \\
\hline Write Lock Bit 2 & 5 V & H & L & \[
\sim^{(3)}
\] & 12 V & H & H & H & L & L & X & X & X \\
\hline Write Lock Bit 3 & 5 V & H & L & \[
\sim^{(3)}
\] & 12 V & H & L & H & H & L & X & X & X \\
\hline Read Lock Bits
\[
1,2,3
\] & 5 V & H & L & H & H & H & H & L & H & L & \[
\begin{aligned}
& \text { P0.2, } \\
& \text { P0.3, } \\
& \text { P0. }
\end{aligned}
\] & X & X \\
\hline Chip Erase & 5 V & H & L & \[
\sim{ }^{(1)}
\] & 12 V & H & L & H & L & L & X & X & X \\
\hline Read Atmel ID & 5 V & H & L & H & H & L & L & L & L & L & 1 EH & 0000 & 00H \\
\hline Read Device ID & 5 V & H & L & H & H & L & L & L & L & L & 51H & 0001 & OOH \\
\hline Read Device ID & 5 V & H & L & H & H & L & L & L & L & L & 06H & 0010 & OOH \\
\hline
\end{tabular}

Notes: 1. Each PROG pulse is \(200 \mathrm{~ns}-500 \mathrm{~ns}\) for Chip Erase.
2. Each \(\overline{\text { PROG }}\) pulse is \(200 \mathrm{~ns}-500 \mathrm{~ns}\) for Write Code Data.
3. Each PROG pulse is \(200 \mathrm{~ns}-500 \mathrm{~ns}\) for Write Lock Bits.
4. RDY/ \(\overline{\mathrm{BSY}}\) signal is output on P3.0 during programming.
5. \(\mathrm{X}=\) don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)


Figure 5. Verifying the Flash Memory (Parallel Mode)


Flash Programming and Verification Characteristics (Parallel Mode)
\(\mathrm{T}_{\mathrm{A}}=20^{\circ} \mathrm{C}\) to \(30^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=4.5\) to 5.5 V
\begin{tabular}{|c|c|c|c|c|}
\hline Symbol & Parameter & Min & Max & Units \\
\hline \(\mathrm{V}_{\text {PP }}\) & Programming Supply Voltage & 11.5 & 12.5 & V \\
\hline \(\mathrm{I}_{\mathrm{PP}}\) & Programming Supply Current & & 10 & mA \\
\hline \(\mathrm{I}_{\mathrm{CC}}\) & \(\mathrm{V}_{\mathrm{CC}}\) Supply Current & & 30 & mA \\
\hline 1/t \({ }_{\text {CLCL }}\) & Oscillator Frequency & 3 & 33 & MHz \\
\hline \(t_{\text {AVGL }}\) & Address Setup to \(\overline{\text { PROG Low }}\) & \(48 \mathrm{t}_{\text {CLCL }}\) & & \\
\hline \(\mathrm{t}_{\text {GHAX }}\) & Address Hold After PROG & \(48 \mathrm{t}_{\mathrm{CLCL}}\) & & \\
\hline \(\mathrm{t}_{\text {DVGL }}\) & Data Setup to \(\overline{\text { PROG }}\) Low & \(48 \mathrm{t}_{\text {CLCL }}\) & & \\
\hline \(\mathrm{t}_{\text {GHDX }}\) & Data Hold After \(\overline{\text { PROG }}\) & \(48 \mathrm{t}_{\text {CLCL }}\) & & \\
\hline \(\mathrm{t}_{\text {EHSH }}\) & P2.7 ( \(\overline{\text { ENABLE }}\) ) High to \(\mathrm{V}_{\mathrm{PP}}\) & \(48 \mathrm{t}_{\mathrm{CLCL}}\) & & \\
\hline \(\mathrm{t}_{\text {SHGL }}\) & \(\mathrm{V}_{\text {PP }}\) Setup to \(\overline{\text { PROG }}\) Low & 10 & & \(\mu \mathrm{s}\) \\
\hline \(\mathrm{t}_{\text {GHSL }}\) & \(V_{\text {PP }}\) Hold After \(\overline{\text { PROG }}\) & 10 & & \(\mu \mathrm{s}\) \\
\hline \(\mathrm{t}_{\text {GLGH }}\) & \(\overline{\text { PROG Width }}\) & 0.2 & 1 & \(\mu \mathrm{s}\) \\
\hline \(\mathrm{t}_{\text {AVQV }}\) & Address to Data Valid & & \(48 \mathrm{t}_{\text {CLCL }}\) & \\
\hline \(t_{\text {ELQV }}\) & ENABLE Low to Data Valid & & \(48 \mathrm{t}_{\text {CLCL }}\) & \\
\hline \(\mathrm{t}_{\text {EHQZ }}\) & Data Float After ENABLE & 0 & \(48 \mathrm{t}_{\text {CLCL }}\) & \\
\hline \(\mathrm{t}_{\text {GHBL }}\) & \(\overline{\text { PROG }}\) High to \(\overline{\text { BUSY }}\) Low & & 1.0 & \(\mu \mathrm{s}\) \\
\hline \(\mathrm{t}_{\text {wc }}\) & Byte Write Cycle Time & & 50 & \(\mu \mathrm{s}\) \\
\hline
\end{tabular}

Figure 6. Flash Programming and Verification Waveforms - Parallel Mode


Figure 7. Flash Memory Serial Downloading


\section*{Flash Programming and Verification Waveforms - Serial Mode}

Figure 8. Serial Programming Waveforms


Table 8. Serial Programming Instruction Set
\begin{tabular}{|l|l|l|l|l|l|}
\hline \multirow{3}{*}{ Instruction } & \begin{tabular}{l} 
Instruction \\
Format
\end{tabular} & & & & \\
\hline & Byte 1 & Byte 2 & Byte 3 & Byte 4 & Operation
\end{tabular}

Note: 1. B1 \(=0, \mathrm{~B} 2=0 \rightarrow\) Mode 1, no lock protection \(\mathrm{B} 1=0, \mathrm{~B} 2=1 \rightarrow\) Mode 2, lock bit 1 activated \(B 1=1, B 2=0 \rightarrow\) Mode 3, lock bit 2 activated \(B 1=1, B 2=1 \rightarrow\) Mode 4, lock bit 3 activated

Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than \(1 / 16\) of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255 . After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

\section*{Serial Programming Characteristics}

Figure 9. Serial Programming Timing


Table 9. Serial Programming Characteristics, \(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\) to \(85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=4.0-5.5 \mathrm{~V}\) (Unless Otherwise Noted)
\begin{tabular}{|l|l|c|c|c|c|}
\hline Symbol & Parameter & Min & Typ & Max & Units \\
\hline \(1 / t_{\text {CLCL }}\) & Oscillator Frequency & 3 & & 33 & MHz \\
\hline \(\mathrm{t}_{\mathrm{CLCL}}\) & Oscillator Period & 30 & & & ns \\
\hline \(\mathrm{t}_{\text {SHSL }}\) & SCK Pulse Width High & \(8 \mathrm{t}_{\mathrm{CLCL}}\) & & & ns \\
\hline \(\mathrm{t}_{\mathrm{SLSH}}\) & SCK Pulse Width Low & \(8 \mathrm{t}_{\mathrm{CLCL}}\) & & ns \\
\hline \(\mathrm{t}_{\mathrm{OVSH}}\) & MOSI Setup to SCK High & \(\mathrm{t}_{\mathrm{CLCL}}\) & & & ns \\
\hline \(\mathrm{t}_{\text {SHOX }}\) & MOSI Hold after SCK High & \(2 \mathrm{t}_{\mathrm{CLCL}}\) & & & ns \\
\hline \(\mathrm{t}_{\text {SLIV }}\) & SCK Low to MISO Valid & 10 & & 16 & 32 \\
\hline \(\mathrm{t}_{\text {ERASE }}\) & Chip Erase Instruction Cycle Time & & & 500 & ns \\
\hline \(\mathrm{t}_{\text {SWC }}\) & Serial Byte Write Cycle Time & & & \(64 \mathrm{t}_{\mathrm{CLCL}}+400\) & \(\mu \mathrm{~s}\) \\
\hline
\end{tabular}

\section*{Absolute Maximum Ratings*}
\begin{tabular}{|l|}
\hline Operating Temperature ............................... \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
Storage Temperature ................................ \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
Voltage on Any Pin \\
with Respect to Ground .................................. -1.0 V to +7.0 V \\
Maximum Operating Voltage ........................................... 6.6 V \\
DC Output Current...................................................... 15.0 mA \\
\hline
\end{tabular}
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\section*{DC Characteristics}

The values shown in this table are valid for \(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\) to \(85^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}\) to 5.5 V , unless otherwise noted.
\begin{tabular}{|c|c|c|c|c|c|}
\hline Symbol & Parameter & Condition & Min & Max & Units \\
\hline \(\mathrm{V}_{\text {IL }}\) & Input Low Voltage & (Except EA) & -0.5 & \(0.2 \mathrm{~V}_{\mathrm{CC}}-0.1\) & V \\
\hline \(\mathrm{V}_{\text {IL1 }}\) & Input Low Voltage ( \(\overline{\mathrm{EA}}\) ) & & -0.5 & \(0.2 \mathrm{~V}_{\mathrm{CC}}-0.3\) & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & Input High Voltage & (Except XTAL1, RST) & \(0.2 \mathrm{~V}_{\mathrm{CC}}+0.9\) & \(\mathrm{V}_{\mathrm{CC}}+0.5\) & V \\
\hline \(\mathrm{V}_{\mathrm{IH} 1}\) & Input High Voltage & (XTAL1, RST) & \(0.7 \mathrm{~V}_{\mathrm{CC}}\) & \(\mathrm{V}_{\mathrm{CC}}+0.5\) & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Output Low Voltage \({ }^{(1)}\) (Ports 1,2,3) & \(\mathrm{I}_{\mathrm{OL}}=1.6 \mathrm{~mA}\) & & 0.45 & V \\
\hline \(\mathrm{V}_{\text {OL1 }}\) & Output Low Voltage \({ }^{(1)}\) (Port 0, ALE, PSEN) & \(\mathrm{I}_{\mathrm{OL}}=3.2 \mathrm{~mA}\) & & 0.45 & V \\
\hline \multirow{3}{*}{\(\mathrm{V}_{\mathrm{OH}}\)} & \multirow{3}{*}{\begin{tabular}{l}
Output High Voltage \\
(Ports 1,2,3, ALE, PSEN)
\end{tabular}} & \(\mathrm{I}_{\mathrm{OH}}=-60 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%\) & 2.4 & & V \\
\hline & & \(\mathrm{I}_{\mathrm{OH}}=-25 \mu \mathrm{~A}\) & \(0.75 \mathrm{~V}_{\mathrm{Cc}}\) & & V \\
\hline & & \(\mathrm{I}_{\mathrm{OH}}=-10 \mu \mathrm{~A}\) & \(0.9 \mathrm{~V}_{\mathrm{CC}}\) & & V \\
\hline \multirow{3}{*}{\(\mathrm{V}_{\mathrm{OH} 1}\)} & \multirow{3}{*}{\begin{tabular}{l}
Output High Voltage \\
(Port 0 in External Bus Mode)
\end{tabular}} & \(\mathrm{I}_{\mathrm{OH}}=-800 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%\) & 2.4 & & V \\
\hline & & \(\mathrm{I}_{\text {OH }}=-300 \mu \mathrm{~A}\) & \(0.75 \mathrm{~V}_{\mathrm{CC}}\) & & V \\
\hline & & \(\mathrm{I}_{\mathrm{OH}}=-80 \mu \mathrm{~A}\) & \(0.9 \mathrm{~V}_{\mathrm{CC}}\) & & V \\
\hline \(\mathrm{I}_{\text {IL }}\) & Logical 0 Input Current (Ports 1,2,3) & \(\mathrm{V}_{\mathrm{IN}}=0.45 \mathrm{~V}\) & & -50 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\mathrm{TL}}\) & Logical 1 to 0 Transition Current (Ports 1,2,3) & \(\mathrm{V}_{\text {IN }}=2 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%\) & & -650 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\mathrm{LI}}\) & Input Leakage Current (Port 0, \(\overline{\mathrm{EA}}\) ) & \(0.45<\mathrm{V}_{\text {IN }}<\mathrm{V}_{\mathrm{CC}}\) & & \(\pm 10\) & \(\mu \mathrm{A}\) \\
\hline RRST & Reset Pulldown Resistor & & 50 & 300 & \(\mathrm{K} \Omega\) \\
\hline \(\mathrm{C}_{10}\) & Pin Capacitance & Test Freq. \(=1 \mathrm{MHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & & 10 & pF \\
\hline \multirow{3}{*}{\(\mathrm{I}_{\mathrm{CC}}\)} & \multirow[b]{2}{*}{Power Supply Current} & Active Mode, 12 MHz & & 25 & mA \\
\hline & & Idle Mode, 12 MHz & & 6.5 & mA \\
\hline & Power-down Mode \({ }^{(2)}\) & \(\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}\) & & 50 & \(\mu \mathrm{A}\) \\
\hline
\end{tabular}

Notes: 1. Under steady state (non-transient) conditions, \(\mathrm{I}_{\mathrm{OL}}\) must be externally limited as follows:
Maximum Iol per port pin: 10 mA
Maximum I \(\mathrm{I}_{\mathrm{OL}}\) per 8-bit port:
Port 0: \(26 \mathrm{~mA} \quad\) Ports 1, 2, 3: 15 mA
Maximum total \(\mathrm{I}_{\mathrm{OL}}\) for all output pins: 71 mA
If \(\mathrm{I}_{\mathrm{OL}}\) exceeds the test condition, \(\mathrm{V}_{\mathrm{OL}}\) may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum \(\mathrm{V}_{\mathrm{CC}}\) for Power-down is 2 V .

\section*{AC Characteristics}

Under operating conditions, load capacitance for Port \(0, A L E / \overline{\text { PROG }}\), and \(\overline{\text { PSEN }}=100 \mathrm{pF}\); load capacitance for all other outputs \(=80 \mathrm{pF}\).

\section*{External Program and Data Memory Characteristics}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multirow[b]{2}{*}{Parameter} & \multicolumn{2}{|l|}{12 MHz Oscillator} & \multicolumn{2}{|l|}{Variable Oscillator} & \multirow[b]{2}{*}{Units} \\
\hline & & Min & Max & Min & Max & \\
\hline 1/t \({ }_{\text {CLCL }}\) & Oscillator Frequency & & & 0 & 33 & MHz \\
\hline \(t_{\text {LHLL }}\) & ALE Pulse Width & 127 & & \(2 \mathrm{t}_{\mathrm{CLCL}}-40\) & & ns \\
\hline \(t_{\text {AVLL }}\) & Address Valid to ALE Low & 43 & & \(\mathrm{t}_{\text {CLCL- }}-25\) & & ns \\
\hline \(\mathrm{t}_{\text {LLAX }}\) & Address Hold After ALE Low & 48 & & \(\mathrm{t}_{\text {CLCL- }} 25\) & & ns \\
\hline \(\mathrm{t}_{\text {LLIV }}\) & ALE Low to Valid Instruction In & & 233 & & \(4 t_{\text {CLCL }}-65\) & ns \\
\hline tLLPL & ALE Low to \(\overline{\text { PSEN }}\) Low & 43 & & \(\mathrm{t}_{\text {CLCL- }}-25\) & & ns \\
\hline \(t_{\text {PLPH }}\) & \(\overline{\text { PSEN Pulse Width }}\) & 205 & & \(3 \mathrm{t}_{\mathrm{CLCL}}-45\) & & ns \\
\hline \(\mathrm{t}_{\text {PLIV }}\) & \(\overline{\text { PSEN Low to Valid Instruction In }}\) & & 145 & & \(3 \mathrm{t}_{\text {CLCL- }}-60\) & ns \\
\hline \(\mathrm{t}_{\text {PXIX }}\) & Input Instruction Hold After \(\overline{\text { PSEN }}\) & 0 & & 0 & & ns \\
\hline \(\mathrm{t}_{\text {PXIZ }}\) & Input Instruction Float After \(\overline{\text { PSEN }}\) & & 59 & & \(\mathrm{t}_{\mathrm{CLCL}}-25\) & ns \\
\hline \(\mathrm{t}_{\text {PXAV }}\) & \(\overline{\text { PSEN }}\) to Address Valid & 75 & & \(\mathrm{t}_{\mathrm{CLCL}}{ }^{-8}\) & & ns \\
\hline \(\mathrm{t}_{\text {AVIV }}\) & Address to Valid Instruction In & & 312 & & \(5 \mathrm{t}_{\mathrm{CLCL}}-80\) & ns \\
\hline \(t_{\text {PLAZ }}\) & \(\overline{\text { PSEN Low to Address Float }}\) & & 10 & & 10 & ns \\
\hline \(\mathrm{t}_{\text {RLRH }}\) & \(\overline{\mathrm{RD}}\) Pulse Width & 400 & & \(6 \mathrm{t}_{\mathrm{CLCL}}-100\) & & ns \\
\hline \(t_{\text {WLWH }}\) & \(\overline{\text { WR Pulse Width }}\) & 400 & & \(6 \mathrm{t}_{\text {CLCLL }}{ }^{-100}\) & & ns \\
\hline \(\mathrm{t}_{\text {RLDV }}\) & \(\overline{\mathrm{RD}}\) Low to Valid Data In & & 252 & & \(5 \mathrm{t}_{\text {CLCL }}-90\) & ns \\
\hline \(\mathrm{t}_{\text {RHDX }}\) & Data Hold After \(\overline{\mathrm{RD}}\) & 0 & & 0 & & ns \\
\hline \(\mathrm{t}_{\text {RHDZ }}\) & Data Float After \(\overline{\mathrm{RD}}\) & & 97 & & \(2 \mathrm{t}_{\mathrm{CLCL}}-28\) & ns \\
\hline tLLDV & ALE Low to Valid Data In & & 517 & & \(8 \mathrm{t}_{\mathrm{CLCL}}-150\) & ns \\
\hline \(\mathrm{t}_{\text {AVDV }}\) & Address to Valid Data In & & 585 & & \(9 \mathrm{t}_{\text {CLCL }}-165\) & ns \\
\hline \(\mathrm{t}_{\text {LLWL }}\) & ALE Low to \(\overline{\mathrm{RD}}\) or \(\overline{\mathrm{WR}}\) Low & 200 & 300 & \(3 \mathrm{t}_{\mathrm{CLCL}}-50\) & \(3 \mathrm{t}_{\mathrm{CLCL}}+50\) & ns \\
\hline \(t_{\text {AVWL }}\) & Address to \(\overline{\mathrm{RD}}\) or WR Low & 203 & & \(4 \mathrm{t}_{\text {CLCLL }}-75\) & & ns \\
\hline \(\mathrm{t}_{\text {QVwX }}\) & Data Valid to \(\overline{\mathrm{WR}}\) Transition & 23 & & \(\mathrm{t}_{\text {CLCL }}\)-30 & & ns \\
\hline \(\mathrm{t}_{\text {QVWH }}\) & Data Valid to \(\overline{W R}\) High & 433 & & \(7 \mathrm{t}_{\text {CLCL }}-130\) & & ns \\
\hline \(\mathrm{t}_{\text {WHQX }}\) & Data Hold After \(\overline{W R}\) & 33 & & \(\mathrm{t}_{\text {CLCL- }}\)-25 & & ns \\
\hline \(\mathrm{t}_{\text {RLAZ }}\) & \(\overline{\mathrm{RD}}\) Low to Address Float & & 0 & & 0 & ns \\
\hline \(\mathrm{t}_{\text {WHLH }}\) & \(\overline{\mathrm{RD}}\) or \(\overline{\mathrm{WR}}\) High to ALE High & 43 & 123 & \(\mathrm{t}_{\mathrm{CLCL}}-25\) & \(\mathrm{t}_{\mathrm{CLCL}}+25\) & ns \\
\hline
\end{tabular}

\section*{External Program Memory Read Cycle}


\section*{External Data Memory Read Cycle}


\section*{External Data Memory Write Cycle}


\section*{External Clock Drive Waveforms}


\section*{External Clock Drive}
\begin{tabular}{|l|l|c|c|c|}
\hline Symbol & Parameter & Min & Max & Units \\
\hline \(1 / t_{\text {CLCL }}\) & Oscillator Frequency & 0 & 33 & MHz \\
\hline \(\mathrm{t}_{\mathrm{CLCL}}\) & Clock Period & 30 & & ns \\
\hline \(\mathrm{t}_{\mathrm{CHCX}}\) & High Time & 12 & & ns \\
\hline \(\mathrm{t}_{\mathrm{CLCX}}\) & Low Time & 12 & & ns \\
\hline \(\mathrm{t}_{\mathrm{CLCH}}\) & Rise Time & & 5 & ns \\
\hline \(\mathrm{t}_{\mathrm{CHCL}}\) & Fall Time & 5 & ns \\
\hline
\end{tabular}

\section*{Serial Port Timing: Shift Register Mode Test Conditions}

The values in this table are valid for \(\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}\) to 5.5 V and Load Capacitance \(=80 \mathrm{pF}\).
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Symbol} & \multirow[b]{2}{*}{Parameter} & \multicolumn{2}{|l|}{12 MHz Osc} & \multicolumn{2}{|l|}{Variable Oscillator} & \multirow[b]{2}{*}{Units} \\
\hline & & Min & Max & Min & Max & \\
\hline \(\mathrm{t}_{\text {XLXL }}\) & Serial Port Clock Cycle Time & 1.0 & & \(12 \mathrm{t}_{\text {CLCL }}\) & & \(\mu \mathrm{s}\) \\
\hline \(\mathrm{t}_{\text {QVXH }}\) & Output Data Setup to Clock Rising Edge & 700 & & \(10 \mathrm{CLLCL}^{-133}\) & & ns \\
\hline \(\mathrm{t}_{\mathrm{XHQX}}\) & Output Data Hold After Clock Rising Edge & 50 & & \(2 \mathrm{t}_{\text {CLCL }}-80\) & & ns \\
\hline \(\mathrm{t}_{\text {XHDX }}\) & Input Data Hold After Clock Rising Edge & 0 & & 0 & & ns \\
\hline \(\mathrm{t}_{\text {XHDV }}\) & Clock Rising Edge to Input Data Valid & & 700 & & \(10 \mathrm{t}_{\text {CLCL }}-133\) & ns \\
\hline
\end{tabular}

\section*{Shift Register Mode Timing Waveforms}


\section*{AC Testing Input/Output Waveforms \({ }^{(1)}\)}


Note: 1. AC Inputs during testing are driven at \(\mathrm{V}_{\mathrm{CC}}-0.5 \mathrm{~V}\) for a logic 1 and 0.45 V for a logic 0 . Timing measurements are made at \(\mathrm{V}_{\mathrm{IH}}\) min . for a logic 1 and \(\mathrm{V}_{\mathrm{IL}}\) max. for a logic 0 .

\section*{Float Waveforms \({ }^{(1)}\)}


Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded \(\mathrm{V}_{\mathrm{OH}} / \mathrm{V}_{\mathrm{OL}}\) level occurs.

\section*{Ordering Information}
\begin{tabular}{|c|c|c|c|c|}
\hline \begin{tabular}{l}
Speed \\
(MHz)
\end{tabular} & Power Supply & Ordering Code & Package & Operation Range \\
\hline \multirow[t]{2}{*}{24} & \multirow[t]{2}{*}{4.0 V to 5.5V} & \[
\begin{aligned}
& \text { AT89S51-24AC } \\
& \text { AT89S51-24JC } \\
& \text { AT89S51-24PC } \\
& \text { AT89S51-24SC }
\end{aligned}
\] & \[
\begin{aligned}
& \hline 44 \mathrm{~A} \\
& 44 \mathrm{~J} \\
& 40 \mathrm{P} 6 \\
& 42 \mathrm{PS} 6
\end{aligned}
\] & \[
\begin{aligned}
& \text { Commercial } \\
& \left(0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C}\right)
\end{aligned}
\] \\
\hline & & \begin{tabular}{l}
AT89S51-24AI \\
AT89S51-24JI \\
AT89S51-24PI \\
AT89S51-24SI
\end{tabular} & \begin{tabular}{l}
44A \\
44J \\
40P6 \\
42PS6
\end{tabular} & \[
\begin{gathered}
\text { Industrial } \\
\left(-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)
\end{gathered}
\] \\
\hline 33 & 4.5 V to 5.5 V & \begin{tabular}{l}
AT89S51-33AC \\
AT89S51-33JC \\
AT89S51-33PC \\
AT89S51-33SC
\end{tabular} & \[
\begin{aligned}
& \hline 44 \mathrm{~A} \\
& 44 \mathrm{~J} \\
& 40 \mathrm{P} 6 \\
& 42 \mathrm{PS} 6
\end{aligned}
\] & Commercial \(\left(0^{\circ} \mathrm{C}\right.\) to \(70^{\circ} \mathrm{C}\) ) \\
\hline
\end{tabular}
\begin{tabular}{|l|l|}
\hline \multicolumn{2}{|c|}{ Package Type } \\
\hline 44A & 44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP) \\
\hline 44J & 44-lead, Plastic J-leaded Chip Carrier (PLCC) \\
\hline 40P6 & 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) \\
\hline 42PS6 & 42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) \\
\hline
\end{tabular}

\section*{Packaging Information}

\section*{44A - TQFP}


\section*{44J - PLCC}


Notes: 1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion.

Allowable protrusion is \(.010 "(0.254 \mathrm{~mm})\) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is \(0.004^{\prime \prime}(0.102 \mathrm{~mm})\) maximum.

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
DRAWING NO. REV.

40P6 - PDIP



Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure \(=\mathrm{mm}\) )
\begin{tabular}{|c|c|c|c|c|}
\hline SYMBOL & MIN & NOM & MAX & NOTE \\
\hline A & - & - & 4.83 & \\
\hline A1 & 0.51 & - & - & \\
\hline D & 36.70 & - & 36.96 & Note 2 \\
\hline E & 15.24 & - & 15.88 & \\
\hline E1 & 13.46 & - & 13.97 & Note 2 \\
\hline B & 0.38 & - & 0.56 & \\
\hline B1 & 0.76 & - & 1.27 & \\
\hline L & 3.05 & - & 3.43 & \\
\hline C & 0.20 & - & 0.30 & \\
\hline eB & - & - & 18.55 & \\
\hline e & \multicolumn{4}{|c|}{1.78 TYP } \\
\hline
\end{tabular}

\section*{Atmel Corporation}

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

\section*{Regional Headquarters}

\author{
Europe \\ Atmel Sarl \\ Route des Arsenaux 41 \\ Case Postale 80 \\ CH-1705 Fribourg \\ Switzerland \\ Tel: (41) 26-426-5555 \\ Fax: (41) 26-426-5500 \\ Asia \\ Room 1219 \\ Chinachem Golden Plaza \\ 77 Mody Road Tsimshatsui \\ East Kowloon \\ Hong Kong \\ Tel: (852) 2721-9778 \\ Fax: (852) 2722-1369 \\ Japan \\ 9F, Tonetsu Shinkawa Bldg. \\ 1-24-8 Shinkawa \\ Chuo-ku, Tokyo 104-0033 \\ Japan \\ Tel: (81) 3-3523-3551 \\ Fax: (81) 3-3523-7581
}

\section*{Atmel Operations}

\author{
Memory \\ 2325 Orchard Parkway \\ San Jose, CA 95131, USA \\ Tel: 1(408) 441-0311 \\ Fax: 1(408) 436-4314
}

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60
ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759
Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G750QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

\section*{RF/Automotive}

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

\section*{Biometrics/Imaging/Hi-Rel MPU/}

High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

\section*{Literature Requests www.atmel.com/literature}

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\section*{Absolute Maximum Ratings}
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{3}{*}{If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.}} & Storage Temperature Range & \multirow[t]{2}{*}{\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)} \\
\hline & & Soldering Information & \\
\hline & & Dual-In-Line Package & \\
\hline Supply Voltage & \(+18 \mathrm{~V}\) & Soldering (10 Seconds) & \(260^{\circ} \mathrm{C}\) \\
\hline Power Dissipation (Note 1) & & Small Outline Package & \\
\hline LM555H, LM555CH & 760 mW & Vapor Phase (60 Seconds) & \(215^{\circ} \mathrm{C}\) \\
\hline LM555, LM555CN & 1180 mW & Infrared (15 Seconds) & \(220^{\circ} \mathrm{C}\) \\
\hline \multicolumn{2}{|l|}{Operating Temperature Ranges} & \multicolumn{2}{|l|}{\multirow[t]{3}{*}{See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.}} \\
\hline LM555C & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & & \\
\hline LM555 & \(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) & & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}\right.\) to +15 V , unless othewise specified)}



\section*{Typical Performance Characteristics}


\section*{Applications Information}

\section*{monostable operation}

In this mode of operation, the timer functions as a one-shot (Figure 1). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than \(1 / 3 \mathrm{~V}_{\mathrm{CC}}\) to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.


\section*{FIGURE 1. Monostable}

The voltage across the capacitor then increases exponentially for a period of \(t=1.1 R_{A} C\), at the end of which time the voltage equals \(2 / 3 V_{C C}\). The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 2 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

\(V_{C C}=5 \mathrm{~V}\)
TIME \(=0.1 \mathrm{~ms} / \mathrm{DIV}\).
\(\mathrm{R}_{\mathrm{A}}=9.1 \mathrm{k} \Omega\)
Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.
FIGURE 2. Monostable Waveforms
During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least \(10 \mu \mathrm{~s}\) before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to \(\mathrm{V}_{\mathrm{CC}}\) to avoid any possibility of false triggering.
Figure 3 is a nomograph for easy determination of R, C values for various time delays.
NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.


TL/H/7851-7
FIGURE 3. Time Delay

\section*{ASTABLE OPERATION}

If the circuit is connected as shown in Figure 4 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through \(R_{A}+R_{B}\) and discharges through \(\mathrm{R}_{\mathrm{B}}\). Thus the duty cycle may be precisely set by the ratio of these two resistors.


TL/H/7851-8
FIGURE 4. Astable
In this mode of operation, the capacitor charges and discharges between \(1 / 3 \mathrm{~V}_{\mathrm{CC}}\) and \(2 / 3 \mathrm{~V}_{\mathrm{CC}}\). As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

\section*{Applications Information (Continued)}

Figure 5 shows the waveforms generated in this mode of operation.


TL/H/7851-9

\section*{\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) \\ Top Trace: Output 5V/Div. \\ TIME \(=20 \mu \mathrm{~s} /\) DIV. Bottom Trace: Capacitor Voltage 1V/Div.}
\(\mathrm{R}_{\mathrm{A}}=3.9 \mathrm{k} \Omega\)
\(\mathrm{R}_{\mathrm{B}}=3 \mathrm{k} \Omega\)
\(\mathrm{C}=0.01 \mu \mathrm{~F}\)
FIGURE 5. Astable Waveforms
The charge time (output high) is given by:
\[
t_{1}=0.693\left(R_{A}+R_{B}\right) C
\]

And the discharge time (output low) by:
\[
\mathrm{t}_{2}=0.693\left(\mathrm{R}_{\mathrm{B}}\right) \mathrm{C}
\]

Thus the total period is:
\[
\mathrm{T}=\mathrm{t}_{1}+\mathrm{t}_{2}=0.693\left(\mathrm{R}_{\mathrm{A}}+2 \mathrm{R}_{\mathrm{B}}\right) \mathrm{C}
\]

The frequency of oscillation is:
\[
f=\frac{1}{T}=\frac{1.44}{\left(R_{A}+2 R_{B}\right) C}
\]

Figure 6 may be used for quick determination of these RC values.
The duty cycle is: \(\quad D=\frac{R_{B}}{R_{A}+2 R_{B}}\)


FIGURE 6. Free Running Frequency

\section*{FREQUENCY DIVIDER}

The monostable circuit of Figure 1 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 7 shows the waveforms generated in a divide by three circuit.

\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\)
Top Trace: Input 4V/Div.
TIME \(=20 \mu \mathrm{~s} /\) DIV. Middle Trace: Output 2V/Div.
\(\mathrm{R}_{\mathrm{A}}=9.1 \mathrm{k} \Omega \quad\) Bottom Trace: Capacitor 2V/Div.
\(\mathrm{C}=0.01 \mu \mathrm{~F}\)

\section*{FIGURE 7. Frequency Divider}

\section*{PULSE WIDTH MODULATOR}

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5 . Figure 8 shows the circuit, and in Figure 9 are some waveform examples.


TL/H/7851-12
FIGURE 8. Pulse Width Modulator


TL/H/7851-13
\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\)
Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.
\(\mathrm{TIME}=0.2 \mathrm{~ms}\)
\(\mathrm{R}_{\mathrm{A}}=9.1 \mathrm{k} \Omega\)
\(R_{\mathrm{A}}=9.1 \mathrm{k} \Omega\)
\(\mathrm{C}=0.01 \mu \mathrm{~F}\)
FIGURE 9. Pulse Width Modulator

\section*{PULSE POSITION MODULATOR}

This application uses the timer connected for astable operation, as in Figure 10, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 11 shows the waveforms generated for a triangle wave modulation signal.

Applications Information (Continued)


TL/H/7851-14
FIGURE 10. Pulse Position Modulator


TL/H/7851-15
\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\)
TIME \(=0.1 \mathrm{~ms} /\) DIV .
\(\mathrm{R}_{\mathrm{A}}=3.9 \mathrm{k} \Omega\)
\(\mathrm{R}_{\mathrm{B}}=3 \mathrm{k} \Omega\)
\(\mathrm{R}=0.01 \mu \mathrm{~F}\)
FIGURE 11. Pulse Position Modulator

\section*{LINEAR RAMP}

When the pullup resistor, \(R_{A}\), in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 12 shows a circuit configuration that will perform this function.


FIGURE 12
Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:
\[
\begin{gathered}
T=\frac{2 / 3 V_{C C} R_{E}\left(R_{1}+R_{2}\right) C}{R_{1} V_{C C}-V_{B E}\left(R_{1}+R_{2}\right)} \\
V_{B E} \cong 0.6 V
\end{gathered}
\]

\(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\)
Top Trace: Input 3V/Div.
TIME \(=20 \mu \mathrm{~s} /\) DIV. Middle Trace: Output 5V/Div.
\(\mathrm{R}_{1}=47 \mathrm{k} \Omega \quad\) Bottom Trace: Capacitor Voltage 1V/Div.
\(\mathrm{R}_{2}=100 \mathrm{k} \Omega\)
\(\mathrm{R}_{\mathrm{E}}=2.7 \mathrm{k} \Omega\)
\(\mathrm{C}=0.01 \mu \mathrm{~F}\)
FIGURE 13. Linear Ramp
50\% DUTY CYCLE OSCILLATOR
For a \(50 \%\) duty cycle, the resistors \(R_{A}\) and \(R_{B}\) may be connected as in Figure 14. The time period for the out-

Applications Information (Continued)
put high is the same as previous, \(t_{1}=0.693 R_{A} C\). For the output low it is \(\mathrm{t}_{2}=\)
\[
\left[\left(R_{A} R_{B}\right) /\left(R_{A}+R_{B}\right)\right] C \ln \left[\frac{R_{B}-2 R_{A}}{2 R_{B}-R_{A}}\right]
\]

Thus the frequency of oscillation is \(f=\frac{1}{t_{1}+t_{2}}\)


TL/H/7851-18
FIGURE 14. 50\% Duty Cycle Oscillator
Physical Dimensions inches (millimeters)


Metal Can Package (H)
Order Number LM555H or LM555CH
NS Package Number H08C



\section*{LIFE SUPPORT POLICY}

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
\begin{tabular}{|c|c|c|c|}
\hline \begin{tabular}{l}
National Semiconductor Corporation \\
1111 West Bardin Road Arlington, TX 76017 \\
Tel: 1(800) 272-9959 \\
Fax: 1(800) 737-7018
\end{tabular} & \begin{tabular}{l}
National Semiconductor Europe \\
Fax: (+49) 0-180-530 8586 \\
Email: cnjwge@tevm2.nsc.com \\
Deutsch Tel: (+49) 0-180-530 8585 \\
English Tel: \((+49)\) 0-180-532 7832 \\
Français Tel: \((+49)\) 0-180-532 9358 \\
Italiano Tel: \((+49)\) 0-180-534 1680
\end{tabular} & \begin{tabular}{l}
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13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong \\
Tel: (852) 2737-1600 \\
Fax: (852) 2736-9960
\end{tabular} & \begin{tabular}{l}
National Semiconductor Japan Ltd. \\
Tel: 81-043-299-2309 \\
Fax: 81-043-299-2408
\end{tabular} \\
\hline
\end{tabular}

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Datasheets for electronics components.


Absolute Maximum Ratings (Note)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Supply Voltage
7V
Input Voltage
\(7 V\)
Operating Free Air Temperature Range
DM54LS and 54LS
DM74LS
Storage Temperature Range
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

\section*{Recommended Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Symbol} & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{Parameter}} & \multicolumn{3}{|c|}{DM54LS74A} & \multicolumn{3}{|c|}{DM74LS74A} & \multirow[t]{2}{*}{Units} \\
\hline & & & Min & Nom & Max & Min & Nom & Max & \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply Voltage} & 4.5 & 5 & 5.5 & 4.75 & 5 & 5.25 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High Level Input Voltage} & 2 & & & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low Level Input Voltage} & & & 0.7 & & & 0.8 & V \\
\hline IOH & \multicolumn{2}{|l|}{High Level Output Current} & & & -0.4 & & & -0.4 & mA \\
\hline \(\mathrm{l}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{Low Level Output Current} & & & 4 & & & 8 & mA \\
\hline \(\mathrm{f}_{\text {CLK }}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 2)} & 0 & & 25 & 0 & & 25 & MHz \\
\hline \(\mathrm{f}_{\mathrm{CLK}}\) & \multicolumn{2}{|l|}{Clock Frequency (Note 3)} & 0 & & 20 & 0 & & 20 & MHz \\
\hline \multirow[t]{3}{*}{\(t_{W}\)} & \multirow[t]{3}{*}{Pulse Width (Note 2)} & Clock High & 18 & & & 18 & & & \multirow{3}{*}{ns} \\
\hline & & Preset Low & 15 & & & 15 & & & \\
\hline & & Clear Low & 15 & & & 15 & & & \\
\hline \multirow[t]{3}{*}{\(t_{W}\)} & \multirow[t]{3}{*}{Pulse Width (Note 3)} & Clock High & 25 & & & 25 & & & \multirow{3}{*}{ns} \\
\hline & & Preset Low & 20 & & & 20 & & & \\
\hline & & Clear Low & 20 & & & 20 & & & \\
\hline tsu & \multicolumn{2}{|l|}{Setup Time (Notes 1 and 2)} & \(20 \uparrow\) & & & \(20 \uparrow\) & & & ns \\
\hline tsu & \multicolumn{2}{|l|}{Setup Time (Notes 1 and 3)} & \(25 \uparrow\) & & & \(25 \uparrow\) & & & ns \\
\hline \(\mathrm{t}_{\mathrm{H}}\) & \multicolumn{2}{|l|}{Hold Time (Note 1 and 4)} & \(0 \uparrow\) & & & \(0 \uparrow\) & & & ns \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Free Air Operating Temperature} & -55 & & 125 & 0 & & 70 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Note 1: The symbol ( \(\uparrow\) ) indicates the rising edge of the clock pulse is used for reference.
Note 2: \(\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\), and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
Note 3: \(\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\), and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).
Note 4: \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) and \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\).



54LS74/DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered
Physical Dimensions inches (millimeters) (Continued)

-Lead Ceramic Flat Package (W)
Order Number 54LS74FMQB or DM54LS74AW
NS Package Number W14B

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Email: cnjwge@tevm2.nsc.com \\
Deutsch Tel: (+49) 0-180-530 8585 \\
English Tel: (+49) 0-180-532 7832 \\
Français Tel: \((+49)\) 0-180-532 9358 \\
Italiano Tel: \((+49)\) 0-180-534 1680
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\end{tabular} & \begin{tabular}{l}
National Semiconductor Japan Ltd. \\
Tel: 81-043-299-2309 \\
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\end{tabular} \\
\hline
\end{tabular}

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INA118

\section*{Precision, Low Power INSTRUMENTATION AMPLIFIER}

\section*{FEATURES}
- LOW OFFSET VOLTAGE: \(50 \mu \mathrm{~V}\) max
- LOW DRIFT: \(0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\) max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO \(\pm 40 \mathrm{~V}\)
- WIDE SUPPLY RANGE: \(\pm 1.35\) to \(\pm 18 \mathrm{~V}\)
- LOW QUIESCENT CURRENT: \(350 \mu \mathrm{~A}\)
- 8-PIN PLASTIC DIP, SO-8

\section*{APPLICATIONS}
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

\section*{DESCRIPTION}

The INA118 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain ( 70 kHz at \(\mathrm{G}=100\) ).
A single external resistor sets any gain from 1 to 10,000 . Internal input protection can withstand up to \(\pm 40 \mathrm{~V}\) without damage.
The INA118 is laser trimmed for very low offset voltage \((50 \mu \mathrm{~V})\), drift \(\left(0.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}\right)\) and high common-mode rejection \((110 \mathrm{~dB}\) at \(\mathrm{G}=1000)\). It operates with power supplies as low as \(\pm 1.35 \mathrm{~V}\), and quiescent current is only \(350 \mu \mathrm{~A}\)-ideal for battery operated systems.
The INA118 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) temperature range.


\section*{SPECIFICATIONS}

\section*{ELECTRICAL}

At \(T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega\) unless otherwise noted.
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{PARAMETER} & \multirow[b]{2}{*}{CONDITIONS} & \multicolumn{3}{|c|}{INA118PB, UB} & \multicolumn{3}{|c|}{INA118P, U} & \multirow[b]{2}{*}{UNITS} \\
\hline & & MIN & TYP & MAX & MIN & TYP & MAX & \\
\hline \begin{tabular}{l}
INPUT \\
Offset Voltage, RTI Initial vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode Linear Input Voltage Range \\
Safe Input Voltage Common-Mode Rejection
\end{tabular} & \[
\begin{gathered}
\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
\mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }} \text { to } \mathrm{T}_{\text {MAX }} \\
\mathrm{V}_{\mathrm{S}}= \pm 1.35 \mathrm{~V} \text { to } \pm 18 \mathrm{~V}
\end{gathered}
\]
\[
\begin{gathered}
V_{\mathrm{CM}}= \pm 10 \mathrm{~V}, \Delta \mathrm{R}_{\mathrm{S}}=1 \mathrm{k} \Omega \\
\mathrm{G}=1 \\
\mathrm{G}=10 \\
\mathrm{G}=100 \\
\mathrm{G}=1000
\end{gathered}
\] & \[
\begin{gathered}
(\mathrm{V}+)-1 \\
(\mathrm{~V}-)+1.1 \\
\\
80 \\
97 \\
107 \\
110
\end{gathered}
\] & \[
\begin{gathered}
\pm 10 \pm 50 / \mathrm{G} \\
\pm 0.2 \pm 2 / \mathrm{G} \\
\pm 1 \pm 10 / \mathrm{G} \\
\pm 0.4 \pm 5 / \mathrm{G} \\
10^{10} \| 1 \\
10^{10} \| 4 \\
(\mathrm{~V}+)-0.65 \\
(\mathrm{~V}-)+0.95
\end{gathered}
\]
\[
\begin{gathered}
90 \\
110 \\
120 \\
125
\end{gathered}
\] & \[
\begin{gathered}
\pm 50 \pm 500 / \mathrm{G} \\
\pm 0.5 \pm 20 / \mathrm{G} \\
\pm 5 \pm 100 / \mathrm{G}
\end{gathered}
\]
\[
\pm 40
\] & \[
\begin{gathered}
* \\
* \\
\\
\\
73 \\
89 \\
98 \\
100 \\
\hline
\end{gathered}
\] & \[
\begin{gathered}
\pm 25 \pm 100 / \mathrm{G} \\
\pm 0.2 \pm 5 / \mathrm{G} \\
* \\
* \\
* \\
* \\
* \\
* \\
\\
* \\
* \\
* \\
*
\end{gathered}
\] & \[
\begin{gathered}
\pm 125 \pm 1000 / \mathrm{G} \\
\pm 1 \pm 20 / \mathrm{G} \\
\pm 10 \pm 100 / \mathrm{G}
\end{gathered}
\] & \[
\begin{gathered}
\mu \mathrm{V} \\
\mu \mathrm{~V} /{ }^{\circ} \mathrm{C} \\
\mu \mathrm{~V} / \mathrm{V} \\
\mu \mathrm{~V} / \mathrm{mo} \\
\Omega \| \mathrm{pF} \\
\Omega \| \mathrm{pF} \\
\mathrm{~V} \\
\mathrm{~V} \\
\mathrm{~V} \\
\\
\mathrm{~dB} \\
\mathrm{~dB} \\
\mathrm{~dB} \\
\mathrm{~dB} \\
\hline
\end{gathered}
\] \\
\hline BIAS CURRENT vs Temperature & & & \[
\begin{gathered}
\pm 1 \\
\pm 40
\end{gathered}
\] & \(\pm 5\) & & \[
\begin{aligned}
& * \\
& * \\
& *
\end{aligned}
\] & \(\pm 10\) & \[
\begin{gathered}
\mathrm{nA} \\
\mathrm{pA} /{ }^{\circ} \mathrm{C}
\end{gathered}
\] \\
\hline OFFSET CURRENT vs Temperature & & & \[
\begin{gathered}
\pm 1 \\
\pm 40
\end{gathered}
\] & \(\pm 5\) & & \[
\begin{aligned}
& * \\
& * \\
& *
\end{aligned}
\] & \(\pm 10\) & \[
\begin{gathered}
\mathrm{nA} \\
\mathrm{pA} /{ }^{\prime} \mathrm{C}
\end{gathered}
\] \\
\hline \begin{tabular}{l}
NOISE VOLTAGE, RTI
\[
\begin{aligned}
& f=10 \mathrm{~Hz} \\
& f=100 \mathrm{~Hz} \\
& f=1 \mathrm{kHz} \\
& f_{B}=0.1 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz}
\end{aligned}
\] \\
Noise Current
\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \\
& \mathrm{f}=1 \mathrm{kHz} \\
& \mathrm{f}_{\mathrm{B}}=0.1 \mathrm{~Hz} \text { to } 10 \mathrm{~Hz} \\
& \hline
\end{aligned}
\]
\end{tabular} & \(\mathrm{G}=1000, \mathrm{R}_{\mathrm{S}}=0 \Omega\) & & \[
\begin{gathered}
11 \\
10 \\
10 \\
0.28 \\
\\
2.0 \\
0.3 \\
80 \\
\hline
\end{gathered}
\] & & & \[
\begin{gathered}
* \\
* \\
* \\
* \\
* \\
* \\
* \\
* \\
\hline
\end{gathered}
\] & & \begin{tabular}{l}
\(n V / \sqrt{\mathrm{Hz}}\) \\
\(\mathrm{nV} / \sqrt{\mathrm{Hz}}\) \\
\(\mathrm{nV} / \sqrt{\mathrm{Hz}}\) \\
\(\mu \vee p-p\) \\
\(\mathrm{pA} / \sqrt{\mathrm{Hz}}\) \\
\(\mathrm{pA} / \sqrt{\mathrm{Hz}}\) \\
pAp-p
\end{tabular} \\
\hline \begin{tabular}{l}
GAIN \\
Gain Equation \\
Range of Gain \\
Gain Error \\
Gain vs Temperature \(50 \mathrm{k} \Omega\) Resistance \({ }^{(1)}\) Nonlinearity
\end{tabular} & \[
\begin{gathered}
G=1 \\
G=10 \\
G=100 \\
G=1000 \\
G=1 \\
G=1 \\
G=10 \\
G=100 \\
G=1000
\end{gathered}
\] & 1 & \[
\begin{gathered}
1+\left(50 \mathrm{k} \Omega / \mathrm{R}_{\mathrm{G}}\right) \\
\pm 0.01 \\
\pm 0.02 \\
\pm 0.05 \\
\pm 0.5 \\
\pm 1 \\
\pm 25 \\
\pm 0.0003 \\
\pm 0.0005 \\
\pm 0.0005 \\
\pm 0.002
\end{gathered}
\] & \[
\begin{gathered}
10000 \\
\pm 0.024 \\
\pm 0.4 \\
\pm 0.5 \\
\pm 1 \\
\pm 10 \\
\pm 100 \\
\pm 0.001 \\
\pm 0.002 \\
\pm 0.002 \\
\pm 0.01
\end{gathered}
\] & * & \begin{tabular}{l}
* \\
* \\
* \\
* \\
* \\
* \\
* \\
* \\
* \\
* \\
*
\end{tabular} & \[
\begin{gathered}
* \\
\pm 0.1 \\
\pm 0.5 \\
\pm 0.7 \\
\pm 2 \\
\pm 10 \\
* \\
\pm 0.002 \\
\pm 0.004 \\
\pm 0.004 \\
\pm 0.02
\end{gathered}
\] & \begin{tabular}{l}
V/V \\
V/V \\
\% \\
\% \\
\% \\
\% \\
\(\mathrm{ppm} /{ }^{\circ} \mathrm{C}\) \\
\(\mathrm{ppm} /{ }^{\circ} \mathrm{C}\) \\
\% of FSR \\
\% of FSR \\
\% of FSR \\
\% of FSR
\end{tabular} \\
\hline OUTPUT
Voltage: Positive
Negative
Single Supply High
Single Supply Low
Load Capacitance Stability
Short Circuit Current & \[
\begin{gathered}
\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
\mathrm{~V}_{\mathrm{S}}=+2.7 \mathrm{~V} / 0 \mathrm{~V}(2), \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
\mathrm{~V}_{\mathrm{S}}=+2.7 \mathrm{~V} / 0 \mathrm{~V}(2), \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega
\end{gathered}
\] & \[
\begin{gathered}
(\mathrm{V}+)-1 \\
(\mathrm{~V}-)+0.35 \\
1.8 \\
60
\end{gathered}
\] & \[
\begin{gathered}
(\mathrm{V}+)-0.8 \\
(\mathrm{~V}-)+0.2 \\
2.0 \\
35 \\
1000 \\
+5 /-12
\end{gathered}
\] & & \[
\begin{aligned}
& * \\
& * \\
& * \\
& *
\end{aligned}
\] & \[
\begin{aligned}
& * \\
& * \\
& * \\
& * \\
& * \\
& * \\
& *
\end{aligned}
\] & & \begin{tabular}{l}
V \\
V \\
V \\
mV pF \\
mA
\end{tabular} \\
\hline \begin{tabular}{l}
FREQUENCY RESPONSE \\
Bandwidth, -3 dB \\
Slew Rate Settling Time, 0.01\% \\
Overload Recovery
\end{tabular} & \[
\begin{gathered}
\mathrm{G}=1 \\
\mathrm{G}=10 \\
\mathrm{G}=100 \\
\mathrm{G}=1000 \\
\mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{G}=10 \\
\mathrm{G}=1 \\
\mathrm{G}=10 \\
\mathrm{G}=100 \\
\mathrm{G}=1000 \\
50 \% \text { Overdrive }
\end{gathered}
\] & & 800
500
70
7
0.9
15
15
21
210
20 & & & \[
\begin{aligned}
& * \\
& * \\
& * \\
& * \\
& * \\
& * \\
& * \\
& * \\
& * \\
& * \\
& *
\end{aligned}
\] & & \begin{tabular}{l}
kHz \\
kHz \\
kHz \\
kHz \\
\(\mathrm{V} / \mu \mathrm{s}\) \\
\(\mu \mathrm{s}\) \\
\(\mu \mathrm{S}\) \\
\(\mu \mathrm{s}\) \\
\(\mu \mathrm{s}\) \\
\(\mu \mathrm{s}\)
\end{tabular} \\
\hline \begin{tabular}{l}
POWER SUPPLY \\
Voltage Range Current
\end{tabular} & \(\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}\) & \(\pm 1.35\) & \[
\begin{gathered}
\pm 15 \\
\pm 350
\end{gathered}
\] & \[
\begin{gathered}
\pm 18 \\
\pm 385
\end{gathered}
\] & * & * & * & \[
\begin{gathered}
\mathrm{V} \\
\mu \mathrm{~A}
\end{gathered}
\] \\
\hline \begin{tabular}{l}
TEMPERATURE RANGE \\
Specification \\
Operating \\
\(\theta_{\mathrm{JA}}\)
\end{tabular} & & \[
\begin{aligned}
& -40 \\
& -40
\end{aligned}
\] & 80 & \[
\begin{gathered}
85 \\
125
\end{gathered}
\] & \[
\begin{aligned}
& * \\
& *
\end{aligned}
\] & * & \[
\begin{aligned}
& * \\
& *
\end{aligned}
\] & \[
\begin{gathered}
{ }^{\circ} \mathrm{C} \\
{ }^{\circ} \mathrm{C} \\
{ }^{\circ} \mathrm{C} / \mathrm{W}
\end{gathered}
\] \\
\hline
\end{tabular}
* Specification same as INA118PB, UB.

NOTE: (1) Temperature coefficient of the " \(50 \mathrm{k} \Omega\) " term in the gain equation. (2) Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

PIN CONFIGURATION

8-Pin DIP and SO-8


\section*{ABSOLUTE MAXIMUM RATINGS}
\begin{tabular}{|c|c|}
\hline Supply Voltage & \(\pm 18 \mathrm{~V}\) \\
\hline Analog Input Voltage Range & \(\pm 40 \mathrm{~V}\) \\
\hline Output Short-Circuit (to ground) & Continuous \\
\hline Operating Temperature & \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline Storage Temperature & \(-40^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) \\
\hline Junction Temperature & \(\ldots . .+150^{\circ} \mathrm{C}\) \\
\hline Lead Temperature (soldering, 10s) & .. \(+300^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{ELECTROSTATIC DISCHARGE SENSITIVITY}

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

\section*{ORDERING INFORMATION}
\begin{tabular}{|l|c|c|c|}
\hline PRODUCT & PACKAGE & \begin{tabular}{c} 
PACKAGE \\
DRAWING \\
NUMBER(1)
\end{tabular} & \begin{tabular}{c} 
TEMPERATURE \\
RANGE
\end{tabular} \\
\hline INA118P & 8-Pin Plastic DIP & 006 & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) \\
INA118PB & 8-Pin Plastic DIP & 006 & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) \\
INA118U & SO-8 Surface-Mount & 182 & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) \\
INA118UB & SO-8 Surface-Mount & 182 & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

\footnotetext{
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.
}

\section*{TYPICAL PERFORMANCE CURVES}

\author{
At \(T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}\), unless otherwise noted.
}







를

\section*{TYPICAL PERFORMANCE CURVES (CONT)}

At \(T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}\), unless otherwise noted.







\section*{TYPICAL PERFORMANCE CURVES (CONT)}

\author{
At \(T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}\), unless otherwise noted.
}


INPUT BIAS AND OFFSET CURRENT






\section*{를}

\section*{TYPICAL PERFORMANCE CURVES (CONT)}

At \(T_{A}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 15 \mathrm{~V}\), unless otherwise noted.



10 \(\mu \mathrm{s} / \mathrm{div}\)

INPUT-REFERRED NOISE, 0.1 Hz to 10 Hz

\(0.1 \mu \mathrm{~V} / \mathrm{div}\)

\(100 \mu \mathrm{~s} / \mathrm{div}\)


\section*{APPLICATION INFORMATION}

Figure 1 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.
The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of \(12 \Omega\) in series with the Ref pin will cause a typical device to degrade to approximately 80 dB CMR \((\mathrm{G}=1)\).

\section*{SETTING THE GAIN}

Gain of the INA118 is set by connecting a single external resistor, \(\mathrm{R}_{\mathrm{G}}\), connected between pins 1 and 8 :
\[
\begin{equation*}
\mathrm{G}=1+\frac{50 \mathrm{k} \Omega}{\mathrm{R}_{\mathrm{G}}} \tag{1}
\end{equation*}
\]

Commonly used gains and resistor values are shown in Figure 1.
The \(50 \mathrm{k} \Omega\) term in Equation 1 comes from the sum of the two internal feedback resistors of \(\mathrm{A}_{1}\) and \(\mathrm{A}_{2}\). These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, \(\mathrm{R}_{\mathrm{G}}\), also affects gain. \(\mathrm{R}_{\mathrm{G}}\) 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

\section*{DYNAMIC PERFORMANCE}

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.
The INA118 exhibits approximately 3 dB peaking at 500 kHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable \(+6 \mathrm{~dB} /\) octave due to a response zero. A simple pole at 300 kHz or lower will produce a flat passband unity gain response.
\begin{tabular}{|c|c|c|}
\hline \begin{tabular}{c} 
DESIRED \\
GAIN
\end{tabular} & \begin{tabular}{c}
\(\mathbf{R}_{\mathbf{G}}\) \\
\((\Omega)\)
\end{tabular} & \begin{tabular}{c} 
NEAREST \(\mathbf{1 \%} \mathbf{R}_{\mathbf{G}}\) \\
\((\Omega)\)
\end{tabular} \\
\hline 1 & NC & NC \\
2 & 50.00 k & 49.9 k \\
5 & 12.50 k & 12.4 k \\
10 & 5.556 k & 5.62 k \\
20 & 2.632 k & 2.61 k \\
50 & 1.02 k & 1.02 k \\
100 & 505.1 & 511 \\
200 & 251.3 & 249 \\
500 & 100.2 & 100 \\
1000 & 50.05 & 49.9 \\
2000 & 25.01 & 24.9 \\
5000 & 10.00 & 10 \\
10000 & 5.001 & 4.99 \\
\hline
\end{tabular}

NC: No Connection.


Also drawn in simplified form:


FIGURE 1. Basic Connections.

\section*{NOISE PERFORMANCE}

The INA118 provides very low noise in most applications. For differential source impedances less than \(1 \mathrm{k} \Omega\), the INA103 may provide lower noise. For source impedances greater than \(50 \mathrm{k} \Omega\), the INA111 FET-Input Instrumentation Amplifier may provide lower noise.
Low frequency noise of the INA118 is approximately \(0.28 \mu \mathrm{~V} p-\mathrm{p}\) measured from 0.1 to \(10 \mathrm{~Hz}(\mathrm{G} \geq 100)\). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

\section*{OFFSET TRIMMING}

The INA118 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good commonmode rejection.


FIGURE 2. Optional Trimming of Output Offset Voltage.

\section*{INPUT BIAS CURRENT RETURN PATH}

The input impedance of the INA118 is extremely highapproximately \(10^{10} \Omega\). However, a path must be provided for the input bias current of both inputs. This input bias current is approximately \(\pm 5 \mathrm{nA}\). High input impedance means that this input bias current changes very little with varying input voltage.
Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the commonmode range of the INA118 and the input amplifiers will saturate.
If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.


FIGURE 3. Providing an Input Common-Mode Current Path.

\section*{INPUT COMMON-MODE RANGE}

The linear input voltage range of the input circuitry of the INA118 is from approximately 0.6 V below the positive supply voltage to 1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of amplifiers \(\mathrm{A}_{1}\) and \(\mathrm{A}_{2}\). Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage-see performance curves "Input Common-Mode Range vs Output Voltage".

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA118 will be near 0V even though both inputs are overloaded.

\section*{LOW VOLTAGE OPERATION}

The INA118 can be operated on power supplies as low as \(\pm 1.35 \mathrm{~V}\). Performance of the INA118 remains excellent with power supplies ranging from \(\pm 1.35 \mathrm{~V}\) to \(\pm 18 \mathrm{~V}\). Most parameters vary only slightly throughout this supply voltage rangesee typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input commonmode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for a various supply voltages and gains.

\section*{SINGLE SUPPLY OPERATION}

The INA118 can be used on single power supplies of +2.7 V to +36 V . Figure 5 shows a basic single supply circuit. The output Ref terminal is connected to ground. Zero differential input voltage will demand an output voltage of 0 V (ground). Actual output voltage swing is limited to approximately 35 mV above ground, when the load is referred to ground as shown. The typical performance curve "Output Voltage vs Output Current" shows how the output voltage swing varies with output current.
With single supply operation, \(\mathrm{V}_{\text {IN }}^{+}\)and \(\mathrm{V}_{\text {IN }}^{-}\)must both be 0.98 V above ground for linear operation. You cannot, for instance, connect the inverting input to ground and measure a voltage connected to the non-inverting input.
To illustrate the issues affecting low voltage operation, consider the circuit in Figure 5. It shows the INA118, operating from a single 3 V supply. A resistor in series with the low side of the bridge assures that the bridge output
voltage is within the common-mode range of the amplifier's inputs. Refer to the typical performance curve "Input Com-mon-Mode Range vs Output Voltage" for 3V single supply operation.

\section*{INPUT PROTECTION}

The inputs of the INA118 are individually protected for voltages up to \(\pm 40 \mathrm{~V}\). For example, a condition of -40 V on one input and +40 V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5 mA . The typical performance curve "Input Bias Current vs Input Overload Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

\section*{INSIDE THE INA118}

Figure 1 shows a simplified representation of the INA118. The more detailed diagram shown here provides additional insight into its operation.
Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 1.5 to 5 mA .

The differential input voltage is buffered by \(Q_{1}\) and \(Q_{2}\) and impressed across \(R_{G}\), causing a signal current to flow through \(\mathrm{R}_{\mathrm{G}}, \mathrm{R}_{1}\) and \(\mathrm{R}_{2}\). The output difference amp, \(\mathrm{A}_{3}\), removes the common-mode component of the input signal and refers the output signal to the Ref terminal.

Equations in the figure describe the output voltages of \(\mathrm{A}_{1}\) and \(\mathrm{A}_{2}\). The \(\mathrm{V}_{\mathrm{BE}}\) and IR drop across \(\mathrm{R}_{1}\) and \(\mathrm{R}_{2}\) produce output voltages on \(A_{1}\) and \(A_{2}\) that are approximately 1 V lower than the input voltages.
\(\mathrm{A}_{1}\) Out \(=\mathrm{V}_{\mathrm{CM}}-\mathrm{V}_{\mathrm{BE}}-(10 \mu \mathrm{~A} \cdot 25 \mathrm{k} \Omega)-\mathrm{V}_{\mathrm{O}} / 2\)
\(A_{2}\) Out \(=V_{C M}-V_{B E}-(10 \mu A \cdot 25 k \Omega)+V_{\mathrm{O}} / 2\)
Output Swing Range \(\mathrm{A}_{1}, \mathrm{~A}_{2} ;(\mathrm{V}+)-0.65 \mathrm{~V}\) to \((\mathrm{V}-)+0.06 \mathrm{~V}\)
Amplifier Linear Input Range: \((\mathrm{V}+)-0.65 \mathrm{~V}\) to \((\mathrm{V}-)+0.98 \mathrm{~V}\)


FIGURE 4. INA118 Simplified Circuit Diagram.


FIGURE 5. Single-Supply Bridge Amplifier.


FIGURE 6. AC-Coupled Instrumentation Amplifier.


FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.


FIGURE 8. Differential Voltage to Current Converter.


FIGURE 9. ECG Amplifier With Right-Leg Drive.

\section*{Appendix O-Index}
\begin{tabular}{|c|c|}
\hline Document/File & Description \\
\hline Presentation & A PowerPoint presentation designed to lead the reader/viewer into some of the more critical screens that will seen on the GUI. Screen captures of the Remote GUI (RGUI) as well as the Acebus - 8051 Microconrtoller Family Development Environment - are also included in this presentation. Each slide/screen capture is accompanied by a brief explanation and notes. \\
\hline System Evaluation & A spreadsheet containing injection, and system acquired data, using the Calibration Screen. This data is used to evaluate the accuracy of the data acquisition hardware as well as the GUI data evaluation and calculation algorithms. Graphs are plotted graphically display the test results. \\
\hline Repeatability Test As Recorded & A spreadsheet containing the raw system acquired and evaluated date for the repeatability test. \\
\hline Repeatability Test with Highlights & A spreadsheet containing the same data as displayed in the file mentioned above "Repeatability Test As Recorded", with the highest and lowest recorded being highlighted. Also displayed is the Forty Point Average and the Difference Between The Averaged Maximum And Minimum Acquired Values. Graphs are plotted graphically display the test results. \\
\hline \[
\begin{gathered}
\text { Test Results } 1 \\
\text { 2006-4-12 } \\
\text { 13H11M2 } \\
\hline
\end{gathered}
\] & Test results captured and stored for a simulated 10 pair bar test. This spreadsheet displays a typical test recording with all possible faults taking into account. \\
\hline \begin{tabular}{l}
Test Results \\
2006-4-12 \\
13H53M53
\end{tabular} & Another set of test results captured and stored for a simulated 10 pair bar test. This spreadsheet displays a typical test recording with all possible faults taking into account. Note that in this spreadsheet there are only 9 recordings of 100 successive readings. This is because an Emergency Stop was invoked on the last pair of bars. \\
\hline All Component Datasheets & Datasheets \\
\hline
\end{tabular}

\section*{International IsR Rectifier}
- Surface Mount (IRLR120N)
- Straight Lead (IRLU120N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

\section*{Description}

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for throughhole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

IRLR/U120N HEXFET \({ }^{\circledR}\) Power MOSFET


\section*{Absolute Maximum Ratings}
\begin{tabular}{|c|c|c|c|}
\hline & Parameter & Max. & Units \\
\hline \(\mathrm{I}_{\mathrm{D}} @ \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}\) & Continuous Drain Current, \(\mathrm{V}_{\mathrm{GS}}\) @ 10V & 10 & \multirow{3}{*}{A} \\
\hline \(\mathrm{I}_{\mathrm{D}} @ \mathrm{~T}_{\mathrm{C}}=100^{\circ} \mathrm{C}\) & Continuous Drain Current, \(\mathrm{V}_{\mathrm{GS}}\) @ 10V & 7.0 & \\
\hline \(\mathrm{I}_{\text {DM }}\) & Pulsed Drain Current (1) © & 35 & \\
\hline \(\mathrm{P}_{\mathrm{D}} @ \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}\) & Power Dissipation & 48 & W \\
\hline & Linear Derating Factor & 0.32 & W/ \({ }^{\circ} \mathrm{C}\) \\
\hline \(\mathrm{V}_{\mathrm{GS}}\) & Gate-to-Source Voltage & \(\pm 16\) & V \\
\hline \(\mathrm{E}_{\text {AS }}\) & Single Pulse Avalanche Energy (2) (6) & 85 & mJ \\
\hline \(\mathrm{I}_{\text {AR }}\) & Avalanche Current(1) © & 6.0 & A \\
\hline \(\mathrm{E}_{\text {AR }}\) & Repetitive Avalanche Energy (1) © & 4.8 & mJ \\
\hline dv/dt & Peak Diode Recovery dv/dt (3) & 5.0 & V/ns \\
\hline \[
\begin{aligned}
& \hline \mathrm{T}_{\mathrm{J}} \\
& \mathrm{~T}_{\mathrm{STG}}
\end{aligned}
\] & Operating Junction and Storage Temperature Range & -55 to +175 & \multirow[t]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & Soldering Temperature, for 10 seconds & 300 (1.6mm from case ) & \\
\hline
\end{tabular}

Thermal Resistance
\begin{tabular}{|l|l|c|c|c|}
\hline & Parameter & Typ. & Max. & Units \\
\hline\(R_{\theta J C}\) & Junction-to-Case & - & 3.1 & \\
\hline\(R_{\theta J A}\) & Junction-to-Ambient (PCB mount) \({ }^{* *}\) & - & 50 & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) \\
\hline \(\mathrm{R}_{\theta \mathrm{JA}}\) & Junction-to-Ambient & - & 110 & \\
\hline
\end{tabular}

Electrical Characteristics \(@ \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\) (unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline & Parameter & Min. & Typ. & Max. & Units & Conditions \\
\hline \(\mathrm{V}_{\text {(BR) }{ }^{\text {dss }}}\) & Drain-to-Source Breakdown Voltage & 100 & - & - & V & \(\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=250 \mu \mathrm{~A}\) \\
\hline \(\Delta \mathrm{V}_{\text {(BR) }{ }^{\text {dss }} / \Delta \mathrm{T}_{\mathrm{J}}}\) & Breakdown Voltage Temp. Coefficient & - & 0.12 & - & V/ \({ }^{\circ} \mathrm{C}\) & Reference to \(25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA}\) \\
\hline \multirow{3}{*}{\(\mathrm{R}_{\text {DS(on) }}\)} & \multirow{3}{*}{Static Drain-to-Source On-Resistance} & - & - & 0.185 & \multirow{3}{*}{W} & \(\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A}\) (4) \\
\hline & & - & - & 0.225 & & \(\mathrm{V}_{\mathrm{GS}}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A} \oplus\) \\
\hline & & - & - & 0.265 & & \(\mathrm{V}_{\mathrm{GS}}=4.0 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=5.0 \mathrm{~A} \mathrm{©}\) \\
\hline \(\mathrm{V}_{\mathrm{GS} \text { (th) }}\) & Gate Threshold Voltage & 1.0 & - & 2.0 & V & \(\mathrm{V}_{\mathrm{DS}}=\mathrm{V}_{\mathrm{GS}}, \mathrm{I}_{\mathrm{D}}=250 \mu \mathrm{~A}\) \\
\hline \(\mathrm{gfs}^{\text {f }}\) & Forward Transconductance & 3.1 & - & - & S & \(\mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A}\) © \\
\hline \multirow[b]{2}{*}{ldss} & \multirow{2}{*}{Drain-to-Source Leakage Current} & - & - & 25 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} & \(\mathrm{V}_{\mathrm{DS}}=100 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}\) \\
\hline & & - & - & 250 & & \(\mathrm{V}_{\mathrm{DS}}=80 \mathrm{~V}, \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V}, \mathrm{~T}_{J}=150^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{IGSs} & Gate-to-Source Forward Leakage & - & - & 100 & \multirow[t]{2}{*}{nA} & \(\mathrm{V}_{\mathrm{GS}}=16 \mathrm{~V}\) \\
\hline & Gate-to-Source Reverse Leakage & - & - & -100 & & \(\mathrm{V}_{\mathrm{GS}}=-16 \mathrm{~V}\) \\
\hline \(\mathrm{Q}_{\mathrm{g}}\) & Total Gate Charge & - & - & 20 & \multirow{3}{*}{nC} & \(\mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A}\) \\
\hline \(\mathrm{Q}_{\mathrm{gs}}\) & Gate-to-Source Charge & - & - & 4.6 & & \(V_{\text {DS }}=80 \mathrm{~V}\) \\
\hline \(\mathrm{Q}_{\mathrm{gd}}\) & Gate-to-Drain ("Miller") Charge & - & - & 10 & & \(\mathrm{V}_{\mathrm{GS}}=5.0 \mathrm{~V}\), See Fig. 6 and 13 (4) © \\
\hline \(\mathrm{t}_{\text {d(on) }}\) & Turn-On Delay Time & - & 4.0 & - & \multirow{4}{*}{ns} & \multirow[t]{4}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{DD}}=50 \mathrm{~V} \\
& \mathrm{I}_{\mathrm{D}}=6.0 \mathrm{~A} \\
& \mathrm{R}_{\mathrm{G}}=11 \Omega, \mathrm{~V}_{\mathrm{GS}}=5.0 \mathrm{~V} \\
& \mathrm{R}_{\mathrm{D}}=8.2 \Omega \text {, See Fig. } 10 \text { (4)(6) }
\end{aligned}
\]} \\
\hline \(\mathrm{tr}_{\mathrm{r}}\) & Rise Time & - & 35 & - & & \\
\hline \(\mathrm{t}_{\mathrm{d} \text { (off) }}\) & Turn-Off Delay Time & - & 23 & - & & \\
\hline \(\mathrm{t}_{\mathrm{f}}\) & Fall Time & & 22 & & & \\
\hline \(L_{D}\) & Internal Drain Inductance & - & 4.5 & - & \multirow[t]{2}{*}{nH} & \multirow[t]{2}{*}{\begin{tabular}{l}
Between lead, \\
6 mm (0.25in.) \\
from package \\
and center of die contact(5)
\end{tabular}} \\
\hline Ls & Internal Source Inductance & - & 7.5 & - & & \\
\hline \(\mathrm{C}_{\text {iss }}\) & Input Capacitance & - & 440 & - & \multirow{3}{*}{pF} & \multirow[t]{3}{*}{\[
\begin{aligned}
& \hline \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{DS}}=25 \mathrm{~V} \\
& f=1.0 \mathrm{MHz} \text {, See Fig. } 5 \odot
\end{aligned}
\]} \\
\hline \(\mathrm{C}_{\text {oss }}\) & Output Capacitance & - & 97 & - & & \\
\hline \(\mathrm{C}_{\text {rss }}\) & Reverse Transfer Capacitance & - & 50 & - & & \\
\hline
\end{tabular}

Source-Drain Ratings and Characteristics
\begin{tabular}{|l|l|c|c|c|c|l|}
\hline & \multicolumn{1}{|c|}{ Parameter } & Min. & Typ. & Max. & Units & \multicolumn{1}{c|}{ Conditions } \\
\hline\(I_{\mathrm{S}}\) & \begin{tabular}{l} 
Continuous Source Current \\
(Body Diode)
\end{tabular} & - & - & 10 & & \begin{tabular}{l} 
MOSFET symbol \\
showing the \\
integral reverse \\
\(p-n\) \\
\(j u n c t i o n ~ d i o d e . ~\)
\end{tabular}
\end{tabular}

\section*{Notes:}
(1) Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11)
(2) \(\mathrm{V}_{\mathrm{DD}}=25 \mathrm{~V}\), starting \(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{L}=4.7 \mathrm{mH}\) \(\mathrm{R}_{\mathrm{G}}=25 \Omega\), \(\mathrm{I}_{\mathrm{AS}}=6.0 \mathrm{~A}\). (See Figure 12)
(3) \(\mathrm{I}_{\mathrm{SD}} \leq 6.0 \mathrm{~A}, \mathrm{di} / \mathrm{dt} \leq 340 \mathrm{~A} / \mu \mathrm{s}, \mathrm{V}_{\mathrm{DD}} \leq \mathrm{V}_{(\mathrm{BR}) \mathrm{DSS}}\), (6) Uses IRL520N data and test conditions. \(\mathrm{T}_{\mathrm{J}} \leq 175^{\circ} \mathrm{C}\)
** When mounted on 1 " square PCB (FR-4 or G-10 Material ) .
For recommended footprint and soldering techniques refer to application note \#AN-994 2


Fig 1. Typical Output Characteristics


Fig 3. Typical Transfer Characteristics


Fig 2. Typical Output Characteristics


Fig 4. Normalized On-Resistance
Vs. Temperature


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage


Fig 8. Maximum Safe Operating Area

International IOR Rectifier


Fig 9. Maximum Drain Current Vs. Case Temperature


Fig 10a. Switching Time Test Circuit


Fig 10b. Switching Time Waveforms


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit


Fig 12b. Unclamped Inductive Waveforms


Fig 13a. Basic Gate Charge Waveform


Fig 12c. Maximum Avalanche Energy Vs. Drain Current


Fig 13b. Gate Charge Test Circuit
www.irf.com


Fig 14. For N-Channel HEXFETS

\section*{IRLR/U120N}

International IER Rectifier

\section*{Package Outline}

\section*{TO-252AA Outline}

Dimensions are shown in millimeters (inches)


Part Marking Information TO-252AA (D-PARK)
```

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P

```


\section*{Package Outline}

\section*{TO-251AA Outline}

Dimensions are shown in millimeters (inches)


\section*{Part Marking Information \\ TO-251AA (I-PARK)}

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY LOT CODE 9U1P
INTERNATIONAL
RECTIFIER
LOGO

\section*{Tape \& Reel Information}

\section*{TO-252AA}


NOTES
1. OUTLINE CONFORMS TO EIA-481.

\title{
International \\ ISR Rectifier
}

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\section*{Absolute Maximum Ratings}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

\section*{(Note 5)}
Supply Voltage
Power Dissipation (Note 1)
Differential Input Voltage
Input Voltage (Note 2)
Output Short Circuit Duration
Operating Temperature Range
Storage Temperature Range
Junction Temperature
Soldering Information
N-Package (10 seconds)
J- or H-Package (10 seconds)
M-Package
Vapor Phase (60 seconds)
Infrared (15 seconds)
LM741A
\(\pm 22 \mathrm{~V}\)
500 mW
\(\pm 30 \mathrm{~V}\)
\(\pm 15 \mathrm{~V}\)
Continuous
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\)
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\(150^{\circ} \mathrm{C}\)

\(260^{\circ} \mathrm{C}\)
\(300^{\circ} \mathrm{C}\)

\(215^{\circ} \mathrm{C}\)
\(215^{\circ} \mathrm{C}\)
LM741E
\(\pm 22 \mathrm{~V}\)
500 mW
\(\pm 30 \mathrm{~V}\)
\(\pm 15 \mathrm{~V}\)
Continuous
\(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
\(100^{\circ} \mathrm{C}\)

\(260^{\circ} \mathrm{C}\)
\(300^{\circ} \mathrm{C}\)

\(215^{\circ} \mathrm{C}\)
\(215^{\circ} \mathrm{C}\)
\begin{tabular}{cc} 
LM741 & LM741C \\
\(\pm 22 \mathrm{~V}\) & \(\pm 18 \mathrm{~V}\) \\
500 mW & 500 mW \\
\(\pm 30 \mathrm{~V}\) & \(\pm 30 \mathrm{~V}\) \\
\(\pm 15 \mathrm{~V}\) & \(\pm 15 \mathrm{~V}\) \\
Continuous & Continuous \\
\(-55^{\circ} \mathrm{C}\) to \(+125^{\circ} \mathrm{C}\) & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) \\
\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
\(150^{\circ} \mathrm{C}\) & \(100^{\circ} \mathrm{C}\) \\
& \\
\(260^{\circ} \mathrm{C}\) & \(260^{\circ} \mathrm{C}\) \\
\(300^{\circ} \mathrm{C}\) & \(300^{\circ} \mathrm{C}\) \\
& \\
\(215^{\circ} \mathrm{C}\) & \(215^{\circ} \mathrm{C}\) \\
\(215^{\circ} \mathrm{C}\) & \(215^{\circ} \mathrm{C}\)
\end{tabular}

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.
ESD Tolerance (Note 6)
400 V
400 V
400 V
400 V

\section*{Electrical Characteristics (Note 3)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{Parameter} & \multirow[t]{2}{*}{Conditions} & \multicolumn{3}{|l|}{LM741A/LM741E} & \multicolumn{3}{|c|}{LM741} & \multicolumn{3}{|c|}{LM741C} & \multirow[t]{2}{*}{Units} \\
\hline & & Min & Typ & Max & Min & Typ & Max & Min & Typ & Max & \\
\hline \multirow[t]{2}{*}{Input Offset Voltage} & \[
\begin{aligned}
& \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\
& \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{S}} \leq 50 \Omega \\
& \hline
\end{aligned}
\] & & 0.8 & 3.0 & & 1.0 & 5.0 & & 2.0 & 6.0 & \[
\begin{aligned}
& \mathrm{mV} \\
& \mathrm{mV}
\end{aligned}
\] \\
\hline & \[
\begin{aligned}
& \mathrm{T}_{\mathrm{AMIN}} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{AMAX}} \\
& \mathrm{R}_{\mathrm{S}} \leq 50 \Omega \\
& \mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega \\
& \hline
\end{aligned}
\] & & & 4.0 & & & 6.0 & & & 7.5 & \[
\begin{aligned}
& \mathrm{mV} \\
& \mathrm{mV}
\end{aligned}
\] \\
\hline Average Input Offset Voltage Drift & & & & 15 & & & & & & & \(\mu \mathrm{V} /{ }^{\circ} \mathrm{C}\) \\
\hline Input Offset Voltage Adjustment Range & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}\) & \(\pm 10\) & & & & \(\pm 15\) & & & \(\pm 15\) & & mV \\
\hline \multirow[t]{2}{*}{Input Offset Current} & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & & 3.0 & 30 & & 20 & 200 & & 20 & 200 & nA \\
\hline & \(\mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }}\) & & & 70 & & 85 & 500 & & & 300 & nA \\
\hline Average Input Offset Current Drift & & & & 0.5 & & & & & & & \(n A /{ }^{\circ} \mathrm{C}\) \\
\hline \multirow[t]{2}{*}{Input Bias Current} & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & & 30 & 80 & & 80 & 500 & & 80 & 500 & nA \\
\hline & \(\mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }}\) & & & 0.210 & & & 1.5 & & & 0.8 & \(\mu \mathrm{A}\) \\
\hline \multirow[t]{2}{*}{Input Resistance} & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}\) & 1.0 & 6.0 & & 0.3 & 2.0 & & 0.3 & 2.0 & & \(\mathrm{M} \Omega\) \\
\hline & \[
\begin{aligned}
& \mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }} \\
& \mathrm{V}_{\mathrm{S}}= \pm 20 \mathrm{~V}
\end{aligned}
\] & 0.5 & & & & & & & & & \(\mathrm{M} \Omega\) \\
\hline \multirow[t]{2}{*}{Input Voltage Range} & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & & & & & & & \(\pm 12\) & \(\pm 13\) & & V \\
\hline & \(\mathrm{T}_{\text {AMIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {AMAX }}\) & & & & \(\pm 12\) & \(\pm 13\) & & & & & V \\
\hline \multirow[t]{2}{*}{Large Signal Voltage Gain} & \[
\begin{aligned}
& \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega \\
& \mathrm{~V}_{\mathrm{S}}= \pm 20 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 15 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}
\end{aligned}
\] & 50 & & & 50 & 200 & & 20 & 200 & & \[
\begin{aligned}
& \mathrm{V} / \mathrm{mV} \\
& \mathrm{~V} / \mathrm{mV}
\end{aligned}
\] \\
\hline & \[
\begin{aligned}
& \mathrm{T}_{\mathrm{AMIN}} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{AMAX}}, \\
& \mathrm{R}_{\mathrm{L}} \geq 2 \mathrm{k} \Omega, \\
& \mathrm{~V}_{\mathrm{S}}= \pm 20 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 15 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{S}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{S}}= \pm 5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 2 \mathrm{~V} \\
& \hline
\end{aligned}
\] & \[
\begin{aligned}
& 32 \\
& 10 \\
& \hline
\end{aligned}
\] & & & 25 & & & 15 & & & \[
\begin{aligned}
& \mathrm{V} / \mathrm{mV} \\
& \mathrm{~V} / \mathrm{mV} \\
& \mathrm{~V} / \mathrm{mV}
\end{aligned}
\] \\
\hline
\end{tabular}



\section*{Physical Dimensions inches (millimeters)}


Physical Dimensions inches (millimeters) (Continued)


Physical Dimensions inches (millimeters) (Continued)


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National Semiconductor Corporation \\
1111 West Bardin Road \\
Arlington, TX 76017 \\
Tel: 1(800) 272-9959 \\
Fax: 1(800) 737-7018
\end{tabular} & \begin{tabular}{l}
National Semiconductor Europe \\
Fax: (+49) 0-180-530 8586 \\
Email: cnjwge @tevm2.nsc.com \\
Deutsch Tel: (+49) 0-180-530 8585 \\
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Italiano Tel: (+49) 0-180-534 1680
\end{tabular} & \begin{tabular}{l}
National Semiconductor Hong Kong Ltd. \\
13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong \\
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\section*{LM211, LM311}

\section*{Single Comparators}

The ability to operate from a single power supply of 5.0 V to 30 V or \(\pm 15 \mathrm{~V}\) split supplies, as commonly used with operational amplifiers, makes the LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the \(\mathrm{V}_{\mathrm{CC}}\) or the \(\mathrm{V}_{\mathrm{EE}}\) supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 V at currents to 50 mA , therefore, the LM211/LM311 can be used to drive relays, lamps or solenoids.

\section*{Features}
- \(\mathrm{Pb}-\) Free Packages are Available


Single Supply
Split Power Supply with Offset Balance


Input polarity is reversed when GND pin is used as an output.

Ground-Referred Load


Input polarity is reversed when GND pin is used as an output.

Load Referred to Negative Supply


Strobe Capability

Figure 1. Typical Comparator Design Configurations


\section*{ON Semiconductor \({ }^{\text {² }}\)}

\section*{http://onsemi.com}


PDIP-8 N SUFFIX CASE 626

SOIC-8
D SUFFIX
CASE 751

PIN CONNECTIONS


\section*{ORDERING \& DEVICE MARKING INFORMATION}

See detailed ordering and shipping information and marking information in the package dimensions section on pag 7 of this data sheet.

\section*{LM211, LM311}

MAXIMUM RATINGS \(\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.\), unless otherwise noted.)
\begin{tabular}{|c|c|c|c|c|}
\hline Rating & Symbol & LM211 & LM311 & Unit \\
\hline Total Supply Voltage & \(\mathrm{V}_{\mathrm{CC}}+\mathrm{V}_{\mathrm{EE}} \mid\) & 36 & 36 & Vdc \\
\hline Output to Negative Supply Voltage & \(\mathrm{V}_{\mathrm{O}}-\mathrm{V}_{\mathrm{EE}}\) & 50 & 40 & Vdc \\
\hline Ground to Negative Supply Voltage & \(\mathrm{V}_{\mathrm{EE}}\) & 30 & 30 & Vdc \\
\hline Input Differential Voltage & \(\mathrm{V}_{\text {ID }}\) & \(\pm 30\) & \(\pm 30\) & Vdc \\
\hline Input Voltage (Note 2) & \(V_{\text {in }}\) & \(\pm 15\) & \(\pm 15\) & Vdc \\
\hline Voltage at Strobe Pin & - & \(\mathrm{V}_{\mathrm{CC}}\) to \(\mathrm{V}_{\mathrm{CC}}-5\) & \(\mathrm{V}_{\mathrm{CC}}\) to \(\mathrm{V}_{\mathrm{CC}}-5\) & Vdc \\
\hline \begin{tabular}{l}
Power Dissipation and Thermal Characteristics Plastic DIP \\
Derate Above \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)
\end{tabular} & \[
\begin{gathered}
\mathrm{P}_{\mathrm{D}} \\
\mathrm{R}_{\text {日JA }} \\
\hline
\end{gathered}
\] & \multicolumn{2}{|c|}{\[
\begin{aligned}
& 625 \\
& 5.0
\end{aligned}
\]} & \[
\begin{gathered}
\mathrm{mW} \\
\mathrm{~mW} /{ }^{\circ} \mathrm{C}
\end{gathered}
\] \\
\hline Operating Ambient Temperature Range & \(\mathrm{T}_{\mathrm{A}}\) & -25 to +85 & 0 to +70 & \({ }^{\circ} \mathrm{C}\) \\
\hline Operating Junction Temperature & \(\mathrm{T}_{\mathrm{J} \text { (max) }}\) & +150 & +150 & \({ }^{\circ} \mathrm{C}\) \\
\hline Storage Temperature Range & \(\mathrm{T}_{\text {stg }}\) & -65 to +150 & -65 to +150 & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS ( \(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\), unless otherwise noted) Note 1
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Characteristic} & \multirow[b]{2}{*}{Symbol} & \multicolumn{3}{|c|}{LM211} & \multicolumn{3}{|c|}{LM311} & \multirow[b]{2}{*}{Unit} \\
\hline & & Min & Typ & Max & Min & Typ & Max & \\
\hline \[
\begin{aligned}
& \text { Input Offset Voltage (Note 3) } \\
& R_{S} \leq 50 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& R_{S} \leq 50 \mathrm{k} \Omega, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*}
\end{aligned}
\] & \(\mathrm{V}_{10}\) & - & \[
0.7
\] & \[
\begin{aligned}
& 3.0 \\
& 4.0
\end{aligned}
\] & & & \[
\begin{gathered}
7.5 \\
10
\end{gathered}
\] & mV \\
\hline \[
\begin{aligned}
& \text { Input Offset Current (Note 3) } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*}
\end{aligned}
\] & 10 & - & \[
1.7
\] & \[
\begin{aligned}
& 10 \\
& 20
\end{aligned}
\] & - & \[
1.7
\] & \[
\begin{aligned}
& 50 \\
& 70
\end{aligned}
\] & nA \\
\hline \[
\begin{aligned}
& \text { Input Bias Current } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*}
\end{aligned}
\] & \(I_{\text {IB }}\) & - & \[
45
\] & \[
\begin{aligned}
& 100 \\
& 150
\end{aligned}
\] & - & & \[
\begin{aligned}
& 250 \\
& 300
\end{aligned}
\] & nA \\
\hline Voltage Gain & \(\mathrm{A}_{V}\) & 40 & 200 & - & 40 & 200 & - & V/mV \\
\hline Response Time (Note 4) & & - & 200 & - & - & 200 & - & ns \\
\hline Saturation Voltage
\[
\begin{aligned}
& \mathrm{V}_{I D} \leq-5.0 \mathrm{mV}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{I D} \leq-10 \mathrm{mV}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}} \geq 4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \\
& \mathrm{~V}_{I D}<\leq 6.0 \mathrm{mV}, \mathrm{I}_{\text {sink }} \leq 8.0 \mathrm{~mA} \\
& \mathrm{~V}_{\mathrm{ID}}<\leq 10 \mathrm{mV}, \mathrm{I}_{\text {sink }} \leq 8.0 \mathrm{~mA}
\end{aligned}
\] & \(\mathrm{V}_{\text {OL }}\) & - & \[
\begin{gathered}
0.75 \\
- \\
0.23
\end{gathered}
\] & \[
\begin{gathered}
1.5 \\
- \\
0.4
\end{gathered}
\] & - & \[
\begin{gathered}
- \\
0.75 \\
- \\
0.23
\end{gathered}
\] & \[
\begin{gathered}
- \\
1.5 \\
- \\
0.4
\end{gathered}
\] & V \\
\hline Strobe "On" Current (Note 5) & Is & - & 3.0 & - & - & 3.0 & - & mA \\
\hline \[
\begin{aligned}
& \text { Output Leakage Current } \\
& \mathrm{V}_{I D} \geq 5.0 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {strobe }}=3.0 \mathrm{~mA} \\
& \mathrm{~V}_{I D} \geq 10 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {strobe }}=3.0 \mathrm{~mA} \\
& \mathrm{~V}_{\text {ID }} \geq 5.0 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \\
& \hline
\end{aligned}
\] & & - & \[
\begin{gathered}
0.2 \\
- \\
0.1
\end{gathered}
\] & \[
\begin{gathered}
10 \\
- \\
0.5
\end{gathered}
\] & - & \[
-\overline{-}
\] & \[
\frac{-}{50}
\] & \[
\begin{aligned}
& \mathrm{nA} \\
& \mathrm{nA} \\
& \mu \mathrm{~A}
\end{aligned}
\] \\
\hline Input Voltage Range ( \(\mathrm{T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*}\) ) & VICR & -14.5 & \[
\begin{gathered}
-14.7 \\
\text { to } \\
13.8
\end{gathered}
\] & +13.0 & -14.5 & \[
\begin{gathered}
-14.7 \\
\text { to } \\
13.8
\end{gathered}
\] & +13.0 & V \\
\hline Positive Supply Current & Icc & - & +2.4 & +6.0 & - & +2.4 & +7.5 & mA \\
\hline Negative Supply Current & \(\mathrm{I}_{\text {EE }}\) & - & -1.3 & -5.0 & - & -1.3 & -5.0 & mA \\
\hline
\end{tabular}
*LM211: \(\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}\) LM311: \(T_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}\)
1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 V supply up to \(\pm 15 \mathrm{~V}\) supplies.
2. This rating applies for \(\pm 15 \mathrm{~V}\) supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 mA to 5.0 mA .

\section*{LM211, LM311}


Figure 2. Circuit Schematic


Figure 3. Input Bias Current versus Temperature


Figure 5. Input Bias Current versus Differential Input Voltage


Figure 4. Input Offset Current versus Temperature


Figure 6. Common Mode Limits versus Temperature


Figure 7. Response Time for Various Input Overdrives


Figure 9. Response Time for Various Input Overdrives


Figure 8. Response Time for Various Input Overdrives


Figure 10. Response Time for Various Input Overdrives


Figure 12. Output Saturation Voltage versus Output Current


Figure 13. Output Leakage Current versus Temperature


Figure 14. Power Supply Current versus Supply Voltage


Figure 15. Power Supply Current versus Temperature

\section*{APPLICATIONS INFORMATION}


Figure 16. Improved Method of Adding Hysteresis Without Applying Positive

Feedback to the Inputs


Figure 17. Conventional Technique for Adding Hysteresis

\section*{TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS}

When a high speed comparator such as the LM211 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with \(0.1 \mu \mathrm{~F}\) disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high \((1.0 \mathrm{k} \Omega\) to \(100 \mathrm{k} \Omega\) ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM211 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 16.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a \(0.01 \mu \mathrm{~F}\) capacitor ( C 1 ) between Pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 16. For the fastest response time, tie both balance pins to \(\mathrm{V}_{\mathrm{CC}}\).

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor ( C 2 ) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R 2 of the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = \(10 \mathrm{k} \Omega\), as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM211 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM211, and a \(0.01 \mu \mathrm{~F}\) capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM211.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 17, the feedback resistor of \(510 \mathrm{k} \Omega\) from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than \(100 \Omega\), such as \(50 \mathrm{k} \Omega\), it would not be practical to simply increase the value of the positive feedback resistor proportionally above \(510 \mathrm{k} \Omega\) to maintain the same amount of hysteresis.
When both inputs of the LM211 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM211 so that positive feedback would be disruptive, the circuit of Figure 16 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 mV to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz . The positive-feedback signal across the \(82 \Omega\) resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the \(5.0 \mathrm{k} \Omega\) pot and \(3.0 \mathrm{k} \Omega\) resistor as shown.

\section*{LM211, LM311}


Figure 18. Zero-Crossing Detector Driving CMOS Logic


Figure 19. Relay Driver with Strobe Capability

ORDERING INFORMATION
\begin{tabular}{|c|c|c|}
\hline Device & Package & Shipping \({ }^{\dagger}\) \\
\hline LM211D & SOIC-8 & \multirow{3}{*}{98 Units / Rail} \\
\hline LM211DR2 & SOIC-8 & \\
\hline LM211DR2G & \[
\begin{gathered}
\text { SOIC-8 } \\
\text { (Pb-Free) }
\end{gathered}
\] & \\
\hline LM311D & SOIC-8 & 2500 Units / Reel \\
\hline LM311DG & \[
\begin{gathered}
\hline \text { SOIC-8 } \\
\text { (Pb-Free) }
\end{gathered}
\] & 98 Units / Rail \\
\hline LM311DR2 & SOIC-8 & \multirow[b]{2}{*}{2500 Units / Reel} \\
\hline LM311DR2G & \[
\begin{gathered}
\text { SOIC-8 } \\
\text { (Pb-Free) }
\end{gathered}
\] & \\
\hline LM311N & PDIP-8 & \multirow[b]{2}{*}{50 Units / Rail} \\
\hline LM311NG & \[
\begin{gathered}
\hline \text { PDIP-8 } \\
\text { (Pb-Free) }
\end{gathered}
\] & \\
\hline
\end{tabular}
\(\dagger\) For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\section*{MARKING DIAGRAMS}

\(x \quad=2\) or 3
A = Assembly Location
WL, L = Wafer Lot
YY, \(Y=\) Year
WW, W = Work Week

\section*{LM211, LM311}

\section*{PACKAGE DIMENSIONS}

PDIP-8
N SUFFIX
CASE 626-05
ISSUE L


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)
3. DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982.
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{DIM} & MILLII & TERS & & \\
\hline & MIN & MAX & MIN & MAX \\
\hline A & 9.40 & 10.16 & 0.370 & 0.400 \\
\hline B & 6.10 & 6.60 & 0.240 & 0.260 \\
\hline C & 3.94 & 4.45 & 0.155 & 0.175 \\
\hline D & 0.38 & 0.51 & 0.015 & 0.020 \\
\hline F & 1.02 & 1.78 & 0.040 & 0.070 \\
\hline G & \multicolumn{2}{|l|}{2.54 BSC} & \multicolumn{2}{|l|}{0.100 BSC} \\
\hline H & 0.76 & 1.27 & 0.030 & 0.050 \\
\hline J & 0.20 & 0.30 & 0.008 & 0.012 \\
\hline K & 2.92 & 3.43 & 0.115 & 0.135 \\
\hline L & \multicolumn{2}{|l|}{7.62 BSC} & \multicolumn{2}{|l|}{0.300 BSC} \\
\hline M & --- & \(10^{\circ}\) & --- & \(10^{\circ}\) \\
\hline N & 0.76 & 1.01 & 0.030 & 0.040 \\
\hline
\end{tabular}

\section*{LM211, LM311}

SOIC-8
D SUFFIX
CASE 751-07
ISSUE AC


\section*{SOLDERING FOOTPRINT*}

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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\section*{MC78XX/LM78XX/MC78XXA 3-Terminal 1A Positive Voltage Regulator}

\section*{Features}
- Output Current up to 1 A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

\section*{Description}

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.


\section*{Internal Block Digram}


Rev. 1.0.1

\section*{Absolute Maximum Ratings}
\begin{tabular}{|l|c|c|c|}
\hline Parameter & Symbol & Value & Unit \\
\hline \begin{tabular}{l} 
Input Voltage (for \(\mathrm{VO}=5 \mathrm{~V}\) to 18 V ) \\
(for \(\mathrm{VO}=24 \mathrm{~V}\) )
\end{tabular} & \(\mathrm{VI}_{\mathrm{I}}\) & 35 & V \\
\hline Thermal Resistance Junction-Cases (TO-220) & \(\mathrm{V}_{\mathrm{I}}\) & 40 & V \\
\hline Thermal Resistance Junction-Air (TO-220) & \(\mathrm{R}_{\theta \mathrm{JC}}\) & 5 & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) \\
\hline Operating Temperature Range & \(\mathrm{R}_{\theta \mathrm{JA}}\) & 65 & \({ }^{\circ} \mathrm{C} / \mathrm{W}\) \\
\hline Storage Temperature Range & TOPR & \(0 \sim+125\) & \({ }^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics (MC7805/LM7805)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=10 \mathrm{~V}, \mathrm{CI}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{Conditions}} & \multicolumn{3}{|l|}{MC7805/LM7805} & \multirow[b]{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \(\mathrm{TJ}=+25^{\circ} \mathrm{C}\) & & 4.8 & 5.0 & 5.2 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{Io} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V}_{\mathrm{I}}=7 \mathrm{~V} \text { to } 20 \mathrm{~V}
\end{aligned}
\]} & 4.75 & 5.0 & 5.25 & \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VO}=7 \mathrm{~V}\) to 25 V & - & 4.0 & 100 & \multirow[b]{2}{*}{mV} \\
\hline & & & \(\mathrm{VI}=8 \mathrm{~V}\) to 12 V & - & 1.6 & 50 & \\
\hline \multirow[b]{2}{*}{Load Regulation (Note1)} & \multirow[b]{2}{*}{Regload} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{IO}=5.0 \mathrm{~mA}\) to 1.5 A & - & 9 & 100 & \multirow[b]{2}{*}{mV} \\
\hline & & & \[
\begin{aligned}
& \mathrm{IO}=250 \mathrm{~mA} \text { to } \\
& 750 \mathrm{~mA}
\end{aligned}
\] & - & 4 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.0 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow[b]{2}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0A} & - & 0.03 & 0.5 & \multirow[b]{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{V I \(=7 \mathrm{~V}\) to 25 V} & - & 0.3 & 1.3 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -0.8 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}^{\text {a }}+25^{\circ} \mathrm{C}\)} & - & 42 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz} \\
& \mathrm{VO}=8 \mathrm{~V} \text { to } 18 \mathrm{~V}
\end{aligned}
\]} & 62 & 73 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 15 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{V I \(=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 230 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T}_{\mathrm{J}=+25^{\circ} \mathrm{C}}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in \(\mathrm{V}_{\mathrm{o}}\) due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7806)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=11 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7806} & \multirow[b]{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & 5.75 & 6.0 & 6.25 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V}=8.0 \mathrm{~V} \text { to } 21 \mathrm{~V}
\end{aligned}
\]} & 5.7 & 6.0 & 6.3 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=8 \mathrm{~V}\) to 25 V & - & 5 & 120 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{VI}=9 \mathrm{~V}\) to 13 V & - & 1.5 & 60 & \\
\hline \multirow[b]{2}{*}{Load Regulation (Note1)} & \multirow[b]{2}{*}{Regload} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{IO}=5 \mathrm{~mA}\) to 1.5 A & - & 9 & 120 & \multirow[b]{2}{*}{mV} \\
\hline & & & \(\mathrm{IO}=250 \mathrm{~mA}\) to 750 A & - & 3 & 60 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 5.0 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow{2}{*}{\(\Delta \mathrm{l} Q\)} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1 A} & - & - & 0.5 & \multirow{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=8 \mathrm{~V}\) to 25 V} & - & - & 1.3 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -0.8 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 45 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz} \\
& \mathrm{VI}=9 \mathrm{~V} \text { to } 19 \mathrm{~V}
\end{aligned}
\]} & 59 & 75 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 19 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7808)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=14 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7808} & \multirow{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 7.7 & 8.0 & 8.3 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V}_{\mathrm{I}}=10.5 \mathrm{~V} \text { to } 23 \mathrm{~V}
\end{aligned}
\]} & 7.6 & 8.0 & 8.4 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=10.5 \mathrm{~V}\) to 25 V & - & 5.0 & 160 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{VI}=11.5 \mathrm{~V}\) to 17 V & - & 2.0 & 80 & \\
\hline \multirow[b]{2}{*}{Load Regulation (Note1)} & \multirow[b]{2}{*}{Regload} & \multirow[b]{2}{*}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & \(\mathrm{IO}=5.0 \mathrm{~mA}\) to 1.5 A & - & 10 & 160 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA & - & 5.0 & 80 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.0 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow[b]{2}{*}{\(\Delta \mathrm{l}\)} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 0.05 & 0.5 & \multirow[b]{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=10.5 \mathrm{~A}\) to 25 V} & - & 0.5 & 1.0 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -0.8 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & \(\mathrm{V} N\) & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 52 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\(\mathrm{f}=120 \mathrm{~Hz}, \mathrm{~V}\) I \(=11.5 \mathrm{~V}\) to 21.5 V} & 56 & 73 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 17 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 230 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7809)}
(Refer to test circuit \(, 0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=15 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7809} & \multirow[b]{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 8.65 & 9 & 9.35 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V}=11.5 \mathrm{~V} \text { to } 24 \mathrm{~V}
\end{aligned}
\]} & 8.6 & 9 & 9.4 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=11.5 \mathrm{~V}\) to 25 V & - & 6 & 180 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{V}=12 \mathrm{~V}\) to 17 V & - & 2 & 90 & \\
\hline \multirow{2}{*}{Load Regulation (Note1)} & \multirow{2}{*}{Regload} & \multirow{2}{*}{\(\mathrm{T}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{lO}=5 \mathrm{~mA}\) to 1.5A & - & 12 & 180 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA & - & 4 & 90 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{T}_{\mathrm{J}=+25^{\circ} \mathrm{C}}\)} & - & 5.0 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow{2}{*}{\(\Delta \mathrm{l} \mathrm{Q}\)} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0A} & - & - & 0.5 & \multirow{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=11.5 \mathrm{~V}\) to 26 V} & - & - & 1.3 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 58 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz} \\
& \mathrm{VI}=13 \mathrm{~V} \text { to } 23 \mathrm{~V}
\end{aligned}
\]} & 56 & 71 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 17 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7810)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=16 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7810} & \multirow[b]{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 9.6 & 10 & 10.4 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}_{\mathrm{I}}=12.5 \mathrm{~V} \text { to } 25 \mathrm{~V}
\end{aligned}
\]} & 9.5 & 10 & 10.5 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{V}=12.5 \mathrm{~V}\) to 25 V & - & 10 & 200 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{VI}=13 \mathrm{~V}\) to 25 V & - & 3 & 100 & \\
\hline \multirow[b]{2}{*}{Load Regulation (Note1)} & \multirow[b]{2}{*}{Regload} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{lO}=5 \mathrm{~mA}\) to 1.5 A & - & 12 & 200 & \multirow{2}{*}{mV} \\
\hline & & & \(1 \mathrm{O}=250 \mathrm{~mA}\) to 750 mA & - & 4 & 400 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 5.1 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow{2}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & - & 0.5 & \multirow{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=12.5 \mathrm{~V}\) to 29 V} & - & - & 1.0 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 58 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz} \\
& \mathrm{VI}=13 \mathrm{~V} \text { to } 23 \mathrm{~V}
\end{aligned}
\]} & 56 & 71 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 17 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7812)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{~V}=19 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7812} & \multirow[b]{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 11.5 & 12 & 12.5 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V} I=14.5 \mathrm{~V} \text { to } 27 \mathrm{~V}
\end{aligned}
\]} & 11.4 & 12 & 12.6 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=14.5 \mathrm{~V}\) to 30 V & - & 10 & 240 & \multirow{2}{*}{mV} \\
\hline & & & V I \(=16 \mathrm{~V}\) to 22 V & - & 3.0 & 120 & \\
\hline \multirow{2}{*}{Load Regulation (Note1)} & \multirow{2}{*}{Regload} & \multirow{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{IO}=5 \mathrm{~mA}\) to 1.5 A & - & 11 & 240 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA & - & 5.0 & 120 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 5.1 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow{2}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 0.1 & 0.5 & \multirow[t]{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=14.5 \mathrm{~V}\) to 30 V} & - & 0.5 & 1.0 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 76 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz} \\
& \mathrm{VI}=15 \mathrm{~V} \text { to } 25 \mathrm{~V}
\end{aligned}
\]} & 55 & 71 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 18 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & - & 230 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7815)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{VI}=23 \mathrm{~V}, \mathrm{CI}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{Parameter} & \multirow{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7815} & \multirow{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 14.4 & 15 & 15.6 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V}_{\mathrm{I}}=17.5 \mathrm{~V} \text { to } 30 \mathrm{~V}
\end{aligned}
\]} & 14.25 & 15 & 15.75 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=17.5 \mathrm{~V}\) to 30 V & - & 11 & 300 & \multirow{2}{*}{mV} \\
\hline & & & V = \(=20 \mathrm{~V}\) to 26 V & - & 3 & 150 & \\
\hline \multirow[b]{2}{*}{Load Regulation (Note1)} & \multirow[b]{2}{*}{Regload} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{IO}=5 \mathrm{~mA}\) to 1.5 A & - & 12 & 300 & \multirow[b]{2}{*}{mV} \\
\hline & & & \[
\begin{aligned}
& \mathrm{IO}=250 \mathrm{~mA} \text { to } \\
& 750 \mathrm{~mA}
\end{aligned}
\] & - & 4 & 150 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.2 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow{2}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0A} & - & - & 0.5 & \multirow{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{V I \(=17.5 \mathrm{~V}\) to 30 V} & - & - & 1.0 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & \(\mathrm{V}_{\mathrm{N}}\) & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & - & 90 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& f=120 \mathrm{~Hz} \\
& V_{I}=18.5 \mathrm{~V} \text { to } 28.5 \mathrm{~V}
\end{aligned}
\]} & 54 & 70 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 19 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{V I \(=35 \mathrm{~V}, \mathrm{~T}_{\text {A }}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7818)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{~V}=27 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7818} & \multirow[b]{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & 17.3 & 18 & 18.7 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V}=21 \mathrm{~V} \text { to } 33 \mathrm{~V}
\end{aligned}
\]} & 17.1 & 18 & 18.9 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=21 \mathrm{~V}\) to 33 V & - & 15 & 360 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{VI}=24 \mathrm{~V}\) to 30 V & - & 5 & 180 & \\
\hline \multirow[b]{2}{*}{Load Regulation (Note1)} & \multirow[b]{2}{*}{Regload} & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{lO}=5 \mathrm{~mA}\) to 1.5 A & - & 15 & 360 & \multirow[b]{2}{*}{mV} \\
\hline & & & \(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA & - & 5.0 & 180 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.2 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow{2}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{lO}=5 \mathrm{~mA}\) to 1.0A} & - & - & 0.5 & \multirow{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=21 \mathrm{~V}\) to 33 V} & - & - & 1 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & V N & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 110 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz} \\
& \mathrm{VI}=22 \mathrm{~V} \text { to } 32 \mathrm{~V}
\end{aligned}
\]} & 53 & 69 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 22 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{~T} A=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7824)}
(Refer to test circuit , \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{IO}=500 \mathrm{~mA}, \mathrm{~V}=33 \mathrm{~V}, \mathrm{C}=0.33 \mu \mathrm{~F}, \mathrm{CO}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{Parameter} & \multirow[b]{2}{*}{Symbol} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{Conditions}} & \multicolumn{3}{|c|}{MC7824} & \multirow[b]{2}{*}{Unit} \\
\hline & & & & Min. & Typ. & Max. & \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & 23 & 24 & 25 & \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& 5.0 \mathrm{~mA} \leq \mathrm{IO} \leq 1.0 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=27 \mathrm{~V} \text { to } 38 \mathrm{~V}
\end{aligned}
\]} & 22.8 & 24 & 25.25 & V \\
\hline \multirow[b]{2}{*}{Line Regulation (Note1)} & \multirow[b]{2}{*}{Regline} & \multirow[b]{2}{*}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=27 \mathrm{~V}\) to 38 V & - & 17 & 480 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{VI}=30 \mathrm{~V}\) to 36V & - & 6 & 240 & \\
\hline \multirow{2}{*}{Load Regulation (Note1)} & \multirow{2}{*}{Regload} & \multirow{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{lO}=5 \mathrm{~mA}\) to 1.5 A & - & 15 & 480 & \multirow{2}{*}{mV} \\
\hline & & & \(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA & - & 5.0 & 240 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 5.2 & 8.0 & mA \\
\hline \multirow[b]{2}{*}{Quiescent Current Change} & \multirow{2}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 0.1 & 0.5 & \multirow{2}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=27 \mathrm{~V}\) to 38 V} & - & 0.5 & 1 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{VO} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1.5 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\(\mathrm{f}=10 \mathrm{~Hz}\) to \(100 \mathrm{KHz}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 60 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz} \\
& \mathrm{VI}=28 \mathrm{~V} \text { to } 38 \mathrm{~V}
\end{aligned}
\]} & 50 & 67 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 28 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 230 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Changes in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7805A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=10 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \(\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}\) & & 4.9 & 5 & 5.1 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=7.5 \mathrm{~V} \text { to } 20 \mathrm{~V}
\end{aligned}
\]} & 4.8 & 5 & 5.2 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V} \mathrm{I}=7.5 \mathrm{~V} \text { to } 25 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 5 & 50 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=8 \mathrm{~V}\) to 12 V} & - & 3 & 50 & \\
\hline & & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{V}=7.3 \mathrm{~V}\) to 20V & - & 5 & 50 & \\
\hline & & & \(\mathrm{V}=8 \mathrm{~V}\) to 12 V & - & 1.5 & 25 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{lO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 9 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1 A} & - & 9 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 4 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}\)} & - & 5.0 & 6 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\(\Delta \mathrm{l}\)} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1 A} & - & - & 0.5 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{V I \(=8 \mathrm{~V}\) to \(25 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{I}}=7.5 \mathrm{~V}\) to \(20 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & - & 0.8 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{lo}=5 \mathrm{~mA}\)} & - & -0.8 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & V N & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}_{\mathrm{A}}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=8 \mathrm{~V} \text { to } 18 \mathrm{~V}
\end{aligned}
\]} & - & 68 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 17 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7806A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{~V} \mathrm{I}=11 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 5.58 & 6 & 6.12 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=8.6 \mathrm{~V} \text { to } 21 \mathrm{~V}
\end{aligned}
\]} & 5.76 & 6 & 6.24 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \hline \mathrm{V}=8.6 \mathrm{~V} \text { to } 25 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 5 & 60 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=9 \mathrm{~V}\) to 13 V} & - & 3 & 60 & \\
\hline & & \multirow[t]{2}{*}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & V I \(=8.3 \mathrm{~V}\) to 21V & - & 5 & 60 & \\
\hline & & & \(\mathrm{V}=9 \mathrm{~V}\) to 13 V & - & 1.5 & 30 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 9 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1 A} & - & 4 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 5.0 & 50 & \\
\hline Quiescent Current & IQ & \(\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}\) & & - & 4.3 & 6 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1 A} & - & - & 0.5 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=9 \mathrm{~V}\) to \(25 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=8.5 \mathrm{~V}\) to \(21 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & - & 0.8 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -0.8 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}_{\mathrm{A}}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=9 \mathrm{~V} \text { to } 19 \mathrm{~V}
\end{aligned}
\]} & - & 65 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 17 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7808A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{~V} \mathrm{I}=14 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \(\mathrm{TJ}=+25^{\circ} \mathrm{C}\) & & 7.84 & 8 & 8.16 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=10.6 \mathrm{~V} \text { to } 23 \mathrm{~V}
\end{aligned}
\]} & 7.7 & 8 & 8.3 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V}=10.6 \mathrm{~V} \text { to } 25 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 6 & 80 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{V I \(=11 \mathrm{~V}\) to 17 V} & - & 3 & 80 & \\
\hline & & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=10.4 \mathrm{~V}\) to 23 V & - & 6 & 80 & \\
\hline & & & V I \(=11 \mathrm{~V}\) to 17 V & - & 2 & 40 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 12 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1 A} & - & 12 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 5 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 5.0 & 6 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\({ }^{\Delta} \mathrm{Q}\)} & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1 A} & - & - & 0.5 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{I}}=11 \mathrm{~V}\) to 25V, \(\mathrm{IO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V} /=10.6 \mathrm{~V}\) to \(23 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & - & 0.8 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -0.8 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\[
\begin{aligned}
& f=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=11.5 \mathrm{~V} \text { to } 21.5 \mathrm{~V}
\end{aligned}
\]} & - & 62 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 18 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7809A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=15 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 8.82 & 9.0 & 9.18 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{~V}=11.2 \mathrm{~V} \text { to } 24 \mathrm{~V}
\end{aligned}
\]} & 8.65 & 9.0 & 9.35 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \hline \mathrm{V}=11.7 \mathrm{~V} \text { to } 25 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 6 & 90 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=12.5 \mathrm{~V}\) to 19 V} & - & 4 & 45 & \\
\hline & & \multirow[t]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{V}=11.5 \mathrm{~V}\) to 24 V & - & 6 & 90 & \\
\hline & & & \(\mathrm{V}=12.5 \mathrm{~V}\) to 19 V & - & 2 & 45 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.0 \mathrm{~A}
\end{aligned}
\]} & - & 12 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 12 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 5 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.0 & 6.0 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\(\Delta \mathrm{l}\)} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\mathrm{I}}=11.7 \mathrm{~V}\) to \(25 \mathrm{~V}, \mathrm{~T} \mathrm{~J}=+25^{\circ} \mathrm{C}\)} & - & - & 0.8 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=12 \mathrm{~V}\) to \(25 \mathrm{~V}, \mathrm{lO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & - & 0.5 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1.0 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & \(\mathrm{V}_{\mathrm{N}}\) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=12 \mathrm{~V} \text { to } 22 \mathrm{~V}
\end{aligned}
\]} & - & 62 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.0 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 17 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant, junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7810A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=16 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \(\mathrm{TJ}=+25^{\circ} \mathrm{C}\) & & 9.8 & 10 & 10.2 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=12.8 \mathrm{~V} \text { to } 25 \mathrm{~V}
\end{aligned}
\]} & 9.6 & 10 & 10.4 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \hline \mathrm{V}=12.8 \mathrm{~V} \text { to } 26 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 8 & 100 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=13 \mathrm{~V}\) to 20V} & - & 4 & 50 & \\
\hline & & \multirow[b]{2}{*}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=12.5 \mathrm{~V}\) to 25 V & - & 8 & 100 & \\
\hline & & & V I \(=13 \mathrm{~V}\) to 20V & - & 3 & 50 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 12 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 12 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 5 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.0 & 6.0 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{VI}=13 \mathrm{~V}\) to \(26 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & - & 0.5 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=12.8 \mathrm{~V}\) to 25 V , \(\mathrm{IO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & - & 0.5 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{lO}=5 \mathrm{~mA}\)} & - & -1.0 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & \(\mathrm{V} N\) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=14 \mathrm{~V} \text { to } 24 \mathrm{~V}
\end{aligned}
\]} & - & 62 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.0 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 17 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{VI}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25{ }^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7812A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=19 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \(\mathrm{TJ}=+25^{\circ} \mathrm{C}\) & & 11.75 & 12 & 12.25 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=14.8 \mathrm{~V} \text { to } 27 \mathrm{~V}
\end{aligned}
\]} & 11.5 & 12 & 12.5 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V} \mathrm{I}=14.8 \mathrm{~V} \text { to } 30 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 10 & 120 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{V I \(=16 \mathrm{~V}\) to 22V} & - & 4 & 120 & \\
\hline & & \multirow[t]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & V I \(=14.5 \mathrm{~V}\) to 27 V & - & 10 & 120 & \\
\hline & & & V I \(=16 \mathrm{~V}\) to 22 V & - & 3 & 60 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 12 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 12 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 5 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.1 & 6.0 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{VI}=15 \mathrm{~V}\) to \(30 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & & 0.8 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=14 \mathrm{~V}\) to \(27 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}\)} & - & & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & & 0.5 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{lO}=5 \mathrm{~mA}\)} & - & -1.0 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}_{\mathrm{A}}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=14 \mathrm{~V} \text { to } 24 \mathrm{~V}
\end{aligned}
\]} & - & 60 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.0 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 18 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{~T} A=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7815A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=23 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & 14.7 & 15 & 15.3 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=17.7 \mathrm{~V} \text { to } 30 \mathrm{~V}
\end{aligned}
\]} & 14.4 & 15 & 15.6 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V} \mathrm{I}=17.9 \mathrm{~V} \text { to } 30 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 10 & 150 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{V I \(=20 \mathrm{~V}\) to 26 V} & - & 5 & 150 & \\
\hline & & \multirow[t]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{V}=17.5 \mathrm{~V}\) to 30 V & - & 11 & 150 & \\
\hline & & & V I \(=20 \mathrm{~V}\) to 26 V & - & 3 & 75 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{lO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 12 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 12 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 5 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.2 & 6.0 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\({ }^{\text {d }} \mathrm{Q}\)} & \multicolumn{2}{|l|}{\(\mathrm{VI}=17.5 \mathrm{~V}\) to \(30 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & - & 0.8 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=17.5 \mathrm{~V}\) to \(30 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & - & 0.5 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{lO}=5 \mathrm{~mA}\)} & - & -1.0 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & VN & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=18.5 \mathrm{~V} \text { to } 28.5 \mathrm{~V}
\end{aligned}
\]} & - & 58 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.0 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 19 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{V}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7818A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=27 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \(\mathrm{TJ}=+25^{\circ} \mathrm{C}\) & & 17.64 & 18 & 18.36 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=21 \mathrm{~V} \text { to } 33 \mathrm{~V}
\end{aligned}
\]} & 17.3 & 18 & 18.7 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{V} \mathrm{I}=21 \mathrm{~V} \text { to } 33 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 15 & 180 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=21 \mathrm{~V}\) to 33V} & - & 5 & 180 & \\
\hline & & \multirow[b]{2}{*}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & \(\mathrm{V}=20.6 \mathrm{~V}\) to 33 V & - & 15 & 180 & \\
\hline & & & \(\mathrm{V}=24 \mathrm{~V}\) to 30V & - & 5 & 90 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 15 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 15 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 7 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25{ }^{\circ} \mathrm{C}\)} & - & 5.2 & 6.0 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\(\Delta \mathrm{l}\)} & \multicolumn{2}{|l|}{\(\mathrm{VI}=21 \mathrm{~V}\) to \(33 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & - & 0.8 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=21 \mathrm{~V}\) to 33 V , \(\mathrm{IO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & - & 0.5 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\)} & - & -1.0 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & V N & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=22 \mathrm{~V} \text { to } 32 \mathrm{~V}
\end{aligned}
\]} & - & 57 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.0 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 19 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{VI}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in Vo due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Electrical Characteristics (MC7824A)}
(Refer to the test circuits. \(0^{\circ} \mathrm{C}<\mathrm{TJ}<125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=1 \mathrm{~A}, \mathrm{VI}=33 \mathrm{~V}, \mathrm{C} \mathrm{I}=0.33 \mu \mathrm{~F}, \mathrm{C} \mathrm{O}=0.1 \mu \mathrm{~F}\), unless otherwise specified)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline Parameter & Symbol & \multicolumn{2}{|r|}{Conditions} & Min. & Typ. & Max. & Unit \\
\hline \multirow[b]{2}{*}{Output Voltage} & \multirow[b]{2}{*}{Vo} & \multicolumn{2}{|l|}{\(\mathrm{T} \mathrm{J}=+25^{\circ} \mathrm{C}\)} & 23.5 & 24 & 24.5 & \multirow[b]{2}{*}{V} \\
\hline & & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1 \mathrm{~A}, \mathrm{PO} \leq 15 \mathrm{~W} \\
& \mathrm{VI}=27.3 \mathrm{~V} \text { to } 38 \mathrm{~V}
\end{aligned}
\]} & 23 & 24 & 25 & \\
\hline \multirow{4}{*}{Line Regulation (Note1)} & \multirow{4}{*}{Regline} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{VI}=27 \mathrm{~V} \text { to } 38 \mathrm{~V} \\
& \mathrm{IO}=500 \mathrm{~mA}
\end{aligned}
\]} & - & 18 & 240 & \multirow{4}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{V}=21 \mathrm{~V}\) to 33V} & - & 6 & 240 & \\
\hline & & \multirow[b]{2}{*}{\(\mathrm{T} J=+25^{\circ} \mathrm{C}\)} & \(\mathrm{VI}=26.7 \mathrm{~V}\) to 38 V & - & 18 & 240 & \\
\hline & & & \(\mathrm{V}=30 \mathrm{~V}\) to 36V & - & 6 & 120 & \\
\hline \multirow[t]{3}{*}{Load Regulation (Note1)} & \multirow{3}{*}{Regload} & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{TJ}=+25^{\circ} \mathrm{C} \\
& \mathrm{IO}=5 \mathrm{~mA} \text { to } 1.5 \mathrm{~A}
\end{aligned}
\]} & - & 15 & 100 & \multirow{3}{*}{mV} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & 15 & 100 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=250 \mathrm{~mA}\) to 750 mA} & - & 7 & 50 & \\
\hline Quiescent Current & IQ & \multicolumn{2}{|l|}{\(\mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 5.2 & 6.0 & mA \\
\hline \multirow{3}{*}{Quiescent Current Change} & \multirow{3}{*}{\(\Delta \mathrm{l}\) Q} & \multicolumn{2}{|l|}{\(\mathrm{VI}=27.3 \mathrm{~V}\) to \(38 \mathrm{~V}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & - & 0.8 & \multirow{3}{*}{mA} \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{VI}=27.3 \mathrm{~V}\) to \(38 \mathrm{~V}, \mathrm{IO}=500 \mathrm{~mA}\)} & - & - & 0.8 & \\
\hline & & \multicolumn{2}{|l|}{\(\mathrm{IO}=5 \mathrm{~mA}\) to 1.0 A} & - & - & 0.5 & \\
\hline Output Voltage Drift & \(\Delta \mathrm{V} / \Delta \mathrm{T}\) & \multicolumn{2}{|l|}{\(\mathrm{lO}=5 \mathrm{~mA}\)} & - & -1.5 & - & \(\mathrm{mV} /{ }^{\circ} \mathrm{C}\) \\
\hline Output Noise Voltage & \(\mathrm{V} N\) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=10 \mathrm{~Hz} \text { to } 100 \mathrm{KHz} \\
& \mathrm{TA}=25^{\circ} \mathrm{C}
\end{aligned}
\]} & - & 10 & - & \(\mu \mathrm{V} / \mathrm{Vo}\) \\
\hline Ripple Rejection & RR & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{f}=120 \mathrm{~Hz}, \mathrm{IO}=500 \mathrm{~mA} \\
& \mathrm{VI}=28 \mathrm{~V} \text { to } 38 \mathrm{~V}
\end{aligned}
\]} & - & 54 & - & dB \\
\hline Dropout Voltage & VDrop & \multicolumn{2}{|l|}{\(\mathrm{IO}=1 \mathrm{~A}, \mathrm{TJ}=+25^{\circ} \mathrm{C}\)} & - & 2.0 & - & V \\
\hline Output Resistance & ro & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{KHz}\)} & - & 20 & - & \(\mathrm{m} \Omega\) \\
\hline Short Circuit Current & ISC & \multicolumn{2}{|l|}{\(\mathrm{VI}=35 \mathrm{~V}, \mathrm{TA}=+25^{\circ} \mathrm{C}\)} & - & 250 & - & mA \\
\hline Peak Current & IPK & \multicolumn{2}{|l|}{\(\mathrm{T} J=+25{ }^{\circ} \mathrm{C}\)} & - & 2.2 & - & A \\
\hline
\end{tabular}

\section*{Note:}
1. Load and line regulation are specified at constant junction temperature. Change in VO due to heating effects must be taken into account separately. Pulse testing with low duty is used.

\section*{Typical Perfomance Characteristics}


Figure 1. Quiescent Current


Figure 3. Output Voltage


Figure 2. Peak Output Current


Figure 4. Quiescent Current

\section*{Typical Applications}


Figure 5. DC Parameters


Figure 6. Load Regulation


Figure 7. Ripple Rejection


Figure 8. Fixed Output Regulator

\[
l_{0}=\frac{V x x}{R_{1}}+l_{0}
\]

Figure 9. Constant Current Regulator

\section*{Notes:}
(1) To specify an output voltage. substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.
(2) \(\mathrm{C}_{\boldsymbol{l}}\) is required if regulator is located an appreciable distance from power Supply filter.
(3) Co improves stability and transient response.

\[
\begin{gathered}
\mathrm{I}_{\mathrm{RI}} \geq 5 \mathrm{IQ} \\
\mathrm{VO}=\mathrm{VXX}_{\mathrm{XI}}\left(1+\mathrm{R}_{2} / \mathrm{R}_{1}\right)+\mathrm{I}_{\mathrm{QR}}^{2}
\end{gathered}
\]

Figure 10. Circuit for Increasing Output Voltage

\(\mathrm{IRI} \geq 5 \mathrm{lQ}\)
\(\mathrm{VO}_{\mathrm{O}}=\mathrm{VXX}_{\mathrm{X}}\left(1+\mathrm{R}_{2} / \mathrm{R}_{1}\right)+\mathrm{IQR}_{2}\)
Figure 11. Adjustable Output Regulator (7 to 30V)


Figure 12. High Current Voltage Regulator


Figure 13. High Output Current with Short Circuit Protection


Figure 14. Tracking Voltage Regulator


Figure 15. Split Power Supply ( \(\pm 15 \mathrm{~V}-1 \mathrm{~A}\) )


Figure 16. Negative Output Voltage Circuit


Figure 17. Switching Regulator

\section*{Mechanical Dimensions}

\section*{Package}


\section*{Mechancal Dimensions (Continued)}

\section*{Package}

\section*{D-PAK}


Ordering Information
\begin{tabular}{|c|c|c|c|}
\hline Product Number & Output Voltage Tolerance & Package & Operating Temperature \\
\hline LM7805CT & \(\pm 4 \%\) & TO-220 & \(0 \sim+125^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|}
\hline Product Number & Output Voltage Tolerance & Package & Operating Temperature \\
\hline MC7805CT & \multirow{15}{*}{\(\pm 4 \%\)} & \multirow{9}{*}{TO-220} & \multirow{24}{*}{\(0 \sim+125^{\circ} \mathrm{C}\)} \\
\hline MC7806CT & & & \\
\hline MC7808CT & & & \\
\hline MC7809CT & & & \\
\hline MC7810CT & & & \\
\hline MC7812CT & & & \\
\hline MC7815CT & & & \\
\hline MC7818CT & & & \\
\hline MC7824CT & & & \\
\hline MC7805CDT & & & \\
\hline MC7806CDT & & & \\
\hline MC7808CDT & & & \\
\hline MC7809CDT & & D-PAK & \\
\hline MC7810CDT & & & \\
\hline MC7812CDT & & & \\
\hline MC7805ACT & \multirow{9}{*}{\(\pm 2 \%\)} & \multirow{9}{*}{TO-220} & \\
\hline MC7806ACT & & & \\
\hline MC7808ACT & & & \\
\hline MC7809ACT & & & \\
\hline MC7810ACT & & & \\
\hline MC7812ACT & & & \\
\hline MC7815ACT & & & \\
\hline MC7818ACT & & & \\
\hline MC7824ACT & & & \\
\hline
\end{tabular}

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www.fairchildsemi.com
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

\section*{LM79XX Series \\ 3-Terminal Negative Regulators}

\section*{General Description}

The LM79XX series of 3-terminal regulators is available with fixed output voltages of \(-5 \mathrm{~V},-12 \mathrm{~V}\), and -15 V . These devices need only one external component-a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.
These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.
Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a
resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.
For applications requiring other voltages, see LM137 datasheet.

\section*{Features}
- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5 A output current
- \(4 \%\) tolerance on preset output voltage

\section*{Connection Diagrams}


Front View
Order Number LM7905CT, LM7912CT or LM7915CT See NS Package Number TO3B

\section*{Typical Applications}

*Required if regulator is separated from filter capacitor by more than \(3^{\prime \prime}\). For value given, capacitor must be solid tantalum. \(25 \mu \mathrm{~F}\) aluminum electrolytic may be substituted.
tRequired for stability. For value given, capacitor must be solid tantalum. \(25 \mu \mathrm{~F}\) aluminum electrolytic may be substituted. Values given may be increased without limit.
For output capacitance in excess of \(100 \mu \mathrm{~F}\), a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

\section*{Absolute Maximum Ratings (Note 1)}

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage
\(\begin{array}{ll}\left(\mathrm{V}_{\mathrm{o}}=-5 \mathrm{~V}\right) & -25 \mathrm{~V} \\ \left(\mathrm{~V}_{\mathrm{o}}=-12 \mathrm{~V} \text { and }-15 \mathrm{~V}\right) & -35 \mathrm{~V}\end{array}\)

Input-Output Differential
\[
\begin{array}{lr}
\qquad\left(\mathrm{V}_{\mathrm{o}}=-5 \mathrm{~V}\right) & 25 \mathrm{~V} \\
\left(\mathrm{~V}_{\mathrm{o}}=-12 \mathrm{~V} \text { and }-15 \mathrm{~V}\right) & 30 \mathrm{~V} \\
\text { Power Dissipation (Note 2) } & \text { Internally Limited } \\
\text { Operating Junction Temperature Range } & 0^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
\text { Storage Temperature Range } & -65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C} \\
\text { Lead Temperature (Soldering, 10 sec.) } & 230^{\circ} \mathrm{C}
\end{array}
\]

\section*{Electrical Characteristics}

Conditions unless otherwise noted: \(\mathrm{I}_{\text {OUT }}=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}\), Power Dissipation \(\leq 1.5 \mathrm{~W}\).


Electrical Characteristics
Conditions unless otherwise noted: \(\mathrm{I}_{\text {OUT }}=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}\), Power Dissipation \(\leq 1.5 \mathrm{~W}\).
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{Part Number} & LM7912C & LM7915C & \multirow[t]{4}{*}{Units} \\
\hline \multicolumn{3}{|c|}{Output Voltage} & -12V & -15V & \\
\hline & Input Voltage (un & erwise specified) & -19V & -23V & \\
\hline Symbol & Parameter & Conditions & Min \({ }^{\text {T }}\) Typ \({ }^{\text {a }}\) Max &  & \\
\hline \(\mathrm{V}^{\circ}\) & Output Voltage & \[
\begin{aligned}
& \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\
& 5 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 1 \mathrm{~A}, \\
& \mathrm{P} \leq 15 \mathrm{~W}
\end{aligned}
\] & \begin{tabular}{ccc}
-11.5 & -12.0 & -12.5 \\
-11.4 & & -12.6 \\
\(\left(-27 \leq \mathrm{V}_{\mathrm{IN}} \leq\right.\) & \(-14.5)\)
\end{tabular} & \begin{tabular}{ccc}
-14.4 & -15.0 & -15.6 \\
-14.25 & & -15.75 \\
\(\left(-30 \leq V_{\text {IN }} \leq\right.\) & \(-17.5)\)
\end{tabular} & \[
\begin{aligned}
& \mathrm{V} \\
& \mathrm{~V} \\
& \mathrm{~V}
\end{aligned}
\] \\
\hline \(\Delta \mathrm{V}_{\mathrm{O}}\) & Line Regulation & \(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\), (Note 3) & \[
\begin{array}{rr}
\hline 5 & 80 \\
\left(-30 \leq \mathrm{V}_{\mathrm{IN}} \leq-14.5\right) \\
3 & 30 \\
\left(-22 \leq \mathrm{V}_{\mathrm{IN}} \leq-16\right) \\
\hline
\end{array}
\] & \[
\begin{gathered}
5 \\
\left(-30 \leq \mathrm{V}_{\text {IN }} \leq\right. \\
3 \quad 100 \\
3 \\
\left(-26 \leq \mathrm{V}_{\mathrm{IN}} \leq-20\right) \\
\hline
\end{gathered}
\] & \[
\begin{gathered}
\mathrm{mV} \\
\mathrm{~V} \\
\mathrm{mV} \\
\mathrm{~V}
\end{gathered}
\] \\
\hline \(\Delta \mathrm{V}\) & Load Regulation & \(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\), (Note 3) & & & \\
\hline
\end{tabular}

Electrical Characteristics
(Continued)
Conditions unless otherwise noted: \(\mathrm{I}_{\mathrm{OUT}}=500 \mathrm{~mA}, \mathrm{C}_{\mathrm{IN}}=2.2 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}\), Power Dissipation \(\leq 1.5 \mathrm{~W}\).


Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee Specific Performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.
Note 2: Refer to Typical Performance Characteristics and Design Considerations for details.
Note 3: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

\section*{Design Considerations}

The LM79XX fixed voltage regulator series has thermal overload protection from excessive power dissipation, internal short circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.
Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature \(\left(125^{\circ} \mathrm{C}\right)\) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:
\begin{tabular}{|l|c|c|c|c|}
\hline \multirow{3}{*}{ Package } & \begin{tabular}{c} 
Typ \\
\(\theta_{\text {JC }}\) \\
\\
\\
\\
\\
\(\mathbf{C} / \mathbf{W}\)
\end{tabular} & \begin{tabular}{c} 
Max \\
\(\theta_{\text {JC }}\) \\
\({ }^{\circ} \mathbf{C} / \mathbf{W}\)
\end{tabular} & \begin{tabular}{c} 
Typ \\
\(\theta_{\text {JA }}\) \\
\({ }^{\circ} \mathbf{C} / \mathbf{W}\)
\end{tabular} & \begin{tabular}{c} 
Max \\
\(\theta_{\text {JA }}\) \\
\({ }^{\circ} \mathbf{C} / \mathbf{W}\)
\end{tabular} \\
\hline TO-220 & 3.0 & 5.0 & 60 & 40 \\
\hline
\end{tabular}
\[
\begin{aligned}
& P_{D M A X}=\frac{T_{J M a X}-T_{A}}{\theta_{J C}+\theta_{C A}} \text { or } \frac{T_{J M a x} T_{A}}{\theta_{J A}} \\
& \theta_{C A}=\theta_{C S}+\theta_{S A} \text { (without heat sink) }
\end{aligned}
\]

Solving for \(T_{J}\) :
\(T_{J}=T_{A}+P_{D}\left(\theta_{J C}+\theta_{C A}\right)\) or
\(=T_{A}+P_{D} \theta_{J A}\) (without heat sink)
Where:
\(\mathrm{T}_{\mathrm{J}}=\) Junction Temperature
\(\mathrm{T}_{\mathrm{A}}=\) Ambient Temperature
\(P_{D}=\) Power Dissipation
\(\theta_{\mathrm{JA}}=\) Junction-to-Ambient Thermal Resistance
\(\theta_{\mathrm{JC}}=\) Junction-to-Case Thermal Resistance
\(\theta_{\mathrm{CA}}=\) Case-to-Ambient Thermal Resistance
\(\theta_{\mathrm{CS}}=\) Case-to-Heat Sink Thermal Resistance
\(\theta_{\mathrm{SA}}=\) Heat Sink-to-Ambient Thermal Resistance

\section*{Typical Applications}

Bypass capacitors are necessary for stable operation of the LM79XX series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response by the regulator.
The bypass capacitors, \((2.2 \mu \mathrm{~F}\) on the input, \(1.0 \mu \mathrm{~F}\) on the output) should be ceramic or solid tantalum which have good
high frequency characteristics. If aluminum electrolytics are used, their values should be \(10 \mu \mathrm{~F}\) or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.


Load and line regulation \(<0.01 \%\) temperature stability \(\leq 0.2 \%\)
†Determine Zener current
\(\dagger \dagger\) Solid tantalum
*Select resistors to set output voltage. \(2 \mathrm{ppm} /{ }^{\circ} \mathrm{C}\) tracking suggested

\({ }^{*}\) IOUT \(=1 \mathrm{~mA}+\frac{5 \mathrm{~V}}{\mathrm{R}_{1}}\)

Typical Applications (Continued)

*Lamp brightness increase until \(\mathrm{i}_{\mathrm{I}}=\mathrm{i}_{\mathrm{Q}}(\approx 1 \mathrm{~mA})+5 \mathrm{~V} / \mathrm{R} 1\).
†Necessary only if raw supply filter capacitor is more that \(2^{\prime \prime}\) from LM7905CT

*Lamp brightness increases until \(\mathrm{i}_{\mathrm{i}}=5 \mathrm{~V} / \mathrm{R} 1\) ( \(\mathrm{l}_{\mathrm{i}}\) can be set as low as \(1 \mu \mathrm{~A}\) )
†Necessary only if raw supply filter capacitor is more that 2 " from LM7905

*Improves transient response and ripple rejection. Do not increase beyond \(50 \mu \mathrm{~F}\).
\(\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SET }}\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 2}\right)\)
Select R2 as follows:
LM7905CT \(300 \Omega\)
LM7912CT \(750 \Omega\)
LM7915CT 1k

Typical Applications (Continued)

\begin{tabular}{lll} 
& (-15) & \(\mathbf{( + 1 5 )}\) \\
Load Regulation at \(\Delta \mathrm{I}_{\mathrm{L}}=1 \mathrm{~A}\) & 40 mV & 2 mV \\
Output Ripple, \(\mathrm{C}_{\mathrm{IN}}=3000 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{L}}=1 \mathrm{~A}\) & \(100 \mu \mathrm{Vms}\) & \(100 \mu \mathrm{Vms}\) \\
Temperature Stability & 50 mV & 50 mV \\
Output Noise \(10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}\) & \(150 \mu \mathrm{Vms}\) & \(150 \mu \mathrm{Vms}\)
\end{tabular}
*Resistor tolerance of R4 and R5 determine matching of ( + ) and ( - ) outputs.
**Necessary only if raw supply filter capacitors are more than 3 " from regulators.

\section*{Dual Trimmed Supply}


Schematic Diagrams



Physical Dimensions inches (millimeters) unless othervise noted


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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
\begin{tabular}{|c|c|c|c|}
\hline \begin{tabular}{l}
National Semiconductor Corporation Americas \\
Email: support@nsc.com \\
www.national.com
\end{tabular} & \begin{tabular}{l}
National Semiconductor \\
Europe \\
Fax: +49 (0) 180-530 8586 \\
Email: europe.support@nsc.com \\
Deutsch Tel: +49 (0) 6995086208 \\
English Tel: +44 (0) 8702402171 \\
Français Tel: +33 (0) 141918790
\end{tabular} & \begin{tabular}{l}
National Semiconductor \\
Asia Pacific Customer \\
Response Group \\
Tel: 65-2544466 \\
Fax: 65-2504466 \\
Email: ap.suppor!@nsc.com
\end{tabular} & \begin{tabular}{l}
National Semiconductor Japan Ltd. \\
Tel: 81-3-5639-7560 \\
Fax: 81-3-5639-7507
\end{tabular} \\
\hline
\end{tabular}
- Meet or Exceed TIA/EIA-232-F and ITU Recommendation V. 28
- Operate With Single 5-V Power Supply
- Operate Up to 120 kbit/s
- Two Drivers and Two Receivers
- \(\pm 30\)-V Input Levels
- Low Supply Current . . . 8 mA Typical
- Designed to be Interchangeable With Maxim MAX232
- ESD Protection Exceeds JESD 22
- 2000-V Human-Body Model (A114-A)
- Applications

TIA/EIA-232-F
Battery-Powered Systems
Terminals
Modems
Computers

\section*{description/ordering information}

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V , and can accept \(\pm 30-\mathrm{V}\) inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASICTM library.

ORDERING INFORMATION
\begin{tabular}{|c|c|c|c|c|}
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|r|}{PACKAGE \(\dagger\)} & ORDERABLE PART NUMBER & TOP-SIDE MARKING \\
\hline \multirow{6}{*}{\(0^{\circ} \mathrm{C}\) to \(70^{\circ} \mathrm{C}\)} & PDIP (N) & Tube & MAX232N & MAX232N \\
\hline & \multirow[b]{2}{*}{SOIC (D)} & Tube & MAX232D & \multirow{2}{*}{MAX232} \\
\hline & & Tape and reel & MAX232DR & \\
\hline & \multirow{2}{*}{SOIC (DW)} & Tube & MAX232DW & \multirow{2}{*}{MAX232} \\
\hline & & Tape and reel & MAX232DWR & \\
\hline & SOP (NS) & Tape and reel & MAX232NSR & MAX232 \\
\hline \multirow{5}{*}{\(-40^{\circ} \mathrm{C}\) to \(85^{\circ} \mathrm{C}\)} & PDIP (N) & Tube & MAX232IN & MAX232IN \\
\hline & \multirow[b]{2}{*}{SOIC (D)} & Tube & MAX232ID & \multirow[b]{2}{*}{MAX2321} \\
\hline & & Tape and reel & MAX232IDR & \\
\hline & \multirow[b]{2}{*}{SOIC (DW)} & Tube & MAX232IDW & \multirow[b]{2}{*}{MAX2321} \\
\hline & & Tape and reel & MAX232IDWR & \\
\hline
\end{tabular}
\(\dagger\) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

\section*{Function Tables}
EACH DRIVER
\begin{tabular}{|c|c|}
\hline \begin{tabular}{c} 
INPUT \\
TIN
\end{tabular} & \begin{tabular}{c} 
OUTPUT \\
TOUT
\end{tabular} \\
\hline L & H \\
H & L \\
\hline
\end{tabular}
H = high level, \(\mathrm{L}=\) low
level

logic diagram (positive logic)


\section*{absolute maximum ratings over operating free-air temperature range (unless otherwise noted) \(\dagger\)}
\begin{tabular}{|c|c|}
\hline Input supply voltage range, \(\mathrm{V}_{\mathrm{CC}}\) (see Note 1) & -0.3 V to 6 V \\
\hline Positive output supply voltage range, \(\mathrm{V}_{\mathrm{S}_{+}}\) & \(\mathrm{V}_{\mathrm{CC}}-0.3 \mathrm{~V}\) to 15 V \\
\hline Negative output supply voltage range, \(\mathrm{V}_{\mathrm{S}}\) & -0.3 V to -15 V \\
\hline Input voltage range, \(\mathrm{V}_{\mathrm{l}}\) : Driver & -0.3 V to \(\mathrm{V}_{\mathrm{CC}}+0.3 \mathrm{~V}\) \\
\hline Receiver & \(\pm 30 \mathrm{~V}\) \\
\hline Output voltage range, \(\mathrm{V}_{\mathrm{O}}\) : T1OUT, T2OUT R1OUT, R2OUT & \[
\begin{aligned}
& \mathrm{V}_{\mathrm{S}_{-}-}-0.3 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{S}_{+}}+0.3 \mathrm{~V} \\
& \ldots . .0 .3 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{cc}}+0.3 \mathrm{~V}
\end{aligned}
\] \\
\hline Short-circuit duration: T1OUT, T2OUT & Unlimited \\
\hline Package thermal impedance, \(\theta_{\text {JA }}\) (see Note 2): D package & \(73^{\circ} \mathrm{C} / \mathrm{W}\) \\
\hline DW package & \(57^{\circ} \mathrm{C} / \mathrm{W}\) \\
\hline N package & \(67^{\circ} \mathrm{C} / \mathrm{W}\) \\
\hline NS package & \(64^{\circ} \mathrm{C} / \mathrm{W}\) \\
\hline Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds & \(260^{\circ} \mathrm{C}\) \\
\hline Storage temperature range, \(\mathrm{T}_{\text {stg }}\) & \(-65^{\circ} \mathrm{C}\) to \(150^{\circ} \mathrm{C}\) \\
\hline
\end{tabular}
\(\dagger\) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
recommended operating conditions
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline & & & MIN & NOM & MAX & UNIT \\
\hline \(\mathrm{V}_{\mathrm{CC}}\) & \multicolumn{2}{|l|}{Supply voltage} & 4.5 & 5 & 5.5 & V \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{High-level input voltage (T1IN,T2IN)} & 2 & & & V \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{Low-level input voltage (T1IN, T2IN)} & & & 0.8 & V \\
\hline R1IN, R2IN & \multicolumn{2}{|l|}{Receiver input voltage} & & & \(\pm 30\) & V \\
\hline \multirow[t]{2}{*}{\(\mathrm{T}_{\mathrm{A}}\)} & \multirow[t]{2}{*}{Operating free-air temperature} & MAX232 & 0 & & 70 & \multirow[t]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & MAX2321 & -40 & & 85 & \\
\hline
\end{tabular}
electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figure 4)
\begin{tabular}{|c|c|c|c|c|}
\hline & PARAMETER & TEST CONDITIONS & MIN & TYP \(\ddagger\) \\
\hline ICC MAX & UNIT \\
\hline Supply current & \begin{tabular}{l}
\(\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \quad\) All outputs open, \\
\(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\)
\end{tabular} & 8 & 10 & mA \\
\hline
\end{tabular}
\(\ddagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) and \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
NOTE 3: Test conditions are \(\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}\) at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}\).

\section*{DRIVER SECTION}
electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)
\begin{tabular}{|l|l|l|r|c|c|}
\hline \multicolumn{3}{|c|}{ PARAMETER } & \multicolumn{1}{|c|}{ TEST CONDITIONS } & MIN & TYP \(\dagger\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High-level output voltage & T1OUT, T2OUT & \(\mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega\) to GND & UNIT \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low-level output voltage \(\ddagger\) & \(\mathrm{T} 1 \mathrm{OUT}, \mathrm{T} 2 \mathrm{OUT}\) & \(\mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega\) to GND & 5 & 7 \\
\hline \(\mathrm{r}_{\mathrm{O}}\) & Output resistance & T1OUT, T2OUT & \(\mathrm{V}_{\mathrm{S}_{+}}=\mathrm{V}_{\mathrm{S}-}=0, \quad \mathrm{~V}_{\mathrm{O}}= \pm 2 \mathrm{~V}\) & 300 & -7 \\
\hline \(\mathrm{I}_{\mathrm{OS}} \S\) & Short-circuit output current & T1OUT, T2OUT & \(\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \quad \mathrm{~V}_{\mathrm{O}}=0\) & V & V \\
\hline \(\mathrm{I}_{\mathrm{IS}}\) & Short-circuit input current & \(\mathrm{T} 1 \mathrm{IN}, \mathrm{T} 2 \mathrm{IN}\) & \(\mathrm{V}_{\mathrm{I}}=0\) & & \(\pm 10\) \\
\hline
\end{tabular}
\(\dagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
\(\ddagger\) The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at a time.
NOTE 3: Test conditions are \(\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}\) at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}\).
switching characteristics, \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (see Note 3)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|r|}{PARAMETER} & TEST CONDITIONS & MIN & TYP & MAX & UNIT \\
\hline SR & Driver slew rate & \[
\mathrm{R}_{\mathrm{L}}=3 \mathrm{k} \Omega \text { to } 7 \mathrm{k} \Omega \text {, }
\] See Figure 2 & & & 30 & \(\mathrm{V} / \mu \mathrm{s}\) \\
\hline SR(t) & Driver transition region slew rate & See Figure 3 & & 3 & & \(\mathrm{V} / \mu \mathrm{s}\) \\
\hline & Data rate & One TOUT switching & & 120 & & kbit/s \\
\hline
\end{tabular}

NOTE 3: Test conditions are \(\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}\) at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}\).

\section*{RECEIVER SECTION}
electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{PARAMETER} & \multicolumn{2}{|r|}{TEST CONDITIONS} & MIN & TYP† & MAX & UNIT \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & High-level output voltage & R10UT, R2OUT & \(\mathrm{I}^{\mathrm{OH}}=-1 \mathrm{~mA}\) & & 3.5 & & & V \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & Low-level output voltage \(\ddagger\) & R1OUT, R2OUT & \(\mathrm{IOL}=3.2 \mathrm{~m}\) & & & & 0.4 & V \\
\hline \(\mathrm{V}_{\text {IT }}+\) & Receiver positive-going input threshold voltage & R1IN, R2IN & \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\), & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & & 1.7 & 2.4 & V \\
\hline VIT- & Receiver negative-going input threshold voltage & R1IN, R2IN & \(\mathrm{V}_{C C}=5 \mathrm{~V}\), & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & 0.8 & 1.2 & & V \\
\hline Vhys & Input hysteresis voltage & R1IN, R2IN & \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}\) & & 0.2 & 0.5 & 1 & V \\
\hline \(\mathrm{r}_{\mathrm{i}}\) & Receiver input resistance & R1IN, R2IN & \(\mathrm{V}_{\mathrm{CC}}=5\), & \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) & 3 & 5 & 7 & k \(\Omega\) \\
\hline
\end{tabular}
\(\dagger\) All typical values are at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\).
\(\ddagger\) The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
NOTE 3: Test conditions are \(\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}\) at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}\).
switching characteristics, \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) (see Note 3 and Figure 1)
\begin{tabular}{|cl|c|c|}
\hline & PARAMETER & TYP & UNIT \\
\hline \(\operatorname{tPLH}(\mathrm{R})\) & Receiver propagation delay time, low- to high-level output & 500 & ns \\
\hline \(\operatorname{tPHL}(\mathrm{R})\) & Receiver propagation delay time, high- to low-level output & 500 & ns \\
\hline
\end{tabular}

NOTE 3: Test conditions are \(\mathrm{C} 1-\mathrm{C} 4=1 \mu \mathrm{~F}\) at \(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 0.5 \mathrm{~V}\).

PARAMETER MEASUREMENT INFORMATION


NOTES: A. The pulse generator has the following characteristics: \(Z_{O}=50 \Omega\), duty cycle \(\leq 50 \%\).
B. \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.
C. All diodes are 1 N3064 or equivalent.

Figure 1. Receiver Test Circuit and Waveforms for \(\mathrm{t}_{\text {PHL }}\) and \(\mathrm{t}_{\text {PLH }}\) Measurements


NOTES: A. The pulse generator has the following characteristics: \(Z_{O}=50 \Omega\), duty cycle \(\leq 50 \%\).
B. \(\mathrm{C}_{\mathrm{L}}\) includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for \(\mathrm{t}_{\text {PHL }}\) and \(\mathrm{t}_{\text {PLH }}\) Measurements ( \(5-\mu \mathrm{s}\) Input)


TEST CIRCUIT


WAVEFORMS
NOTE A: The pulse generator has the following characteristics: \(Z_{O}=50 \Omega\), duty cycle \(\leq 50 \%\).
Figure 3. Test Circuit and Waveforms for \(\mathrm{t}_{\mathrm{THL}}\) and \(\mathrm{t}_{\mathrm{TLH}}\) Measurements ( \(20-\mu \mathrm{s}\) Input)

\section*{APPLICATION INFORMATION}


Figure 4. Typical Operating Circuit

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Mailing Address: \\ Texas Instruments \\ Post Office Box 655303 \\ Dallas, Texas 75265
}

This datasheet has been download from:
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Datasheets for electronics components.

\section*{General Description}

The MAX700／701／702 are supervisory circuits used to monitor the power supplies in \(\mu \mathrm{P}\) and digital systems．The RESET／RESET outputs of the MAX700／701／702 are guar－ anteed to be in the correct state for VCC voltages down to +1 V （Figure 4）．They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5 V powered circuits．
The MAX702 is the simplest part in the family．When VCC falls to 4.65 V ，RESET goes low．The MAX702 also pro－ vides a debounced manual reset input．The MAX701 performs the same functions but has both RESET and RESET outputs．Their primary function is to provide a system reset．Accordingly，an active reset signal is supplied for low supply voltages and for at least 200 ms after the supply voltage reaches its operating value．
In addition to the features of the MAX701 and MAX702， the MAX700 provides preset or adjustable voltage de－ tection so thresholds other than 4.65 V can be selected， and adjustable hysteresis．All parts are supplied in 8－pin Plastic DIP and Narrow SO packages in commercial and extended temperature ranges．

Applications
Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical \(\mu\) P Power Monitoring
－Min 200ms RESET Pulse on Power－Up， Power－Down，and During Low－Voltage Conditions
－Reset Threshold Factory Trimmed for +5 V Systems
－No External Components or Adjustments With +5 V Powered Circuits
－Debounced Manual Reset Input
－Preset or Adjustable Voltage Detection（MAX700）
－Adjustable Hysteresis（MAX700）
－8－Pin Plastic DIP and Narrow SO Packages
Ordering Information
\begin{tabular}{|lcl|}
\hline \multicolumn{1}{|c}{ PART } & TEMP．RANGE & PIN－PACKAGE \\
\hline MAX700CPA & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 8 Plastic DIP \\
\hline MAX700CSA & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 8 Narrow SO \\
\hline MAX700C／D & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & Dice \\
\hline MAX700EPA & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 8 Plastic DIP \\
\hline MAX700ESA & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 8 Narrow SO \\
\hline MAX701CPA & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 8 Plastic DIP \\
\hline MAX701CSA & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 8 Narrow SO \\
\hline MAX701C／D & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & Dice \\
\hline MAX701EPA & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 8 Plastic DIP \\
\hline MAX701ESA & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 8 Narrow SO \\
\hline MAX702CPA & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 8 Plastic DIP \\
\hline MAX702CSA & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 8 Narrow SO \\
\hline MAX702C／D & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & Dice \\
\hline MAX702EPA & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 8 Plastic DIP \\
\hline MAX702ESA & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 8 Narrow SO \\
\hline
\end{tabular}

Pin Configurations


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\section*{Power-Supply Monitor with Reset}

ABSOLUTE MAXIMUM RATINGS
VCC . . . ..................................... 3 V to +15.5 V
Voltage (with respect to GND) at RESET, RESET, HYST,
CTL, SENSE
Operating Temperature Range
MAX70_C
MAX70-E
-0.3 V to Vcc
\(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
\(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\)
\begin{tabular}{|c|c|}
\hline Rate of Rise & 100V/ \(/ \mathrm{s}\) \\
\hline Power Dissipation, any package & 380 mW \\
\hline Storage Temperature Range & \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\) \\
\hline Lead Temperature (Soldering, 10 sec .) & \(300^{\circ}\) \\
\hline
\end{tabular}

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability

\section*{ELECTRICAL CHARACTERISTICS}
\(\left(T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{CTL}=\mathrm{GND}\right.\) on MAX700, unless otherwise noted.)
\begin{tabular}{|c|c|c|c|c|c|}
\hline PARAMETER & CONDITIONS & MIN & TYP & MAX & UNITS \\
\hline VCC Monitor Voltage Range MAX700 Only & \[
\begin{aligned}
& \text { TA }_{A}=T_{\text {MIN to }} \text { TMAX } \\
& \text { CTL }=\text { VCC }
\end{aligned}
\] & 3 & & 15 & V \\
\hline Min VCC For Valid Reset Output, Declining Supply & \(\mathrm{T}_{A}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) \(\overline{\text { RESET }} \leq 0.4 \mathrm{~V}\) when sinking 1 mA & 1.5 & 1 & & V \\
\hline Supply Current & & & 100 & 200 & \(\mu \mathrm{A}\) \\
\hline Reset Threshold Power-up Power-down & \(T_{A}=T_{\text {MIN }}\) to \(T_{\text {MAX }}\) & \[
\begin{aligned}
& 4.5 \\
& 4.5
\end{aligned}
\] & \[
\begin{aligned}
& 4.65 \\
& 4.62
\end{aligned}
\] & \[
\begin{aligned}
& 4.75 \\
& 4.75
\end{aligned}
\] & V \\
\hline Internal Hysteresis & HYST not connected & & 30 & & mV \\
\hline Reset Output Pulse Width & & 200 & 350 & 500 & ms \\
\hline RESET Fall Time & MAX700/701 Only, CLOAD \(=100 \mathrm{pF}\) & & 200 & & ns \\
\hline VCC Pulse Duration Guaranteeing No Reset Reset & 5 V to 4V Vcc Pulse & 100 & \[
\begin{aligned}
& 10 \\
& 10
\end{aligned}
\] & 1 & \(\mu \mathrm{s}\) \\
\hline MR Input Threshold & & & 0.7 & & \(V\) \\
\hline MR Pullup Current & & & -5 & -30 & \(\mu \mathrm{A}\) \\
\hline MAX700 & & & & & \\
\hline \begin{tabular}{l}
RESET Output Low \\
RESET Output High
\end{tabular} & \[
\begin{aligned}
& \text { ISINK }=3.2 \mathrm{~mA}, V C C=5 \mathrm{~V} \\
& \text { ISINK }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\
& \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\
& \text { ISOURCE }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\
& \text { ISOURCE }=0.5 \mathrm{~mA}, V C C=1.5 \mathrm{~V}
\end{aligned}
\] & \begin{tabular}{l}
VCC-0. 4 \\
VCC-0. 4 \\
VCC-0. 4
\end{tabular} & & \[
\begin{aligned}
& 0.4 \\
& 0.4
\end{aligned}
\] & V \\
\hline \begin{tabular}{l}
RESET Output Low \\
\(\overline{\text { RESET Output High }}\)
\end{tabular} & \[
\begin{aligned}
& \text { ISINK }=16 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\
& \text { ISINK }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\
& \text { ISINK }=0.4 \mathrm{~mA}, V C C=1.5 \mathrm{~V} \\
& \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=5 \mathrm{~V} \\
& \text { ISOURCE }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V}
\end{aligned}
\] & \begin{tabular}{l}
Vcc-0.4 \\
VCC-0.4
\end{tabular} & & \[
\begin{aligned}
& 0.4 \\
& 0.4 \\
& 0.4
\end{aligned}
\] & V \\
\hline MAX701 & & & & & \\
\hline RESET Output Low RESET Output High & \[
\begin{aligned}
& I \text { SINK }=16 \mathrm{~mA}, V C C=5 \mathrm{~V} \\
& \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\
& \text { ISOURCE }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\
& \text { ISOURCE }=0.5 \mathrm{~mA}, V C C=1.5 \mathrm{~V}
\end{aligned}
\] & \begin{tabular}{l}
\(\mathrm{V}_{\mathrm{CC}}-0.4\) \\
\(V_{C C}-0.4\) \\
VCC-0.4
\end{tabular} & & 0.4 & V \\
\hline \begin{tabular}{l}
RESET Output Low \\
RESET Output High
\end{tabular} & \begin{tabular}{l}
ISINK \(=3.2 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=4.25 \mathrm{~V}\) \\
ISINK \(=1.6 \mathrm{~mA}, V_{C C}=3 \mathrm{~V}\) \\
ISINK \(=0.4 \mathrm{~mA}, V_{C C}=1.5 \mathrm{~V}\) \\
ISOURCE \(=3.2 \mathrm{~mA}, \mathrm{VCC}=5 \mathrm{~V}\)
\end{tabular} & Vcc-0.4 & & \[
\begin{aligned}
& 0.4 \\
& 0.4 \\
& 0.4
\end{aligned}
\] & V \\
\hline
\end{tabular}
\(\qquad\)

\title{
Power－Supply Monitor with Reset
}

\section*{ELECTRICAL CHARACTERISTICS（continued）}
\(\left(T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V}, \mathrm{CTL}=\mathrm{GND}\right.\) on MAX700，unless otherwise noted．）
\begin{tabular}{|c|c|c|c|c|c|}
\hline PARAMETER & CONDITIONS & MIN & TYP & MAX & UNITS \\
\hline \multicolumn{6}{|l|}{MAX702} \\
\hline \begin{tabular}{l}
RESET Output Low \\
RESET Output High
\end{tabular} & \[
\begin{aligned}
& \text { ISINK }=3.2 \mathrm{~mA}, V C C=4.25 \mathrm{~V} \\
& \text { ISINK }=1.6 \mathrm{~mA}, V C C=3 \mathrm{~V} \\
& \text { ISINK }=0.4 \mathrm{~mA}, V C C=1.5 \mathrm{~V} \\
& \text { ISOURCE }=3.2 \mathrm{~mA}, V C C=5 \mathrm{~V}
\end{aligned}
\] & Vcc－0．4 & & \[
\begin{aligned}
& 0.4 \\
& 0.4 \\
& 0.4
\end{aligned}
\] & V \\
\hline \multicolumn{6}{|l|}{MAX700 ONLY（CTL＝Vcc，unless otherwise noted．）} \\
\hline SENSE Input Threshold & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {min }}\) to \(\mathrm{Tmax}^{\text {ma }}\) & 1.25 & 1.29 & 1.35 & \(V\) \\
\hline SENSE Input Current & & & 0.1 & & nA \\
\hline HYST Input On Resistance & & & 0.5 & & k \(\Omega\) \\
\hline CTL Input Threshold & & & 2 & & \(\checkmark\) \\
\hline CTL Pulldown Current & & & 30 & 100 & \(\mu \mathrm{A}\) \\
\hline
\end{tabular}

Pin Description
\begin{tabular}{|c|c|}
\hline NAME & FUNCTION \\
\hline VCC & Chip power and +5 V sensing input（when CTL ＝GND on MAX700） \\
\hline GND & Ground \\
\hline RESET & Goes low when VCC falls below 4.65 V ，or when \(C T L=V C C\) on the MAX700 goes low when SENSE falls below 1.9 V ． \\
\hline RESET & MAX700， 701 only－Inverted Version of \(\overline{\text { RESET }}\) ． \\
\hline MR & Input for manual push button reset．Has inter－ nal \(5 \mu \mathrm{~A}\) pull up．Low input activates the RESET／RESET outputs． \\
\hline CTL & MAX700 only－When CTL＝GND．VCC is moni－ tored by the reset circuit．When CTL \(=\mathrm{VCC}_{C}, ~ \mathrm{VCC}\) is ignored and SENSE is monitored，allowing the threshold to be set with external resistors． \\
\hline HYST & MAX700 only－Normally NOT used when volt－ age is monitored through VCC（CTL＝GND）． When monitoring through SENSE（CTL＝VCC）， HYST allows hysteresis to be added，reducing noise and spurious reset activity（Figure 3）．HYST turns on \(5 \mu\) s before the RESET／RESET outputs are activated，and its on resistance to GND is typi－ cally \(1 \mathrm{k} \Omega\) ． \\
\hline SENSE & MAX700 only－The voltage sense input when \(C T L=V C C\) ．Its threshold is 1.29 V ．Sense al－ ways remains connected to the internal compa－ rator．So，when VCC is being monitored internally（CTL＝GND），SENSE should be left open circuit． \\
\hline
\end{tabular}

\section*{Power－Supply Monitor with Reset}


Figure 1．MAX700 Block Diagram


Figure 3．MAX700 Connected for External Sense and Hysteresis


Figure 2．MAX700 Typical Connection Diagram


Figure 4．Typical MAX700／701／702 \(\overline{\text { RESET }}\) Output vs．VCC

Figure 4 shows the \(\overline{\operatorname{RE} \overline{S E T}}\) output of the MAX700／701／702 in the correct state for VCC voltages down to OV．Note the effect of the built－in hysteresis on the trigger level of RESET．

\section*{Low-Power, 16-Bit Analog-to-Digital Converters with Parallel Interface}

\begin{abstract}
General Description
\end{abstract}

The MAX1165/MAX1166 16-bit, low-power, successiveapproximation analog-to-digital converters (ADCs) feature automatic power-down, factory-trimmed internal clock, and a 16-bit wide (MAX1165) or byte wide (MAX1166) parallel interface. The devices operate from a single +4.75 V to +5.25 V analog supply and \(\mathrm{a}+2.7 \mathrm{~V}\) to +5.25 V digital supply.
The MAX1165/MAX1166 use an internal 4.096V reference or an external reference. The MAX1165/MAX1166 consume only 1.8 mA at a sampling rate of 165 ksps with external reference and 2.7 mA with internal reference. AutoShutdown \({ }^{\top 1}\) reduces supply current to 0.1 mA at 10ksps.
The MAX1165/MAX1166 are ideal for high-performance, battery-powered, data-acquisition applications. Excellent dynamic performance and low power consumption in a small package make the MAX1165/ MAX1166 ideal for circuits with demanding power consumption and space requirements.
The 16 -bit wide MAX1165 is available in a 28 -pin TSSOP package and the byte wide MAX1166 is available in a 20-pin TSSOP package. Both devices are available in either the \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) commercial, or the \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) extended temperature range.

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

\section*{Applications}

Temperature Sensor/Monitor Industrial Process Control
I/O Boards
Data-Acquisition Systems
Cable/Harness Tester
Accelerometer Measurements
Digital Signal Processing

Pin Configurations appear at end of data sheet. Functional Diagram appears at end of data sheet.

Features
- 16-Bit Wide (MAX1165) and Byte Wide (MAX1166) Parallel Interface
- High Speed: 165ksps Sample Rate
- Accurate: \(\pm 2\) LSB INL, 16 Bit No Missing Codes
- 4.096V, 35ppm/ \({ }^{\circ} \mathrm{C}\) Internal Reference
- External Reference Range: +3.8V to +5.25V
- Single +4.75V to +5.25V Analog Supply Voltage
- +2.7V to +5.25V Digital Supply Voltage
- Low Supply Current
1.8mA (External Reference)
2.7mA (Internal Reference)
\(0.1 \mu \mathrm{~A}\) (10ksps, External Reference)
- Small Footprint

28-Pin TSSOP Package (16-Bit Wide)
20-Pin TSSOP Package (Byte Wide)
Ordering Information
\begin{tabular}{|lrlc|}
\hline \multicolumn{1}{|c}{ PART } & TEMP RANGE & PIN-PACKAGE & INL \\
\hline MAX1165ACUI & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 28 TSSOP & \(\pm 2\) \\
\hline MAX1165BCUI & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 28 TSSOP & \(\pm 2\) \\
\hline MAX1165CCUI & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 28 TSSOP & \(\pm 4\) \\
\hline MAX1165AEUI* & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 28 TSSOP & \(\pm 2\) \\
\hline MAX1165BEUI & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 28 TSSOP & \(\pm 2\) \\
\hline MAX1165CEUI \({ }^{\star}\) & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 28 TSSOP & \(\pm 4\) \\
\hline
\end{tabular}
*Future product-contact factory for availability.

Ordering Information continued at end of data sheet.
Typical Operating Circuit


\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}

\section*{ABSOLUTE MAXIMUM RATINGS}
\begin{tabular}{|c|c|}
\hline AVDD to AGND & -0.3V to +6V \\
\hline DV \({ }_{\text {D }}\) to DGND & 0.3V to ( \(\mathrm{AV}_{\text {DD }}+0.3 \mathrm{~V}\) ) \\
\hline AGND to DGND. & -0.3V to +0.3V \\
\hline AIN, REF, REFADJ to AGND & .-0.3V to ( \(\mathrm{AV} \mathrm{V}_{\text {D }}+0.3 \mathrm{~V}\) ) \\
\hline \(\overline{\mathrm{CS}}, \mathrm{HBEN}, \mathrm{R} / \overline{\mathrm{C}}, \mathrm{RESET}\) to DGND & -0.3V to +6V \\
\hline Digital Output (D15-D0, \(\overline{\mathrm{EOC}}\) ) to DGND & .-0.3V to (DVDD +0.3 V ) \\
\hline Maximum Continuous Current & . 50 mA \\
\hline
\end{tabular}

Continuous Power Dissipation ( \(\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}\) )
20-Pin TSSOP (derate \(10.9 \mathrm{~mW} /{ }^{\circ} \mathrm{C}\) above \(+70^{\circ} \mathrm{C}\) ) ........ 879 mW 28-Pin TSSOP (derate \(12.8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}\) above \(+70^{\circ} \mathrm{C}\) ) ..... 1026 mW Operating Temperature Ranges
MAX116_ _CU_ _................................................................ \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\)
MAX116_ EU_

Storage Temperature Range ............................. \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
Junction Temperature ...................................................... \(150^{\circ} \mathrm{C}\)
Lead Temperature (soldering, 10s) ................................. \(300^{\circ} \mathrm{C}\)
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\section*{ELECTRICAL CHARACTERISTICS}
( \(A V_{D D}=D_{D D}=+5 \mathrm{~V}\), external reference \(=+4.096 \mathrm{~V}, C_{R E F}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\text {REFADJ }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\) to \(\mathrm{T}_{\mathrm{MAX}}\), unless otherwise noted. Typical values are at \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\).)


\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}

\section*{ELECTRICAL CHARACTERISTICS (continued)}
\(\left(A V_{D D}=D V_{D D}=+5 V\right.\), external reference \(=+4.096 \mathrm{~V}, C_{R E F}=4.7 \mu F, C_{R E F A D J}=0.1 \mu F, T_{A}=T_{M I N}\) to \(T_{M A X}\), unless otherwise noted. Typical values are at \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\).)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline PARAMETER & SYMBOL & \multicolumn{2}{|c|}{CONDITIONS} & MIN & TYP & MAX & UNITS \\
\hline \multicolumn{8}{|l|}{INTERNAL REFERENCE} \\
\hline REF Output Voltage & VREF & & & 4.056 & 4.096 & 4.136 & V \\
\hline REF Output Tempco & TCREF & & & & \(\pm 25\) & & ppm \(/{ }^{\circ} \mathrm{C}\) \\
\hline REF Short-Circuit Current & IREFSC & & & & \(\pm 10\) & & mA \\
\hline Capacitive Bypass at REFADJ & Crefadj & & & 0.1 & & & \(\mu \mathrm{F}\) \\
\hline Capacitive Bypass at REF & CreF & & & 1 & & & \(\mu \mathrm{F}\) \\
\hline REFADJ Input Leakage Current & IREFADJ & & & & 20 & & \(\mu \mathrm{A}\) \\
\hline \multicolumn{8}{|l|}{EXTERNAL REFERENCE} \\
\hline REFADJ Buffer Disable Threshold & & \multicolumn{2}{|l|}{To power down the internal reference} & \[
\begin{gathered}
\text { AVDD } \\
0.4
\end{gathered}
\] & & \[
\begin{gathered}
A V_{D D}- \\
0.1
\end{gathered}
\] & V \\
\hline REF Input Voltage Range & & \multicolumn{2}{|l|}{Internal reference disabled} & 3.8 & & AVDD & V \\
\hline \multirow[b]{2}{*}{REF Input Current} & \multirow[b]{2}{*}{IREF} & \multicolumn{2}{|l|}{\(\mathrm{V}_{\text {REF }}=+4.096 \mathrm{~V}\), fSAMPLE \(=165 \mathrm{ksps}\)} & & 50 & 120 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & \multicolumn{2}{|l|}{Shutdown mode} & \multicolumn{3}{|c|}{\(\pm 0.1\)} & \\
\hline \multicolumn{8}{|l|}{DIGITAL INPUTS/OUTPUTS} \\
\hline Input High Voltage & \(\mathrm{V}_{\mathrm{IH}}\) & & & \[
\begin{gathered}
0.7 \times \\
D V_{D D}
\end{gathered}
\] & & & V \\
\hline Input Low Voltage & VIL & & & & & \[
\begin{aligned}
& 0.3 \times \\
& D V_{D D}
\end{aligned}
\] & V \\
\hline Input Leakage Current & IIN & \(\mathrm{V}_{\mathrm{IH}}=0\) or \(\mathrm{V}_{\text {DD }}\) & & & \(\pm 0.1\) & \(\pm 1\) & \(\mu \mathrm{A}\) \\
\hline Input Hysteresis & \(\mathrm{V}_{\text {HYST }}\) & & & & 0.1 & & V \\
\hline Input Capacitance & CIN & & & & 15 & & pF \\
\hline Output High Voltage & VOH & \[
\begin{aligned}
& \text { ISOURCE }=0.5 \mathrm{~mA}, \\
& \mathrm{AV}_{\mathrm{DD}}=+5.25 \mathrm{~V}
\end{aligned}
\] & \[
\mathrm{o}+5.25 \mathrm{~V}
\] & \[
\begin{gathered}
\text { DVDD - } \\
0.4
\end{gathered}
\] & & & V \\
\hline Output Low Voltage & Vol & \[
\begin{aligned}
& I_{S I N K}=1.6 \mathrm{~mA}, D V_{I} \\
& A V_{D D}=+5.25 \mathrm{~V}
\end{aligned}
\] & \[
5.25 \mathrm{~V},
\] & & & 0.4 & V \\
\hline Three-State Leakage Current & IOZ & D0-D15 & & & \(\pm 0.1\) & \(\pm 10\) & \(\mu \mathrm{A}\) \\
\hline Three-State Output Capacitance & Coz & & & & 15 & & pF \\
\hline \multicolumn{8}{|l|}{POWER REQUIREMENTS} \\
\hline Analog Supply Voltage & AVDD & & & 4.75 & & 5.25 & V \\
\hline Digital Supply & DVDD & & & 2.7 & & AVDD & V \\
\hline \multirow{8}{*}{Analog Supply Current} & \multirow{8}{*}{IAVDD} & \multirow{4}{*}{Internal reference} & 165ksps & & 2.7 & 3.2 & \multirow{8}{*}{mA} \\
\hline & & & 100ksps & & 2.0 & & \\
\hline & & & 10ksps & & 1.0 & & \\
\hline & & & 1ksps & & 1.0 & & \\
\hline & & \multirow{4}{*}{External reference} & 165ksps & & 1.8 & 2.3 & \\
\hline & & & 100ksps & & 1.1 & & \\
\hline & & & 10ksps & & 0.1 & & \\
\hline & & & 1ksps & & 0.01 & & \\
\hline
\end{tabular}

\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}

\section*{ELECTRICAL CHARACTERISTICS (continued)}
\(\left(A V_{D D}=D_{D D}=+5 V\right.\), external reference \(=+4.096 \mathrm{~V}, C_{R E F}=4.7 \mu F, C_{R E F A D J}=0.1 \mu F, T_{A}=T_{\text {MIN }}\) to \(T_{M A X}\), unless otherwise noted. Typical values are at \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\).)
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline PARAMETER & SYMBOL & \multicolumn{2}{|l|}{CONDITIONS} & MIN TYP & MAX & UNITS \\
\hline \multirow{4}{*}{Digital Supply Current} & \multirow{4}{*}{IDVDD} & \multirow{4}{*}{D0-D15 = all zeros} & 165ksps & 0.5 & 0.7 & \multirow{4}{*}{mA} \\
\hline & & & 100ksps & 0.3 & & \\
\hline & & & 10ksps & 0.03 & & \\
\hline & & & 1ksps & 0.003 & & \\
\hline \multirow{4}{*}{Shutdown Supply Current} & \multirow{4}{*}{ISHDN} & \multirow[b]{2}{*}{Full power-down} & IAVDD & 0.5 & 5 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & IDVDD & 0.5 & 5 & \\
\hline & & \multirow[b]{2}{*}{REF and REF buffer enabled (standby mode)} & IAVDD & 1.0 & 1.2 & mA \\
\hline & & & \begin{tabular}{l}
IDVDD \\
(Note 3)
\end{tabular} & 0.5 & 5 & \(\mu \mathrm{A}\) \\
\hline Power-Supply Rejection Ratio & PSRR & \multicolumn{2}{|l|}{\(\mathrm{AV} \mathrm{V}_{\mathrm{DD}}=+5 \mathrm{~V} \pm 5 \%\), full-scale input (Note 4)} & \multicolumn{2}{|l|}{68} & dB \\
\hline
\end{tabular}

\section*{TIMING CHARACTERISTICS (Figures 1 and 2)}
\(\left(\mathrm{AV}_{\mathrm{DD}}=+4.75 \mathrm{~V}\right.\) to \(+5.25 \mathrm{~V}, \mathrm{DV}\) DD \(=+2.7 \mathrm{~V}\) to \(\mathrm{AV}_{\mathrm{DD}}\), external reference \(=+4.096 \mathrm{~V}, \mathrm{CREF}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REFAD}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{LOAD}}=20 \mathrm{pF}\), \(T_{A}=T_{\text {MIN }}\) to \(T_{M A X}\), unless otherwise noted. Typical values are at \(T_{A}=+25^{\circ} \mathrm{C}\).)
\begin{tabular}{|c|c|c|c|c|c|}
\hline PARAMETER & SYMBOL & CONDITIONS & MIN & TYP MAX & UNITS \\
\hline Acquisition Time & tacQ & & 1.1 & & \multirow[b]{2}{*}{\(\mu \mathrm{s}\)} \\
\hline Conversion Time & tconv & & & 4.7 & \\
\hline \(\overline{\mathrm{CS}}\) Pulse Width High & tCSH & (Note 5) & 40 & & ns \\
\hline \multirow[b]{2}{*}{\(\overline{\mathrm{CS}}\) Pulse Width Low (Note 5)} & \multirow[b]{2}{*}{tCSL} & \(\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}\) to 5.25 V & 40 & & \multirow[b]{2}{*}{ns} \\
\hline & & V \({ }_{\text {DVDD }}=2.7 \mathrm{~V}\) to 5.25 V & 60 & & \\
\hline  & tDS & & 0 & & ns \\
\hline \multirow{2}{*}{\(\mathrm{R} / \overline{\mathrm{C}}\) to \(\overline{\mathrm{CS}}\) Fall Hold Time} & \multirow[b]{2}{*}{tD} & \(\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}\) to 5.25 V & 40 & & \multirow{2}{*}{ns} \\
\hline & & V \({ }_{\text {DVDD }}=2.7 \mathrm{~V}\) to 5.25 V & 60 & & \\
\hline \multirow[t]{2}{*}{\(\overline{\mathrm{CS}}\) to Output Data Valid} & \multirow[b]{2}{*}{tDO} & \(\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}\) to 5.25 V & & 40 & \multirow[t]{2}{*}{ns} \\
\hline & & \(\mathrm{V}_{\text {DVDD }}=2.7 \mathrm{~V}\) to 5.25 V & & 80 & \\
\hline \multirow[t]{2}{*}{HBEN Transition to Output Data Valid (MAX1166 Only)} & \multirow[b]{2}{*}{tDO1} & \(\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}\) to 5.25 V & & 40 & \multirow[t]{2}{*}{ns} \\
\hline & & V \({ }_{\text {DVDD }}=2.7 \mathrm{~V}\) to 5.25 V & & 80 & \\
\hline \(\overline{\text { EOC }}\) Fall to \(\overline{\mathrm{CS}}\) Fall & tDV & & 0 & & ns \\
\hline \multirow[t]{2}{*}{\(\overline{\mathrm{CS}}\) Rise to \(\overline{\mathrm{EOC}}\) Rise} & \multirow[b]{2}{*}{teoc} & V \({ }_{\text {DVDD }}=4.75 \mathrm{~V}\) to 5.25 V & & 40 & \multirow[t]{2}{*}{ns} \\
\hline & & \(\mathrm{V}_{\text {DVDD }}=2.7 \mathrm{~V}\) to 5.25 V & & 80 & \\
\hline \multirow[b]{2}{*}{Bus Relinquish Time (Note 5)} & \multirow[b]{2}{*}{tBR} & \(\mathrm{V}_{\text {DVDD }}=4.75 \mathrm{~V}\) to 5.25 V & & 40 & \multirow{2}{*}{ns} \\
\hline & & V \({ }_{\text {DVDD }}=2.7 \mathrm{~V}\) to 5.25 V & & 80 & \\
\hline
\end{tabular}

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after offset and gain errors have been removed.
Note 2: Offset nulled.
Note 3: Shutdown supply currents are typically \(0.5 \mu \mathrm{~A}\), maximum specification is limited by automated test equipment.
Note 4: Defined as the change in positive full scale caused by a \(\pm 5 \%\) variation in the nominal supply.
Note 5: To ensure best performance, finish reading the data and wait tBR before starting a new acquisition.

\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}

Typical Operating Characteristics
\(\left(A V_{D D}=D_{D D}=+5 \mathrm{~V}\right.\), external reference \(=+4.096 \mathrm{~V}, \mathrm{CREF}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\text {REFAD }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\), unless otherwise noted..\()\)



OFFSET ERROR
vs. TEMPERATURE


DNL vs. OUTPUT CODE


IAVDD + IDVDD SHUTDOWN CURRENT vs. TEMPERATURE


GAIN ERROR
vs. TEMPERATURE


IAVDD + IDVDD SUPPLY CURRENT
vs. SAMPLE RATE


INTERNAL REFERENCE
vs. TEMPERATURE


SINAD vs. FREQUENCY


\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}
\(\left(A V_{D D}=D V_{D D}=+5 \mathrm{~V}\right.\), external reference \(=+4.096 \mathrm{~V}, \mathrm{CREF}=4.7 \mu \mathrm{~F}, \mathrm{C}_{\text {REFADJ }}=0.1 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\), unless otherwise noted. \()\)





\title{
Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface
}

Pin Description
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{PIN} & \multicolumn{2}{|l|}{NAME} & \multirow[b]{2}{*}{FUNCTION} \\
\hline MAX1165 & MAX1166 & MAX1165 & MAX1166 & \\
\hline 1 & 1 & D8 & D4/D12 & Three-State Digital Data Output \\
\hline 2 & 2 & D9 & D5/D13 & Three-State Digital Data Output \\
\hline 3 & 3 & D10 & D6/D14 & Three-State Digital Data Output \\
\hline 4 & 4 & D11 & D7/D15 & Three-State Digital Data Output. D15 is the MSB. \\
\hline 5 & - & D12 & - & Three-State Digital Data Output \\
\hline 6 & - & D13 & - & Three-State Digital Data Output \\
\hline 7 & - & D14 & - & Three-State Digital Data Output \\
\hline 8 & - & D15 & - & Three-State Digital Data Output (MSB) \\
\hline 9 & 5 & \(\mathrm{R} /\) & & Read/Convert Input. Power up and put the MAX1165/MAX1166 in acquisition mode by holding \(\mathrm{R} / \overline{\mathrm{C}}\) low during the first falling edge of \(\overline{\mathrm{CS}}\). During the second falling edge of \(\overline{C S}\), the level on \(R / \bar{C}\) determines whether the reference and reference buffer power down or remain on after conversion. Set R/C high during the second falling edge of \(\overline{\mathrm{CS}}\) to power down the reference and buffer, or set \(\mathrm{R} / \overline{\mathrm{C}}\) low to leave the reference and buffer powered up. Set R/C high during the third falling edge of \(\overline{\mathrm{CS}}\) to put valid data on the bus. \\
\hline 10 & 6 & \(\overline{\mathrm{EO}}\) & & End of Conversion. \(\overline{\mathrm{EOC}}\) drives low when conversion is complete. \\
\hline 11 & 7 & AV & & Analog Supply Input. Bypass with a \(0.1 \mu \mathrm{~F}\) capacitor to AGND. \\
\hline 12 & 8 & AGN & & Analog Ground. Primary analog ground (star ground). \\
\hline 13 & 9 & AIN & & Analog Input \\
\hline 14 & 10 & AGN & & Analog Ground. Connect pin 14 to pin 12 (MAX1165). Connect pin 10 to pin 8 (MAX1166). \\
\hline 15 & 11 & REFA & ADJ & Reference Buffer Output. Bypass REFADJ with a \(0.1 \mu \mathrm{~F}\) capacitor to AGND for internal reference mode. Connect REFADJ to AVDD to select external reference mode. \\
\hline 16 & 12 & RE & & Reference Input/Output. Bypass REF with a \(4.7 \mu \mathrm{~F}\) capacitor to AGND for internal reference mode. External reference input when in external reference mode. \\
\hline 17 & - & RES & & Reset Input. Logic high resets the device. \\
\hline - & 13 & HBE & & \begin{tabular}{l}
High-Byte Enable Input. Used to multiplex the 14-bit conversion result: \\
1: Most significant byte available on the data bus. \\
0: Least significant byte available on the data bus.
\end{tabular} \\
\hline 18 & 14 & \(\overline{C S}\) & & Convert Start. The first falling edge of \(\overline{\mathrm{CS}}\) powers up the device and enables acquire mode when \(R / \bar{C}\) is low. The second falling edge of \(\overline{C S}\) starts conversion. The third falling edge of \(\overline{\mathrm{CS}}\) loads the result onto the bus when \(\mathrm{R} / \overline{\mathrm{C}}\) is high. \\
\hline 19 & 15 & DGN & & Digital Ground \\
\hline 20 & 16 & DV & & Digital Supply Voltage. Bypass with a \(0.1 \mu\) F capacitor to DGND. \\
\hline 21 & 17 & D0 & D0/D8 & Three-State Digital Data Output \\
\hline 22 & 18 & D1 & D1/D9 & Three-State Digital Data Output \\
\hline 23 & 19 & D2 & D2/D10 & Three-State Digital Data Output \\
\hline 24 & 20 & D3 & D3/D11 & Three-State Digital Data Output \\
\hline 25 & - & D4 & - & Three-State Digital Data Output \\
\hline 26 & - & D5 & - & Three-State Digital Data Output \\
\hline 27 & - & D6 & - & Three-State Digital Data Output \\
\hline 28 & - & D7 & - & Three-State Digital Data Output \\
\hline
\end{tabular}

\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}


Figure 1. Load Circuits

\section*{Detailed Description}

Converter Operation
The MAX1165/MAX1166 use a successive-approximation (SAR) conversion technique with an inherent track-and-hold (T/H) stage to convert an analog input into a 16-bit digital output. Parallel outputs provide a highspeed interface to most microprocessors ( \(\mu \mathrm{Ps}\) ). The Functional Diagram shows a simplified internal architecture of the MAX1165/MAX1166. Figure 3 shows a typical application circuit for the MAX1166.

\section*{Analog Input}

The equivalent input circuit is shown in Figure 4. A switched capacitor digital-to-analog converter (DAC) provides an inherent T/H function. The single-ended input is connected between AIN and AGND.

\section*{Input Bandwidth}

The ADC's input-tracking circuitry has a 4 MHz smallsignal bandwidth, so it is possible to digitize highspeed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, use anti-alias filtering.

\section*{Analog Input Protection}

Internal protection diodes, which clamp the analog input to AVDD and/or AGND, allow the input to swing from \(A G N D-0.3 V\) to \(A V D D+0.3 V\), without damaging the device.
If the analog input exceeds 300 mV beyond the supplies, limit the input current to 10 mA .


Figure 2. MAX1165/MAX1166 Timing Diagram

\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}


Figure 3. Typical Application Circuit for the MAX1166
Track and Hold (T/H)
In track mode, the analog signal is acquired on the internal hold capacitor. In hold mode, the T/H switches open and the capacitive DAC samples the analog input.
During the acquisition, the analog input (AIN) charges capacitor CDAC. The acquisition ends on the second falling edge of CS. At this instant, the T/H switches open. The retained charge on CDAC represents a sample of the input.
In hold mode, the capacitive DAC adjusts during the remainder of the conversion time to restore node ZERO to zero within the limits of 16-bit resolution. Force \(\overline{\mathrm{CS}}\) low to put valid data on the bus at the end of the conversion.
The time required for the \(\mathrm{T} / \mathrm{H}\) to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time ( \(\mathrm{t}_{\mathrm{ACQ}}\) ) is the maximum time the device takes to acquire the signal. Use the following formula to calculate acquisition time:
\[
t_{A C Q}=11\left(R_{S}+R_{I N}\right) \times 35 p F
\]
where \(\mathrm{RIN}_{\mathrm{IN}}=800 \Omega\), RS \(=\) the input signal's source impedance, and taCQ is never less than \(1.1 \mu \mathrm{~s}\). A source impedance less than \(1 \mathrm{k} \Omega\) does not significantly affect the ADC's performance.
To improve the input signal bandwidth under AC conditions, drive AIN with a wideband buffer ( \(>4 \mathrm{MHz}\) ) that can drive the ADC's input capacitance and settle quickly.


Figure 4. Equivalent Input Circuit
Power-Down Modes
Select standby mode or shutdown mode with the R/C bit during the second falling edge of \(\overline{\mathrm{CS}}\) (see the Selecting Standby or Shutdown Mode section). The MAX1165/MAX1166 automatically enter either standby mode (reference and buffer on) or shutdown (reference and buffer off) after each conversion depending on the status of \(\mathrm{R} / \overline{\mathrm{C}}\) during the second falling edge of \(\overline{\mathrm{CS}}\).

\section*{Internal Clock}

The MAX1165/MAX1166 generate an internal conversion clock. This frees the microprocessor from the burden of running the SAR conversion clock. Total conversion time after entering hold mode (second falling edge of \(\overline{\mathrm{CS}}\) ) to end of conversion ( \(\overline{\mathrm{EOC}}\) ) falling is \(4.7 \mu \mathrm{~s}\) (max).

\section*{Applications Information}

\section*{Starting a Conversion}
\(\overline{\mathrm{CS}}\) and \(\mathrm{R} / \overline{\mathrm{C}}\) control acquisition and conversion in the MAX1165/MAX1166 (Figure 2). The first falling edge of \(\overline{\mathrm{CS}}\) powers up the device and puts it in acquire mode if \(R / \bar{C}\) is low. The convert start is ignored if \(R / \bar{C}\) is high. The MAX1165/MAX1166 need at least 10 ms (CREFADJ \(=0.1 \mu \mathrm{~F}\), CREF \(=4.7 \mu \mathrm{~F}\) ) for the internal reference to wake up and settle before starting the conversion if powering up from shutdown. The ADC can wake up, from shutdown, to an unknown state. Put the ADC in a known state by completing one "dummy" conversion. The MAX1165/MAX1166 are in a known state, ready for actual data acquisition, after the completion of the dummy conversion. A dummy conversion consists of one full conversion cycle.
The MAX1165 provides an alternative reset function to reset the device (see the RESET section).

\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}


Figure 5. Selecting Standby Mode

\section*{Selecting Standby or Shutdown Mode}

The MAX1165/MAX1166 have a selectable standby or low-power shutdown mode. In standby mode, the ADC's internal reference and reference buffer do not power down between conversions, eliminating the need to wait for the reference to power up before performing the next conversion. Shutdown mode powers down the reference and reference buffer after completing a conversion. The reference and reference buffer require a minimum of \(10 \mathrm{~ms}(\) CREFADJ \(=0.1 \mu \mathrm{~F}, \mathrm{CREF}=4.7 \mu \mathrm{~F})\) to power up and settle from shutdown.
The state of \(R / \bar{C}\) at the second falling edge of \(\overline{C S}\) selects which power-down mode the MAX1165/ MAX1166 enter upon conversion completion. Holding R/C low causes the MAX1165/MAX1166 to enter standby mode. The reference and buffer are left on after the conversion completes. R/C high causes the MAX1165/ MAX1166 to enter shutdown mode and shut down the reference and buffer after conversion (Figures 5 and 6). When using an external reference, set the REF powerdown bit high for lowest current operation.

\section*{Standby Mode}

While in standby mode, the supply current is reduced to less than 1mA (typ). The next falling edge of \(\overline{C S}\) with R/C low causes the MAX1165/MAX1166 to exit standby mode and begin acquisition. The reference and reference buffer remain active to allow quick turn-on time. Standby mode allows significant power savings while running at the maximum sample rate.

Shutdown Mode
In shutdown mode, the reference and reference buffer are shut down between conversions. Shutdown mode reduces supply current to \(0.5 \mu \mathrm{~A}\) (typ) immediately after the conversion. The falling edge of \(\overline{C S}\) with \(R / \bar{C}\) low


Figure 6. Selecting Shutdown Mode
causes the reference and buffer to wake up and enter acquisition mode. To achieve 16-bit accuracy, allow \(10 \mathrm{~ms}(\) CREFADJ \(=0.1 \mu \mathrm{~F}, \mathrm{CREF}=4.7 \mu \mathrm{~F})\) for the internal reference to wake up.

\section*{Internal and External Reference}

Internal Reference
The internal reference of the MAX1165/MAX1166 is internally buffered to provide +4.096 V output at REF. Bypass REF to AGND and REFADJ to AGND with \(4.7 \mu \mathrm{~F}\) and \(0.1 \mu \mathrm{~F}\), respectively.
Fine adjustments can be made to the internal reference voltage by sinking or sourcing current at REFADJ. The input impedance of REFADJ is nominally \(5 \mathrm{k} \Omega\). The internal reference voltage is adjustable to \(\pm 1.5 \%\) with the circuit of Figure 7.


Figure 7. MAX1165/MAX1166 Reference Adjust Circuit

\section*{External Reference}

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1165/ MAX1166s' internal buffer amplifier. When connecting an

\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}
external reference to REFADJ, the input impedance is typically \(5 \mathrm{k} \Omega\). Using the buffered REFADJ input makes buffering the external reference unnecessary; however, the internal buffer output must be bypassed at REF with a \(1 \mu \mathrm{~F}\) capacitor.
Connect REFADJ to AVDD to disable the internal buffer. Directly drive REF using an external reference. During conversion the external reference must be able to drive \(100 \mu \mathrm{~A}\) of DC load current and have an output impedance of \(10 \Omega\) or less. REFADJ's impedance is typically \(5 k \Omega\). The DC input impedance of REF is a minimum \(40 \mathrm{k} \Omega\).
For optimal performance, buffer the reference through an op amp and bypass REF with a \(1 \mu \mathrm{~F}\) capacitor. Consider the MAX1165/MAX1166s' equivalent input noise \(\left(38 \mu V_{\mathrm{RMS}}\right)\) when choosing a reference.

\section*{Reading a Conversion Result}
\(\overline{\mathrm{EOC}}\) is provided to flag the microprocessor when a conversion is complete. The falling edge of \(\overline{\mathrm{EOC}}\) signals that the data is valid and ready to be output to the bus.
D0-D15 are the parallel outputs of the MAX1165/ MAX1166. These three-state outputs allow for direct connection to a microcontroller I/O bus. The outputs remain high-impedance during acquisition and conversion. Data is loaded onto the bus with the third falling edge of \(\overline{C S}\) with \(R / \bar{C}\) high after tDO. Bringing \(\overline{C S}\) high forces the output bus back to high impedance. The MAX1165/MAX1166 then wait for the next falling edge of \(\overline{\mathrm{CS}}\) to start the next conversion cycle (Figure 2).
The MAX1165 loads the conversion result onto a 16-bit wide data bus while the MAX1166 has a byte-wide output format. HBEN toggles the output between the most/least significant byte. The least significant byte is loaded onto the output bus when HBEN is low and the most significant byte is on the bus when HBEN is high (Figure 2).

RESET
Toggle RESET with \(\overline{\mathrm{CS}}\) high. The next falling edge of \(\overline{\mathrm{CS}}\) begins acquisition. This reset is an alternative to the dummy conversion explained in the Starting a Conversion section.

\section*{Transfer Function}

Figure 8 shows the MAX1165/MAX1166 output transfer function. The output is coded in standard binary.

\section*{Input Buffer}

Most applications require an input buffer amplifier to achieve 16 -bit accuracy. If the input signal is multi-


Figure 8. MAX1165/MAX1166 Transfer Function
plexed, the input channel should be switched immediately after acquisition, rather than near the end of or after a conversion. This allows more time for the input buffer amplifier to respond to a large step change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change before the beginning of the acquisition time. At the beginning of acquisition, the internal sampling capacitor array connects to AIN (the amplifier output), causing some output disturbance. Ensure that the sampled voltage has settled to within the required limits before the end of the acquisition time. If the frequency of interest is low, AIN can be bypassed with a large enough capacitor to charge the internal sampling capacitor with very little ripple. However, for AC use, AIN must be driven by a wideband buffer (at least 10 MHz ), which must be stable with the ADC's capacitive load (in parallel with any AIN bypass capacitor used) and also settle quickly. An example of this circuit using the MAX4434 is given in Figure 9.


Figure 9. MAX1165/MAX1166 Fast Settling Input Buffer

\title{
Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface
}

\begin{abstract}
Layout, Grounding, and Bypassing
For best performance, use printed circuit boards. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital ground planes with only one point connecting the two ground systems (analog and digital) as close to the device as possible.
Route digital signals far away from sensitive analog and reference inputs. If digital lines must cross analog lines, do so at right angles to minimize coupling digital noise onto the analog lines. If the analog and digital sections share the same supply, then isolate the digital and analog supply by connecting them with a low-value (10 resistor or ferrite bead.
The ADC is sensitive to high-frequency noise on the AVDD supply. Bypass AVDD to AGND with a \(0.1 \mu \mathrm{~F}\) capacitor in parallel with a \(1 \mu \mathrm{~F}\) to \(10 \mu \mathrm{~F}\) low-ESR capacitor with the smallest capacitor closest to the device. Keep capacitor leads short to minimize stray inductance.
\end{abstract}

\section*{Definitions}

\section*{Integral Nonlinearity}

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1165/MAX1166 are measured using the end-point method.

\section*{Differential Nonlinearity}

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of \(\pm 1\) LSB guarantees no missing codes and a monotonic transfer function.

\section*{Aperture Jitter and Delay}

Aperture jitter is the sample-to-sample variation in the time between samples. Aperture delay is the time between the rising edge of the sampling clock and the instant when the actual sample is taken.

\section*{Signal-to-Noise Ratio}

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization
noise error only and results directly from the ADC's resolution (N bits):
\[
\text { SNR }=(6.02 \times N+1.76) \mathrm{dB}
\]
where \(\mathrm{N}=16\) bits.
In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:
\[
\text { SINAD }(\mathrm{dB})=20 \times \log \left[\frac{\text { Signal }_{\text {RMS }}}{(\text { Noise }+ \text { Distortion })_{\mathrm{RMS}}}\right]
\]

Effective Number of Bits Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the fullscale range of the ADC, calculate the effective number of bits as follows:
\[
\mathrm{ENOB}=\frac{\mathrm{SINAD}-1.76}{6.02}
\]

\section*{Total Harmonic Distortion}

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:
\[
\mathrm{THD}=20 \times \log \left[\frac{\left(\sqrt{V_{2}^{2}+V_{3}^{2}+V_{4}^{2}+V_{5}^{2}}\right)}{V_{1}}\right]
\]
where \(\mathrm{V}_{1}\) is the fundamental amplitude and \(\mathrm{V}_{2}\) through \(V_{5}\) are the 2nd- through 5th-order harmonics.

\section*{Spurious-Free Dynamic Range}

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component.

\title{
Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface
}

Functional Diagram


Ordering Information (continued)
\begin{tabular}{|lrlc|}
\hline \multicolumn{1}{|c}{ PART } & TEMP RANGE & PIN-PACKAGE & INL \\
\hline MAX1166ACUP & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 20 TSSOP & \(\pm 2\) \\
\hline MAX1166BCUP & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 20 TSSOP & \(\pm 2\) \\
\hline MAX1166CCUP & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 20 TSSOP & \(\pm 4\) \\
\hline MAX1166AEUP & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 20 TSSOP & \(\pm 2\) \\
\hline MAX1166BEUP \({ }^{\star}\) & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 20 TSSOP & \(\pm 2\) \\
\hline MAX1166CEUP \({ }^{*}\) & \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\) & 20 TSSOP & \(\pm 4\) \\
\hline
\end{tabular}
*Future product-contact factory for availability

TRANSISTOR COUNT: 15,140
PROCESS: BiCMOS

Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface


\section*{Low-Power, 16-Bit Analog-to-Digital Converter with Parallel Interface}
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)


This datasheet has been download from:
www.datasheetcatalog.com
Datasheets for electronics components.

\title{
Dual, \(5 \Omega\) Analog Switches
}

\section*{General Description}

The MAX4621/MAX4622/MAX4623 are precision, dual, high-speed analog switches. The single-pole/singlethrow (SPST) MAX4621 and double-pole/single-throw (DPST) MAX4623 dual switches are normally open (NO). The single-pole/double-throw (SPDT) MAX4622 has two normally closed (NC) and two NO poles. All three parts offer low \(5 \Omega\) on-resistance guaranteed to match to within \(0.5 \Omega\) between channels and to remain flat over the full analog signal range ( \(\Delta 0.5 \Omega\) max). They also offer low leakage ( \(<500\) pA at \(+25^{\circ} \mathrm{C}, \angle 5 n A\) at \(+85^{\circ} \mathrm{C}\) ) and fast switching times (turn-on time \(<250 \mathrm{~ns}\), turn-off time <200ns).
These analog switches are ideal in low-distortion applications and are the preferred solution over mechanical relays in automatic test equipment or applications where current switching is required. They have low power requirements, use less board space, and are more reliable than mechanical relays.
The MAX4621/MAX4622/MAX4623 are pin-compatible replacements for the DG401/DG403/DG405, respectively , offering improved overall performance. These monolithic switches operate from a single positive supply \((+4.5 \mathrm{~V}\) to +36 V ) or with bipolar supplies ( \(\pm 4.5 \mathrm{~V}\) to \(\pm 18 \mathrm{~V}\) ) while retaining CMOS-logic input compatibility.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Features
- Low On-Resistance: \(3 \Omega\) (typ), \(5 \Omega\) (max)
- Guaranteed Ron Match Between Channels ( \(0.5 \Omega\) max)
- Guaranteed Break-Before-Make Operation (MAX4622)
- Guaranteed Off-Channel Leakage \(<5 n A\) at \(+85^{\circ} \mathrm{C}\)
- Single-Supply Operation ( +4.5 V to +36 V )

Bipolar-Supply Operation ( \(\pm 4.5 \mathrm{~V}\) to \(\pm 18 \mathrm{~V}\) )
- TTL/CMOS-Logic Compatible
- Rail-to-Rail \({ }^{\circledR}\) Analog Signal Handling Capability
- Pin Compatible with DG401/DG403/DG405
\begin{tabular}{ll} 
& \multicolumn{1}{c}{ Applications } \\
\hline Reed Relay Replacement & Military Radios \\
Test Equipment & PBX, PABX Systems \\
Communication Systems & Audio-Signal Routing \\
Data-Acquisition Systems & Avionics
\end{tabular}

Ordering Information
\begin{tabular}{|lll|}
\hline \multicolumn{1}{|c}{ PART } & TEMP. RANGE & PIN-PACKAGE \\
\hline MAX4621CSE & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 16 Narrow SO \\
\hline MAX4621CPE & \(0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\) & 16 Plastic DIP \\
\hline
\end{tabular}

Ordering Information continued at end of data sheet.


For free samples \& the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 1-800-835-8769.

\section*{Dual, \(5 \Omega\) Analog Switches}
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ABSOLUTE MAXIMUM RATINGS

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(Voltages Referenced to GND)


Continuous Power Dissipation ( \(\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}\) )
Narrow SO (derate \(8.70 \mathrm{~mW} /{ }^{\circ} \mathrm{C}\) above \(+70^{\circ} \mathrm{C}\) ) ............. 696 mW Narrow DIP (derate \(10.53 \mathrm{~mW} /{ }^{\circ} \mathrm{C}\) above \(+70^{\circ} \mathrm{C}\) ) .......... 842 mW Operating Temperature Ranges
MAX462_C \(\qquad\) \(.0^{\circ} \mathrm{C}\) to \(+70^{\circ} \mathrm{C}\)
MAX462 E \(-40^{\circ} \mathrm{C}\) to \(+85^{\circ} \mathrm{C}\)
Storage Temperature Range \(\qquad\) \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
Lead Temperature (soldering, 10sec) \(\qquad\) \(+300^{\circ} \mathrm{C}\)

Note 1: Signals on NO_, NC_, or COM_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\section*{ELECTRICAL CHARACTERISTICS—Dual Supplies}
\(\left(\mathrm{V}+=+15 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{L}}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{~V}_{\mathrm{INH}}=+2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{I} L \mathrm{~L}}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.\) to \(\mathrm{T}_{\mathrm{MAX}}\), unless otherwise noted. Typical values are at \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\).) (Note 2)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline PARAMETER & SYMBOL & \multicolumn{2}{|c|}{CONDITIONS} & MIN & TYP & MAX & UNITS \\
\hline \multicolumn{8}{|l|}{ANALOG SWITCH} \\
\hline Input Voltage Range (Note 3) & VCOM_ VNO_, \(\mathrm{VNC}_{-}\) & & & V- & & V+ & V \\
\hline \multirow[t]{2}{*}{On-Resistance} & \multirow[b]{2}{*}{Ron} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{ICOM}_{-}=10 \mathrm{~mA} \\
& \mathrm{~V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}_{-}}= \pm 10 \mathrm{~V}
\end{aligned}
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 3 & 5 & \multirow[t]{2}{*}{\(\Omega\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & & & 7 & \\
\hline \multirow[t]{2}{*}{On-Resistance Match Between Channels (Notes 3, 4)} & \multirow{2}{*}{\(\Delta \mathrm{RoN}\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{ICOM}_{-}=10 \mathrm{~mA} \\
& \mathrm{~V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}}^{-}
\end{aligned}= \pm 10 \mathrm{~V} .
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 0.25 & 0.5 & \multirow{2}{*}{\(\Omega\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to TMAX & & & 0.7 & \\
\hline \multirow[t]{2}{*}{\begin{tabular}{l}
On-Resistance Flatness \\
(Notes 3, 5)
\end{tabular}} & \multirow{2}{*}{RFLAT(ON)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{ICOM}_{-}=10 \mathrm{~mA} ; \\
& \mathrm{V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}_{-}}=-5 \mathrm{~V} \text {, } \\
& 0,5 \mathrm{~V}
\end{aligned}
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 0.2 & 0.5 & \multirow{2}{*}{\(\Omega\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & & & 0.7 & \\
\hline \multirow[t]{2}{*}{Off-Leakage Current (NO_ or NC_) (Note 6)} & \multirow[b]{2}{*}{\({ }^{\prime} \mathrm{NO}_{-}, \mathrm{INC}^{\prime}\)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{\mathrm{NO}_{-} \text {or }} \mathrm{V}_{\mathrm{NC}_{-}}= \pm 10 \mathrm{~V}, \\
& \mathrm{~V}_{\mathrm{COM}}=\mp 10 \mathrm{~V}
\end{aligned}
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.01 & 0.5 & \multirow[b]{2}{*}{nA} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -5 & & 5 & \\
\hline \multirow[t]{2}{*}{COM_ Off-Leakage Current (Note 6)} & \multirow[b]{2}{*}{ICOM_(OFF)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{V}_{C O M}= \pm 10 \mathrm{~V} \\
& \mathrm{~V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=\mp 10 \mathrm{~V}
\end{aligned}
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.01 & 0.5 & \multirow[t]{2}{*}{nA} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -5 & & 5 & \\
\hline \multirow[t]{2}{*}{COM_ On-Leakage Current (Note 6)} & \multirow{2}{*}{ICOM_(ON)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{VCOM}_{\mathrm{CO}}= \pm 10 \mathrm{~V}, \\
& \mathrm{~V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=\mp 10 \mathrm{~V}
\end{aligned}
\]
or floating} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -1 & 0.02 & 1 & \multirow{2}{*}{nA} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to TMAX & -10 & & 10 & \\
\hline \multicolumn{8}{|l|}{LOGIC INPUT} \\
\hline Input Current with Input Voltage High & IINH & \multicolumn{2}{|l|}{VIN_ \(=2.4 \mathrm{~V}\)} & -0.5 & 0.001 & 0.5 & \(\mu \mathrm{A}\) \\
\hline Input Current with Input Voltage Low & IINL & \multicolumn{2}{|l|}{\(\mathrm{V}_{1} \mathrm{~N}_{-}=0.8 \mathrm{~V}\)} & -0.5 & 0.001 & 0.5 & \(\mu \mathrm{A}\) \\
\hline Logic Input Voltage High & VINH & & & \multicolumn{3}{|l|}{2.4} & V \\
\hline Logic Input Voltage Low & VINL & & & & & 0.8 & V \\
\hline
\end{tabular}

\section*{Dual, \(5 \Omega\) Analog Switches}

\section*{ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)}
\(\left(\mathrm{V}+=+15 \mathrm{~V}, \mathrm{~V}-=-15 \mathrm{~V}, \mathrm{VL}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{~V} \operatorname{INH}=+2.4 \mathrm{~V}, \mathrm{~V} \operatorname{INL}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.\) to \(\mathrm{T}_{\mathrm{MAX}}\), unless otherwise noted. Typical values are at \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\).) (Note 2)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline PARAMETER & SYMBOL & \multicolumn{2}{|c|}{CONDITIONS} & MIN & TYP & MAX & UNITS \\
\hline \multicolumn{8}{|l|}{POWER SUPPLY} \\
\hline Power-Supply Range & & & & \(\pm 4.5\) & & \(\pm 20.0\) & V \\
\hline \multirow[b]{2}{*}{Positive Supply Current} & \multirow[t]{2}{*}{I+} & \multirow[b]{2}{*}{\(\mathrm{V}_{1} \mathrm{~N}_{-}=0\) or 5 V} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.001 & 0.5 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -5 & & 5 & \\
\hline \multirow[b]{2}{*}{Negative Supply Current} & \multirow[t]{2}{*}{I-} & \multirow[b]{2}{*}{\(\mathrm{V} \mathrm{IN}_{-}=0\) or 5 V} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.001 & 0.5 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to TMAX & -5 & & 5 & \\
\hline \multirow[b]{2}{*}{Logic Supply Current} & \multirow[t]{2}{*}{IL} & \multirow[t]{2}{*}{VIN_ \(=0\) or 5 V} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.001 & 0.5 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -5 & & 5 & \\
\hline \multirow[b]{2}{*}{Ground Current} & \multirow[b]{2}{*}{IGND} & \multirow[b]{2}{*}{\(\mathrm{V} \mathrm{N}_{-}=0\) or 5 V} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.001 & 0.5 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to TMAX & -5 & & 5 & \\
\hline \multicolumn{8}{|l|}{SWITCH DYNAMIC CHARACTERISTICS} \\
\hline \multirow[t]{2}{*}{Turn-On Time} & \multirow[b]{2}{*}{ton} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C O M}= \pm 10 \mathrm{~V},
\] \\
Figure 2
\end{tabular}} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 120 & 250 & \multirow[b]{2}{*}{ns} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & & & 325 & \\
\hline \multirow[t]{2}{*}{Turn-Off Time} & \multirow[t]{2}{*}{toff} & \multirow[t]{2}{*}{\begin{tabular}{l}
\[
V_{C O M}= \pm 10 \mathrm{~V},
\] \\
Figure 2
\end{tabular}} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 90 & 200 & \multirow[t]{2}{*}{ns} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & & & 275 & \\
\hline Break-Before-Make Time Delay (MAX4622 only) & tD & \multicolumn{2}{|l|}{\(\mathrm{VCOM}_{-}= \pm 10 \mathrm{~V}\), Figure \(3, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & 5 & 25 & & ns \\
\hline Charge Injection & Q & \multicolumn{2}{|l|}{\[
\begin{aligned}
& C_{L}=1.0 n F, V_{G E N}=0, \text { RGEN }=0 \text {, Figure } 4, \\
& T_{A}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & & 480 & & pC \\
\hline Off-Isolation (Note 7) & VISO & \multicolumn{2}{|l|}{\(\mathrm{RL}_{\mathrm{L}}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}\), Figure \(5, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & & -62 & & dB \\
\hline Crosstalk (Note 8) & \(\mathrm{V}_{\text {CT }}\) & \multicolumn{2}{|l|}{\(R \mathrm{~L}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}\), Figure 6, \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & & -60 & & dB \\
\hline NC_ or NO_ Capacitance & Coff & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{MHz}\), Figure 7, \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & & 34 & & pF \\
\hline COM_ Off-Capacitance & Ссом & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{MHz}\), Figure 7, \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & & 34 & & pF \\
\hline On-Capacitance & Ccom & \multicolumn{2}{|l|}{\(\mathrm{f}=1 \mathrm{MHz}\), Figure \(8, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\)} & & 150 & & pF \\
\hline
\end{tabular}

\section*{Dual, \(5 \Omega\) Analog Switches}

\section*{ELECTRICAL CHARACTERISTICS—Single Supply}
\(\left(\mathrm{V}+=+12 \mathrm{~V}, \mathrm{~V}-=0, \mathrm{VL}_{\mathrm{L}}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{VINH}=+2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{INL}}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.\) to \(\mathrm{T}_{\mathrm{MAX}}\), unless otherwise noted. Typical values are \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\).) (Note 2)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline PARAMETER & SYMBOL & \multicolumn{2}{|c|}{CONDITIONS} & MIN & TYP & MAX & UNITS \\
\hline \multicolumn{8}{|l|}{ANALOG SWITCH} \\
\hline Input Voltage Range (Note 3) & VCOM_ VNO_, \(\mathrm{V}_{\mathrm{NC}}\) & & & GND & & V+ & V \\
\hline \multirow[b]{2}{*}{On-Resistance} & \multirow[b]{2}{*}{Ron} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{ICOM}_{-}=10 \mathrm{~mA}, \\
& \mathrm{~V}_{\mathrm{NO}}^{2} \\
& \text { or } \mathrm{V}_{\mathrm{NC}}^{-}
\end{aligned}=10 \mathrm{~V} .
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 5.5 & 8 & \multirow[b]{2}{*}{\(\Omega\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\) TMIN to \(\mathrm{T}_{\text {MAX }}\) & & & 10 & \\
\hline On-Resistance Match Between Channels (Notes 3, 4) & \(\Delta \mathrm{RoN}\) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \mathrm{ICOM}_{-}=10 \mathrm{~mA}, \mathrm{~V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}_{-}}=10 \mathrm{~V} \text {, } \\
& \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & & 0.2 & 0.5 & \(\Omega\) \\
\hline On-Resistance Flatness (Notes 3, 5) & RFLAT(ON) & \multicolumn{2}{|l|}{\[
\begin{aligned}
& \text { ICOM_ }=10 \mathrm{~mA} ; \mathrm{V}_{\mathrm{NO}_{-}} \text {or } \mathrm{V}_{\mathrm{NC}_{-}}=3 \mathrm{~V}, 6 \mathrm{~V}, 9 \mathrm{~V} \text {; } \\
& \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}
\end{aligned}
\]} & & 0.9 & 1.3 & \(\Omega\) \\
\hline \multirow[t]{2}{*}{NO_ or NC_ Off-Leakage Current (Notes 6, 9)} & \multirow[t]{2}{*}{\begin{tabular}{l}
INO_(OFF), \\
INC_(OFF)
\end{tabular}} & \multirow[t]{2}{*}{\[
\begin{aligned}
& \mathrm{VCOM}_{-}=1 \mathrm{~V}, 10 \mathrm{~V} ; \\
& \mathrm{V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=10 \mathrm{~V}, 1 \mathrm{~V}
\end{aligned}
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.01 & 0.5 & \multirow[t]{2}{*}{nA} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -5 & & 5 & \\
\hline \multirow[t]{2}{*}{COM_ Off-Leakage Current (Notes 6, 9)} & \multirow[t]{2}{*}{ICOM_(OFF)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C O M}^{-}=10 \mathrm{~V}, 1 \mathrm{~V} \\
& \mathrm{~V}_{\text {NO_ }} \text { or } \mathrm{V}_{\text {NC_ }}=1 \mathrm{~V}, 10 \mathrm{~V}
\end{aligned}
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.01 & 0.5 & \multirow[t]{2}{*}{nA} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -5 & & 5 & \\
\hline \multirow[t]{2}{*}{COM_ On-Leakage Current (Notes 6, 9)} & \multirow{2}{*}{ICOM_(ON)} & \multirow[t]{2}{*}{\[
\begin{aligned}
& V_{C O M}=10 \mathrm{~V}, 1 \mathrm{~V} ; \\
& \mathrm{V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=10 \mathrm{~V}, \\
& 1 \mathrm{~V} \text {, or floating }
\end{aligned}
\]} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -1 & 0.02 & 1 & \multirow{2}{*}{nA} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -10 & & 10 & \\
\hline \multicolumn{8}{|l|}{LOGIC INPUT} \\
\hline Input Current with Input Voltage High & IINH & \multicolumn{2}{|l|}{\(\mathrm{V}_{1} \mathrm{~N}_{-}=2.4 \mathrm{~V}\)} & -0.5 & 0.001 & 0.5 & \(\mu \mathrm{A}\) \\
\hline Input Current with Input Voltage Low & IINL & \multicolumn{2}{|l|}{\(\mathrm{V} \mathrm{IN}_{-}=0.8 \mathrm{~V}\)} & -0.5 & 0.001 & 0.5 & \(\mu \mathrm{A}\) \\
\hline Logic Input Voltage High & VINH & & & 2.4 & & & V \\
\hline Logic Input Voltage Low & VINL & & & & & 0.8 & V \\
\hline \multicolumn{8}{|l|}{POWER SUPPLY} \\
\hline Power-Supply Range & & & & 4.5 & & 36.0 & V \\
\hline \multirow[b]{2}{*}{Positive Supply Current} & \multirow[t]{2}{*}{I+} & \multirow[b]{2}{*}{VIN_ \(=0\) or 5 V} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.001 & 0.5 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\) TMIN to TMAX & -5 & & 5 & \\
\hline \multirow[b]{2}{*}{Logic Supply Current} & \multirow[b]{2}{*}{IL} & \multirow[b]{2}{*}{VIN_ \(=0\) or 5 V} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.001 & 0.5 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to TMAX & -5 & & 5 & \\
\hline \multirow[t]{2}{*}{Ground Current} & \multirow[b]{2}{*}{IGND} & \multirow[b]{2}{*}{\(\mathrm{V} \mathrm{N}_{-}=0\) or 5 V} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & -0.5 & 0.001 & 0.5 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & -5 & & 5 & \\
\hline
\end{tabular}

\section*{Dual, \(5 \Omega\) Analog Switches}

\section*{ELECTRICAL CHARACTERISTICS—Single Supply (continued)}
\(\left(\mathrm{V}+=+12 \mathrm{~V}, \mathrm{~V}-=0, \mathrm{~V}_{\mathrm{L}}=+5 \mathrm{~V}, \mathrm{GND}=0, \mathrm{~V} \operatorname{INH}=+2.4 \mathrm{~V}, \mathrm{~V} \operatorname{INL}=+0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{MIN}}\right.\) to \(\mathrm{T}_{\mathrm{MAX}}\), unless otherwise noted. Typical values are \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\).) (Note 2)
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline PARAMETER & SYMBOL & \multicolumn{2}{|c|}{CONDITIONS} & MIN & TYP & MAX & UNITS \\
\hline \multicolumn{8}{|l|}{SWITCH DYNAMIC CHARACTERISTICS} \\
\hline \multirow[b]{2}{*}{Turn-On Time (Note 3)} & \multirow[b]{2}{*}{ton} & \multirow[b]{2}{*}{\(\mathrm{VCOM}_{-}=10 \mathrm{~V}\), Figure 2} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 200 & 350 & \multirow[b]{2}{*}{ns} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & & & 475 & \\
\hline \multirow[b]{2}{*}{Turn-Off Time (Note 3)} & \multirow[b]{2}{*}{tofF} & \multirow[b]{2}{*}{\(\mathrm{VCOM}_{-}=10 \mathrm{~V}\), Figure 2} & \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) & & 100 & 200 & \multirow[b]{2}{*}{ns} \\
\hline & & & \(\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}\) to \(\mathrm{T}_{\text {MAX }}\) & & & 300 & \\
\hline Break-Before-Make Time Delay (MAX4622 only) (Note 3) & tD & \multicolumn{2}{|l|}{\(R L=100 \Omega, C L=35 p F\), Figure 3, \(T_{A}=+25^{\circ} \mathrm{C}\)} & 10 & 75 & & ns \\
\hline Charge Injection & Q & \multicolumn{2}{|l|}{\(\mathrm{CL}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{V}_{\mathrm{GEN}}=0\), RGEN \(=0\), Figure 4} & & \multicolumn{2}{|l|}{45} & pC \\
\hline Off-Isolation (Note 7) & VISO & \multicolumn{2}{|l|}{\(\mathrm{RL}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}\), Figure 5} & & \multicolumn{2}{|l|}{-62} & dB \\
\hline Crosstalk (Note 8) & \(\mathrm{V}_{\mathrm{C}}\) T & \multicolumn{2}{|l|}{\(\mathrm{RL}=50 \Omega, \mathrm{f}=1 \mathrm{MHz}\), Figure 6} & & -60 & & dB \\
\hline
\end{tabular}

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: \(\Delta\) RON = RON_MAX - RON_MIN.
Note 5: Flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog signal range.
Note 6: Leakage currents are \(100 \%\) tested at the maximum-rated hot temperature and guaranteed by correlation at \(+25^{\circ} \mathrm{C}\).

Note 8: Between any two switches.
Note 9: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

\section*{Dual, \(5 \Omega\) Analog Switches}

\section*{Typical Operating Characteristics}
( \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\), unless otherwise noted.)



ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)






\section*{Dual, \(5 \Omega\) Analog Switches}

Pin Description
\begin{tabular}{|c|c|c|}
\hline PIN & NAME & FUNCTION \\
\hline \multicolumn{3}{|l|}{MAX4621} \\
\hline 1, 8 & COM1, COM2 & Switch Common Terminal \\
\hline 2-7 & N.C. & Not internally connected \\
\hline 9, 16 & NO2, NO1 & Switch Normally Open Terminal \\
\hline 10, 15 & IN2, IN1 & Digital Logic Inputs \\
\hline 11 & V+ & Positive Supply-Voltage Input \\
\hline 12 & VL & Logic Supply-Voltage Input \\
\hline 13 & GND & Ground \\
\hline 14 & V- & Negative Supply Voltage Input \\
\hline \multicolumn{3}{|l|}{MAX4622} \\
\hline 1, 3, 6, 8 & COM_ & Switch Common Terminal \\
\hline 2, 7 & N.C. & Not internally connected \\
\hline 4, 5, 9, 16 & NC_, NO_ & Switch Normally Closed/Open Terminal \\
\hline 10, 15 & IN2, IN1 & Digital Logic Inputs \\
\hline 11 & V+ & Positive Supply-Voltage Input \\
\hline 12 & VL & Logic Supply-Voltage Input \\
\hline 13 & GND & Ground \\
\hline 14 & V- & Negative Supply Voltage Input \\
\hline \multicolumn{3}{|l|}{MAX4623} \\
\hline 1, 3, 6, 8 & COM_ & Switch Common Terminal \\
\hline 2, 7 & N.C. & Not internally connected \\
\hline 4, 5, 9, 16 & NO_ & Switch Normally Open Terminal \\
\hline 10, 15 & IN2, IN1 & Digital Logic Inputs \\
\hline 11 & V+ & Positive Supply-Voltage Input \\
\hline 12 & VL & Logic Supply-Voltage Input \\
\hline 13 & GND & Ground \\
\hline 14 & V- & Negative Supply Voltage \\
\hline
\end{tabular}

\section*{Applications Information}

\section*{Operation with Supply Voltages Other than \(\pm 15 \mathrm{~V}\)}

The MAX4621/MAX4622/MAX4623 switches operate with \(\pm 4.5 \mathrm{~V}\) to \(\pm 18 \mathrm{~V}\) bipolar supplies and \(\mathrm{a}+4.5 \mathrm{~V}\) to +36 V single supply. In either case, analog signals ranging from V+ to V-can be switched. The Typical Operating Characteristics graphs show the typical on-resistance variation with analog signal and supply voltage.

\section*{Overvoltage Protection}

Proper power-supply sequencing is recommended for all CMOS devices. It is important not to exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence \(V+\) on first, followed by \(V_{L}, V_{-}\), and logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with the supply pins and a Schottky diode between V+ and VL (Figure 1). Adding diodes reduces the analog signal range to 1 V below V+ and 1V above V-, but low switch resistance and low leakage characteristics are unaffected. The difference between \(V+\) and \(V\) - should not exceed +44 V .


Figure 1. Overvoltage Protection Using Blocking Diodes

\section*{Dual, \(5 \Omega\) Analog Switches}


Figure 2. Switching-Time Test Circuit


Figure 3. MAX4622 Break-Before-Make Test Circuit

\(Q=\left(\Delta V_{0}\right)\left(C_{L}\right)\)

Figure 4. Charge-Injection Test Circuit

\section*{Dual， \(5 \Omega\) Analog Switches}


Figure 5．Off－Isolation
\begin{tabular}{|c|c|c|}
\hline \begin{tabular}{c} 
FREQUENCY \\
TESTED
\end{tabular} & \begin{tabular}{c} 
SIGNAL \\
GENERATOR
\end{tabular} & ANALYZER \\
\hline 1 MHz & \begin{tabular}{c} 
AUTOMATIC \\
SYNTHESIZER
\end{tabular} & \begin{tabular}{c} 
TRACKING SPECTRUM \\
ANALYZER
\end{tabular} \\
\hline
\end{tabular}

Figure 6．Crosstalk Test Circuit


Figure 7．Channel－On Capacitance


Figure 8．Channel－Off Capacitance

\section*{Dual, \(5 \Omega\) Analog Switches}
_Cordering Information (continued)
Chip Information
TRANSISTOR COUNT: 82

Package Information


\section*{Dual, \(5 \Omega\) Analog Switches}

Package Information (continued)


\title{
Dual, \(5 \Omega\) Analog Switches
}

\section*{NOTES}

\title{
The Design Of An Embedded Controller For An Automated Volt-Drop Test
}

\section*{A Collection Of Screen Captures And Notes}

\title{
The Design Of An Embedded Controller For An Automated Volt-Drop Test
}

\author{
The Graphic User Interface
}

\section*{(GUI)}





The GUI Start-up Screen


Test In Progress Fields
Fault Log




The only input available is the "Lock Out Password" input box.



\section*{Manual Reading Controls}


\section*{GUI Special Fuction Controls}

View Controls












Test Parameter


- View User Profile Setup

View User Profile







\section*{Test In Progress Fields}











View User Profile Setup
View User Profile






Click To Remove Highlighted Armature

\section*{- Job Number}

\begin{tabular}{ll} 
Test Option \\
\begin{tabular}{ll} 
Choose an Operating \\
Option
\end{tabular} & C Manual Operation \\
& C Automated Operation
\end{tabular}


\section*{Test In Progress Fields}

\section*{Fault Log}



Test In Progress Fields


\section*{- Manual Reading Controls}



Job Number
001 Test Results

\section*{Test In Progress Fields}


GUI Special Fuction Controls
-View/Change Directory Path Settings
View Controls

- View User Profile Setup

View User Profile

\title{
The Design Of An Embedded Controller For An Automated Volt-Drop Test
}

\section*{The Remote Graphic User Interface (RGUI)}





-Print Displayed Data
Print

\begin{tabular}{|l|l|}
\hline File Names \\
\hline matadin \\
sunveer \\
dude \\
sun \\
bday \\
diff \\
sss \\
sunnyy \\
sunveertry 2 \\
adDdAd \\
ASA \\
ssss & \\
\hline
\end{tabular}

\section*{Refined Search - Dates}

\section*{ViewAll}
-Display Data
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Job Number: sunveer
Operator's Name: sun1
Armature Name: b Number of Bars: 10
Percentage Variance: \(20 \%\)
Date: \(2005 / 05 / 05\)} \\
\hline \multicolumn{2}{|l|}{Recorded Faults} \\
\hline \multicolumn{2}{|l|}{Emergency Stop on Bar 0 End Of Recorded Results} \\
\hline \multicolumn{2}{|l|}{Job Number: sunveer Operator's Name: sun2 Armature Name: g Number of Bars: 100 Percentage Variance: 30\% Date: 2005/05/05} \\
\hline \multicolumn{2}{|l|}{Recorded Faults} \\
\hline Emergency Stop on Bar 0 & On clicking on a specific serial number, a \\
\hline \begin{tabular}{l}
End Of Recorded Results \\
Job Number: sunveer Operator's Name: sun'3 \\
Armature Name. Number of Bars: 50 \\
Percentage Variance: \(40 \%\) \\
Date? 2005/05/05
\end{tabular} & list of all test dates on which tests on that armature were carried out, will appear, beginning with the "View All" option. On clicking on a specific date, only the results \\
\hline \begin{tabular}{l}
Recorded Faults \\
Emergency Stop on Bar 0 \\
End Of Recorded Results
\end{tabular} & clicking on the "View All" option, all test results for that armature serial number will be displayed. \\
\hline \begin{tabular}{l}
Job Number: sunveer \\
Operator's Name: ffgiffifgifff \\
Armature Name: c Number of Bars: 15 \\
Percentage Variance: 20\% \\
Date: 2005/05/05
\end{tabular} & \begin{tabular}{l}
(Displayed here, are all the tests recorded for the specified armature serial number. \\
Note that all the displayed test results were
\end{tabular} \\
\hline Recorded Faults & recorded on the same day, hence only one \\
\hline Emergency Stop on Bar 0 End Of Recorded Results & date appears after the "View All" option.) \\
\hline
\end{tabular}

Directory Path
\(\left[\begin{array}{|l|}\hline \text { Path Propeties } \\ \text { View Default Path } \\ \hline \\ \text { View Selected Path } \\ \hline\end{array}\right.\)

Drive / Network Path
Əc:[PHIL-C]
\begin{tabular}{|l|}
\hline Folders \\
GDocuments and Settings \\
Gcky370 \\
My Documents \\
sun \\
IM.Sc. Design \\
M.Sc Ony \\
data
\end{tabular}
\(\left[\begin{array}{ll}\text { Files } \\ \hline \text { Admin Password Form.frm } & \\ \text { ana.fm } & \\ \text { ana.vbp } & \\ \text { ana.vbw } & \\ \text { ana.2.fm } & \\ \text { Animation.frm } & \\ \text { Animation.vbp } & \\ \text { Animation.vbw } \\ \text { Backup of PCB1.PCB } & \\ \text { Backup of Sheet2.Sch } & \\ \text { binary to interger.frm } & \\ \hline\end{array}\right.\)


\section*{Directory Path}
-Path Propeties
View Default Path

View Selected Path Change Default Path

\section*{Drive / Network Path}
\(\sqsupseteq \mathrm{c}:[\mathrm{PHIL}-\mathrm{C}] \quad \nabla\)
-Folders


-Print Displayed Data
Print

Open File


Exit Program displayed.

By clicking on a specific date, only the results from tests on that date will be
Operator's Name: Sunveer Matadin
Armature Name: b Number of Bars: 10
View Default Path

View Selected Path Change Default Path Drive / Network Path
\(\square \mathrm{c}:[\mathrm{PHIL}-\mathrm{C}]\)
-Folders


Files


\title{
The Design Of An Embedded Controller For An Automated Volt-Drop Test
}

\section*{The Calibration Screen}

The value recorded by the system for this injected value is recorded in the \(2^{\text {nd }}\)


1mv/ \(\Gamma\)
Reading: :22[220mV \(+\uparrow \cdot 1 \mathrm{mV}]\)




\(\qquad\) r
 Reading: \(31[310 \mathrm{~m} / \mathrm{V}+/\) -
displayed in this list box.
\[
\begin{aligned}
& \text { Reading: } 32[320 \mathrm{mV}+/- \\
& \text { Reading: } 33[330 \mathrm{mV}+/-
\end{aligned}
\]
\[
100 \text { successive readings for }
\]
each pair of bars is
displayed in its "raw" from as it is received from the controller.



\title{
The Design Of An Embedded Controller For An Automated Volt-Drop Test
}

\author{
The Microcontroller Software Development Environment
}


\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & 0.17894 & & 02081 & 0.185363 & & & 0.1995 & & \\
\hline 0.171538 & 0.183744 & 0.200181 & 0.190025 & 0.171563 & 0.185588 & 0.1987 & 6 & 0.176869 & 0.1883 \\
\hline & 0.182819 & 0.203 & & & & ． 2056 & & & \\
\hline & 0.171237 & 0.18700 & & & & & & & \\
\hline & & 0.178681 & & & & 0.172263 & ， & & \\
\hline 199513 & 0.176206 & 0.178813 & 0.20018 & & & 0.1867 & 8 & & \\
\hline 03 & & & & & & 0.173894 & & & \\
\hline & & & 0.1 & & & 0.2 & 0.188894 & & \\
\hline 200838 & 0. & 0.172 & & & 0.190575 & 0. & 3 & & \\
\hline 0.194475 & 0.2 & 0. & 0.17288 & 0. & 0. & 0.1719 & & 0.202838 & \\
\hline & 0 & 0.18008 & 0 & 0.19118 & 0.174 & 0.18115 & 0.202212 & 0.191031 & \\
\hline & 0.197744 & 0.200606 & 0 & 0.176606 & 0.198588 & 0.200337 & 9 & & \\
\hline 0.175219 & 0 & 0.201556 & 0.1935 & & 0.176681 & 0.202013 & 0.187931 & & \\
\hline 200506 & 0.190525 & & 0.18900 & & & & 6 & 0.189406 & \\
\hline ． 181406 & 0.2026 & 0. & & & & & 9 & 0.188594 & \\
\hline 0240 & & & & & & & & & \\
\hline 0.2024 & 0. & & & & & & & & \\
\hline & 0.1 & 0.201406 & 0.18 & & & & 1 & 0.176419 & \\
\hline & 0.1825 & & 0.192 & & 0.181406 & 0.173406 & & 0.20175 & \\
\hline & 202 & & & & 0.204088 & & & 0.195019 & \\
\hline 0075 & 0.19 & & & & & & & & \\
\hline 182144 & 0.202713 & & & & & 0.1835 & & & \\
\hline & & & & & & ， & & 0.199913 & \\
\hline 200925 & 0.173913 & & & & & & & 0.183006 & \\
\hline & 0． & 0.2008 & & 0.173 & 201988 & 0.1899 & 0.174425 & 仡 & \\
\hline & 0.1 & & & & & & & & \\
\hline 0.19765 & 0 & & & & & & & 0.205613 & \\
\hline & 0.2 & & & & 0. & & & & \\
\hline 18 & 0.199 & & & & 0.20 & & & & \\
\hline 0.1 & & & 0. & & & & & 0.173944 & \\
\hline & 0.19 & & & & 0.2 & & & & \\
\hline 0.201919 & & & & & & & & 0.199225 & \\
\hline & 0.17 & 0.17 & & & & & & 0.184794 & \\
\hline 199563 & 0.1 & 0.1 & & 0.2 & & 7 & & & \\
\hline 0.194813 & 0.20 & 0.1 & 0.1736 & 0.1958 & ． & ． & ． 172988 & 0.2024 & \\
\hline & 0.174488 & 1755 & 0.20226 & 0.2 & 0.174319 & 0.184813 & 0.200075 & 0.18 & \\
\hline 0.198213 & 0.199006 & 0.17330 & 0.17362 & 0.198 & 0.2003 & ． 17 & 0.179781 & 0.202231 & 0.19 \\
\hline 00813 & 0.18 & 0.17 & 0.188 & 0.2 & 0.181744 & 0.1734 & 2011 & 0.195606 & \\
\hline 0.1855 & 0.203006 & 0.18 & 0.175 & 0.184738 & 0.1998 & 0.183588 & 0413 & 0.1923 & \\
\hline 0.204 & 0.18 & 1732 & ． 1 & 0.200 & 0.1 & 0.175669 & 0.1 & 200 & \\
\hline
\end{tabular}
\(\begin{array}{llllllllll}0.174681 & 0.200888 & 0.1939 & 0.1752 & 0.179606 & 0.201206 & 0.197531 & 0.174144 & 0.176806 & 0.201406\end{array}\) \(\begin{array}{lllllllllll}0.200306 & 0.181431 & 0.172631 & 0.194906 & 0.199988 & 0.1742 & 0.176594 & 0.2003 & 0.197644 & 0.172181\end{array}\) \(\begin{array}{lllllllllll}0.196306 & 0.1719 & 0.177556 & 0.201469 & 0.194425 & 0.1734 & 0.180413 & 0.199831 & 0.193781 & 0.1723\end{array}\) \(\begin{array}{llllllllllll}0.199963 & 0.1819 & 0.176219 & 0.202444 & 0.1979 & 0.173481 & 0.184838 & 0.202306 & 0.189663 & 0.174144\end{array}\) \(\begin{array}{llllllllllllll}0.175806 & 0.192075 & 0.200406 & 0.172994 & 0.1787 & 0.2015 & 0.190788 & 0.172313 & 0.186444 & 0.198594\end{array}\) \(\begin{array}{lllllllllllll}0.199513 & 0.200319 & 0.1687 & 0.185125 & 0.198306 & 0.184813 & 0.173138 & 0.193431 & 0.204644 & 0.1803\end{array}\) \(\begin{array}{llllllllll}0.1896 & 0.201669 & 0.1807 & 0.174638 & 0.19995 & 0.190219 & 0.175994 & 0.190319 & 0.2043 & 0.179344\end{array}\) \(\begin{array}{lllllllllllll}0.200794 & 0.180013 & 0.172731 & 0.198838 & 0.194419 & 0.173406 & 0.179581 & 0.2022 & 0.188038 & 0.175006\end{array}\) \(\begin{array}{lllllllllll}0.172181 & 0.19515 & 0.199488 & 0.175831 & 0.1719 & 0.199488 & 0.1899 & 0.173188 & 0.1914 & 0.203806\end{array}\) \(\begin{array}{llllllllllll}0.172181 & 0.179206 & 0.200738 & 0.1944 & 0.172075 & 0.181613 & 0.202463 & 0.193406 & 0.1717 & 0.1795\end{array}\) \(\begin{array}{llllllllll}0.182869 & 0.201269 & 0.191031 & 0.177219 & 0.187806 & 0.2014 & 0.186438 & 0.174844 & 0.188181 & 0.202438\end{array}\) \(\begin{array}{llllllllll}0.190038 & 0.173406 & 0.201406 & 0.193813 & 0.1752 & 0.183988 & 0.202 & 0.190844 & 0.169281 & 0.1839\end{array}\) \(\begin{array}{llllllllll}0.200813 & 0.1768 & 0.181694 & 0.2007 & 0.1891 & 0.169675 & 0.1864 & 0.198863 & 0.182206 & 0.1723\end{array}\) \(\begin{array}{llllllllll}0.193538 & 0.199806 & 0.173675 & 0.171506 & 0.202206 & 0.1915 & 0.172344 & 0.180025 & 0.2008 & 0.191806\end{array}\) \(\begin{array}{lllllllllll}0.17655 & 0.178281 & 0.200306 & 0.193219 & 0.172306 & 0.1848 & 0.204144 & 0.192413 & 0.170813 & 0.183931\end{array}\) \(\begin{array}{llllllllll}0.171581 & 0.203019 & 0.1932 & 0.169094 & 0.187019 & 0.2019 & 0.190806 & 0.173988 & 0.184725 & 0.199663\end{array}\) \(\begin{array}{lllllllllll}0.188606 & 0.202488 & 0.176694 & 0.176013 & 0.200881 & 0.189788 & 0.171619 & 0.19435 & 0.1995 & 0.177606\end{array}\) \(\begin{array}{lllllllllll}0.198081 & 0.1867 & 0.172025 & 0.193419 & 0.2059 & 0.183106 & 0.172344 & 0.1939 & 0.201206 & 0.1804\end{array}\) \(\begin{array}{llllllllll}0.180619 & 0.202356 & 0.183019 & 0.172944 & 0.196825 & 0.1999 & 0.176381 & 0.175006 & 0.198206 & 0.198438\end{array}\) \(\begin{array}{llllllllll}0.182206 & 0.172044 & 0.196088 & 0.200813 & 0.177406 & 0.173925 & 0.198381 & 0.202281 & 0.172794 & 0.174694\end{array}\) \(\begin{array}{llllllllll}0.1791 & 0.201894 & 0.1889 & 0.176406 & 0.186475 & 0.199894 & 0.189406 & 0.170544 & 0.192888 & 0.200875\end{array}\) \(\begin{array}{lllllllllllll}0.177688 & 0.1768 & 0.1982 & 0.200406 & 0.175362 & 0.175094 & 0.199869 & 0.199413 & 0.174081 & 0.176606\end{array}\) \(\begin{array}{llllllllllll}0.172606 & 0.18075 & 0.200306 & 0.192806 & 0.173625 & 0.191194 & 0.200763 & 0.176213 & 0.1751 & 0.198788\end{array}\) \(\begin{array}{llllllllllll}0.196875 & 0.201212 & 0.179219 & 0.1751 & 0.198263 & 0.197681 & 0.175888 & 0.177206 & 0.202019 & 0.199913\end{array}\) \(\begin{array}{llllllllll}0.1819 & 0.170206 & 0.194394 & 0.2024 & 0.173613 & 0.179819 & 0.203713 & 0.1887 & 0.173138 & 0.188606\end{array}\) \(\begin{array}{llllllllllllll}0.201406 & 0.173644 & 0.19555 & 0.202613 & 0.172825 & 0.184606 & 0.204013 & 0.188481 & 0.172375 & 0.185594\end{array}\) \(\begin{array}{lllllllllll}0.1704 & 0.1971 & 0.200044 & 0.172606 & 0.182981 & 0.203006 & 0.189431 & 0.1707 & 0.186319 & 0.202206\end{array}\) 0.17420 .1838690 .2031690 .1919440 .1713440 .184306 \(\begin{array}{lllllllllll}0.172881 & 0.178194 & 0.205406 & 0.18795 & 0.168288 & 0.193644 & 0.201212 & 0.1778 & 0.178231 & 0.201344\end{array}\) \(\begin{array}{lllllllllll}0.200619 & 0.1742 & 0.178744 & 0.200181 & 0.196 & 0.173625 & 0.175781 & 0.202806 & 0.1879 & 0.1727\end{array}\) \(\begin{array}{llllllllll}0.186713 & 0.1762 & 0.187381 & 0.199388 & 0.187613 & 0.172306 & 0.1894 & 0.200188 & 0.183219 & 0.169\end{array}\) \(\begin{array}{lllllllllll}0.185006 & 0.2011 & 0.1887 & 0.170206 & 0.185506 & 0.199644 & 0.185394 & 0.171506 & 0.198081 & 0.202988\end{array}\) \(\begin{array}{llllllllll}0.1921 & 0.200606 & 0.1715 & 0.1831 & 0.202006 & 0.187 & 0.1752 & 0.194438 & 0.202219 & 0.174206\end{array}\) \(\begin{array}{lllllllllll}0.172075 & 0.201219 & 0.191631 & 0.173638 & 0.183994 & 0.201125 & 0.191006 & 0.173625 & 0.1843 & 0.2028\end{array}\) \(\begin{array}{lllllllllll}0.1743 & 0.189188 & 0.2027 & 0.182175 & 0.173619 & 0.198806 & 0.199606 & 0.1731 & 0.184406 & 0.204938\end{array}\) \(\begin{array}{llllllllll}0.191406 & 0.203394 & 0.18315 & 0.171406 & 0.1915 & 0.202413 & 0.180406 & 0.172438 & 0.200656 & 0.203\end{array}\) \(\begin{array}{lllllllllll}0.173406 & 0.178381 & 0.2003 & 0.1927 & 0.172606 & 0.186006 & 0.200613 & 0.181131 & 0.1731 & 0.1959\end{array}\) \(\begin{array}{lllllllllll}0.179088 & 0.203006 & 0.193638 & 0.1711 & 0.185594 & 0.206 & 0.189594 & 0.175738 & 0.186481 & 0.203606\end{array}\) \(\begin{array}{lllllllllllll}0.178806 & 0.174363 & 0.201269 & 0.192794 & 0.172794 & 0.183913 & 0.202006 & 0.182781 & 0.169025 & 0.192413\end{array}\) \(\begin{array}{lllllllllll}0.1768 & 0.200975 & 0.199169 & 0.172344 & 0.186013 & 0.2018 & 0.192406 & 0.172013 & 0.1864 & 0.202206\end{array}\)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & 0.174206 & & 0.196606 & & & & & 0.2024 & \\
\hline 178838 & 0.2028 & 0.191006 & & 0.184375 & 0.199288 & 0.187088 & 0.172038 & 0.1931 & 0.20405 \\
\hline 0.179806 & 0.201188 & & 0.179806 & & & & & 0.173281 & \\
\hline 0.185563 & 0.2 & & & & & & & 0.178206 & \\
\hline & & 0. & & & & & 0.200356 & & \\
\hline & & & & 0.173681 & & 0. & & & \\
\hline 172719 & 0.19233 & 0.2032 & 0.188 & & & & 0.188438 & 0.175031 & \\
\hline 1883 & 0. & 0.1 & 0.1747 & 0.1 & . & 0. & 5 & 0.1818 & \\
\hline 181888 & 0. & 0. & 0.199338 & 0.1883 & & & 0.202181 & 8 & 0.172794 \\
\hline 020731 & 0. & 0. & 0. & 0.2008 & 0.2026 & 0.175138 & 0.175213 & 3 & \\
\hline 0.182088 & 0 & 0.189619 & 0.199806 & 0.184781 & 0.1759 & & 0.199663 & 6 & \\
\hline 0.2026 & 0 & 0.1702 & 0.191006 & 0.201981 & 0.18647 & & 0.186413 & & \\
\hline 198069 & & 0.178269 & 0.173888 & & 0.2023 & & 0.175219 & 4 & \\
\hline & & 0.201912 & 0. & & 0.17580 & 0.1955 & 0.203925 & 2 & \\
\hline 20060 & & 0.169531 & & 0.202406 & 0. & 0.172606 & & 5 & \\
\hline & & & 0.201219 & & & & & 3 & \\
\hline & & & & & 0.192 & & & & \\
\hline & & 0.2007 & 0.180706 & & 0.190231 & 0.1983 & & , & \\
\hline & & & & & & 0.190894 & 0.200331 & & \\
\hline & & & & & 0.199 & & & 6 & \\
\hline & & & & & & & 0.201737 & & \\
\hline 99806 & 0. & & & & & & & & \\
\hline & & & & & & & 3 & 8 & \\
\hline & & 0 & & & & 0.200819 & & & \\
\hline & 0. & 0 & 0.1900 & , & 0.19026 & 0.16 & 0.18035 & 0.202425 & \\
\hline & & & 0.184838 & 0.200081 & 0.194 & 0.175 & & & \\
\hline 0.1885 & 0 & 0.18 & & 0.193219 & & & 0 & 3 & \\
\hline 200825 & & & & 0.203006 & & & & 3 & \\
\hline & & & & & & & & 199606 & . 190038 \\
\hline & & & & & & & 0. & & \\
\hline 19 & & 0.1 & & & & & & & \\
\hline & & & & & & & & 5 & \\
\hline & & & & & & & & & \\
\hline 186475 & 0.1 & 0.19 & & & & & & 4 & \\
\hline . & 0.17 & 0.1 & 0.20248 & 0. & & 0.176 & 0.198444 & . 200025 & \\
\hline & 0.1740 & .19 & 0.2046 & , & 0.176 & 0.187 & & 90219 & \\
\hline 0.2024 & 0.177238 & 0.1718 & 19820 & 0.200656 & 0.1799 & 0.1 & 0.190 & . 201781 & . 18 \\
\hline 182594 & 0.1 & 0.187819 & 0.201456 & 0.189406 & 0.1 & 0.18 & 0.202019 & 197531 & \\
\hline . 2019 & 0.188144 & 0.175 & 0.187225 & 0.200025 & 0.19021 & 0.172013 & 0.1836 & 0.2036 & \\
\hline 0.191 & 0.1 & . 179 & 0.2 & 0.2008 & 0.1763 & 0.1 & 0.1976 & 203906 & 184406 \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline 0.172025 & 0.1836 & 0.201838 & 0.194713 & 0.175794 & 0.176888 & 0.1991 & 0.198325 & 0.178744 & 0.169 \\
\hline 0.1815 & 0.167 & 0. & 0.199106 & 0. & 0.170775 & 0.186806 & 6 & 0.189625 & 1 \\
\hline 0.203 & 0.189106 & 0.1 & 0.1 & 0.200838 & 0.200406 & 0.173688 & 0.1743 & 0.195906 & 0.204038 \\
\hline 200413 & 0.180025 & 0.174 & 0.1942 & 0.201181 & 0.184231 & 0.174206 & 0.188487 & 0.200413 & 0.190094 \\
\hline 0.175919 & 0.198775 & 0.202438 & 0.170794 & 0.177625 & 0.197906 & 0.200419 & 0.179406 & 0.17355 & 0.201194 \\
\hline 0.201244 & 0.19275 & 0.171 & 0.174525 & 0.199213 & 0.200025 & 0.175581 & 0.172694 & 0.1935 & 0.1986 \\
\hline 0.199106 & 0.189469 & 0.174806 & 0.183375 & 0.202994 & 0.192825 & 0.172238 & 0.17435 & 0.1972 & 0.200606 \\
\hline 0.194394 & 0.174538 & 0.1724 & 0.196463 & 0.204525 & 0.1844 & 0.171531 & 0.187581 & 0.199138 & 0.188013 \\
\hline 0.183087 & 0.20291 & 0.1972 & 0.175606 & 0.17495 & 0.2008 & 0.201419 & 0.177975 & 0.170488 & 0.188381 \\
\hline 0.174481 & 0.172988 & 0.202 & 0.193681 & 0.174206 & 0.173688 & 0.198806 & 0.204 & 0.183113 & 0.172094 \\
\hline 0.18041 & 0.2 & 0.2 & 0. & 0.172725 & 0. & 0.2055 & 0.184025 & 4 & 0.185531 \\
\hline 0.173 & 0.17 & 0. & 0.195531 & 0.1747 & 0.176413 & 0.197206 & 0.204488 & 0.180381 & 0.170744 \\
\hline 0.18543 & 0.1 & 0. & 0.203919 & 0.1 & 0.1 & 0. & 0.203387 & 0.1855 & 0.1746 \\
\hline 0.1934 & 0.20300 & 0.1 & 0.1766 & 0.184706 & 0.204606 & 0.1 & 0.172788 & 0.175556 & 0.200075 \\
\hline 0.1735 & 0.1 & 0.1999 & 0.20 & 0.178819 & 2 & 0.196 & 0.206281 & 0.185206 & 0.176606 \\
\hline 0.200419 & 0.188 & 0.17 & 0.1 & 0.201406 & 0.192831 & 0.175219 & 0.184038 & 0.201206 & 0.1927 \\
\hline 0.2004 & 0.17 & 0.174 & . & 0.204406 & 0.183894 & 2 & 0.189625 & 200606 & 0.189006 \\
\hline 0.206219 & 0.187563 & 0.17 & 0.1916 & 0.2019 & 0.179381 & 0.170963 & 0.192144 & 0.2031 & 0.182394 \\
\hline 0.186406 & 0.199131 & 0.18998 & 0.1739 & 0.178475 & 0.2019 & 0.1947 & 0.1 & 0.175325 & 0.1947 \\
\hline 0.1755 & 0.1752 & 0.20280 & 0.191606 & 0.1722 & 0.1868 & 0.2038 & 0.1767 & 0.174788 & 0.204413 \\
\hline 0.173294 & 0.197981 & 0.20139 & 0.1814 & 0.1683 & 0.189075 & 0.198981 & 0.189825 & 0.170706 & 0.18085 \\
\hline 0.1903 & 0.175638 & 0.176606 & 0.199225 & 0.2003 & 0.177188 & 0.1739 & 0.195106 & 0.2035 & 1844 \\
\hline 174231 & 0.196794 & 0.19913 & 0.174806 & 0.175031 & 0.1983 & 0.2012 & 0.1815 & 0.167588 & 0.1867 \\
\hline 0.187294 & 0.199831 & 0.189181 & 0.172606 & 0.182819 & 0.200337 & 0.195594 & 0.174188 & 0.176619 & 0.196387 \\
\hline 0.176606 & 0.177219 & 0.20206 & 0.197888 & 0.174269 & 0.177219 & 0.1947 & 0.2 & 0.183219 & 0.173638 \\
\hline 0.1787 & 0.174713 & 0.199006 & 0.202994 & 0.1734 & 0.174425 & 0.196094 & 0.196706 & 0.1747 & 0.1747 \\
\hline 0.180013 & 0.19993 & 0.1955 & 0.172488 & 0.175281 & 0.2003 & 0.20235 & 0.177806 & 0.174206 & 0.194419 \\
\hline 0.172994 & 0.176281 & 0.2019 & 0.200606 & 0.1794 & 0.171 & 0.189081 & 0.1982 & 0.186944 & 0.17355 \\
\hline 0.171113 & 0.185213 & 0.2007 & 0.197481 & 0.174781 & 0.173581 & 0.194988 & 0.2019 & 0.18355 & 0.177419 \\
\hline 0.196681 & 0.190206 & 0.17356 & 0.181638 & 0.202969 & 0.200606 & 0.179806 & 0.169294 & 0.193444 & 0.202306 \\
\hline 0.193 & 0.172638 & 0.17190 & 0.196306 & 0.198331 & 0.1784 & 0.1718 & 0.1915 & 0.201806 & 0.188313 \\
\hline 0.175344 & 0.195913 & 0.20390 & 0.1863 & 0.174306 & 0.187881 & 0.199613 & 0.189625 & 0.17045 & 0.181325 \\
\hline 0.204 & 0.1859 & 0.175806 & 0.186013 & 0.2028 & 0.1899 & 0.1731 & 0.1822 & 0.2024 & 0.192306 \\
\hline 0.184081 & 0.20398 & 0.1912 & 0.1738 & 0.178344 & 0.19838 & 0.201 & 0.179913 & 0.171806 & 0.1912 \\
\hline 0.1711 & 0.190194 & 0.198775 & 0.189944 & 0.172981 & 0.186419 & 0.2027 & 0.1907 & 0.174425 & 0.174019 \\
\hline 0.186019 & 0.2056 & 0.1916 & 0.174281 & 0.181406 & 0.198506 & 0.202019 & 0.179619 & 0.171581 & 0.1922 \\
\hline 0.176044 & 0.184306 & 0.204406 & 0.191613 & 0.173531 & 0.177213 & 0.1991 & 0.2014 & 0.180413 & 0.173212 \\
\hline 0.172313 & 0.193406 & 0.206256 & 0.183788 & 0.174819 & 0.189663 & 0.199638 & 0.189619 & 0.173675 & 0.187238 \\
\hline 0.176981 & 0.172675 & 0.191606 & 0.1991 & 0.187931 & 0.172 & 0.184994 & 0.2024 & 0.195019 & 0.172494 \\
\hline 0.173619 & 0.187513 & 0.203113 & 0.1892 & 0.173475 & 0.180981 & 0.201219 & 0.186706 & 0.175 & 0.195188 \\
\hline
\end{tabular}
\(\begin{array}{llllllllll}0.1896 & 0.195906 & 0.191 & 0.17195 & 0.185394 & 0.202406 & 0.192819 & 0.173 & 0.1794 & 0.2006\end{array}\) \(\begin{array}{llllllllll}0.182344 & 0.19955 & 0.198525 & 0.174269 & 0.176706 & 0.2005 & 0.198269 & 0.177244 & 0.175544 & 0.195981\end{array}\) \(\begin{array}{lllllllllll}0.182288 & 0.172144 & 0.1918 & 0.1985 & 0.187725 & 0.175806 & 0.187 & 0.200381 & 0.191894 & 0.173975\end{array}\) \(\begin{array}{lllllllllll}0.173738 & 0.1827 & 0.2027 & 0.195019 & 0.174206 & 0.1798 & 0.202006 & 0.200238 & 0.1752 & 0.175281\end{array}\) \(\begin{array}{lllllllllll}0.196656 & 0.171844 & 0.175794 & 0.200038 & 0.199594 & 0.178219 & 0.175288 & 0.196925 & 0.2008 & 0.1779\end{array}\) \(\begin{array}{llllllllll}0.184887 & 0.173625 & 0.188719 & 0.2006 & 0.1871 & 0.173106 & 0.1815 & 0.203806 & 0.198394 & 0.176819\end{array}\)
\(\begin{array}{llllllllll}0.1794 & 0.170275 & 0.1899 & 0.200363 & 0.1892 & 0.172281 & 0.1851 & 0.201406 & 0.192994 & 0.173469\end{array}\) \(\begin{array}{lllllllllll}0.174125 & 0.185194 & 0.20075 & 0.193106 & 0.1723 & 0.192138 & 0.199669 & 0.189406 & 0.173244 & 0.185419\end{array}\) \(\begin{array}{lllllllllll}0.202063 & 0.18325 & 0.175938 & 0.185788 & 0.2019 & 0.1887 & 0.172144 & 0.177944 & 0.200388 & 0.201581\end{array}\)
\(\begin{array}{llllllllll}0.1863 & 0.1995 & 0.1891 & 0.170231 & 0.187119 & 0.201125 & 0.191006 & 0.176681 & 0.186713 & 0.198331\end{array}\) \(\begin{array}{lllllllllll}0.201144 & 0.190231 & 0.172525 & 0.190006 & 0.197994 & 0.188694 & 0.176606 & 0.186219 & 0.2027 & 0.190438\end{array}\) \(\begin{array}{llllllllll}0.187225 & 0.198813 & 0.1898 & 0.1699 & 0.184838 & 0.202413 & 0.1921 & 0.172788 & 0.173188 & 0.195969\end{array}\) \(\begin{array}{lllllllllll}0.185175 & 0.203806 & 0.192419 & 0.173194 & 0.178563 & 0.2006 & 0.199194 & 0.178206 & 0.175744 & 0.202013\end{array}\) \(\begin{array}{lllllllllll}0.200406 & 0.175706 & 0.1729 & 0.191881 & 0.2035 & 0.1811 & 0.168888 & 0.190269 & 0.199238 & 0.189638\end{array}\) \(\begin{array}{llllllllll}0.186363 & 0.202256 & 0.188894 & 0.171081 & 0.183606 & 0.200875 & 0.19435 & 0.171194 & 0.173131 & 0.197156\end{array}\)
\(\begin{array}{llllllllll}0.1752 & 0.17495 & 0.2022 & 0.200606 & 0.180144 & 0.174325 & 0.197113 & 0.201238 & 0.181219 & 0.171019\end{array}\) \(\begin{array}{llllllllll}0.171669 & 0.185481 & 0.201638 & 0.1926 & 0.173888 & 0.17995 & 0.199106 & 0.203006 & 0.1755 & 0.175019\end{array}\) \(\begin{array}{lllllllllll}0.173894 & 0.187619 & 0.199244 & 0.190806 & 0.171006 & 0.180388 & 0.199513 & 0.200306 & 0.177638 & 0.172606\end{array}\) \(\begin{array}{llllllllll}0.201613 & 0.180025 & 0.1726 & 0.192144 & 0.1991 & 0.190444 & 0.174438 & 0.185688 & 0.201681 & 0.192631\end{array}\) \(\begin{array}{lllllllllll}0.191344 & 0.173238 & 0.1735 & 0.198388 & 0.197406 & 0.172606 & 0.171538 & 0.196075 & 0.200075 & 0.176206\end{array}\) \(\begin{array}{lllllllllll}0.202006 & 0.2014 & 0.1755 & 0.174438 & 0.195038 & 0.204419 & 0.186006 & 0.172544 & 0.191744 & 0.203613\end{array}\) \(\begin{array}{lllllllllll}0.175613 & 0.1892 & 0.200825 & 0.188744 & 0.172788 & 0.1864 & 0.203806 & 0.192819 & 0.175219 & 0.178081\end{array}\) \(\begin{array}{lllllllllll}0.19975 & 0.1883 & 0.173613 & 0.1871 & 0.1985 & 0.189625 & 0.173212 & 0.183869 & 0.1995 & 0.1947\end{array}\) \(\begin{array}{llllllllll}0.202588 & 0.1787 & 0.171225 & 0.1928 & 0.200706 & 0.1851 & 0.174544 & 0.186013 & 0.201488 & 0.188081\end{array}\) \(\begin{array}{lllllllllll}0.188606 & 0.2024 & 0.1916 & 0.175031 & 0.177675 & 0.202713 & 0.2024 & 0.177469 & 0.172606 & 0.195106\end{array}\) \(\begin{array}{llllllllll}0.197581 & 0.199275 & 0.180025 & 0.175619 & 0.197244 & 0.2011 & 0.179194 & 0.170819 & 0.188744 & 0.199288\end{array}\) \(\begin{array}{llllllllllll}0.202037 & 0.188606 & 0.176812 & 0.1855 & 0.203613 & 0.190869 & 0.171619 & 0.179394 & 0.201394 & 0.192813\end{array}\) \(\begin{array}{llllllllll}0.185144 & 0.204038 & 0.189531 & 0.1723 & 0.183606 & 0.1995 & 0.1974 & 0.173638 & 0.175744 & 0.194738\end{array}\)
\(\begin{array}{lllllllllll}0.1848 & 0.202688 & 0.191588 & 0.173406 & 0.178481 & 0.20075 & 0.198269 & 0.175619 & 0.177406 & 0.197594\end{array}\)
\(\begin{array}{lllllllllll}0.1857 & 0.176819 & 0.186413 & 0.2026 & 0.187906 & 0.170869 & 0.1835 & 0.203344 & 0.187969 & 0.170425\end{array}\) \(\begin{array}{lllllllllll}0.172181 & 0.186306 & 0.199288 & 0.191006 & 0.170844 & 0.1823 & 0.2015 & 0.200038 & 0.172981 & 0.175225\end{array}\) \(\begin{array}{lllllllllll}0.200894 & 0.2003 & 0.176406 & 0.1727 & 0.197625 & 0.201406 & 0.179213 & 0.170081 & 0.191619 & 0.199238\end{array}\) \(\begin{array}{llllllllll}0.173794 & 0.174356 & 0.1982 & 0.201775 & 0.184419 & 0.175806 & 0.1859 & 0.1987 & 0.1891 & 0.169944\end{array}\) \(\begin{array}{llllllllll}0.199806 & 0.190163 & 0.168769 & 0.180094 & 0.201231 & 0.201687 & 0.1743 & 0.174475 & 0.196825 & 0.200731\end{array}\) \(\begin{array}{llllllllll}0.198206 & 0.2026 & 0.181194 & 0.171813 & 0.1883 & 0.201319 & 0.190219 & 0.173094 & 0.181625 & 0.201406\end{array}\) \(\begin{array}{lllllllllll}0.201219 & 0.1855 & 0.174425 & 0.186544 & 0.203806 & 0.191406 & 0.174806 & 0.179806 & 0.202013 & 0.201125\end{array}\) \(\begin{array}{llllllllll}0.190812 & 0.1999 & 0.1875 & 0.173294 & 0.184025 & 0.201037 & 0.195931 & 0.1752 & 0.173013 & 0.197988\end{array}\) \(\begin{array}{llllllllll}0.202019 & 0.1918 & 0.172038 & 0.176888 & 0.199619 & 0.200713 & 0.178425 & 0.173613 & 0.191881 & 0.200731\end{array}\) \(\begin{array}{llllllllll}0.177244 & 0.201344 & 0.201319 & 0.178325 & 0.1695 & 0.1871 & 0.201806 & 0.1896 & 0.174369 & 0.179606\end{array}\) \(\begin{array}{lllllllllll}0.205613 & 0.187225 & 0.174813 & 0.18395 & 0.202037 & 0.195169 & 0.174088 & 0.1747 & 0.198675 & 0.201406\end{array}\)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & 0.1736 & & & & & & & & \\
\hline 0.203088 & 0.181625 & 0.169406 & & 0.201406 & & 0.173381 & 0.182606 & 0.202231 & \\
\hline & 0.202406 & 0.19979 & 0.173625 & & 0.196013 & & 0.1783 & & \\
\hline & 0.203006 & 0.1807 & & & & 0.189688 & 0.171806 & 0.183288 & \\
\hline & & 0.19682 & & & & & & & \\
\hline & 0.195806 & 0.201538 & & & 0. & & . & & \\
\hline & 0.197806 & 0.20380 & 0.180769 & & & & 0.189613 & & \\
\hline . 2015 & & 0. & & & & & & . & \\
\hline 19 & 0. & & & & & & 0.202706 & & \\
\hline 0.18675 & 0. & 0.183 & 0.200781 & 0. & 0. & & 0. & 0.2 & \\
\hline 0.171956 & 0. & 0. & 0. & 0 & 0.171 & 0. & 0. & & 0.17 \\
\hline 0.200419 & 0. & 0. & 0.194412 & 0.203 & 0.185456 & 0.175588 & 0.188013 & 0.200144 & \\
\hline 0.1963 & 0. & 0 & 0.200419 & 0.199806 & 0.1768 & 0.175819 & 0.198219 & 0.198594 & \\
\hline 171494 & & 0.202 & & 0.172881 & 0.183213 & 0.201325 & 0.200038 & 0.177244 & \\
\hline & 0 & 0.172 & 0.194806 & 0.201394 & 0.18155 & 0.1671 & 0.194994 & 0.200581 & \\
\hline 0.189606 & 0.1 & 0.189625 & & & 0.202438 & 0.196406 & & 0.175206 & \\
\hline 196025 & 0.2 & & 0.1 & . & 0. & 0.183194 & 0. & 0.1879 & \\
\hline 195806 & 0. & 0.1836 & & & 0.2044 & 0.1 & 0. & 0.17615 & 0.20 \\
\hline & & & & & & 0.200144 & & 0.175 & \\
\hline & & & & & & & & 0.176825 & \\
\hline & & & & & & & & & \\
\hline & & 0.175 & & & & 0.185156 & & 0.184181 & \\
\hline & 0. & & & & & & & & \\
\hline 0.172694 & & & & & & 0.198006 & 0.204013 & 0.183006 & \\
\hline - & & 0.17666 & 0.188606 & & & & 0.185588 & & \\
\hline & & 0.18260 & & 0.19608 & & 0.174544 & 0.197419 & 0.205738 & \\
\hline 0.1707 & . 184 & & & . 173888 & & 0.201181 & 995 & & \\
\hline 0.200306 & & 0. & & & & & & & \\
\hline 0.2006 & 0.1 & 0.173 & & 0. & 0.1 & & & & \\
\hline & 0.20 & & & & 0. & 0.20 & & & \\
\hline & 0.202 & 0.18 & & & & 0.193 & & 0.174044 & 0.19 \\
\hline 0.189913 & & & & & 0.17 & & & - & \\
\hline 0.182325 & 0.20 & & & & & 0.19 & & & \\
\hline & & & 0. & & & & & & \\
\hline 0.199606 & & & & 0.2 & 0.18 & & & & \\
\hline 0.178419 & 0.171 & 0.19 & 0.205 & & 0.176 & 0.185406 & 0.2028 & 0.191969 & \\
\hline 01206 & 0.18192 & 0. & 0.1884 & 0.2 & 0.1911 & 0.1723 & 0.1787 & 0.1982 & \\
\hline 89206 & 0.17338 & 0.18641 & 0.202813 & 0.196719 & 0.1768 & . 17 & 0.195 & 0.204025 & \\
\hline 0.201387 & 0.201163 & 0.17442 & 0.1732 & 0.194856 & 0.204363 & 0.1846 & . 175588 & 9 & \\
\hline 0.182069 & 0.1689 & 0.187 & 0.2000 & 0.1 & 0.17185 & 0.18 & . 20 & 0.192706 & 0.174 \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & 0.199225 & 0.190206 & 0.1726 & 0.182475 & 0201113 & 0.18715 & 0.178 & 0.186181 & 0.1974 \\
\hline & & & 0.199819 & 0.180094 & & 0.1 & 0.206306 & 0.181581 & \\
\hline & & & & & & & & & \\
\hline & & & & & & & & & \\
\hline 0.202281 & 0.186 & 0.17 & 0.18 & 0.2 & 0.19 & 0.1715 & 0.1799 & & \\
\hline & 0. & & & & & & & & \\
\hline & & & & & & & & & \\
\hline & & & & & & & & & \\
\hline 0.185 & 0.2022 & 0.19 & 0.1 & & 0.2 & 0.201006 & 0.174819 & 0.174606 & \\
\hline & 0. & 0360 & & & & & & & \\
\hline & 0.20 & & & & & & & & \\
\hline . 75 & 0. & 0. 201 & 0.19 & & 0.1 & & . 1963 & & \\
\hline & 0.1 & 0.199 & 0.18 & 0.175 & & & 0.189688 & & \\
\hline & & & & & & & & & \\
\hline . 68 & 0.1911 & 0.19923 & 0.189 & 0.17 & 0.18 & & 0.191006 & & \\
\hline & 0.1 & 0.1723 & & 0.203069 & 0.18 & & & 0.200781 & 0.172394 \\
\hline & 0.1 & 0.186463 & & & & & & & \\
\hline & & & & & & & & & \\
\hline 0.194781 & 0.2015 & 0.184 & & & 0.203 & & & & \\
\hline 0.206013 & 0.1 & & & & 0.19 & & & & \\
\hline & 0.202 & & & & 0.202 & & & & \\
\hline & & & & 0.200 & & & & & \\
\hline & 0.2018 & 0.200825 & & 0.17 & & & & & \\
\hline & 0.20241 & & & & 0.202 & & & & \\
\hline & 0. & & & & & & & & \\
\hline & & & & & & & & & \\
\hline & & & & & . & & & & \\
\hline & 0.174 & & & 0.178 & & & & & \\
\hline & & & & & & & & & \\
\hline & 0.1 & 0.17 & 0.18 & & 0. & & 0.186206 & . 2 & \\
\hline & 0.18 & 0.17443 & & & & & & 0.201488 & \\
\hline & 0.193 & & & & 0.185 & & & & \\
\hline & 197 & & & & & & & & \\
\hline & 0.19 & 0.2 & 0.183 & 0.1 & 0.186 & 0.206013 & 0.19 & 0.172894 & \\
\hline & 0.17878 & 9958 & 0.200 & 0.178463 & . & & 0.20 & & \\
\hline 206 & 0.199525 & 0.20242 & 0.1763 & & 0.1970 & 0.206 & & & \\
\hline & 0.17320 & 1023 & & & & & & & \\
\hline 0.175006 & 0.185913 & 0.204025 & 0.191538 & 0.17 & 0.173925 & 0.2019 & 0.194425 & 0.174863 & \\
\hline & 0.172 & 0.179213 & 0.20 & 0.20 & 0.17 & 0.171237 & & & \\
\hline 17 & 0.19 & 0.201281 & & & 0.18 & & & & \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & & & & & & & & & \\
\hline 0.187281 & 0.201231 & 0.1902 & 0.175006 & 0.1 & 0.1 & 0.1975 & 0.175269 & 5 & \\
\hline 0.172731 & 7 & 0.20 & 0.1 & 0. & 0. & 0.198537 & 0.2012 & 6 & \\
\hline & 0.1966 & 0.2028 & 0.1819 & & & 0. & 0.190812 & & \\
\hline & & 0.192756 & 0.200413 & & & 0.1902 & & & \\
\hline & 0 & 0 & 0.1979 & 0.174475 & 0.173688 & 0.196825 & 0.204025 & 0.182219 & \\
\hline & & & 0.204388 & & & & & & \\
\hline & 0.201963 & 0.19484 & & 0.1723 & & & & & \\
\hline & 0.183819 & 0.175606 & 0.188631 & & & & 0.185406 & & \\
\hline 203806 & 0.1 & 0.175 & 0.1767 & 0.201806 & & 0.178413 & 6 & 0.199806 & \\
\hline 196606 & & 0. & 0.197625 & 0.2 & 0.178325 & 0. & 0.1915 & 0.199 & \\
\hline 96306 & 0.204488 & 0.1815 & 0.173188 & & & 0.1912 & 0.168506 & . 18 & \\
\hline 0.2031 & & 0.17289 & 0. & 0.20100 & & 0.170575 & 0.183213 & . 19969 & \\
\hline 93 & & 0.1 & 0. & 0.1995 & 0. & 0.1791 & 0.2022 & 3 & 0.173506 \\
\hline 0.20 & 0. & & 0. & 0. & 0. & 0. & 0.175238 & 6 & . 2018 \\
\hline 172444 & 0. & 0. & 0. & 0 & 0. & 0 & 0.193 & & \\
\hline & & 0 & & 0 & & 0.193338 & & & \\
\hline 190819 & 0 & & 0.201806 & & 0.176863 & & 0.192813 & 0.203238 & \\
\hline 0.1964 & 0.1 & 0. & 0.197813 & & 0.180013 & 0.172406 & 0.192219 & 0.199794 & \\
\hline 176981 & 0. & 0. & 0.205 & 0. & 0. & 0.18 & 0.196756 & 0.183956 & \\
\hline 199594 & 0.17 & 0. & 0.195288 & 0.204406 & 0.1 & 0. & 0.188538 & 0.200825 & 0.189725 \\
\hline 1689 & 0.184 & . 2007 & 0. & 0.17560 & 0.17 & 0. & 0.198738 & 0.176881 & \\
\hline 0.1 & 0.1 & & 0.183606 & 0.201538 & 0.197 & 0.17355 & & 0.1951 & \\
\hline 206 & 0. & & & & & & & & \\
\hline & & & & & & & 0. & & \\
\hline & 0.2 & & & & & & & & \\
\hline & 0. & & 0.201 & & & & & & \\
\hline & 0. & 0. & 0.1 & 0.180469 & & 0. & 0.180144 & 0.170788 & \\
\hline & 0.2 & 0.184825 & 0.1772 & 0.186019 & 0.200719 & 0.1907 & 0.173106 & 0.175781 & \\
\hline 3819 & 0.175738 & 0.197613 & 0.2060 & 0. & 0 & 0. & 00125 & 0.191619 & \\
\hline 7125 & 0. & 0.1926 & 0.197106 & 0.188 & 0. & 0.1827 & 0.20148 & 0.197431 & \\
\hline 02013 & 0.20285 & 0.1 & 0. & 0. & 0.200 & 885 & 0.17586 & 0.18553 & . 20413 \\
\hline 69 & 0.1780 & 0. & 42 & 0.2033 & & 92 & 0.188487 & . 19939 & 0. 19036 \\
\hline 15 & 0.1 & 0.1758 & 85 & 0.2007 & 0.1 & 0.173219 & 0.1803 & 0.1992 & . 20079 \\
\hline & 0.20 & 0.1 & 0. & & 0.1 & 0. & 0. & 0.173638 & \\
\hline 0.204 & 0.1 & 0.1 & 0.175 & 0.200 & & & 0.1 & 0.1922 & \\
\hline 0.17 & 0.20 & 0.2 & 0.17 & 0. & 0.19 & 0. & 0. & 0.175263 & 0.185113 \\
\hline 0.1 & 0.202425 & 0.1798 & 0.1719 & 0.189938 & 0.2028 & 0. & 0. & 0.185688 & 0.202675 \\
\hline 174425 & 0.18 & 0.2017 & 0.19 & 0.175806 & 0.17 & 0. & 0.205406 & 0.1827 & \\
\hline 0.1999 & . 1 & 0.180025 & 0.168556 & 0.1913 & 0.200 & 0.188038 & 0.171156 & . 185269 & 0 \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & & 0.1975 & 0.17368 & 0.176063 & & & & & \\
\hline & 0.172381 & 0.176838 & 0.195875 & 0.199538 & & 0.1675 & 0.1891 & 0.201269 & 0.185581 \\
\hline & 0.200813 & 0.188606 & & & 0.202544 & 0． & 0.172694 & & 0.200888 \\
\hline & 0． & & & & & & & & \\
\hline 0.187119 & 0.2035 & & & & & 0.195138 & & & \\
\hline & 㖪 & 0.189406 & & & & 0.189625 & & & \\
\hline 18785 & & & 0.17190 & & & & & & \\
\hline 0.201244 & 0.18 & & & & & & & & \\
\hline & 0. & 0. & 0.2 & 0. & 0. & & 0.2 & 0.185906 & \\
\hline 178206 & 0. & 0. & 0. & 0.1815 & 0. & 0. & 0.199238 & 0.189619 & \\
\hline & 0. & 0. & 0.18908 & 0.173006 & 0.1807 & 0.203006 & 0.197419 & & \\
\hline & 0 & 0.183806 & 0.203169 & 0.192831 & 0.1732 & & 0.200013 & 5 & \\
\hline & 0.1766 & 0.1992 & 0.20065 & 0.176075 & 0.173506 & 0.198194 & 0.2019 & 0.18155 & \\
\hline & 0 & & & & & 0.202438 & 0.188406 & 0.173975 & \\
\hline 0.191606 & 0. & & 0.1995 & 0.200606 & & & & & \\
\hline & 0 & & & & & & & & \\
\hline & & & & & & & & 0.202988 & \\
\hline & 0.185188 & 0.201638 & & & & & 0.200619 & & \\
\hline & 0.1 & 0.20 & & & & 0.198806 & & & \\
\hline & & & & & & 0.201219 & & & \\
\hline & 0. & & & & & & ， & & \\
\hline & 0. & & & & & & & & \\
\hline & 0. & 0.188038 & 0.19990 & & & 0 & & & \\
\hline & 0. & & & & & & 7625 & & \\
\hline & 0.187 & 0.1758 & 0.183556 & 0.204 & & 0.174 & 75806 & & \\
\hline & 0.175606 & 0．1 & 0. & & & & & & 0.190206 \\
\hline & 0.201525 & 0.107 & 0.1 & & & & & & \\
\hline 0.199006 & 0. & ． 1 & & 0.2 & & & & & 0.20128 \\
\hline & & 0.16 & 0.18 & & & & 0.18 & 0.172075 & \\
\hline & 0.2 & & 0.17 & & & & & & \\
\hline & & 0.2 & & & & & & & \\
\hline & & & & & & & & & \\
\hline ． 170 & & & & & & & & & \\
\hline ． 177406 & 0.1 & 0 & & & & & & & \\
\hline 0．199 & 0.17 & 0.1708 & & 0.200 & & 0.171 & 0.184138 & ． 2 & \\
\hline 0.18825 & 0. & 0.1847 & 0.202438 & 0.1 & 0. & 0. & 0.200606 & 0.201744 & 0.173581 \\
\hline 205419 & 0.1 & ．17 & 0. & 0. & 0. & 0.173125 & ， & 0.199913 & \\
\hline & 0.172706 & 0.177788 & 0.20220 & 0.20082 & 0.1786 & 0.173806 & 0.1912 & 0.20139 & \\
\hline 86806 & 0.203562 & 0.193219 & 0.173 & 0.1741 & 0.198219 & 0.2015 & 0.180694 & 0.168494 & \\
\hline ． 193194 & 0.17255 & 0.17740 & ． 2004 & 0.1 & 0.1 & 0.16935 & 0.1885 & 0.2006 & \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & 0.19 & 18 & & & & & 0. 1753 & 0.185194 & \\
\hline & 0.18 & 0.202 & 0.19 & 0.173613 & 0.180025 & 0.202219 & 0.197631 & 0.1743 & \\
\hline & 0.173638 & & & & & & 0.187613 & & \\
\hline & & & & & & & & & \\
\hline 0.199 & 0.1 & & & & & & & & \\
\hline 201 & 0.176 & 0.170 & 0.19 & 0.20 & 0.178706 & 0.171225 & . 1 & 0.204606 & \\
\hline 20007 & 0.180 & & 0.19 & & & & & & \\
\hline & & & & & & & & & \\
\hline & & 0.189 & & & & & & & \\
\hline 0.18681 & 0.20 & 0.1891 & 0.1 & 0.181 & 0.2 & . 20 & 0.170475 & & \\
\hline & 0. & 0.18321 & 0.17453 & . 186 & 0.19 & 0.18 & & & \\
\hline & & & & & & & & & \\
\hline & & & & & & & & & \\
\hline 20402 & & 0.1 & 0.18162 & . 008 & & 0. & 0.174613 & & \\
\hline & 0.188 & & & & & & & & \\
\hline & & & 0.20 & & & & & & \\
\hline & 0. & 0.2 & & & & 0.204781 & 0.181681 & 0.168894 & \\
\hline & 0. & & & & & & & & \\
\hline & & & & & & & & & \\
\hline & 0.186 & & 0.18 & & 0.18 & & & & \\
\hline & 0.205 & 0. & & & & & & 33 & . 203244 \\
\hline & 0.17 & & & & & & & & \\
\hline & 0.2012 & & 0,179 & & & & & & \\
\hline & 0.2 & 0.18412 & 0.17638 & 0.18 & & 0.19 & 0.1748 & 0.173 & \\
\hline & 0.17045 & 0.188944 & 0.2003 & & & 0.185 & 0.201113 & & \\
\hline & & & & & & & & & \\
\hline & 0.19100 & & . 18 & & & & & & \\
\hline & 0.169 & 0.188 & 0.2008 & 0.1 & 0.172281 & 0.1 & 0.20068 & 0.200631 & \\
\hline & & & , & 2 & & 0.172694 & & & \\
\hline & 0.18208 & & 0.185 & & & & & & \\
\hline & & & & & & & & & \\
\hline & 0.1 & & 0.19 & & & 0.1951 & 0.2008 & 18 & \\
\hline & & & . & & & & & & \\
\hline & 0.1 & & & & & & & & \\
\hline & 0.172 & & , & 0.1 & & 0.187 & & & \\
\hline & 0.192 & & 0.1867 & & & & & & \\
\hline & 0.1 & & 0.20060 & 0.19 & & & & & \\
\hline & & & & & & & & & \\
\hline & 0.19 & 0. & 0. & 0.2 & 0.203019 & 0.172706 & 0. & 0.1964 & \\
\hline 173594 & 0.1 & 0.20200 & 0.1991 & 0.174425 & & 0.195588 & 0.205625 & 0.1823 & \\
\hline
\end{tabular}
\begin{tabular}{|c|c|}
\hline 0.187461 & 0.187412 \\
\hline 0.187057 & 0.187412 \\
\hline 0.18747 & 0.187412 \\
\hline 0.187408 & \\
\hline 0.187291 & \\
\hline 0.187247 & \\
\hline 0.187497 & \\
\hline 0.187049 & \\
\hline 0.1874 & \\
\hline 0.187308 & \\
\hline 0.187454 & \\
\hline 0.187196 & \\
\hline 0.187217 & \\
\hline 0.187707 & \\
\hline 0.18727 & \\
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\hline 0.18751 & \\
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\hline 0.187458 & \\
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\hline 0.187903 & \\
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\hline 0.187163 & \\
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\hline 0.187493 & \\
\hline 0.187667 & \\
\hline 0.187488 & \\
\hline 0.187586 & \\
\hline 0.18765 & \\
\hline 0.187708 & \\
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\end{tabular}
\(\begin{array}{lllllllllll}0.199563 & 0.178944 & 0.180944 & 0.200813 & 0.185363 & 0.193806 & 0.177512 & 0.1995 & 0.197625 & 0.174088\end{array}\) \(\begin{array}{lllllllllll}0.171538 & 0.183744 & 0.200181 & 0.190025 & 0.171563 & 0.185588 & 0.1987 & 0.186706 & 0.176869 & 0.1883\end{array}\)
\(\begin{array}{llllllllll}0.1727 & 0.182819 & 0.203 & 0.191444 & 0.1735 & 0.181775 & 0.2056 & 0.1795 & 0.175606 & 0.196194\end{array}\) \(\begin{array}{llllllllll}0.190256 & 0.171237 & 0.187006 & 0.201838 & 0.179819 & 0.176413 & 0.2007 & 0.1974 & 0.171981 & 0.184763\end{array}\)
\(0.19350 .2070060 .1786810 .1742060 .1972190 .2003130 .1722630 .1740190 .201325 \quad 0.1891\) \(\begin{array}{llllllllll}0.199513 & 0.176206 & 0.178813 & 0.200181 & 0.194756 & 0.170788 & 0.1867 & 0.1998 & 0.180944 & 0.172713\end{array}\) \(\begin{array}{lllllllllllllllll}0.203619 & 0.182475 & 0.170231 & 0.1947 & 0.201694 & 0.178106 & 0.173894 & 0.201513 & 0.191006 & 0.175225\end{array}\)
\(\begin{array}{llllllllll}0.1775 & 0.172544 & 0.1976 & 0.198525 & 0.172263 & 0.1795 & 0.204438 & 0.188894 & 0.173775 & 0.191494\end{array}\) 0.2008380 .1939630 .1726060 .1842440 .2018130 .1905750 .17321200 .19030 .2060190 .178325 \(\begin{array}{llllllllllll}0.194475 & 0.202813 & 0.177938 & 0.172881 & 0.199225 & 0.202394 & 0.1719 & 0.1738 & 0.202838 & 0.198019\end{array}\) \(\begin{array}{llllllllllll}0.194206 & 0.174044 & 0.180081 & 0.199994 & 0.191181 & 0.174 & 0.18115 & 0.202212 & 0.191031 & 0.173788\end{array}\) \(\begin{array}{llllllllll}0.17555 & 0.197744 & 0.200606 & 0.178806 & 0.176606 & 0.198588 & 0.200337 & 0.174019 & 0.1811 & 0.203125\end{array}\) \(\begin{array}{llllllllllll}0.175219 & 0.177638 & 0.201556 & 0.1935 & 0.171831 & 0.176681 & 0.202013 & 0.187931 & 0.1755 & 0.195406\end{array}\) \(\begin{array}{llllllllllllllll}0.200506 & 0.190525 & 0.172025 & 0.189006 & 0.200394 & 0.179806 & 0.179619 & 0.205806 & 0.189406 & 0.168825\end{array}\) \(\begin{array}{lllllllllll}0.181406 & 0.2026 & 0.191563 & 0.172838 & 0.184206 & 0.2022 & 0.191094 & 0.1719 & 0.188594 & 0.201594\end{array}\) \(\begin{array}{lllllllllllll}0.202406 & 0.19715 & 0.1752 & 0.178344 & 0.200075 & 0.190819 & 0.169925 & 0.184325 & 0.1996 & 0.183813\end{array}\) \(\begin{array}{llllllllllll}0.2024 & 0.180606 & 0.173913 & 0.201206 & 0.202488 & 0.174194 & 0.177188 & 0.203244 & 0.1918 & 0.174206\end{array}\) \(\begin{array}{lllllllllll}0.175225 & 0.185794 & 0.201406 & 0.188 & 0.176606 & 0.1886 & 0.200038 & 0.186331 & 0.176419 & 0.1867\end{array}\) \(\begin{array}{llllllllllll}0.206369 & 0.1825 & 0.172769 & 0.192206 & 0.204544 & 0.181406 & 0.173406 & 0.192781 & 0.20175 & 0.1764\end{array}\) \(\begin{array}{llllllllllll}0.189613 & 0.202019 & 0.185394 & 0.174013 & 0.191213 & 0.204088 & 0.18215 & 0.168156 & 0.195019 & 0.205637\end{array}\) \(\begin{array}{llllllllll}0.20075 & 0.193875 & 0.174425 & 0.183806 & 0.2019 & 0.1912 & 0.1722 & 0.186006 & 0.203275 & 0.187806\end{array}\) \(\begin{array}{lllllllllll}0.182144 & 0.202713 & 0.1903 & 0.174219 & 0.18325 & 0.198838 & 0.1835 & 0.171494 & 0.196125 & 0.1991\end{array}\) \(\begin{array}{lllllllllll}0.1947 & 0.2039 & 0.18155 & 0.174206 & 0.195794 & 0.199831 & 0.176606 & 0.175381 & 0.199913 & 0.199575\end{array}\) \(\begin{array}{llllllllllllll}0.200925 & 0.173913 & 0.175619 & 0.201663 & 0.193206 & 0.170681 & 0.1894 & 0.204406 & 0.183006 & 0.172794\end{array}\) \(0.16990 .1983060 .2008250 .1744940 .1730810 .201988 \quad 0.18990 .1744250 .1864250 .199413\) \(\begin{array}{lllllllllllllll}0.171931 & 0.185194 & 0.201212 & 0.187275 & 0.175806 & 0.186475 & 0.200313 & 0.185344 & 0.172888 & 0.197638\end{array}\) \(\begin{array}{lllllllllll}0.19765 & 0.187913 & 0.174594 & 0.189675 & 0.204619 & 0.182 & 0.170806 & 0.191125 & 0.205613 & 0.1815\end{array}\) \(\begin{array}{llllllllllllll}0.187006 & 0.202294 & 0.189613 & 0.173788 & 0.188406 & 0.200606 & 0.187613 & 0.169538 & 0.198388 & 0.191144\end{array}\) \(\begin{array}{lllllllllll}0.188238 & 0.199906 & 0.183844 & 0.168988 & 0.191888 & 0.204519 & 0.183631 & 0.172975 & 0.196888 & 0.201819\end{array}\) \(\begin{array}{llllllllllll}0.174006 & 0.1784 & 0.20075 & 0.188706 & 0.175031 & 0.1807 & 0.201663 & 0.189131 & 0.173944 & 0.198206\end{array}\) \(\begin{array}{llllllllll}0.1734 & 0.197481 & 0.201188 & 0.1727 & 0.172781 & 0.202212 & 0.191213 & 0.172175 & 0.1855 & 0.200613\end{array}\) \(\begin{array}{llllllllllllll}0.201919 & 0.1895 & 0.171856 & 0.194206 & 0.203406 & 0.1783 & 0.171994 & 0.195419 & 0.199225 & 0.175006\end{array}\) \(\begin{array}{lllllllllllll}0.1928 & 0.173738 & 0.179613 & 0.203144 & 0.193206 & 0.174613 & 0.183969 & 0.199988 & 0.184794 & 0.169888\end{array}\) \(\begin{array}{lllllllllll}0.199563 & 0.178544 & 0.1751 & 0.1966 & 0.2006 & 0.177794 & 0.175225 & 0.197619 & 0.1999 & 0.179619\end{array}\) \(\begin{array}{lllllllllll}0.194813 & 0.20175 & 0.18 & 0.173613 & 0.195806 & 0.2018 & 0.182 & 0.172988 & 0.2024 & 0.1894\end{array}\) \(\begin{array}{lllllllllll}0.199513 & 0.174488 & 0.175513 & 0.202269 & 0.2006 & 0.174319 & 0.184813 & 0.200075 & 0.187531 & 0.1695\end{array}\) \(\begin{array}{lllllllllll}0.198213 & 0.199006 & 0.173306 & 0.173625 & 0.198306 & 0.2003 & 0.1715 & 0.179781 & 0.202231 & 0.194425\end{array}\) \(\begin{array}{llllllllll}0.200813 & 0.188669 & 0.17445 & 0.188 & 0.201456 & 0.181744 & 0.1734 & 0.2011 & 0.195606 & 0.17275\end{array}\) \(\begin{array}{llllllllll}0.1855 & 0.203006 & 0.189 & 0.175619 & 0.184738 & 0.1998 & 0.183588 & 0.170413 & 0.1923 & 0.203938\end{array}\) \(\begin{array}{lllllllllllllllll}0.204 & 0.183738 & 0.173294 & 0.197006 & 0.200862 & 0.1779 & 0.175669 & 0.197269 & 0.200363 & 0.177806\end{array}\)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & 0.200888 & 0.1939 & 0. & 0.179606 & 0.201206 & 0.197531 & 0.174144 & 0.176806 & 6 \\
\hline 0.200306 & 0.181431 & 0.172631 & 0.194906 & 0.199988 & 0.1742 & 0.176594 & 0.2003 & 0.197644 & 0.172181 \\
\hline 0.196306 & 0.1719 & 0.177556 & 0.201469 & 0.194425 & 0.1734 & 0.180413 & 0.199831 & 0.193781 & 0.1723 \\
\hline 0.199963 & 0.1819 & 0.176219 & 0.202 & 0.1979 & 0.173481 & 0.184838 & 0.202306 & 0.189663 & 0.174144 \\
\hline 0.175806 & 0.192075 & 0.200406 & 0. & 0.1787 & 0.2015 & 0.190788 & 0.172313 & 0.186444 & 0.198594 \\
\hline 0.199 & 0.200319 & 0.1687 & 0. & 0.198306 & 0.184813 & 0.173138 & 0.193431 & 0.204644 & 33 \\
\hline 0.1896 & 0. & 0. & 0. & 0.19995 & 0. & 0.175994 & 9 & 3 & 44 \\
\hline 0. & 0. & 0.172731 & 0. & 0. & 0.173406 & 0.179581 & 2 & 8 & 析 \\
\hline 0.172181 & 0.19515 & 0.199488 & 0.175831 & 0.1719 & 8 & 0.1899 & 8 & 4 & \\
\hline 0.172181 & 0 & 0 & 0.1944 & 0.172075 & 0.181613 & 0.202463 & 6 & 7 & \\
\hline & 0. & 0. & 0.177219 & 0 & & 0.186438 & 4 & 1 & 38 \\
\hline 0. & 0. & 0 & 0.193813 & & 0.183988 & 0.202 & 4 & 1 & \\
\hline 0.200 & 0.1 & 0. & 0.2007 & 0.1891 & 0.169675 & 0.1864 & 3 & 6 & 3 \\
\hline 0.1935 & 0.199806 & 0.1736 & 0.171506 & 0.202206 & 5 & 0.172344 & 0.180025 & 8 & 06 \\
\hline 5 & 0.17 & 0.200306 & 0. & 0.172306 & 8 & 0. & 0.192413 & 0.170813 & 331 \\
\hline 171581 & 0.203019 & 0.1932 & 0.16909 & 0.187019 & 0.2019 & 0.190806 & 0.173988 & 0.184725 & 0.199663 \\
\hline 0.188606 & 0.202488 & 0.176694 & 0.17601 & 0.200881 & 0.189788 & 0.171619 & 0.19435 & 0.1995 & 0.177606 \\
\hline 0.198081 & 0.1867 & 0.172025 & 0.1934 & 0.2059 & 0.183106 & 0.172344 & 0.1939 & 0.201206 & 04 \\
\hline 0.180619 & 0.202356 & 0.183019 & 0.172 & 0.196825 & 0.1999 & 0.176381 & 0.175006 & 0.198206 & 0.198438 \\
\hline 0.1822 & 0.172044 & 0.196088 & 0.2008 & 0.177406 & 0.173925 & 0.198381 & 0.202281 & 0.172794 & 4 \\
\hline 0.1 & 0.201894 & 0.1 & 0. & 0.186 & 0.199894 & 0.1 & 0. & 0.192888 & 5 \\
\hline 0.177688 & 0.1768 & 0.1982 & 0 & 0. & 0. & 0. & 0， & 0.174081 & 6 \\
\hline 0.1 & 0.18 & 0.2 & 0.19 & 0. & 0.191194 & 0. & 0.176213 & 1 & 8 \\
\hline 0.196875 & 0.20 & 0.17 & 0.1751 & 0. & 0. & 0.175888 & 0.177206 & 0.202019 & 0.199913 \\
\hline 0.1819 & 0.170206 & 0.1943 & 0.2 & 0.1 & 0.179819 & 0.203713 & 0.1887 & 0.173138 & 0.188606 \\
\hline 0.201406 & 0.173644 & 0.19555 & 0.202 & 0.1728 & 0.184606 & 0.204013 & 0.188481 & 0.172375 & 0.185594 \\
\hline 0.1704 & 0.1971 & 0.20004 & 0.172606 & 0.1829 & 0.203006 & 0.189431 & 0.1707 & 0.186319 & 0.202206 \\
\hline 0.1742 & 0.183869 & 0.203169 & 0.191944 & 0. & 0.184306 & 0.2019 & 0.188775 & 0.175344 & 0.187363 \\
\hline 0.172881 & 0.17 & 0 & 0. & 0 & 0 & 0.201212 & 0.1778 & 1 & ． 201344 \\
\hline 0. & 0. & 0. & 0.20 & 0. & 0. & 0.1 & 0.202806 & 9 & 27 \\
\hline 0.1 & 0.1762 & 0. & 0.199388 & 0.18 & 0.172306 & 0.1894 & 0.200188 & 0.183219 & 69 \\
\hline 0.185006 & 0. & 0. & 0.170206 & 0. & 0.199644 & 0.185394 & 0.171506 & 0.198081 & 0.202988 \\
\hline 0.1921 & 0.200606 & 0.1715 & 0.1831 & 0.2020 & 0.187 & 0.1752 & 0.194438 & 0.202219 & 0.174206 \\
\hline 0.172075 & 0.201219 & 0.191631 & 0.173638 & 0.183994 & 0.201125 & 0.191006 & 0.173625 & 0.1843 & 0.2028 \\
\hline 0.1743 & 0.189188 & 0.2027 & 0.182175 & 0.173619 & 0.198806 & 0.199606 & 0.1731 & 0.184406 & 0.204938 \\
\hline 0.191406 & 0.203394 & 0.18315 & 0.171406 & 0.1915 & 0.202413 & 0.180406 & 0.172438 & 0.200656 & 0.203 \\
\hline 0.173406 & 0.178381 & 0.2003 & 0.1927 & 0.172606 & 0.186006 & 0.200613 & 0.181131 & 0.1731 & 0.1959 \\
\hline 0.179088 & 0.203006 & 0.193638 & 0.1711 & 0.185594 & 0.206 & 0.189594 & 0.175738 & 0.186481 & 0.203606 \\
\hline 0.178806 & 0.174363 & 0.201269 & 0.192794 & 0.172794 & 0.183913 & 0.202006 & 0.182781 & 0.169025 & 0.192413 \\
\hline 0.1768 & 0.200975 & 0.199169 & 0.172344 & 0.186013 & 0.2018 & 0.192406 & 0.172013 & 0.1864 & 0.202206 \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline & 0.174206 & & & & & & & 0.2024 & \\
\hline 178838 & 0.2028 & & & 0.184375 & 0.199288 & 0.187088 & 0.172038 & 0.1931 & 0.20405 \\
\hline & 0.201188 & & 0.17980 & & & 0.204488 & 0.1851 & 0.173281 & \\
\hline 0.185563 & . 2 & & & & & & & 0.178206 & \\
\hline & 0.1743 & 0.18514 & & 0.1899 & & & 0.200356 & & \\
\hline & & 0.200 & & 0.173681 & , & . 2 & & & \\
\hline 172 & 92 & 0.20324 & & & & 0.2035 & & 0.1 & \\
\hline 0.1883 & 0.200 & 0. & & 0.1 & 20158 & 190 & & 0.1 & 0.201 \\
\hline 181888 & 0 & 0.18967 & 0.199338 & 0.1 & & 0.185294 & 0.202181 & 0.189738 & 0.17 \\
\hline . 200731 & 0. & 0. & 0.17307 & 0.200 & 0. & 0.175138 & 0.175213 & 0. & \\
\hline 0.182088 & 0 & 0.189 & 0.1998 & 0.18478 & 0.175913 & 0.186425 & 0.199663 & 0.1896 & \\
\hline 0.2026 & 0.184581 & 0.170 & 0.19100 & 0.201 & 0.186475 & 0.174494 & 0.186413 & & 0.189 \\
\hline 198069 & & 0.178 & & & & 0.181206 & 0.175219 & & \\
\hline & 0. & & 0. & & & & 0.203925 & & \\
\hline 200606 & 0. & 0.1695 & & & & 0.172606 & & & \\
\hline & & 0.202044 & 0. & & & 0. & 0.190588 & & \\
\hline & & 0.204394 & & & & & & & \\
\hline & & 0.200 & & & & & 0.1899 & & \\
\hline & & & & & & 0.190894 & 0.200331 & & \\
\hline . 2 & 0.1 & 0.175019 & 0. & & 0. & 0.1 & 0.1683 & 0.1 & \\
\hline & & 0.18829 & & 0. & 0. & 0.185 & . 20 & 0.1946 & \\
\hline 199806 & 0.200413 & & & & & & & & \\
\hline & & & & & & & & 199288 & \\
\hline & 0.182088 & & & & & 0.200819 & & & \\
\hline 202813 & 0.17888 & 0.1702 & 0.190 & , & 0.190269 & 0.169 & 1803 & , & \\
\hline & 0 & & & & 0.19 & 0.17 & & & \\
\hline & 0 & & & & & & & & \\
\hline 200825 & & & & & 0. & & & & \\
\hline 0.191819 & & & & & & & & 0.199606 & \\
\hline 0. & & 0.191 & & & & 0. & & & \\
\hline 197431 & 0.2 & 0.183 & & & & & & & \\
\hline & & & & & & & & 0.192975 & \\
\hline & & , & & & & & & & \\
\hline 186475 & 0.17 & 0.19 & & & & & & & \\
\hline . 190969 & 0.172 & & 0.202 & 0.196794 & & 0.1 & 0.198444 & 0.200025 & \\
\hline & 0. & & 0.2046 & 0.184025 & 0. & 0. & 0.200813 & & \\
\hline . & 0. & 0. & 0.198206 & 0. & 0. & 0. & 0.190975 & . 20 & . 1 \\
\hline 182594 & 0.17 & 0.187 & 0. & 0.1 & 0.170888 & 0.181638 & 0.2020 & 0.197531 & 0.176 \\
\hline 0.2019 & 0.188144 & 0.17 & 0.187 & 0.2000 & 0.190219 & 0.172013 & 0.1836 & 0.2036 & . \\
\hline 0.191 & 0.175006 & 0.17983 & 0.20238 & 0.20081 & 0.176356 & 0.1768 & 0.1976 & 0.20390 & 184 \\
\hline
\end{tabular}
.
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline 0.172025 & 0.1836 & 0.201838 & 0.194713 & 0.175794 & 0.176888 & 0.1991 & 0.198325 & 0.178744 & 0.169 \\
\hline 0.1815 & 0.167675 & 0.190788 & 0. & 0. & 0.170775 & 0.186806 & 6 & 5 & 1 \\
\hline 0.203 & 0.189106 & 0.175019 & 0.1 & 0.200838 & 0.200406 & 0.173688 & 0.1743 & 6 & 888 \\
\hline 200413 & 0.180025 & 0.174194 & , & 0. & 0.184231 & 0.174206 & 0.188487 & 0.200413 & 0.190094 \\
\hline 0.175919 & 0.198775 & 0.202438 & 0.170794 & 0.177625 & 0.197906 & 0.200419 & 0.179406 & 0.17355 & 0.201194 \\
\hline 0.201244 & 0.19275 & 0.1711 & 0.174525 & 0.19921 & 0.200025 & 0.175581 & 0.172694 & . 1935 & 0.1986 \\
\hline 0.199106 & 0.189469 & 0.174806 & 0.183375 & 0.20299 & 0.192825 & 0.172238 & 0.17435 & . 1972 & . 200606 \\
\hline 0.194394 & 0.174538 & 0.1724 & 0.196463 & 0.204525 & 0.1844 & 0.171531 & 0.187581 & 0.199138 & 0.188013 \\
\hline 0.183087 & 0.202919 & 97 & 0.17560 & 0.1749 & 0.200 & 0.20141 & 0.177975 & 0.170488 & 0.188381 \\
\hline 0.17 & 0.172988 & 0.2 & 0.19368 & 0.1 & 0.173688 & 0.198806 & 0.204 & 0.183113 & 0.172094 \\
\hline 0.1 & 0.2 & 0. & 0. & 0. & 0. & 0.2055 & 0.184025 & 4 & 0.185531 \\
\hline 0.1736 & 0.1 & 0. & 0. & 0. & 0.1 & 0.197206 & 0.204488 & 0.180381 & 0.170744 \\
\hline 0.185 & 0.1 & 0. & 0.2 & 0. & 0. & 0. & 7 & 5 & 6 \\
\hline 0.19 & 0.203006 & 0. & 0.1766 & 0.1 & 0.204606 & 0. & 8 & 0.175556 & 0.200075 \\
\hline 1735 & 0.1 & 0.1999 & . 2 & 0. & 0.1742 & 0.1 & 1 & 0.185206 & 0.176606 \\
\hline 0.200 & 0.188 & 0.174069 & 0.1854 & 0.20 & 0.1928 & 0.175219 & 0.184038 & 0.201206 & 27 \\
\hline 0.200 & 0.1 & 0.174063 & & 0 & 0. & 0.1732 & 0.189625 & 6 & 6 \\
\hline 0.206219 & 0.187563 & 0.1726 & 0.1 & 0.2 & 0. & 0.170963 & 0.192144 & . 2031 & 0.182394 \\
\hline 0.186406 & 0.199131 & 0.189988 & 0.1 & 0.178 & 0.2 & 0.194744 & 0.173294 & 0.175325 & 47 \\
\hline 0.1755 & 0.1752 & 0.202806 & 0.191606 & 0.172 & 0.1868 & 0.2038 & 0.176719 & 0.174788 & 0.204413 \\
\hline 0.173294 & 0.197981 & 0.201394 & 0.181 & 0.1683 & 0.189075 & 0.198981 & 0.189825 & 0.170706 & 0.18085 \\
\hline 0.1903 & 0.175638 & 0.176606 & . 19922 & 0.200 & 0.177188 & 739 & 0.195106 & 0.2035 & 1844 \\
\hline 0.174231 & 0.196794 & 0.199131 & 0.174806 & 0.17503 & 0.1983 & 0.2012 & 0.1815 & 0.167588 & 0.1867 \\
\hline 0.187294 & 0.199831 & 0.189181 & 0.172606 & 0.18281 & 0.200337 & 0.195594 & 0.174188 & 0.176619 & 0.196387 \\
\hline 0.176606 & 0.177219 & 0.202069 & 0.197888 & 0.174 & 0.177219 & 0.1947 & 0.203956 & 0.183219 & 0.173638 \\
\hline 0.1787 & 0.174713 & 0.199006 & 0.202994 & 0.173 & 0.174425 & 0.196094 & 0.196706 & 0.1747 & 0.1747 \\
\hline 0.180013 & 0.199931 & 0.19555 & 0.172488 & 0.175 & 0.2003 & 0.20235 & 0.177806 & 0.174206 & 0.194419 \\
\hline 0.17299 & 0.176281 & 0.201912 & 0.20060 & 0.1 & 0. & 0.189081 & 0.1982 & 0.186944 & 0.17355 \\
\hline 0.171113 & 0.185213 & 0.20075 & 0.19748 & 0.1747 & 0.1735 & 0.194988 & 0.2019 & 0.18355 & 0.177419 \\
\hline 0.196681 & 0.190206 & 0.173569 & 0.18163 & 0.2029 & 0.200606 & 0.179806 & 0.169294 & 0.193444 & 0.202306 \\
\hline 0.193 & 0.172638 & 0.171906 & 0.196306 & 0.19833 & 0.1784 & 0.1718 & 0.1915 & 0.201806 & 0.188313 \\
\hline 0.175344 & 0.195913 & 0.203906 & 0.1863 & 0.17430 & 0.1878 & 0.199613 & 0.189625 & 0.17045 & 0.181325 \\
\hline 0.204 & 0.1859 & 0.175806 & 0.18601 & 0.202 & 0.1899 & 0.1731 & 0.1822 & 0.2024 & 0.192306 \\
\hline 0.184081 & 0.20398 & 0.1912 & 0.173 & 0.1783 & 0.1983 & 0.201 & 0.179913 & 0.171806 & 0.1912 \\
\hline 0.1711 & 0.190194 & 0.198775 & 0.18994 & 0.17298 & 0.186419 & 0.2027 & 0.1907 & 0.174425 & 0.174019 \\
\hline 0.1860 & 0.2056 & 0.1916 & 0.174281 & 0.18140 & 0.198506 & 0.202019 & 0.179619 & 0.171581 & 0.1922 \\
\hline 0.1760 & 0.184306 & 0.204406 & 0.191613 & 0.17353 & 0.177213 & 0.1991 & 0.2014 & 0.180413 & 0.173212 \\
\hline 0.172313 & 0.193406 & 0.206256 & 0.183788 & 0.174819 & 0.189663 & 0.199638 & 0.189619 & 0.173675 & 0.187238 \\
\hline 0.176981 & 0.172675 & 0.191606 & 0.1991 & 0.187931 & 0.172 & 0.184994 & 0.2024 & 0.195019 & 0.172494 \\
\hline 0.173619 & 0.187513 & 0.203113 & 0.1892 & 0.173475 & 0.180981 & 0.201219 & 0.186706 & 0.175 & 0.195188 \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline 0.1896 & 0.195906 & 0.191 & 0.17195 & 0.185394 & 0.202406 & 0.192819 & 0.173 & 0.1794 & 0.2006 \\
\hline 182 & 0.19955 & 0.198525 & 0.1 & 0. & 0.2005 & 9 & 0.177244 & 0.175544 & 0. \\
\hline 182288 & 0.17 & & 0.1985 & 0. & 0.175806 & 0.187 & 0.200381 & 0.191894 & 5 \\
\hline 0.173738 & 0.1827 & 0.2027 & 0.105019 & 0. & 0.1798 & 0.202006 & 0.200238 & 1752 & 0.175281 \\
\hline 0.196656 & 0.171844 & 0.175794 & 0.200038 & 0.199594 & 0.178219 & 0.175288 & 0.196925 & 0.2008 & 779 \\
\hline 0.184887 & 0.173625 & 0.188719 & 0.2006 & 0.187 & 0.173106 & 0.1815 & 0.203806 & 0.198394 & 0.176819 \\
\hline 0.1794 & 0.170275 & 0.1899 & 0.200363 & 0.1892 & 0.172281 & 0.1851 & 0.201406 & 0.192994 & 0.173469 \\
\hline 0.174125 & 0.185194 & 0.20075 & 0.193106 & 0.1723 & 0.192138 & 0.199669 & 0.189406 & 0.173244 & 0.185419 \\
\hline 0.202063 & 0.18325 & 0.175938 & 0.185788 & 0.20 & 0.188 & 0.17214 & 0.177944 & 0.200388 & 0.201581 \\
\hline 0.1863 & 0.1995 & 0.189 & 0.17023 & 0.187 & 0.20 & 0.191006 & 0.176681 & 0.186713 & 0.198331 \\
\hline 0.201 & 0.190231 & 0.17 & 0.1 & 0. & 0. & 0.176606 & 0.186219 & 0.2027 & 0.190438 \\
\hline 0.18 & 0. & 0.1 & 0. & 0. & 0.2 & 0. & 0.172788 & 0.173188 & 0.195969 \\
\hline 0.185 & 0. & 0. & 0. & 0.1 & 0.2006 & 0.199194 & 0.178206 & 4 & 3 \\
\hline 0.20 & 0.1 & 0. & 0.1 & 0.2 & 0.1811 & 0. & 0.190269 & 0.199238 & 38 \\
\hline 0.186363 & 0.2 & 0.18 & 0.1 & 0.183 & 0.2 & 0.19435 & 4 & 0.173131 & 0.197156 \\
\hline 0.1752 & 0.17 & 0.2022 & 0.2006 & 0.1 & 0.174325 & 0.197113 & 0.201238 & 0.181219 & 0.171019 \\
\hline 17 & 0.1 & 0.20 & 0.1926 & 0. & 0.17995 & 0.199106 & 6 & 5 & 9 \\
\hline 0.17 & 0.187619 & 0.199244 & 0.190806 & 0.1 & 0.180388 & 0.199513 & 0.200306 & 0.177638 & 0.172606 \\
\hline 0.20 & 0.180025 & 0.1726 & 0.192 & 0.1 & 0.19 & 0.174438 & 0.185688 & 0.2 & 0.192631 \\
\hline 0.191344 & 0.173238 & 0.1735 & 0.198388 & 0.197406 & 0.172606 & 0.171538 & 0.196075 & 0.200075 & 0.176206 \\
\hline 0.202006 & 0.2014 & 0.1755 & 0.174438 & 0.195038 & 0.204419 & 0.186006 & 0.172544 & 0.191744 & 0.203613 \\
\hline 0.175613 & 0.1892 & 0.200825 & 0.18874 & 0.17278 & 0.1864 & 0.203806 & 0.192819 & 0.175219 & 0.178081 \\
\hline 19975 & 0.1883 & 0.173613 & 1 & 0.1985 & 0.189625 & 0.1732 & 0.183869 & 0.1995 & 947 \\
\hline 0.202588 & 0.1787 & 0.171225 & 0.1928 & 0.200706 & 0.1851 & 0.174544 & 0.186013 & 0.201488 & 0.188081 \\
\hline 0.188606 & 0.2024 & 0.1916 & 0.175031 & 0.177675 & 0.202713 & 0.2024 & 0.177469 & 0.172606 & 0.195106 \\
\hline 0.197581 & 0.199275 & 0.180025 & 0.175619 & 0.197244 & 0.2011 & 0.179194 & 0.170819 & 0.188744 & 0.199288 \\
\hline 0.202037 & 0.188606 & 0.176812 & 0.1855 & 0.203613 & 0.190869 & 0.171619 & 0.179394 & 0.201394 & 0.192813 \\
\hline 0.185144 & 0.204038 & 0.18953 & 0.1723 & 0.1836 & 0.1995 & 0.1974 & 0.173638 & 0.175744 & 0.194738 \\
\hline 0.1848 & 0.202688 & 0.191588 & 0.173406 & 0.178481 & 0.20075 & 0.198269 & 0.175619 & 0.177406 & 0.197594 \\
\hline 0.1857 & 0.176819 & 0.186413 & 0.20 & 0.1879 & 0.170869 & 0.1835 & 0.203344 & 0.187969 & 0.170425 \\
\hline 0.172181 & 0.186306 & 0.199288 & 0.191006 & 0.1708 & 0.1823 & 0.2015 & 0.200038 & 0.172981 & 0.175225 \\
\hline 0.200894 & 0.2003 & 0.176406 & 0.172 & 0.19762 & 0.201406 & 0.179213 & 0.170081 & 0.191619 & 0.199238 \\
\hline 0.173794 & 0.174356 & 0.1982 & 0.2017 & 0.1844 & 0.175806 & 0.1859 & 0.1987 & 0.1891 & 0.169944 \\
\hline 0.199806 & 0.190163 & 0.168769 & 0.18009 & 0.20123 & 0.201687 & 0.1743 & 0.174475 & 0.196825 & 0.200731 \\
\hline 0.198206 & 0.2026 & 0.181194 & 0.17181 & 0.188 & 0.201319 & 0.190219 & 0.173094 & 0.181625 & 0.201406 \\
\hline 0.201219 & 0.1855 & 0.174425 & 0.186544 & 0.20380 & 0.191406 & 0.174806 & 0.179806 & 0.202013 & 0.201125 \\
\hline 0.190812 & 0.1999 & 0.1875 & 0.173294 & 0.184025 & 0.201037 & 0.195931 & 0.1752 & 0.173013 & 0.197988 \\
\hline 0.202019 & 0.1918 & 0.172038 & 0.176888 & 0.199619 & 0.200713 & 0.178425 & 0.173613 & 0.191881 & 0.200731 \\
\hline 0.177244 & 0.201344 & 0.201319 & 0.178325 & 0.1695 & 0.1871 & 0.201806 & 0.1896 & 0.174369 & 0.179606 \\
\hline 0.205613 & 0.187225 & 0.174813 & 0.18395 & 0.202037 & 0.195169 & 0.174088 & 0.1747 & 0.198675 & 0.201406 \\
\hline
\end{tabular}
\begin{tabular}{llllllllll}
41 & 42 & 43 & 44 & 45 & 46 & 47 & 48 & 49 & 50
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline . 196413 & 0.1736 & 0.1882 & 0.201381 & 0.180294 & 0.174438 & 6 & 0.200894 & 0.182725 & 0.175444 \\
\hline & 0.181 & 0.169406 & , & 0. & 0.1887 & 0.173381 & 0.182606 & 0.202231 & 3 \\
\hline 0.175581 & 0.202406 & 0.199794 & 0.173625 & 0.1 & 0.196013 & 0.201663 & 0.1783 & 4 & 88 \\
\hline . & 0.203006 & 0.1807 & 0.172069 & 0.19115 & 0.1981 & 0.189688 & 0.171806 & 0.183288 & 44 \\
\hline 0.169463 & 0.192394 & 0.196825 & 0.172538 & . 1766 & 0.200813 & 0.198394 & 0.1806 & 0.175406 & 69 \\
\hline 0.174869 & 0.195806 & 0.201538 & 0.182131 & 0.1719 & 0.192419 & 0.199994 & 0.18405 & 0.176825 & 194 \\
\hline 0.171288 & 0.197806 & 0.203806 & 0.180769 & 171806 & 0.1912 & 0.199131 & 0.189613 & 0.1734 & 0.186406 \\
\hline 0.2015 & 0.190594 & 0.169944 & 0.183794 & 0.201438 & 0.193 & 0.172025 & 0.1742 & 0.200419 & 0.201469 \\
\hline 17661 & 0.173738 & 0.1942 & 0.2 & 0.183006 & 0. & 0.19329 & 0.202706 & 0.1831 & 0.1762 \\
\hline 0 & 0.1695 & 0.183106 & 0.20 & 0.191038 & 0.173 & 0. & 0.199475 & 0.200444 & 0.1748 \\
\hline 0.17 & 0.1 & 0.2 & 0.2 & 0. & 0. & 0.191638 & 0.201912 & 7 & 0.170813 \\
\hline 0.20 & 0.1 & 0. & 0. & 0.203 & 0.185456 & 0.175588 & 0.188013 & 0.200144 & 38 \\
\hline 0.1 & 0.1 & 0.1 & 0. & 0.199806 & 0.1768 & 0.175819 & 0.198219 & 4 & 0.179944 \\
\hline . 17 & 0.1 & 0.2 & 0.1 & 0. & 0.183213 & 0.201325 & 0.200038 & 44 & 0.175006 \\
\hline 0.20 & 0.1792 & 0.17 & 0.194806 & 0.20 & 0.18155 & 0.1671 & 0.194994 & 0.200581 & 0.182206 \\
\hline 0.1896 & 0.19932 & 0.189625 & 0.1706 & 0.182588 & 0.202438 & 0.196406 & 0.1719 & 0.175206 & 0.1983 \\
\hline 0.1 & 0.2 & 0.177906 & O. & 0.191744 & 0.204438 & 0.183194 & 5 & 0.1879 & 13 \\
\hline 0.1958 & 0.20 & 0.183 & 0.1 & 0.1843 & 0.2044 & 0.19045 & 0.171838 & . 17615 & 0.201206 \\
\hline 0.17526 & 0.175875 & 0.201406 & 200038 & 0.176 & 0.173288 & 0.200 & 0.200406 & 0.175 & 751 \\
\hline 0.173913 & 0.197406 & 0.206819 & 0.181406 & 0.170469 & 0.193406 & 0.2035 & 0.185488 & 0.176825 & 0.187006 \\
\hline 0.179038 & 0.173138 & 0.1911 & 0.2026 & 0.18719 & 0.175744 & 0.1847 & 0.203844 & 0.191206 & 0.172606 \\
\hline 0.201763 & 0.198206 & 0.175513 & 0.1743 & 0.194769 & 0.20417 & 0.185156 & 0.172981 & 0.184181 & 0.203806 \\
\hline 0.173506 & 0.176731 & 0.1947 & 0.204406 & 0.1832 & 0.172981 & 0.1863 & 0.204544 & 0.1912 & 0.174319 \\
\hline 0.172694 & 0.1848 & 0.202806 & 0.196875 & 0.173481 & 0.1742 & 0.198006 & 0.204013 & 0.183006 & 806 \\
\hline 0.203325 & 0.1848 & 0.176669 & 0.188606 & 0.1983 & 0.189644 & 0.1719 & 0.185588 & 0.2028 & 819 \\
\hline 0.1889 & 0.174 & 0.182606 & 0.203006 & 0.196081 & 0.1727 & 0.174544 & 0.197419 & 0.205738 & 0.183806 \\
\hline 0.170 & 0.18493 & 0.203806 & 0.190425 & 0.173888 & 0.1802 & 0.201181 & 0.199506 & 0.176888 & 0.1758 \\
\hline 0.20030 & 0.1 & 0.174019 & 0.18 & 0.1963 & 0. & 0.170763 & 0.183006 & 0.201737 & 0.197406 \\
\hline 0.2006 & 0.1800 & 0.173288 & 0.192787 & 0.206 & 0.1848 & 0.1768 & 0.187006 & 0.204144 & 0.183238 \\
\hline 0.181675 & 0.20038 & 0.2003 & 0.178488 & 0.173625 & 0.192288 & 0.202844 & 0.188669 & 0.176338 & 0.196669 \\
\hline 0.194425 & 0.202481 & 0.187225 & 0.174206 & 0.183513 & 0.1994 & 0.193538 & 0.172875 & 0.174044 & 0.197613 \\
\hline 0.189913 & 0.1704 & 0.18275 & 0.200825 & 0.193238 & 0.174206 & 0.1727 & 0.199806 & 0.2019 & 0.1783 \\
\hline 0.182325 & 0.20139 & 0.196406 & 0.174819 & 0.175744 & 0.1987 & 0.199375 & 0.178425 & 0.1736 & 0.1928 \\
\hline 0.18300 & 0.172363 & 0.192706 & 0.200606 & 0.18965 & 0.170588 & 0.1831 & 0.202819 & 0.200838 & 0.176213 \\
\hline 0.19960 & 0.178206 & 0.176013 & 0.196 & 0.205744 & 0.185581 & 0.1752 & 0.184081 & 0.203131 & 0.190544 \\
\hline 0.17841 & 0.171963 & 0.191575 & 0.205494 & 0.1846 & 0.1766 & 0.185406 & 0.202881 & 0.191969 & 0.172325 \\
\hline 0.201206 & 0.181925 & 0.169181 & 0.188406 & 0.2014 & 0.19115 & 0.1723 & 0.1787 & 0.1982 & 0.202413 \\
\hline 0.189206 & 0.173381 & 0.186413 & 0.202813 & 0.196719 & 0.1768 & 0.1731 & 0.195 & 0.204025 & 0.183994 \\
\hline 0.201387 & 0.201163 & 0.174425 & 0.1732 & 0.194856 & 0.204363 & 0.1846 & 0.175588 & 0.186819 & 0.203325 \\
\hline 0.182069 & 0.168994 & 0.187225 & 0.200025 & 0.19 & 0.171856 & 0.1843 & 0.203006 & 0.192706 & 0.174044 \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline 0.188238 & 0.199225 & 0.190206 & 0.1726 & 0.182475 & 0.201113 & 0.18715 & 0.178 & 0.186181 & + \\
\hline 0 & 0.1 & 0.2 & 0.199819 & 0.180094 & 0. & 0.195388 & 0.206306 & 81 & 6 \\
\hline 0.202 & 0.1 & 0.1 & 0.186306 & 0. & 0. & 0.1 & 0.184406 & 1 & 8 \\
\hline , & 0.174 & 0.181975 & 0.202519 & 0.194475 & 0. & 8 & 2 & 0.199588 & 0.179513 \\
\hline 202281 & 0.186306 & 0.173994 & 0.186425 & 0.203606 & 0.190613 & 0.1715 & 0.1799 & 014 & 0.200856 \\
\hline 0.202294 & 0.185494 & 0.174713 & 0.186819 & 0.200706 & 0.19119 & 0.175213 & 0.172194 & 0.2054 & 0.196138 \\
\hline 0.205006 & 0.190819 & 0.169538 & 0.179906 & 0.201488 & 0.197644 & 0.176219 & 0.1758 & 0.196594 & 0.205469 \\
\hline 0.17625 & 0.1734 & 0.1926 & 0.202819 & 0.188325 & 0.174806 & 0.184388 & 0.2018 & 0.1935 & 0.172181 \\
\hline 0.185744 & 0.202231 & 0.191 & 0.173206 & 0.182144 & 0.200038 & 0.201006 & 0.174819 & 0.174606 & 0.197406 \\
\hline 0.1752 & 0.196825 & 0.203606 & 0.179906 & 0.170013 & 0.1899 & 0.202475 & 0.186381 & 0.176419 & 0.186294 \\
\hline 0.19 & 0.20109 & 0.188 & 0.173306 & 0.1848 & 0.200825 & 0.191006 & 0.171813 & 0.181406 & 0.2024 \\
\hline 17581 & 0.186 & 0.2 & 0.1 & 0. & 0.1 & 0. & 0.1963 & 9 & 0.173625 \\
\hline 0.16819 & 0. & 0. & 0.1 & 0. & 0. & 0. & 0.189688 & 0.172006 & 1 \\
\hline 0.1 & 0.2 & 0.1 & 0. & 0.1908 & 0.1 & 0. & 0. & 0.185113 & 06 \\
\hline 0.168094 & 0.19 & 0.199238 & 0. & 0.1 & 0. & 0. & 0.191006 & 13 & 1 \\
\hline 202 & 0.176 & 0.1723 & 0.1959 & 0.203069 & 0.183 & 0. & 0.1894 & 0.200781 & 0.182394 \\
\hline 190213 & 0.175213 & 0.186463 & 0.202806 & 0.1883 & 0.171294 & 0.184406 & 0.201375 & 0.193188 & 0.1752 \\
\hline 0.1998 & 0.17198 & 0.17 & 0.1 & 0.20263 & 0.1826 & 0.174831 & 0.176875 & 0.184781 & 0.201269 \\
\hline 0.19478 & 0.201 & 0.1848 & 0.1 & 0.18515 & 0.203069 & 0.1891 & 0.16915 & 0.182281 & . 202413 \\
\hline 0.206013 & 0.18920 & 0.175606 & 0.181794 & 0.1995 & 0.196619 & 0.1737 & 0.173181 & 0.1958 & 0.205406 \\
\hline 0.1787 & 0.20220 & 0.200813 & 0.173506 & 0.1751 & 0.202206 & 0.199 & 0.17338 & 0.175806 & 0.197519 \\
\hline 191806 & 0.17420 & 0.175006 & 0.199163 & 0.200806 & 0.180619 & 0.16832 & 0.190675 & 0.1987 & 0.188088 \\
\hline 0.178538 & 0.201 & 0.200825 & 0.1772 & 0.1731 & 0.196 & 0.20 & 0.180875 & 0.171069 & 0.190206 \\
\hline 0.187225 & 0.202413 & 0.1898 & 0.172013 & 0.18 & 0.202944 & 0.203019 & 0.177538 & 0.171994 & . 195663 \\
\hline 0.172706 & 0.174069 & 0.197688 & 0.2023 & 0.178425 & 0.172412 & 0.1921 & 0.202606 & 0.186475 & 0.1739 \\
\hline 0.173994 & 0.1894 & 0.202413 & 0.188331 & 0.169131 & 0.188 & 0.202481 & 0.191219 & 0.174019 & 0.177744 \\
\hline 0.1979 & 0.1986 & 0.173625 & 0.174869 & 0.2014 & 0.196631 & 0.171188 & 0.177213 & 0.1963 & 0.1999 \\
\hline 0.173675 & 0.17478 & 0.197606 & 0.198331 & 0.178813 & 0.176606 & 0.194581 & 0.2024 & 0.183619 & 0.166981 \\
\hline 0.171681 & 0.18714 & 0.2044 & 0.190794 & 0.173744 & 0.177219 & 0.1983 & 0.196413 & 0.1719 & 0.175819 \\
\hline 0.20614 & 0.183225 & 0.1741 & 0.187806 & 0.1992 & 0.188944 & 0.173675 & 0.186206 & 0.202006 & 0.192437 \\
\hline 0.203006 & 0.181988 & 0.174438 & 0.187919 & 0.201544 & 0.189406 & 0.170806 & 0.181494 & 0.201488 & 0.201588 \\
\hline 0.171994 & 0.19344 & 0.2005 & 0.187338 & 0.175606 & 0.185806 & 0.20315 & 0.191219 & 0.1752 & 0.179894 \\
\hline 0.202031 & 0.19767 & 0.1854 & 0.173881 & 0.1878 & 0.202206 & 0.191006 & 0.171013 & 0.1794 & 0.2022 \\
\hline 0.17445 & 0.19791 & 0.200594 & 0.183794 & 0.175375 & 0.186488 & 0.2060 & 0.191488 & 0.172894 & 0.186206 \\
\hline 0.174294 & 0.17878 & 0.19958 & 0.200075 & 0.178463 & 0.174206 & 0.191663 & 0.202019 & 0.183913 & 0.175225 \\
\hline 0.178206 & 0.199525 & 0.202425 & 0.1763 & 0.171381 & 0.197013 & 0.206813 & 0.186206 & 0.176406 & 0.185088 \\
\hline 0.178419 & 0.17320 & 0.192838 & 0.202781 & 0.185444 & 0.175906 & 0.18545 & 0.204544 & 0.192756 & 0.174425 \\
\hline 0.175006 & 0.185913 & 0.204025 & 0.191538 & 0.174369 & 0.173925 & 0.201975 & 0.194425 & 0.174863 & 0.1719 \\
\hline 0.190425 & 0.172 & 0.179213 & 0.200331 & 0.201238 & 0.177231 & 0.171237 & 0.192038 & 0.199225 & 0.189113 \\
\hline 0.177206 & 0.1974 & 0.201281 & 0.18235 & 0.172756 & 0.186006 & 0.2038 & 0.191869 & 0.174188 & 0.177456 \\
\hline
\end{tabular}


\begin{tabular}{llllllllll}
81 & 82 & 83 & 84 & 85 & 86 & 87 & 88 & 89 & 90 \\
\hline
\end{tabular}
\begin{tabular}{rrrrrrrrrr}
0.203631 & 0.199619 & 0.1816 & 0.168038 & 0.189625 & 0.1979 & 0.186581 & 0.1753 & 0.185194 & 0.199744 \\
0.173206 & 0.186438 & 0.202044 & 0.192813 & 0.173613 & 0.180025 & 0.202219 & 0.197631 & 0.1743 & 0.175763 \\
0.199094 & 0.173638 & 0.175 & 0.196613 & 0.206206 & 0.182481 & 0.172025 & 0.187613 & 0.201394 & 0.189638 \\
0.189213 & 0.175338 & 0.186438 & 0.200825 & 0.1883 & 0.172769 & 0.184388 & 0.2003 & 0.191006 & 0.174606 \\
0.1992 & 0.179244 & 0.170838 & 0.195006 & 0.2023 & 0.1835 & 0.1743 & 0.187581 & 0.199794 & 0.190206 \\
0.2019 & 0.176794 & 0.170594 & 0.195606 & 0.204025 & 0.178706 & 0.171225 & 0.194475 & 0.204606 & 0.182269 \\
\(0200 \cap 75\) & 0.1806 & 0.1716 & 0.194412 & 0203475 & 0187831 & 0.175944 & 0185538 & 0204588 & 0.188881
\end{tabular}

100 Cycle Averaged Acquisition Value Vs Reading Number
0.173638
0.196831
\[
0.1967
\]

0.202488
0.184356
0.195806
0.202356
0.177406
0.181688 0.19115
0.203288
0.200188 0.2011
0.203244 0.1887 0.1848
0.202331
0.171394
0.176206
0.202763
0.177688 0.18995
0.202806
0.203106
0.169294
\begin{tabular}{llllllllll}
0.1891 & 0.199856 & 0.188775 & 0.172769 & 0.185406 & 0.203363 & 0.191619 & 0.173212 & 0.182019 & 0.1997
\end{tabular} \(\begin{array}{lllllllllll}0.174581 & 0.196138 & 0.203006 & 0.1842 & 0.172019 & 0.186344 & 0.200206 & 0.191213 & 0.173794 & 0.177162\end{array}\) \(\begin{array}{lllllllllll}0.172981 & 0.172306 & 0.197444 & 0.203606 & 0.181181 & 0.172494 & 0.187275 & 0.200694 & 0.187994 & 0.174738\end{array}\) \(\begin{array}{llllllllll}0.174194 & 0.192206 & 0.204044 & 0.1867 & 0.16885 & 0.189744 & 0.2014 & 0.190013 & 0.172388 & 0.184406\end{array}\) \(\begin{array}{lllllllllll}0.181625 & 0.1711 & 0.188069 & 0.200606 & 0.190169 & 0.170294 & 0.184988 & 0.202819 & 0.195425 & 0.17515\end{array}\) \(\begin{array}{llllllllllll}0.175619 & 0.186413 & 0.205644 & 0.1902 & 0.1735 & 0.180038 & 0.200075 & 0.203606 & 0.178606 & 0.174344\end{array}\) \(\begin{array}{lllllllllll}0.199869 & 0.190281 & 0.170806 & 0.182813 & 0.202013 & 0.203019 & 0.172706 & 0.175069 & 0.1964 & 0.2015\end{array}\) \(\begin{array}{lllllllllll}0.173594 & 0.180888 & 0.202006 & 0.199119 & 0.174425 & 0.175819 & 0.195588 & 0.205625 & 0.1823 & 0.175744\end{array}\)
\begin{tabular}{llllllllll}
91 & 92 & 93 & 94 & 95 & 96 & 97 & 98 & 99 & 100 \\
\hline
\end{tabular}
\begin{tabular}{|c|c|c|}
\hline & 0.187461 & 0.187412 \\
\hline & 0.187057 & 0.187412 \\
\hline & 0.18747 & 0.187412 \\
\hline & 0.187408 & 0.187412 \\
\hline & 0.187291 & 0.187412 \\
\hline & 0.187247 & 0.187412 \\
\hline & 0.187497 & 0.187412 \\
\hline & 0.187049 & 0.187412 \\
\hline & 0.1874 & 0.187412 \\
\hline & 0.187308 & 0.187412 \\
\hline & 0.187454 & 0.187412 \\
\hline & 0.187196 & 0.187412 \\
\hline & 0.187217 & 0.187412 \\
\hline & 0.187707 & 0.187412 \\
\hline & 0.18727 & 0.187412 \\
\hline & 0.187382 & 0.187412 \\
\hline & 0.18751 & 0.187412 \\
\hline & 0.18719 & 0.187412 \\
\hline & 0.187458 & 0.187412 \\
\hline & 0.187448 & 0.187412 \\
\hline & 0.187903 & 0.187412 \\
\hline & 0.187528 & 0.187412 \\
\hline & 0.18734 & 0.187412 \\
\hline & 0.187855 & 0.187412 \\
\hline & 0.187163 & 0.187412 \\
\hline & 0.187396 & 0.187412 \\
\hline & 0.187361 & 0.187412 \\
\hline & 0.187279 & 0.187412 \\
\hline & 0.187278 & 0.187412 \\
\hline & 0.18757 & 0.187412 \\
\hline & 0.187091 & 0.187412 \\
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\hline & 0.187474 & 0.187412 \\
\hline & 0.187493 & 0.187412 \\
\hline & 0.187667 & 0.187412 \\
\hline & 0.187488 & 0.187412 \\
\hline & 0.187586 & 0.187412 \\
\hline & 0.18765 & 0.187412 \\
\hline & 0.187708 & 0.187412 \\
\hline & & \\
\hline & & \\
\hline \(t\) Average & 0.187412 & \\
\hline & & \\
\hline ed Values & 0.000854 & \\
\hline
\end{tabular}

\begin{abstract}
\(\begin{array}{lllllllllll}0.009837 & 0.008574 & 0.009171 & 0.008926 & 0.010446 & 0.008398 & 0.010038 & 0.009183 & 0.009881 & 0.006539\end{array}\) \(\begin{array}{lllllllllll}0.017268 & 0.016394 & 0.018555 & 0.016796 & 0.018405 & 0.018103 & 0.016225 & 0.019541 & 0.016281 & 0.020465\end{array}\) \(\begin{array}{lllllllllll}0.025126 & 0.029648 & 0.02755 & 0.02848 & 0.029353 & 0.0238 & 0.033888 & 0.02642 & 0.031545 & 0.029083\end{array}\) \(\begin{array}{llllllllllll}0.044856 & 0.034962 & 0.041074 & 0.038788 & 0.04103 & 0.039585 & 0.038273 & 0.043078 & 0.034177 & 0.043618\end{array}\) \(\begin{array}{lllllllllll}0.056564 & 0.044114 & 0.055327 & 0.039095 & 0.055854 & 0.04294 & 0.054975 & 0.045258 & 0.053241 & 0.046357\end{array}\) \(\begin{array}{lllllllllll}0.061438 & 0.051859 & 0.063448 & 0.050138 & 0.065823 & 0.050459 & 0.062839 & 0.05348 & 0.058222 & 0.06157\end{array}\) \(\begin{array}{lllllllllll}0.077198 & 0.059303 & 0.07566 & 0.065295 & 0.067431 & 0.074001 & 0.061011 & 0.075119 & 0.06191 & 0.076225\end{array}\) \(\begin{array}{lllllllllllll}0.073373 & 0.08255 & 0.075082 & 0.081099 & 0.078197 & 0.071187 & 0.082839 & 0.085766 & 0.086514 & 0.075779\end{array}\) \(0.0895790 .0841140 .0967090 .0814760 .095704 \quad 0.080590 .0975940 .0791270 .0965330 .078191\) \(\begin{array}{llllllllllllllllll}0.108279 & 0.090986 & 0.109786 & 0.090785 & 0.102117 & 0.097494 & 0.102123 & 0.098216 & 0.099296 & 0.103298\end{array}\) \(\begin{array}{llllllllllll}0.103078 & 0.118926 & 0.100239 & 0.123844 & 0.097312 & 0.11941 & 0.096118 & 0.119824 & 0.100031 & 0.12059\end{array}\) \(\begin{array}{llllllllllll}0.109755 & 0.130948 & 0.107374 & 0.128147 & 0.109535 & 0.135013 & 0.107946 & 0.13108 & 0.108681 & 0.128976\end{array}\) \(\begin{array}{lllllllllllll}0.113976 & 0.140898 & 0.118756 & 0.142921 & 0.121552 & 0.130584 & 0.126866 & 0.132676 & 0.128668 & 0.129058\end{array}\) \(\begin{array}{llllllllllllll}0.154579 & 0.136778 & 0.135207 & 0.146771 & 0.130276 & 0.150974 & 0.123857 & 0.153172 & 0.129083 & 0.153687\end{array}\) \(\begin{array}{lllllllllll}0.136363 & 0.160603 & 0.134177 & 0.156778 & 0.14554 & 0.152104 & 0.154397 & 0.135905 & 0.160697 & 0.133335\end{array}\) \(\begin{array}{lllllllllll}0.150352 & 0.171382 & 0.147136 & 0.174064 & 0.146225 & 0.172814 & 0.144523 & 0.17331 & 0.148003 & 0.167946\end{array}\) \(\begin{array}{llllllllll}0.149943 & 0.183731 & 0.157494 & 0.176124 & 0.166872 & 0.17179 & 0.169454 & 0.165415 & 0.176288 & 0.161621\end{array}\) \(\begin{array}{lllllllllllllllll}0.169454 & 0.190666 & 0.167443 & 0.192845 & 0.163562 & 0.192626 & 0.173474 & 0.181495 & 0.165132 & 0.166526\end{array}\) \(\begin{array}{lllllllllllll}0.191476 & 0.192205 & 0.185345 & 0.197619 & 0.176388 & 0.202487 & 0.174366 & 0.205308 & 0.176646 & 0.203323\end{array}\) \(0.1843150 .2103140 .1939130 .215358 \quad 0.1841330 .2146730 .1855470 .2104150 .1946110 .201313\) \(\begin{array}{lllllllllll}0.200245 & 0.227538 & 0.196595 & 0.223913 & 0.194623 & 0.225521 & 0.195923 & 0.22593 & 0.200195 & 0.21522\end{array}\) \(\begin{array}{llllllllll}0.215264 & 0.23358 & 0.20483 & 0.239209 & 0.20348 & 0.22956 & 0.21657 & 0.213273 & 0.225459 & 0.210101\end{array}\) \(\begin{array}{lllllllllllll}0.242023 & 0.232412 & 0.226526 & 0.237211 & 0.2174 & 0.241545 & 0.213116 & 0.245226 & 0.216319 & 0.246784\end{array}\) \(\begin{array}{llllllllllllll}0.248285 & 0.224334 & 0.254466 & 0.22593 & 0.258116 & 0.223769 & 0.256627 & 0.224987 & 0.251683 & 0.229139\end{array}\) \(\begin{array}{llllllllllllllllll}0.261652 & 0.244724 & 0.252607 & 0.252877 & 0.243229 & 0.257494 & 0.240232 & 0.264937 & 0.23642 & 0.263662\end{array}\) \(\begin{array}{llllllllllllll}0.245647 & 0.2776 & 0.247236 & 0.275804 & 0.252073 & 0.266432 & 0.252054 & 0.265741 & 0.257582 & 0.257896\end{array}\) 0.2504460 .2832290 .2532660 .2864380 .2560930 .2729080 .2664450 .2721730 .2688570 .265936 \(\begin{array}{lllllllllllllll}0.266696 & 0.298241 & 0.26299 & 0.295967 & 0.263549 & 0.291903 & 0.280917 & 0.273976 & 0.287827 & 0.271784\end{array}\) \(\begin{array}{llllllllllllll}0.309573 & 0.275804 & 0.304384 & 0.273976 & 0.298587 & 0.283361 & 0.295101 & 0.291903 & 0.284133 & 0.296225\end{array}\) \(\begin{array}{lllllllllllllllll}0.284121 & 0.314768 & 0.288248 & 0.304127 & 0.298317 & 0.300597 & 0.300044 & 0.296998 & 0.305942 & 0.290992\end{array}\) \(\begin{array}{lllllllllllllllllll}0.324416 & 0.299391 & 0.317984 & 0.304761 & 0.316005 & 0.307889 & 0.314183 & 0.307933 & 0.308486 & 0.316382\end{array}\) \(\begin{array}{llllllllllllllllllll}0.308951 & 0.337029 & 0.305188 & 0.338938 & 0.306357 & 0.336043 & 0.306878 & 0.335691 & 0.304529 & 0.335842\end{array}\) \(\begin{array}{llllllllllllll}0.327381 & 0.335691 & 0.328907 & 0.332085 & 0.334673 & 0.319001 & 0.34495 & 0.315961 & 0.346979 & 0.314617\end{array}\) \(\begin{array}{llllllllllllllllllll}0.338028 & 0.332607 & 0.349824 & 0.329259 & 0.352475 & 0.323423 & 0.358455 & 0.326897 & 0.357814 & 0.324435\end{array}\) \(\begin{array}{lllllllllllllllll}0.354717 & 0.349774 & 0.350151 & 0.354378 & 0.341514 & 0.362117 & 0.334774 & 0.365974 & 0.331457 & 0.362952\end{array}\) \(\begin{array}{lllllllllllllllll}0.36559 & 0.349579 & 0.370195 & 0.349774 & 0.378354 & 0.343712 & 0.375892 & 0.344535 & 0.379234 & 0.345057\end{array}\) \(\begin{array}{lllllllllllllllllll}0.354573 & 0.383518 & 0.361602 & 0.373675 & 0.367852 & 0.373869 & 0.36951 & 0.368543 & 0.375553 & 0.365873\end{array}\) \(\begin{array}{llllllllllllll}0.364152 & 0.394579 & 0.36907 & 0.386715 & 0.37348 & 0.383109 & 0.377682 & 0.380936 & 0.381922 & 0.374699\end{array}\) \(\begin{array}{llllllllllllll}0.373367 & 0.403423 & 0.377632 & 0.397563 & 0.388788 & 0.392663 & 0.391583 & 0.388003 & 0.395471 & 0.383518\end{array}\)

\end{abstract}
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\begin{abstract}
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0.071281 & 0.064215 & 0.075565\end{array}\) \(\begin{array}{lllllllllllllllll}0.086162 & 0.08483 & 0.075603 & 0.079466 & 0.080201 & 0.078178 & 0.080892 & 0.075823 & 0.080333 & 0.070785\end{array}\) \(\begin{array}{lllllllllllllll}0.079793 & 0.096646 & 0.080678 & 0.095879 & 0.084422 & 0.095314 & 0.082714 & 0.093681 & 0.084529 & 0.094083\end{array}\) \(\begin{array}{llllllllllll}0.087437 & 0.108134 & 0.092462 & 0.112173 & 0.085421 & 0.111558 & 0.085427 & 0.108568 & 0.089579 & 0.111288\end{array}\) \(\begin{array}{lllllllllllllllll}0.116482 & 0.09853 & 0.11941 & 0.098436 & 0.116552 & 0.104447 & 0.108876 & 0.103926 & 0.113832 & 0.110697\end{array}\) \(\begin{array}{llllllllllllllllll}0.129378 & 0.10934 & 0.129742 & 0.109428 & 0.126256 & 0.114077 & 0.119598 & 0.121432 & 0.118982 & 0.121533\end{array}\) \(\begin{array}{lllllllllllll}0.132067 & 0.126822 & 0.13272 & 0.127864 & 0.130861 & 0.127839 & 0.136294 & 0.119824 & 0.140207 & 0.118097\end{array}\) \(\begin{array}{llllllllllll}0.15517 & 0.12706 & 0.150741 & 0.129441 & 0.150364 & 0.131602 & 0.144359 & 0.137356 & 0.139943 & 0.14044\end{array}\) \(\begin{array}{lllllllllll}0.13809 & 0.15625 & 0.143555 & 0.154579 & 0.148744 & 0.149158 & 0.152412 & 0.146539 & 0.153876 & 0.141922\end{array}\) \(\begin{array}{lllllllllll}0.17267 & 0.146771 & 0.175402 & 0.142117 & 0.17468 & 0.146382 & 0.174937 & 0.144121 & 0.173474 & 0.144391\end{array}\) \(\begin{array}{lllllllllll}0.18071 & 0.156991 & 0.183926 & 0.158405 & 0.185113 & 0.153568 & 0.18093 & 0.154384 & 0.186432 & 0.157431\end{array}\) \(\begin{array}{lllllllllllll}0.176872 & 0.184535 & 0.172864 & 0.185804 & 0.173461 & 0.187732 & 0.167035 & 0.190559 & 0.166834 & 0.19919\end{array}\) \(\begin{array}{llllllllllll}0.199008 & 0.184121 & 0.19218 & 0.192161 & 0.191093 & 0.19076 & 0.186935 & 0.197167 & 0.180006 & 0.201677\end{array}\) \(\begin{array}{llllllllll}0.21429 & 0.180308 & 0.216941 & 0.182318 & 0.212129 & 0.18897 & 0.209874 & 0.18934 & 0.207173 & 0.196036\end{array}\) \(\begin{array}{llllllllll}0.226526 & 0.196325 & 0.230094 & 0.191658 & 0.229573 & 0.194378 & 0.198128 & 0.224127 & 0.19478 & 0.22495\end{array}\) \(\begin{array}{llllllllllllll}0.213116 & 0.223813 & 0.220396 & 0.217293 & 0.224322 & 0.216891 & 0.220986 & 0.216482 & 0.224384 & 0.207827\end{array}\) \(\begin{array}{llllllllllll}0.229083 & 0.230961 & 0.22544 & 0.232167 & 0.222374 & 0.240848 & 0.21718 & 0.246495 & 0.212092 & 0.245773\end{array}\) \(0.2238320 .2577510 .2222490 .255804 \quad 0.227940 .2514890 .2298120 .2501260 .2289070 .247952\) \(0.2607790 .2378710 .2585050 .245226 \quad 0.2522550 .2526380 .2480530 .254856\) \(\begin{array}{lllllllllll}0.276175 & 0.244629 & 0.276979 & 0.245226 & 0.277205 & 0.245264 & 0.274491 & 0.245641 & 0.277701 & 0.244014\end{array}\) \(0.2758730 .2603640 .2838440 .254372 \quad 0.284830 .2560930 .2878890 .2564950 .284560 .253266\) \(\begin{array}{llllllllllllll}0.295622 & 0.265396 & 0.294479 & 0.26294 & 0.298342 & 0.267764 & 0.296709 & 0.264667 & 0.297098 & 0.267764\end{array}\) \(\begin{array}{llllllllllllllllll}0.271822 & 0.302242 & 0.274837 & 0.304673 & 0.274234 & 0.306947 & 0.27527 & 0.303097 & 0.276175 & 0.306357\end{array}\) 0.3051380 .2919350 .3147860 .2834110 .3133730 .2854770 .3198120 .2832290 .3123560 .283222 \(\begin{array}{llllllllllllll}0.292173 & 0.327173 & 0.296683 & 0.327186 & 0.290641 & 0.324755 & 0.295371 & 0.322726 & 0.296225 & 0.321539\end{array}\) \(\begin{array}{llllllllllllllllll}0.318731 & 0.317902 & 0.318807 & 0.325666 & 0.313982 & 0.335226 & 0.305 & 0.337475 & 0.304868 & 0.333612\end{array}\) \(\begin{array}{llllllllllll}0.333474 & 0.319001 & 0.343951 & 0.314686 & 0.348166 & 0.31598 & 0.348555 & 0.317601 & 0.345339 & 0.313373\end{array}\) \(\begin{array}{lllllllllllllllllllll}0.328882 & 0.351394 & 0.333694 & 0.345339 & 0.343731 & 0.337299 & 0.342023 & 0.340302 & 0.343763 & 0.338907\end{array}\) \(\begin{array}{llllllllllllllll}0.349799 & 0.354573 & 0.34505 & 0.352368 & 0.343317 & 0.354183 & 0.341784 & 0.359837 & 0.336407 & 0.364089\end{array}\) \(\begin{array}{llllllllllllllll}0.343631 & 0.378693 & 0.348166 & 0.370967 & 0.348681 & 0.370459 & 0.349554 & 0.363763 & 0.359397 & 0.362224\end{array}\) \(\begin{array}{lllllllllllllllllll}0.374196 & 0.371068 & 0.370314 & 0.366979 & 0.374416 & 0.364366 & 0.378499 & 0.364246 & 0.381709 & 0.356596\end{array}\) \(\begin{array}{llllllllllllll}0.388323 & 0.367048 & 0.394918 & 0.364617 & 0.394604 & 0.361834 & 0.392707 & 0.36456 & 0.396043 & 0.362494\end{array}\) \(\begin{array}{llllllllllll}0.39799 & 0.378687 & 0.406621 & 0.375182 & 0.40152 & 0.379095 & 0.407663 & 0.375528 & 0.408128 & 0.373367\end{array}\) \(\begin{array}{llllllllllllllllllllllll}0.388386 & 0.411652 & 0.387563 & 0.411652 & 0.384736 & 0.411652 & 0.386344 & 0.410848 & 0.384497 & 0.41652\end{array}\)
\end{abstract}


\begin{abstract}
\(\begin{array}{llllllllllll}0.008725 & 0.010923 & 0.008624 & 0.01098 & 0.008216 & 0.009491 & 0.006621 & 0.011935 & 0.007136 & 0.010383\end{array}\) \(\begin{array}{llllllllllll}0.018781 & 0.018028 & 0.017324 & 0.018612 & 0.015773 & 0.017111 & 0.019711 & 0.016608 & 0.020258 & 0.014428\end{array}\) \(0.0284860 .0282410 .0297610 .0282850 .0313510 .0275750 .0334920 .0257220 .033894 \quad 0.02559\) \(\begin{array}{llllllllllll}0.03419 & 0.044642 & 0.035572 & 0.044686 & 0.032996 & 0.043204 & 0.034818 & 0.040031 & 0.03826 & 0.039146\end{array}\) \(\begin{array}{llllllllllllll}0.054359 & 0.047418 & 0.051872 & 0.048851 & 0.048166 & 0.051583 & 0.045433 & 0.054717 & 0.042852 & 0.058235\end{array}\) \(\begin{array}{llllllllllll}0.053976 & 0.05679 & 0.059692 & 0.055308 & 0.058945 & 0.054121 & 0.063009 & 0.051884 & 0.065452 & 0.050119\end{array}\) \(\begin{array}{lllllllllll}0.062155 & 0.076652 & 0.06142 & 0.077751 & 0.062437 & 0.075377 & 0.061589 & 0.077111 & 0.06191 & 0.074799\end{array}\) 0.0819350 .0795920 .0776570 .0822170 .0739510 .0880840 .0732350 .0850310 .0665330 .086765 \(\begin{array}{llllllllllllllll}0.100503 & 0.079529 & 0.097236 & 0.075609 & 0.098486 & 0.079403 & 0.096313 & 0.083405 & 0.094095 & 0.084253\end{array}\) \(\begin{array}{lllllllllll}0.102123 & 0.096307 & 0.100704 & 0.095672 & 0.108153 & 0.090258 & 0.107318 & 0.08696 & 0.113813 & 0.090546\end{array}\) \(\begin{array}{lllllllllllllll}0.100515 & 0.119089 & 0.09544 & 0.124026 & 0.09968 & 0.120716 & 0.097494 & 0.123084 & 0.096866 & 0.119183\end{array}\) \(\begin{array}{llllllllllllllll}0.107531 & 0.132688 & 0.106734 & 0.129987 & 0.111281 & 0.130119 & 0.112487 & 0.123222 & 0.115804 & 0.118662\end{array}\) \(\begin{array}{llllllllll}0.140232 & 0.124026 & 0.135949 & 0.11799 & 0.141514 & 0.11941 & 0.145616 & 0.1137 & 0.140101 & 0.115905\end{array}\) \(\begin{array}{llllllllllllll}0.127638 & 0.151388 & 0.125214 & 0.153706 & 0.129209 & 0.150477 & 0.129843 & 0.145333 & 0.134177 & 0.14326\end{array}\) \(\begin{array}{lllllllllll}0.168053 & 0.136124 & 0.159529 & 0.132996 & 0.159391 & 0.133876 & 0.164014 & 0.137343 & 0.1625 & 0.137079\end{array}\) \(\begin{array}{llllllllllllllll}0.176627 & 0.146294 & 0.172475 & 0.148769 & 0.170484 & 0.151018 & 0.169994 & 0.150961 & 0.167029 & 0.154667\end{array}\) \(\begin{array}{lllllllllllll}0.165226 & 0.175691 & 0.160327 & 0.181319 & 0.154466 & 0.182318 & 0.153913 & 0.187098 & 0.157714 & 0.185327\end{array}\) \(\begin{array}{lllllllllllll}0.194699 & 0.161225 & 0.194441 & 0.174799 & 0.178518 & 0.179906 & 0.172758 & 0.187337 & 0.165157 & 0.188474\end{array}\) \(\begin{array}{llllllllllll}0.179322 & 0.197192 & 0.185622 & 0.19076 & 0.18875 & 0.188009 & 0.192607 & 0.184114 & 0.195685 & 0.1775\end{array}\) \(\begin{array}{llllllllllll}0.18495 & 0.212255 & 0.188894 & 0.209981 & 0.190578 & 0.207224 & 0.194102 & 0.181237 & 0.215892 & 0.186363\end{array}\) \(\begin{array}{llllllllllll}0.206036 & 0.21115 & 0.214485 & 0.204428 & 0.220044 & 0.206244 & 0.217293 & 0.201809 & 0.221903 & 0.208254\end{array}\) \(\begin{array}{lllllllllll}0.233474 & 0.202607 & 0.23934 & 0.20103 & 0.235603 & 0.203411 & 0.232569 & 0.203028 & 0.233373 & 0.208254\end{array}\) \(0.2195230 .2425570 .2193030 .2378830 .223832 \quad 0.23358\) 0.23157 0.227626 \(\begin{array}{llllllllllll}0.252676 & 0.227732 & 0.255754 & 0.220647 & 0.256288 & 0.226476 & 0.258367 & 0.222626 & 0.25267 & 0.226074\end{array}\) \(\begin{array}{lllllllllll}0.232362 & 0.264937 & 0.236589 & 0.259711 & 0.24691 & 0.248819 & 0.253543 & 0.24723 & 0.253072 & 0.238888\end{array}\) \(\begin{array}{llllllllll}0.247236 & 0.274585 & 0.246156 & 0.275584 & 0.243668 & 0.278241 & 0.246068 & 0.27745 & 0.244837 & 0.277412\end{array}\) \(\begin{array}{llllllllllll}0.254278 & 0.283116 & 0.256482 & 0.288116 & 0.253568 & 0.285892 & 0.253706 & 0.287582 & 0.257274 & 0.280949\end{array}\) \(\begin{array}{lllllllllllllll}0.286193 & 0.282626 & 0.27902 & 0.283229 & 0.274001 & 0.290798 & 0.266344 & 0.295088 & 0.264799 & 0.294667\end{array}\) 0.2948810 .2763880 .2985870 .2757290 .3021730 .2810180 .3047740 .2743720 .3026260 .274585 \(\begin{array}{llllllllllll}0.292274 & 0.301822 & 0.296087 & 0.30397 & 0.298329 & 0.306313 & 0.288788 & 0.314372 & 0.285773 & 0.316005\end{array}\) \(\begin{array}{llllllllllllllllll}0.325622 & 0.290245 & 0.325622 & 0.293807 & 0.325628 & 0.291935 & 0.326847 & 0.29723 & 0.322412 & 0.298637\end{array}\) \(\begin{array}{lllllllllllll}0.322437 & 0.320829 & 0.323241 & 0.316024 & 0.329774 & 0.3038 & 0.335082 & 0.305471 & 0.33696 & 0.304761\end{array}\) \(\begin{array}{llllllllllllll}0.333668 & 0.335276 & 0.326263 & 0.332456 & 0.327286 & 0.335823 & 0.325653 & 0.339234 & 0.316294 & 0.34495\end{array}\) \(\begin{array}{llllllllllllllll}0.356206 & 0.326043 & 0.357814 & 0.322852 & 0.353763 & 0.325955 & 0.354987 & 0.326068 & 0.352833 & 0.330641\end{array}\) \(\begin{array}{llllllllllll}0.346338 & 0.350967 & 0.351671 & 0.346401 & 0.361005 & 0.337896 & 0.366627 & 0.33767 & 0.365854 & 0.332651\end{array}\) \(\begin{array}{lllllllllllllll}0.377173 & 0.345559 & 0.377701 & 0.342908 & 0.373819 & 0.344585 & 0.374171 & 0.349774 & 0.368072 & 0.354969\end{array}\) \(\begin{array}{lllllllllllll}0.387745 & 0.351822 & 0.386344 & 0.355019 & 0.384133 & 0.359812 & 0.378524 & 0.36299 & 0.373675 & 0.37125\end{array}\) \(\begin{array}{lllllllllllllllllll}0.381771 & 0.380107 & 0.378354 & 0.383543 & 0.375308 & 0.388342 & 0.370967 & 0.391552 & 0.364969 & 0.392563\end{array}\) \(\begin{array}{lllllllllllllllll}0.407638 & 0.373894 & 0.404403 & 0.375503 & 0.402349 & 0.378499 & 0.406696 & 0.373913 & 0.406696 & 0.375854\end{array}\)

\end{abstract}
\(\begin{array}{lllllllllll}0.00831 & 0.008894 & 0.009139 & 0.009045 & 0.008511 & 0.007858 & 0.009768 & 0.009246 & 0.010716 & 0.00728\end{array}\)
\(\begin{array}{lllllllllll}0.019334 & 0.013813 & 0.020879 & 0.014366 & 0.019158 & 0.015019 & 0.021445 & 0.014887 & 0.020025 & 0.01571\end{array}\)
\(\begin{array}{llllllllllll}0.033562 & 0.026602 & 0.031991 & 0.024177 & 0.032142 & 0.025019 & 0.031464 & 0.026558 & 0.031853 & 0.028266\end{array}\)
\(\begin{array}{lllllllllll}0.040616 & 0.037469 & 0.041476 & 0.036771 & 0.044548 & 0.034026 & 0.044303 & 0.032255 & 0.04348 & 0.033781\end{array}\)
\(\begin{array}{lllllllllll}0.042016 & 0.055666 & 0.042481 & 0.057312 & 0.041972 & 0.053505 & 0.042211 & 0.052387 & 0.04566 & 0.050031\end{array}\)
\(\begin{array}{lllllllllllll}0.064592 & 0.05125 & 0.067004 & 0.051545 & 0.065327 & 0.049491 & 0.065245 & 0.050157 & 0.063568 & 0.051928\end{array}\)
\(0.0653830 .0732980 .0646550 .070823 \quad 10.07 \quad 0.068430 .074058 \quad 0.0629150 .0758790 .060396\)
0.0715580 .0910430 .0721230 .0851320 .0697550 .0873620 .0704460 .0840140 .0753710 .081036
0.0903890 .0916270 .0880530 .0912370 .0844220 .0908980 .0839130 .097726
\(\begin{array}{lllllllllllll}0.113379 & 0.089215 & 0.110848 & 0.086796 & 0.109472 & 0.091891 & 0.111332 & 0.088675 & 0.109479 & 0.088637\end{array}\)
\(\begin{array}{llllllllllllllllll}0.100113 & 0.117575 & 0.103524 & 0.115967 & 0.102041 & 0.114366 & 0.103247 & 0.107167 & 0.111288 & 0.106828\end{array}\)
\(\begin{array}{llllllllllllll}0.121288 & 0.115873 & 0.123078 & 0.113562 & 0.122274 & 0.115578 & 0.122412 & 0.110546 & 0.131784 & 0.107268\end{array}\)
\(\begin{array}{llllllllllll}0.14434 & 0.115704 & 0.144334 & 0.118593 & 0.141715 & 0.118191 & 0.137626 & 0.124648 & 0.133662 & 0.131093\end{array}\)
\(\begin{array}{lllllllllllll}0.138599 & 0.139328 & 0.141112 & 0.136489 & 0.142324 & 0.137305 & 0.147908 & 0.129378 & 0.148951 & 0.128046\end{array}\)
\(\begin{array}{lllllllllllll}0.163109 & 0.136225 & 0.15468 & 0.1425 & 0.154422 & 0.143612 & 0.152814 & 0.150352 & 0.147186 & 0.153982\end{array}\)
\(\begin{array}{llllllllllllll}0.164824 & 0.157406 & 0.1587 & 0.159617 & 0.160609 & 0.151193 & 0.166778 & 0.152268 & 0.162343 & 0.159868\end{array}\)
\(\begin{array}{llllllllllll}0.153951 & 0.185754 & 0.149378 & 0.183518 & 0.155848 & 0.180433 & 0.159064 & 0.179736 & 0.163015 & 0.175741\end{array}\)
\(\begin{array}{lllllllllllllll}0.166457 & 0.191847 & 0.168248 & 0.190484 & 0.162217 & 0.196891 & 0.159529 & 0.190559 & 0.164221 & 0.194611\end{array}\)
\(\begin{array}{llllllllllll}0.20343 & 0.17527 & 0.205025 & 0.174504 & 0.202544 & 0.176288 & 0.202915 & 0.170672 & 0.204296 & 0.175509\end{array}\)
\(\begin{array}{llllllllllll}0.2138 & 0.180917 & 0.216294 & 0.18348 & 0.215082 & 0.187462 & 0.211482 & 0.191156 & 0.208072 & 0.195069\end{array}\)
\(\begin{array}{llllllllllll}0.217475 & 0.202224 & 0.226376 & 0.195377 & 0.227563 & 0.193781 & 0.215773 & 0.205634 & 0.211263 & 0.212462\end{array}\)
\(\begin{array}{llllllllllllll}0.232808 & 0.206036 & 0.230239 & 0.206633 & 0.23316 & 0.207305 & 0.230283 & 0.208637 & 0.224227 & 0.216413\end{array}\)
\(\begin{array}{lllllllllllllll}0.225333 & 0.228549 & 0.232312 & 0.225465 & 0.235974 & 0.216891 & 0.242035 & 0.212469 & 0.244736 & 0.214271\end{array}\)
\(\begin{array}{lllllllllll}0.259309 & 0.22326 & 0.257324 & 0.224384 & 0.253317 & 0.22919 & 0.248053 & 0.232406 & 0.242619 & 0.240402\end{array}\)
\(\begin{array}{llllllllllllll}0.263756 & 0.237751 & 0.264133 & 0.235188 & 0.265641 & 0.235992 & 0.267249 & 0.233901 & 0.265138 & 0.237186\end{array}\)
\(\begin{array}{llllllllllllll}0.248053 & 0.270358 & 0.250044 & 0.272965 & 0.253291 & 0.269296 & 0.254786 & 0.259692 & 0.261583 & 0.257582\end{array}\)
\(\begin{array}{llllllllllll}0.259102 & 0.281212 & 0.261332 & 0.276979 & 0.264535 & 0.273662 & 0.270905 & 0.26843 & 0.276633 & 0.256797\end{array}\)
\(\begin{array}{lllllllllll}0.260817 & 0.293003 & 0.26321 & 0.294956 & 0.264523 & 0.293461 & 0.264516 & 0.289843 & 0.272513 & 0.286124\end{array}\)
\(0.309158 \quad 0.276470 .3051880 .2717960 .3060240 .2757220 .3063320 .2752890 .3014010 .281822\)
\(\begin{array}{llllllllllll}0.281903 & 0.312814 & 0.282274 & 0.316325 & 0.286093 & 0.313078 & 0.290666 & 0.307952 & 0.294209 & 0.30745\end{array}\)
\(\begin{array}{llllllllllllll}0.321351 & 0.302205 & 0.314384 & 0.31157 & 0.308687 & 0.316005 & 0.299705 & 0.322726 & 0.298706 & 0.323825\end{array}\)
\(\begin{array}{llllllllllll}0.33326 & 0.304328 & 0.336156 & 0.30353 & 0.334686 & 0.306313 & 0.332676 & 0.309353 & 0.324322 & 0.318386\end{array}\)
\(\begin{array}{llllllllllllllll}0.313511 & 0.348606 & 0.312569 & 0.346558 & 0.316124 & 0.348166 & 0.313907 & 0.34495 & 0.316376 & 0.338298\end{array}\)
\(\begin{array}{lllllllllllllllllllllll}0.346482 & 0.337324 & 0.339096 & 0.342016 & 0.335741 & 0.348166 & 0.328982 & 0.348122 & 0.323562 & 0.353662\end{array}\)
\(\begin{array}{lllllllllllll}0.365892 & 0.336683 & 0.366972 & 0.335873 & 0.365829 & 0.33669 & 0.362776 & 0.340101 & 0.36103 & 0.340245\end{array}\)
\(\begin{array}{lllllllllllllllllll}0.360226 & 0.363028 & 0.358335 & 0.367984 & 0.353555 & 0.374535 & 0.348141 & 0.377136 & 0.344956 & 0.375427\end{array}\)
\(\begin{array}{lllllllllllll}0.379812 & 0.362758 & 0.377481 & 0.364127 & 0.370534 & 0.374284 & 0.366495 & 0.37919 & 0.359058 & 0.383524\end{array}\)
\(\begin{array}{llllllllllllll}0.364246 & 0.396796 & 0.362927 & 0.399209 & 0.362927 & 0.395157 & 0.361834 & 0.394655 & 0.365842 & 0.39348\end{array}\)
\(\begin{array}{llllllllllll}0.404303 & 0.376275 & 0.402808 & 0.376696 & 0.406376 & 0.375528 & 0.404837 & 0.375471 & 0.400716 & 0.378687\end{array}\)
\(\begin{array}{lllllllllllllllllll}0.411652 & 0.383423 & 0.411652 & 0.384931 & 0.411652 & 0.384931 & 0.411652 & 0.392004 & 0.407984 & 0.391168\end{array}\)



0.0084860 .012142
0.0207850 .01407 70.0347990 .025515 80.0420540 .034026 90.0486370 .047368 \(\begin{array}{lll}5 & 0.064969 & 0.052211\end{array}\) \(\begin{array}{lll}2 & 0.062959 & 0.074535\end{array}\) \(\begin{array}{lll}6 & 0.072293 & 0.07983\end{array}\) 70.0974810 .079906 60.0994850 .099686 \(1 \begin{array}{lll}1 & 0.119585 & 0.10017\end{array}\) \(6 \quad 0.1230150 .114064\) 50.1401070 .12304 40.1253640 .152946
                                    0.1591270 .142205
                                    \(0.163166 \quad 0.15365\)
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                                    0.1683480 .188945
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                                    0.2560930 .259692
                                    0.2853640 .251589
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                                    \(9 \quad 0.3475380 .353379\)
                                    90.3630590 .343731
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                                    \(4 \quad 0.397393 \quad 0.398737\)
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\(\mathbf{0 . 0 3 9 0 8}\) & 0.04 & 0.00092 & 4 \\
\(\mathbf{0 . 0 4 9 0 7 8}\) & 0.05 & 0.000922 & 5 \\
\(\mathbf{0 . 0 5 7 8 2 6}\) & 0.059 & 0.001174 & 6 \\
\(\mathbf{0 . 0 6 9 1 2 2}\) & 0.07 & 0.000878 & 7 \\
\(\mathbf{0 . 0 7 9 1 1 3}\) & 0.08 & 0.000887 & 8 \\
\(\mathbf{0 . 0 8 9 0 2 7}\) & 0.09 & 0.000973 & 9 \\
\(\mathbf{0 . 0 9 9 5 1 3}\) & 0.1 & 0.000487 & 10 \\
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\(\mathbf{0 . 1 3 9 7 7 5}\) & 0.14 & 0.000225 & 14 \\
\(\mathbf{0 . 1 4 8 8 8}\) & 0.15 & 0.00112 & 15 \\
\(\mathbf{0 . 1 5 9 3 7 7}\) & 0.16 & 0.000623 & 16 \\
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\(\mathbf{0 . 1 7 9 5 6 4}\) & 0.18 & 0.000436 & 18 \\
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\(\mathbf{0 . 1 9 9 6 9 9}\) & 0.2 & 0.000301 & 20 \\
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\(\mathbf{0 . 2 1 9 5 8 7}\) & 0.22 & 0.000413 & 22 \\
\(\mathbf{0 . 2 2 9 7 4 3}\) & 0.23 & 0.000257 & 23 \\
\(\mathbf{0 . 2 3 9 9 2 6}\) & 0.24 & \(7.42 \mathrm{E}-05\) & 24 \\
\(\mathbf{0 . 2 5 0 1 4 9}\) & 0.25 & 0.000149 & 25 \\
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\(\mathbf{0 . 2 6 9 7 6 9}\) & 0.27 & 0.000231 & 27 \\
\(\mathbf{0 . 2 8 0 2 4 8}\) & 0.28 & 0.000248 & 28 \\
\(\mathbf{0 . 2 9 0 0 7 9}\) & 0.29 & \(7.89 \mathrm{E}-05\) & 29 \\
\(\mathbf{0 . 3 0 0 0 2}\) & 0.3 & \(1.96 \mathrm{E}-05\) & 30 \\
\(\mathbf{0 . 3 1 0 5}\) & 0.31 & 0.0005 & 31 \\
\(\mathbf{0 . 3 2 0 1 7 3}\) & 0.32 & 0.000173 & 32 \\
\(\mathbf{0 . 3 3 0 7 3 4}\) & 0.33 & 0.000734 & 33 \\
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\(\mathbf{0 . 3 5 0 2 3}\) & 0.35 & 0.00023 & 35 \\
\(\mathbf{0 . 3 6 0 3 1 9}\) & 0.36 & 0.000319 & 36 \\
\(\mathbf{0 . 3 7 0 3 8 5}\) & 0.37 & 0.000385 & 37 \\
\(\mathbf{0 . 3 7 9 7 1 2}\) & 0.38 & 0.000288 & 38 \\
\(\mathbf{0 . 3 9 0 2 9 1}\) & 0.39 & 0.000291 & 39 \\
\(\mathbf{0 . 3 9 9 1 6}\) & 0.4 & 0.00084 & 40 \\
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\begin{tabular}{rrrrrrrrrr}
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0.135207 & 0.127173 & 0.142349 & 0.147186 & 0.127148 & 0.126834 & 0.144422 & 0.139673 & 0.126244 & 0.137286 \\
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0.13772 & 0.135151 & 0.137481 & 0.138417 & 0.135057 & 0.136438 & 0.136602 & 0.136784 & 0.135276 & 0.137682 \\
0.117475 & 0.124209 & 0.126231 & 0.115597 & 0.116997 & 0.126294 & 0.118492 & 0.113574 & 0.120936 & 0.128191 \\
0.12723 & 0.143141 & 0.14071 & 0.122921 & 0.133354 & 0.143536 & 0.134271 & 0.126652 & 0.138913 & 0.147136 \\
0.13875 & 0.155892 & 0.167582 & 0.145188 & 0.134278 & 0.160069 & 0.160025 & 0.131451 & 0.142632 & 0.169837 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted \\
0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646
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0.169673 & 0.153976 & 0.133681 & 0.148781 & 0.164962 & 0.150157 & 0.132475 & 0.14995 & 0.169403 & 0.153449 \\
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\begin{tabular}{rrrrrrrrrr}
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0.127324 & 0.135678 & 0.146457 & 0.135471 & 0.123518 & 0.136099 & 0.14598 & 0.13956 & 0.127368 & 0.135534 \\
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0.137016 & 0.135339 & 0.139981 & 0.133832 & 0.133266 & 0.134026 & 0.13983 & 0.137305 & 0.136049 & 0.136212 \\
0.115289 & 0.120553 & 0.128059 & 0.121005 & 0.120057 & 0.122349 & 0.124623 & 0.12321 & 0.117293 & 0.120609 \\
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0.145383 & 0.137374 & 0.12657 & 0.134768 & 0.142513 & 0.137959 & 0.127443 & 0.134824 & 0.146043 & 0.14017 \\
0.159121 & 0.156709 & 0.165905 & 0.171928 & 0.162487 & 0.158549 & 0.163147 & 0.169648 & 0.159139 & 0.155176 \\
0.13956 & 0.137557 & 0.132067 & 0.132582 & 0.140201 & 0.137588 & 0.136445 & 0.138222 & 0.139535 & 0.137657 \\
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0.136514
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0.136671 & 0.133725 & 0.136181 & 0.135829 & 0.133844 & 0.135779 & 0.139196 & 0.134554 & 0.13615 & 0.1362 \\
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0.144033 & 0.143719 & 0.126771 & 0.136677 & 0.146746 & 0.137431 & 0.124077 & 0.143153 & 0.148109 & 0.127833 \\
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\hline 0.152293 & 0.16571 & 0.152663 & 0.139523 & 0.149705 & 0.163235 & 0.152035 & 0.135383 & 0.150553 & 62814 \\
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0.152362 & 0.163926 & 0.144623 & 0.133455 & 0.159171 & 0.169246 & 0.145477 & 0.135314 & 0.159397 & 0.16657 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted \\
0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted
\end{tabular}
\begin{tabular}{cccccccccc}
\(\mathbf{0 . 1 3 4 0 8 3}\) & \(\mathbf{0 . 1 4 9 4 4 7}\) & \(\mathbf{0 . 1 3 7 9 0 2}\) & \(\mathbf{0 . 1 2 1 1 5 6}\) & \(\mathbf{0 . 1 3 8 4 9 9}\) & \(\mathbf{0 . 1 5 0 3 0 2}\) & \(\mathbf{0 . 1 3 7 7 1 4}\) & \(\mathbf{0 . 1 2 5 4 5 9}\) & \(\mathbf{0 . 1 3 6 8 4 7}\) & \(\mathbf{0 . 1 5 0 6 3 4}\) \\
0.145534 & 0.127224 & 0.131828 & 0.14934 & 0.143882 & 0.127707 & 0.129516 & 0.148882 & 0.139642 & 0.12657 \\
0.163863 & 0.161558 & 0.158467 & 0.162111 & 0.167883 & 0.162852 & 0.156451 & 0.165251 & 0.172431 & 0.161809 \\
0.13772 & 0.139636 & 0.137494 & 0.134579 & 0.136796 & 0.13593 & 0.137092 & 0.134171 & 0.135006 & 0.134874 \\
0.124856 & 0.11946 & 0.123128 & 0.126533 & 0.124347 & 0.118656 & 0.125452 & 0.129008 & 0.1224 & 0.116771 \\
0.132544 & 0.147004 & 0.138097 & 0.12684 & 0.136005 & 0.146822 & 0.13767 & 0.12907 & 0.135503 & 0.146036 \\
0.144786 & 0.139196 & 0.160283 & 0.165415 & 0.140854 & 0.136759 & 0.161928 & 0.16483 & 0.136112 & 0.137041 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted \\
0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.41646 & 0.411646 & 0.411646 & 0.411646 & 0.41646 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted
\end{tabular}
\begin{tabular}{cccccccccc}
0.133486 & \(\mathbf{0 . 1 2 4 1 0 2}\) & \(\mathbf{0 . 1 4 5 1 8 8}\) & \(\mathbf{0 . 1 5 2 1 1 7}\) & \(\mathbf{0 . 1 3 4 0 0 8}\) & \(\mathbf{0 . 1 2 0 6 6 6}\) & \(\mathbf{0 . 1 4 0 5 0 9}\) & \(\mathbf{0 . 1 5 1 7 5 9}\) & \(\mathbf{0 . 1 3 1 6 5 8}\) & \(\mathbf{0 . 1 2 0 4 0 8}\) \\
0.13434 & 0.146539 & 0.139095 & 0.122412 & 0.133411 & 0.147035 & 0.139699 & 0.127544 & 0.135879 & 0.148894 \\
0.158059 & 0.169504 & 0.165107 & 0.158392 & 0.15995 & 0.165691 & 0.163687 & 0.156734 & 0.160019 & 0.164328 \\
0.136281 & 0.135829 & 0.137889 & 0.139234 & 0.135999 & 0.136614 & 0.137852 & 0.137318 & 0.137023 & 0.134114 \\
0.123028 & 0.126319 & 0.121018 & 0.116514 & 0.126275 & 0.128254 & 0.120747 & 0.118172 & 0.125408 & 0.12691 \\
0.135446 & 0.125402 & 0.130157 & 0.146131 & 0.137406 & 0.128543 & 0.139699 & 0.143291 & 0.13397 & 0.129045 \\
0.164372 & 0.162211 & 0.138807 & 0.139491 & 0.166828 & 0.162613 & 0.137833 & 0.142896 & 0.164353 & 0.165653 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted \\
0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted
\end{tabular}
\begin{tabular}{cccccccccc}
0.144121 & \(\mathbf{0 . 1 5 4 1 7 1}\) & \(\mathbf{0 . 1 3 1 0 5 5}\) & \(\mathbf{0 . 1 2 0 8 1}\) & \(\mathbf{0 . 1 4 5 5 2 1}\) & \(\mathbf{0 . 1 5 3 4 7 4}\) & \(\mathbf{0 . 1 3 0 1 0 7}\) & \(\mathbf{0 . 1 2 1 1 9 3}\) & \(\mathbf{0 . 1 4 8 6 9 3}\) & \(\mathbf{0 . 1 5 3 1 9 1}\) \\
0.139629 & 0.126181 & 0.135879 & 0.147802 & 0.140534 & 0.126489 & 0.131313 & 0.148744 & 0.142173 & 0.127852 \\
0.164667 & 0.157544 & 0.161407 & 0.170302 & 0.163951 & 0.158964 & 0.161489 & 0.168065 & 0.163342 & 0.158003 \\
0.137041 & 0.137004 & 0.137487 & 0.132462 & 0.134994 & 0.134579 & 0.133907 & 0.135484 & 0.138216 & 0.139824 \\
0.118392 & 0.121168 & 0.125892 & 0.126683 & 0.119925 & 0.118794 & 0.125647 & 0.125848 & 0.115389 & 0.11598 \\
0.140647 & 0.146715 & 0.134906 & 0.128072 & 0.141778 & 0.144529 & 0.131187 & 0.127312 & 0.143945 & 0.146407 \\
0.135038 & 0.141351 & 0.161106 & 0.159975 & 0.135829 & 0.14434 & 0.164472 & 0.163046 & 0.137155 & 0.143951 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted \\
0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted
\end{tabular}
\begin{tabular}{cccccccccc}
\(\mathbf{0 . 1 2 1 2 6 3}\) & \(\mathbf{0 . 1 3 4 0 7}\) & \(\mathbf{0 . 1 5 2 3 6 2}\) & \(\mathbf{0 . 1 3 9 1 2 1}\) & \(\mathbf{0 . 1 2 3 9 1 3}\) & \(\mathbf{0 . 1 3 5 9 0 5}\) & \(\mathbf{0 . 1 5 2 1 3 6}\) & \(\mathbf{0 . 1 3 6 6 0 2}\) & \(\mathbf{0 . 1 2 1 3 1 3}\) & \(\mathbf{0 . 1 3 5 8 7 9}\) \\
0.131055 & 0.147173 & 0.139699 & 0.124642 & 0.128279 & 0.145075 & 0.142286 & 0.124428 & 0.135094 & 0.149994 \\
0.163285 & 0.165961 & 0.161608 & 0.157217 & 0.163116 & 0.169454 & 0.162996 & 0.15517 & 0.163511 & 0.170911 \\
0.134259 & 0.137494 & 0.139611 & 0.140704 & 0.135509 & 0.136595 & 0.136018 & 0.135892 & 0.138053 & 0.136878 \\
0.122984 & 0.124384 & 0.117381 & 0.120352 & 0.12831 & 0.125415 & 0.120082 & 0.119793 & 0.128178 & 0.124623 \\
0.129397 & 0.126633 & 0.143945 & 0.144391 & 0.125798 & 0.126181 & 0.143725 & 0.147035 & 0.128543 & 0.126338 \\
0.166715 & 0.162908 & 0.137513 & 0.144755 & 0.16865 & 0.151564 & 0.134271 & 0.146137 & 0.166432 & 0.154064 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted \\
0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 & 0.411646 \\
Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted & Adjusted
\end{tabular}
0.137312
0.137252
0.162571
0.136502
0.122324
0.136679
0.151439

0
0.411645

0

\section*{Chapter 3}

\section*{Graphic User Interface (GUI) Development}

The GUI provides a means to control the automated machine as well a means to capture, analyse and store data. See Appendix A for a screen capture of the GUI and Appendix C for the complete GUI source code. In order to perform the above two functions, reliable communication between the GUI and the Controller is imperative. As previously mentioned, the GUI communicates directly with the Communication Microcontroller (CM) which then in turn communicates with the Automation Microcontroller (AM).


FIGURE 3-1: SYSTEM BLOCK DIAGRAM

In order to understand the function of the GUI, the communication between GUI and the CM has to first be discussed.

The GUI and the CM communicate serially using their respective serial ports which are setup to interact as required. In this chapter the author will discuss how data is processed from the point at which it is present in the GUI serial buffer as well as the prompts transmitted by the GUI to the controller, more specifically, the CM.

The interface between the GUI and the serial port (RS232) of a PC or Laptop using the Visual Basic 6 development environment is the MSComm component (only
available in more recent versions of Visual Basic). Once enabled the properties of the MSComm component have to be set so that they mirror the settings for the CM serial port. Under Properties in the MSComm component, the serial port that is to be used must be specified. For the purposes of this project, CommPort 1 was chosen. Under Settings, a baud rate of 2400, no parity bit, eight data received bits and one stop bit was specified. See Figure 3-2, below for a screen capture of the input property box for the MSComm component.


FIGURE 3-2: SCREEN CAPTURE OF THE INPUT PROPERTY FIELDS FOR MSCOMM1.

Along with MSComm1 settings, the serial port is initialised in the Form Load procedure using the statements in Code Extract 3-1, below.
```

${ }^{1 * * * * * * *}$ nitilise Serial Comm port $1^{* * * * * * *}$
'Rec data
MSComm1.RThreshold = 1
MSComm1. InputLen = 1
MSComm1.DTREnable = False
MSComm1.Settings = "2400,N,8,1"
MSComm1. CommPort = 1
MSComm1.PortOpen = True
'Trans data
MSComm1.OutBufferCount = 0
${ }^{\prime * * * *}$ End Initilise Serial Comm port 1*****

```

\section*{CODE EXTRACT 3-1: SERIAL PORT INITIALISATION IN THE FORM LOAD PROCEDURE}

For receiving data the first statement sets the threshold to 1 , thus firing the Receive Event on every received byte. The second statement ensures that data is input one byte at a time. The third statement disables the DTR (Data Terminal Ready line), during communications, hence the DTR line is always Low (0). The fourth statement is included for redundancy in order to ensure the aforementioned settings. The fifth statement selects the communication port that is to be used and the sixth statement opens the selected port. Finally, the seventh statement clears the transmit buffer on loading of the GUI form.

The information that is transmitted and received can be divided into two categories. One being ASCII characters for control operations, event prompts and selections made and the other being data in the form of the High and Low Bytes of a sixteen bit word that represents the digitised volt-drop reading. See Appendix B for the complete list of ASCII commands and their respective function or event prompts.

The transmission of ASCII prompts from the GUI to the CM is accomplished by using the line of code below:
MSComm1.Output = "B"

Here the ASCII code for the character B is transmitted to the CM in order to signal that the END button has been clicked on the GUI. ASCII characters are not only transmitted on a click event on the GUI, but they are also transmitted to signal the
beginning or the end of certain procedures as well as selections that have been made in the GUI input fields before the test can be started.

For any activity on the serial port or the associated buffers the OnComm procedure is initiated. The GUI has to decipher if this initiation occurred on the Send Event, Receive Event or any other activity. If,
MSComm1.CommEvent = comEvReceive
the OnComm procedure was initiated on the receive event. This means that data is present in the serial port buffer. The line of code below:
Let Serln = MSComm1. Input
reads the serial port buffer and copies the data into the variable SerIn. This variable is read in the OnComm procedure as well as in various other parts of the analysis and calculation procedures without being altered. The analysis and calculation processes will be discussed later in this chapter.

When in the OnComm procedure SerIn falls into a Case Select loop. Here the contents of SerIn is compared to all of the possible ASCII characters that are used as prompts and performs the tasks associated with the character that SerIn is equal to. When SerIn is equivalent to 'z', flag 'Incomming_HighB_Flag' is set. The setting of this flag alerts the GUI that upon the next initiation of the OnComm procedure that is due to a receive event, SerIn, will hold the high byte of the sixteen-bit, digitised voltdrop reading. SerIn will therefore not enter the case select loop.

When SerIn is equivalent to ' \(y\) ', flag 'Incomming_LowB_Flag' is set to alert the GUI that on the next initiation of the OnComm procedure that is due to a receive event SerIn will hold the low byte of the sixteen-bit, digitised volt-drop reading. Here again, SerIn does not enter the case select loop. The high and low bytes are each transmitted as eight bits by the controller, however, once in the GUI serial buffer it is read as the letter or symbol that is the ASCII code representation of the eight received bits. For example, if the binary number ' 01100001 ' was transmitted by the controller, the GUI
will read it as the letter ' \(a\) '. It is therefore necessary to convert the ASCII represented input to the decimal value that it represents in order to use the value in further calculations. This is accomplished in Visual Basic using the Asc function as shown below,
Low_Byte = Asc(Serln)

This line of code converts the ASCII coded value held in variable SerIn into the decimal value representing the ASCII code and places it in the variable that holds the low byte of the acquired volt-drop reading.

The decimal value for the received high byte is acquired in the same manner as can be seen in the Code Extract that follows. Please note that the Code Extracts and Flow Diagrams that follow, represents the expected input prompts from the controller before the Additional Features. With the inclusion of the Additional Features, incoming prompts such as the ASCII code for " S " was added as a further case that is to be tested in the Case Select Loop. Figure 3-3 depicts the flow chart for the Case Select loop in the OnComm procedure and Code Extract 3-2 presents the related source code.


A (pp. 33)


FIGURE 3-3: FLOW CHART FOR THE CASE SELECT LOOP
```

Private Sub MSComm1_OnComm()
If MSComm1.CommEvent = comEvReceive Then
Let SerIn = MSComm1.Input
If Serln = "" Then
Let Serln = "x"
End If
If Incomming_LowB_Flag = True Then
Low_Byte = Asc(Serln)
Let Incomming_LowB_Flag = False
Let Incomming_HighB_Flag = False
Call Calculation
Elself Incomming_HighB_Flag = True Then
High_Byte = Asc(Serln)
Let Incomming_HighB_Flag = False
Else
Select Case Serln
Case "b"
MSComm1.Output = Auto_Man

```
```

Case "d"
Command5.BackColor = \&H8000000F
Let Command5.Caption = "Start"
Command5.Enabled = True
Let Command8.Enabled = True
Screen.MousePointer = vbArrow
Case "O"
Command8.BackColor = QBColor(12)
Command7.BackColor = \&H8000000F
Let Command6.Enabled = True
Let Command6.BackColor = \&HFF8080
Let Picture6.BackColor =\&H8000000F
Call TestEnd_States
Let Emergency = True
Command8.Enabled = False
List1.FontBold = True
List1.AddItem "Emergency Stop on Bar " \& Text6.Text
List1.FontBold = False
Case "l"
Call Bar_count
Case "J"
Let Command10.Enabled = True ' error1
Command10.BackColor = QBColor(12)
Frame14.ForeColor = QBColor(12)
Frame14.FontSize = 10
Frame14.FontBold = True
Command9.Enabled = True
Frame20.ForeColor = QBColor(10)
Picture5.BackColor = QBColor(10)
Frame21.ForeColor = QBColor(10)
Command9.BackColor = \&HFF8080
Case "m"
Let Command11.Enabled = True ' error2
Command11.BackColor = QBColor(12)
Frame16.ForeColor = QBColor(12)
Frame16.FontSize = 10
Frame16.FontBold = True
Command9.Enabled = True
Frame20.ForeColor = QBColor(10)
Picture5.BackColor = QBColor(10)
Frame21.ForeColor = QBColor(10)
Command9.BackColor = \&HFF8080
Case "L"
Let Command12.Enabled = True 'error3
Command12.BackColor = QBColor(12)
Frame17.ForeColor = QBColor(12)
Frame17.FontSize = 10
Frame17.FontBold = True
Command8.Enabled = True
Command7.Enabled = True
Command7.BackColor = \&HFF8080
Command8.BackColor = \&HFF8080
Command8.BackColor = QBColor(12)

```
```

Command7. BackColor $=$ \&H8000000F
Let Command6. Enabled = True
Let Command6. BackColor $=$ \&HFF8080
Let Picture6.BackColor $=$ \& H 8000000 F
Call TestEnd_States
Let Emergency = True
Command8.Enabled $=$ False
List1. FontBold = True
List1.AddItem "Emergency Stop on Bar " \& Text6. Text
List1. FontBold = False
Let Command12.Enabled $=$ True
Command12.BackColor = QBColor(12)

```

Case "Q"
Let Command13.Enabled = True 'error4
Command13.BackColor = QBColor(12)
Frame15.ForeColor = QBColor(12)
Frame15.FontSize = 10
Frame15.FontBold = True
Command8.Enabled = True
Command7. Enabled = True
Command7. BackColor \(=\) \&HFF8080
Command8. BackColor \(=\) \&HFF8080
Case "z"
Let Incomming_HighB_Flag = True
Picture8.BackColor \(=\) QBColor(4)
Picture9. BackColor \(=\) \& H8000000F
Case "y"
Let Incomming_LowB_Flag = True
End Select
End If
End If
End Sub

\section*{CODE EXTRACT 3-2: ONCOMM EVENT RECEIVE}

\subsection*{3.1 A walk through the GUI}

The aim of this walk through is to lead the reader through the features, functions and code behind the Graphic User Interface. Screen captures will help the reader to understand how the GUI responds to user prompts and data that is received. See Appendix A for a true representation of the GUI and Appendix O for a GUI PowerPoint Presentation. The GUI is divided into two separate parts, one being the Test Setup Fields and the other being the Test In Progress Fields. Each of these will be discussed individually in the sections that follow.

\subsection*{3.1.1 Test Setup Fields}

\subsection*{3.1.1.1 User Identification Frame}

The input fields in this section are used to setup the system for the specific armature that is to be tested. See Figure 3-4A and Figure 3-4B. The User Identification frame is the location in which the details of the staff member that is to perform the test are entered.


FIGURE 3-4A: INITIAL TEST SCREEN


FIGURE 3-4B: USER IDENTIFICATION FRAME ON THE INITIAL TEST SCREEN

Initially, except for the New Test button encircled in Figure 3-4A, all the buttons and text input boxes are disabled. On clicking on the New Test button in the Password frame the Enter button is enabled and replaces the New Test button. See Figure 3-5A, and Figure 3-5B.


FIGURE 3-5A: INITIATE TEST SCREEN


\section*{FIGURE 3-5B: USER IDENTIFICATION FRAME ON THE INITIATE TEST SCREEN}

At this stage, except for the Enter button, all other control buttons are disabled and except for the Password text input box all the text input boxes are still disabled. To enable the GUI the correct user password has to be entered. This password was originally a generic password that was assigned to the system. Any staff member that was assigned to use this system was to use this password. This has subsequently been changed such that each user has a unique username and password that is chosen by the individual. The username and password is stored in a file on the PC or laptop hard-drive and is accessed and/or edited via the GUI whenever need be.

This login system is very much like the standard Windows® username and password login system except for the fact that only the password is entered in order to use the system. If the password is one that exists in the Username and Password file, the username that is associated with the entered password is displayed in the Name text box. This method is used to ensure accountability as the username displayed in the Name text box is the name that is printed in the test report and saved in the test history file. The username and password feature is discussed in detail in Chapter 6 under the heading, Multiple User Names and Passwords.

On entering the incorrect password GUI informs the user that the password is incorrect as well as the number of attempts that remain. See Figure 3-6A and Figure 3-6B.


FIGURE 3-6A: GUI REPRESENTATION WHEN AN INCORRECT PASSWORD HAD BEEN ENTERED

Incorrect Password X
Incorrect Password, Tries left: 2

OK

FIGURE 3-6B: MESSAGE BOX INFORMING THE USER OF THE NUMBER OF TRIES THAT REMAIN

If, on the third attempt, an incorrect password is entered the message box depicted in Figure 3-7A appears informing the user that he/she is about to be locked out by the system.
```

Lock Out
X
You DO NOT have the authority to use this equipment. You have been LOCKED OUT
OK

```

FIGURE 3-7A: MESSAGE BOX INFORMING THE USER THAT HE/SHE HAS BEEN LOCKED OUT

On acknowledgement of this message (by clicking on the OK button) the Lock Out frame is activated. The Lock Out frame hides every input and output function of the GUI, except for the Administrator Password functionality. See Figure 3-7B. The administrator password is used by a member of staff that is responsible for the supervision of the tests as well as the test technicians. This password allows the administrator to access and edit properties such as the Armature Properties, Test Parameters, Directory path and Unlocking. A user with a basic user password does not have the ability to edit these properties. Note that only the administrator can unlock the system once it has been locked.


FIGURE 3-7B: LOCK OUT SCREEN

\subsection*{3.1.1.2 Armature Properties Frame}

It is here that the user selects the armature type that is to be tested. See Figure 3-7C.


FIGURE 3-7C: ARMATURE PROPERTIES FRAME

The list of armatures is created by completing the New Armature Name and Number of Commutator Bars field and then clicking on the Add New Armature button. As mentioned previously this functionality is only available to the administrator, therefore upon clicking the above mentioned button, the user is asked for the administrator password before the new armature is added, see Figure 3-8A and Figure 3-8B. If an incorrect password is entered the new armature will not be added. For the removal of armatures from the list the Click To Remove Highlighted Armature functionality is used and is a functionality only available to the administrator. The reason for limiting access to these property fields is simply to exercise control over the test system. The user may only use the system and may not define any test limits and conditions other than those available to him/her.


FIGURE 3-8A: ADMINISTRATOR'S PASSWORD PROMPT


FIGURE 3-8B: GUI DISPLAYING THE ADMINISTRATOR'S PASSWORD PROMPT

All armatures appearing in the list are stored in a sequential file. This sequential file is accessed and/or edited when creating the list of armatures that are to be tested, adding a new armature to an existing list or deleting an armature from the list. The code extract below is responsible for the addition of a new armature to an existing file.
```

Private Sub Command3_Click()
If InputBox("Enter Administrators Password", "Administrators Password") = "AdminAutoSun6" Then
If (Text4.Text <> "") And (Text5.Text <> "") Then
Combo2.Addltem "Armature Name: " \& Text4.Text \& " Number of Bars: " \& Text5.Text
Let a = Combo2.ListCount ' used as a record number, 1st item starts at 1
Open Default Path \& "Arm.TXT" For Append As \#1
Write \#1, Text4.Text, Val(Text5.Text), (a)
Let Text4.Text = ""
Let Text5.Text = ""
Close \#1
Else
MsgBox "Enter new Armature Name and Number of Bars"
End If
Else: MsgBox "You are NOT Authorised to perform this action"
End If
End Sub

```

CODE EXTRACT 3-3: ADD NEW ARMATURE - COMMAND CLICK

The destination to which this file is saved is determined by Default Path. This path is specified in the Directory Path frame which will be discussed later in this chapter. The name of the file, as shown in Code Extract 3-3, is Arm. Data is written to this file using the Write statement. The data from the Text4.Text input box, which reflects the name of the new armature, the value of the data from the Text5.Text input box, which holds the number of bars on the commutator of the new armature, and the value that variable ' \(\mathbf{a}\) ' holds is written into the file.

The data from the two input text boxes is also displayed in a Combo Box using the AddItem method. With reference to Code Extract 3-3,

\section*{Let a = Combo2. ListCount}
assigns the value representing the number of items presently in the Combo Box to variable ' \(\mathbf{a}\) '. In this way, the last item added to the list is given the value that corresponds to the number of items in the Combo Box. For example, if the sixth armature is added to the Combo Box list the value returned by the ListCount method will be six.

The value that variable ' \(\mathbf{a}\) ' holds is stored with the intention for it to be used as an index to access a particular armature and its associated data from the file when selected. In this way, each entry into the file is much like a record. When an item (armature) is selected from the Combo Box, it already has an index (the ListIndex) associated to it by virtue if its place in the Combo Box. This ListIndex is not to be confused with the index created when saving the record.

Referring to Code Extract 3-4, when an armature is selected, it's associated ListIndex is written into variable ' \(\mathbf{d}\) ', the value in ' \(\mathbf{d}\) ' is then incremented by one using Let \(\mathbf{d}=\mathrm{d}+\) 1. Each entry in the Arm file is read using the Input \#1, nam, num, cnt, statement, after opening the file using Open DefaultPath \& "Arm.TXT" For Input As \#1. The value in variable 'ent' is compared to that of the value held in variable ' \(\mathbf{d}\) '. The reader should note that value read into variable 'ent' is the index that was created and assigned to variable 'a' when saving each record. When the value in variables ' \(\mathbf{d}\) ' and ' \(\mathbf{e n t}\) ' are
the same, the record holding the data for the selected armature has been identified. The data string read into 'nam' holds the name of the selected armature and the value read into the variable 'num' is the number of bars on the commutator of the selected armature. This value is read into Text Box 7 on the GUI which reflects the number of bars that remain to be tested. Each time a reading is taken this value is decremented by one until all the bars have been tested. Recall that 'd' was incremented. The reason for this is as follows. The ListCount value which was assigned to 'a' represented the number of items that was presently on the list when the last item was stored.

The number system for the ListCount method starts from one. Using the example from above, 'a' will hold and store the value six for the sixth armature added to the list. Now, when selecting an armature, the value from the current ListIndex method (held in variable ' \(\mathbf{d}\) ') is compared with the value of the stored ListCount method, (held in variable 'cnt'). The ListIndex number system begins from zero. Again using the previous example, the sixth item in the Combo Box list will return a ListIndex value of five due to the number system starting at zero. So in order for the sixth item in the Combo Box list to return a ListIndex of six, the ListIndex value is incremented by one.
```

Private Sub Combo2_Click()
Dim d As Integer
Let $\mathrm{d}=$ Combo2.ListIndex
Let $\mathrm{d}=\mathrm{d}+1$
Open DefaultPath \& "Arm.TXT" For Input As \#1
Do While Not EOF(1)
Input \#1, nam, num, cnt
If $\mathrm{cnt}=\mathrm{d}$ Then
Let Text7.Text = num
Let Text6. Text = 0
Let Text8.Text = 0
Let No_of_Bars = Val(num)
End If
Loop
Close \#1
End Sub

```

\section*{CODE EXTRACT 3-4: COMBO BOX ARMATURE SELECT - COMMAND CLICK}

The question that now arises is what happens when an armature (record) is deleted from the list? How is the saved index edited? See Code Extract 3-5.
```

Private Sub Command4_Click()
If InputBox("Enter Administrators Password", "Administrators Password") = "AdminAutoSun6" Then
If MsgBox("Are You Sure That You Want to Delete The Selected Item?",vbYesNo) = vbYes Then
Dim c As Integer
Let b = Combo2.ListIndex
Combo2.Clear
If Dir(DefaultPath \& "Arm.TXT") <> "" Then
Open DefaultPath \& "Arm.TXT" For Input As \#1
Open "Del" For Output As \#2
Do While Not EOF(1)
Input \#1, nam, num, cnt
If cnt <> (b + 1) Then
Combo2.Addltem "Armature Name:" \& nam \& " Number of Bars:" \& num
Let c = Combo2.ListCount
Write \#2, nam, num, c
End If
Loop
Close \#1
Close \#2
Kill DefaultPath \& "Arm.TXT"
Name "Del" As DefaultPath \& "Arm.TXT"
Else: MsgBox "No Armature Properties Found"
End If
End If
Else: MsgBox "You are NOT Authorised to perform this action"
End If
End Sub

```

\section*{CODE EXTRACT 3-5: CLICK TO REMOVE HIGHLIGHTED ARMATURE COMMAND CLICK}

Before clicking on the 'Click to Remove Highlighted Armature' button, an armature must have already been selected. The delete process is only initiated if the administrator's password has been entered correctly. The process entails opening the Arm file to read data, opening a further file named 'Del' to write data into, then searching for the selected armature (record) and deleting it. Each record is read from Arm, its record (variable 'cnt') index is compared to the value of ListIndex method plus one (variable 'b’).

If these two variables are not equal then that record is written into the Del file. This means that every record except the selected one is copied into the Del file hence, the

Del file holds all records except the omitted record. The selected record has been deleted from the list. The question still remains, how is the saved index values edited? Referring to Code Extract 3-5, the reader will notice that each time a record is copied into the Del file, it is copied with a new index using variable ' \(\mathbf{c}\) '.
```

Let c = Combo2.ListCount
Write \#2, nam, num, c

```

The new index associated with each record is the value of the ListCount method for the new list being created during the delete process. The original content of the Combo Box is deleted and a new list is created using the AddItem method. As an example, if the third item in the old list is to be deleted, items one and two are copied into the Del file as their saved index (variable 'cnt') is not equal to variable ' \(\mathbf{b}\) '.

When copying into the Del file, each item is also added (using the AddItem method) to the previously cleared (using the Combo2.Clear statement) ComboBox. Hence the stored index value using variable ' \(\mathbf{c}\) ' is one for item one, as after this item was added to the Combo Box list, the ListCount method returned a value of one. In the same way, item two will have an index value of 2 . Now, because item three is the item selected to be deleted, its saved index (variable 'cnt') is equal to variable 'b'.

When this occurs, the item (item three in this case) is not copied to the Del file, nor is it added to the Combo Box list. Hence the Combo Box List still contains two items and its current ListCount method value will still be two. When the fourth item is read and the index values compared, the values will not be equal. Item four is then added to the ComboBox list and also copied into the Del file. Once added to the ComboBox list, the ListCount method will return a value of three which is copied into variable ' \(\mathbf{c}\) ' and saved in the Del file as the new index for the previously known item four, but now the current renamed item three.

Hence item four, with an index value of four, from the Arm file is saved as item three with an index value of three in the Del file. Each item copied into the Del file from this point forward will be saved with a new index. After all the records (except the one selected to be deleted) from the Arm file has been copied into the Del file, the entire Arm file is deleted using the,

Kill DefaultPath \& "Arm.TXT"
statement. The Del file is then renamed Arm using,

Name "Del" As DefaultPath \& "Arm.TXT"

The new Arm file now contains all items except the one that was selected to be deleted. See Figure 3-9 for a flow chart of the delete process.



\section*{FIGURE 3-9: CLICK TO REMOVE HIGHLIGHTED ARMATURE COMMAND CLICK FLOWCHART}

\subsection*{3.1.1.3 Job Number Property Frame}


FIGURE 3-10: JOB NUMBER PROPERTY INPUT FRAME

It is in this input box that the armature serial number is entered. This serial number is reflected in the test report printout and it is also used as a file name under which the test results are saved. As will be discussed later in this chapter, tests are saved in files bearing the serial numbers of armatures as filenames in order to generate a test history for each armature. When a test is carried out on an armature with a file name (serial number) which does not appear in the file containing the list of armatures that were previously tested, that armature is added to the saved list, i.e. its serial number is added to a sequential file named 'Saved_List'.

A sequential file bearing the name of the serial number of the armature is also created and it is here that the test results are saved. When saving a test for an armature with a serial number that already exists the content of the Job Number Property frame is compared with the list of serial numbers in the 'Saved_List' file. When a match is found that file is opened and the present test details are added to it. If no match is found then a new file is created and the name of the file is added to the 'Saved_List' file.

\subsection*{3.1.1.4 Test Option Property Frame}


FIGURE 3-11: TEST OPTION PROPERTY FRAME

This property frame allows the user to choose between Automated and Manual modes by clicking on the appropriate option. Once a selection is made it is reflected in the Test Status property frame, as show on Figure 3-12 below.


FIGURE 3-12: TEST STATUS PROPERTY FRAME

In Automated mode the entire system is enabled. This means that the controller, more specifically the Automation Microcontroller (AM), controls the mechanical system according to the commands from the GUI and the Communication Microcontroller (CM). In Manual mode, the automated control functionality of the system is disabled and the AM enters power-down mode. Only the data acquisition, analysis and storage functionalities of the system are available to the user. In this mode, the test technician is responsible for placing the test probes on the commutator bars and switching the test current using a footswitch. On selecting the Manual option, ' \(G\) ' is placed into variable Auto_Man, using the statement:
```

Let Auto_Man = "G"

```

Auto_Man is read and the ASCII representation of its contents is transmitted to the CM when the test settings are being uploaded to the controller. The Load event is initiated on clicking the Load button on the GUI. More detailed discussions will follow later in this chapter. On selecting the Automated option, ' \(g\) ' is placed into the Auto_Man variable.

\subsection*{3.1.1.5 Test Parameter Property Frame}


FIGURE 3-13: TEST PARAMETER PROPERTY FRAME

The Parameter Property Frame is where the user stipulates the allowable percentage variance (i.e. percentage difference) of present reading from the reference reading. This value is then stored in variable Percentage to be used in the Calculation subprogram. Different ranges can be added and removed from the available options by the administrator in exactly the same was way as in the Armature Properties

Frame. The operation of this frame is identical to that of Armature Properties Frame therefore the author will not enter into a discussion on the operation of this frame.

\subsection*{3.1.1.6 The Date and Time Frames}


FIGURE 3-14: DATE AND TIME PROPERTY FRAME

These output fields reflect the date of a test and the test duration. On starting the test, by clicking the Start button, the date and the current time (Test Started) is uploaded from the PC's internal clock.
```

'1********** load begin time and date*******
Let Text11.Text = Space(30) \& Date
Let Text12.Text = Space(20) \& Time
timed = Second(Time)
timee = Minute(Time)
timef = Hour(Time)

```

\section*{CODE EXTRACT 3-6: RECORDING THE TIME WHEN THE TEST WAS STARTED.}

When a test ends, either naturally (when all the bars have been tested) or unnaturally (when an emergency stop has been invoked), the end time of the test (Test Ended) is uploaded from the PC's internal clock. The duration is computed as shown in Code Extract 3-7, below.
```

'*************** Time\&Date
If Emergency = False Then
Let Text13.Text = Space(20) \& Time

```
```

    timed = Second(Time) - timed
    If timed < 0 Then
    timed = 60 + timed
    timee = timee + 1
    End If
    timee = Minute(Time) - timee
    If timee < 0 Then
    timee = 60 + timee
    timef= timef + 1
    End If
    timef = Hour(Time) - timef
    If timef < 0 Then
    timed = 24 + timef
    End If
    Let Text14.Text = Space(20) & timef & ":" & Space(1) & timee & ":" &
    Space(1) \& timed
End If
\************** End Time\&Date

```

CODE EXTRACT 3-7: CALCULATION OF THE DURATION OF THE TEST

\subsection*{3.1.2 Test In Progress Fields}

\subsection*{3.1.2.1 Fault Log List}

The Fault Log list is a list that displays each reading that falls outside the specified percentage variance range. It is also the screen that is used to display all relevant test information and test history that is retrieved from stored files.


FIGURE 3-15A: THE FAULT LOG SCREEN DISPLAYING PRESENT TEST FAULTS

Figure 3-15A depicts a typical test fault log. This is what the user will see during the test as faults are recorded. Figure 3-15B below, illustrates the same test results that has been recalled from a stored file.
```

Job Number: Test Results
\Delta
Operator's Name: Sunveer Matadin
Armature Name: b Number of Bars:10
Percentage Variance: 5%
Date: 2006/04/12
Recorded Faults
Fault on Bar: 3, Percentage Variance =19.28123, Bar Reading: 0.1626973V, Reference: 0.136398V
Fault on Bar: 5, Percentage Variance =10.88503, Bar Reading: 0.1215511V, Reference: 0.136398V
Fault on Bar: 7. Percentage Variance =10.3879, Bar Reading: 0.1505669V, Reference: 0.136398V
Fault on Bar: 8, Volt-Drop Reading Is Zero (0V). Indicating A Possible Short Circuit
Fault on Bar: 9,Volt-Drop Reading Is Out Of Range, Indicating A Possible Open Circuit
Emergency Stop on Bar 10
End Of Recorded Results

FIGURE 3-15B: THE FAULT LOG SCREEN DISPLAYING RETRIEVED FILE DATA

Figure 3-15B depicts a saved test that has been recalled in order to view the stored results. Critical information such as the job (serial) number, the operators name, the type of armature (the armature name and the number of bars on the commutator), the allowable percentage variance and the date of the test is displayed.

Under 'Recorded Faults', each fault is recorded with the following information: the number of the pair of bars on which the fault was recorded, the percentage variance from the reference reading, the actual volt-drop reading across the present two bars, the actual reference reading and, in the event of an emergency stop, the pair of bars on which such a stop was initiated.

### 3.1.3 The Control Commands

The control commands are used to prompt the controller, and where necessary the automated machine, to react to a user initiated event. There are three controls that may be used under normal test conditions when none of the system errors have occurred.

These are the Load/Start, End and the Emergency Stop controls as shown in Figure 316.


FIGURE 3-16: CONTROLS FOR NORMAL TEST CONDITIONS
In the event of an error, the two controls to be used are the Continue After Error Pause and the Manual Reading as shown in Figure 3-17A and Figure 3-17B. On an error that requires a manual reading to be taken, i.e. Error1 and Error2, the Manual Reading Control is enabled and the Reading Prompt turns green. A red Reading Prompt alerts the user that the system is not ready to take a manual reading whilst a green setting indicates to the user that the system has been prepared for a manual reading procedure. The user clicks on the Manual Reading button on the GUI when the reading is about to be taken. Thereafter the user presses a Manual Reading switch situated on the automated machine after the test current is switched on and the test probes are set in place. The volt-drop reading is then captured and processed.


FIGURE 3-17A: DISABLED MANUAL READING CONTROL


FIGURE 3-17B: ENABLED MANUAL READING CONTROL

Referring to Figure 3-16, the reader will notice that the first button in the Controls frame is the Load button and all the other control buttons are disabled. This is to ensure that all the data required for a test has been entered correctly in the Test Setup Fields as discussed earlier.

Once all the data has been entered the Load button is clicked to upload the applicable information to the controller (more specifically the Communications Microcontroller). All the input data fields on the GUI are disabled when the Load button is clicked in order to ensure that the input setting can not be altered during a test. If any input data field has not been completed when the Load button is clicked a message box or an input box appears prompting the user to enter the required data. See Figure 3-18A for the flow diagram relating to this process. Once the CM has received the information it acknowledges having done so by transmitting the ASCII code for the letter 'd' back to the GUI.

On receiving this, the Load button is replaced by the Start Button and the Emergency Stop Button is enabled as depicted in Figure 3-18B. When the user is ready to begin the test the Start button is clicked and ' A ' is transmitted to the controller to begin. When the Start button is clicked it turns green, as shown in Figure 3-18C, and the mouse pointer changes to a pointer and hourglass signifying that the test is in progress.



FIGURE 3-18A: DATA FIELD VERIFICATION PROCEDURE


FIGURE 3-18B: START AND EMERGENCY STOP CONTROL ENABLED


FIGURE 3-18C: START CONTROL BUTTON CLICKED TO BEGIN TEST

After the last pair of bars has been tested the End control button is highlighted in blue as shown in Figure 3-19A below. This alerts the user that the test is complete. The user must acknowledge this alert by clicking on the End button. The End control is also enabled and highlighted when an Emergency Stop is initiated. This is further discussed below.


FIGURE 3-19A: END CONTROL HIGHLIGHTED BLUE TO ALERT USER

When the End control button is clicked, ' B ' is transmitted to the controller and the End button is highlighted in green to signify the completion of the test. This signifies that the controller has entered powerdown mode and that the data is ready to be printed and saved or only saved. Referring to Figure 3-19B, the reader will notice that the Print and Save options are now enabled. All the output fields in the Test Status Frame and all the input fields in the Test Setup Frame are cleared. Further, all control and input buttons, except for the password Enter Button, are disabled. This allows the user to begin the next test once a valid password has been entered.


FIGURE 3-19B: END CONTROL HIGHLIGHTED GREEN AFTER ALERT IS ACKNOWLEDGED

When the detection unit, containing the test probes and optical sensor, is not raised to its initial position within the allocated time Error 4 is invoked and the Continue After Error Pause control, The Emergency Stop control as well as the Error 4 status display are enabled and highlighted as depicted in Figure 3-20.

The GUI is made aware of this error when the ASCII code for the letter ' L ' is received. When this error occurs the user has to assess the problem and if the fault is not serious enough to abandon the test, the user will physically raise the unit to its initial position. Once this is done and the user is confident that the error was not due to an event that may be recurring, the user will click on the Continue After Error Pause control for the test to progress as usual. Once clicked all the control buttons and displays that were highlighted and enabled due to the error are disabled and are no longer highlighted. If the fault is deemed to be serious and possibly recurring in nature the user will then click on the highlighted Emergency Stop control to immediately stop the test.


## FIGURE 3-20: CONTINUE AFTER ERROR PAUSE CONTROL ENABLED FOR ERROR 4

The last control featured in the Controls frame is the Emergency Stop button. This functionality is enabled as soon as the test is started and remains enabled throughout the test. If at any point during the test, for whatsoever reason, the user decides that it
is unsafe to continue with the test, an emergency stop can be evoked by clicking on the Emergency Stop control button. When clicked, the Emergency Stop control is highlighted in red, the End button is enabled and the ASCII code for the Letter ' F ' is transmitted from the GUI to the CM. The CM then Sets (1) P0.5, which is connected to the AM P1.5 and P3.2 (External Interrupt 0). When the AM is interrupted due to External Interrupt 0 being triggered and P1.5 is High (1), the AM immediately initiates an emergency stop. The AM immediately halts the task that was being carried out, switches off the Test Current by Clearing (0) P2.7 and safely shuts the system down before entering Powerdown mode. The GUI reflects the fact that an Emergency Stop was evoked in the Fault Log and waits for the user to click the End button in order to end the present test.


FIGURE 3-21: EMERGENCY STOP EVOKED

### 3.1.4 Error Status Frame

The Error Status Frame is where errors are reflected as or when they occur. When no errors have occurred, the frame looks like Figure 3-22, with each error status display being disabled.


FIGURE 3-22: ERROR STATUS FRAME

When an error does occur the appropriate display is highlighted red and is enabled. Once the user clicks on the error a display message box pops up informing the user of the type of error, the cause, and possible steps to follow. Only once the error has been corrected and the controller communicates this to the GUI, will the highlighted display be disabled. Each error and flow charts depicting the steps taken when they occur will be discussed in detail in detail in Chapter 4. For the purposes of this discussion, the author will only concentrate on what events trigger these errors and on how the GUI reflects them.

Error 1 occurs when a pair of bars is not detected within an allocated time. The controller is responsible for the timing of this process and if the allocated time has elapsed before the next pair of bars are detected, the controller transmits the ASCII code for the letter ' J ' to the GUI. When the GUI receives a ' $J$ ' it immediately enables and highlights the Error 1 display as well as the Manual reading control. As mentioned earlier, a detailed discussion concerning this, and all the other errors, will follow in Chapter 4. See Figure 3-23A for a representation of the Error 1 display. When the Error 1 display is clicked the following message appears in a message box:
"The next pair of bars has not been detected within the allowable period. A Manual Reading must now be taken"


## FIGURE 3-23A: ERROR 1 DISPLAY

Error 2 occurs when the detection unit has not been lowered onto the surface of the commutator within the allowable time. Here again the controller is responsible for the timing of this process and if the allocated time has elapsed before the detection unit has been lowered, the controller transmits the ASCII code for the letter ' $m$ ' to the GUI. On receiving this character the GUI highlights Error 2 and enables the Manual reading control.


FIGURE 3-23B: ERROR 2 DISPLAY

When the Error 2 display is clicked the following message appears in a message box:
"The Test Probes have not been lowered within the allowable period. A Manual Reading must now be taken"

Error 3 occurs when the test current is switched on for a period longer than a predetermined allowable time. In this case the controller transmits the ASCII code for the letter 'L' to the GUI. Unlike the previous two errors, Error 3 initiates an immediate Emergency Stop (by transmitting the ASCII code for the letter ' F ' to the controller) and enables the End control function. The GUI still however highlights Error 3 to inform the user that the Emergency Stop was initiated due to Error 3. On clicking the Error 3 display the following message appears in a message box:
"The Test Current has been switched on for too long, and as a safety measure an Emergency Stop has been invoked. Please Click End, check the device and Restart the Test"


FIGURE 3-23C: ERROR 3 DISPLAY AND INVOKED EMERGENCY STOP

Error 4 was discussed in the explanation pertaining to the Continue After Error Pause Control, but for completeness the author will briefly discuss Error 4 here.

Error 4 occurs when the detection unit has not been raised to its initial position within the allowable time. When the allowable time has elapsed before the detection unit is raised to its initial position, the controller transmits the ASCII code for the letter 'Q' to the GUI. On receiving this the GUI highlights and enables the Error 4 display as well as the Continue After Error Pause and Emergency Stop controls as shown in Figure 3-20 and Figure 3-23D, below. The user then assesses the fault and elects to either continue with the test by clicking on the Continue After Error Pause button or stopping the test by clicking on the Emergency Stop button.


FIGURE 3-23D: CONTINUE AFTER ERROR PAUSE CONTROL ENABLED FOR ERROR 4

### 3.1.5 Test Status Display

The Status Display is responsible for the summary of the present test at any point in time. As can be seen from Figure 3-24, the information displayed includes the number of the pair of bars (i.e. first pair, second pair etc) that is currently under test, the number of pairs of bars that remains to be tested, the number of faults that were logged, the mode that the system is operating in (i.e. manual or automated) and the
task that the system is presently performing (i.e. either searching for the next pair of bars or taking a reading).


FIGURE 3-24: TEST STATUS DISPLAY

### 3.1.6 Recorded Test Data Option

The user has four options when it comes to the handling of recorded test data. These are the print, save, open and delete options. Each will be discussed individually in the subsections that follow. Below is a representation of which options are available at different stages of the process.

Figure 3-25A depicts the options available after the correct password is entered but before a test has started. Figure 3-25B depicts the options available while a test is in progress and Figure 3-25C depicts the options available at the end of a test.


FIGURE 3-25: TEST DATA OPTIONS

### 3.1.6.1 Print Option

A printed test report is useful for three reasons. Firstly, a hard copy of a specific test or a test history of an individual armature can be made available. The second reason is that a written record travels with the armature after this test so that staff in the next stage of the process will have a written record of the test and failures recorded therein. The third use for a printed test report is that it aids in accountability, i.e. the technician that performs the test can be held accountable for the test and the results as his/her name appears in the test report as well as his/her signature acknowledging the faults.

The user may view and print saved test records by opening a specified file using the Open button. It is for this reason that the print option is made available to the user after the correct password is entered but before a test is started. When Print is clicked, all the data contained in the opened file is printed in the format shown in Appendix D. If a file was not opened, thus implying that no data is displayed when Print is clicked, the following message appears:
"No Data Available To Print"

Once a test is in progress the print option is disabled until the end of the test when it is again enabled. Here, when Print is clicked, only the data recorded during the test that was just completed is printed in the format shown in Appendix E. One of the main features of this new system is the fact that test data can be printed and stored. It is for this reason that when the user prints the present test the data is also automatically saved in the appropriate file.

### 3.1.6.2 Save Option

As mentioned above, when a completed test is printed it is also automatically saved therefore there is no need to click on the Save button. The Save button is useful when the user wishes to only save the present test data without having a printed copy.

A dual sequential file system is used to save a test record. The first sequential file is the one used to store the names or serial numbers of the armatures that have been tested and saved, in order to generate a list when required. This file is named DefaultPath \& "Saved_List.TXT" as shown in Code Extract 3-8. DefaultPath is the specified location of the file named Saved_List. The above-mentioned list is available when the user clicks on the Open or Delete buttons.

The second sequential file is the one in which the test data is saved. The file name is the serial number of the armature under test. Each record added to this file has the following fields: the serial number of the armature, the name of the test technician, the type of armature, the allowable percentage variance specified for the test, the date of the test and recorded faults (if any) read by incrementing the index number of the Fault Log list and the actual fault logged on that pair of bars. In other words, each fault recorded in the Fault Log list is saved in the file with the test parameters and identification data fields preceding it. A typical record in the file is found below,
"matadin","sun 04/05","Armature Name: f Number of Bars: 50","Percentage Variance: 20\%","2005/05/04","Emergency Stop on Bar 0"

The flow diagram for the Save event is depicted in Figure 3-26 and the code for this event is shown in Code Extract 3-8.


FIGURE 3-26: SAVE EVENT FLOW DIAGRAM

```
Private Sub Command15_Click()
Dim Add_Flag As Boolean
Command14.Enabled = False
Command15.Enabled = False
Let Add_Flag = False
Let Save_Test = Text9.Text
If Dir(DefaulPPath & "Saved_List.TXT") <> "" Then
    Open DefaultPath & "Saved_List.TXT" For Input As #7 ' file for the list of all jobs saved
        Do While Not EOF(7)
            Input #7, Add_list
            If Add_list = Save_Test Then
                    Let Add_Flag = True
            End If
        Loop
    Close #7
        If Add_Flag = False Then
            Let Add_Flag = False ' redundant
            Open DefaultPath & "Saved_List.TXT" For Append As #7
            Write #7, Save_Test
            Close #7
        End lf
Else
        Open DefaultPath & "Saved_List.TXT" For Append As #7
        Write #7, Save_Test
        Close #7
End If
    Open DefaulPPath & Save_Test For Append As #5
    Let i=0
    Do While i <= (List1 ListCount - 1)
        Write #5, Text9.Text, Text2.Text, Combo2.List(Combo2.ListIndex),
                        Combo1.List(Combo1.ListIndex), LTrim(Text11.Text), List1.List(i)
        Let i = i + 1
    Loop
    Write #5, "End", "xxx", "xxx", "xxx", LTrim(Text11.Text), "End Of Recorded Results"
    Close #5
```

End Sub

## CODE EXTRACT 3-8: SAVE - EVENT CLICK

After the last item from the Fault Log has been saved, a record containing 'xxx' in the user name, armature name and allowable percentage variance fields together with the serial number field is saved to indicate the end of a test record.
"End","xxx","xxx","xxx","2005/05/04","End Of Recorded Results"

### 3.1.6.3 Open option

This option is only available to the user after a valid password has been entered. By clicking on Open, the user may view any and all saved tests. When clicked an input box as shown in Figure 3-27 appears prompting the user to enter the serial number of the armature for which the test data is wished to be viewed. When this number has been entered all the recorded tests for that serial number i.e. the armature test history, are displayed on the Fault Log display.


## FIGURE 3-27: INPUT PROMPT WHEN ‘OPEN’ IS CLICKED

In order to refine the search, for example if a test on a specific date is required, the user enters 'Find' in the input box. A list of armature serial numbers appears as shown in Figure 3-28. This list is generated by reading the 'Save_List' file mentioned above.


FIGURE 3-28: LIST OF SAVED SERIAL NUMBERS

By clicking on a serial number from this list a search is initiated. This search entails the opening of the file with the name matching the selected serial number, in this case matadin, reading through each record and displaying the dates on which tests were carried out on that armature, see Code Extract 3-9. All these dates along with a 'View All' option are displayed in a list box as depicted in Figure 3-29.

On clicking on a specific date the user may view the data recorded in the test (or tests) carried out on that armature on the specified date. By clicking on the 'View All' option a test history containing every test recorded and saved under the specified serial number is displayed, see Code Extract 3-10A and Code Extract 3-10B. The user clicks on the Exit button provided to exit from the Open procedure at any time.

```
Private Sub List2_Click()
Let Save_Test = List2.Text
List1.Clear
Let Dspl_Date = "'
List4.Clear
List4.Addltem "View All"
Open DefaultPath & Save_Test For Input As #5
    Do While Not EOF(5)
    Input #5, aa, bb, cc, dd, ee, ff
            If (Dspl_Date <> ee) And (bb <> "xxx") Then
                List4.Addltem LTrim(ee)
                Let Dspl_Date = ee
            End If
    Loop
    If List4.ListCount = 1 Then
    MsgBox "There are no items to View"
    List4.Clear
    Else
    List4.Visible = True
    End If
Close #5
End Sub
```

CODE EXTRACT 3-9: GENERATION OF A LIST OF DATES FOR A SPECIFIED SERIAL NUMBER


FIGURE 3-29: LIST OF TEST DATES FOR A SPECIFIED ARMATURE SERIAL

## NUMBER

```
Private Sub List4_Click()
List1.Clear
Let Test_Date = List4.Text
Call FopenSub
List2.Visible = False
List4.Visible = False
Command33.Visible = False
End Sub
```


## CODE EXTRACT 3-10A: EVENT CLICK - ON THE DATE LIST

```
Public Sub FopenSub()
    If Test_Date = "View All" Then
    Open DefaultPath & Save_Test For Input As #5
        Let j = False
        Do While Not EOF(5)
            Input #5, aa, bb, cc, dd, ee, ff
            If j = False Then
                List1.Addltem "Job Number: " & aa
                    List1.Addltem "Operator's Name: " & bb
                        List1.Addltem cc
            List1.Addltem dd
            List1.Addltem "Date: " & LTrim(ee)
            List1.Addltem ""
            List1.Addltem "Recorded Faults "
            List1.Addltem "'
            List1.AddItem ff
```

```
                Let j = True
            Else
            List1.Addltem ff
                        If aa = "End" Then
                Let j = False
                List1.Addltem ""
                List1.Addltem ""
                    End If
                End If
            Loop
            Close #5
    Else
    Open DefaultPath & Save_Test For Input As #5
        Let j = False
        Do While Not EOF(5)
            Input #5, aa, bb, cc, dd, ee, ff
                If (Test_Date = LTrim(ee)) Then
                    If j = False Then
                        List1.Addltem "Job Number: " & aa
                        List1.AddItem "Operator's Name: " & bb
                        List1.Addltem cc
                        List1.Addltem dd
                        List1.AddItem "Date:" & LTrim(ee)
                        List1.AddItem ""
                        List1.Addltem "Recorded Faults "
                        List1.Addltem ""
                        List1.Addltem ff
                        Let j = True
                    'End lf
                    Else
                            List1.Addltem ff
                                    If aa = "End" Then 'xxx (or End) signals end of a test and all the fields for
                                    the next test has to be printed
                                    Let j = False
                                    List1.Addltem ""
                                    List1.Addltem ""
                                    End If
                    End If
                End If
            Loop
    Close #5
    End If
'aa is the Job No field
'bb is the Operators Name field
'cc is the Armature Selection field
'dd is the Percentange Variance field
'ee is the Date field
'ff is the Recorded Faults field
End Sub
```

CODE EXTRACT 3-10B: FOPEN SUBPROGRAM CALLED IN CODE

### 3.1.6.4 Delete Option

The delete option allows a user with administrative rights to delete a file with a specified serial number. When an armature is discarded it may be decided that the history of that armature is no longer relevant however, the opposite may also be true. The relevance of the history of a discarded armature can only be decided by the workshop management and maintenance engineers.

The Delete option works in much the same way as the Open option. All the records with the specified serial number are located when that serial number is entered into the input box prompt or, a list containing all the saved serial numbers is generated when "Find" is entered into the input box as depicted in Figure 3-30. The difference however is when the Delete button is clicked, the GUI requests the Administrator's password. If the password is entered correctly and a serial number is selected the GUI will ensure that the user is sure of his decision by prompting a response using a pop up box as shown in Figure 3-31.


FIGURE 3-30: LIST OF SERIAL NUMBERS GENERATED ON THE DELETE

## CLICK EVENT



FIGURE 3-31: POP UP PROMPT ON SELECTING AN ITEM TO BE DELETED

If Yes is selected by the user the deletion process is initiated. This process entails the removal of the selected serial number from the sequential file that generates the list of saved serial numbers, i.e. "Saved_List.TXT", as well as removing the file that contains the test history saved under the name of the selected serial number. Removing the selected item from the "Saved_List.TXT" file is accomplished by reading this file and copying all items except the one selected into another file, in this case 'Saved_List_Del". At the end of this process, 'Saved_List.TXT"' is deleted and 'Saved_List_Del" is renamed as "Saved_List.TXT"'.

To delete the file containing the test history the following statement:
Kill (DefaultPath \& Save_Test)
is used to remove the file with the name stored in Save_Test (which is the serial number of the selected item) using DefaultPath to locate it. See Figure 3-32, Code Extract 3-11A and Code Extract 3-11B, for the associated flow diagram and code respectively.


FIGURE 3-32: DELETE PROCESS FLOW DIAGRAM

```
Private Sub Command32_GotFocus()
If Form3.AdminPasswordFlag = True Then
Let Form3.AdminPasswordFlag = False
Save_Test = InputBox("Enter File Name", "Delete file")
    If Save_Test <> "" Then
        If Save_Test <> "Find" Then
            If Dir(DefaultPath & Save_Test) <> "" Then
                        Open DefaultPath & Save_Test For Input As #5
                        If MsgBox("Are You Sure That You Want to Delete The Selected Item?", vbYesNo,
                            "Confirm Delete") = vbYes Then
                                Call Delete
                End If
                    Close #5
                    Else: MsgBox " File Does Not Exist", vbOKOnly, "Data Error"
            End If
        Else
        If Dir(DefaultPath & "Saved_List.TXT") <> "" Then
        Open DefaultPath & "Saved_List.TXT" For Input As #7
        List3.Clear
            Let Del_Hold = "'
                Do While Not EOF(7)
                Input #7, Delx
                    If Del_Hold <> Delx Then
                        List3.Addltem Delx
                        Let Del_Hold = Delx
                        End If
                    Loop
                            If List3.ListCount <> 0 Then
                            List3.Visible = True
                            Command34.Visible = True
                            Else
                            MsgBox "There Are No Tests To View", vbOKOnly, "Data Error"
                    End lf
                Close #7
        Else: MsgBox "There Are No Tests To View", vbOKOnly, "Data Error"
        End If
        End If
    Else: MsgBox "Job Number Not Entered", vbOKOnly, "Enter Data"
    End lf
'Else
'MsgBox " You are Not Authorised to use this fuctionality"
End If
End Sub
```

CODE EXTRACT 3-11A: DELETE FILE CODING

```
Public Sub Delete()
If \(\operatorname{Dir}(\) DefaultPath \& "Saved_List.TXT") <> "" Then
Open DefaultPath \& "Saved_List.TXT" For Input As \#7
    Open "Saved_List_Del" For Output As \#8
        Do While Not EOF(7)
        Input \#7, look
            If Save_Test <> look Then
                Write \#8, look
            End If
        Loop
                Close \#7
                Close \#8
                Kill DefaultPath \& "Saved_List.TXT"
                Name "Saved_List_Del" As DefaultPath \& "Saved_List.TXT"
    Else: MsgBox "File Does Not Exist"
    End If
    If Dir(DefaultPath \& Save_Test) <> "" Then
    Kill (DefaultPath \& Save_Test)
    List1.Clear
    End If
    End Sub
```

CODE EXTRACT 3-11B: DELETE SUBPROGRAM CODING

### 3.1.7 Directory Path Specification

The Directory Path specifies the location where all files generated and accessed by the GUI are saved. This location is copied into the variable DefaultPath which precedes the file name. Using DefaultPath files can be saved on the local hard drive, written to removable data storage devices or, by mapping a network drive, files can be stored in allocated locations on the network.

The Directory Path settings can be viewed and reset via the Directory Path frame. The Directory Path frame is made visible by clicking on the View Setting button found on the View/Change Directory Path Settings Frame. The user can return to the View/Change Directory Path Settings Frame from the Directory Path Frame by clicking on the Exit Settings button. See Figure 3-33A and Figure 3-33B.

View/Change Directory Path Settings
View Settings

View User Profile Setup
View User Profile

FIGURE 3-33A: DIRECTORY PATH SPECIFICATION


## FIGURE 3-33B: DIRECTORY PATH SPECIFICATION

Visual Basic provides a simple approach for displaying drives, directories and files. All of these can be viewed using,

```
Private Sub Drive1_Change()
Let Dir1.Path = Drive1.Drive
End Sub
```

to display directories in the selected drive and
Private Sub Dir1_Change()
Let File1.Path = Dir1.Path
End Sub
to display files in the selected directory.

The Default Path can only be set or changed by an administrator. A directory path is selected using the drive, directory and file input boxes. The administrator then clicks on 'View Selected Path' to verify that this is the correct selected destination. When satisfied with the selected path the administrator clicks on Change Default Path. An input box, which prompts the administrator for the administrator's password, appears and if the correct password is entered, the selected path is saved as the new default directory path.

The default path can also be viewed by clicking on the 'View Default Path' button. The Default Path setting is dynamic (i.e. it can be changed when required and is not hard-coded) and points to the location in memory in which data can be saved. The Default Path itself also has to be saved in a file so that it can be referred to whenever
the default path is required. The location of this file however, is static i.e. it is hardcoded and cannot be changed by the user nor the administrator.

The name and location of this file is SavePath and "C:\Program Files\SavePath" respectively. When the GUI is loaded for use each time it is initiated, the Form_Load procedure opens the SavePath file and copies its contents into the Default Path variable. See Code Extract 3-12. This is carried out on the onset of a test so that the Default Path variable can be accessed whenever the path is required instead of opening, reading and closing a sequential file each time it is required.

If Dir("C:|Program Files|SavePath") <> "' Then<br>Open "C:IProgram FilesISavePath" For Input As \#10<br>Input \#10, DefaultPath ' holds the path to the saved files<br>Close \#10<br>Else<br>MsgBox "Default Path is Not Valid, it has been changed"<br>Command17.Enabled $=$ False<br>End If

## CODE EXTRACT 3-12: INITIALISING THE DEFAULT DATA PATH

### 3.1.8 Exit Command

The exit command allows the user to exit from the GUI before a test is started or after the test has ended. The Exit functionality is disabled during a test.


FIGURE 3-34: EXIT COMMAND CLICK

### 3.2 Percentage Variance Calculation.

All the literature in this chapter thus far has concentrated on the activities of the GUI when being prompted by a user or the controller and the output commands or signals that are transmitted by the GUI to the controller based on the data received and calculations carried out by the GUI. One such calculation is carried out when the GUI receives the test data from the Analogue-to-Digital converter (ADC) via the CM. This is the calculation of the percentage variance of the present reading from the stored reference reading. This is arguably the most critical calculation as the need for the entire project has evolved around it. Referring to Code Extract 3-13, the author will discuss this subprogram in as much detail as possible.



FIGURE 3-35: FLOW DIAGRAM FOR THE CALCULATION SUBPROGRAM

```
Public Sub Calculation()
Picture8.BackColor = QBColor(4)
Picture9.BackColor = &H8000000F
StnBit_WD = ((High_Byte * 256) + Low_Byte)
'*******************Actual Voltage Reading*****************
Let ActVolReadRes = (4.096 / 65536)
Let ActVolRead = (StnBit_WD * ActVolReadRes)
Let mVActVolRead = (ActVolRead / Gain)
'*******************End Actual Voltage reagings************
' set Reference value on first reading
If Initial_Count = 0 Then
    Let Reference = StnBit_WD
    Let ActReference = (Reference *ActVolReadRes)
    Let mVActReference = (ActReference / Gain)
End If
If Reference <> 0 Then ' checking if reference value =0
' calc variance of current reading
    If Initial_Count > 0 Then
```

```
Current_Variance = (((Abs(StnBit_WD - Reference)) / Reference) * 100)
End lf
' compare to selected % variance and log if a fault
If (Current_Variance > Percentage) Then
List1.Addltem "Fault on Bar: " & Text6.Text & ", Percentage Variance = " & 
    "Current_Variance & ", Segment Reading: " & ActVolRead & "V" & 
    ", Reference Reading: " & ActReference & "V"
Let Text8.Text = Val(Text8.Text) + 1
End lf
'end current reading and comparison
    Command9.Enabled = False 'disables man reading but and dsply
    Frame20.Enabled = False
    Picture5.BackColor = QBColor(12)'
    Frame21.Enabled = False
    Let Command10.Enabled = False ' error1
    Command10.BackColor = &H8000000F
    Frame14.ForeColor =&H80000012
    Frame14.FontSize = 8
    Frame14.FontBold = False
    Let Command11.Enabled = False ' error2
    Command11.BackColor =&H8000000F
    Frame16.ForeColor = &H80000012
    Frame16.FontSize = 8
    Frame16.FontBold = False
    MSComm1.Output = "E" ' to microcontroller
    Picture8.BackColor = &H8000000F
    Picture9.BackColor = QBColor(10)
    ' checking the 1st 5 readings to see if the ref reading is from a fault bar.
Let Initial_Count = Initial_Count + 1
    If (Initial_Count = 6) And (Val(Text8.Text) = 5) Then
    Let Reference = StnBit_WD
    Let ActReference = (Reference * ActVolReadRes)
    Let mVActReference = (ActReference / 1000
    Let Text8.Text = ""
    Let No_of_Bars = ((Val(Text6.Text) + Val(Text7.Text)) - 1)
    Let Text7.Text = No_of_Bars
    Let Text6.Text = 1
    Let Initial_Error = True ' flag to indicate Ref value error.
    List1.FontBold = True
    List1.Addltem "Test Restarted, Bar 5 is reset as the Initial (First) Bar!"
    List1.FontBold = False
    End If
```

```
MsgBox " The Recorded reference value is 0 Volts \& is therefore not Valid. Please Restart this Test"
```


## End If

```
End Sub
```


## CODE EXTRACT 3-13: CALCULATION SUBPROGRAM

This subprogram has two objectives; the first is to calculate the percentage variance of a present reading from the reference reading whilst the second objective is centered around the reference reading itself. Consider this, what if the reference reading is in fact a fault reading, i.e. what if the reference reading is the reading across an open or short circuit or a damaged winding on the armature? The first step would be to check if the first reading recorded is very close or equal to zero volts.

This would indicate a short circuit and this value will therefore not be stored as a reference value. A true open circuit would be indicated by a reading that is very close or equal to the supply voltage. But the supply voltage and current is not the same for every type of armature tested due to the armature characteristics as well as the arc length between the test current supply probes on the commutator. Also considering that damaged and potentially problematic windings also have to be detected, there is no clear cut value that can be used to reject a reference reading (that is other than the reading for a short circuit). In order to detect that the reference value being used is indeed a value that was recorded on a fault winding, the GUI performs a check after the first five readings taken, after the reference reading.

This essentially means that this check is carried out on the sixth reading captured. Variable Initial Count keeps track of the number of readings taken and by recalling an earlier discussion regarding the Test Status display, the reader will remember that the number of faults recorded is displayed in a text box (Text8). Noting this, and as shown in Code Extract 3-13, in the event that the value in Initial Count is six and the value of Text8 is five,

$$
\text { If (Initial_Count = 6) And }(\text { Val(Text8.Text })=5) \text { Then }
$$

this event will indicate that five (5) faults have been logged immediately after the reference value was set.

If such an event occurs, the GUI will conclude that based on the last five captured readings, the reference value was set on a fault or damaged winding reading. The reference value is then reset to that of the value recorded on the present bar (which will be the sixth bar). The values in the Test Status display as well as the variables that hold the values that reflect the number of bars that remain to be tested and the bar presently under test, are also adjusted appropriately to reflect this change. The test is reset on the sixth bar and continues as normal from that point forward.

For all of the above to occur the data transmitted from the controller has to be converted, manipulated and passed through mathematical formulae in order to obtain usable values that can be compared, displayed and stored. The following discussion will cover the manner in which this is done. Recall, that ASCII codes are transmitted by the controller. These ASCII codes are then converted into their associated numerical values in the OnComm procedure using the Visual Basic Asc function, as shown below,
Low_Byte = Asc(Serln)
and,
High_Byte = Asc(Serln)

When the calculation subprogram is called by the OnComm procedure, the Low_Byte and High_Byte variables already contain the required numerical values. The first step in the calculation subprogram is to convert these two bytes of data into the original sixteen (16) bit word that was present in the ADC register before its transmission as two separate bytes to the CM. This is accomplished using:
StnBit_WD = ((High_Byte * 256) + Low_Byte)

Once the sixteen-bit word has been realised, it is then necessary to calculate the actual voltage that this word represents. This is accomplished by dividing the ADC reference value (which is also the maximum input ADC voltage) by the sixteen-bit word when each bit is equal to 1 (i.e. 1111111111111111 which equals 65536). By doing this,
the voltage-per-bit value is obtained, or the resolution in volts (stored in variable ActVolReadRes). With an ADC internal $\mathrm{V}_{\text {Ref }}$ of 4.096 V and sixteen bit resolution, the smallest voltage increment that the input signal can broken down into is:

$$
\text { Resolution in Volts }=4.096 / 65536=62.5 \mu \mathrm{~V}
$$

This value is then multiplied by the value of the sixteen-bit word that was captured (StnBit_WD) to produce the actual voltage associated with the sixteen bit word. This actual voltage is then stored in variable, ActVoIRead. Furthermore, the actual voltage is divided by the analogue gain to obtain the true voltage reading that is present on the bars before the analogue gain. Note that the variable named "Gain" holds the value of the analogue gain as set using the Instrumentation Amplifiers external gain resistor $\mathrm{R}_{\mathrm{G}}$.

```
Let ActVoIReadRes = (4.096 / 65536)
Let ActVoIRead = (StnBit_WD * ActVolReadRes)
Let mVActVoIRead = (ActVoIRead / Gain)
```

For the calculation of the percentage variance however, these actual voltage values are not used. The percentage variance is calculated using the numerical value of the sixteen bit words that are stored in variable StnBit_WD (which holds the value of present reading) and in variable Reference (which holds the value of the reference reading). This is done in order to use values as close to the original recorded values as possible and to decrease the probability of any errors that may arise by using values that have been rounded off. The equation below is responsible for the calculation of the percentage variance of the present reading from the reference reading.

$$
\text { Current Variance }=(((\text { Abs(StnBit_WD }- \text { Reference })) / \text { Reference }) * 100)
$$


#### Abstract

Abs is a Visual Basic function that produces the absolute value of a mathematical calculation. Here it is used to provide the absolute value for the difference between the present reading value (StnBit_WD) and the reference reading value (Reference), as either value may greater than the other for any reading taken. This value is then divided by the reference value and multiplied by a hundred to obtain the percentage variance.


The next step is to compare the percentage variance value (Current Variance) to the allowable or pre-selected percentage variance that was selected by the user. Recall that this pre-selected percentage variance is stored in variable, Percentage.

```
If (Current_Variance > Percentage) Then
List1.Addltem "Fault on Bar: " & Text6.Text & ", Percentage Variance = " & 
    "Current_Variance & ", Segment Reading: " & ActVoIRead & "V" & 
    ", Reference Reading: " & ActReference & "V"
Let Text8.Text = Val(Text8.Text) + 1
End lf
```

The statements above show the comparison of the two values. In the instance where Current Variance is greater than Percentage, a fault will be recorded in the Fault Log display.

Another subprogram that is executed on every bar is the calculation of the number of bars that remain to be tested. The Bar_count subprogram decrements the number of bars remaining to be tested (stored in variable No_of_Bars) by one each time the controller transmits an increment prompt (ASCII code for the letter 'I'). This increment prompt is transmitted by the controller before the rotation of the armature under test is initiated hence the total number of bars is decremented before the very first rotation.

With this in mind, the reader will follow that when the increment signal is transmitted by the controller before the last pair of bars is tested, the decremented value in Bar_count will be zero. After the last pair of bars has been tested and when the controller next sends an ' $I$ ' the decremented value will be less than one. It is at this point that the GUI signals to controller that the last bar has been tested and that the test must now end.

The prompt to the CM that signals that the last bar has been tested is the ASCII code for the letter ' P '. For every increment signal received by the GUI before the last one, the ASCII code for the letter ' p ' is transmitted to the controller to indicate the last bar has not been tested and that rotation should be initiated. See Code Extract 3-14.

```
Public Sub Bar_count()
Let No_of_Bars = No_of_Bars - 1
If No_of_Bars < 0 Then ' <0 cos for the last bar this variable = 0
MSComm1.Output = "P"
Command6.BackColor = QBColor(9)
Command5.BackColor = &H8000000F
Command6.Enabled = True
Else
MSComm1.Output = "p"
Let Text7.Text = No_of_Bars
Let Text6.Text = Val(Text6.Text) + 1
End If
End Sub
```


## CODE EXTRACT 3-14: BAR_COUNT SUBPROGRAM

### 3.3 The Remote Graphic User Interface (RGUI)

The Remote Graphic User Interface is used by authorised users in remote locations to view test records via the network, see Appendix F for a true representation of the RGUI and Appendix G for a printout of the associated code. The RGUI can only access information when the test station GUI stores data in a location on the network by mapping the network as a drive. The Default Path that is set on the RGUI must be the same as that of the GUI on the workshop floor. The RGUI only allows users to read and print information from saved files. Note that the format in which test data is displayed is exactly the same as the format in which the GUI displays retrieved file data as shown in Figure 3-37A and Figure 3-37B.

The user cannot edit, replace or delete files from remote location. The RGUI contains three fields, namely the Search Information field, Data Display field and Directory path field. The inputs and button prompts are much the same as those on the test station GUI. They carry out the same functions and operate in the exact same way. The only variation from the test station GUI is the File Names and Refined Search Dates display lists. The File Names list and contents is the same as the list that appears on the test station GUI when the Open button is clicked. In the RGUI this list box is permanently displayed.

The Refined Search - Dates list and contents is the same as the list that appears when a serial number is clicked on in the serial number list on the GUI. Here as well, the difference is that this list box is permanently displayed on the RGUI. As in the GUI, when Open is clicked, an input box appears prompting the user to enter a serial number. If a valid serial number is entered all test results for that serial number will be displayed in the Data Display screen. If 'Find' is entered into the input box all the serial numbers of armatures are displayed on the RGUI in the File Names list.

Upon clicking on an item from this list, all dates on which tests were carried out on the selected armature as well as a 'View All' option appears in the Refined Search Dates list. By clicking on a specific date the results of test(s) carried out on that date will be displayed in the Data Display screen. If 'View All' is selected, results of all tests carried out on the selected armature are displayed. All other functionalities that are available on the RGUI operate in the same manner as those on the GUI.


FIGURE 3-36: REMOTE GRAPHIC USER INTERFACE (RGUI)


FIGURE 3-37A: REMOTE GRAPHIC USER INTERFACE (RGUI) DATA DISPLAY

Job Number: Test Results 1
Operator's Name: Sunveer Matadin
Armature Name: b Number of Bars: 10
Percentage Variance: $5 \%$
Date: 20106/04/12
Recorded Faults
Fault on Bar: 2. Percentage Variance $=4370112 \mathrm{E}-\mathrm{n2}$. Segment Reading: 0.1372522y, Reference Reading: 0.1373122y Fault on Bar: 3. Percentage Variance $=18.39461$. Segment Reading: 0.1625705y, Fieference Reading: 0.1373122 y
Fault on Bar: 4. Percentage Variance = 0.5904046, Segment Reading: 0.1365015v, Reference Reading: 0.137312zv
Fault on Bar: 5. Percentage 'ariance = 10.91533. Seqment Feading: 0.1223241V' Fieference Fieading: 0.1373122 y

Fault on Bar: 7. Percentage Variance $=10.20797$, Segment Reading: 0.1514309v, Reference Reading: 0.1373122 ,
Fault on Bar: B. Volt-Drop Reading Is Zero [TV]. Indicating A Possible Short Circuit
Fault on Bar: 9. Volt-Drop Reading ls Dut Di Finge. Indicating A Possible Dpen Cirouit
Fault on Bar: 10. Volt-Drop Reading Is Zero ([V') Indicating A. Possible Short Circuit
End DF Recorded Results

FIGURE 3-37B: REMOTE GRAPHIC USER INTERFACE (RGUI) DISPLAY
FORMAT

## Chapter 4

## Microcontrollers and Embedded Programming

In this chapter the author will discuss the core of the controller. This core comprises a pair of microcontrollers that communicate with each other via their port pins in order to perform the appropriate physical tasks, at the precise time, based on information received from the GUI and transducers on the automated machine i.e. the Physical Test Station. Both are AT89S51 microcontrollers and are enhanced derivatives of the 8051 family. These microcontrollers were chosen on the basis of them having the following essential features: four eight pin input/output ports, 4 K bytes of Flash memory, two external interrupts, two sixteen bit timers and a full duplex UART serial channel. For further information on this microcontroller, see Appendix H for a comprehensive datasheet.

A microcontroller is the bridge between software instructions (commands) and electrical hardware. Programs written in C, Assembly or any other compiler compatible language are compiled and assembled, and stored in microcontroller memory which currently is most likely to be EEPROM technology. The speed at which these programs are stepped through (or executed) is dependent on the length of time that one machine cycle takes to execute and the number of machine cycles that are required for each instruction to execute. Depending on the instruction, data is either processed or input and output ports are addressed to either read signals or produce signals from or to interfacing electrical hardware.

The length of time that one machine cycle takes to execute depends on the frequency of the oscillator that provides the clocking source for the microcontroller. This design is not time critical which means that commands based on processed information did not have to execute at a very rapid rate. It is for this reason that a 12 MHz quartz crystal was chosen to drive the on-chip oscillator resulting in a machine cycle of one microsecond $(1 \mu \mathrm{~s})$ duration. The tasks performed by these microcontrollers do not involve complex mathematical calculations or algorithms. It is for this reason that code was written in assembly language as opposed to a higher level programming
language. The advantages that assembly language have over higher level languages for these types of applications (bit manipulation, logic operations and input/output port interaction) are execution speed and the efficient use of program memory space. The Acebus development environment was used to develop and simulate the code for both microcontrollers. This tool allows the developer to write, assemble, simulate and debug code written in assembly language. In the simulation environment code can be stepped through line-by-line and the changes in the respective registers, special function registers, input/output ports etc. are reflected accordingly. See Figure 4-1A and Figure $4-1 b B$ for a screen captures of the Acebus development environment and Appendix I for a labeled representation of the development environment.


FIGURE 4-1A: SCREEN CAPTURE OF THE ACEBUS DEVELOPMENT ENVIRONMENT


FIGURE 4-1B: SCREEN CAPTURE OF THE ACEBUS DEVELOPMENT ENVIRONMENT IN SIMULATION MODE

Each microcontroller has a specific function, one being communication and acquisition of data, as preformed by the Communication Microcontroller (CM) and the other being the control of the automation tasks, as performed by the Automation Microcontroller (AM).

### 4.1 The Communication Microcontroller

The Communication microcontroller communicates with the GUI via its onboard serial port and with the Automation Microcontroller and the Analogue-to-Digital Converter (ADC) via its input/output pins (I/O pins).


FIGURE 4-2: SYSTEM BLOCK DIAGRAM

The function of the CM includes the transmission and reception of prompts to and from the GUI, the control of the ADC, the capture of data (high and low bytes) and storage thereof in two registers in its memory and the transmission of this data to the GUI for analysis. When the analysis is complete the GUI prompts the CM which in turn signals the AM to continue with the test.

While the AM is in control it communicates with the CM in the event of any system errors. If no errors occur, the AM will hand over control to the CM in order for the CM to take the volt-drop readings after the test current has been switched on and the test probes have been lowered onto the bars of the commutator. These readings are then transmitted to the GUI and so the process continues until the last pair of bars has been tested. See Figure 4-3 for the flow diagram for the CM. A discussion follows thereafter.




## FIGURE 4-3: FLOW DIAGRAM FOR THE COMMUNICATIONS MICROCONTROLLER

On power up the CM initialises the ADC (i.e. the MAX 1166). Referring to the MAX 1166 datasheet, included as Appendix J, the ADC manufacturer's application information found on page 9 suggests that a 'dummy' conversion should be run in order to put the ADC in a known state after powering up from shut down. The CM then waits for the GUI to transmit a "Status: Ready" prompt, i.e. the ASCII code for the letter ' A '. When this has been received the CM transmits ' $b$ ' to the GUI to request the mode of operation in which the test is to be run. If a ' $G$ ' is received then the test is to be run in manual mode, the CM then informs the AM of this by Clearing (0) the CM P0.6 so that the AM can enter Powerdown mode.

The CM notes that the test is being run in manual mode by setting flag 04 H in the bit addressable ram. This flag is tested in the CM Reading Subroutine in order to establish whether communication with the AM should be attempted. Recalling that AM is in Powerdown mode during a manual test any attempt by the CM to communicate with the AM will be futile and will ultimately leave the CM in a continuous wait loop as it will be waiting for communication signals from the AM that will never arrive. When flag 04H is tested in the Reading Subroutine and is found to be Set (1), the CM will not attempt to communicate with the AM as the test is
being run in manual mode. However, if this flag is tested and is found to be Low (0) the CM will establish communication with the AM as the test will be running in automated mode. If a ' g ' is received the test will be run in the automated mode. The AM will be informed of this by Setting (1) the CM P0.6. Once the CM captures the mode of operation it transmits a ' $d$ ' to the GUI to indicate that it is ready to begin the test. Recalling the discussion on the GUI Start control, it is after receiving the 'd' that the Start Button is enabled. On clicking the Start button an 'A' is transmitted by the GUI. On receiving this prompt ('A') the controller begins the test.

For the first pair of bars to be tested the CM transmits an increment prompt to the GUI, the ASCII code for the letter 'I' without waiting for an increment signal from the AM. However, after the first pair of bars has been tested, the CM will wait for the increment signal from the AM before transmitting the 'I' prompt to the GUI. The increment signal from the AM is signaled by setting its output P0.0, High (logic level 1). See Appendix K for a complete list of Input/Output port utilisations for both microcontrollers.

The input P2.3 of the CM which is directly connected to P 0.0 of the AM is then also read as a High. This High state on the CM input pin is recognised as an increment signal from the AM. This signal from the AM serves to inform the GUI, via the CM, that the system is ready to test the next pair of bars. When the increment prompt is transmitted to the GUI, the Bar_count subroutine is called in order to ascertain whether the last pair of bars has been tested. If it has been tested, the GUI transmits a ' $P$ ' to the CM to acknowledge that the test has been completed. On receiving this prompt the CM in turn informs the AM that the test is over and that Powerdown mode should be entered into. After verifying that the AM has received the command to enter Powerdown the CM itself enters Powerdown.

Note that in manual mode, the CM does not read an increment pulse from the AM as the AM is in Powerdown mode. An increment signal is generated by the user pressing on a switch that is connected to P3.6 which sends the increment prompt to the GUI.

The end of a test is signaled by the reception of a ' B ' prompt from the GUI. This prompt is transmitted when the END control button is clicked on the GUI. The
prompt ' $B$ ' is transmitted regardless of the mode in which the test has been run. However, in the automated mode the CM does not wait for the receipt of this prompt to enter Powerdown as it is already aware of the end of the test due to the AM increment signal and the GUI Bar_count subroutine.

If the last pair of bars has not yet been tested, the GUI transmits ' p '. When the CM receives this signal it instructs the AM to begin the rotation of the armature under test by setting P0.0 High. The CM now waits for the AM to detect the next pair of bars, stop the armature rotation, switch on the test current and lower the test probes onto the detected bars. Once the AM receives a signal from the detection unit indicating that the test probes are on the commutator it signals the CM to take a reading. When the CM reads P2.2 as a High it calls the subroutine that captures the volt-drop reading for the pair of bars under test. This subroutine will be discussed in detail later in this chapter. The captured data is stored as a High byte and Low Byte in two registers in the CM memory (RAM). The CM then transmits each byte to the GUI where it is analysed. Upon completion of the calculation and the analysis process by the GUI, the GUI transmits an ASCII ' E ' to the CM. This prompt serves to inform the CM that the data has been analysed and that the GUI is ready to proceed to the next pair of bars.

It should be noted here that as an additional feature, one hundred consecutive readings are captured at $1000 \mu \mathrm{~s}$ intervals and averaged for each pair of bars. The CM and GUI Reading Subroutines were therefore modified to enable this functionality. The details and discussion offered in this chapter are aimed at providing an understanding of the basic features and concepts before the more complex additional features are discussed in Chapter 6.

On receiving this prompt, the CM informs the AM that it too is ready to proceed to the next pair of bars by setting its P0.7 High (1). On receiving a High on P1.7, the AM confirms that it is ready to proceed to the next pair of bars by setting its P0.1 High (1) which is the increment signal that the CM reads on its P 2.3 . When P 2.3 is read as a High (1) the CM transmits the increment prompt ('I') to the GUI.

The CM follows this process until the last pair of bars has been tested or until any one of the four possible system errors interrupts the process flow. When such an interrupt
is encountered there is a branch from the main program flow to an interrupt handling procedure (an ISR) that caters specifically for the encountered error. Once the error has been 'handled' control is handed back to the main program. These Interrupts, their associated Interrupt Service Routines (ISRs) and critical subroutines will be discussed in the sections that follow. See Appendix L for the source code for both the Communication and Automation microcontrollers.

### 4.1.1 Microcontroller Initialisation

On power up the microcontroller must perform an initialisation procedure to ensure that all the ports, timers and special function registers are set up appropriately to undertake the tasks that they are assigned. As the name indicates, the AT89S51 input/output ports can be used as either inputs that read signals from the interfacing digital system or outputs that transmit signals to the interfacing digital system. Each pin can be addressed independently and can therefore be configured individually as an input or an output pin. Pins can be configured as inputs by writing a logic level 1 (High) to their port latches. If a port latch contains the logic level 0 (Low), it will be configured as an output pin. Code Extract 4-1 shows the input/output port configuration for the CM as depicted in Appendix K.

| MAIN: | MOV | $\mathrm{FO}, \# 00000100 \mathrm{~B}$ |
| :--- | :--- | :--- |
|  | MOV | $\mathrm{Fl}, \# 11111111 \mathrm{~B}$ |
|  | MOV | $\mathrm{F} 2, \# 01111110 \mathrm{~B}$ |
|  | MOV | $\mathrm{F} 3, \# 01010111 \mathrm{~B}$ |

## CODE EXTRACT 4-1: COMMUNICATION MICROCONTROLLER I/O PORT CONFIGURATION

Also to be initialised are the various Special Function Registers (SFRs) and Timers as shown in Code Extract 4-2.

```
MAIN2: MOV
    GCON #01010000B
    MOV TMOD,#20H
    MOV TH1r#-13
    SETB TRI
MOV IEr#10000000B
MOV IPr#00010000B
SETB ITI
```


## CODE EXTRACT 4-2: INITIALISATION OF SPECIAL FUNCTION REGISTERS FOR THE CM

Special Function Registers are associated with specific microcontroller features, properties and settings. For example, the SCON SFR is used in conjunction with the serial port, the TMOD SFR is used in conjunction with the timers, and the IE and IP SFRs are used in conjunction with the interrupts. It is for this reason that the author has opted to discuss the initialisation of these SFRs when discussing their associated microcontroller features.

### 4.1.2 Serial Port

The serial port provides a means of data transmission and reception. A parallel-toserial conversion takes place on transmission of data and a serial-to-parallel conversion takes place on reception of data. In other words, when data from a register which holds data as eight parallel bits needs to be transmitted serially, i.e. one bit after the other, a parallel-to-serial conversion needs to take place. And when receiving serially transmitted data and storing it in a register the opposite conversion, i.e. a serial-to- parallel conversion, must take place. See Figure 4-4A and Figure 4-4B.

Eight Bit Register


FIGURE 4-4A: SERIAL PORT DATA TRANSMISSION

Eight Bit Register

| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |



Serial Data Reception

## FIGURE 4-4B: SERIAL PORT DATA RECEPTION

The AT89S51 serial port features full duplex operation and two SFRs that provide access to the serial port. These are the SCON and the SBUF registers. SBUF, the serial port buffer, is in fact two individual buffers/registers. A write-only register is accessed when SBUF is written to when the data is to be transmitted and the readonly register that is accessed when SBUF is read from when data has been received. For example, the statement:

MOV SBUF, A
transmits data from the general purpose register, i.e. the Accumulator (A), by copying the value from A to the SBUF register. Similarly using:

$$
\operatorname{MOV} \quad A_{r} \operatorname{SBUF}
$$

received data is read from the SBUF register and copied into A. The SCON special function register, when initiated, sets the mode in which the serial port will operate as well as the individual bits that enable reception, sets flags etc. The statement:

$$
\text { MOV } \quad \mathrm{SCON}, \# 01010000 \mathrm{~B}
$$

initialises the serial port for operation in mode 1 by setting bits SCON. $7=0$ and SCON. $6=1$. The Receive Enable bit, SCON. 4 is also set to enable the reception of characters.

| Bit | Symbol | Address | Description |
| :---: | :---: | :---: | :--- |
| SCON.7 | SM0 | 9FH | Serial Port mode bit 0 |
| SCON.6 | SM1 | 9EH | Serial Port mode bit 1 |
| SCON.5 | SM2 | 9DH | Serial Port mode bit 2 |
| SCON.4 | REN | 9CH | Receive Enable |
| SCON.3 | TB8 | 9BH | Transmit bit 8. Ninth bit transmitted in modes 2 \& 3 |
| SCON.2 | RB8 | 9AH | Receive bit 8. Ninth bit received in modes 2 \& 3 |
| SCON.1 | TI | 99H | Transmit Interrupt flag |
| SCON.0 | RI | 98H | Receive Interrupt flag |

## TABLE 4-1: SERIAL PORT CONTROL (SCON) REGISTER SUMMARY SOURCE: THE 8051 MICROCONTROLLER (REFERENCE BOOK)

The serial port can operate in one of four modes. In Mode 1 the serial port operates as an eight bit UART (Universal asynchronous receiver/transmitter) with variable Baud Rate. The baud rate is set to 2400 using Timer 1. In this mode, transmission and reception involves ten bits. The first bit being the start bit which is always a Low (0), followed by eight bits of data with the leading bit being the LSB and a stop bit which is always a High (1). Setting of the baud rate is discussed in this chapter under Timers i.e. Section 4.1.4.

| MAIN2: | MOV | SCON, \#01010000B |
| :--- | :--- | :--- |
|  | $M O V$ | TMOD, \#20H |
|  | $M O V$ | $T H 1, \#-13$ |
|  | GETB | TR1 |

## CODE EXTRACT 4-3: SERIAL PORT AND BAUD RATE INITIALISATION

### 4.1.3 Interrupts and Interrupt Service Routines (ISRs)

In real world applications, systems are required to respond to random events that may or may not occur and if they do occur the time at which they do so cannot be predicted. It is this random, unpredictable nature of the event that makes it difficult to program the event detection and handling as part of a process flow or main program. A normal program flow is defined and executes statement by statement, jumps, calls subroutines and returns from subroutines, hence leaving no allowance for random, unpredictable events.

The most efficient way to handle such events is to pause the normal program flow or the main program, which operates at base-level, jump to a location in memory in which code for handling the event resides (the Interrupt Service Routine), execute the ISR at interrupt-level and then return control to the main program. An Interrupt Service Routine is a block of code that is developed to handle the specific event that triggers its associated interrupt. A microcontroller has various interrupt sources which indicates that such an event has occurred. The AT89S51 has two External Interrupts, two Timer Interrupts and a Serial Port Interrupt. The CM however, only makes use of one external interrupt, External Interrupt 0, and the Serial Port Interrupt.

Whenever a specified event occurs, an interrupt is triggered. Each interrupt has an associated flag to signal that a specific interrupt has occurred. All flags, except the serial port interrupt flags, and level triggered external interrupts flags, are cleared by hardware, i.e. the programmer does not have to clear the flag using software because flags are automatically cleared when vectoring to the ISR. Edge triggered external interrupts flags are cleared by hardware and are therefore favored for this application. When a serial port interrupt occurs the source of the interrupt, i.e. whether the interrupt was triggered on a receive or transmit event, needs to be verified. The only way of verifying this is by checking the status of each flag. The serial port flags must therefore be cleared in software after being checked.

Each interrupt also has an assigned location in memory in which its ISR should reside. See Table 4-2 below. When an interrupt occurs, the location in memory allocated to the associated interrupt is loaded into the Program Counter (PC). This value (location) is called the interrupt vector.

| Interrupt | Flag | Vector Address |
| :---: | :---: | :---: |
| System Reset | RST | 0000 H |
| External Interrupt 0 | IE0 | 0003 H |
| Timer Interrupt 0 | TF0 | 000 BH |
| External Interrupt 1 | IE1 | 0013 H |
| Timer Interrupt 1 | TF1 | 001 BH |
| Serial Port Interrupt | RI or TI | 0023 H |

TABLE 4-2: INTERRUPT VECTORS SOURCE: THE 8051 MICROCONTROLLER

The reader will notice that each interrupt has only eight bytes of memory in which to code the ISR. In the event that an ISR is longer than eight bytes, a jump statement is used to direct the program counter to another location in memory. Note that the program counter (PC) holds the memory address of the next statement (instruction) that is to be executed.

| ORG | OH |
| :--- | :--- |
| LJMP | MAIN |
| ORG | $0003 H$ |
| LJMP | EXOISR |
| ORG | $0023 H$ |
| LJMP | SPISR |

## CODE EXTRACT 4-4: CM VECTORING ADDRESSES

Referring to Code Extract 4-4 on a system reset (or startup), the program counter is loaded with the Reset vector address $(0000 \mathrm{H})$, when at this location, the program counter is then loaded with the address of the MAIN label thus executing a jump to the location in memory where the main program resides under the label MAIN. When External Interrupt 0 is triggered, the PC is loaded with the External Interrupt 0 vector address $(0003 \mathrm{H})$.

When at this location, the PC is loaded with the vector address for the EXOISR label. This label represents the beginning of the External Interrupt 0 ISR. The program then jumps to the location in memory where this label resides and executes each instruction in the ISR until the RETI (return from interrupt) instruction. This instruction signals the end of the ISR and hands over control to the main program so that it may continue from where it left off. All interrupts are handled in the same way.

### 4.1.3.1 Interrupt Enabling

The Interrupt Enable (IE) register is responsible for the enabling and disabling of all interrupts. Each interrupt is enabled and disabled individually by addressing the specified bit. However, if the Global enable/disable bit EA, is not set High (1), none of the individual interrupts can be enabled. Therefore by Setting (1) or Clearing (0)
the Global enable/disable bit all individually enabled interrupts can be enabled or disabled at the same instant. Interrupts can be enabled or disabled anywhere in program code by using statements such as the following:

```
SETB EXO
SETB EA
CLR EXO
```

or by addressing the entire IE register. all the interrupts can be individually enabled or disabled using one statement. This method is used most often when initialising the interrupts as shown in Code Extract 4-2 and in the statement below.
MOV IE, \#10000000E

This statement sets the Global enable/disable bit High (1), thus enabling the use of interrupts whenever they are individually enabled during the program. Table 4-3 presents a summary for Interrupt Enable register.

| Bit | Symbol | Bit Address | Description (1=Enable, 0 = Disable) |
| :---: | :---: | :---: | :--- |
| IE. 7 | EA | AFH | Global enable/disable |
| IE.6 | - | AEH | Undefined |
| IE.5 | - | ADH | Undefined for the AT89S51 |
| IE.4 | ES | ACH | Enable Serial Port Interrupt |
| IE.3 | ET1 | ABH | Enable Timer 1 Interrupt |
| IE.2 | EX1 | AAH | Enable External 1 Interrupt |
| IE.1 | ET0 | A9H | Enable Timer 0 Interrupt |
| IE.0 | EX0 | A8H | Enable External 0 Interrupt |

## TABLE 4-3: INTERRUPT ENABLE REGISTER SUMMARY SOURCE: THE 8051 MICROCONTROLLER

### 4.1.3.2 Interrupt priority

The events that trigger certain interrupts may be more critical than the events that trigger others, these critical events therefore demand immediate attention. This may entail the interruption of an already executing ISR that was triggered by an earlier event, i.e. the non critical ISR must be interrupted to hand over control to the more critical ISR. This is achieved by using the Interrupt Priority (IP) register. By setting the bit assigned to a certain interrupt High (1), that interrupt is assigned a high-level priority and can therefore interrupt the ISR of an interrupt with a low-level priority if
required. The interrupt priority can be set when initialising the interrupts as shown in Code Extract 4-2 and in the statement below.

```
MOV IF,#00010000B.
```

Referring to Table 4-4, for a summary of the IP register, the reader will notice that in the instruction above only bit IP. 4 is set High (1). This means that of all the interrupts that are, or will be enabled, the serial port interrupt has the highest priority and its ISR takes precedence over any program, subroutine or ISR that is executing at the time.

| Bit | Symbol | Bit Address | Description (1=High Level, 0 = Low Level) |
| :---: | :---: | :---: | :--- |
| IP.7 | - | - | Undefined |
| IP.6 | - | - | Undefined |
| IP.5 | PT2 | 0BDH | Undefined for the AT89S51 |
| IP.4 | PS | 0BCH | Priority for Serial Port Interrupt |
| IP.3 | PT1 | 0BBH | Priority for Timer 1 Interrupt |
| IP.2 | PX1 | 0BAH | Priority for External 1 Interrupt |
| IP.1 | PT0 | 0B9H | Priority for Timer 0 Interrupt |
| IP.0 | PX0 | 0B8H | Priority for External 0 Interrupt |

TABLE 4-4: INTERRUPT PRIORITY REGISTER SUMMARY SOURCE: THE 8051 MICROCONTROLLER

### 4.1.3.3 Polling sequence

A fixed polling sequence determines which of two interrupts having the same priority is serviced first, if these two interrupts are triggered at exactly the same time. The polling sequence for the AT89S51 is:

- External Interrupt 0
- Timer Interrupt 0
- External Interrupt 1
- Timer Interrupt 1
- Serial Port Interrupt


### 4.1.3.4 External Interrupts

Signals from interfacing systems are processed by a digital system which then outputs a signal to one or both of the external interrupt port pins, P3.2 (pin 12) and/or P3.3 (pin 13). These interrupts can be triggered in two ways, i.e. low-level activation or negative (or falling) edge activation. In the former instance, an external interrupt is triggered when the interrupt pin is held Low (0). In the latter instance, the interrupt is triggered on a High-to-Low (1-to-0) transition. The activation mode is configured by setting or clearing the IT0 bit (which is associated with External Interrupt 0) and the IT1 bit (which is associated with External Interrupt 1) in the TCON SFR. By setting IT0 to 1 (High), as shown in Code Extract 4-2, External Interrupt 0 is configured to trigger on a negative edge.
SETB ITD

The CM makes use of External Interrupt 0 by enabling and disabling it on demand and initialising it with a low-level interrupt priority and negative-edge activation. The function of this interrupt is to indicate and service system errors if or when they occur and to inform the GUI (by transmitting a 'O') when a manual Emergency Stop has been initiated by pressing on the Emergency Stop switch (on P3.2) on the Test Station or by the activation of a safety interlock. Once the GUI has been informed of an Emergency Stop, the CM enters Powerdown mode.

Recall from Chapter 2, Errorl occurs when a pair of bars is not detected within a specified time, Error2 occurs when the test probes are not present on the surface of the commutator within a pre-selected default time, Error3 occurs when the test current is not switched off after a pre-selected default time and Error4 occurs when the test probes are not raised to their original position within a specified time.

The AM is the first to recognise any errors should they occur as system monitoring signals produced by proximity switches and other transducers are input to the AM via the interfacing digital system. The AM then sets High (1) output pins that correspond to the error that has occurred. See Appendix K and Table 4-5.

| Automation Microcontroller (AM) - Automation Control |  |  |
| :--- | :--- | :--- |
| P2.6 | $(27)$ | $\mathbf{O}$ - Error 4 - Test Probes Not Raised. |
| P3.5 | $(15)$ | $\mathbf{O}$ - Error 1 - Pair Not Detected. |
| P3.6 | $(16)$ | O - Error 2 - Test Probes Not Lowered. |
| P3.7 | $(17)$ | $\mathbf{O}$ - Error 3 - Current On-Time Exceeded. |

TABLE 4-5: TABLE OF THE AM ERROR OUTPUT INDICATION PINS

These output pins are connected to individual input pins on the CM as well as the External 0 interrupt as depicted in Appendix K and Table 4-6.

| Communications Microcontroller (CM) - Communication \& Signalling |  |  |  |
| :--- | :---: | :--- | :---: |
| P2.4 | $(25)$ | I - Error 1 - Pair Not Detected. |  |
| P2.5 | $(26)$ | I - Error 2 - Test Probes Not Lowered. |  |
| P2.6 | $(27)$ | I - Error 3 - Current On-Time Exceeded. |  |
| P3.2 | $(12)$ | I - External Interrupt 0 - All Error Inputs Connected here as well. |  |
| P3.4 | $(14)$ | I - Error 4 - Test Probes Not Raised. |  |

TABLE 4-6: TABLE OF THE CM ERROR INPUT INDICATION PINS

When a system error occurs, the AM signals the CM by setting the associated pin High (1). When any one of the error lines go High (1) the interfacing digital system also triggers External Interrupt 0 . The reason for this becomes apparent when looking at the flow diagram in Figure 4-5 and Code Extract 4-5.


FIGURE 4-5: FLOW DIAGRAM FOR EXTERNAL INTERRUPT 0 - CM

```
;***********************************;
; EXTERNAL INTERRUPT D ISR
;FOR ERRORS 1 TO 4 & Emergency Stop
;**********************************:
EXOISR: JNB P2.4,ERR2
    CALL ER1_SUB
    SETB 03H
    TME EXDOUT
ERR2: JNB F2.5,ERR3
    CALL ER2 SUB
    SETB 03H
    TMP EX0OUT
ERR3: JNB P2.G,ERR4
    CALL ER3 SUB
    TMP EXDOUT
ERR4: JNB P3.4,EXDOUT
    CALL ER4 SUB
EX0OUT: MOV A, #'O'
    CALL CH_OUT
    JMP EXT
    RETI
```


## CODE EXTRACT 4-5: CODE FOR EXTERNAL INTERRUPT 0 - CM

When the interrupt is triggered the External Interrupt 0 ISR is initiated. Once in the ISR, each input error pin is tested for a High (1) status and when an error pin is identified the associated subroutine is called to handle it. The error subroutines will be discussed in detail in the section entitled Subroutines i.e. Section 4.1.5.

### 4.1.3.5 Serial Port Interrupts

The serial port interrupt is triggered when any activity is detected on the serial port. When data is received the Receive Interrupt (RI) flag is set High (1) and when data is being transmitted the Transmit Interrupt flag is set High (1). The interrupt is triggered on either of these events. As previously mentioned, the RI and TI flags have to be cleared by software the reason for this will be discussed with reference to Figure 4-6 and Code Extract 4-6.


FIGURE 4-6: FLOW DIAGRAM FOR SERIAL PORT INTERRUPT - CM

```
;***********************************************
; GERIAL FORT ISR
;**********************************************
SPISR: CLR EXD
    JNB TI,REC
    ;CLR TI; cleared in ch_out
    JMP SP_OUT
REC: NOE
SLCH_IN:TNB RI,今
    CLR RI
    MOV A, SBUF
    CONE Ar#'B',SENXT ; END
ENDD: SETB PO.1; END TO U2
SP_END: JNB P3.4,SP_END
    CLR PO.1
    MOV PO,#OH
    MOV P1,#OH
    MOV P2,#OH
    MOV F3,#00000011B
    MOV FCON,#00000010B; FOWER DOWN
    NOE
    TMP ED
SPNXT: CJNE A,#'F'r,SP_END3 ; EMERGENCY STOP
CRNT_E: SETB PO.5
SP_ENDA:JNB P3.4,SP_ENDM
    CLR PO.5
    MOV EO,#OH
    MOV P1,#OH
    MOV P2,#OH
    MOV F3,#00000011B
    MOV PCON,#00000010B; POWER DOTNN
    NOP
    JMP ED
SP_END3:JME SE_OUT
SP_OUT: SETB EXD
    RETI
;
```

CODE EXTRACT 4-6: CODE FOR SERIAL PORT INTERRUPT - CM

The CM receives prompts as well as transmits prompts and data. The only significant events that would require the main program to be interrupted are the End event or an Emergency Stop event prompt from the GUI. Hence an ISR only needs to be initiated on a receive event or only when the RI flag triggers the interrupt. As mentioned previously, the ISR is initiated on both the receive and transmit event.

A method of exiting the ISR on a transmit event is to check the status of the TI and RI flags. As show in Code Extract 4-6, the TI flag is tested and if it is found to be High (1) a jump to the end of and an exit from, the ISR is initiated. Control is then handed over to the point in the program from which it left off. If the TI flag is not found to be set, i.e. Low (0), then the RI flag is cleared and the received data is tested to verify if it corresponds to either the End ('B') or Emergency Stop ('F') prompt. If it does correspond, the AM is instructed by the CM to enter Powerdown. Once the CM verifies the AM having received this instruction, the CM configures its port pins appropriately before also entering Powerdown.

If the received data does not correspond to either of these conditions i.e. a ' $B$ ' or ' $F$ ', the ISR is exited and control is handed over to the main program at the point from which it left off. When the ISR is initiated on a receive event that is not an End or an Emergency Stop prompt, the point at which the main program was interrupted, was a waiting point for a prompt. When control is handed back to the main program, control is handed back at this waiting point. It is here that the received data is tested again to verify whether the received prompt is the prompt that the main program was waiting for at that point.

### 4.1.4 Timers

The AT89S51 features two sixteen-bit timers, Timer 0 and Timer 1 , which can be used in any one of four modes as shown in Table 4-7. These timers make use of six special function registers, TCON, TMOD, TL0, TL1, TH0 and TH1. For this project, CM utilises Timer 1 in mode 2, auto-reload mode, to generate the required baud rate for the serial port and the AM utilises Timer 0 and Timer 1 in mode 1 , as sixteen-bit timers. In both cases, the clocking source is the on-chip oscillator which is used for
interval timing as opposed to an external clocking pulse which is used for event counting.

| Mode | M1 | M0 | Description |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 13-Bit timer mode |
| 1 | 0 | 1 | 16-Bit timer mode |
| 2 | 1 | 0 | 8 - Auto-reload mode |
| 3 | 1 | 1 | Split timer mode - Timer 0 split into two 8-bit timers \& Timer |
|  | 1 is stopped |  |  |

TABLE 4-7: TABLE OF TIMER MODES
SOURCE: THE 8051 MICROCONTROLLER

The selection between these two clocking sources is made by either setting the $C / \bar{T}$ bit in the TMOD SFR High (1) for interval timing using the on-chip oscillator or, by setting the $C / \bar{T}$ bit Low (0) for event counting using external clocking sources. When using interval timing the on-chip oscillator clocking source is followed by a divide-by-twelve stage. This means that the timer registers are incremented at a rate of $1 / 12^{\text {th }}$ the frequency of the clocking source. For example, if a 12 MHz crystal was used, as in this case, the on-chip oscillator will provide a clocking frequency of 12 MHz before the divide-by-twelve stage. After the divide-by-twelve stage the clock rate will be 1 MHz , or in terms of time, one microsecond $(1 \mu \mathrm{~s})$.

As previously mentioned, the timer makes use of six special function registers. These SFRs along with their respective purposes are summarised in Table 4-8.

| Timer SFR | Purpose | Address | Bit-Addressable |
| :---: | :---: | :---: | :---: |
| TCON | Control | 88 H | Yes |
| TMOD | Mode | 89 H | No |
| TL0 | Timer 0 Low-Byte | 8 AH | No |
| TL1 | Timer 1 Low-Byte | 8BH | No |
| TH0 | Timer 0 High-Byte | 8CH | No |
| TH1 | Timer 1 High Byte | 8DH | No |

TABLE 4-8: TIMER SPECIAL FUNCTION REGISTER SUMMARY SOURCE: THE 8051 MICROCONTROLLER

The Timer Control Register (TCON) is the only one of the timer SFRs that is bit addressable. These registers contain status bits (timer flags) and control bits (timer triggers). It is necessary to Set (1) or Clear (0) each of these bits independently and at
different times in order to control the timers. See Table 4-9 for the TCON register bit summary.

| Bit | Symbol | Bit Address | Description |
| :---: | :---: | :---: | :--- |
| TCON.7 | TF1 | 8FH | Timer 1 overflow flag |
| TCON.6 | TR1 | 8EH | Timer 1 run-control bit |
| TCON.5 | TF0 | 8DH | Timer 0 overflow bit |
| TCON.4 | TR0 | 8CH | Timer 0 overflow bit |
| TCON.3 | IE1 | 8BH | External Interrupt 1 edge flag |
| TCON.2 | IT1 | 8AH | External Interrupt 1 type flag |
| TCON.1 | IE0 | 89H | External Interrupt 0 edge flag |
| TCON.0 | ITO | 88H | External Interrupt 0 type flag |

## TABLE 4-9: TCON REGISTER SUMMARY

 SOURCE: THE 8051 MICROCONTROLLERA timer can be started or stopped using theTRx ${ }^{1}$ bit. For example when using Timer 0 , the statement:
SETB TRO
is used to start the timer. The timer register(s) will increment by one from 0000 H or from any pre-loaded value. The duration between each increment is determined by the clocking pulse, which as discussed above, provides a clocking pulse every $1 \mu$ s for a 12 MHZ crystal. The timer is stopped by using the statement below.
CLR TRD

Flags are used to indicate a timer overflow. For example, if Timer 0 is used as a sixteen-bit timer, when started, it will increment from 0000 H or a pre-loaded value, every $1 \mu$ s until it reaches the maximum sixteen-bit count, FFFFH. Once FFFFH has been reached, the counter beings counting from 0000 H again. On the FFFFH to the 0000 H transition the Timer 0 flag (TF0) is Set (1). This flag is set by hardware and is cleared by software after the status of the flag has been tested as shown below.
WAIT_T3:JNB TF1, WAIT_T3

The use of timers for long interval timing is discussed in the sub-section entitled Timers and Timer Operation i.e. Section 4.2.4 in the Automation Microcontroller discussion.

[^4]The TMOD register is used primarily to set the mode of the timers during initialisation. After initialisation the TMOD register is generally not re-addressed. See Table 4-10 for a summary of the TMOD register.

| Bit | Name | Timer | Description |
| :---: | :---: | :---: | :--- |
| 7 | GATE | 1 | Gate Bit |
| 6 | C/ $\bar{T}$ | 1 | Counter/Timer select bit. (1 $=$ event counter, $0=$ interval counting $)$ |
| 5 | M1 | 1 | Mode bit 1 |
| 4 | M0 | 1 | Mode bit 0 |
| 3 | GATE | 0 | Timer 0 gate bit |
| 2 | C/ $\bar{T}$ | 0 | Timer 0 Counter/Timer select bit. |
| 1 | M1 | 0 | Timer 0 Mode bit 1 |
| 0 | M0 | 0 | Timer 0 Mode bit 0 |

## TABLE 4-10: TMOD REGISTER SUMMARY

 SOURCE: THE 8051 MICROCONTROLLERTH0 and TH1 are the respective Timer 0 and Timer 1 High byte registers, while TL0 and TL1, are the respective Timer 0 and Timer 1 Low byte registers. Depending on the mode in which the timers are used, the SFRs are written to when pre-loading values (and incremented at each clock pulse), and/or read from when recording the time that has elapsed.

The Communication Microcontroller uses Timer 1 to set the baud rate for the serial port. The baud rate is set by the overflow rate of Timer 1 . Timer 1 is initialised in mode 2, 8-bit auto-reload mode, as shown using the second instruction in Code Extract 4-7. Referring to the third instruction in Code Extract 4-7, a reload value of -13 is stored in the Timer 1 high byte register (TH1). In this mode the Timer low byte register (TL1), is incremented by one from the pre-loaded value stored in the Timer high byte register, to FFH. On the Timer overflow, the Timer flag is set as usual but in mode 2, the re-load value that is held in the Timer high byte register, is reloaded into the Timer low byte and counting begins from this value to FFH. This cycle runs continuously.

```
MAIN2: MOV GCON, #01010000B
MOV TMOD, #2OH
MOV TH1,#-13
GETB TRI
```


## CODE EXTRACT 4-7: SERIAL PORT AND BAUD RATE INITIALISATION

The re-load value is determined by the required baud rate and the selected serial port mode that was set upon initialisation of the SCON SFR. With the serial port being initialised in mode 1 , the default baud rate is $1 / 32$ of the oscillator frequency. (Note that this value can be doubled by setting the SMOD bit in the Power Control (PCON) register, High [1]). The equation used to calculate the re-load value for a given baud rate when operating in a pre-selected serial port mode, is as follows:


Source: The 8051 Microcontroller
Substituting the values

$$
\begin{array}{rlrr}
2400 \mathrm{KHz}=\frac{\text { Timer Overflow Rate }}{32} & \ldots \ldots . . & 4-2 \\
\begin{aligned}
\text { Timer Overflow Rate }=2400 \mathrm{kHz} \times 32 & \ldots \ldots . . \\
& =76800 \mathrm{kHz} \\
& =76.8 \mathrm{kHz}
\end{aligned} & \ldots \ldots \ldots & 4-3
\end{array}
$$

What now remains to be calculated is the number of clocking cycles, at 1 MHz , it will take to provide an overflow every 76.8 kHz .

$$
\begin{aligned}
\text { Number of clocks } & =\frac{1 \mathrm{MHz}}{76.8 \mathrm{kHZ}} \\
& =13.02 \\
& \approx 13 \mathrm{clocks}
\end{aligned}
$$

Alternatively, using time instead of frequency,
from (4-4),

$$
\begin{aligned}
\text { Time }=\frac{1}{76.8 \mathrm{kHz}} & =13.02 \mu \mathrm{~s} \quad \ldots \ldots . . \quad 4-6 \\
& \approx 13 \mu \mathrm{~s}
\end{aligned}
$$

and a clocking rate of

$$
\frac{1}{1 \mathrm{MHz}}=1 \mu \mathrm{~s} \quad \ldots \ldots \ldots . \quad 4-7
$$

The number of clocks, at a rate of $1 \mu \mathrm{~s}$, that is takes to produce an overflow after $13 \mu \mathrm{~s}$ is:

$$
\text { Number of clocks }=\frac{13 \mu \mathrm{~s}}{1 \mu \mathrm{~s}}=13 \text { clocks } \ldots \ldots . . \quad 4-8
$$

This value (13) is multiplied by -1 and stored in the Timer high byte (TH1) register. Because an overflow occurs on the FFH-to-0H transition, using the negative of the calculated value, the assembler is told that the reload value is 13 less than 0 . In this way, an overflow is forced after every 13 clocks, hence providing the required baud rate.

### 4.1.5 Subroutines

Subroutines are small programs that can be called by the main program, other subroutines as well as interrupt service routines (ISRs). They often consist of a block of code that is used more than once by the calling program. When developing and debugging a program, it is easier to divide the large and often complex program into smaller programs that are less complex. These smaller programs, or subroutines, are then called at will, to perform the task that they were designed to undertake before returning control to the calling program. A subroutine is initiated by using a CALL statement, for example:

CALL DELAYLOOP
calls the subroutine labeled Delayloop. Each subroutine begins with a name or label which is used to identify the subroutine as well as its location in memory. A subroutine ends with a Return (RET) statement, which hands over control to the calling program at the instruction immediately following the CALL instruction.

At this point it is perhaps appropriate to discuss the difference between an Interrupt Service Routine (ISR) and a Subroutine. A subroutine is called at specific and
predetermined points, using a CALL statement. The program then branches to the location in memory at which the called label resides. Instructions are then executed until the RET statement is reached at which point control is handed back to the calling program at the instruction immediately following the CALL instruction. The point from which the main program branches, as well as the point of return is predetermined and known.

By contrast, the Interrupt Service Routine (ISR), is not called using a CALL statement but rather initiated when its associated interrupt is triggered in response to an event. This event can occur at any time. It can therefore not be predicted or predetermined. When an interrupt occurs, the location in memory space allocated to the associated ISR is loaded into the Program Counter (PC).

This value (location) is called the interrupt vector. When vectoring to an interrupt, the main program (which may include subroutines), is paused as control is handed over to the ISR. After the interrupt has been handled, control is returned to the main program using the Return From Interrupt statement (RETI). Control is handed over at the point from which the program was initially interrupted so that it may continue from where it left off. As opposed to a subroutine, the point at which an interrupt occurs and returns, control is unknown and cannot be predetermined. Each of the subroutines used by the Communications Microcontroller will be discussed in the sections that follow.

### 4.1.5.1 The CH_OUT Subroutine

This subroutine is called when ASCII prompts and data are to be transmitted via the serial port. The data is loaded into the Accumulator register (A), prior to the CALL statement, as show below:

$$
\begin{array}{ll}
\text { MOV } & A_{r} \#^{\top} I^{\top} \\
\text { CALL } & \text { CH_OUT }
\end{array}
$$

Recalling the discussion on the serial port interrupt, the reader is reminded that the serial port interrupt is triggered when either the RI or TI flag is set. When data is transmitted, the TI flag that is set to signal the end of transmission of a byte will be set High (1) thereby triggering the interrupt. In order to avoid the interrupt being triggered, it is disabled using the first statement in Code Extract 4-8. However, as previously described, it is still possible to transmit data with the serial port interrupt enabled and vectoring off to the serial port ISR when TI is set High (1).

This is due to the ISR being exited when the TI flag is read and found to be High (1). On exiting the ISR control is handed back to CH_OUT to continue as normal. A choice had to be made between the two options. On one hand the serial port interrupt can be disabled for the short transmission period. The advantage of doing this is that the program is more efficient as time is not wasted unnecessarily triggering interrupts, vectoring to the ISR and testing the status of the TI flag, only to exit the ISR and return to the subroutine exactly where it left off.

The disadvantage of this option is that when the serial port interrupt is disabled the system cannot respond to an Emergency Stop immediately. It will only respond to the serial port interrupt when it is enabled again after the transmission of the byte of data. This is because the RI flag will still be Set (1) and will remain so until it is Cleared (0) by software. Considering the fact that ten bits of data is transmitted at a rate of $13 \mu \mathrm{~s}$ per bit, the worst case delay before the interrupt is handled is $130 \mu \mathrm{~s}$ and will apply if the interrupt was triggered by the RI flag immediately after the serial port was disabled.

The second option is to leave the serial port enabled during transmission. The advantage of this is that the system can respond to an Emergency Stop immediately. The disadvantage is inefficiency due to the serial port interrupt being triggered and serviced every time data is to be transmitted

If an event that is serious enough to initiate an Emergency Stop, the probability of the Emergency Stop being initiated at the exact moment that data is being transmitted is minimal. This is because the number of times data is transmitted during a typical (no system errors) cycle is five (four times during transmission of data and once for the transmission of prompts) and the duration of each transmit operation is $130 \mu \mathrm{~s}$. The total time that the CM is transmitting data during a typical cycle is therefore $650 \mu \mathrm{~s}$. Considering the time taken to complete a typical cycle from the rotation of the armature to taking a reading to the rotation of the armature again, is approximately ten to fifteen seconds, depending on the speed of the armature drive motor and the detection unit drive motor, the probability of an error occurring during transmission of data for a typical cycle is:

$$
\frac{650 \mu \mathrm{~s}}{10 \mathrm{~s}} \times 100=0.0065 \% \quad \ldots \ldots \ldots . \quad 4-9
$$

The probability decreases if the typical cycle takes more than 10 s (due to lower speeds of the drive motors).

Further, considering that the worst case delay from the time an Emergency Stop is initiated till the time it the serviced is $130 \mu \mathrm{~s}$ which in real terms is almost negligible and the fact that the initiation of an Emergency Stop is an event that rarely occurs, option two was chosen (the option that involved the disabling and enabling of the serial port interrupt). In summary, efficiency was chosen over a low probability of an occurrence of an event that even if it occurred will cause no ill effect to the system as a whole.

| CH_OUT: | CLR | ES |
| :--- | :--- | :--- |
|  | MOV | SBUF, A |
| TX2: | JNB | TI, TX2 |
|  | CLR | TI |
|  | SETB | ES |
|  | RET |  |

## CODE EXTRACT 4-8: CH_OUT SUBROUTINE

The second statement in this subroutine copies the value held in A into SBUF. Writing to SBUF in this manner begins transmission. In the third statement the TI flag is continuously tested in order to ascertain if the data has been transmitted. Recall that the TI flag is set when all data has been transmitted and SBUF is empty. Once transmission is complete, the TI flag is set High (1) and the test loop is exited. In the fourth statement, the TI flag is cleared and in the fifth statement the serial port interrupt is enabled. The RET statement exits from the subroutine and returns control to the calling program. See Figure 4-7 for the associated flow diagram.


## FIGURE 4-7: CH_OUT FLOW DIAGRAM

### 4.1.5.2 The Error 1 Subroutine

Error 1 occurs when a pair of bars is not detected within a predefined time. The AM alerts the CM to this error by triggering External Interrupt 0 as described earlier. The Error 1 subroutine is then called from the External Interrupt 0 ISR. If this error is to occur, it will do so before a volt-drop reading is taken. The error subroutine must therefore cater for a manual reading that is to be taken by the test technician. The execution of this process is described in the discussion that follows with reference to Code Extract 4-9 and Figure 4-8.



FIGURE 4-8: ERROR 1 FLOW DIAGRAM


```
; ERROR l SUB
;*****************************
ERl_SUB:MOV A,#"J"
    CALI CH_OUT
E1E2: NOP
MAN RDG:CJNE A,#'D'`,ElE2
    SETB PO.3
TK RDG: JNB F3.G,TK RDG
TK_RDG2:TB P3.G,TK_RDG2
    SETB PO.4
E1_CK1: JNB P2.2,E1_CK1
    JB P2.2,5
    CLR PO.4
E3_RDNG:TNB P2.2.E3_RDNG
    SETB PO.7
    NOF
    NOP
    NOP
    CLR PO.7
    CALL RDG_gUB
    CLR PO.3
    SETB PO.4
E1_侕T: TNB P2.2,E1_而T
    CLR PO.4
    NOP
    NOP
    RET
```

CODE EXTRACT 4-9: ERROR 1 SUBROUTINE

The first step in this subroutine is to alert the GUI to the fact that Error 1 has occurred by transmitting ' J '. The subroutine then enters a wait loop until the test technician acknowledges this error and signals his intention to take a manual reading by clicking on the Take Manual Reading button on the GUI. The GUI then transmits a 'D' to the CM. The CM then enters another wait loop where it waits for the test technician to press a switch connected to P3.6 when he/she has set the test probes in place on the pair of bars that are to be tested. Once this switch is pressed, the CM uses P0.4 to signal to the AM that it is ready to take a manual reading. The AM then checks whether the test current is switched on and if all is well, it will signal to the CM that it too is ready to take a reading by Setting (1) and Clearing (0) the CM P2.2. The AM
then calls its Reading subroutine. Once called this subroutine signals to the CM that it has been called by again setting the CM P2.2 hence allowing it to exit the wait loop. The CM signals that it has received the message sent and that it is about to call its Reading subroutine by Setting (1) P0.7. At this point, the Reading subroutines for both the CM and AM are synchronised with each other. A volt-drop reading is then taken. The CM then signals the AM by Setting (1) P0.4 that the reading has been taken upon completion of its reading subroutine. When the AM receives this signal it responds by setting the CM P2.2 High (1). The Error 1 subroutine returns control to the calling program upon receiving this signal. Note that the CM P0.4 and P2.2 are used for communication with the AM where CM P0.4 transmits signals which are read by the AM P1.4 and CM P2.2 is used to read the status (signals) of the AM P0.0.

### 4.1.5.3 The Error 2 Subroutine

Error 2 occurs when the test probes do not reach the surface of the commutator within the allowable predetermined time. In terms of the CM when this error occurs the procedure that has to be followed is exactly the same as that of Error 1 as a voltdrop reading has not yet been taken. The route followed by the CM is to call the Error 1 subroutine from the point after it has transmitted ' J ' to the GUI, i.e. from label E1E2, as shown in Code Extract 4-10.


## CODE EXTRACT 4-10: ERROR 2 SUBROUTINE

Referring to Code Extract 4-9 the reader will notice that the E1E2 label follows immediately after informing the GUI that Error 1 has occurred by transmitting 'J'. This label is also the beginning point of the E1E2 subroutine. A subroutine within a larger subroutine, such as E1E2 is created by calling a label at any point before the

RET statement. This label is then regarded as the name and starting point for the smaller subroutine with the common RET statement being the end or return of control instruction. With this being the case all that the Error 2 subroutine has to do is alert the GUI that Error 2 has occurred by transmitting 'm' before calling the E1E2 subroutine.

### 4.1.5.4 The Error 3 Subroutine

Error 3 occurs when the allowable time for the Test Current to be switched on is exceeded. This occurs when the period of time measured from the instant that the microcontroller pulses the IGBT driver to switch on the Test Current till the instant that the microcontroller pulses the IGBT driver to switch off the Test Current, is greater than the default time. This is present because of the high test supply current used (350A to 400A). Such a system error may be dangerous to the test technician, nearby personnel and may also cause damage to the armature under test due to overheating. With this in mind, it was decided that the safest option is to immediately end the test on the occurrence of this error. As shown in Code Extract 4-11 the Error 3 subroutine simply informs the GUI that Error 3 has occurred by transmitting "L" (the GUI subsequently initiates an Emergency Stop) before jumping to the CRNT_E label, in the serial port ISR, in order to initiate the Powerdown procedure for both the AM and CM.

```
;*******************************
; ERROR 3 GUB
```



```
ER3_GUB:MOV A,#'L'
    CALL CH_OUT
    JMP CRNT_E ; IN EPISR
    RET
```


## CODE EXTRACT 4-11: ERROR 3 SUBROUTINE

### 4.1.5.5 The Error 4 Subroutine

Error 4 occurs when the test probes are not raised to their initial position within the allowable time. The procedure for this error is not as complex as that for Error 1 and Error 2 because the volt-drop reading would have already been taken before this error
occurs. As shown in Code Extract 4-12 the Error 4 subroutine informs the GUI that Error 4 has occurred by transmitting a ' Q ', and waits for the test technician to attend to the fault. If the fault is not serious the technician will manually raise the test probes to the correct position before clicking on the Continue After Error button on the GUI. The GUI then transmits a ' C ' to the CM . On receiving this prompt. (' C ') the wait loop is exited and the AM is signaled to continue with the test using P0.4 and P2.2 as described earlier.

| ; ERROR 4 SUB |  |
| :---: | :---: |
| ; *************************** |  |
| ER4_SUB:MOV | A, \# ${ }^{+} \mathrm{Q}^{\top}$ |
| CALL | CH OUT |
| E3E4: NOP |  |
| TT_NBC3: CJNE | A, $\#^{+C} \mathrm{C}^{\top}$, E3E4 |
| SETB | P0. 4 |
| E3_TTT: JNB | P2.2,E3_WT |
| CLR | P0. 4 |
| RET |  |



## CODE EXTRACT 4-12: ERROR 4 SUBROUTINE

### 4.1.5.6 The Reading Subroutine

The Reading Subroutine is responsible for communication with the Reading subroutine in the AM, controlling the ADC via the ADC control lines, capturing the recorded data from the ADC and transmitting this data to the GUI.


FIGURE 4-9: SYSTEM BLOCK DIAGRAM



FIGURE 4-10: READING SUBROUTINE FLOW DIAGRAM

```
RDG_SUB:NOP
NO_NEG: JB 04H,NO_COM
WT_RD: JNB P2.2,WT_RD ; WAIT FOR CURRENT - SWITCHED BY U2
    SETB P0.7; TO U2 TO SIGNAL READY TO TAKE READING
    NOP
    NOP
    CLR P0.7
NO_COM: NOP
;EXTRA 1S DELAY IN UC2 (X) 4 INPUT CCTRY
OV_CHK: JNB PO.2,DWN ; for pcb, for tst cet, jb p0.2
    JMP EET_ON
DWN: LJMP OVRVOL
EET_ON: SETB PO.0 ; ANA SW ON
    CLR P2.0
    CLR RSO ;20US
    SETB RS1
    MOV R6,#24
D4: DJNZ R6,D4
    CLR RSO
    CLR RS1 ;20US
;AQU MODE, p3,5 cleared lus after p2.0 ***(CS fALIING eDGE 1)
    CLR P3.5
    CLR RSO ;20US
    SETB RS1
    MOV R6,#20
D5: DJNZ R6,D5
    CLR RSO
    CLR RS1 ;20US
    NOP ;Tcsl and tdh
    SETB P3.5
    CLR RSO ;20US
    SETB RS1
    MOV R6,#24
```

```
D6: DJN2 R6,D6
    CLR RS0
    CLR RS1 ;20US
    CLR P3.5; FOR STANDBY MODE ***(CS fALLING eDGE 2)
```

ADC_W: JB P2.1,ADC_W ;EOC ${ }^{7}$
SETB P3.5
SETB P2.0; TO PUT DATA OUT
CLR P3.3; ;HBEN - LOW BYTE
NOP ; EXTRA TIME BEFORE CS FORCED LOW
CLR P3.5; *** (CS fALLING eDGE 3)
NOP ;WAIT FOR VALID DATA,TdotTdv ( $t d v=0$ )
CLR P3.3; ; HBEN - LOW BYTE redundancy
CLR RSO ;20US
SETB RS1
MOV R6,\#10
D7: DJNZ R6, D7
CLR RSO
CLR RS1 ;20US nop
MOV R3, P1 ;HOLD L BYT
SETB P3.3 ;HBEN - HIGH BYTE
CLR RS0 ;20US
SETB RSI
MOV R6,\#10
D8: DJN2 R6,D8
CLR RSO
CLR RS1 ;20US
MOV R5, P1 ; HOLD H BYT
SETB P3.5;** (CS 1ST RISING EDGE AFTER fALLING eDGE 3)
NA CK: CJNE R5,\#11111111B, OUT RNG ; CHECK IF NOT ALLOWED CODE
CJNE R3,\#11111110B, OUT_RNG
MOV R5,\#11111111B
MOV R3,\#11111111B
OUT_RNG:MOV A, \#'z'
CALL CH_OUT

```
OUT H: MOV A, R5
    CALL CH_OUT
    MOV A,#'Y'
    CALI CH_OUT
OUT_L: MOV A, R3
    CALL CH_OUT
```



```
    SETB 05H
    JMP RDG_SUB
MT_100C:CJNE A,年'S ',WT_NBCT
    CLR 05H
RDG_END:JB 04H,NO_COM2
    JB 05H,NO_COM2
    SETB P0.7; TO U2 TO CONT AFTER READING TAKEN
RG_END: JNB P2.2,RG_END
    CLR P0.7
    CLR PO.0 ;ANA SW OFF
    JMP NO_COM2
OVRVOL: MOV A,#'z'
    CALL CH_OUT
    MOV A,#11111111B
    CALL CH_OUT
    MOV A,#'Y'
    CALL CH_OUT
    MOV A,#11111110B
    CALL CH_OUT
```



```
    SETB 05H
    JMP RDG_SUB
WT_100E:CJNE A, #' S', %MT_NBC
    CLR 05H
RDG_EDS:JB 04H,NO_COM2
    JB 05H,NO_COM2
    SETB P0.7; TO U2 TO CONT AETER READING TAKEN
RG_EDS: JNB P2.2,RG_EDS
    CLR P0.7
    CLR PO.0 ;ANA SW OFF
NO COM2: RET
```

CODE EXTRACT 4-13: READING SUBROUTINE

The operation of this subroutine is discussed with reference to Figure 4-10 and Code Extract 4-13. Once called the first operation undertaken by this subroutine is to verify if flag 04 H has been set. Flag 04 H is set when the system is to be operated in Manual mode. When running in Manual mode the AM is in Powerdown and will therefore not respond to any communication signals from the CM. When operating in the Automated mode there is constant communication between the AM and the CM in order to maintain synchronisation.

When being operated in the Manual mode this communication is fruitless as the CM will be waiting for signals from the AM that will never be transmitted. The CM will therefore be caught in an endless waiting loop. The reason that 04 H flag is tested is to ensure that the CM knows if it should communicate with the AM (as when it is in Automated mode) or if all its communication instructions should be skipped, when it is operating in Manual mode as discussed earlier in this chapter. Flag 05H is used to indicate that 100 successive readings are to be taken. This is an additional feature and will therefore be discussed in detail in Chapter 6.

If the system is in Automated mode, P2.2 is tested in order to verify that the AM has called and is presently executing its Reading subroutine and to ensure that it is ready to take a reading. The CM then confirms having received this signal by setting its P0.7 pin. As mentioned above, these steps are skipped when in Manual mode. Next, P0.2 is tested in order to verify that the reading about to be taken is within the maximum input range of the ADC and other interfacing circuitry. The exact mechanics behind this process will be discussed in detail in Chapter 5 under the section dealing with the interfacing analogue circuitry (Section 5.3). However, in order to facilitate a better understanding, the author will briefly discuss the principle and concept used.

Although the test is setup by the technician to record values within a particular range, 200 mV to 350 mV , the possibility exists that a volt-drop equal to the potential of the Test Supply can be recorded across a pair of bars. This will occur when the pair of bars being tested is connected to an open circuited winding. According to tests carried out by the author, the typical Test Supply potential when setting the aforementioned range, is between ten and fifteen volts ( 10 V to 15 V ) depending on the type and rating
of the armature under test. As will be explained in chapter five the first stage in the input circuitry is more than capable of handling these values as well as negative input potentials, as in the case when the polarity of the Test Supply Current, or the orientation of the input test probes is reversed. The ADC input stage however, cannot handle such potentials. The ADC absolute maximum rating for the input pin is positive 6 volts to negative $0.3 \mathrm{~V}(+6 \mathrm{~V}$ to $-0.3 \mathrm{~V})$. It is for this reason that an Analogue Switch (MAX 4622) is placed on the ADC input line. This switch is only switched on by the CM when the interfacing analogue circuitry confirms that the potential on the ADC input line is safely within its operating range. This circuitry is explained in Chapter 5, Section 5.3.

If the CM P0.2 is High (1), the Analogue Switch is off due to the input value being out-of-range. In this case 11111111 (binary code) is transmitted as the High Byte and 11111110 (binary code) is transmitted as the Low Byte to the GUI as the reading for the pair presently under test. Upon receiving this value the GUI immediately recognises the out-of-range reading and displays a possible open circuit on this pair of bars. After this transmission the CM sits in a wait loop, waiting for the GUI to transmit the Continue Test prompt, i.e. 'E'. Note that in order to facilitate the 100 reading additional feature, a second prompt is used to verify that all 100 readings have been captured. This prompt is the ASCII code for the character 'S'. More details on this additional feature will be provided in Chapter 6.

If P0.2 is low, the Analogue Switch is switched on and the ADC can read the input potential. The ADC control pins are then prompted and read by the CM in order to capture a reading. The High Byte is stored in the CM register 5, R5 and the Low Byte is stored in the CM register 3, R3. See Appendix K for a list of the registers used for both the AM and CM.

The next step is to check if R5 holds 11111111 and R3 holds 1111 1110. This is the previously mentioned out-of-range default value. If the default value has been recorded, the value held in R3 is changed to 1111 1111. This new value and the out-of-range default value should normally not be recorded on a non-fault bar. As discussed in Chapter 3, the ASCII code for the letter ' $z$ ' is transmitted to the GUI before the High Byte (the value held in R5) of the captured reading is transmitted to
the GUI. The ASCII code for the letter ' y ' is transmitted to the GUI before the Low Byte (the value held in R3) of the captured reading is transmitted to the GUI. The CM then waits for the GUI to process the transmitted data and inform the CM that it is ready to continue by transmitting an ' E ' (the Continue Test prompt).

On receiving this prompt the CM again tests if flag 04H is set High (1). If it is not set High, then using P0.7 and P2.2 as described above, the CM communicates with the AM to inform it that the reading has been successfully captured, transmitted and analysed and that it should ready itself to proceed with the next task in the process. If the flag 04 H is set, then this communication process is skipped as mentioned earlier. The CM then switches off the analogue switch on the ADC input line in order to protect the ADC in the event of an out-of-range input value on the next pair of bars. The subroutine is then exited and control is returned to the calling program at the statement immediately following the CALL instruction.

### 4.1.6 ADC Control

The ADC control pins and the associated connection pins on the CM are listed below. The $\overline{C S}$, Convert Start ADC input pin, is connected to the CM P3.5 pin which is configured as an output pin. The $\mathrm{R} / \bar{C}$, Read $/ \overline{\text { Convert }}$ ADC input pin is connected to the CM P2.0 pin which is configured as an output pin. The $\overline{E O C}$, End Of Conversion ADC output pin, is connected to the CM P2.1 pin which is configured as an input pin.

And finally, the HBEN, High-Byte Enable ADC input pin is connected to the CM P3.3 pin which is configured as an output pin. Figure 4-11 depicts the flow diagram that describes the process that is followed when the ADC captures a reading. Figure $4-12 \mathrm{~A}$ depicts the flow diagram that shows the steps taken by the CM to implement the process followed in Figure 4-11. Figure 4-12B depicts the timing diagram for the ADC control process. See Appendix J to view the ADC (MAX 1166) datasheet.



FIGURE 4-11: FLOW DIAGRAM FOR THE ADC CONTROL PROCESS



FIGURE 4-12A: FLOW DIAGRAM OF STEPS TAKEN BY THE CM TO IMPLEMENT THE ADC CONTROL PROCESS


FIGURE 4-12B: TIMING DIAGRAM FOR ADC CONTROL PROCESS

The control process is as follows: to start up the ADC and enable acquisition mode, the R/ $\bar{C}$ pin must be held low during the $\overline{C S}$ falling edge. This is the $\overline{C S}$ first falling edge. The above is accomplished by the CM by Clearing (0) P2.0 and after a short delay, also Clearing (0) P3.5. Both P2.0 and P3.5 would have been set at the end of the previous reading or acquisition cycle or in the case of the first reading to be taken, these ports would have been set by the 'dummy' conversion cycle as mentioned earlier. Next, to start a conversion and choose the ADC 'Standby Mode' option, $\mathrm{R} / \bar{C}$ must remain Low (0) during the $\overline{C S}$ second falling edge. (The second $\overline{C S}$ falling edge will start the conversion process and the logic level of $\mathrm{R} / \bar{C}$ during this falling edge will determine the mode of operation).

To accomplish this, after a delay that is greater than the stipulated $t_{\mathrm{CS}}$ (i.e. the minimum time that the $\overline{C S}$ pin should be held Low (0) before setting it High (1)) the $\overline{C S}$ pin is set High (1). Then after a delay that is greater than $\mathrm{t}_{\mathrm{CHS}}$ (i.e. the minimum time that the $\overline{C S}$ pin should be held High (1) before setting it Low (0)) the $\overline{C S}$ pin is set Low (0) to produce the second falling edge. Note that the time between the first and second falling edge, $\mathrm{t}_{\mathrm{ACQ}}$, is the acquisition time and cannot be less than the stipulated $4.7 \mu \mathrm{~s}$. Hence the sum of $\mathrm{t}_{\mathrm{CSL}}$ and $\mathrm{t}_{\mathrm{CHS}}$ must be greater than or equal to $\mathrm{t}_{\mathrm{ACQ}}$, as shown in Figure 2, Page 8 of the MAX 1166 datasheet.

Note that for Standby Mode the $\mathrm{R} / \bar{C}$ pin is held low during the second $\overline{C S}$ falling edge. In this mode the reference and buffer remain powered up after a conversion cycle. For Shutdown Mode the $\mathrm{R} / \bar{C}$ pin is held high during the second $\overline{C S}$ falling edge. In this mode the reference and buffer are powered down after a conversion cycle. The advantage of Standby Mode over Shutdown Mode is that in the case of the Standby Mode there is no need to wait for the internal reference to wake up and settle and to run a 'dummy' conversion before a new acquisition and conversion cycle takes place. The ADC can simply exit Standby Mode and begin an acquisition and conversion cycle

After the $\overline{C S}$ second falling edge the CM waits to the $\overline{E O C}$ pin to drive Low (0). This signals the end of a conversion and occurs on the expiration of the conversion time,
$\mathrm{t}_{\text {CONV }}$, following the $\overline{C S}$ second falling. When P2.1 is driven Low (0) the wait loop is exited and the Low-Byte can be put on the ADC eight-bit output bus. In order to read the Low-Byte certain conditions must first be satisfied. These are that the $\mathrm{R} / \bar{C}$ pin must be held High on the $\overline{C S}$ third falling edge and the HBEN pin must be held Low. This is done as follows: after a delay of $\mathrm{t}_{\mathrm{Dv}}{ }^{2}$ (i.e. the minimum time that has to elapse after $\overline{E O C}$ is driven Low (0) and before the $\overline{C S}$ third falling edge), the $\overline{C S}$ pin can be driven Low (0) to produce the third falling edge. But this pin is not driven Low until it is first driven High (to recover from the last falling edge transition) and P2.0 is driven High.

After the third falling edge, a delay that is greater than $\mathrm{t}_{\mathrm{DO}}$ is enforced to allow for valid data to be put on the eight-bit output bus. Then by setting HDEN High (1) and waiting for a period grater than $\mathrm{t}_{\mathrm{DO}}$ (i.e. the time that is required for valid data to be put on the eight-bit output bus after toggling HBEN), the High-Byte is put on the eight-bit output bus. After the CM has recorded and stored the high and low bytes of data that was output by the ADC, P3.5 is set High (1) hence driving the $\overline{C S}$ pin High (1). The process of driving the $\overline{C S}$ pin high after the $\overline{C S}$ third falling edge forces the ADC eight-bit output bus into a high impedance state and readies the device for the next acquisition and conversion on the next $\overline{C S}$ falling edge.

The $\overline{E O C}$ pin is also forced High (after a time delay determined by $\mathrm{t}_{\mathrm{EOC}}$ ) on this $\overline{C S}$ raising edge. Note that the next acquisition should be initiated after a delay period greater than $t_{B R}$ (i.e. Bus Relinquish Time) as stipulated for best results by the manufacturer. This delay period is more than compensated for by the execution time for the CM instructions that follow before the next acquisition and conversion process is initiated.

[^5]
### 4.2 Automation Microcontroller

The Automation Microcontroller (AM) controls the Physical Test Station based on input signals received from the Physical Test Station itself, as well as commands and prompts received from the CM and the GUI via the CM .


FIGURE 4-13: SYSTEM BLOCK DIAGRAM

This section will describe the tasks undertaken by the AM and the manner in which these tasks are executed. As the previous section, The Communications Microcontroller, provided detailed explanations on all the relevant microcontroller functionalities, such as Timers, Interrupts, Subroutines etc, this section will concentrate solely on discussing the AM's use of these functionalities to efficiently complete specific tasks. In order to provide an overview of the AM's process flow, a diagrammatic depiction is presented in the form of a flow diagram in Figure 4-15.

### 4.2.1 Explanation of functions, tasks and flow process

The program for the AM was developed using three control levels based on interrupts and interrupt priorities. The first level is the base level, where the Main program has control. Here the required initialisations are carried out as well as the control and timing of the Armature Drive Motor and the calling of Error 1 subroutine, should Error 1 occur. When a pair of bars is detected, External Interrupt 1 is triggered and the External Interrupt 1 Interrupt service routine assumes control thereby entering the second control level. The EX1 ISR is responsible for stopping the Armature Drive

Motor, the lowering and raising of the Detection Unit, switching of the Test Current, communication with the CM in order to capture the volt-drop readings and calling of error subroutines should the associated errors occur. The third level is the domain of the External Interrupt 0 (EX0) ISR. EX0 is assigned a higher priority than EX1 and can therefore interrupt the EX1 ISR as in the case when the test probes have reached the surface of the detected bars. In fact this is the function of EX0, i.e. to ascertain the status of the Detection Unit. When the test probes reach the surface of the bars EX0 is triggered, the Detection Unit Drive Motor is stopped, and the time period taken for the probes to be lowered to the surface of the bars is recorded in the EX0 ISR. EX0 is also triggered when the test probes have been raised to their initial position.

In summary, the base level allows for initialisations and also prompts the Armature Drive Motor to begin the rotation of the armature under test. When a pair of bars is detected EX1 is triggered and EX1s ISR is initiated as the second control level and assumes control from the base level. In the EX1 ISR, the Armature Drive Motor is stopped, the Detection Unit Drive Motor is prompted to lower the Detection Unit and the Test Current is switched on. The time taken for the test probes to reach the bars allows the test current to settle. Once the test probes on the Detection Unit reach the surface of the bars EX0 is triggered, the EX1 ISR is interrupted and the EX0 ISR executes, initiating control level three and assuming control from the EX1 ISR. When the EX0 ISR has stopped the Detection Unit Drive Motor and completed recording the relevant times, the ISR is exited and control is handed back to the EX1 ISR hence control level two.

The EX1 ISR then proceeds to communicate with the CM and a volt-drop reading is taken after which the Detection Unit Drive Motor is prompted to raise the Detection Unit. When the Detection Unit Drive Motor reaches its initial position EX0 is again triggered thereby initiating control level three and assuming control from the EX1 ISR and control level two. The EX0 ISR stops the Detection Unit Drive Motor and exits handing control back to EX1 ISR and control level two. EX1 ISR is then also exited and control is handed to the base control level and the Main program. Based on the commands from the GUI via the CM, the cycle is repeated until the last bar is tested. See Figure 4-14 for a diagrammatic representation of the above discussion. A more
detailed explanation of the Automation Microcontrollers process flow follows after Figure 4-15.


FIGURE 4-14: DIAGRAMMATIC REPRESENTATION OF THE THREE LEVEL CONTROL SYSTEM


A (pp. 151) B (pp. 151)

$\mathrm{C}(\mathrm{pp} .152) \quad \mathrm{D}(\mathrm{pp} .152)$


FIGURE 4-15: FLOW DIAGRAM FOR THE AUTOMATION MICROCONTROLLER

The AM first executes an initialisation process in which all the timers, interrupts and input/output ports that will be utilised for the duration of a test are initialised. Thereafter, the AM waits for the start pulse from the CM on P1.0. Upon receiving this pulse, the AM tests P1.6 to ascertain whether the test will be run in the Automated or Manual mode. If P1.6 is High (1) then the Manual mode has been selected and the AM initiates Powerdown mode. If P1.6 is Low (0) then Automated mode has been selected and the AM then Sets (1) and Clears (0) P0.1, which is responsible for signaling 'Increment The Number Of Bars'.

The AM then waits for the GUI to inform it, via the CM, whether or not the last pair of bars has been tested. If P3.0 is Low (0), then the last pair of bars have been tested and the AM waits for the End command from the GUI via the CM. Once this is
received, the AM enters Powerdown mode. If P3.0 is High (1), then the last pair has not been tested and the command is given to the Armature Drive Motor to initiate the rotation of the armature under test by setting P0.4 High (1). The AM then waits for the next pair of bars to be detected while timing the period between the initiation command and when the pair of bars has been detected. Detection of a pair of bars triggers External Interrupt 1 (EX1). If EX1 is not triggered before a maximum allowable time for detection is exceeded, Error 1 has occurred and the associated subroutine is called. Recall that Error 1 occurs when a pair of bars has not been detected within the maximum allowable time. The maximum allowable time for detection for each of the first three pairs is a preset value of 10 seconds.

The time duration recorded on the third pair of bars is stored to be used to calculate a tolerance or the maximum allowable time for the detection of a pair of bars after initiating the rotation of the armature under test. This new maximum allowable time will be the Detection Reference Time for the duration of the test. The time recorded on the third pair plus twenty percent is used as the reference value, i.e.

## Detection Reference Time $=$ Third Pair Time Recording x 1.2

From the fourth pair of bars onwards, if EX1 is not triggered before the Detection Reference Time has expired, Error 1 subroutine is called. The use of the Detection Reference Time allows for greater control of the system as the unique reference value that is used for the duration of the test is based on the bar widths and spaces between the bars of the particular armature under test. In this way an error is detected sooner than if a preset value that catered for all armatures was used, hence the possibility of excessive damage to the system and the armature under test due to a system error is reduced. The reason that the Detection Reference Time is calculated based on the time recorded for the third pair of bars is simply because the system is given time to settle during the first and second cycles.

The question that now arises is what happens if a detection error occurs on the third pair of bars, i.e. when the time is being recorded to calculate the Detection Reference Time? The answer is that if Error 1 was called before External Interrupt 1 was triggered, then a time period will not be recoded as all time recordings is done by the

External Interrupt 1 interrupt service routine (ISR). The Error 1 subroutine does not have the capability to perform any time interval recording. Hence the value that will be used to calculate the Detection Reference Time will now be recorded on the next detection cycle, i.e. on the forth pair of bars. However, to introduce redundancy, the Error 1 subroutine also takes appropriate measures when this event occurs. Note that the use of timers to record time, set preset intervals and introduce delays is discussed in Section 4.1.4.

When a pair of bars has been detected before the Detection Reference Time has exceeded, hence triggering EX1, the rotation of the armature under test is immediately stopped by Clearing (0) P0.4. The rest of the process from this point onwards is executed in the External Interrupt 1 ISR. From this ISR, the signal to the Detection Unit Drive Motor to begin lowering the Detection Unit is given. The Test Current is also switched on by Setting (1) P2.7. The Test Current is switched on before the Test Probes on the Detection Unit reach the bars as opposed to when they are already on the bars. This is done to prevent large voltage spikes due to the switching of the large test current to the inductive load (i.e. the inductance ( L ) of the armature under test), from damaging the input circuitry.

The Test Probes must not be confused with the Test Current Probes. The Test Current Probes are the probes from which the Test Current is injected though the armature under test via an IGBT. The Test Current Probes are lowered onto the commutator and are fixed into place at the start of the test and are in no way attached to the Detection Unit. These probes are not raised off or lowered onto the commutator as in the case of the Test Probes on the Detection unit. The Test Current is switched on when a reading is to be taken and is switched off when a reading is complete and the Test Probes have been raised off the surface of the commutator.

The Test Current probes are never raised off the surface of the commutator at any time during the test. When the IGBT is switched off, the collapsing magnetic energy that is stored in the armature is dissipated via an onboard fly-back diode. Fly-back diodes are a standard feature on most modern IGBT units and are built into the semiconductor structure of the IGBT to provide onboard protection in a single unit. The Test Current is switched on between 2 and 4 seconds after it was last switched off
depending on the speed of rotation and the spacing of the commutator bars. The low switching frequency allows for sufficient time for the stored magnetic energy to be dissipated via the onboard fly-back diode hence there is no arcing.

The spring mounted Test Probes are fixed onto the Detection Unit. These probes are lowered and raised when a reading is to be taken. A minute current flows through these test probes due to the extremely high input impedance of the Data Acquisition Module, more specifically the input impedance of the precision Instrumentation Amplifier, the INA 118, as discussed in Section 5.3. It is due to this high input impedance and the low Test Supply Voltage of typically +15VDC maximum that arcing does not occur when the test probes are raised off and lowered onto the commutator when the Test Current is flowing through the armature. Tests on the Data Acquisition Module proved that no arcing takes place when the test probes are raised off and lowered onto the commutator while a Test Current was allowed to flow through the armature.

The only undesirable electrical effect that would have to be catered for is the bouncing of the input signal due to the mechanical bounce created when spring loaded test probes make contact with the surface of the bars. This bounce will create oscillations in the input signal however, the amplitude of these oscillations should not exceed the amplitude of the input signal when it has settled. This means that although there will be oscillations due to the bounce, there will be no voltage spikes as created when switching the Inductive load. In order to cater for the above-mentioned oscillations, the ADC is instructed to perform acquisition and conversion only after a delay period has been enforced.

If the test probes on the detection unit do not reach the surface of the bars within a preset time then Error 2 occurs and the associated subroutine is called. When the test probes do reach the surface of the bars within the allocated time, the Detection Unit outputs a signal which triggers External Interrupt 0 (EX0). As mentioned previously, EX0 is assigned a higher priority than EX1. Error 2 will be initiated when the preset allowable time of ten seconds, for reaching the surface of the bars, expires before EX0 is triggered. If EX0 is triggered before the aforementioned time expires, the EX0 ISR is initiated. The EX0 ISR stops the Detection Unit Drive Motor and stores the time
that was taken for the test probes to reach the surface of the bars by copying the values held in the timer registers. Once on the surface of the bars, the AM signals the CM that a volt-drop reading can now be taken be Setting (1), P0.0. The AM then waits for one of two signals from the CM. The first is the signal received on P1.7, which informs the AM that the reading has successfully been taken by the CM, transmitted to the GUI, analysed and stored. Now both the GUI and the CM are ready to proceed.

The second signal is received on P3.1, which informs the AM that the maximum allowable time that the Test Current can be switched on for an individual volt-drop reading has been exceeded. The timing of the Test Current on-time is carried out by external interfacing circuitry and is discussed in Section 5.1.6. If P3.1 is Set (1) before P1.7, Error 3 has occurred. The Error 3 subroutine is then called and due to the severity of the effects of such high currents being applied to the armature under test for a prolonged period of time, an Emergency Stop is automatically initiated and the AM immediately halts the task that was being carried out, switches off the Test Current by Clearing (0) P2.7 and safely shuts the system down before entering Powerdown mode. If however, P1.7 is Set (1) before P3.1 then the volt-drop reading will be captured with no system irregularities and the process flow continues as normal.

The next step is to prompt the Detection Unit Drive Motor to begin raising the test probes off the surface of the bars. Here again EX0 is triggered when the Detection Unit reaches its initial position. If, however, EX0 is not triggered before the maximum allowable time has elapsed Error 4 occurs and the associated subroutine is called. This maximum allowable predetermined time for this process is called the Unit Raising Reference Time. This period is derived by adding twenty percent of the time taken for test probes to reach the surface of the bars (during lowering) to the recorded time itself, i.e.

Unit Raising Reference Time $=$ Recorded Test Probe Lowering Time x 1.2
When EX0 is triggered before the Unit Raising Reference Time expires, the Detection Unit Drive Motor is stopped and control is returned to the EX1 ISR, which in turn returns control to the Main program. The Main program then transmits an Increment
signal to the GUI via the CM and waits for the response. This cycle continues until each pair of bars on the commutator of the armature under test has been tested.

### 4.2.2 Initialisation and main program

The Main program is responsible for performing all the required initialisations on startup. This includes the initialisations of the input/output ports, timers, interrupts and interrupt priorities. The above-mentioned initialisations can be viewed in Code Extract 4-14.

|  | ORG | 0H |
| :---: | :---: | :---: |
|  | LJMP | MAIN |
|  | ORG | 0003H |
|  | L.JMP | EXOISR |
|  | ORG | 0013H |
|  | LJMP | EXIISR |
| Count | EQU | -10000 ; DELAY LOOP |
| COUNT2 | EQU | -50000 ; SAFty tIme |
| MAIN: | ORG | 0030 ${ }^{\text {H }}$ |
|  | MOV | TMOD, \#00010001B |
|  | MOV | IF, \#00000001B |
|  | MOV | IE, \#00000101B |
| ; *******iNTILIZE I/O PORTS ******** |  |  |
|  | MOV | PO, \#0H |
|  | MOV | P1, \#111111118 |
|  | MOV | F2, \#0H |
|  | MOV | P3, \#00011111B |
| *******iNTILIZE I/O PORTS *** |  |  |

## CODE EXTRACT 4-14: AUTOMATION MICROCONTROLLER INITIALISATION

The first six statements redirect the program counter (PC) to different locations in program memory (ROM), via labels, when vectoring off to the defined addresses (i.e. in this case $0 \mathrm{H}, 0003 \mathrm{H}$, and 0013 H ). The starting location or address for a program is 0 H , this is the system reset vector address. Once at this location, a Long Jump (LJMP) to the label Main is initiated. This label is the starting point of the Main program. Similarly, when interrupts are triggered, the PC is loaded with the default vectoring address of the associated ISR. Once at that address, the program is redirected to
locations in memory where the associated ISR resides using LJMP statements. This is because the eight-byte provision made for ISR's is too small to cater for the ISR's needs. The main program memory space is available from 0030 H , as the space from 0000 H to 002 FH is allocated to system reset and ISR code. The statement below,

```
MOV TMOD,#00010001B
```

initiate the timers using the TMOD SRF. Both Timer0 and Timer1 are initialised as sixteen-bit timers. Interrupt priority is assigned using,
MOV IP, \#00000001B
where, as discussed earlier, External Interrupt 0 is assigned a higher priority than External Interrupt 1. The statement,
MOV IE, \#00000101E
is used to initialise the required interrupts which are, External Interrupt 0 and External Interrupt 1. Following these statements, the input/output ports are initialised by setting the port pins that are to be used as inputs High (1) and setting the port pins that are to be used as outputs Low (0). The EQU directive is used to assign a numeric value to the associated symbol. This symbol is then substituted whenever this value is to be used. For example, the statements below make use of COUNT2 symbol to access its associated numeric value which, referring to Code Extract 4-14, is 50000 . The negative sign implies 50000 less than the timer overflow value of 0 H .

$$
\begin{array}{ll}
\text { MOV } & \text { R1, \#HIGH COUNT2 } \\
\text { MOV } & \text { R2, \#LOW COUNT2 }
\end{array}
$$

Here the high byte of -50 000 is loaded into register R1 and the low byte is loaded into register R2. The timer high and low byte registers are loaded in the same manner. See Appendix L for the AM source code. Following the initialisation steps, the Main program clears all flag bits (located in general purpose RAM) that are to be used in the program. This is done as a precaution. See Appendix K for a list of flags used. Following this step, the AM initiates and waits for communication signals from the CM. It then waits in a loop for the start signal from the CM. On receiving this signal it ascertains the mode of operation. Thereafter, the AM Clears (0) P0.5, in order to clear the D Flip-Flops that provide the interrupt trigger signal when a pair of bars have been detected. This is also a precautionary measure taken to ensure that the flip-flops are in
a known state. The AM then enables the interrupts, transmits the increment signal (on P0.1) to CM and after an enforced delay created by calling the DELAYLOOP subroutine, it waits for a Continue pulse/signal (when the last pair of bars have not been tested) or an End signal (when the last pair of bars have been tested) on port pins P3.0 and P1.1 respectively. The DELAYLOOP subroutine is used often in the program to enforce a one second delay and will be discussed in length under Subroutines.

If a Continue pulse was received the AM then determines if the pair of bars to be tested is pair one, two or three or if it is pair four or above using flags $00 \mathrm{H}, 01 \mathrm{H}$ and 02 H . This is done for the following reason. As the reader may recall, a Detection Reference Time is calculated using the values stored in the timer registers when the third pair was being tested. The Detection Reference Time is then used as a tolerance for the detection period for the fourth pair of bars onward. Hence if the AM 'knows' that pair four or greater is being tested, the Detection Reference Time is used as a reference instead of the preset maximum allowable time of ten seconds that is used for bars one, two and three.

After this point, the AM waits for either the maximum allowable time (using the appropriate value) to expire or External Interrupt 1 to be triggered when a pair of bars has been detected. The Main program does this by checking if the EX1 flag, 04H, has been set. This flag is set at the start of the EX1 ISR and serves to flag or signal the ISR execution event. Once the Armature Drive Motor has been prompted to start, the timers whose registers have been loaded with the appropriate values, are also started/triggered. Once the preloaded time has expired, the status of flag 04 H is checked, as shown in Code Extract 4-15. The reason ${ }^{3}$ that this flag is always tested at this point is that the preloaded time either expires due to an error or it is forced to expire by reloading the timer and R3 registers with values that are slightly less than the allowable time hence causing this allowable time to expire almost immediately after the EX1 ISR is exited.

[^6]When EX1 is triggered the timers are paused, the ISR handles the interrupt and control is returned to the timers which will resume their count from the new "forcing" reloaded value until the maximum allowable value has been reached. So upon completion of this count, the Main program has to check if EX1 had been triggered and if the ISR had been initiated by testing flag 04H. If EX1 ISR had indeed been initiated (flag 04 H is High (1)) then no error would have occurred. However if flag 04 H was Low (0) at this point, then the EX1 ISR had not been initiated before the maximum allowable time was exceeded and an error is reflected.


## CODE EXTRACT 4-15: EXTERNAL INTERRUPT 1 FLAG 04 H TEST

Note that prior to exiting the EX1 ISR, the timers are reloaded with values that force the them to overflow almost immediately, hence eliminating the need to wait for the timer to count for the remainder of the preloaded duration, as shown in Code Extract 4-16.

EXR1OUT: | MOV | TH1,\#-10 |
| ---: | :--- |
| MOV | TL1,\#-10 |
| MOV | R3,\#1 |
| GETB | TR1 | TR

## CODE EXTRACT 4-16: TIMER REGISTER RELOADED "FORCING" VALUES

If the predefined duration is exceeded before EX1 is triggered then Error I subroutine is called and upon regaining control from the subroutine the Main program loops back to the block of code below,

| NLBAR: | TNB | B3. $\mathrm{O}_{\text {, LBAR }}$ |
| :---: | :---: | :---: |
|  | JMP | CONT |
| LBAR: | JNB | El. 1, NLBAR |
|  | CLR | PO. 1 |
|  | L.JMP | END |

CODE EXTRACT 4-17: START / RESTART LOOP
where it waits for a Continue or End signal from the CM. The Error 1 subroutine will be discussed in detail under the section entitled Subroutines. If the triggering of EX1 is first to occur then the program vectors to the EX1 ISR where the interrupt is handled and after completion of this process, the timers are reloaded and control is handed back to the Main program. From this point a jump is initiated and the Main program enters a wait loop where it waits for a Continue or End signal from the CM, as shown in Code Extract 4-17.

This entire process is repeated until the last pair bars have been tested and is identified as having been completed by the reception of an End signal from the CM.

### 4.2.3 Interrupts and Interrupt Service Routines (ISRs)

External Interrupt 1 and External Interrupt 0 are the only interrupts enabled for use by the AM. The interrupt priority is assigned such that External Interrupt 0 has a higher priority than External Interrupt 1 and can therefore interrupt the External Interrupt 1 Interrupt Service Routine (ISR) when the associated triggering event occurs. External Interrupt 1 is triggered on the detection of a pair of bars by the optical sensor. The EX1 ISR then takes control for the duration of that test cycle except for when External Interrupt 0 is triggered and EX0 ISR briefly assumes control. External Interrupt 0 is triggered when the test probes reach the bars under test, when the test probes are raised to their initial position, when an Emergency Stop is initiated by pressing the Emergency Stop switch (on P1.5) on the Test Station or if one of the systems Safety Interlocks are triggered. Safety Interlocks are switches on access points to the test area, e.g. gates or doors. When a gate or door is opened during a test, the Safety Interlock is triggered. This is a safety measure implemented to prevent unauthorised staff from entering the test area while a test is in progress. Each interrupt and the associated interrupt service routine will be discussed individually below.

### 4.2.3.1 External Interrupt 1 and External Interrupt 1 ISR

External Interrupt 1 is triggered when the optical sensors on the detection unit detects a pair of bars and signals this event via a D flip-flop and an interfacing digital network. On triggering this interrupt, the program is immediately paused and the program vectors off to the location in memory that is allocated to the EX1 ISR $(0013 H)$. Due to its size, eight bytes is too little space to contain the entire ISR. The ISR has to therefore be located elsewhere in memory and identified by a label. Once at the vectored address, i.e. 0013 H , a long jump is initiated to the ISR using the label EX1ISR to identify the ISR's location in memory. The label is the beginning point of the ISR and once identified, the ISR executes and returns control to the interrupted program i.e. the Main program in this case using the Return Form Interrupt (RETI) statement. Figure 4-16 depicts the flow diagram for the EX1 ISR and Code Extract 418 shows the EX1 ISR coding.



FIGURE 4-16: EXTERNAL INTERRUPT 1 ISR FLOW DIAGRAM

```
;********************************
; EXTERNAL INTERUPT 1 - ISR - v2
;********************************
EXIISR: CLR PO.4
    SETB PO.5
    nop
    nop
    nop
    nop
    CLR PO.5
    CALL DELAYLOOP
    CLR TR1
    CLR TRO
    SETB [4H
    JNB [2HrRUN_DWN
    JB O.5HrRUN_DTWN
    MOV R4.THD
    MOV R5,TLD
    MOV B,R3
    MOV RGrB
    SETB 0.5H
```



```
; DOWNN
```



```
RUN DWN:CALL RUN DWNX
;****************************
    CALL READING
;****************************
EXR1OUT:MOV TH1, #-10
    MOV TL1&#-10
    MOV R3&#1
    SETB TRI
    RETI
```

CODE EXTRACT 4-18: EXTERNAL INTERRUPT 1 ISR CODING.

On entering the ISR, the first task carried out is to stop the rotation of the Armature Drive Motor by Clearing (0) P0.4 and also stopping the Timers by Clearing (0) TR1 and TR0. The next task is to Clear (0) the D flip-flops that produce the triggering pulse. This is accomplished by setting port pin P0.5 High (1) for a short period before clearing it again. This is done to ensure that the D flip-flops are in a known state for the next detection cycle. The operation of the input detection circuitry will be discussed in Chapter 5. Next, the EX1 flag, 04H, is set. This indicates to the Main program that External Interrupt 1 was triggered and that EX1 ISR did execute.

Following this, the ISR checks whether the pair of bars that were detected are the third pair. If it is the third pair, then the values that are stored in the timer registers are copied into registers R4 (high byte) and R5 (low byte). Further, the value stored in register R3 (Timer 1 overflow count) is copied into register R6 in Register Bank 0, see Appendix K. These values are used in the calculation of the Detection Reference Time. (Note that the use of Timers will be discussed later in the chapter under the section entitled Timers).

The Detection Unit Drive Motor is prompted to begin lowering the unit and the test probes onto the surface of the commutator by calling the RUN_DWNX subroutine. Once the test probes are on the surface of the bars the READING subroutine is called. This subroutine communicates with the CM READING subroutine in order to capture a volt-drop reading for that pair of bars. When the process reading is complete the RUN_UP subroutine is called to raise the bars to its initial position. Note that all subroutines will be discussed in the section entitled Subroutines.

Finally, prior to exiting the ISR and returning control to the Main program, the timer registers and the Timer 1 overflow count register, R 3 , is reloaded with values that will force an almost immediate timer overflow thereby forcing the maximum allowable time to be exceeded, as discussed earlier. Control is then returned to the Main program.

### 4.2.3.2 External Interrupt 0 and External Interrupt 0 ISR

External Interrupt 0 is triggered when the test probes on the Detection Unit has reached the bars under test (when the unit is being lowered), the test probes have been raised to their initial position (when the unit is being raised), when an Emergency stop has been initiated (by pressing the Emergency Stop switch on the Test Station) or if one of the systems Safety Interlocks are triggered. When triggered the program vectors off to 0003 H where it is redirected using a jump statement to the location in memory where the label EXOISR resides. The location of this label is the beginning point of the EX0 ISR code. An explanation of the EX0 ISR is provided with reference to Figure 4-17 for the EX0 ISR flow diagram and Code Extract 4-19.



FIGURE 4-17: EX0 ISR FLOW DIAGRAM

```
; EXTERNAL INTERUPT 0 - ISR - v2
;***********************************
EXOISR: jnb Pl.5,no_stop
no_stop:JB OEH,IG
    CLR PO.2
    CLR PO.3
    CLR TRI
    CLR TRO
    JNB 0CH,S
    CLR P2.7
    CALL DELAYLOOP
    getb 08H
    JB OCH, EXROOUT
    MOV B,R3
    MOV R7,B
    CLR RSO ;
    SETE RSI :REG EANK 1
    MOV R1,THO
    MOV RZ,TLO
    CLR RSO ;
    CLR RSI ;REG BANK 0
EXRDOUT:CLR DCH
    MOV TH1,#-10
    MOV TL1,#-10
    MOV R3,#1
    gETB TR1
IG: RETI
```


## CODE EXTRACT 4-19: EX0 ISR CODING

The first task undertaken by the interrupt service routine is to test port pin P1.5. If this pin is High (1) then EX0 was triggered by the initiation of an emergency stop or one of the systems Safety Interlocks was triggered. The ISR then jumps to the End label where the input/output ports are cleared and Powerdown mode is entered into. If P1.5 was Low (1) then the interrupt was triggered by the test probes reaching the surface of bars when being lowered or its initial position when being raised.

However, the ISR has to further ascertain if the interrupt was triggered while the ERROR READING PROCEDURE Subroutine was being executed by testing flag 0EH. This flag is Set (1) by the ERROR READING PROCEDURE Subroutine when a manual reading has to be taken due to an error and when it is Set (1), the EX0 ISR is
to ignore the interrupt and exit the ISR. The ERROR READING PROCEDURE Subroutine will be further discussed later in this chapter. When flag 0EH is tested and found to be Low (0), the interrupt was not triggered during the execution of the ERROR READING PROCEDURE Subroutine. Both the raising and lowering motion is then stopped by Clearing ( 0 ) the port pins responsible for prompting the action, i.e. P0.2 and P0.3 respectively. Thereafter, the Timers are stopped by Clearing (0) TR1 and TR0. Following this, flag 0 CH is tested. This flag is set by the RUN_UP subroutine to indicate that the Detection Unit was in the process of being raised at the moment of the interrupt.

If 0CH is set, i.e. High (1), the Detection Unit was being raised before the ISR, which means that a reading was already completed and the test probes are off the surface of the bars and at its initial position when this interrupt was triggered. It is then required that the Test Current is switched off, and this is accomplished by Clearing P2.7. If flag 0 CH was not set, i.e. Low (0), then the interrupt was triggered when the test probes reached the surface of the bars in order to take a volt-drop reading. The Test Current is therefore left on. After this process a delay is enforced by calling the DELAYLOOP subroutine.

The EX0 flag, 08 H , is then set to indicate that this interrupt has been triggered and that the associated ISR has executed. Next, flag 0CH is retested. In this case if the flag is not set (which implies that the interrupt was triggered when the Detection Unit was being lowered) the values in the timer registers are stored in Register Bank 1, register R1 (high byte) and R2 (low byte).

The Timer 1 overflow value that is stored in register R3 is copied into register R7 in Register Bank 0, see Appendix K. These values are recalled and used to calculate the Unit Raising Reference Time. Register Bank 0 is accessed using the Mode bits RS0 and RS1 in the Program Status Word Register (PSW), see Table 4-11 and Table 4-12. By setting RS0 $=1$ and $\mathrm{RS} 1=0$, the eight registers, R 0 to R 7 in Register Bank 1 can be accessed.

| CLR | RSD | : |
| :--- | :--- | :--- |
| CLR | RSI | :REG BANK |

And by resetting RS0 $=0$ and $\mathrm{RS} 1=0$, the eight registers, R0 to R7 in Register Bank 0 can be accessed

| CLR | RGO | ; |
| :--- | :--- | :--- |
| GETB | RSI | ;REG BANK |

. Note that Register Bank 0 is the default register.

| Bit | Symbol | Bit Address | Description |
| :---: | :---: | :---: | :--- |
| PSW.7 | CY | D7H | Carry Flag |
| PSW.6 | AC | D6H | Auxiliary Carry Flag |
| PSW.5 | F0 | D5H | Flag 0 |
| PSW.4 | RS1 | D4H | Register Bank Select 1 |
| PSW.3 | RS0 | D3H | Register Bank Select 0 |
| PSW.2 | OV | D2H | Overflow Flag |
| PSW.1 | - | D1H | Reserved |
| PSW.0 | P | D0H | Even Parity Flag |

TABLE 4-11: PROGRAM STATUS WORD REGISTER (PSW) SUMMARY SOURCE: THE 8051 MICROCONTROLLER

| RS1 | RS1 | Bank | Address |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | $00 \mathrm{H}-07 \mathrm{H}$ |
| 0 | 1 | 1 | $08 \mathrm{H}-0 \mathrm{FH}$ |
| 1 | 0 | 2 | $10 \mathrm{H}-17 \mathrm{H}$ |
| 1 | 1 | 3 | $18 \mathrm{H}-1 \mathrm{FH}$ |

TABLE 4-12: REGISTER BANK SUMMARY - SOURCE: THE 8051 MICROCONTROLLER

Prior to exiting and returning control to EX1 ISR the timer registers and the Timer 1 overflow count register, R3, are reloaded to force an almost immediate timer overflow hence forcing the maximum allowable time to be exceeded, as discussed earlier. Control is then handed back to the EX1 ISR by executing the RETI statement.

### 4.2.4 Timers and Timer Operation

The Automation Microcontroller makes use of both Timer 0 and Timer 1 in the Sixteen-Bit Timer mode as initialised at the beginning of the program. This means that the timer counts in $1 \mu$ s intervals from 0000 H to FFFFH. On a FFFFH to 0000 H transition an overflow occurs and the Timer Overflow Flag, TFx, is set. Both timers are used together with an overflow count register, R3, to time the duration of certain events/processes. The timer registers as well as the overflow count register are also reloaded with predefined values so that an event is allowed a maximum time in which to occur. Timer 0 is also used to enforce a delay of one second when the DELAYLOOP subroutine is called.

Timer 0 and Timer 1 are used to time how long an event takes to complete (when raising or lowering the Detection Unit) or how long an event takes to begin (When waiting for a pair of bars to be detected). To store the timer register and overflow count register values the following procedure is used referring to Figure 4-18 and Code Extract 4-20.



## FIGURE 4－18：FLOW DIAGRAM FOR THE INTERVAL TIMING PROCEDURE

|  | MOV | R1，\＃HIGH COUNT2 |
| :---: | :---: | :---: |
|  | MOV | R2，\＃LOTi COUNT2 |
|  | MOV | R3ヶ \＃200 |
| TMR2： | MOV | TH0，\＃ 0 H |
|  | MOV | TL口，\＃0H |
|  | MOV | TH1，R1 |
|  | MOV | TL1，R2 |
|  | SETB | TR1 |
|  | SETB | TRD |
| WAIT | JNB | TF1，何ATT＿T2 |
|  | Clr | trl |
|  | CLR | TRO |
|  | Clr | tEl |
|  | CLR | TF |
|  | DUNZ | R3，TMR2 |

## CODE EXTRACT 4－20：CODING FOR THE INTERVAL TIMING PROCEDURE

The process begins with Timer 1 being preloaded with the values associated with the COUNT2 symbol，i．e．-50000 ．This value is negative because it has to be loaded as 50000 less than the overflow value which for a sixteen－bit counter is 0000 H （recall that at an overflow occurs on a FFFFH to 0000 H transition）． Registers R1 and R2 are preloaded with the high and low bytes respectively of the COUNT2 value，i．e．-50000 ．R1 and R2 are later used to load the Timer 1 high and low byte registers respectively．Thereafter，the Timer Overflow Register is
preloaded with 200 . This means that a maximum of 200 cycles of $50000 \mu \mathrm{~s}$ duration will be counted, i.e.

$$
50000 \mu \mathrm{~s} \times 200=10 \mathrm{~s}
$$

This 10s is the maximum allowable time for an event to occur or begin and is the default allowable period when an interval is being timed in order to store the duration. If this time is exceeded before the event is completed or has begun, the Error subroutine associated with the interval being timed is called.

After being loaded, Timer 1 is triggered and a count is started from the preloaded value to 0000 H . While counting the Timer 1 Overflow Flag, TF1, is continuously tested in a loop. As soon as an overflow occurs, TF1 is set High (1) and the test loop is exited. The timer is stopped and the overflow flag is Cleared (0). Register R 3 is then decremented to indicate that one $50000 \mu \mathrm{~s}$ cycle has been completed. R3 is then tested to check if it holds a value of zero, indicating that $200,50000 \mu \mathrm{~s}$ cycles have been completed, hence implying that the 10s maximum allowable time has been reached.

If this is the case, the timer has exceeded the maximum allowable time before the event being timed has occurred, therefore not stopping the timer in order to store the value. When this occurs the Error subroutine associated with the interval being timed is called. For every completed $50000 \mu \mathrm{~s}$ cycle for which R3 does not hold zero after being decremented, a jump is initiated to the point where the timer registers are reloaded and then triggered to begin the next $50000 \mu \mathrm{~s}$ cycle. The reader will note that Timer 0 is also triggered and stopped at the same time that Timer 1 is triggered and stopped. The only difference in the use of these two timers is that when being reloaded, Timer 1 registers are reloaded with -50000 , i.e. 50000 counts below 0000 H , and Timer 1 registers are reloaded with 0 H . The explanation is provided with reference to Figure 4-19.


Timer 1
Timer 0


FIGURE 4-19: TIMER REGISTER OPERATION

When the stored timer register and overflow count register, R3, values are used to calculate the Detection Reference Time and the Unit Raising Reference Time, the calculation subroutine (which will be discussed under Subroutines) subtracts the value remaining in R3 from the initially loaded 200, producing the number of $50000 \mu \mathrm{~s}$ cycles that were completed during the interval that was timed. The number of cycles is not an accurate indication of the entire interval. For example, in the event that the timers were stopped due to an expected event $10255 \mu \mathrm{~s}$ after the last $50000 \mu \mathrm{~s}$ was completed and this cycle was the tenth cycle. The overflow count register, R3 will only hold the value after the last timer overflow i.e. $200-10=90$. After being processed by the calculation subroutine, the value to be reloaded into the timers and overflow count register will be $200-90=10$. Because the reloaded value is just

$$
10 \text { cycles } x 50000 \mu \mathrm{~s}=0.5 \mathrm{~s}
$$

and not the true value of,

$$
10 \text { cycles } \times 50000 \mu \mathrm{~s}+10255 \mu \mathrm{~s}=510255 \mu \mathrm{~s}=0.510255 \mathrm{~s},
$$

it is obvious that the $10255 \mu$ s that was counted just before the timers were stopped is 'lost'. In order to capture the most accurate time for an interval this "lost" time must also be captured. This is where Timer 0 is important. Referring to Figure 4-19a, it is shown that when the timers are being loaded, Timer 1 registers are loaded -50000 , i.e. 50000 counts below 0000 H . At the same time, Timer 0 is loaded with 0000 H . When the timers are started they both count up from their preloaded values. When Timer 1 reaches the FFFFH to 0000 H transition and overflows, Timer 0 registers holds 50000. In this way Timer 0 is performing a positive count/timing, beginning at 0000 H of the same period that is being counted/timed by Timer 1 from its preloaded value.

Figure $4-19 b$ provides a true representation of the timer register values for the example given above. After the ten $50000 \mu$ s cycles have been completed the timer registers are reloaded as described above, i.e. Timer 1 with a preloaded value and Timer 0 with 0000 H . The timers are then triggered and the both begin the counting/timing process. When the an event occurs that stops the timers, Timer 1 registers hold a value that is equal to the preloaded value plus the period that was just timed i.e. $10255 \mu$ s. Or, put differently, Timer 1 registers hold a value that is 10255
counts closer to the FFFFH to 0000 H transition than the preloaded value. But at the same instant Timer 0 registers holds exactly 10255. This is because the Timer 0 registers were loaded with an initial starting point of 0000 H and timed the exact period that Timer 1 did. This value, stored in the Timer 0 registers are used by the calculation subroutine to calculate the reload value for the time interval that has to be counted after the ten cycles have elapsed, hence providing a true reflection of the interval time.

Although it is good engineering practice to obtain the most accurate values as possible, for the purposes of this project, such accuracy is not imperative as a twenty percent time duration is added to the recorded time (as an allowable tolerance) by adding twenty percent more cycles to the recorded completed cycled. This will be discussed in CALC_TIME subroutine. When counting down or timing an interval for which a calculated preloaded value is being used to verify that an event is completed or begins, before the preloaded interval expires, the use of only one timer is necessary.

Here, the calculated number of $50000 \mu$ s cycles, which included the twenty percent tolerance, is loaded into register R3 and the registers of the timer being used is loaded with -50000 i.e. the same value used when recording the time interval. The timer is then triggered and at the end of each $50000 \mu$ s the timer overflow flag is Set (1) and R3 is decremented until zero is reached. When zero has been reached the timer registers are reloaded with the calculated remainder value and again triggered. If after this duration has expired the expected event has not began or been completed, the error subroutine associated with the expected event is called. If the event has started or has been completed before this interval is exceeded, the timers and overflow count register are reloaded with values that will force an almost immediate overflow when control is handed back, as described under Interrupts and Interrupt Service Routines.

### 4.2.5 Subroutines

### 4.2.5.1 The CALC_TIME Subroutine

This subroutine, as mention earlier, is used to calculate the reload values for the timer and overflow count registers when timing the completion or beginning of an event that has been allocated a maximum allowable preset time. Before the CALC_TIME subroutine is called, the calling program loads, 200 into register A in order to calculate the number of overflow counts/cycles that occurred. Further, the stored high byte timer value is loaded into Register R1, the stored low byte timer value is loaded into register R2 and the overflow count register value is loaded into R3. Referring to Figure 4-20 and Code Extract 4-21 the calculation procedure is as follows.


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FIGURE 4-20: CALC_TIME SUBROUTINE FLOW DIAGRAM

, CALC_TIME

CALC_TIME:
SUM:
MOV
R1, A
CLR C
CLR AC
CLR OV
GOl: $\operatorname{MOV} \quad A, R 3$
$\mathrm{MOV} \quad \mathrm{Br}$ \# 5
DIV AB
$\mathrm{ADD} \quad \mathrm{A}, \mathrm{R} 3$
JNC TOLL
MOV R3,\#255
CLR C
TOLL: MOV RЗ, д
CLR OV
CLR AC
RET

## CODE EXTRACT 4-21: CALC_TIME SUBROUTINE CODING

The first calculation performed is to establish the number of overflow counts that had taken place. This is done by subtracting the value held in register R 3 from the value held in register A, i.e. 200, as preloaded by the calling program. Register A is loaded with 200 because 200 was loaded into register R3 when the interval was being timed.

Register R3 was then decremented on the timer overflow every 50000 counts. So subtracting the contents of R3 from 200 produces the number of over flow cycles.

Next, all the arithmetic flags, i.e. C, CY, OV are Cleared (0). Following this, the reload value for the timer registers is calculated. Recall that the reload values for the timer registers are negative so as to load a value that is the required amount less than 0000 H . The calculation of this negative value is accomplished by finding the 2 's compliment ${ }^{4}$ of the value that was originally recorded and stored in Timer 2 registers. This calculation will now be discussed.

The contents of register R2 which holds the timer register low byte value is copied into register A. The contents of register A is then complimented. Note that register A and $B$ are used extensively during this subroutine. This is because certain instructions can only be performed using these registers. For example, the compliment instruction cannot be performed using any other register apart from register A. One (1) is then added to the contents of register A before the contents is copied back into Register R2.

The contents of Register R1, which holds the timer register high byte value, is then copied into register A where it is complimented. The Carry Flag C, which is Set (1) when there is an overflow of an eight bit register, is then tested to determine if there was an overflow of the timer low byte register R2 when one was added to it.

Example: If R2 contained 11011100 before one was added to it, it would contain 11011101 after one was added to it and the Carry Flag C will not be set.
i.e. $11011100+1=11011101$, and $C=0$

However, if R2 contained 11111111 before one was added to it, it would contain 00000000 after one was added to it and the Carry Flag C will be set.
i.e. $11111111+1=00000000$, and $C=1$

[^7]When the C is tested and found to be High (1) an overflow of R 2 is implied and one has to be added to the contents of A. If C was found to be Low (0), the contents of A is left as is. See Figure 4-21 for numerical examples using the discussed calculation process.

Next a twenty percent tolerance is added to the calculated number of cycles that are held in register R3. This is accomplished by copying the contents of R3 into register A and loading register $B$ with 5. Register $A$ is then divided by register $B$ leaving the integer part of quotient in register A and the remainder in register B . The contents of R3 is then added to the contents of A which should be twenty percent of the original value held in R3. If the Carry Flag C is Set (1) after this addition, implying an overflow, A is simply reloaded with 255 (or FFH) which is the largest value than can be counted to before an overflow in an eight bit register. Finally, the contents of A is copied back into R3, all arithmetic flags are cleared and the subroutine is exited using the RET statement.

## Example 1: Without Low Byte Overflow


$\Rightarrow$ The number of counts from 0000 H to the FFFFH to 0000 H transition

$$
=\text { FFFFH }+1=65535+1=65536,
$$

because it takes one count more from FFFFH to reach 0000 H , hence forcing an overflow

The calculated reload value $=55536$, which is 10000 less than 0000 H i.e. $65536+(-10000)=55536$

## Example 2: With Low Byte Overflow

$256=$| High Byte | Low Byte |
| :---: | :---: |
| 00000001 | 00000000 |

[ Low Byte, 1's Compliment]
Compliment of Low Byte $=11111111$
[Low Byte,2's Compliment]
Compliment of Low Byte $+1=00000000$, $\mathrm{C}=1$ [ Note: Overflow]
[ High Byte, 1's Compliment]
Compliment of High Byte $=11111110$
[ Due to Carry Flag, C being Set (1)]
Compliment of High Byte $+1=11111111$

16-Bit Word, High \& Low Byte $=1111111100000000=65280$
16-Bit Value $=1111111111111111=65535=\mathrm{FFFH}$
Overflow Value $=0000000000000000=0=0000 \mathrm{H}$
$=>$ The number of counts from 0000 H to the FFFFH to 0000 H transition

$$
=\mathrm{FFFFH}+1=65535+1=65536,
$$

because it takes one count more from FFFFH to reach 0000 H , hence forcing an overflow

The calculated reload value $=65280$, which is 256 less than 0000 H i.e. $65536+(-256)=65280$

FIGURE 4-21: EXAMPLE 2: CALCULATION OF TIMER REGISTER RELOAD VALUES USING THE 2'S COMPLIMENT ${ }^{4}$ METHOD.

### 4.2.5.2 The READING Subroutine

The READING Subroutine for the AM has only two functions. The first is to ensure constant communication with the CM READING Subroutine using port pins P0.0 and P1.7, in order to synchronise both microcontrollers during a volt-drop reading procedure. If this is not done the AM will 'run away' or continue executing statements while the CM is busy taking a reading causing the two microcontrollers to lose synchronisation with each other leading to an instability in the system.

The second function of this subroutine is to test port pin P3.1 in order to establish whether the Test Current On time is exceeded. If port pin P3.1 is High (1) then the Test Current On time has been exceeded and the Error 3 subroutine is called. See Code Extract 4-22.

```
                ;****************************
                    RD_而T: JNB Fl.7.RD_NT
                        CLR PO.0
        NOP
        NOP
        CALL DELAYLOOP
        SETB PO.0
RDNGO: JNB P1.7.RDNGO
        CLR PO.0
        CALL DELAYLOOP
RDNG: JNB E1.7.RDNGX
    JME RDNGOK
RDNGX: JNB E3.1,RDNG
        CALL ERROR3
        CLR FO.D
        JMP OUT2
RDNGOK: SETB PO.0
        NOP
        NOP
        CLR PO.0
        NOP
        NOP
        JNB P3.1,cnt_chk
        CALL ERROR3
cnt_chk:RET
```


## CODE EXTRACT 4-22: READING SUBROUTINE CODING

### 4.2.5.3 The RUN_DWNX Subroutine

The role of this subroutine is to lower the Detection Unit that houses the test probes onto the surface of the bars within a predefined time of 10 s . If the lowering process is not completed within this time, a system fault has occurred and the Error 2 subroutine is called. The operation of this subroutine is discussed below with reference to Figure 4-22 and Code Extract 4-23.

Firstly, External Interrupt 0 is enabled so that an interrupt can be generated when the test probes are on the bars to be tested and when the test probes are raised to their initial positions. Flag 0CH is cleared as a safety precaution. The Test Current is then
switched on by Setting port pin P2.7. The DELAYLOOP subroutine is then called to enforce a one second delay before the timers are loaded with the appropriate values and are triggered. The reason a delay is enforced, is to ensure that the switching times, in this case turn-on times, for the various devices such as the Detection Unit Drive Motor and the test current switch (an IGBT) are catered for before the process continues. In other words the system is forced to wait for the devices to be switched on before it continues.

A one second delay is excessive for the devices being switched here and indeed for most modern electrical switches where the worst-case turn-on and turn-off times are in the order of a few hundred milliseconds. However in order to make the system flexible in terms of replacing system components a worst case delay of one second was used to cater for almost any type of switching device turn-on and turn-off times. Note that all subroutines will be discussed in the section entitled Subroutines. Following this, the Timer registers are loaded with the 10s maximum allowable time before the Detection Unit Drive Motor is prompted to begin lowering the Detection Unit by Setting P0.3.

The timer is triggered and the ISR then waits for the timer to overflow as in the Main program and then test flag 08 H . This flag is set by EX0 and signals that the interrupt was triggered and the associated ISR has executed. If flag 08H is Set (1), then EX0 has been triggered when the test probes reached the surface of the bars before the maximum allowable time had been exceeded. The program can therefore continue as normal. If however flag 08 H was not Set (1) when it was tested the maximum allowable time had been exceeded before EX0 was triggered hence signaling Error 2. The Error 2 subroutine is the called to handle the error.



FIGURE 4-22: RUN_DWNX SUBROUTINE FLOW DIAGRAM


## CODE EXTRACT 4-23: RUN DWNX SUBROUTINE CODING

### 4.2.5.4 The RUN_UP Subroutine

The RUN_UP Subroutine is called when the Detection Unit has to be raised off the surface of the bars to its initial position. Once the subroutine is called, External Interrupt 0 is enabled so that it may be triggered when the unit has reached its initial
position. Flag 0CH is Set (1) to indicate to the EX0 ISR that the raising event is in process (for the reasons discussed earlier). Registers R1, R2 and R3 from Register Bank 0 are then loaded with the appropriate values from registers R1 and R2 (in Register Bank 1) and Register R7 respectively, for use in the CALC_TIME Subroutine in order to calculate the reload values. Following this, the Detection Unit Drive Motor is prompted by Setting (1) port pin P0.2 to begin raising the unit.

The timer is then triggered to begin the count. The subroutine then waits for the preloaded interval to expire either due to the Detection Unit not being raised to its initial position in the maximum allowable time or due to Detection unit reaching its initial within the maximum allowable time hence triggering EX0. The EX0 ISR loads the timer and overflow count registers with values that force the interval to expire prematurely. In order to determine which of the aforementioned events occurred when the interval expired, flag 08 H is tested.

This flag is Set (1) when External Interrupt 0 is triggered and the EX0 ISR executes implying that the Detection Unit did reach its initial position within the preloaded interval. When 08 H is tested and it is not Set (1) the indication is that the Detection Unit did not reach its initial position within the preloaded interval. This signals that Error 4 has occurred and therefore the Error 4 subroutine is called. Prior to exiting, the relevant flags are Cleared (0) and the subroutine is exited by executing the RET instruction. See Figure 4-23 and Code Extract 4-24.


FIGURE 4-23: RUN_UP SUBROUTINE FLOW DIAGRAM


### 4.2.5.5 The ERROR READING PROCEDURE Subroutine

This subroutine is called by error subroutines that require a manual test to be taken, i.e. Error 1 and Error 2. Recall that when an automatic volt-drop test is taken by the Test Station, the test current is switched on before the test probes are to reach the surface of the bars and switched off after the test probes have been raised off the surface of the bars (for reasons discussed earlier). This same process has to be followed when a manual test is to be taken, however, there is no guarantee that the test technician will always abide by this. Thus, the process has to be enforced.

This is the main role of this subroutine, i.e. to ensure that the test probes are not on the surface of the bars when the Test Current is switched on and off. Note that although a volt-drop reading has to be taken manually due to the error, the test is still been run in Automated mode hence the Test Current is still switched on by the controller and not the test technician. Recall that in Manual mode the Test Current is switched on by the test technician using a footswitch. The process is enforced by pausing the system and alerting the test technician, by lighting up a lamp/LED on P2.0, when the test current is being applied before the test probes are on the surface of the bars. Note that when a manual reading is being taken the lamp/LED on P2.0 will also be on if the Detection Unit, hence the Test Probes are in the initial position, i.e. fully raised, before lowering. This is to ensure that the technician investigates the possible causes of Error2, i.e. a possible malfunction of the Detection Unit drive motor, or a mechanical malfunction before continuing.

Only when the test technician raises the test probes off the bars and below the initial position before switching on the Test Current will the alert lamp/LED on P2.0 be switched off and the process be allowed to continue. The same will apply when the test probes are being raised off the surface of the bars after a reading has been taken. The Test Current will not be switched off until the test probes have been raised off the surface of the bars. As long as the test probes remain on the surface of the bars after the volt-drop reading was taken the alert lamp/LED on P2.1 will inform the test technician that the test probes should be raised. The ERROR READING

PROCEDURE Subroutine is discussed below with reference to Figure 4-24 and Code Extract 4-25.


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FIGURE 4-24: ERROR READING PROCEDURE SUBROUTINE FLOW DIAGRAM

| ERROR READING PROCEDURE |  |  |
| :---: | :---: | :---: |
|  |  |  |
| ER_I_STit <br> El_CKl: <br> AGN: | gETB | DEH |
|  | JNB | Pl. 4, El_CKl |
|  | JB | P3.2,0N_I |
|  | SETB | P2. 0 |
|  | TMP | AGN |
| ON_I: | CALL | DELAYLOOP |
|  | SETB | P2. 7 |
|  | CLR | P2. ${ }^{\text {a }}$ |
| PRBS_WT: |  | P3.2, PRBS_WT |
|  | CALL | DELAYLOOP |
|  | JB | P3.2, PRES_TT |
|  | SETB | PO. 0 |
|  | NOP |  |
|  | NOP |  |
|  | CLR | PO. 0 |
|  | CALL | READING |
| El_HLD: | JNB | Pl. 4, El_HLD |
|  | SETB | PO. $\square^{1}$ |
|  | NOP |  |
|  | NOP |  |
|  | CLR | PO. 0 |
| AGN2: | JB | P3.2,OF_I |
|  | SETB | P2. 1 |
|  | TMP | AGN2 |
| OF_工: | CALL | DELAYLOOP |
|  | CLR | P2. 7 |
|  | CLR | P2.1 |
|  | CALL | DELAYLOOP |
|  | CLR | DEH |
|  | RET |  |

## CODE EXTRACT 4-25: ERROR READING PROCEDURE SUBROUTINE CODING

Once called the ERROR READING PROCEDURE Subroutine Sets (1) flag 0EH, to indicate to the EX0 ISR that it has been called, and waits for a proceed signal from the CM Error 1 subroutine on P1.4. When received, port pin P3.2 is tested to establish whether the test probes are on the surface of the bars or at its initial position i.e. in a fully raised position. Recall that port pin P3.2 is the External Interrupt 0 trigger pin however in this case only the status of the pin is being tested. When P3.2 is Low (0) the test probes are either on the surface of the bars or at its initial position. In this case the program/process pauses, waiting for the test probes to be positioned between the surface of the bars and the Detection Unit's initial position, by the test technician. The
pausing and incorrect position of the Test Probes are indicated by the lighting up the alert lamp/LED on P2.0. When P3.2 is High (1), the test probes are not on the surface of the bars nor are they in the initial position. Although it is important to test if the test probes are on the surface of the bars before the test current is switched on it is equally important to test if the Detection Unit, hence the test probes are fixed in its initial position. The reason for this is that Error2 indicates that the test probes did not reach the surface of the bars within the allowed time due to the Detection Unit not moving from its initial position caused by a malfunction of the Detection Unit drive motor or a mechanical malfunction. When the Detection Unit and the test probes are between the surface of the bars and the initial position it indicates that the test technician has assessed the possible cause of the error. Once the test probes are in the correct position a delay is enforced, the Test Current is switched on (P2.7) and a proceed signal is transmitted to the CM before the READING subroutine is called. The ERROR READING PROCEDURE Subroutine then waits for a continue signal from the CM on P1.4 which indicates that the volt-drop reading has been captured. Once received, the AM confirms receipt of this signal by Setting (1), P0.0. Before the test current is switched off P3.2 is again tested to ascertain whether the test probes are on the surface of the bars.

As described above, if the test probes are on the surface of the bars the program/process is paused waiting for the test probes to be raised by the test technician and this is indicated by lighting up the alert lamp/LED on P2.1. When P3.2 is High (1) the test probes are not on the surface of the bars nor are they at the initial position. A delay is then enforced, the Test Current is switched off, the lamp/LED on P2.1 is switched off and further delay is enforced before the subroutine is exited using the RET statement.

### 4.2.5.6 The ERROR 1 Subroutine

This subroutine is called when Error 1 occurs due to a pair of bars not being detected within the maximum allowable preset time. The discussion that follows is with reference to Figure 4-25 and Code Extract 4-26.


FIGURE 4-25: ERROR 1 SUBROUTINE FLOW DIAGRAM

```
;*****************************
;*******************************
ERROR1: CLR PO.4
        JB 0.5H,S1
        JNB 02H,S1
        MOV R4,#HIGH COUNT2
        MOV R.5,#LOW COUNT2
        MOV B,#200
        MOV RG,B
        CLR 0.5H
        CLR 02H
        SETB 00H
        gETB 01H
S1: SETB P0.5
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        CLR FO.5
        SETB P3.5
        CALL ER_I_STK
        CLR
        B3.5
        RET
```


## CODE EXTRACT 4-26: ERROR 1 SUBROUTINE CODING

When called, the first task undertaken is to stop the Armature Drive Motor by Clearing (0) port pin P0.4. Then, as a safety measure the subroutine checks if it was called on the third pair of bars cycle, i.e. on the cycle that a reference time is stored in order to calculate the Detection Reference Time. If this is the case then the storage registers are reloaded with the default maximum allowable time of 10 s and the bar count that detects the third pair of bars is reset to the second pair.

This is done so that the reference time used to calculate the Detection Reference Time, is stored on the next pair cycle i.e. the fourth pair. Because of the reset, the fourth pair of bars is recognised as the third pair. If this subroutine was not called on the third pair cycle the above steps are simply skipped. Following this, the D flipflops that trigger External Interrupt 1 when a pair of bars is detected are cleared to put them in a known state for the next cycle by Setting (1) and Clearing (0) port pin P0.5.

The CM is then notified that Error 1 has occurred by Setting (1) port pin P3.5. This is done so that the CM can inform the GUI that Error 1 has occurred which is then displayed. Also, the CM calls its Error 1 subroutine to synchronise with the AM Error 1 subroutine.

Next, the ERROR READING PROCEDURE Subroutine is called in order to record the volt-drop reading. Once the ERROR READING PROCEDURE Subroutine is completed and returns control to the Error 1 subroutine, port pin P3.5 is Cleared (0). Control is handed back to the calling program by executing the RET statement.

### 4.2.5.7 The ERROR 2 Subroutine

The ERROR 2 Subroutine is called by the AM when the test probes do not reach the surface of the bars under test within the maximum allowable time. The discussion that follows is with reference to Figure 4-26 and Code Extract 4-27.



FIGURE 4-26: ERROR 2 SUBROUTINE FLOW DIAGRAM


```
; ERROR 2
;TEGT PROBES NOT LOWERED
;*************************:
ERROR2: CLR P0.3
    CLR P2.7
    CALL DELAYLOOF
    SETB DAH
    CALL RUN_UF
    IB OBH&E2_OUT
    SETB P3.G
    CALL ER_I_SW
    CLR E3.6
E2 OUT: CLR DAH
    CLR DBH
    RET
```


## CODE EXTRACT 4-27: ERROR 2 SUBROUTINE CODING

Once called, this subroutine first stops the Detection Unit Drive Motor from lowering the Detection Unit by Clearing (0) port pin, P0.3. The Test Current is then switched off by Clearing (0) port pin P2.7. After a delay is enforced, flag 0AH is Set (1) to
signal to the Error 4 subroutine that the Error 2 subroutine has been called. Following this, the RUN_UP subroutine is called to raise the Detection Unit to its original position using the time recorded for the error lowering process. In the event that there is also an error when raising the Detection Unit, and Error 4 is handled by calling the Error 4 subroutine, Flag 0AH is used to indicate if the Error 4 subroutine was called during the raising process called from the Error 2 subroutine.

If this is the case, the Error 4 subroutine will also handle Error 2. Next flag 0BH is tested. Flag 0BH is Set (1) by the Error 4 subroutine to indicate that it had been indirectly called from the Error 2 subroutine and that it has already signaled the CM and called the ERROR READING PROCEDURE Subroutine to record a manual voltdrop reading. If this flag is not Set (1), the ERROR 2 Subroutine alerts the CM that this error has occurred by Setting (1) port pin, P3.6.

The CM, upon receiving this signal, will call its ERROR 2 Subroutine in order to notify the GUI of the error and to synchronise with the AM. Next, the ERROR READING PROCEDURE Subroutine is called to facilitate a manual reading. On receiving control from the ERROR READING PROCEDURE Subroutine, port pin P3.6 is cleared along with flags 0AH and 0BH. Finally control is returned to the calling program by executing the RET statement.

### 4.2.5.8 The ERROR 3 Subroutine

Error 3 occurs when the Test Current on time has been exceeded. This is regarded by the system as a critical error and therefore enforces an Emergency Stop, hence a system shut down. As soon as Error 3 occurs the AM The ERROR 3 Subroutine informs the GUI via the CM. The GUI then displays this error before taking the relevant steps in preparation for a system shut down before signaling the CM and AM to do the same. The discussion that follows is with reference to Figure 4-27 and Code Extract 4-28.


```
;****************************
; ERROR 3
;TEST CUTTENT TIME EXCEEDED
;****************************
ERROR3: SETB ODH
    CALL RUN_UP
    CLR P2.7
    SETB P3.7
    nop
    CALL DELAYLOOP
    CLR P3.7
E3_HLD: JNB Fl.4, E3_HLD
    SETB PO.D
    NOP
    NOF
    GLR PD.O
    CLR ODH
    RET
```


## CODE EXTRACT 4-28: ERROR 3 SUBROUTINE CODING

When called, the ERROR 3 Subroutine first Sets (1) flag 0DH to indicate that it has been called due to the associated system error. The reason for Setting (1) this flag will be discussed shortly. Following this step, the RUN_UP subroutine is called so that the test probes are raised off the surface of the bars before the Test Current is switched off as programmed in the ERROR 3 Subroutine. The question that now arises is what happens if there is an error when the Detection Unit hence the test probes are being raised, i.e. it does not reach its initial position in the maximum allowable preset time? Well, Error 4 would have occurred and the associated subroutine i.e. the ERROR 4 Subroutine would be called to handle it appropriately.

This will however halt the system until the test technician arrives at the Test Station and assesses the problem. The time taken to assess the problem will only add to the time for which the Test Current is switched on, which is undesirable as Error 3 calls for an immediate system shut down. This is were flag 0DH plays its role. If the Error 4 subroutine is called while Error 3 has occurred, the Error 4 subroutine is immediately exited. This is because when flag 0DH is tested at the start of the Error 4 subroutine, it will be High (1). If the Error 4 subroutine was called to handle Error 4 at any point other then when Error 3 has occurred, this flag will not be set hence
allowing the Error 4 subroutine to execute as normal. The next step in the Error 3 subroutine is to switch off the Test Current, alert the CM that that Error 3 has occurred and enforce a delay. The CM will inform the GUI that Error 3 has occurred. Following this, the steps reflected in the flow diagram in Figure 4-27 and Code Extract 4-28 would technically be executed, however, since this error enforces an emergency stop both the CM and the AM are informed via their respective interrupts. Because the interrupts are triggered and the associated ISRs assume control the remaining instructions are not executed as the AM is forced to Clear (0) its input/output ports and enter Powerdown mode.

### 4.2.5.9 The ERROR 4 Subroutine

This subroutine is called when the Detection Unit hence the test probes do reach their initial position within the maximum allowable time. The discussion that follows is with reference to Figure 4-28 and Code Extract 4-29.



FIGURE 4-28: ERROR 4 SUBROUTINE FLOW DIAGRAM


```
; ERROR 4
;TEST PROBES NOT RAISED
;*****************************
ERROR4: JB ODH,E4_OUT
    CLR FO.2
    CLR E2.7
    CALL DELAYLOOP
    gETB P2.G
    nop
    CALL DELAYLOOP
    CLR P2.G
E4_HLD: TNB Pl.4,E4_HLD
    GETB PO.O
        NOP
        NOP
        CLR PO.O
        TNB DAH, E4_OUT
        SETB DBH
        SETB P3.G ;TO MICl
        CALL ER_I_首隹
        CLR P3.G
        CLR DAH
    E4_OUT: RET
```


## CODE EXTRACT 4-29: ERROR 4 SUBROUTINE CODING

When entered into, the ERROR 4 Subroutine first sets flag 0DH for the reasons mentioned in the ERROR 3 Subroutine discussion above. Next the Detection Unit Drive Motor is stopped from raising the Unit by Clearing (0) port pin P0.2. The Test Current is then switched off by Clearing (0) port pin P2.7. Following this, the CM is informed of Error 4 having occurred by setting port pin P2.6. The ERROR 4 Subroutine then enters a wait loop where it waits for the CM's ERROR 4 Subroutine to inform it that it may continue by setting port pin P1.4.

Once Set (1), the ERROR 4 Subroutine acknowledges having received this signal by Setting and Clearing P0.0. Flag 0AH is then tested to establish if Error 4 has occurred during the Run_UP procedure that was called by the ERROR 2 Subroutine. (Recall that when an error occurs while the Detection Unit is being lowered, i.e. Error 2, the RUN_UP subroutine is called to raise the Detection Unit to its original position using the time recorded for the error lowering process.) If flag 0AH is Set (1), then Error 4
did indeed occur during the RUN_UP procedure that was called by the ERROR 2 Subroutine and the steps then taken by the ERROR 4 Subroutine handles Error 2 as well. The ERROR 2 Subroutine is then simply exited when control is handed back to it due to flag 0BH being Set (1), as described earlier in the ERROR 2 Subroutine discussion. The steps taken are as follows. First flag 0BH is Set (1) in order to inform the ERROR 2 Subroutine that the ERROR 4 Subroutine has already handled Error 2.

Then the CM is informed that Error 2 has occurred by Setting (1) port pin P3.6 and the ERROR READING PROCEDURE Subroutine is called to capture a volt-drop reading. Port pin P3.6 is then Cleared (0) along with flag 0AH. The subroutine is then exited by executing the RET instruction. If flag 0AH was found to be Low (0) when it was tested the implication is that Error 4 did not occur during the ERROR 2 Subroutine and the ERROR 4 Subroutine is simply exited.

### 4.2.5.10 The DELAY LOOP subroutine

The DELAY LOOP subroutine is called whenever a delay has to be enforced, for example, when the system needs to be paused in order to allow for a device to be switched on or off after their specified switching time. Although the delay is set to be one second it can easily be shortened or increased by loading new values onto the Timer 0 and timer-overflow-count, R0, registers. The discussion that follows is with reference to Figure 4-29 and Code Extract 4-30.


FIGURE 4-29: DELAY LOOP SUBROUTINE FLOW DIAGRAM


```
RET
```


## CODE EXTRACT 4-30: DELAY LOOP SUBROUTINE CODING

Once called the timer-overflow-count register, R0, is loaded with a value of 100 . The Timer 0 , high and low byte registers are the loaded with the value (i.e. 10000 ) assigned to the COUNT symbol as initialised using the EQU directive in the main program. The high byte of the value (i.e. 10 000) assigned to the COUNT symbol is loaded into the Timer 0 high byte register and the low byte of the value (i.e. 10 000) assigned to the COUNT symbol is loaded into the Timer 0 low byte register. The timer is then triggered to begin the count. Recall that each count is one microsecond, hence 10000 counts implies $10000 \mu \mathrm{~s}$.

The DELAY LOOP subroutine then enters a waiting loop where it waits for the Timer 0 Overflow Flag (TF0) to be Set (1). This signals that the timer has overflowed implying that $10000 \mu \mathrm{~s}$ has elapsed. The timer is then stopped by Clearing (0) TR0 followed by TF0 also being Cleared (0). The timer-overflow-count register, R0, is then decremented and tested to check if the value it holds is zero. If the value is higher that zero, the Timer 0 registers are reloaded (i.e. with a value of 10000 ) and the timer is triggered to restart the cycle. If R0 does hold a value of zero then one second has elapsed and the subroutine is exited by executing the RET instruction.

In summary R0 is decremented after each $10000 \mu$ s cycle (due to a timer overflow) until it holds a value of zero. Hence, $10010000 \mu$ s cycles would have been counted.

$$
1 \text { second }=100 \times 10000 \mu \mathrm{~s}
$$

## Chapter 5

## Hardware Design

This chapter discusses the hardware design that enables the software that is executing within the embedded mirocontrollers and the GUI to be transformed into physical pulses and signals that control actuators that initiate the motion of objects in the physical world. Hardware also converts, conditions and monitors signals that are produced by transducers, which monitor the external environment, into signals and pulses that are decipherable and understood by the embedded microcontrollers.

This enables the system to respond to various inputs by executing the appropriate blocks of code in response to specific events. The author used the Protel Design Environment to draw schematics and develop the layout and routing of the PCB (Printed Circuit Board). The controller circuit was drawn in modules that link to each other using Netlables (this is a functionality that is available in the Protel Development Environment). The "Bottom-Up" design approach was used to develop this schematic. This approach involves drawing modules on independent sheets and using a Master Sheet (Entitled "Master" in this design) to facilitate linking between all schematic sheets using the above-mentioned Netlables.

Drawing schematics in modules that link to each other makes the circuit easy to understand and modify if need be, as it is uncluttered and easy to isolate a problem area. Each module will be discussed independently however, the reader will be informed as to how the module being discussed is connected to interfacing modules. The complete circuit schematic which includes all the modules discussed can be found in Appendix M, all datasheets can be found in Appendix J, and all test results are presented in Chapter 7.

### 5.1 Digital System Design

The digital system includes all digital circuitry, from the embedded controllers to the logic gates and drivers that are used in signal conditioning and level shifting respectively. The first modules to be discussed will be the Automation Microcontroller module and the Communication Microcontroller module. In both cases the 40 pin AT89S51 microcontroller was used.

### 5.1.1 The Communication Microcontroller Module

The Communication Micrcontroller module interfaces and communicates with the ADC by pulsing and reading the ADC control pins, HBEN, $\overline{C S}, \overline{E O C}$ and $\mathrm{R} / \bar{C}$ as well as receiving the 8 bit output from the ADC parallel output bus. This module also communicates with the Automation Microcontroller, reads the status on the Manual Reading switch and reacts to a forced emergency stop whether it was initiated by pressing the Emergency Stop switch or by the activation of any one of the four safety interlocks. See Figure 5-1 for a representation of the Communication Microcontroller Module and Appendix M for the complete circuit schematic.


FIGURE 5-1: THE COMMUNICATION MICROCONTROLLER MODULE.

The on-chip oscillator is driven by a quartz crystal X1 with the aid of two stabilising capacitors ( C 1 and C 2 ). Using a 12 MHz crystal and noting that each machine cycle is 12 oscillator periods, each machine cycle is calculated to be $1 \mu \mathrm{~s}$ in duration, as shown below.

$$
\begin{gathered}
\mathrm{T}=\frac{1}{12 \mathrm{MHz}}=83.33333 \times 10^{-9} \\
\mathrm{~T}_{\text {Machine Cycle }}=83.33333 \times 10^{-9} \times 12 \text { periods }=1 \mu \mathrm{~s}
\end{gathered}
$$

The reset pin (9) of the microcontroller is connected to the Reset pin of MAX 701 (see Appendix J for a complete datasheet for the MAX 701). The MAX 701 is a
supervisory circuit that monitors the supply to the microcontroller in order to detect Brown-out conditions. A Brown-out ${ }^{5}$ occurs when the supply falls to a level that is appreciably lower than the normal supply level for a prolonged amount of time. This will cause components that are powered by this supply to behave erratically and unpredictably. In the event of a Brown-out, which in the case of the MAX 701 is anything equal to or less than 4.65 V , the Reset pin of the MAX 701 goes High $(4.65 \mathrm{~V}$ or the present available positive logic High voltage) and is held at this level until the supply returns to its normal rating.

This procedure effectively holds the microcontroller in a Reset state until the supply is within its normal operating range. Note that holding the Reset pin (9) of the AT89S51 high (1) for at least two machine cycles effectively resets the microcontroller. The MAX 701 also provides a Reset-On-Power-up pulse to the microcontroller. This ensures that the microcontroller is in a known state on power-up i.e. all its input/output ports, internal registers, special function registers, program counter etc. are loaded with the default reset values reflected on Page 6 of the AT89S51 datasheet found in Appendix J.

The author originally used the RC network depicted in Figure 5-2 to provide the reset pulse on power-up. But the author's experience has shown that this network behaves erratically and is therefore unreliable in environments where EMI (Electromagnetic Interference) is a factor.

The MAX 701 solved the EMI related problems, specifically relating to Reset-On-Power-up. There were various other methods adopted to negate the effects of EMI on the circuit as a whole. Some of these include, but are not limited to, proper PCB layout and design, which involved, amongst other things, placing the microcontrollers in the center of the board and the quartz crystals as close to the microcontroller oscillator pins (XTAL1 and XTAL2) as possible.

[^8]Reduced track lengths, avoiding $90^{\circ}$ bends in tracks, routing power and signal tracks away from each other, designing multilayer PCBs with paired power and ground planes, placing $0.1 \mu \mathrm{~F}$ capacitors across all ICs with the addition of a $4.7 \mu \mathrm{~F}$ capacitor directly across the microcontrollers. Along with these, the circuit was kept compact and a common grounded guard ring was routed around the edge of the PCB.

The first line of defense against EMI is the metal enclosure in which the circuit is housed. Keeping the size of the holes on the enclosure as small as possible and ensuring that the lid makes proper electrical contact with the rest of the enclosure, this metal enclosure forms a Faraday Cage around the circuit. To further reduce the impact of EMI via conductors from the external environment, shielded cables were used.


FIGURE 5-2: PREVIOUSLY USED POWER-UP RC NETWORK

Port 0 of the AT89S51 is an open drain input/output port hence the use of external pull-up resistors. Ports 1, 2 and 3 all have internal pull-ups. The basic input/output port structure is depicted in Figure 5-3 and is sourced from The 8051 Microcontroller, by I. Scott Mackenzi.


FIGURE 5-3: INPUT/OUTPUT PORT STRUCTURE - SOURCE: THE 8051 MICROCONTROLLER

When used as an output port, writing a 1 (high) to the latch, switches off the FET holding the port pin high (VCC) via the pull-up (internal or external) resistor. When a 0 (low) is written to the latch the FET is switched on pulling the port pin to ground ( $\mathrm{V}_{\mathrm{DS}}$ to be exact). When used as in input, 1 (high) must be written to the latch to switch off the FET. In this way, only the load on the port pin can determine its state. For example, if the load on the port pin was the output of a TTL logic IC, when the IC output is high (1), typically 3.4 V , a small current will flow producing the required 1.6 V drop across the pull-up resistor to keep the Port pin at 3.4 V . The potential read on the Port pin will therefore be a high (1). When the IC output is low (0) the potential on the IC pin will be a maximum of 0.4 V .

This will allow a maximum current of 4 mA to 8 mA (depending on the type of IC and the maximum current it can sink during an output low, $\mathrm{I}_{\mathrm{OL}}$ ) to flow from VCC through the pull-up resistor down to ground via the load IC. This current flow will produce the required 4.6 V potential drop across the pull-up resistor such that when the port pin is read, it would reflect a potential of 0.4 V implying a logic level low ( 0 ). Port 1 is the input port for the 8 bit wide parallel ADC output, with port pin P1.0 set up as the LSB (Least Significant Bit) and port pin P1.7 set up as the MSB (Most Significant Bit). Ports 0,2 and 3 are used as inputs and outputs as required. This facilitates
communication with the Automation Microcontroller, control of the ADC, reading of switches, switching of LEDs and also communication with the GUI via serial port pins P3.0 and P3.1.

The interconnections between the Automation and Communications microcontrollers are summarised in the respective Microcontroller Port Utilisation tables found in Appendix K. The connections from the Communications Microcontroller to other devices are also summarised in the Communications Microcontroller Port Utilisation table found in Appendix K. Note that the $\overline{E A}$ (External Access) pin is connected to VCC. This is because when the $\overline{E A}$ pin is held low (0) the microcontroller executes programs from external ROM whilst holding the pin high (1) forces the microcontroller to execute programs from internal ROM.

The input to External Interrupt 0, P3.2, is an OR and NOR gate network which allows any of the system errors (Error 1, 2, 3 or 4) or an Emergency Stop, labeled "EmgcyStop_SW\&Intlks", (initiated by pressing the Emergency Stop switch or triggering a Safety Interlock) to trigger the interrupt. The Emergency Stop signal is an input to both microcontrollers that enforces a complete system stop by interrupting both microcintrollers forcing them to enter a safe shutdown procedure before entering power-down themselves. This Emergency Stop is initiated by the triggering of switches (push-button and interlock) on the physical system and should not be confused with the Emergency Stop that is initiated by clicking on the Emergency Stop button on the GUI, although both events yield the same end result. Including Emergency Stop triggers from various sources makes the entire system safer in the occurrence of an undesirable or dangerous event. The Emergency Stop is generated by an independent network which will be discussed later in this chapter.

### 5.1.2 The Automation Microcontroller Module

The Automation Microcontroller module is responsible for the control of all the system's actuators which include the Armature Drive Motor and the Detection Unit Drive Motor as well as the switching of the Test Current Supply via an IGBT. It also
receives input signals from the physical system to indicate the system status and the occurrence of events whether desirable or undesirable.

These input signals include the signal indicating the detection of a pair of bars, labeled "u2_EX1_Bar_Dect", the signal that indicates that the Detection Unit has reached its initial position, labeled "Detect_Unit_Switches", as well as Emergency Stop signals, labeled "EmgcyStop_gui" and "EmgcyStop_SW\&Intlks". All of the above mention signals, except "EmgcyStop_gui", are generated by independent networks all of which will be discussed later in this chapter. The "EmgcyStop_gui" signal is generated by the Communication Microcontroller to inform the Automation Microcontroller that an Emergency Stop has been initiated via the GUI. See Figure 54 for a representation of the Automation Microcontroller Module and Appendix M for the complete circuit schematic.


FIGURE 5-4: THE AUTOMATION MICROCONTROLLER MODULE

The Automation Microcontroller is set up in exactly the same way as the Communications Microcontroller. The interconnections between the Automation and Communications microcontrollers are summarised in the respective Microcontroller Port Utilisation tables in Appendix K. The connections from the Automation

Microcontroller to other devices are also summarised in the Automation Microcontroller Port Utilisation table in Appendix K.

The input to External Interrupt 0, P3.2, is an OR and NOR gate network which triggers the interrupt in the occurrence of any of the two Emergency Stop events ("EmgcyStop_gui" and "EmgcyStop_SW\&Intlks") or the occurrence of the bar detection event ("Detect_Unit_Switches"). The input to port pin P1.5 is also an OR gate with "EmgcyStop_gui" and "EmgcyStop_SW\&Intlks" as input signals. The reason for this becomes apparent when the reader recalls the discussion in Chapter 4 concerning the External Interrupt 0 ISR for the Automation Microcontroller.

The first task undertaken by the interrupt service routine is to test port pin P1.5. If this pin is High (1) then EX0 was triggered by the initiation of an emergency stop".

As soon as External Interrupt 0 (EX0) is triggered, the associated ISR first checks if P1.5 is High (1), indicating that any one of the Emergency Stop sources had been triggered. If this is the case, the system shut down and controller power-down procedures are entered into. If this not the case and P1.5 is Low (0) then the interrupt was triggered due to the detection of a pair of bars, i.e. the"Detect_Unit_Switches" signal. Hence this port pin is only used to decipher whether an interrupt was initiated due to an emergency stop or the detection of a pair of bars.

### 5.1.3 The Bar Detection Module

The Bar Detection module is responsible for alerting the Automation Microcontroller when a pair of bars has been detected. The actual detection of each copper bar on the commutator of the armature under test is undertaken using optical sensors that detect the reflection of an emitted laser beam. The Omron E3X-NA11 amplification unit together with the Omron E32-DC200 fiber optic unit (with reflective sensors) was used to carry out this task. See Appendix J for complete datasheets. The combination of these two units allow for the accurate detection of a copper bar from a distance of between 50 mm and 70 mm above the surface of the commutator. See Figure $5-5$ and Figure 5-6 for images of the commutator and the copper bars that are to be detected.


FIGURE 5-5: TYPICAL COMMUTATOR OF AN ARMATURE UNDER TEST


FIGURE 5-6: COPPER BARS ON A COMMUTATOR

The above images depict a typical commutator, however in this case, the reader will notice that there are grooves present between each copper bar. Grooves are created by
a process called Undercutting which entails the use of a motorised, revolving, circular saw blade typically 20 mm in diameter. These grooves are not present in all commutators that are to be tested. In some instances the armature that is to be tested still has an epoxy resin (from the VIP stage of the armature refurbishing process) between the bars. Due to the Turning stage (using a lathe) in the armature refurbishing process the surface of the commutator is smooth, with the copper bars and the epoxy resin being exactly the same level. It is for this reason that a high accuracy proximity sensor was abandoned. After testing various sensors, the optical sensor produced the best results and proved to be the most reliable means of detecting the copper bars.

The sensor is set on Light On mode. In this mode, an open collector NPN transistor, which is the output of the Omron E3X-NA11, is switched on when a reflected beam is detected by the reflective sensor. See Figure 5-7 below, for an extract from the device datasheet (see the complete datasheet in Appendix J), that illustrates the modes of operation and the device output circuit.


FIGURE 5-7: OPERATIONAL MODES AND THE OUTPUT CIRCUIT FOR THE OMRON E3X-NA11

The optical sensors are supplied with +15 V and the outputs from these sensors provide a clock pulse to respective positive-edge-triggered D flip-flops. The output of the D flip-flops provide the two inputs to the NAND gate which in-turn triggers the External Interrupt 1 pin on the Automation Microcontroller when driven low (0). This signal, "u2_EX1_Bar_Dect", must go low (0) only when a PAIR of bars has been detected. It must return to high (1) when the D flip-flops are cleared by the Automation Microcontroller and go low (0) again when the next pair or bars are detected. The network shown in Figure 5-8A fulfils the above triggering requirements. See Figure 5-9 for a timing diagram for the bar detection network.


FIGURE 5-8A: BAR DETECTION NETWORK

The voltage divider resistor-network ensures that 5 V is present at the output when the transistor is off (implying that no bars have been detected) and 0 V ( $\mathrm{V}_{\mathrm{CE}}$ to be exact) is present at the output when the transistor is on (implying that a bar has been detected). A 6.2 V zener diode, with a very low response time, or a Tranzorb, depending on the operating environment, is placed in parallel with the output resistor for protection purposes to ensure that the output of the voltage divider resistor-network will not exceed 6.2 V .

Initially, the network that was used as a level shifter to provide a TTL level input to the digital interface from the optical sensor output of 0 V to 15 V was a simple series resistor and zener diode network as depicted in the figure below.


FIGURE 5-8B: INITIAL LEVEL SHIFTER NETWORK

It may seem like an adequate solution, however, when one considerers the fact that the zener diode has response time, although very small, one will become aware of a potential problem that may arise when using this series network. The instant that the NPN transistor in the output circuit of the optical sensor is switched off, the zener diode is still essentially "off" as it does not respond instantaneously to the applied source. Ideally, the zener diode will be seen as an open circuit to the rest of the network for this period of time.

This being the case, the output of this series network, which is the input to the NOT gate, will for all intents and purposes, be pulled up to +15 V by the series resistor which acts as a pull-up resistor for the period before the zener diode responds or "switches on". This +15 V input is well above the absolute maximum rating for the IC and will ultimately damage it. The author used the word ultimately because, due to the very small response time of the zener diode, the IC will only be exposed to +15 V for a very short period. The IC may therefore not be damaged instantly however, repeated exposure to such high input potentials will damage the IC over time.

It is for the above reason that the voltage divider comprising of a $1 \mathrm{k} \Omega$ and $2 \mathrm{k} \Omega$ with adequate protection was used. This network produces a 5 V drop across the $1 \mathrm{~K} \Omega$ resistor when a +15 V source is applied.

$$
\mathrm{V}_{\mathrm{R} 1 \mathrm{~K}}=\frac{1 K}{1 K+2 K} \times 15 \mathrm{~V}=5 \mathrm{~V}
$$

This network ensures that the input to the NOT gate is exposed to a maximum of 6.2 V which is within recommended operating range for the IC.

The output of the resistor-zener network enters a NOT gate which inverts the signal producing an output high (1) when a bar has been detected and a low (0) when no bars have been detected. The output of this NOT gate clocks a positive-edge-triggered D flip-flop whenever a bar has been detected. Because the D input of the flip-flop is tied high (Vcc) when clocked, the output of the flip-flop, Q, goes high. The output of the D flip-flop provides the input to the NAND gate which triggers the external interrupt pin on the Automation Microcontroller. The microcontroller clears both D flip-flops, in order to put them into a known state, as soon as it enters the Interrupt Service Routine (ISR) that it vectored to when a pair of bars have been detected.


FIGURE 5-9: TIMING DIAGRAM FOR THE DETECTION NETWORK

The discussion that follows is with reference to Figure 5-9 and Figure 5-8A and describes the operation of the Bar Detection module. Assume that the commutator is rotating slowly and Sensor 1 detects a bar, the output of the NOT gate [point A] is
high (1). The low-to-high transition (positive edge) clocks the D flip-flop producing an output [at point F] that is also high (1). If, at this point, Sensor 2 has not yet detected a bar the output of the NAND gate remains high (1). The commutator will continue slowly rotating with Sensor 1 directly over it's bar until Sensor 2 detects a bar. For the purposes of this explanation, assume that Sensor 2 has also detected a bar at the same time that Sensor 1 has detected a bar (Ideal situation with an ideal commutator) the output of the NOT gate [point B], is high (1). The low-to-high transition (positive edge) clocks the D flip-flop producing an output [at point E ] that is high (1). With both the inputs to the NAND gate being high (1), the output [at point G] goes low (0).

This high-to-low transition (negative edge) triggers External Interrupt 1 of the Automation Microcontroller. The microcontroller clears both flip-flops in the associated ISR. When rotation begins again, control is handed back to the Bar Detection module. At this point both sensors indicate that they detect a bar. This is because the Armature Rotation Drive Motor was stopped as soon as both bars were detected. The outputs of the NOT gates at both point A and point B are now high (1). These high outputs however, do not clock the D flip-flops as they are positive edge triggered. Since the clock did not go low (0) before going high (1), the outputs of the flip-flops remain cleared (0) implying that the output of the NAND gate remains high (1). As the commutator rotates the sensors will pass over the groove (or epoxy resin gap) between a pair of consecutive bars.

This causes the output of the sensors to produce a low (0), via the NOT gates. On the detection of the next bar, a low-to-high transition will be created and this positive edge will again trigger the D flip-flops. Its is thus clear that the Bar Detection module only detects the NEXT pair of bars to be tested by using positive edge triggered flipflops to reject the high (1) signal from the sensors when they are still over the pair of bars that were previously detected. Note that, although theoretically both bars should be detected at the exact same time by their respective optical sensors, this is not the case practically. There are two reasons for this, one being that when the commutator is undercut some of the copper is also cut into producing bars and gaps of varying widths. The other reason is dirt, spots or marks on a bar that do not allow for the reflection of the laser. If the bars and the gaps between bars were the exact same
width throughout the circumference of the commutator and the commutator was clean, as in the case of a new commutator, both bars will be detected at the exact same time.

### 5.1.4 Mechanical Switch Input Module

This project makes use of both mechanical switches and inductive proximity switches. Inductive proximity switches are used where a high number of repetitive onoff transitions will occur as in the case when monitoring the position and initial positions of the Detection Unit. Because mechanical switches entail the physical "making" and "breaking" of metal alloy contacts the life span of mechanical switches are lower than that of non-contact switches (inductive and capacitive types) due to the wear of the metal contacts. Non-contact switches however, are much more expensive than traditional mechanical switches. It is for these two reasons that mechanical switches were used to monitor events or conditions that should not occur, and if they do, these occurrences will be very seldom thereby eliminating the contact wear as a factor. Another shortcoming that is associated with mechanical switches, and even mechanical relays for that matter, is contact bounce. When the metal contacts "make" or "break" there is a physical, high frequency bouncing action between the movable and stationary contact. See Figure 5-10 for and illustration of the above explanation.


FIGURE 5-10: MECHANICAL CONTACT BOUNCE OSCILLATIONS

Bouncing contacts lead to undesirable high frequency oscillations when a switch or relay "makes" or "breaks". These oscillations cause immense problems to digital circuitry such as multiple switching, multiple interrupt edge triggering etc. De-
bouncing refers to the elimination of these oscillations. There are two methods that can be implemented to achieve this. The first is de-bouncing using software. There various algorithms can be used to detect a change of state and thereafter verify the stability of the input line/signal, for example, allowing a delay after a change of state, pulse counting, pulse timing etc. The author has worked with many software debouncing techniques and in his experience has obtained the best results using a technique that involves the monitoring of the line after the first change of state. After the first change in state the line is read after a predefined delay, typically in the order of tens of microseconds.

If, when read, the line yields the same state for a predefined number of reading events typically twenty to fifty that state is accepted as an input. The delay time between readings, as well as the number of read events required to be stable before an input is accepted, are both variables that can be varied depending on the contact type, bounce oscillation frequency and the length of time that the oscillations are typically present for after the switch or relay "makes" or "breaks". Software de-bouncing however, becomes more complicated when the input pin is an edge triggered microcontroller interrupt. Because there are a large number of oscillations, the interrupt will be triggered on each rising or falling edge. This means that the associated ISR needs to be disabled on the first raising or falling edge and the de-bouncing algorithm needs to be initiated within the ISR. This process entails taking control from the main program for the entire de-bouncing period plus the duration of the ISR executing time.

For this design the author has opted to use a hardware de-bouncing technique that overcomes the above inconvenience as well as frees the microcontroller to use its processing power on tasks more critical to the system than de-bouncing. With reference to Figure 5-11, a $\bar{S}-\bar{R}$ latch is used to latch the line output to a stable state and keeping it stable regardless of any oscillations that may occur.


FIGURE 5-11: MECHANICAL SWITCH INPUT NETWORK

An illustration aiding the explanation of this network can be found in Figure 5-12.
In the first state with the switch on the normally closed (NC) contact the reset pin ( $\bar{R}$ ) of the latch is pulled down to ground hence resetting the latch and producing an output of 0 V . Next, the switch is to be switched on by breaking contact with the NC contact and making contact with the normally open (NO) contact. As soon as this transition is initiated, the instant contact with the NC contact is broken and the $\bar{R}$ pin is pulled high to Vcc via pull up resistor, R 2 .

The instant contact is made with the NO contact (i.e. the $\bar{S}$ pin), it is pulled down to ground initially before the bouncing oscillations begin. This first low pulse duration is sufficient to latch the output in a stable High (1) state before the oscillation have any effect on the line being read. With $\bar{R}$ held to Vcc the oscillations have no bearing on the output. See the truth table provided in Table 5-1. When $\bar{S}$ goes High (1) with $\bar{R}$ held High (1), the output remains unchanged i.e. latched High (1). And when $\bar{S}$ goes Low (0) with $\bar{R}$ held $\operatorname{High}(1)$, the output is Set (1) leaving it unchanged i.e. latched High (1). The same latching principal will apply when the switch is switched off.


FIGURE 5-12: THE $\bar{S}-\bar{R}$ LATCH USED FOR DE-BOUNCING

| $\bar{S}-\bar{R}$ Latch Truth Table |  |  |  |
| :---: | :---: | :---: | :---: |
| Inputs |  | Output | Comment |
| $\bar{S}$ | $\bar{R}$ | $\mathbf{Q}$ |  |
| 1 | 1 | NC | No Change in State |
| 0 | 1 | 1 | Latch Set |
| 1 | 0 | 0 | Latch Reset |
| 0 | 0 | 1 | Invalid Condition |

TABLE 5-1: $\bar{S}-\bar{R}$ LATCH TRUTH TABLE

As shown in Figure 5-11, hardware de-bouncing is used for all mechanical switches that provided input signals to the system. These include the Safety Interlock switches, Emergency Stop switch, Take Manual Reading switch, Manual Test Current switch etc. An OR gate network is used to output a High (1) via signal "EmgcyStop_SW\&Intlks" if any of the safety interlocks or the Emergency Stop Switch is activated. And the "Tk_Man_Rdng_SWITCH" signal alerts the controller that a manual reading is about to be taken.

### 5.1.5 The Inductive Proximity Switch Module

The Inductive Proximity Switch module is responsible for triggering External Interrupt 0 on the Automation Microcontroller when the Detection Unit has reached either its initial position, i.e. the point from which it was lowered, or when the spring loaded test probe has reached the surface of the armature under test. A single inductive proximity switch is used to monitor the position of the Detection Unit when
it is being raised to its initial position and two inductive proximity switches, one on each spring loaded probe, are used to monitor when the probes have reached the surface of the bars. See Figure 5-12. The AND gate ensures that the interrupt is only triggered when both test probes are on the surface of the commutator. The OR gate facilitates the triggering of the interrupt (by signal "Detect_Unit_Switches") when either raising or lowering the Detection unit. The outputs of the inductive switches are open collector PNP, an example of which is depicted in Figure 5-7.


FIGURE 5-12: INDUCTIVE PROXIMITY SWITCH NETWORK

When switched on, the PNP transistor connects the load, in this case the resistor-zener network, to the supply. When switched off, the PNP transistor is also turned off and is ideally seen as an open circuit. When the inductive proximity switch is switched on the inputs to the interfacing ICs are High (1), i.e. 5 V . When the inductive proximity switch is off the PNP transistor is also off. This is where the $1 \mathrm{k} \Omega$ resistor serves a second purpose - it is also a pull-down resistor, pulling the TTL input Low (0) i.e. 0V when the inductive proximity switch is off. If there was no $1 \mathrm{k} \Omega$ resistor present when the transistor is switched off, the input to the TTL circuitry will essentially be floating. The introduction of the $1 \mathrm{k} \Omega$ resistor provides a path down to ground pulling
the TTL input to ground when the Inductive switch and hence, the transistor is switched off. The $1 \mathrm{k} \Omega$ resistor together with the $2 \mathrm{k} \Omega$ resistor forms a voltage divider network and with a 6.2 V zener diode or Tranzorb in parallel with the $1 \mathrm{k} \Omega$ resistor for protection. This network operates exactly the same as the network described in the Bar Detection module.

### 5.1.6 Test Current On-Time Timing Module

This module is used to monitor the amount of time the Test Current is applied to the armature under test. Under normal test conditions the Test Current should not be required to be applied for a period longer than twenty seconds. If for any reason there is a system fault or an oversight on the part of the test technician (when taking a manual reading) that may cause the Test Current to be applied to the armature for excessive amounts of time, the system needs to be shut down in order to prevent any damage to the armature under test, the test system or any potentially dangerous situations for the test technician or any personnel in the vicinity. A 555 timer set to operate in monostable mode is preset with a period (using a $300 \mathrm{k} \Omega$ resistor, a $500 \mathrm{k} \Omega$ variable resistor, and a $100 \mu \mathrm{~F}$ capacitor) that the Test Current On-Time should not exceed. Using the equation

$$
\mathrm{T}=1.1 \mathrm{x}\left(\mathrm{R}+\mathrm{V}_{\mathrm{r}}\right) \mathrm{C}
$$

with the $500 \mathrm{k} \Omega$ variable resistor set to zero ohms, the allowable on-time is set to,

$$
\mathrm{T}=1.1 \times(300 \mathrm{k}+0)(100 \mathrm{uF})=33 \mathrm{~s}
$$

and setting the variable resistor to its full resistance value the allowable on-time is set to

$$
\mathrm{T}=1.1 \mathrm{x}(300 \mathrm{k}+500 \mathrm{k})(100 \mathrm{uF})=88 \mathrm{~s}
$$

The allowable Test Current On-Time can be preset to any value within the above range. The 555 timer is triggered by the same microcontroller output that switches the Test Current on, "Test_Current", via a NOT gate as the 555 timer is a negative edge
triggered device. The 555 timer's output is then set High (1) for the period preset by the aforementioned capacitor and resistors. When this period has expired the output returns to a Low (0) state. The Automation Microcontroller continually monitors the output of the 555 timer, "I_On_T_Exceded", during a Volt-Drop reading procedure. If this output goes Low (0) before the reading has been completed, Error 3 is signalled and the system enters shutdown by initiating an Emergency Stop. When the Test current is switched off under normal conditions (i.e. before the allowable time is exceeded) the 555 timer is reset for triggering on the next reading cycle. See Figure 513 below, for an illustration of this module.


FIGURE 5-13: TEST CURRENT ON-TIME TIMING NETWORK

### 5.1.7 The Test Current Pulse Module

Recall that this system was designed to operate in two modes, namely, Automated Mode and Manual Mode. In Automated Mode the test current is pulsed/switched on and off via an IGBT by the controller (the Automation Microcontroller to be specific) using P2.7 ("Test_Current" signal). When operating in Manual Mode the test technician is required to pulse/switch the test current on and off manually via a push
button or foot switch. This implies the IGBT driver must have two triggering sources, one for manual operation and one for automated operation. The Test Current Pulse module fulfils this purpose. With reference to Figure 5-14, the first input signal, "Test_Current" to the OR gate is provided during operation in automated mode. The second input signal to the OR gate, "Man_I", is provided during manual operation. It is clear that the IGBT that switches the test current can be triggered either during manual or automatic operation (via the "TestCuttent_Sw_Out" signal).

However for completeness and safety reasons it is required that any pulses from the push button or foot switch be ignored during automatic operation. This is accomplished using the AND and NOT gates as follows. The input signal to the NOT gate ("Auto-Man_Togl") is the same signal that the Communications Microcontroller uses to inform the Automation Microcontroller in which mode the test is to be run. For automated mode, a High (1) is signalled and for manual mode, a Low (0) is signalled. So in manual mode this signal is always Low (0) and due to the NOT gate the input to the AND gate is High (1).

The second input to this AND gate, "Man_I_Sw", is provided by the push button or foot switch that is used for the manual pulsing of the IGBT. During automated operation the signal, "Auto-Man_Togl", is always High (1). Due to the NOT gate, a Low (0) is input to the AND gate while operating in this mode. Hence, it is only during manual operation that the pulses from the manual reading, push button or foot switch, are recognised. Note that during manual operation, the Automation Microcontroller is forced to enter Power-down with all its output ports cleared (i.e. 0). This implies that the "Test_Current" input will always be Low (0) and will therefore have no influence on the triggering of the IGBT during manual operation.


FIGURE 5-14: TEST CURRENT PULSE NETWORK

### 5.1.8 The Serial Port Driver/Receiver Module

This module facilitates serial communication between the on-board serial port on the Communication Microcontroller and the serial port on the PC or Laptop that is running the GUI. The MAX 232 is an industry standard level shifter that was designed for this purpose. As shown in Figure 5-15, the interconnection of this device is simple and straight-forward with only capacitors being used as additional components, as prescribed in the MAX 232 datasheet (see Appendix J).


FIGURE 5-15: SERIAL PORT DRIVER/RECEIVER MODULE

### 5.2 Supply Regulation

The controller will be powered by a $\pm 24 \mathrm{~V}$ Switch Mode, off-the-shelf, power supply. The controller circuitry requirements include $\mathrm{a}+5 \mathrm{~V}$ supply for the digital circuitry, $\pm$ 15 V supply to power up the Op-Amps, Comparators, Optical Sensors and Inductive Proximity Switches, and a +24 V supply for any interfacing power circuitry that may be needed. The 78xx and 79xx series of voltage regulators along with stabilisation and filtering capacitors were used to provide the required regulated supply voltages. See Sheet 3 of the circuit schematic in Appendix M. Note that the string of $0.1 \mu \mathrm{~F}$ capacitors found at the bottom of this sheet are bypass capacitors that were distributed to the appropriate locations on the PCB when the PCB layout was being finalised.

### 5.3 The Data Acquisition Module

The Data Acquisition module is responsible for measuring the difference in potential between two successive bars, signal conditioning to rejecting any inputs outside the expected input range and converting the input analogue signal to a sixteen-bit word that is to be transmitted to the Graphic User Interface (GUI) via the Communications Microcontroller. See Figure 5-16A and Figure 5-16B for the block diagram describing this module.


FIGURE 5-16A: BLOCK DIAGRAM FOR THE DATA ACQUISITION MODULE


FIGURE 5-16B: DETAILED BLOCK DIAGRAM FOR THE DATA ACQUISITION MODULE

Before discussing this module any further it is important for the reader to know the type and magnitude of the input signal that is to be measured. The test supply is a maximum of $+15 \mathrm{~V} / 400 \mathrm{~A}$. The typical potential difference (or volt drop) expected to be measured between a pair of successive bars, on any armature that is to be tested, is in the range of between 100 mV and 350 mV for a healthy winding. Before the test begins the test technician will verify that readings within this range are produced by
measuring the volt drop across the first pair of bars and, if need be, varying the magnitude of the test supply or varying the arc length of the test supply probes or both to ensure that the reading produced is within the stipulated range.

The technician will thereafter measure the volt drop across at least five other successive pairs of bars that lie within the arc length of the test supply probes in order to verify the range. If the readings on these bars fall outside the range that was set on the first pair of bars the implication is that the windings of first pair of bars are unhealthy or damaged. In this case the input range must be set and verified on one of the other five measured pairs of bars.

The expected input range discussed above only applies to healthy windings, i.e. windings that are not open circuited, shot circuited or damaged. If a winding is open circuited the volt drop across the connected pair of bars will be equal to the supply potential. If a winding is short circuited the volt drop across the pair of connected bars will be zero volts. If a winding is damaged the volt-drop across the connected pair of bars will fall outside the preset variance (or tolerance) from the reference reading specified at the beginning of the test. The input signals are DC with no expected AC components. Any AC components encountered are regarded as noise and will be rejected and/or filtered.

A precision Instrumentation Amplifier, the INA 118 is used to acquire the potential difference (or volt drop) between two successive bars. See Appendix J for the complete datasheet for the INA 118. This amplifier features, amongst other things, a high Common Mode Rejection (CMR) of 110dB (at a gain of 10) and input protection up to $\pm 40 \mathrm{~V}$. It also offers a non-linearity of typically $\pm 0.0005 \%$ of the full-scale range (at a gain of 10). Some of the specifications mentioned above are stipulated at a gain of 10 . This is because a gain of 10 is set (using the external resistor, $\mathrm{R}_{\mathrm{G}}$ - see datasheet) to amplify the input signal from the hundreds of millivolts to the volt range. Hence, an input of 350 mV will be amplified to 3.5 V . This is done in order to utilise the full input range of the sixteen-bit Analogue-to-Digital Converter hence maximising the 16 -bit resolution and reducing the effects of any conversion errors should they occur.

A sixteen-bit, successive approximation, Analogue-to-Digital Converter, the MAX 1166 , with an input range of between -0.3 V and $\mathrm{V}_{\text {Ref }}(4.096 \mathrm{~V})$ is used to convert the input signal to a sixteen-bit word ( 2 eight-bit wide, parallel output words). See Appendix J for the complete datasheet for the MAX 1166. The operation of the ADC was discussed in detail in Chapter 4, under the section entitled ADC Control. The ADC was set-up to make use of the internal reference voltage as prescribed in the datasheet and shown in Figure 5-17.


FIGURE 5-17: ANALOGUE-TO-DIGITAL CONVERTER NETWORK

The ADC features, amongst other things, sixteen-bit resolution, a high speed sampling rate, an eight-bit wide parallel output and an accuracy of $\pm 2$ LSB (Least Significant Bit). With an internal $\mathrm{V}_{\text {Ref }}$ of 4.096 V and sixteen bit resolution, the smallest voltage increment that the input signal can broken down into is:

$$
\text { Resolution in Volts }=4.096 / 65536=62.5 \mu \mathrm{~V}
$$

i.e. each digital bit is equal to an analogue step of $62.5 \mu \mathrm{~V}$.

Recalling that the input signal is amplified by a factor of 10 the true analogue step size (after being scaled down in software) is $6.25 \mu \mathrm{~V}$. Similarly, the true input voltage range after being scaled down by software will be 0 to 350 mV .

This implies that a variance of

$$
\text { Variance }(\%)=\frac{6.25 \mu \mathrm{~V}}{350 \mathrm{mV}} \times 100=1.786 \times 10^{-3} \%
$$

can theoretically/ideally be detected by the system. This value has two important connotations, the first being the fact that the smallest input change that can be detected is well below $1 \%$ hence, the percentage variance from the reference reading can be calculated with a great degree of accuracy and the second connotation is that the ADC error of $\pm 2$ LSB will be almost negligible when considering the percentage variance from the reference value.

Recalling that the input range for the ADC is between -0.3 V and $\mathrm{V}_{\text {Ref }}(4.096 \mathrm{~V}$ ), the ADC has to be protected from any inputs outside this range as they will potentially damage the ADC. Out of range input signals can be produced in two ways, the first being due to an open circuit. In this case, the potential difference across the pair of bars that are connected to an open circuited winding will equal to potential of the test supply current (which may be as high as 15 V ). The second way an out of range reading can be produced is by the reversal of the orientation of the test probes with respect to the test supply probes.

This means that when the test current positive probe is to the right of the negative probe and the positive test probe is to the left of the negative test probe (or versa-visa) a negative reading of equal magnitude to the positive reading will be produced. This situation can arise when the test technician setting up the test reverses the polarity of the test supply or when the test technician is taking a manual reading and uses an independent (unauthorised) set of test probes to take a manual reading and unknowingly reverses the orientation of the polarity of the inputs with respect to the potential of the test supply probes. Although this situation should not occur protection has to be designed into the system to prevent any hardware damage that may occur. The reader may ask why an ADC with an equal positive and negative input range (e.g. $\pm 5 \mathrm{~V}$ ) is not used.

The answer to this is - the expected input range is between 0 and 3.5 V (after amplification). And with a sixteen-bit ADC that has a positive input range (eg. +5 V ), all sixteen bits are dedicated to conversions within this positive range. If a sixteen-bit ADC with an equal positive and negative range was to be used, eight bits will be dedicated to the positive range, 0 to +5 V , and the other eight bits will be dedicated to the negative range, 0 to -5 V . Hence only an eight bit resolution can be expected for the readings of importance i.e. those within the 0 to 5 V range. The eight bits dedicated to the conversion of negative values will only be used in events of unwanted or undesirable readings that are produced by an incorrect system set up or use. In the author's opinion, the eight bit resolution used for the negative range of inputs is wasted. The author has hence elected to use a sixteen-bit ADC with only a positive input range and has devised a method of rejecting all unwanted and potentially damaging input signals. This method will be discussed in the paragraphs that follow.

With reference to Sheet 4 of the circuit schematic found in Appendix M, the first stage of the data acquisition module is the INA 118 instrumentation amplifier. This stage is followed by a filtering stage that comprises capacitors of various values which facilitates more efficient filtering over a range of frequencies. Seeing as the output of the instrumentation amplifier is expected (and required) to be purely DC in nature, any AC components found on this signal must be filtered before the signal progresses to the next phase of the system. It is for this reason that capacitors were used as low-pass filters instead of low-pass high order passive or active filters with a cut-off frequencies set very low (almost zero Hertz, in this case).

In the phase that follows, three Voltage Followers (or Buffers) makes three identical copies of the original signal. A Voltage Follower is simply an Op-Amp (LM 741 in this case) with its output fed directly into its inverting input. The non-inverting input is the input pin for the signal. This network produces an output with zero gain, i.e. an output that is equal to the input. A fourth Voltage Follower is placed at the input to the ADC .

Note that all the Op-Amp and Comparator ICs that are used make provision for a potentiometer that is used to nullify the output offset voltage. These potentiometers are also used for "tuning" purposes to ensure that the signal which is the input to the
$A D C$ is equal to the signal at the input end of the data acquisition module provided that the magnitude of signal is within the allowable $A D C$ input range.

Three identical copies of the input signal are made purely to maintain the integrity of the input signal to the ADC. Two comparator stages are required to determine whether the input signal is outside the ADC input range. These two stages are in parallel implying that they each require a perfect copy of the original input signal. The third copy of the input signal flows directly to the ADC input via an analogue switch. If only one signal was used in each of the comparison stages before being input to the ADC , the integrity of that one signal would be compromised, i.e. the ADC input signal will vary from the original input signal to the data acquisition module.

Recalling that the input of the ADC must be within the -0.3 V to 4.096 V range, a comparison must be done in order to reject all inputs outside this range. This comparison is done in two parallel stages. The first stage determines if the input signal is less than the ADC reference voltage, $\mathrm{V}_{\text {Ref }}$, which is equal to 4.096 V . In order to do this a comparator (the LM 311) is used with the input signal connected to the comparator's inverting input and a reference voltage connected to the noninverting input pin. The reference voltage is set up using a voltage divider network that comprises of a $2 \mathrm{k} \Omega$ and a $9 \mathrm{k} \Omega$ resistor both with a $1 \%$ tolerance. With these values the expected reference at zero percent variance is:

$$
\mathrm{V}_{\mathrm{Ref}}=\frac{9 k \Omega}{9 k \Omega+2 k \Omega} \times 5 \mathrm{~V}=4.091 \mathrm{~V}
$$

with $\mathrm{a} \pm 1 \% \mathrm{~V}_{\text {Ref }}$ variance of the range between 4.076 V and 4.105 V .

The output of LM 311 is open-collector, with pin 7 being the collector end and pin 1 being the emitter end of the output transistor. Connecting the collector (pin 7) via a pull-up resistor to the +5 V supply and connecting the emitter (pin 1) to ground, the comparator outputs a High (1), i.e. +5 V , when the non-inverting input is greater than the inverting input and a Low ( 0 ), 0 V (or $\mathrm{V}_{\mathrm{ce}}$ ) when the inverting input is greater than the non-inverting input. The output of this comparison stage is connected to the first of two inputs of an AND gate.

The second comparison stage is tasked to ensure that all negative input signals are rejected. Here the input signal is connected to the non-inverting input pin of the comparator (LM 311) and the reference is connected to the inverting input. The reverence voltage, $\mathrm{V}_{\text {Ref, }}$ is set to 0 V by connecting the inverting input directly to ground. However, the reader should note that a voltage divider network that is set up between -15 V and ground (Gnd) is provided in the event that a slightly negative reference is required due to the operating environment. To set a 0 V reference using this network the resistor to ground is replaced with a physical jumper and the resistor to the negative supply is not inserted. The output of this comparison stage is connected to the second of the two inputs to the AND gate.

When the input signal is within range the first comparator stage will produce a High input signal to the AND gate because the potential at the inverting pin will be greater than that at the non-inverting pin. The second comparator stage will also produce a High input signal to the AND gate for the same reason. The output of the AND gate is hence High. The output of the AND gate ("V_RangeDetect") provides the input to the Communication Microcontroller's P0.2. Before a reading can be taken this input port (i.e. P0.2) is tested to verify if it is High (1).

If this is the case, the Analogue Switch (MAX 4622) is switched on by the Communication Microcontroller port pin P0.0, allowing the signal to pass through to the ADC input pin. See Appendix J for a complete datasheet for the MAX 4622. If this port pin is Low, the analogue switch is left off, connecting the ADC input pin to ground. The MAX 4622 analogue switch has a low on-resistance, with a normally open, normally closed and a common pin. It can be operated from a bipolar supply of $\pm 18 \mathrm{~V}$, although in this case the operating supply is $\pm 15 \mathrm{~V}$. This allows the analogue switch to control any input within this range without any damage which makes it perfect for this application. When the input pin of this device is low, as in the case where the input signal is found to be outside the allowable range, the common pin is "connected" to the normally closed pin which in this case is connected to ground. When the input pin of this device is High, as in the case where the input signal is found to be within the allowable range, the common pin is "connected" to the normally open pin which in this case is connected to output pin of the first voltage follower stage which represents the input signal to the data acquisition unit.

For completeness, if the input signal is higher than the preset reference, $\mathrm{V}_{\text {Ref, }}$, of the first comparison stage as in the case where an open circuit is detected on a winding connected to the pair of bars under test, the output of the comparison stage will be Low. This is because the inverting input will be at a higher potential than the noninverting input. The output of the AND gate will therefore be Low hence ensuring that the Communication Microcontroller keeps the analogue switch off. This in turn ensures that the ADC input remains connected to ground, i.e. 0 V , and not to the out-of-range input signal.

If the input signal is lower than preset reference, 0 V , of the second comparison stage, as in the case where the orientation of the test probes is reversed with respect to that of the Test Supply probes, the output of the comparison stage will be Low. This is because the inverting input will be at a higher potential than the non-inverting input. The output of the AND gate will be Low ensuring that the Communication Microcontroller keeps the analogue switch off. This in turn ensures that the ADC input remains connected to ground, i.e. 0 V , and not to the out-of-range input signal. It is in this way that all out-of-range inputs are rejected by the data acquisition module.

This method was not the first approach that was tried. After researching and experimenting with adaptive (variable) gain Op-Amp networks, arithmetic using a number of Op-Amp stages, scaling and using various switching devices such as relays, BJTs and FETs, this approach was found to be the simplest, most effective and most accurate method of rejecting out-of-range input signals while still maintaining the integrity of the original input signal.

### 5.4 Automation Output Module

This relatively simple module provides the signals that control the actuators in the automated system via the respective electronic control drives such as inverters in the case of motors and IGBT drivers in the case if IGBTs. The controller is just one module of the entire Automated Test Station. Other modules that interact with this module are the two electronic motor drives (one for the rotation of the armature under test and the other for lowering and raising the detection unit), the IGBT driver and the GUI. With this in mind, the author provided two types of control outputs.

The first being simple 5V TTL control signals. These can be used to pulse any type of drive or drivers via a second output module that will have to be designed depending on the input requirements of the drivers that are being used. This second output module can be considered as a level shifter or adapter that will make it possible for the controller to be more versatile and to be seen as a "plug and play" module that can be used with an array of different transducers, drivers and drives, provided that the adaptor is designed for those transducers, drivers and drives that are being used.


FIGURE 5-18: CONTROLLER OUTPUT MODULE

The other outputs that are provided are specifically designed for the drives and drivers being used for this project. As per the contractor's requirements, three switching devices that can 'make' and 'break' a $24 \mathrm{~V} / 20 \mathrm{~mA}$ input must be provided for the drives that control the motors. The drive itself has a $24 \mathrm{~V} / 20 \mathrm{~mA}$ source that will be the input to the switching device with the output of the switching device providing an
input to the input pins of electronic drive. Hence the electronic motor drive is controlled by controlling the switching device. As has been the pattern throughout this design process, the author has opted to use semiconductor switches rather than mechanical switching devices such as mechanical relays, for the reasons explained earlier. In this case, a gate logic level power MOSFET was used. See Appendix J for a complete datasheet for the IRLU120N. The IRLU120N is a power MOSFET with a gate that is activated and deactivated by 5 V and 0 V logic level pulses respectively, hence avoiding the need for gate drivers. Off the shelf IGBT drivers are today available with inputs that operate on 5 V and 0 V logic level pulses. It is for this reason that one TTL output is provided for IGBT switching.


[^0]:    ${ }^{5}$ Brown-out refers to the condition where the rms supply voltage falls to a value that is appreciably lower than the normal value but not zero. In the case of a Black-out, the supply falls to zero, i.e. there is a complete loss of the supply.

[^1]:    ${ }^{6}$ When installing the GUI onto a Desktop Computer or Notebook, the installer must create a folder entitled Calibration in the Program files folder on the C drive.

[^2]:    OMRON Corporation
    Industrial Automation Company
    Industrial Sensors Division
    Sensing Devices and Components Division H.Q.
    Shiokoji Horikawa, Shimogyo-ku, Kyoto, 600-8530 Japan
    Tel: (81)75-344-7068/Fax: (81)75-344-7107
    Regional Headquarters
    OMRON EUROPE B.V.
    Sensor Business Unit, Carl-Benz-Str. 4, D-71154 Nufringen, Germany
    Tel: (49)7032-811-0/Fax: (49)7032-811-199
    OMRON ELECTRONICS LLC
    1 East Commerce Drive, Schaumburg, IL 60173 U.S.A.
    Tel: (1)847-843-7900/Fax: (1)847-843-8568
    OMRON ASIA PACIFIC PTE. LTD.
    83 Clemenceau Avenue,
    \#11-01, UE Square, 239920 Singapore
    Tel: (65) 835-3011/Fax: (65)835-2711
    OMRON CHINA CO., LTD.
    BEIJING OFFICE Note: Specifications subject to change without notice.

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[^4]:    ${ }^{1}$ The ' $x$ ' in TRx represents 0 or 1, thus implying TR0 or TR1. From this point forward, an ' $x$ ' used in this form, in conjunction with any other register, will also represent a 1 or a 0.

[^5]:    ${ }^{2}$ Note that the $\overline{C S}$ third falling edge can occur immediately after $\overline{E O C}$ is driven Low, as $\mathrm{t}_{\mathrm{DV}}$ is stipulated as a minimum of $0 \eta \mathrm{~s}$

[^6]:    ${ }^{3}$ Note that the preloaded time always expires. Hence, a check has to be made to verify if it expired due to having exceeded the maximum allowable time or if it was forced to expire due the External Interrupt ISR.

[^7]:    ${ }^{4}$ A negative of a binary number is the 2 's compliment of its corresponding positive number. To calculate the negative value using the 2 's compliment system, the original positive binary number has to be first complimented (this is 1's compliment), before one (1) is added to the Least Significant Bit (LSB).

[^8]:    ${ }^{5}$ Brown-out refers to the condition where the rms supply voltage falls to a value that is appreciably lower than the normal value but not zero. In the case of a Black-out, the supply falls to zero, i.e. there is a complete loss of the supply.

