DESIGN AND ANALYTICAL PERFORMANCE OF SUBTHRESHOLD CHARACTERISTICS OF CSDG MOSFET

Thesis submitted for the fulfillment of requirements for the degree of

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Electronic Engineering

by

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As the candidate's supervisor, I have approved this dissertation for submission.

Signed……. Date: **22st Feb. 2019**

Prof. (Dr.) Viranjay M. Srivastava

Declaration

I declare that the content of this dissertation is original except where due reference has been made. It has not been submitted prior to this time for any degree to any other institution.

---------- **22st Feb. 2019**

Uchechukwu Anthony Maduagwu Date

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Dedication

This thesis is dedicated:

To God Almighty

First and foremost, I dedicate this research work to God Almighty. God have always been faithful to me. His loving kindness and favour are unmeasurable towards me all through this process. This whole programme would not have been successful without his guidance and protection.

To My Dad, Mr. Chidi Maduagwu, and My Aunty and Uncle, Mr. and Mrs. Ifi

I am indeed grateful for raising me up. Your sacrifices and efforts will never be forgotten. Thank you for all the prayers, love and care, you have shown me. It is because of your words that I decided to embark in this research work and you have always been there all through this research work. Accept my eternal gratitude for all your efforts.

To the memory of my late mum, Mrs. Afadi Vivian Maduagwu

All the love in this world cannot express the immense love I have for you. How I wish you stayed longer with me before your departure. May your soul rest in peace. I am very grateful for bringing me into this world. Adieu mum.

To my Aunts and Uncles, Gift Ife, Promise Ife, Ndubisi Ifi, Oluchi Ifi, and Idu Onyemize

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List of Abbreviations

1D	One Dimensional
2D	Two Dimensional
3D	Three Dimensional
AC	Alternative Current
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide Semiconductor
CSDG	Cylindrical Surrounding Double-Gate
CSG	Cylindrical Surrounding Gate
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DG	Double-Gate
DSGM	Double Surrounding Gate Material
ECP	Effective Conduction Path
ECPE	Effective Conduction Path Effect
EMA	Evanescent-Mode Analysis
IC	Integrated Circuit
ITRS	International Technology and Roadmap for Semiconductors
MEMS	Microelectromechanical System
MOS	Metal-Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PPA	Parabolic Approximation Analysis
RF	Radio Frequency
SCEs	Short Channel Effects
SOI	Silicon-On-Insulator
SRAM	Static Random-Access Memory
TSGM	Triple Surrounding Gate Material
VLSI	Very Large-Scale Integration

List of Symbols

L	Channel length
W	Channel Width
$\boldsymbol{\phi_{MS}}$	Work Function
$\boldsymbol{Q_{eff}}$	Effective charge
Q_c	Surface charge
Q_B	Depletion charge
n_i	Intrinsic carrier concentration
N_a	Doping concentration
V_T	Thermal voltage
V_{th}	Threshold voltage
$\boldsymbol{V_{GS}}$	Gate-source voltage
$\boldsymbol{V_{GB}}$	Gate-body voltage
$\boldsymbol{V_{FB}}$	Flat-band voltage
$\boldsymbol{V_{DS}}$	Drain-source voltage
V_{bi}	Built in Voltage
V_{bs}	Substrate bias voltage
$\boldsymbol{C_{ox}}$	Oxide capacitance
C_{si}	Silicon capacitance
$\boldsymbol{E_g}$	Band gap energy
$\boldsymbol{\chi}$	Electron affinity
$\boldsymbol{\psi_s}$	Surface Potential
$\boldsymbol{\psi_{ox}}$	Oxide potential
$\boldsymbol{\varepsilon_{ox}}$	Permittivity of the oxide
$\boldsymbol{\varepsilon_{si}}$	Permittivity of the silicon
$\boldsymbol{t_{ox}}$	Oxide thickness
t_{si}	Silicon thickness
λ	Scaling length
q	Electronic charge
r	radius

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Journal Publications

1. **Uchechukwu A. Maduagwu** and Viranjay M. Srivastava**,** "Analytical Performance of the threshold voltage and subthreshold swing of CSDG MOSFET" ***Journal of Low Power Electronics and Applications*** *(JLPEA),* vol. 9, no. 1, pp. 1-20, March 2019. ***[SCOPUS]***

2. **Uchechukwu A. Maduagwu** and Viranjay M. Srivastava**,** "analytical performance of potential distribution of CSDG MOSFET Using Evanescent-Mode Analysis," ***Int. J. of Engineering and Technology, UAE*** (*IJET),* vol. 7, no. 4, pp. 5649-5633, 2018. ***[SCOPUS]***

Conference Papers

3. **Uchechukwu A. Maduagwu** and Viranjay M. Srivastava, "Bridge rectifier with Cylindrical Surrounding Double-Gate MOSFET: A model for better efficiency," *25th Int. Conf. on the Domestic Use of Energy (DUE 2017),* Cape Town, South Africa, 3-5 April 2017, pp. 109-113. ***[IEEE Xplore]***

4. **Uchechukwu A. Maduagwu** and Viranjay M. Srivastava, "Effect of radius on thermal noise for cylindrical surrounding double-gate MOSFET," *IEEE Int. Conf. on Engineering and Technology (ICET 2016),* Coimbatore, India, 16-17 Dec. 2016, vol. 2, pp. 217-220.

ABSTRACT

The downscaling of the Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) devices have been the driving force for Nanotechnology and Very Large-Scale Integration (VLSI) systems. This is affirmed by *Moore's law* which states that *"The number of transistors placed in an Integrated Circuit (IC) or chip doubles approximately every two years".* The main objectives for the transistor scaling are: to increase functionality, switching speed, packing density and lower the operating power of the ICs. However, the downscaling of the MOSFET device is posed with various challenges such as the threshold roll-off, Drain Induced Barrier Lowing (DIBL), surface scattering, and velocity saturation known as Short Channel Effects (SCEs). To overcome these challenges, a cylindrically structured MOSFET is employed because it increases the switching speed, current flow, packing density, and provides better immunity to SCEs.

This thesis proposes a Cylindrical Surrounding Double-Gate (CSDG) MOSFET which is an extended version of Double-Gate (DG) MOSFET and Cylindrical Surrounding-Gate (CSG) MOSFET in terms of form factor and current drive respectively. Furthermore, employing the Evanescent-Mode analysis (EMA) of a two-dimensional (2D) Poisson solution, the performance analysis of the novel CSDG MOSFET is presented. The channel length, radii Silicon film difference, and the oxide thickness are investigated for the CSDG MOSFET at the subthreshold regime.

Using the minimum channel potential expression obtained by EMA, the threshold voltage and the subthreshold swing model of the proposed CSDG MOSFET are evaluated and discussed. The device performance is verified with various values of radii Silicon film difference and gate oxide thickness

Finally, the low operating power and switching characteristics of the proposed CSDG MOSFET has been employed to design a simple CSDG bridge rectifier circuit for micropower electricity (energy harvester). Similar to the traditional MOSFETs, the switching process of CSDG MOSFET is in two operating modes: switch-ON (conduction of current between the drain and source) or switched-OFF (no conduction of current). However, unlike the traditional diode bridge rectifier which utilizes four diodes for its operation, the CSDG bridge rectifier circuits employs only two CSDGs (*n-channel and p-*

channel) for its operation. This optimizes cost and improves efficiency. Finally, the results from the analyses demonstrate that the proposed CSDG MOSFET is a promising device for nanotechnology and self-micro powered device system application.

CHAPTER-1

INTRODUCTION

1.1 Background

The advent of solid-state electronics began with the Bipolar Junction Transistor (BJT) which was one of the most trending inventions of the 20th century [1]. Over the past years, such inventions have been shown to have an unparalleled impact on the improvement of semiconductor science and technology [2]. However, the BJT shows a delay characteristic when turned *ON* and *OFF*. This limits it for high frequency switching applications because of large base-storage times. Due to this lapse in digital integrated circuits design, Complementary Metal-Oxide-Semiconductor (CMOS) technology has replaced the BJT with a unipolar device called the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).

The MOSFET was proposed and fabricated by Kahng and Attalla in 1960 [3]. The phrase 'Metal–Oxide–Semiconductor' is a benchmark for the physical structure of certain field effect transistors, containing a silicon substrate on which an oxide layer is grown and an electrode of metal (polysilicon) is placed on the top of the oxide. The MOSFETs are generally voltage-controlled devices with high input impedance, which enhances their application in both analog and digital circuits. As a voltage is applied on the gate electrode of MOSFETs, some charges are induced at the interface between the oxide and the substrate. These induced charges create a channel by connecting the two other contacts of the MOSFET structure called the source and drain end as shown in Figure 1.1. The channel allows the flow of current between the drain and the source. Moreover, their lack of gate current, resulting in switching ability faster than BJT, enables them to form the basis of semiconductor memory devices called microchips.

In 1958, Jack Kilby proposed the idea of Integrated Circuit (IC) and the first IC known as the 'S-R flip flop' was fabricated by Robert Noyce in 1961 as shown in Figure 1.2. The design methodologies of the modern ICs are reputable in the CMOS technology. The term 'CMOS' is defined as a semiconductor technology used to produce the integrated circuits known as microchips.

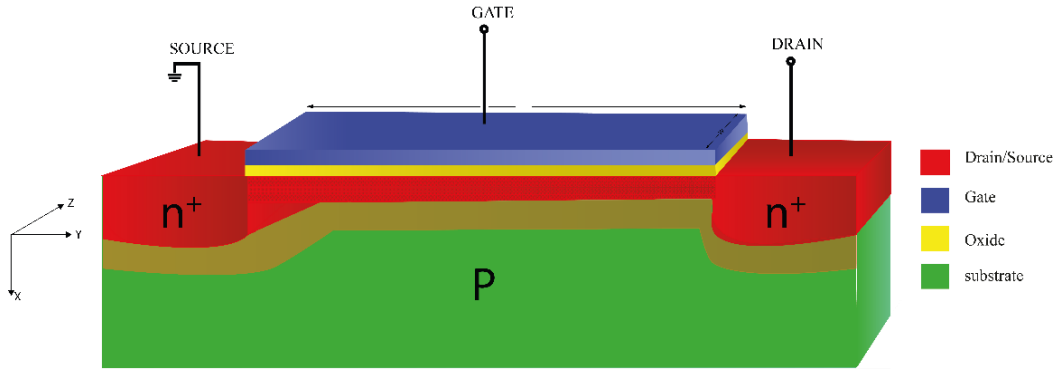


Figure 1.1. Bulk MOSFET.

The CMOS circuits comprised the *n-type* and *p-type* MOSFETs arranged in complementary form. In analog systems, CMOS circuits are used as data converters, image sensors and highly integrated transceivers in analog communication technology, whereas in digital systems CMOS circuits are used in microprocessors, Static Random-Access Memory (SRAM), microcontrollers and other digital logic circuits. Characteristically, the commercial integrated circuits contain billions of MOS transistors of both *n-type* and *p-type* MOSFETs on a rectangular silicon piece of 10 mm height and 400 mm breadth.

1.2 Justification for the Research Work

This section presents the challenges of CMOS technology from one generational node to another as the MOSFET size is being downscaled. Moreover, a brief description of the evolution and the advantages of the multi-gate structures as a promising device for the *22-nm* technological generation is presented.

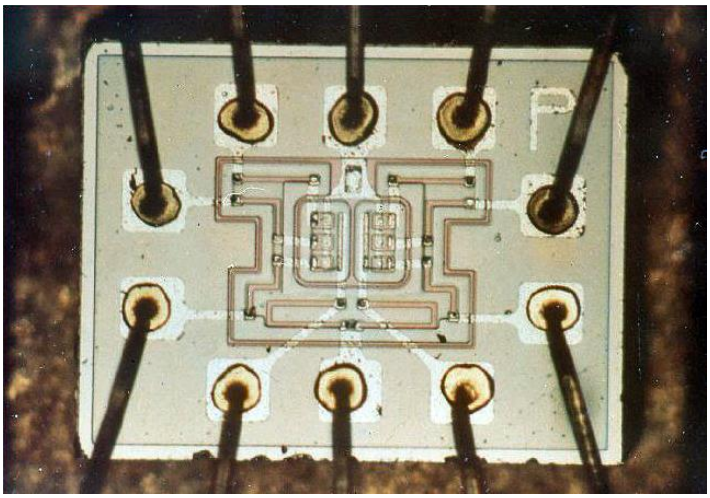


Figure 1.2. S-R Flip Flop IC [4].

1.2.1 Challenges of CMOS Technology

For the last few decades, the downscaling of CMOS devices has been the driving force of the semiconductor industry [5, 6]. The main objective behind the device scaling is to increase the number of transistors (CMOS devices) per unit area (packing density) of an IC, its functionality, speed and low operating power from one technological node to another. This was predicted by Moore's Law [7] that 'the number of transistors per chip will increase by twice its size every 18 months'; as illustrated in Figure 1.3. However, some issues like reduction in threshold voltage (voltage roll-off), increase in subthreshold leakage current and irregularity in the switching (subthreshold swing) of the devices arise as the MOSFET size is being downscaled. These adverse effects are known as the Short Channel Effects (SCEs) which increase drastically in MOS structures at nanoscale [8].

In 1974, Dennard et al. [9] proposed a scaling theory to downscale the conventional bulk MOSFET to sustain Moore's Law based on three variables: (i) The dimension, (ii) voltage, and (iii) doping. First, it states that all linear dimensions are reduced by the unitless scaling factor *k* both horizontally and vertically. Secondly, the voltage applied to the device should be reduced by the same factor *k*. Finally, the substrate doping concentration should be increased by the same factor *k*. For almost three decades, the work of Dennard et al. [10] became the benchmark in the semiconductor industry. It provided guideline principles to MOSFET design, circuit design, and chip design in the early history of integrated circuits.

However, the adoption of the scaling theory in conventional MOSFETs will not be relevant beyond *22-nm* technology node generation as predicted by the International Technology and Roadmap for Semiconductors (ITRS) 2008 guideline [11, 12]. The reason is that the conventional MOSFETs have compelled a physical limit on additional scaling. Further scaling will result in excessive SCEs which increase the device's static power dissipation and overall performance. Hence, at sub-micron level Moore's Law becomes invalid in conventional MOSFETs.

Therefore, to sustain the CMOS technology trend the SCEs needed to be suppressed [13]. In view of this, it has been established that non-conventional multi-gate structures such as Silicon-On-Insulator (SOI) MOSFETs, Double-Gate (DG) MOSFETs, and Cylindrical Surrounding Gate (CSG) MOSFETs as shown in Figure 1.4 have emerged to provide better control of the SCEs [14-19]. The CSG MOSFETs provide greater coupling

of the gate around the silicon pillar, resulting in more improved gate control over the MOSFET channel than SOI and DG MOSFETs [20]. But in terms of current drive, the CSG MOSFETs have lesser current compared with the DG MOSFETs, and this makes them limited for high performance [21]. That is, they cannot operate at higher frequencies and lower voltages. Double-gate structures [22-24] introduce the concept of volume inversion leading to higher current drive. However, the fabrication process remains the major challenge, especially the alignment of the front and back gates [25].

Therefore, the modification of the CSG MOSFET became a necessity to boost the current drive and further improve the SCEs' immunity. Such promising device structure for the *22-nm* technology node generation is called the Cylindrical Surrounding Double-Gate (CSDG) MOSFETs.

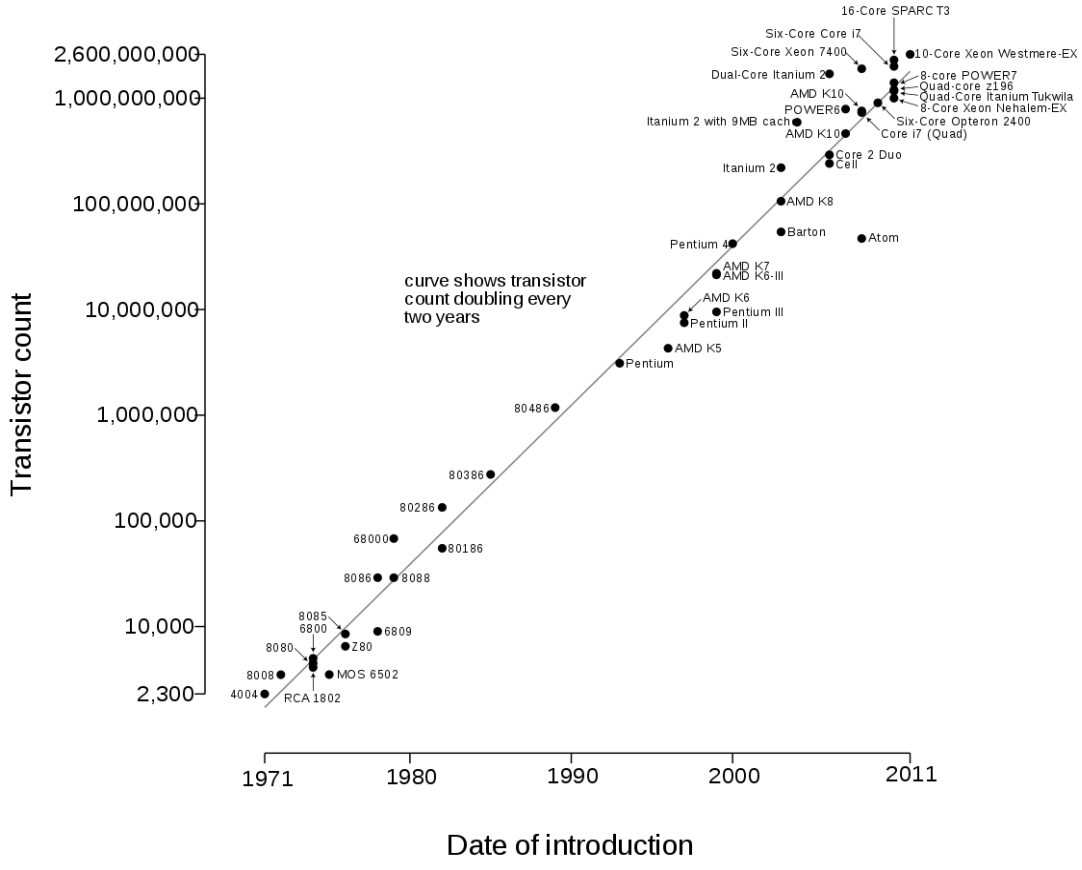
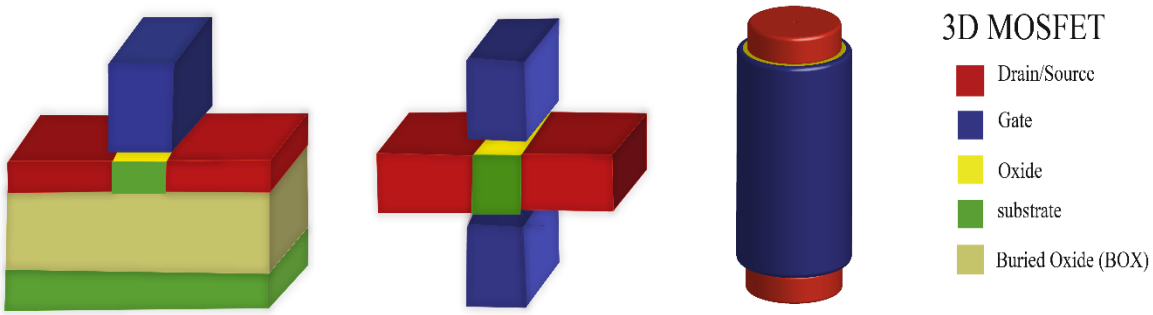


Figure 1.3. Transistor Integration on chips displaying Moore's Law [26].



a) b) c)

Figure 1.4. 3D Structural view of the a) SOI MOSFET b) DG MOSFET c) CSG MOSFET.

1.2.2 Cylindrical Surrounding Double-Gate (CSDG) MOSFET

CSDG MOSFET belongs to the family of multi-gates with a hollow-like cylindrical structure. It has a similar structure to that of non-conventional CSG MOSFET and to conventional MOSFET in terms of source, drain, gate, and channel. However, the control of the channel is from both the internal and external gate, and the structure is basically formed from DG MOSFET. Srivastava et al [24] have proposed an undoped CSDG MOSFET as shown in Figure 1.5 with the aim of controlling the silicon channel very efficiently and further suppressing SCEs. It has been proved that CSDG MOSFETs have higher drive current and greater gate controllability compared to single SOI MOSFETs, CSG MOSFETs, and DG MOSFETs.

1.2.3 Advantages of CSDG MOSFET

A. **Better scalability:** The CSDG MOSFET has higher scalability than DG MOSFET, CSG MOSFET and other GAA MOSFETs and better immunity to SCEs, the reason being that the internal and external cylindrical surrounding gates create an electrical sheltering action for lateral electric field resulting from the charges in the drain and source regions. This superior scalability makes CSDG MOSFET a promising device for the *22-nm* technological node in 2018.

B. **Solution to Gate misalignment challenges of DG MOSFET**: The major drawback of DG MOSFET, the misalignment of the front and back gates, is mitigated with CSDG MOSFET. The CSDG MOSFET gates can easily contact the circular source and drain in a long and circular path thereby avoiding gate misalignment challenges.

C. **Better channel control than CSG MOSFET:** In comparison with CSG MOSFET, the CSDG MOSFET offers maximum gate controllability over the channels. This is achieved with the help of the internal cylindrical gate present in it. The internal gate, with the external gate, provides superior control over the channel and improvement in SCEs when compared to CSG MOSFET.

D. **Higher drive current:** CSDG MOSFET operates in two different modes: (i) separate inversion and (ii) volume inversion. In the former, two conduction channels are formed; one is in the interface between the external gate oxide and silicon substrate while the other is at the interface between the internal gate oxide and the silicon substrate. The total current from the channel flows all around the cylindrical structure, unlike the DG MOSFET, where the volume inversion is only at the top and bottom. Hence, the volume inversion can be practically higher than that of DG MOSFET.

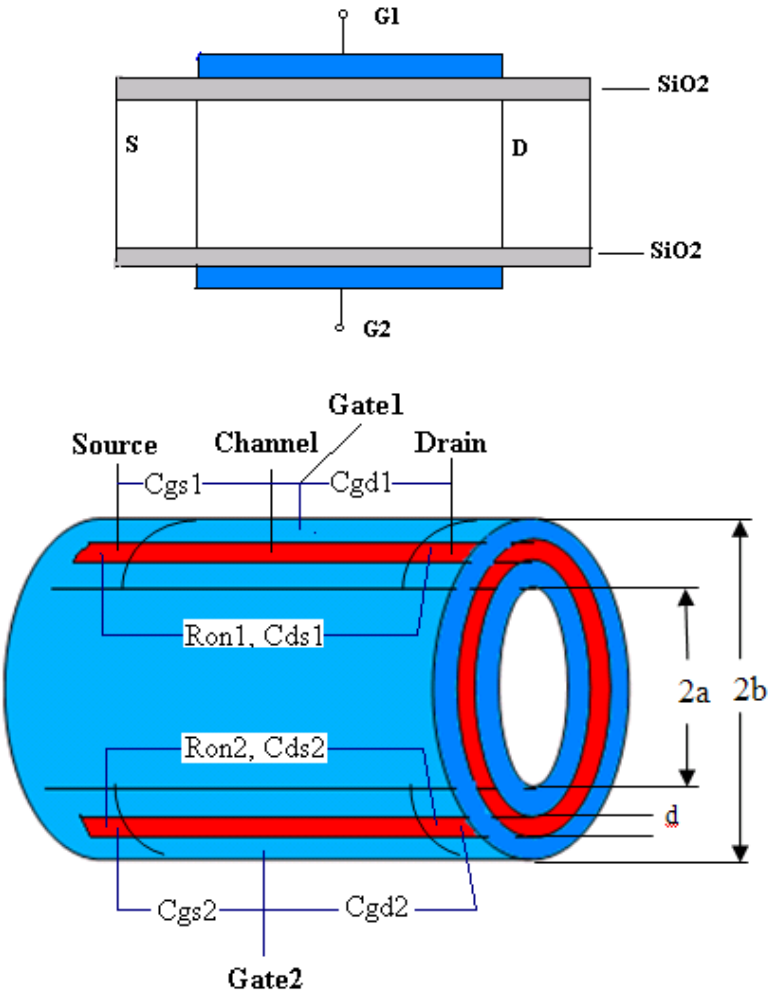


Figure 1.5. Capacitive and Resistive equivalent structure of CSDG MOSFET [27].

E. Higher transconductance: CSDG MOSFETs provide higher transconductance when compared with CSG MOSFETs, since they operate at high current drive. This makes the device a good candidate for Radio Frequency (RF) applications because RF CMOS requires higher transconductance for better switching and speed.

F. High switching frequency: Since CSDG MOSFET provides better immunity to SCEs and minimizes the problem of current leakage, it becomes a suitable device in integrated circuits due to its higher *On-to-OFF* current ratio than the DG MOSFET and CSG MOSFET devices.

1.2.4 Disadvantages of CSDG MOSFET

A. The structure of the device might pose a challenge in the fabrication processes.

B. The complexity of the structure makes it rigorous to analyze.

Based on the advantages, this dissertation considers the modelling of the novel CSDG MOSFET structure at subthreshold regime. Moreover, a simple model has been proposed to predict the device's characteristics.

1.3 Research Objectives

Diverse research has been done with models that could help provide a solution to the 2D Poisson equation of non-conventional MOSFETs like SOI MOSFET, DG MOSFET and CSG MOSFET. However less work has been done on CSDG MOSFETs, especially in the subthreshold regime. The main objectives of the research work are to:

A. Analytically model the minimum channel surface potential of the external and internal gates of the CSDG MOSFET using Evanescent-Mode Analysis (EMA).

B. Derive a close-form expression for threshold voltage, subthreshold current and subthreshold swing of the CSDG MOSFETs using minimum surface channel potential.

C. Apply the switching characteristics of CSDG MOSFET in rectification of the energy harvested from the environment with microelectromechanical systems (MEMS).

Furthermore, the secondary objective of this research is to:

D. Investigates the effects of the device parameters like channel length, oxide thickness and the radii silicon film difference on the channel potential in comparison with the device simulation; and

E. Observe the effects of the SCEs and various means of minimising it through the device parameters.

1.4 Research Methodology

This research dissertation uses the Evanescent-Mode Analysis (EMA) proposed by Frank et al. [28] to model the potential distribution of the lightly doped Cylindrical Surrounding Double-Gate (CSDG) MOSFET because the subthreshold conduction is governed by it. The EMA is a mathematical method used to simplify the 2D Poisson equation. It has been used to analyse the device characteristics of both heavily and lightly doped devices like SOI MOSFET, DG MOSFET, and CSG MOSFET. This research focuses on the 2D analytical modelling of the 3D structure of CSDG MOSFET to evaluate its potential distribution. The 2D Poisson equation is solved with the proposed model and the minimum surface potentials for both internal and external gates of the CSDG MOSFET is obtained. Furthermore, its threshold voltage, subthreshold current, and subthreshold swing expressions are equally deduced analytically.

The approach at which the models are used in this work is different from that proposed by other researchers. In the modelling of the 2D structure we considered the internal and external radius independently with the help of the boundary condition. Then, we applied the EMA model different from Parabolic Approximation Analysis (PPA) [29] to obtain the channel potential distribution of the novel 3D structure. The EMA has been applied with the method of separating variables. This method involves combining actions of many factors by dividing the potential into several parts and each of them representing a single physical factor, which makes it more efficient in determining the total potential in the channel.

The channel potential is subjected to the boundary condition along the channel axis to obtain the minimum channel potential for both the external and the internal gate of the CSDG MOSFET. Furthermore, the derived minimum channel potential is employed in the derivation of the threshold voltage, subthreshold current and the subthreshold swing. The obtained analytical expression is compared with the numerical simulation for verification.

1.5 Scope and Limitation

This research work considers precisely the analytical modelling and numerical simulation of the channel potential, threshold voltage, subthreshold current, and subthreshold swing of the proposed novel multi-gate structure called CSDG MOSFET in the subthreshold (weak inversion) region. The essence of this work is to observe the behaviour of the CSDG MOSFET at the subthreshold region with device parameters – also, to minimise the effects caused by downscaling convectional MOSFET and other proposed non-conventional MOSFETs as the CMOS technology approaches the *22-nm* technology node in 2018. This work is limited to analytical models of subthreshold characteristics using EMA approach. The model is used analytically to obtain the channel potential that matches the experimental value from device simulation using the MOSFET parameters. Furthermore, the short channel effects like the surface scattering, velocity saturation and impact ionization have not been considered in this work. With regards to scaling, our analytical model of CSDG MOSFET is valid for only channel length of *30 nm* and above. The quantum mechanical effects and tunneling which dominate in a very short channel device of *10 nm* are neglected in our model.

1.6 Contribution to Knowledge

The following contributions have been made in this research work:

A. A new device structure of CSDG MOSFET has been proposed for the simple modelling of the subthreshold characteristics.
B. Analysis of the subthreshold characteristics shows that the proposed CSDG MOSFET is among the promising device structures for further downscaling of CMOS technology and better immunity to SCEs.
C. In terms of application, the CSDG MOSFET was used in the rectification of the energy harvesting system (energy harvested from the environment) for better efficiency and cost effectiveness.

1.7 Thesis Organisation

This dissertation focuses on the performance analysis of the CSDG MOSFET. The primary goal is to study, derive and analyses the performance of the channel length of

CSDG MOSFET with respect to the variation in the device parameters like oxide thickness, radii silicon film difference and gate voltage. The remaining part of this dissertation is divided in five chapters, each with multiple sub-sections.

Chapter 2 explains the background study of the MOS structure and preliminary requirement for further understanding of the remaining chapters. Also, the analytical models proposed by different authors from traditional MOSFETs to multi-gate MOSFETs ranging from the charge sharing model to PPA have been reviewed. The reasons why they failed to give proper description of SCEs are pointed out and a better solution is proposed. Furthermore, the generalised EMA model as applicable to other structures is reviewed and the previous work on CSDG MOSFET also highlighted.

Chapter 3 introduces the proposed CSDG MOSFET, the structural view and the detailed modelling of the CSDG MOSFET using an EMA model flow chart to solve the 2D Poisson equation. The channel potential distribution of the structure has been derived from which the minimum surface potential of the internal and external gate of CSDG MOSFET is obtained. Also, the behaviour of the short channel has been observed with respect to variation of the oxide thickness and radii silicon film difference to analyse the Short Channel Effects on the structure.

Chapter 4 is an extension of chapter 3. The minimum surface potential derived from chapter 3 is utilised in the derivation of the threshold voltage model. The behavior of the threshold voltage with respect to the channel length has been observed, based on the variation of oxide thickness and radii silicon film difference. Also, the subthreshold current and the subthreshold swing model are derived. The subthreshold current model is based on diffusion mechanism while the subthreshold swing model is obtained with the minimum surface potential. Furthermore, the behavior of the model with respect to the radii silicon film difference and oxide thickness is observed.

Chapter 5 explains the application of CSDG MOSFET in the micro-power system. The energy harvested from the environments through the microelectromechanical system (MEMS) is rectified by CSDG MOSFET for useful input to the micro electronic devices such as wireless remote controls and the wireless sensor nodes. The CSDG MOSFET *turn-on* threshold voltage at short channel is within $0.2\ V$ to $0.4\ V$. This makes it an important substitute for traditional bridge rectifier in the micro power system.

Finally, **Chapter 6** contains the conclusion and discussion of the future works.

CHAPTER-2

BACKGROUND INFORMATION AND LITERATURE REVIEW

2.1 Introduction

This chapter introduces various definitions of the general physics of MOS structure and terms used. Also, several models like charge sharing model, empirical model, polynomial model and Parabolic Approximation Analysis (PPA) have been reviewed from Bulk MOSFET to multi-gate structures. Their strengths and weaknesses are clearly highlighted. Also, the EMA model is reviewed for different MOSFET structures. Furthermore, the previous works by various researchers for the CSDG MOSFETs are reviewed.

2.2 General Physics of MOS Structure Terms

The understanding of the MOSFET's device operation relies on the fundamental principles of the MOS structure. This section presents the general MOS structure terms for better understanding of the subsequent chapters.

2.2.1 Fermi Level

Fermi level [30] is defined as the highest energy state occupied by an electron in the semiconductor at absolute zero temperature. This concept was derived from Fermi-Dirac statistics. Since electrons are fermions, only two electrons of opposite spin can exist in the same energy state according to the Pauli Exclusion Principle [31]. So, the remaining electrons pack into the lower available energy state and build up a 'Fermi sea' of electron energy states. That surface of the sea at which no electron has energy to rise above at absolute zero temperature is called the Fermi level. The concept of Fermi energy becomes necessary to understand the electrical and thermal properties of solids. Fermi energy is in the order of electron volts and it plays a crucial rule in the band theory of semiconductors.

For an intrinsic semiconductor, the Fermi potential level lies in the same position, whereas in a doped semiconductor, *n-type* and *p-type*, the Fermi-level is shifted by the

impurities due to their band gaps. The position of the Fermi level with respect to the conduction band is the main parameter in determining the electrical properties of a device.

2.2.2 Energy Band Diagram of MOS Structure

The energy band diagram [32] displays the electron energy level in metals and in a semiconductor of MOS structure with respect to the conduction (E_C) and valence band (E_V) edge in the oxide and silicon, as described by Fermi energy. Deep inside the semiconductor, the electron energy is assumed to be zero because of charge neutrality. And, as the electrons gain energy above the *1.1 eV* band gap energy of silicon, conduction takes place. Whereas in oxide it is *8 eV*, which make it act as an insulator. The band energy diagram described in Figure 2.1 shows the modes of operation (p-type semiconductor): Flat band condition, Accumulation, Depletion and Inversion.

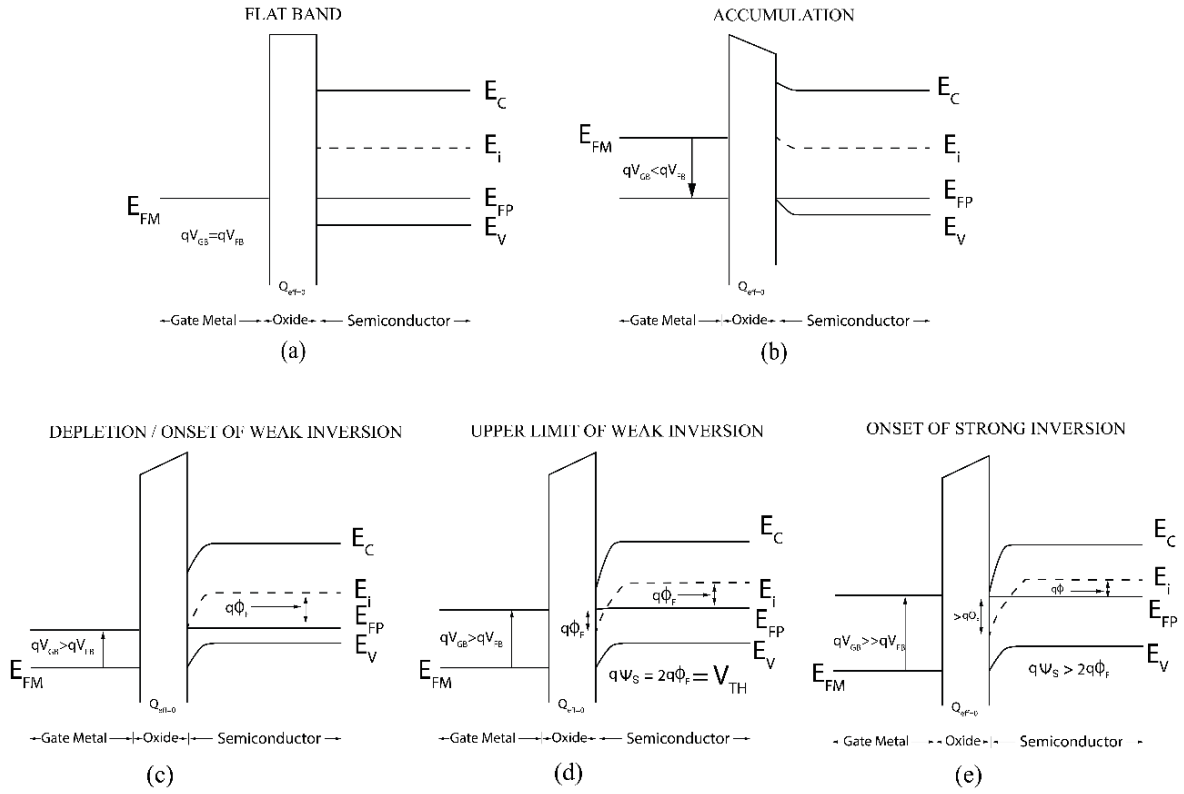


Figure 2.1. Energy band diagram for MOS structure with *p-type* substrate assuming work function $(\phi_{MS}) = 0$ and effective oxide charge $(Q_0) = 0$ for various value of gate-source voltage (V_{GS}): (a) Flat-band condition (b) Accumulation (c) Depletion (d) Weak inversion (e) Strong inversion [30, 33].

2.2.3 Flat-band Condition

As the name implies, the flat-band condition [34] refers to the fact that the semiconductor has a flat energy band diagram because of zero net charges in it as described in Figure 2.1. The flat-band voltage (V_{FB}) condition is obtained when the applied gate voltage equals the work function difference between the gate metal and the semiconductor, assuming zero parasitic charges in the oxide and zero net charge difference in the oxide-semiconductor interface. The flat-band voltage plays an important role in determining the threshold voltage of modern short channel devices. The authors from [32] presented the condition for the flat-band voltage as:

$$Flatband \triangleq \begin{cases} V_{GB} = V_{FB} \\ Q_s = 0 \\ \psi_s = 0 \end{cases} \tag{2.1}$$

The flat band voltage is given by the well-known formula [34]:

$$\left.\begin{aligned} V_{FB} &= \phi_{MS} - \frac{Q_{eff}}{C_{ox}} \\ \phi_{MS} &= E_{Fm} - \left(\chi + \frac{E_g}{2e} + E_{fp} \right) \end{aligned}\right\} \tag{2.2}$$

where ϕ_{MS}, Q_{eff}, C_{ox}, χ, E_g, E_{fm}, E_{fp}, e *and* ψ_s are the work function difference between channel and the gate, effective charge in the oxide, oxide capacitance, electron affinity of the semiconductor, band gap energy, Fermi energy level of the gate metal, Fermi energy level of the *p-type* substrate, the electric charge and the surface potential respectively.

2.2.4 Work Function

An electrostatic potential is established when an electron moves from one material to the other through the junction. The measure of how difficult it is for an electron to leave the host material is called the work function [8]. The contact potential between two different materials is basically the work function difference between the two dissimilar materials in electron Volts (*eV*). It varies from one material to another [8].

2.2.5 Effective Charges at the Interface

In MOS structure, various charges exist at the interface, namely; (i) fixed oxide charges, (ii) oxide trapped interface charges, (iii) mobile ionized charges and (iv) interface trapped charges. All these charges are collectively known as effective charge [35]. Due to charge neutrality law, all these effective charges cause a total charge of $+Q_0$ to appear on the system. So, the $+Q_0$ will cause a $-Q_0$ to be in the system. Since these charges are present at the gate, substrate end of the oxide, a potential drop of ψ_{ox} will occur across the oxide. The value is given as [35]:

$$\left.\begin{aligned} \psi_{ox} &= -\frac{Q_o}{C_{ox}} \\ C_{ox} &= \frac{\varepsilon_{ox}}{t_{ox}} \end{aligned}\right\} \tag{2.3}$$

where C_{ox} is the total capacitance per unit area between the two ends of the oxide, ε_{ox} is the permittivity of the oxide and t_{ox} is the oxide thickness.

2.2.6 Accumulation Region

Considering a *p-type* MOS structure in which the gate-to-body voltage (V_{GB}) decreases below the Flat-Band voltage (V_{FB}), that is when the V_{GB} becomes more negative, the negative change in (V_{GB}) results in negative change in the gate charges per unit area (Q_G). Q_G must be balanced by positive silicon charges at the interface (Q_S) according to charge neutrality [34]. Thus, a hole will accumulate at the oxide-silicon interface to provide a net positive charge. Furthermore, the negative charges in V_{GB} will cause a negative change in the surface potential ψ_s and potential drop across the oxide ψ_{ox}, as shown in the energy band diagram in Figure 2.1, and the band bends upward [36].

$$\text{Accumulation Conditions} \triangleq \begin{cases} V_{GB} < V_{FB} \\ Q_s > 0 \\ \psi_s < 0 \end{cases} \tag{2.4}$$

2.2.7 Depletion Region

Assuming the V_{GB} is slightly greater than V_{FB}., then the positive charge per unit area at the surface will drive holes away from the oxide-silicon interface. This causes the interface to be depleted of holes. So, as the (V_{GB}) increases above (V_{FB}), the hole density keeps decreasing below the doping concentration value, N_A. Then, the charge Q_S is due to the uncovered acceptor atoms in which each contributes to negative charges -q leading to the band bending downward towards the oxide-silicon interface as shown in the energy diagram in Figure. 2.1 [8].

$$\text{Depletion} \triangleq \begin{cases} V_{GB} > V_{FB} \\ Q_s < 0 \\ \psi_s > 0 \end{cases} \tag{2.5}$$

2.2.8 Inversion Region

The inversion region is divided into two parts. The weak inversion and the strong inversion as described below.

Weak Inversion Region

As the V_{GB} is increased further, more acceptor atoms are uncovered and the ψ_s becomes more positive to attract number of electrons (e^-_s) to the surface. Further increase in V_{GS} will result to attraction of significant number of electrons towards the surface and further downward bending of the energy band. Each of these electrons contributes charges, -q to Q_s. So, the V_{GB} at which electron concentration n_s under the gate equates the concentration of the hole in the silicon substrates, $N_{A,}$ is called the threshold voltage. It's also called the upper limit of weak inversion as proposed by Arora [33]:

$$\left.\begin{aligned} \psi_s &= 2\phi_f \\ n_s &= N_A \\ \phi_f &= \phi_t \ln \frac{N_a}{n_i} \end{aligned}\right\} \tag{2.5}$$

where ϕ_f, n_i, $\phi_{f,}$ is the Fermi-potential drop, intrinsic carrier concentration, and thermal voltage respectively. Under threshold, few electrons or minority carriers exist in the

region. This enables subthreshold conduction to take place, although not strong enough to cause the stream flow of current, hence the region is called the weak inversion or subthreshold regime.

As the MOS integrated circuit has evolved to exploit the nanotechnology regime, it became expedient to research more deeply the minority carriers that are present under the gate when the gate voltage is less than the threshold voltage, since they play an important role in causing undesirable leakage current in the device and the IC structure. Thus, the subthreshold region of operation is as important as the traditional cut off, linear and saturation region of operation in the traditional MOSFET.

Strong Inversion Region

At higher value of V_{GB}, the density of electrons exceeds the holes at the surface. As a result, the ψ_s rises above Fermi-potential by several thermal voltages ϕ_t. Hence, the MOS operates in a strong inversion region and current tends to flow from the drain to the source

$$\left.\begin{aligned} \psi_s &= 2\phi_f + \phi_0 \\ n_s &> N_A \end{aligned}\right\} \tag{2.6}$$

where ϕ_o depends on several values of ϕ_t whose value depends on the substrate doping and oxide thickness [8].

$$Inversion \triangleq \begin{cases} V_{GB} >> V_{FB} \\ Q_s < 0 \\ \psi_s > 0 \end{cases} \tag{2.7}$$

2.2.9 Potential Balance and Charge Balance

Surface potential is the total potential drop across the surface region of a MOS structure. There are three types of potential drop in the MOS structure when connected to an external environment (source voltage, V_{GB}). These include the following:

a) Potential drop across the oxide, ψ_{ox}
b) Surface potential drop, ψ_s
c) Several contact potential drops, ϕ_{MS}

The several potential drops of the external gate voltage across the MOS interface results to the potential balance equation as given [37]:

$$V_{GB} = \psi_{ox} + \psi_s + \phi_{MS} \tag{2.8}$$

Since, the contact potential is a known constant, it can be neglected. Therefore, any change in the external gate voltage will result in a corresponding change in the oxide and surface potential drop as given [37]:

$$\Delta V_{GB} = \Delta\psi_{ox} + \Delta\psi_s \tag{2.9}$$

Likewise, the charges must balance one another for overall charge neutrality in the structure and, assuming the oxide effective charges are fixed, then the charge balance equation is expressed as [8]:

$$\left.\begin{aligned} Q_G + Q_0 + Q_C = 0 \\ \Delta Q_G + \Delta Q_C = 0 \end{aligned}\right\} \tag{2.10}$$

Also, the gate charge-potential balance and semiconductor charge-potential balance are given as [37]:

$$\left.\begin{aligned} Q_G = C_{ox}\psi_{ox} \\ Q_C = Q_C(\psi_s) \end{aligned}\right\} \tag{2.11}$$

Solving equation (2.8), (2.9) and (2.11) yields basic semiconductor MOS equation that is consistent in the silicon-oxide interface as given:

$$Q_C = C_{ox}(V_{GB} - V_{FB} - \psi_S) \tag{2.12a}$$

where

$$\begin{aligned} \frac{Q_G}{C_{ox}} &= \frac{-Q_C}{C_{ox}} = \psi_{ox} \\ C_{ox} &= \frac{\varepsilon_{ox}}{t_{ox}} \end{aligned} \tag{2.12b}$$

This equation is widely used in the analytical modelling of all MOSFET structures both conventional and non-conventional. The major difference to its application to any MOSFET structure is based on the boundary conditions.

2.2.10 Threshold Voltage

Threshold voltage is the value of the gate voltage required to attain the threshold inversion point as given by the equation (2.6) for NMOS. Although, in our work, we reported the *n*-channel MOS, its extension, PMOS is considered in our application of CSDG MOSFET in chapter 5. There are several ways of determining the threshold voltage; one of the methods is by using the I_d-V_{GS} graph [38]; another method is called the extrapolation method [39] by finding the minimum surface potential at the gate [40, 41]. We utilised the minimum surface potential with the help of EMA to obtain the threshold voltage of the CSDG MOSFET structure, since this method is analytically based.

2.2.11 Subthreshold Swing

The subthreshold swing [42] determines how effectively the gate voltage could stop the flow of drain current when decreased below the threshold voltage. Hence, it predicts the *OFF*-current with respect to the subthreshold current. Furthermore, the subthreshold current was obtained on the principle of the trapezium integration in consonance with the approach with Liang et.al. [42].

2.3 Review of Short Channel MOSFET models with their established Limitations

This section reviews different short channel models of MOSFETS structures from decades ago to date. The models are discussed as follows:

2.3.1 Yau's Charge Sharing Model

Since 1970, many analytical models for threshold voltage of short channel devices have been published, among which is the charge sharing model proposed by *Yau* in *1974* [43]. As the channel length is decreased, the drain and source magnetic field lines contribute to the channel of the MOSFET as shown in Figure 2.2. The x_j is the depth of the drain and

source junction, L is the channel length, W_{dm} is the maximum depletion depth of the gate, and t_{ox} is the gate oxide thickness. For lightly doped substrate $N_{A,}$ the classical threshold condition is given as $2\phi_f$ [44].

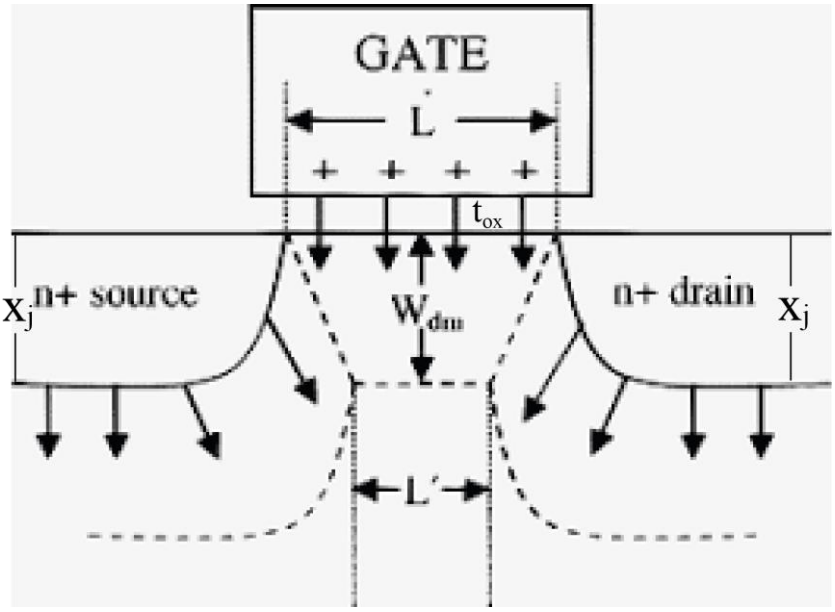


Figure 2.2. Short channel P-Type MOSFET illustrating Charge sharing [43].

Hence, the author obtained:

$$\left.\begin{aligned} W_{dm} &= \sqrt{\frac{2\varepsilon_{si}(2\phi_f + V_{bs})}{qN_a}} \\ \phi_f &= \phi_t \ln\frac{N_a}{n_i} \end{aligned}\right\} \tag{2.13}$$

where ε_{si}, ϕ_t, V_{bs} and n_i are the permittivity, thermal voltage, substrate biased voltage and carrier concentration respectively. Furthermore, the authors obtained the threshold voltage for long channel as given:

$$\left.\begin{aligned} V_{th} &= V_{FB} - 2\phi_f - \frac{Q_B}{C_{ox}} \\ Q_B &= qN_aW_{dm}(L + L^1) \end{aligned}\right\} \tag{2.14}$$

where V_{FB} is the flatland voltage, C_{ox} is the oxide capacitance per unit area, Q_B is the total depletion charge, W_{dm} is the width of the MOSFET structure and L is the gate length at the top and L^1 is the gate length at the bottom. Considering the area of trapezium within the MOSFET structure, excluding the charges from the source and drain, Q'_B with respect to the channel length due the short channel within the area of the trapezium, shape was obtained by the author as:

$$Q'_B L = qN_a W_{dm}((L + L^1)/2) \tag{2.15}$$

$$\frac{L + L^1}{2L} = \left(1 - \left(\sqrt{1 + \frac{2W_{dm}}{r_j}} - 1\right)\frac{r_j}{L}\right) \tag{2.16}$$

It was assumed that the under the depletion depth, W_{dm} under the gate is the same as that of the drain and the source. Hence, in the analysis, the short channel threshold voltage for bulk MOSFET was obtained as:

$$V_{th} = V_{FB} - 2\phi_f - \frac{Q_B}{C_{ox}}\left(1 - \left(\sqrt{1 + \frac{2W_{dm}}{r_j}} - 1\right)\frac{r_j}{L}\right) \tag{2.17}$$

As r_j/L tends to infinity, the threshold voltage equation obtained in equation (2.17) reduces to that of the Long channel case obtained in equation (2.14).

The most impressive significance of Yau's model is the ability to predict the depletion depth at which the SCEs occur. He pointed out that SCEs become negligible if $L >> W_{dm}$. However, Yau's model did not provide adequate analysis for the effect of oxide thickness. It is obvious that a gate with thicker oxide would have less effect on the depletion charge than the corresponding thin oxide [45]. Another shortcoming of Yau's model is the lack of consideration of Drain Induced Barrier Lowering (DIBL) effect which decreases the channel potential at the drain end. Also, there was an incorrect prediction of SCE as approximately *1/L*.

Furthermore, earlier literature [46] also obtained SCEs as an approximately *1/L* expression by creating a partition of three regions in the depletion region as drain region, source region and gate region, explaining that the region near the drain and source contains less charges per width compared to the region under the gate. The derivation was not based

on charge sharing but rather on 1D capacitance of the three regions with respect to their vertical depths. However, this is not true because without charge sharing, the drain and source depletion region should have more charges per width in accordance with Yau's sharing model and not fewer. Several articles have appeared in literature which deal with charge sharing and almost all the work neglected the effect of oxide thickness, incorrect prediction of SCE and the DIBL [47-49].

2.3.2 Toyabe's Polynomial Potential Model

This model assumes that the *2D* potential function occurs on a specific pattern of a cubic polynomial. The *x* is in the vertical direction with coefficient function of *y* in the lateral direction as shown in Figure 2.3.

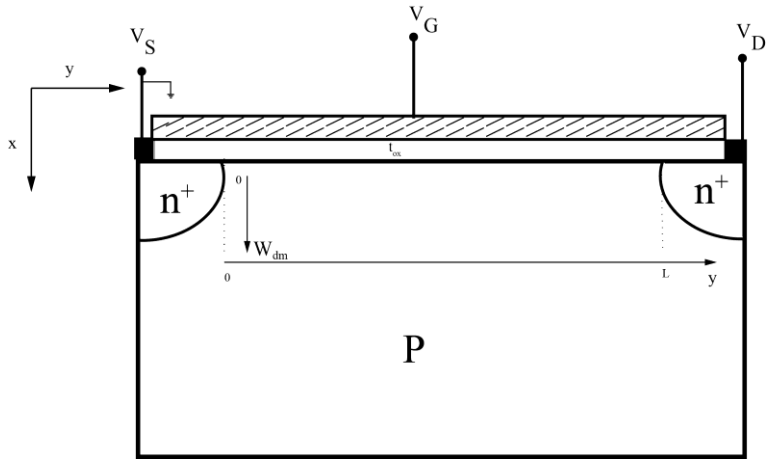


Figure 2.3. Biased MOSFET coordinates for polynomial potential model [50].

By applying the boundary conditions at the surface, where the vertical variable *x=0*, the *2D* Poisson equation is reduced to the *1D* differential equation. Hence, the surface potential is determined as a function of variable *y* from which the exponential dependence of the SCE model on channel length is derived with characteristic scaling length expressed as a function of vertical variable *x*.

In 1979, Toyabe and Asai [50] were the first to publish the polynomial potential model and researchers have emulated their method in the modelling of the surface potential of the short channel devices. However, they all ended up with a slight difference in the expression of the characteristic scaling length as a function of the depletion depth, W_{dm} and the gate oxide thickness. Toyabe and Asai's model is summarised as follows: The 2D

Poisson's equation of the electrostatic potential $\psi\ (x, y)$ of the gate's depletion region of nMOSFET with uniformly doped N_A biased at subthreshold is given as:

$$\frac{d^2\psi(x,y)}{dx^2}+\frac{d^2\psi(x,y)}{dy^2}=\frac{qN_A}{\varepsilon_{si}} \tag{2.18}$$

where x is the vertical direction with $x=0$ for the silicon surface and x=W_{dm} for maximum depletion depth at classical threshold condition of $2\phi_f$ and y is the lateral direction with $y=0$ for source region and $y=L$ for drain region. A polynomial approximation is formed to derive the equation for surface potential as:

$$\psi(x,y)=a_0(y)+a_1(y)x+a_2(y)x^2+a_3(y)x^3 \tag{2.19}$$

where the coefficients a_0, a_1, a_2, and a_4 are y-dependent. The boundary conditions in the vertical x directions are given as follows:

At $x=0$, assuming $V_{FB}=0$ for simplicity

$$V_{GS}-\psi(0,y)=\psi_{ox}=-t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{d\psi(0,y)}{dx} \tag{2.20a}$$

At $x=W_{dm}$

$$\begin{aligned}\psi(W_{dm},y)&=V_{GS}\\ \frac{d\psi(W_{dm},y)}{dx}&=0\end{aligned} \tag{2.20b}$$

The coefficients a_0, a_1, a_2 and a_4 are determined from equation (2.19) and (2.20) and the value of $d^2\psi_s/dx^2$ at the surface can be easily obtained. By assuming $x=0$, from equation (2.20), the authors obtained the surface potential using equation (2.18) as follows:

$$\psi(0,y)=a_0(y)=\psi_s \tag{2.21}$$

$$\frac{d^2\psi_S}{dx^2}-\left(\frac{2}{\gamma}\right)^2\psi_S=A \tag{2.22}$$

where the characteristic scale length is given as:

$$\gamma = \sqrt{\frac{2\varepsilon_{si} t_{ox}}{2\varepsilon_{ox} W_{dm} + 3\varepsilon_{si} t_{ox}}} W_{dm} \tag{2.23}$$

where A consists of qN_A/ε_{si}, V_{bi}, and V_{GS}-V_{FB}.

Considering the lateral direction for $y=0$ and $y=L$, the solution of the surface potential, $\psi_s(y)$ was obtained from equation (2.21), (2.22) given as:

$$\psi_S(y) = (V_{bi} - A_1)e^{\frac{-2y}{\gamma}} + (V_{bi} + V_{DS} - A_1)e^{\frac{-2(y-L)}{\gamma}} + A_1 \tag{2.24}$$

where V_{bi} is the built-in potential voltage and $A_1=-(\gamma/2)^2 A_0$. By assuming ($2L >> \gamma$), the authors obtained the minimum surface potential's value as given:

$$\psi_{s(\min)} = 2\sqrt{V_{bi} - A_1)(V_{bi} + V_{DS} - A1)}e^{2(y-L)/\gamma} \tag{2.25}$$

The minimum surface potential plays a major role in the derivations of subthreshold characteristics like the threshold voltage, subthreshold swing, and subthreshold currents. Their work gave a benchmark for the analytic understanding of the SCEs based on boundary conditions. They were the first to depict the drain and source fields effects in the channel in exponential form. This leads to the derivation of the so-called point of minimum surface potential which plays a major role in the derivation of the characteristic natural length as a function of gate oxide. It also plays an important role in the determination of the depletion width under the gate of short channel MOSFET.

However, the polynomial approximation methods used in equation (2.19) for their physical analysis do not satisfy the 2D Poisson equation for all of the channel region. The model is only valid at $x=0$. Also, the gate oxide region was not treated in 2D and the boundary conditions used were only valid for long channel devices because they assumed a constant vertical field in the x-direction of the oxide region ignoring the lateral effects from the y-direction.

2.3.3 Brews' Empirical Expression Model

In the 1980s, *Brews et al.* [51] proposed limited minimum channel length *(L_{min})* for a short channel device as a function of drain and source junction depth, oxide thickness, and drain and source depletion widths. His model was on the numerical fitting of 2-D computer aided simulation results. The proposed empirical relation was given as:

$$L_{\min} = A.\left[x_j t_{ox} (W_S + W_D)^{\frac{1}{2}} \right]^{\frac{1}{3}} \tag{2.26}$$

where A is the proportionality factor and x_j is the junction depth. All the units are in micrometers except A and t_{ox} which are in angstroms. W_S and W_D are the depletion region width for source and drain respectively in one dimension given as:

$$W_D = \sqrt{2L_B}\left[\beta(V_{DS} + V_{bi} + V_{GS})\right]^{\frac{1}{2}} \tag{2.27}$$

where L_B is the bulk debye length given as:

$$\left.\begin{aligned} L_B &= \left[\frac{\varepsilon_s}{\beta q N_A} \right]^{\frac{1}{2}} \\ \beta &= \left(\frac{KT}{q} \right)^{-1} \end{aligned}\right\} \tag{2.28}$$

where V_{DS} is the drain to source voltage, V_{bi} is the built-in voltage, and V_{GS} is the gate to source reverse voltage. For $V_{DS}=0$, $W_D=W_S$.

Brews et al. used a two-dimensional computer calculation to determine L_{min} while the A was fixed by fitting the minimum channel length to single power of *(1/3)* of the product. The A was assigned a value of *0.41* with the unit of the reciprocal of cube root of Armstrong $(A^0)^{-1/3}$.

The *Brew's et al.* empirical model fits the 2D numerical simulation and considers the effects of the gate oxide on the channel length and depletion width effect. His model also introduces advanced 2D numerical simulation of parameters. However, it is obvious that

the result is dimensionally inconsistent: the left-hand side (LHS) dimension is not equal to the right-hand side (RHS) dimension based on dimensional analysis [52]. Also, if all the linear parameters, x_j, t_{ox}, W_D, and W_S are scaled by *2*, L_{min} will be downscaled by $2^{4/3}$ and the general scaling principle is violated [53]. Another major shortcoming is that there is no analytical basis for the expression of SCE. Its model seems to be based on observations.

Another empirical model was proposed by *Ng et al.* [54] as an improved generalised guide for MOSFET scaling. The authors improved on the Brews et al. empirical model's drawback at the sub-half micro regime. However, the authors did not provide an analytical basis for their expression, hence their model is observation oriented.

2.4 Parabolic Approximation Potential (PPA) Model

It has become an established fact based on literature [55-59] that the most appropriate way to analytically model short channel devices is by solving the 2D Poisson's equations as a boundary valued problem. The boundary conditions eradicate the need for specification of the surface potential, but physically predict the description of it in consistency with the long channel models. Every MOSFET structure has its respective boundary condition that is applicable to its model.

2.4.1 Silicon on Insulator (SOI) MOFET

In 1989, Young [29] finalised the fundamental work by using a simplified parabolic approximation to solve the 2D Poisson equation described in equation (2.21) for an SOI MOSFET. He described the potential distribution in the vertical direction as shown in Figure 2.4. However, this model is based on a quadratic equation rather than Toyabe's Polynomial Potential Model approach. For convenience, the analysis is derived again as follows:

$$\psi(x, y) = c_0(y) + c_1(y)x + c_2(y)x^2 \tag{2.29}$$

where the coefficients c_o, c_1, and c_2, are functions of x only. Three boundary conditions were used on the assumption that the potential at the bottom interface is negligible due to buried oxide thickness.

a) At $x=0$

$$\psi(0, y) = \psi_f(y) = c_0(y) \tag{2.30}$$

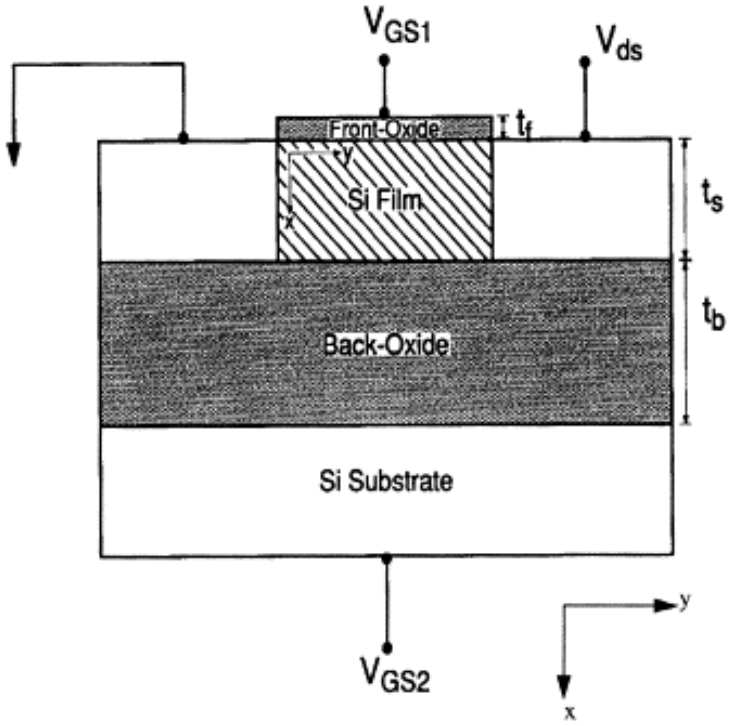


Figure 2.4. The 2D structural view of SOI MOSFTET [29].

b) The electric field at *x=0* is given by the difference in gate voltage and the oxide thickness as given:

$$\left.\frac{d\psi(x,y)}{dy}\right|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\psi_f(y) - V_{GS} - V_{FB}}{t_{ox}} = c_1(y) \tag{2.31}$$

c) The electric field at $x=t_{si}$ is approximately zero because of the structure of SO1 MOSFET and it is given:

$$\left.\begin{aligned}&\left.\frac{d\psi(x,y)}{dy}\right|_{x=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_{Sub} - V_{FB} - \psi_b(y)}{t_{ox}}\\ &c_1(y) + 2t_{si}c_2(y) = 0\end{aligned}\right\} \tag{2.32}$$

Their potential distribution was expressed in quadratic form using the three-boundary condition Equation (2.30), (2.31) and (2.32) as given:

$$\psi(x,y)=\psi_f(y)+\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\psi_f(y)-V_{GS}-V_{FB}}{t_{ox}}\right)\right)x - \left(\frac{\varepsilon_{ox}}{2t_{si}\varepsilon_{si}}\left(\frac{\psi_f(y)-V_{GS}-V_{FB}}{t_{ox}}\right)\right)x^2 \tag{2.34}$$

Also, in 1992, *Yan* [60] introduced a new concept, called natural length λ to the parabolic approximation model of SOI MOSFET. The natural length is a key parameter in suppressing SCEs and it is used to describe the surface potential channel of the structure. A simplified equation is obtained by substituting Equation (2.31) into Equation (2.19) and setting *y=0* leading to:

$$\frac{d^2\psi_f(y)}{dy^2}-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\psi_f(y)-V_{GS}-V_{FB}}{t_{si}t_{ox}}=\frac{qN_a}{\varepsilon_{si}} \tag{2.35}$$

Solving the equation (2.31) and (2.34), Yan obtained the equation (2.36).

$$\left.\begin{aligned}\lambda&=\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{si}t_{ox}}\\ \psi(y)&=\psi_f(y)-V_{GS}+\frac{qN_a}{\varepsilon_{si}}\lambda^2\end{aligned}\right\} \tag{2.36}$$

substituting equation (2.36) into (2.18), a simplified form of ID differential equation to describe the surface potential was obtained as:

$$\frac{d^2\psi(y)}{dy^2}-\frac{\psi(y)}{\lambda^2}=0 \tag{2.37}$$

To solve Equation (2.37), *Yan* used a new boundary condition along the channel as follows:

At *y=0*, at the source end, he obtained :

$$\psi(0)=V_{bi}-V_{GS}+\frac{qN_a}{\varepsilon_{si}}\lambda^2=\psi_s \tag{2.38}$$

At $y=L$, at the drain end he obtained:

$$\psi(L) = V_{DS} + V_{bi} - V_{GS} + \frac{qN_a}{\varepsilon_{si}}\lambda^2 = \psi_d \tag{2.39}$$

He obtained the channel potential using equation (2.37), (2.38) and (2.39) as given:

$$\left(\psi(y) = \frac{\psi_{so}\left(e^{\frac{L-y}{\lambda}} - e^{\frac{y-L}{\lambda}} \right) + \psi_{Do}\left(e^{\frac{y}{\lambda}} - e^{-\frac{L}{\lambda}} \right)}{e^{\left(\frac{L}{\lambda}\right)} - e^{\left(\frac{-L}{\lambda}\right)}} \right) \tag{2.40}$$

By differentiating the equation (2.40) at y= $y_{\min}$ and equating to zero, the minimum surface potential for the SOI MOSFET structure was obtained as:

$$\left.\begin{aligned} \psi_{\min} &= 2\sqrt{\psi_{so}\psi_D}\, e^{\left(-\frac{L}{2\lambda}\right)} \\ y_{\min} &= \frac{L}{2} + \frac{\lambda}{2} In\left(\frac{\psi_{so}}{\psi_D}\right) \end{aligned}\right\} \tag{2.41}$$

The obtained close-form expression can be employed in determining the behaviour of the SOI MOSFET devices at short channel. The model can be extended to other structures as explained in the next section.

2.4.2 Double-Gate (DG) MOSFET

Yan further extended the model to accommodate the potential distribution of a double gate MOSFET as shown in Figure 2.5. The natural length he introduced was a key parameter in suppressing the short channel effects. Based on his model, the short channel effect can be suppressed by reducing the oxide thickness, using high *k*-dielectric, and using a multi-gate structure to increase gate controllability [61].

Thus, for double gate, the device should be designed based on the scaling parameter and natural length as given by Yan:

$$\left.\begin{aligned} \alpha_1 &= \frac{L}{2\lambda} \\ \lambda &= \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox}} \end{aligned}\right\} \tag{2.42}$$

However, in 1993 *Suzuki* [62] used the model but with a contrary approach. He proposed that the punch-through current did not flow along the surface but through the centre in double gate MOSFET, making the natural length result slightly different from what Yan proposed for double gate. He proposed that the SCEs 'in double' were more pronounced than what Yan predicted.

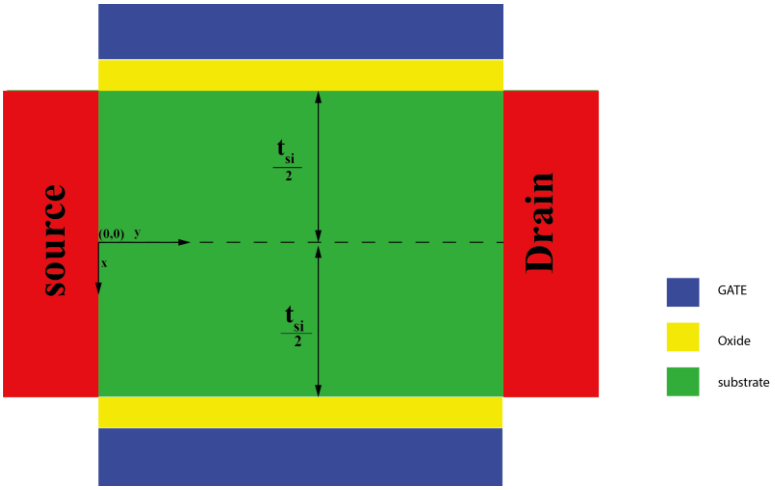


Figure 2.5. Schematic diagram of Double-Gate (DG) MOSFET.

However, the remaining analysis is the same as obtained by Yan. Hence, the natural length he obtained for double gate with a scaling parameter was as follows:

$$\left.\begin{aligned} \alpha_1 &= \frac{L}{2\lambda} \\ \lambda &= \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}}\right) t_{si} t_{ox}} \end{aligned}\right\} \tag{2.43}$$

2.4.3 Cylindrical Surrounding Gate (CSG) MOSFET

In 1997, *Plummer* [18] extended the PPA to Cylindrical Surrounding Gate (CSG) MOSFET in the radial direction as shown in Figure 2.6. The natural length described by Suzuki cannot be effectively utilised in the modelling of CSG MOSFET, since the surrounding-gate has a greater impact on the channel potential than double gate MOSFET [63].

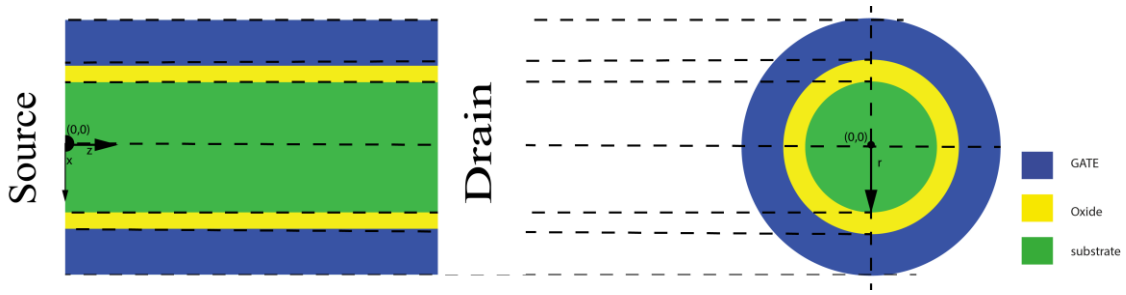


Figure 2.6. Cross section of CSG MOSFET

The Poisson equation for CSG MOSFET based on cylindrical coordinate was obtained by Plummer as follows:

$$\frac{d^2\psi(r,z)}{dz^2}+\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}\psi(r,z)\right)=\frac{qN_a}{\varepsilon_{si}} \tag{2.44}$$

Young's parabolic approximation model for CSG MOSFET was written as

$$\psi(r,z)=C_o(z)+C_1(z)r+C_2(z)r^2 \tag{2.45}$$

The boundary conditions for the CSG MOSFET structure were given based on Figure. 2.6 as follows:

a) The centre potential where the radius equals zero

$$\psi_c(z)=\psi(z,0)=C_0(z) \tag{2.46}$$

b) the electric field in the centre of the silicon pillar is zero

$$\left.\frac{d\psi(r,z)}{dr}\right|_{r=0}=C_1(z) \tag{2.47}$$

c) the electric field at the silicon-oxide interface was obtained as

$$\left.\frac{d\psi(r,z)}{dr}\right|_{r=\frac{t_{si}}{2}}=t_{si}C_2(z) \tag{2.48}$$

The potential distribution was determined by applying the equation (2.46), (2.47) and (2.48) to equation (2.44) and (2.45) in the same approach as Yan. Hence, Plummer obtained natural length for CSG MOSFET which is different from DG MOSFET and the scaling parameter as given:

$$\left.\begin{aligned}\alpha_1 &= \frac{L}{2\lambda} \\ \lambda &= \sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox}}\end{aligned}\right\} \tag{2.48}$$

There model shows a greater improvement in CSG MOSFET over double gate MOSFET by 30% reduction in the natural length. Several studies have been written based on this model for the threshold voltage analysis of double gate MOSFETs [64-67] and CSG MOSFETs [68, 69]. Many studies have been done based on PPA, on double gate and CSG MOSFET threshold voltage modelling using different gate-oxide material to suppress the SCEs as reported in [70-73]. PPA has attracted more research interest due to its simplified approach for solving the Poisson equation, especially in the area of junctionless MOSFETs [74, 75]. Recently, some authors have modelled the subthreshold swing and threshold voltage of the multi-gates MOSFETs using PPA with Effective Conduction Path (ECP) [76, 77]. However, in terms of accuracy and universality, the PPA has been shown to be inferior to EMA analysis [78] because of its estimated value of natural length, λ, in which the dormant subthreshold current occurs at the centre of the channel. Also, the 2D Poisson equation does not satisfy the channel potential inside the device. Furthermore, the use of 1D equation in the oxide region neglects the lateral field effects across the boundary which is also a major shortcoming of PPA in DG MOSFET and CSG MOSFET, except in special cases where some authors neglect the lateral effect (Junctionless MOSFET) and assume a quasi-2-D model [79, 80] or use it with ECP. The best approach in solving the 2D Poisson equation is by considering the oxide and silicon regions as a two-dimensional problem to yield physically consistent results, only possible if we can handle the different permittivity in the oxide and silicon in such a way that a 2D solutions can be obtained for both regions. This can be achieved by using the EMA model. Hence, the EMA model provides a solution to the 2D Poisson equation which accurately predicts the potential distribution in the entire device channel.

2.5 Evanescent-Mode Analysis (EMA)

In 1998, Frank et al. [28] solved the 2D Poisson equation by evanescent-mode analysis. This method became a generalised scaling length model for 2D effects in MOSFET. This model predicts the natural length, λ as a function of transverse confinement of the device

structure with respect to its boundary condition. This leads to an eigenvalue equation from which the characteristic scale length of the structural is obtained.

2.5.1 Modelling of MOSFET Structures

According to Frank et al. the potential function is divided into two parts, one in the oxide region, $\psi_{1(x,y)}$ and the other in the silicon region, $\psi_{2(x,y)}$ as shown in Figure 2.7. The authors represent each potential as a physical factor as shown in equation (2.49).

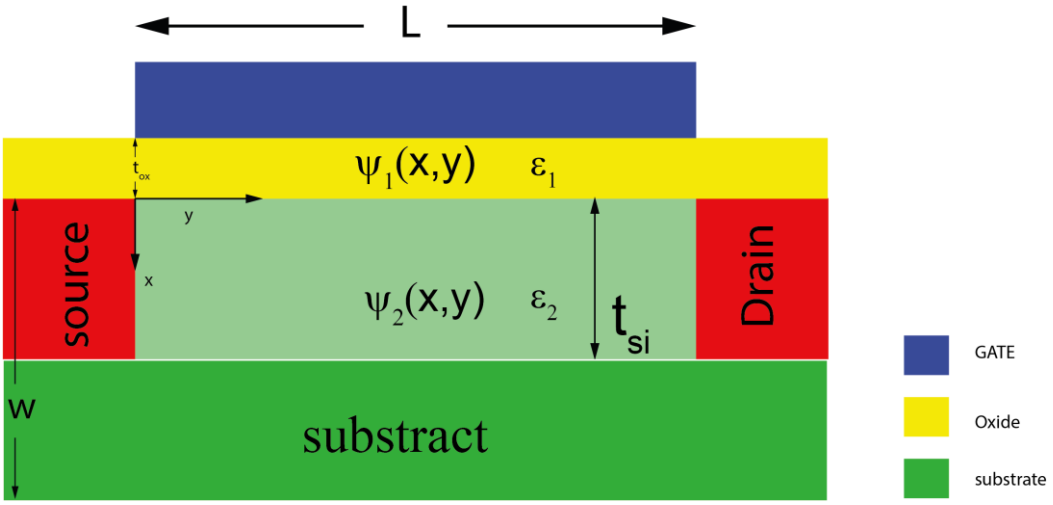


Figure 2.7. Schematic diagram of two-region MOSFET scale length model

$$\left.\begin{aligned}\psi_1(x,y) &= V_1(x)+U_{L1}(x,y)+U_{R1}(x,y)\\ \psi_2(x,y) &= V_2(x)+U_{L2}(x,y)+U_{R2}(x,y\end{aligned}\right\} \tag{2.49a}$$

The simplified form of equation is given as:

$$\psi(x,y) = \psi_{1D}(x)+\psi_{2D}(x,y) \tag{2.49b}$$

From equation (2.49), there is an inhomogeneous component, $V_1(x)$ and $V_2(x)$ which satisfies the 1D Poisson's equation at the top with the bottom boundary conditions and the dielectric boundary conditions like that in PPA model ($\psi_{1D}(x)$). The U_{L1}, U_{L2}, U_{R1}, and U_{R2} are the left and right homogenous components satisfying the drain and source boundary conditions. The *U'S* satisfies the 2D Laplace equation ($\psi_{2D}(x,y)$) for any λ_n and can be expressed in series along the *y*-axis and *x*-axis as a solution of *sinh(y)sin(x)* as given by Frank et al. as follows:

$$\left.\begin{aligned} U_{L1} &= \sum_{n=1}^{\infty}\left(\frac{b_{n1}\sinh(\lambda_n(L-y))}{\sinh(\lambda_n L)}\sin(\lambda_n(x+t_{ox}))\right) \\ U_{R1} &= \sum_{n=1}^{\infty}\left(\frac{c_{n1}\sinh(\lambda_n y))}{\sinh(\lambda_n L)}\sin(\lambda_n(x+t_{ox}))\right) \end{aligned}\right\} -t_{ox} \le x \le 0 \qquad (2.50)$$

$$\left.\begin{aligned} U_{L2} &= \sum_{n=1}^{\infty}\left(\frac{b_{n2}\sinh(\lambda_n(L-y))}{\sinh(\lambda_n L)}\sin(\lambda_n(x-W)+n\pi)\right) \\ U_{R2} &= \sum_{n=1}^{\infty}\left(\frac{c_{n2}\sinh(\lambda_n y))}{\sinh(\lambda_n L)}\sin(\lambda_n(x-W)+n\pi)\right) \end{aligned}\right\} 0 \le x \le W \qquad (2.51)$$

According the authors, at the top when $x=-t_{ox}$, U_{L1} and U_{R1} vanish. Also, when $x=w$, U_{L2} and U_{R2} vanish at the bottom. Considering the dielectric boundary condition at the oxide-silicon interface where $x=0$, the potential and electric field must be consistent if:

$$\left.\begin{aligned} U_{L1}(0,y) &= U_{L2}(0,y) \\ \varepsilon_{ox}\frac{dU_{L1}(0,y)}{dx} &= \varepsilon_{si}\frac{dU_{L2}(0,y)}{dx} \end{aligned}\right\} \qquad (2.52)$$

$$\left.\begin{aligned} U_{R1}(0,y) &= U_{R2}(0,y) \\ \varepsilon_{ox}\frac{dU_{R1}(0,y)}{dx} &= \varepsilon_{si}\frac{dU_{R2}(0,y)}{dx} \end{aligned}\right\} \qquad (2.53)$$

Evaluating the boundary condition on either the equation (2.50) or (2.51) respectively yields an equation for the eigenvalues, λ_n. which satisfy the Laplace equations as given:

$$\frac{1}{\varepsilon_{ox}}\tan(\lambda_n t_{ox}) + \frac{1}{\varepsilon_{si}}\tan(\lambda_n W) = 0 \qquad (2.54)$$

The authors assumed the lowest term of $n=1$ for the u series since the hyperbolic Sine function decays very fast at higher orders. They assumed channel length of $\lambda_1 L \gg 1$ for 1D gradual channel approximation. Their major contribution was introduction of a generalised form of solving the 2D Poisson equation using EMA. Also, they introduced the eigenvalue λ_n as a scaling parameter. However, the authors did not consider the threshold voltage and subthreshold swing in their analysis.

2.5.2 Double-Gate (DG) MOSFET and Cylindrical Surrounding Gate (CSG) MOSFET

In 2000, Monroe et al. [20] extended the EMA to DG MOSFET and CSG MOSFET. In their general expression, the three different layers of the device were based on the boundary condition that at the silicon-oxide interface the electric field must be continuous. Hence, the general scale length, λ for double gate was estimated as follows:

$$\frac{\varepsilon_{si}}{\varepsilon_{ox}}\tan\left(\frac{t_{si}}{2\lambda}\right).\tan\left(\frac{t_{ox}}{\lambda}\right)=1 \tag{2.55}$$

where, $\lambda=(t_{si}\varepsilon_{ox}+\varepsilon_{si}t_{ox})/\varepsilon_{ox}\pi)$ for thin oxide which is similar to Frank's analysis but differs from the Yan et al. model since λ does not tend zero when t_{ox} tends zero. This is because the silicon channel is non-zero. The 2-D Laplacian equation from equation (2.49b) was derived using Fourier's expansion mode in which each mode has its own characteristic decay length, as given [20]:

$$\psi_{2D}(x,y)=\sum_{n=1}^{\infty}A_n\,\mathrm{Cos}(\tfrac{ny}{\lambda})\left[B_n e^{\frac{nx}{\lambda}}+C_n e^{\frac{-nx}{\lambda}}\right] \tag{2.56}$$

By considering the lowest order of $n=1$ in accordance with Frank's analysis, the equation (2.56) can be rewritten as:

$$\psi_{2D}(x,y)=A_n\,\mathrm{Cos}(\tfrac{ny}{\lambda})\left[B_1 e^{\frac{nx}{\lambda}}+C_1 e^{\frac{-nx}{\lambda}}\right] \tag{2.57}$$

Monroe et al. extended their analysis to CSG MOSFET, where the channels are represented in terms of radius and the *z* axis, with the $\psi_{1D}(r)$ representing the long channel solution in the silicon and the $\psi_{2D}(x, y)$ denoting the Laplacian equation in the cylindrical coordinate. The Bessel function was introduced to the channel potential due to cylindrical coordinate as follows:

$$\psi(r, f, z) = \sum_{m=0}^{\infty}\sum_{n=1}^{\infty} J_m(rk_{mn})(A_{mn}\cos(mf) + B_{mn}\sin(mf))(C_{mn}e^{k_{mn}z} + D_{mn}e^{-k_{mn}z}) \qquad (2.58)$$

However, since the ϕ is independent of the channel, the general potential distribution for cylindrical coordinate can be written as:

$$\psi(r, z) = \sum_{n=0}^{\infty} J_n(r\lambda_n)(Ce^{k_n z} + D_n e^{-k_n z}) \qquad (2.59)$$

where for thin oxide,

$$\lambda = \frac{(D_{si} + 2\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox})}{4.810} \qquad (2.60)$$

After comparison, Monroe et al. concluded that the EMA model predicts 35% reduction in the natural length of CSG MOSFET when compared to double gate MOSFEETS, thereby making the cylindrical structure a better scaling device for nanotechnology. However, there is an omission of the threshold voltage and subthreshold swing characterisation in their analysis.

In 2002, Qiang et al. [14] used the EMA model to derive the general subthreshold swing for double gate MOSFET and introduced an effective conduction path effect (ECPE) to emphasise the position for the overall conduction in DG MOSFET. The channel potential is highlighted as in equation (2.11). The 1D Poisson equation is derived by the general approximation as given [14]:

$$\left.\begin{aligned} \psi_{1D}(y) &= \frac{V_0}{2}\left(\frac{y^2}{t^2_{si}} - \frac{1}{4} - \frac{1}{r}\right) \\ r &= \frac{C_{ox}}{C_{si}} \\ V_0 &= \frac{qN_A t^2_{si}}{\varepsilon_{si}} \end{aligned}\right\} \qquad (2.61)$$

The authors obtained the 2D Poisson equation based the boundary condition according to the structure in Figure 2.5 as given:

$$\psi_{2D}(x,y)=\frac{\sum_{1}\Gamma_1\cos(\frac{x}{\lambda_1})\left[V_1\left(\sinh(\frac{x}{\lambda_1})+\sinh(\frac{L-y}{\lambda_1})\right)+V_{DS}\left(\sinh(\frac{y}{\lambda_1})\right)\right]}{\sinh(\frac{L}{\lambda_1})} \tag{2.62}$$

The minimum surface potential was obtained by differentiating equation (2.62) with respect to *x* based on the boundary condition assumed by the authors as given [14]:

$$\psi_{\min}(x)=(V_{GS}-V_{FB})+\psi_{1D}(y)+2\Gamma_1\left(\cos(\frac{x}{\lambda_1})\sqrt{V_1(V_1+V_{DS})}e^{\frac{-L}{2\lambda_1}}\right) \tag{2.63}$$

They obtained the subthreshold swing as given:

$$SS=V_T ln10\left(\frac{dV_{GS}}{dI_{DS}}\right)^{-1}=\frac{V_T ln10}{\left(\frac{d\psi_{\min}(x)}{dV_{GS}}\right)}=\frac{V_T ln10}{1-2\Gamma_1\,\mathrm{Cos}(\frac{d_{eff}}{\lambda_1})\sqrt{V_1(V_1+V_{DS})}e^{\frac{-L}{2\lambda_1}}} \tag{2.64}$$

where $$\cos\left(\frac{d_{eff}}{\lambda_1}\right)=\frac{\int_{x=0}^{t_{si}/2}\cos(\frac{y}{\lambda_1})n_m(x)dx}{\int_{x=0}^{t_{si}/2}n_m(x)dx} \tag{2.65}$$

Qiang concluded in the ECPE he introduced, that overall conduction was between the centre and the surface and not in the centre as previously predicted in the PPA model [81] and by and with the help of the ECPE, he derived the subthreshold swing. The d_{eff} and $n_m(x)$ represent ECPE and Boltzmann distribution function respectively. However, he did not consider the threshold voltage in his analysis.

In 2005, *Kuang* [82] introduced the ECPE to the CSG MOSFET with the help of EMA model in order to determine the threshold voltage of the device structure via the minimum channel potential. The author observed that the threshold voltage was dependent on the scaling factor of $\lambda_1 L$. He extended the reference proposed by *Qiang* by redefining the ECPE as:

$$\cos\left(d_{eff}\lambda_1\right)=\frac{\int_{r=0}^{r=t_{si}/2}\cos(r\lambda_1)n_m(r)dr}{\int_{r=0}^{r=t_{si}/2}n_m(r)dr} \tag{2.66}$$

The 1D and 2D Poisson solution are similar to what Monroe obtained; however his eigenvalue derived to satisfy the silicon-oxide interface for CSG MOSFET was given as:

$$\lambda_n J_1(\lambda_n \tfrac{t_{si}}{2})=CJ_0(\lambda_n \tfrac{t_{si}}{2}) \tag{2.67}$$

The minimum surface potential with ECPE was used to obtain the threshold voltage since, with volume inversion [83], the current leakage at subthreshold would not be at the centre of the channel but rather between the silicon-oxide surface and the centre. However, the author did not consider the subthreshold swing of the CSG MOSFET.

In 2007, El Hamid et al. [84] presented an analytical model for the threshold voltage and subthreshold swing for CSG MOSFETS by solving the 2D Poisson equation with EMA model. The models were based on the minimum value of the channel potential. The subthreshold swing was based on Qiang's model while the threshold voltage was based on the minimum surface potential. Several articles have been written based on multi-gate MOSFET structure in which EMA has been used as a powerful tool in analysing the 2D Poisson equation [85-88]. However, CSDG MOSFET is yet to be fully exploited with EMA.

2.6 Cylindrical Surrounding Double-Gate (CSDG) MOSFET

Researchers have extensively studied the issues related to SCEs in SOI MOSFETS and multi-gate devices such as DG MOSFETS and CSG MOSFETS as previously reported. In 2011, Srivastava et al. [24] proposed a new multi-gate device known as CSDG MOSFET with application in the RF switching due to its low power consumption and high-speed radio frequency switching. However, the authors did not provide a detailed physics analysis supporting the proposed device structure.

In 2013, Srivastava et al. [89, 90], presented an explicit model of CSDG MOSFT based on a unified charge control model. The authors derived the channel current expression for

the structure with the terminal charges, transconductance, trans-capacitance and drain conductance as a function of the structural parameter and applied voltage. However, the authors did consider the subthreshold characteristics in their model and gave no analytical expression for the device threshold voltage. Also, only the 1D Poisson equation was solved in the derivation of channel potential. In 2014, Srivastava et. al. [91] analytically modelled the device characterization of the CSDG structure in which the internal and external drain currents were derived. The authors reviewed that CSDG MOSFET had a better energy efficiency when compared with CSG MOSFET in terms of volume inversion and gate controllability, although, their structure was slightly different from our proposed structure.

In 2015, *Verma et al.* [92] proposed a new CSDG structure in which they provided a physics-based analysis of CSDG MOSFETs at subthreshold characteristics to investigate the threshold voltage and subthreshold behavior. However, the authors assumed a non-hollow concentric cylindrical structure in their analysis which was different from that of *Srivastava et al.* [93]. In 2017, *Hong et al.* [94] presented a general 1D Poisson equation model for CSDG MOSFET, based on a special variable transformation method. However, the authors did not consider the subthreshold characteristics in their model. Also, in 2017, S. Bairagya and A. Chakraborty [95] proposed a model for the electrical characteristics of CSDG MOSFET in strong inversion region. In their approach, they solved the 1D Poisson equation in CSG MOSFET, and then extended the result to obtain the CSDG MOSFET model. However, they considered only the strong inversion region in their analysis.

Our proposed CSDG MOSFET has a hollow concentric cylindrical structure identical to *Hong et al's* design. A simple analytical channel potential model has been derived at subthreshold regime. The 2D Poisson equation is solved with the EMA as a boundary-valued problem to obtain the minimum surface potential. The minimum surface potential is further extended in the derivation of the threshold voltage model, subthreshold current and subthreshold swing of the device structure. Its performance is investigated with device parameters. Moreover, we neglected the quantum mechanical effects by assuming a minimum silicon film thickness of 5*nm* [96].

2.7 Chapter Summary

This chapter gives an overview of the background information on MOS structures, and the literature pertaining to different models was presented with a detailed explanation of their derivations. Their contributions and shortcomings were also highlighted in the multi-

gate structures like SOI MOSFTET, DG MOSFET and CSG MOSFET. Also, the related research work on CSDG MOSFET was also investigated.

CHAPTER 3

PROPOSED CSDG MOSFET SURFACE POTENTIAL MODEL

3.1 Introduction

This chapter describes the proposed CSDG MOSFET structure with a hollow concentric cylindrical structure. In the CSDG structure, the 2D Poisson equation is solved with EMA at subthreshold regime as a boundary-valued problem to obtain the minimum surface potential. The minimum surface potential obtained is varied along the channel length with other device parameters like gate oxide thickness and radii silicon film difference. Although in our analysis we have neglected the quantum mechanical effects by assuming a minimum radii silicon film thickness of 5 *nm* and oxide thickness of 2 *nm* [96], its performance shows perfect agreement with numerical simulation.

3.2 Structure of Proposed CSDG MOSFET

The CSDG MOSFET is a rotatory version of DG MOSFET and an advanced version of CSG MOSFET which was comprised of drain, source, gate oxide, gate and silicon substrate. It belongs to the GAA MOSFET family. The DG MOSFET has two gates (blue colour), the oxides (yellow colour), the drain/source (red colour) and a silicon substrate (P, green colour). When this DG MOSFET is rotated with respect to the reference point, the first gate (G_1) forms the internal radius ($r = a$) with a circular thin oxide to immune the effect of SCEs. The second gate (G_2) forms the external radius ($r = b$) with circular thin oxide, forming a hollow concentric cylinder [97, 98]. Between the oxides is the silicon substrate, while the extension forms the source and drain part of the cylinder as shown in Figure 3.1.

The internal and external gates of the CSDG MOSFET can be biased either separately or simultaneously to form separate inversion or volume inversion respectively. However, the simultaneous biasing of the CSDG MOSFET is usually preferred due to higher current drive (volume inversion), assuming the gate of an *n*-channel CSDG MOSFET is simultaneously positively biased. Below threshold voltage, the minority carrier electrons are attracted towards the oxide-silicon interface forming weak inversion. As the biasing

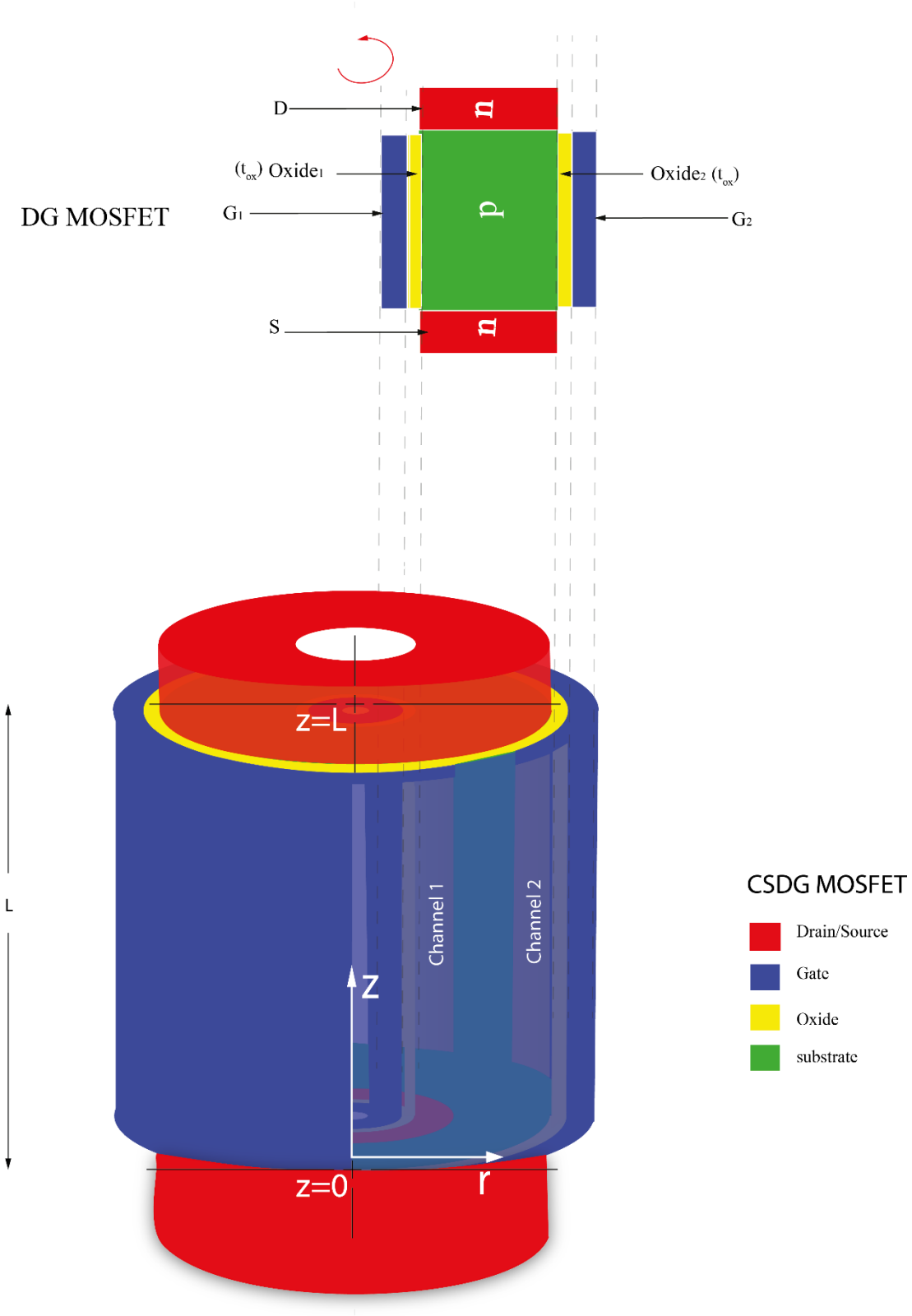


Figure 3.1. 3D View of proposed CSDG MOSFET in cylindrical structure.

voltage exceeds the threshold voltage, the onset of strong inversion occurs in CSDG MOSFET in a manner similar to the traditional MOSFET. Both biasing gates' voltage forms the internal and external channel of the device structure at subthreshold region. However, above threshold voltage the two channels contribute to higher current drive, known as volume inversion.

3.3 Evanescent Mode Analysis (EMA)

The best approach in solving the 2D Poisson equation is by considering the oxide and silicon regions in a two-dimensional analysis to produce physically consistent results. This can be achieved if the 2D Poisson equation is split into 1D Poisson for both the oxide and silicon region and 2D Laplace for the drain/source SCEs in the channel potential. For this reason, the EMA is used as shown in the flow chart in Figure 3.2. The EMA provides solution to the 2D Poisson equation and accurately predicts the potential in the entire device channel.

3.4 2D Poisson Equation and Boundary Condition

The 2D Poisson equation is solved using the EMA model, and the boundary conditions are obtained based on the structure of CSDG MOSFET with respect to the internal and external gate. Furthermore, the minimum surface potential for the internal and external gates is derived with the obtained boundary values.

3.4.1 2D Poisson Equation

In the subthreshold (weak inversion) regime, the 2D channel potential region, ψ (r, z), is determined from Poisson's cylindrical equation in the cylindrical coordinate system. The 3D structure can be analysed as 2D problem by assuming uniform channel doping and the independence of the channel potential on the angle θ as highlighted by [24]. The 2D Poisson equation is expressed as:

$$\frac{d^2\psi(r,z)}{dr^2}+\frac{1}{r}\frac{d^2\psi(r,z)}{dr^2}+\frac{d^2\psi(r,z)}{dz^2}=\frac{qN_A}{\varepsilon_{si}} \tag{3.1}$$

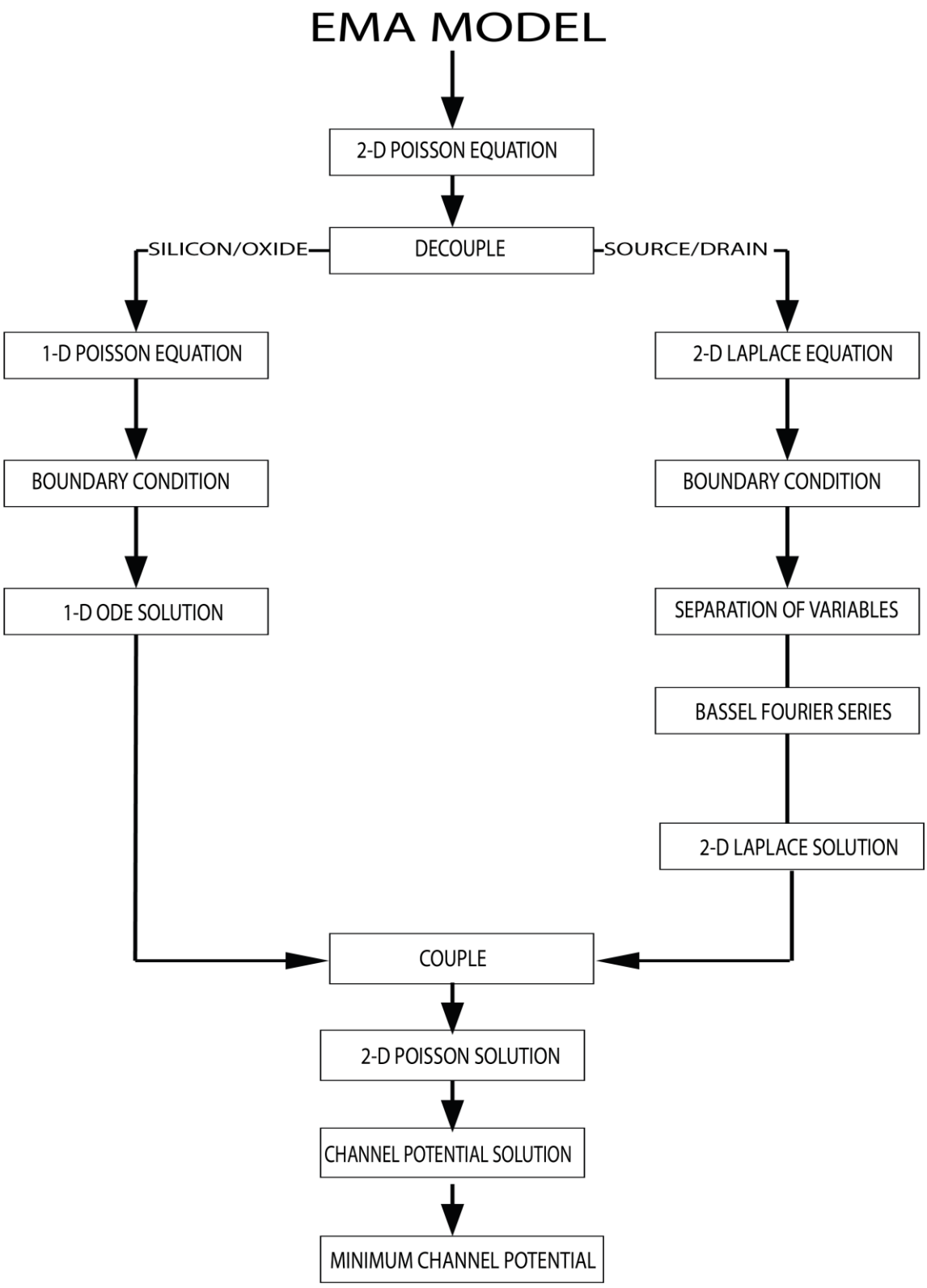


Figure 3.2. EMA model flow chart with PPA model.

The electrostatic potential, ψ (r, z) can be modeled by decoupling the 2D Poisson equation into two-part:

(i) 1D in the silicon region through the oxide thickness, and

(ii) 2D based on the source and drain impact on the channel [99].

Mathematically, the two parts are given as:

$$\psi(r,z) = \psi_{1D}(r) + \psi_{2D}(r,z) \tag{3.2}$$

where ψ_{1D} (r, z) is the channel potential approximation which satisfies 1D Poisson's equation under depletion approximation along the silicon thickness and it is given as:

$$\frac{d^2\psi_{1D}(r)}{dr^2} + \frac{1}{r}\frac{d\psi_{1D}(r)}{dr} = \frac{qN_a}{\varepsilon_{si}} \tag{3.3a}$$

This can be further simplified as:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}\psi_{1D}(r)\right) = \frac{qN_a}{\varepsilon_{si}} \tag{3.3b}$$

where N_A, ε_{si}, and q are the doping concentration permittivity in silicon and the electric charge respectively. Also, ψ_{2D} (r, z) accommodates the 2D variation of the channel potential at the oxide-silicon interface with zero charges which satisfies the 2D Laplace equation and describes the impact of the source and drain on the channel potential [100]:

$$\frac{d^2\psi_{2D}(r,z)}{dr^2} + \frac{1}{r}\frac{d^2\psi_{2D}(r,z)}{dr^2} + \frac{d^2\psi_{2D}(r,z)}{dz^2} = 0 \tag{3.4a}$$

This can be further simplified as:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}\psi_{2D}(r,z)\right) + \frac{d\psi_{2D}(r,z)}{dz^2} = 0 \tag{3.4b}$$

The equations (3.3) and (3.4) derived are solved analytically with the boundary conditions to obtain the potential distribution of the CSDG MOSFET structure. The boundary condition is derived in the next section.

3.4.2 Boundary Condition for the CSDG MOSFET

The boundary conditions for the Silicon body and gate oxide are used to solve the decoupled Poisson equation given in equation (3.3) and equation (3.4) with respect to the structures in Figure 3.3 and Figure 3.4.

Based on *Gauss's Law* [101], zero electric field must exist within the centre of the silicon substrate region indicated by the circular dash line known as the Gaussian surface in Figure 3.3(a) and Figure 3.4(a). The CSDG MOSFET is a rotary version of double-gate MOSFET as shown in Figure 3.3. It can also be treated as CSG MOSFET since the total electric field beyond $E = 0$ does not have effect on the enclosed surface within the circular dash line, and likewise the electric field at the hollow centre is zero assuming no charge exists in the centre [102]. Hence, the internal and the external radius of CSDG MOSFET can be treated separately as two CSG MOSFETs as shown in Figure 3.4.

In order to obtain the boundary condition for the CSDG MOSFET, Figure 3.3 and Figure 3.4 are considered as follows:

a) The potential at the gate surface for internal and external gates respectively are obtained as:

$$\left.\begin{aligned}\psi(r=a,z)&=\psi_a(a)\\ \psi(r=b,z)&=\psi_b(b)\end{aligned}\right\} \tag{3.5}$$

The potential at the centre of silicon for the internal and external gates respectively with respect to the hollow structure:

$$\left.\begin{aligned}\psi(r=0,z)=\psi(r=b,z)\big|_{r=a}&=\psi_{1D}(0)\\ \psi(r=0,z)=\psi(r=a,z)\big|_{r=b}&=\psi_{1D}(0)\end{aligned}\right\} \tag{3.6}$$

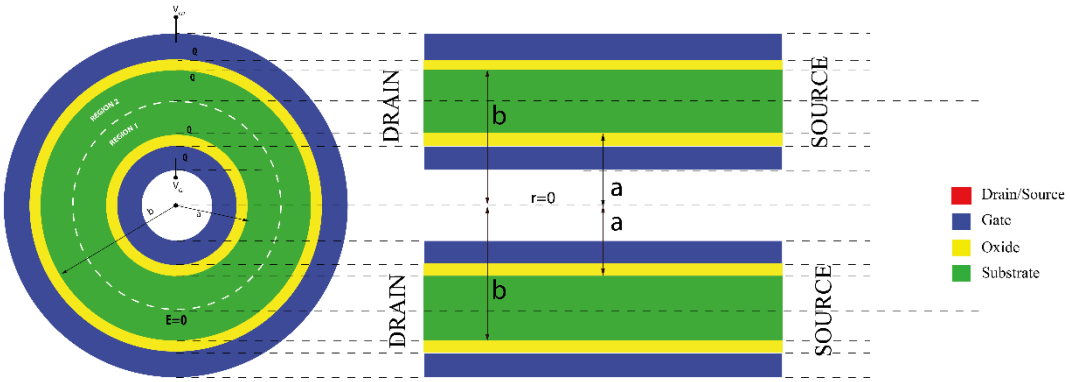


Figure 3.3. (a) CSDG MOSFET's circular cross-sectional view, and (b) it's views in DG MOSFET.

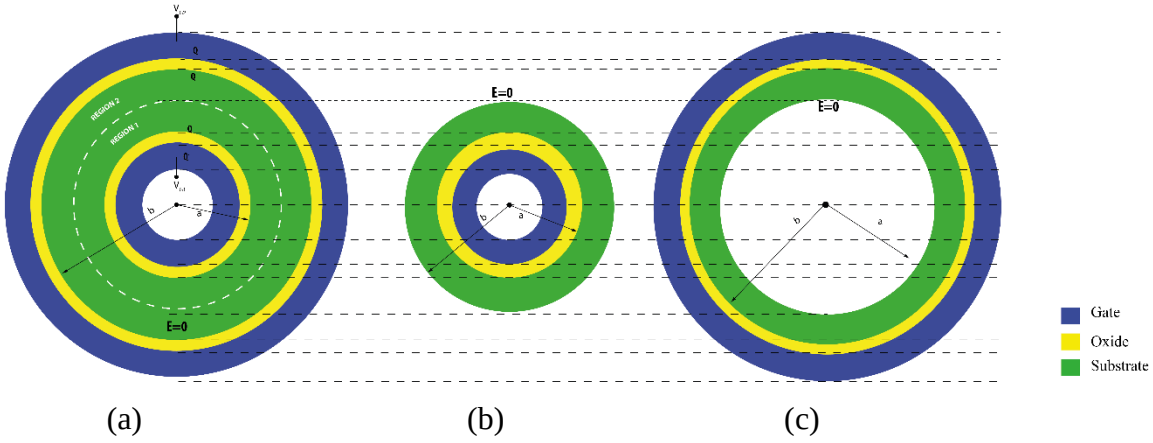


Figure 3.4. (a) CSDG MOSFET's cross section and (b) Internal circular cross-sectional view, and (c) External circular cross-sectional view.

b) The electric field at the channel centre for internal and external potential, respectively:

$$\left.\begin{aligned} \left.\frac{d\psi(r,z)}{dr}\right|_{r=0} &= \left.\frac{d\psi(r,z)}{dr}\right|_{r=b} = 0 \\ \left.\frac{d\psi(r,z)}{dr}\right|_{r=0} &= \left.\frac{d\psi(r,z)}{dr}\right|_{r=a} = 0 \end{aligned}\right\} \tag{3.7}$$

c) The electric field at the silicon-oxide interface for internal and external potential, respectively:

$$\left.\begin{aligned} C_{ox1}(V_{GS}-V_{FB}-\psi_{1D}(a,z)) &= \varepsilon_{si}\frac{d\psi(r,z)}{dr}|_{r=a} \\ C_{ox2}(V_{GS}-V_{FB}-\psi_{1D}(b,z)) &= \varepsilon_{si}\frac{d\psi(r,z)}{dr}|_{r=b} \end{aligned}\right\} \tag{3.8}$$

d) The internal Electrostatic Field boundary condition based on 1D Poisson equation:

$$\left.\begin{aligned} C_{ox1}(V_{GS}-V_{FB}-\psi_{1D}(a)) &= \varepsilon_{si}\frac{d\psi_{1D}(r)}{dr}|_{r=a} \\ C_{ox2}(V_{GS}-V_{FB}-\psi_{1D}(b)) &= \varepsilon_{si}\frac{d\psi_{1D}(r)}{dr}|_{r=0} = \varepsilon_{si}\frac{d\psi_{1D}(r)}{dr}|_{r=b}=0 \end{aligned}\right\} \tag{3.9}$$

where

$$C_{ox1} = \frac{\varepsilon_{ox}}{\left[a\ln\left(1+\frac{t_{ox}}{a}\right)\right]} \tag{3.10}$$

e) The external electrostatic field boundary condition based on 1D Poisson equation:

$$\left.\begin{aligned} C_{ox2}(V_{GS}-V_{FB}-\psi_{1D}(b)) &= \varepsilon_{si}\frac{d\psi_{1D}(r)}{dr}|_{r=b} \\ C_{ox1}(V_{GS}-V_{FB}-\psi_{1D}(a)) &= -\varepsilon_{si}\frac{d\psi_{1D}(r)}{dr}|_{r=a} = \varepsilon_{si}\frac{d\psi_{1D}(r)}{dr}|_{r=a}=0 \end{aligned}\right\} \tag{3.11}$$

where

$$C_{ox2} = \frac{\varepsilon_{ox}}{\left[b\ln\left(1+\frac{t_{ox}}{b}\right)\right]} \tag{3.12}$$

f) The boundary condition along the *Z*-direction can be used to solve the 2D Laplace equation at the source and drain end. Therefore, the potential at the source end where (*Z=0*) is given as:

$$\psi(r,0) = V_{bi} \tag{3.13a}$$

The potential at the drain end ($Z=L$) is given as:

$$\psi(r,L)=V_{bi}+V_{DS} \tag{3.13b}$$

$$\left.\begin{aligned} C_{ox1}(V_{GS}-V_{FB}-\psi_{1D}(0)) &= \varepsilon_{si}\frac{d\psi(r,z)}{dr}\Big|_{r=0} \\ C_{ox2}(V_{GS}-V_{FB}-\psi_{1D}(0)) &= \varepsilon_{si}\frac{d\psi(r,z)}{dr}\Big|_{r=0} \\ \psi_{1D}(0) &= \frac{\left(\psi_{1D}(a)+\psi_{1D}(b)\right)}{2} \end{aligned}\right\} \tag{3.14}$$

By substituting equation (3.13) into equation (3.2), we obtained:

$$\left.\begin{aligned} &\psi(r,0)=\psi_{1D}(r)+\psi_{2D}(r,0)=V_{bi} \\ &\Rightarrow \psi_{2D}(r,0)=V_{bi}-\psi_{1D}(r) \\ &\Rightarrow \psi_{2D}(r,L)=V_{bi}+V_{DS}-\psi_{1D}(r) \end{aligned}\right\} \tag{3.15}$$

where V_{bi}, $V_{FB,}$ V_{GS}, and V_{DS}, are the built-in potential, flat band voltage, gate-to-source voltage and drain voltage, respectively. C_{ox1} and C_{ox2} are internal gate and external gate oxide capacitance, respectively, and ε_{ox} and ε_{si} are the dielectric permittivity of the oxide and dielectric permittivity of silicon. Also, r varies to a when considering the internal potential and to b when considering the external potential in equation (3.9), (3.11) and (3.15) respectively.

3.5 1D Poisson Equation of the Internal and External Gate of CSDG MOSFET

This section presents the 1D Poisson equation with respect to the effects of the minority carriers due to the internal and external gates-induced electric field. Also, the structure is assumed to be affected by only the induced electric field from the gates, neglecting the source and drain effects on the channel.

3.5.1 Internal Gate

The 1D part of the equation can be solved with the given approximation along the oxide base on the boundary condition equation (3.9) and equation (3.11) are given as:

$$\psi_{1D}(a) = \frac{V_0}{4}\left[\frac{a^2}{t_{si}^{\ 2}} - \frac{1}{4} - \frac{1}{M}\right],\ V_0 = \frac{qN_A t_{si}^{\ 2}}{\varepsilon_{si}},\ M = \frac{C_{si}}{C_{ox1}},\ C_{si} = \frac{\varepsilon_{si}}{t_{si}}\Bigg\} \tag{3.16}$$

Hence, the 1D Poisson equations for the internal cylinder after mathematical transformation can be expressed based on the boundary condition equations (3.11), (3.14) and (3.16) as:

$$\psi_{1D}(a) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A a^2}{4\varepsilon_{si}} - \frac{qN_A t_{si}^{\ 2}}{16\varepsilon_{si}} - \frac{qN_A t_{si}^{\ 2} C_{si}}{4\varepsilon_{si} C_{ox1}} \tag{3.17}$$

3.5.2 External Gate

Similarly, the 1D Poisson equation for the external gate can be obtained using the boundary condition equations (3.9), (3.14), and (3.16) as:

$$\psi_{1D}(b) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t_{si}^{\ 2}}{16\varepsilon_{si}} - \frac{qN_A t_{si}^{\ 2} C_{si}}{4\varepsilon_{si} C_{ox2}} \tag{3.18}$$

where V_0, a, b and C_{si}, are the significant of induced field, the radius and silicon substrate capacitance, respectively.

3.6 2D Poisson Equation using Method of Separation of Variables

Authors have solved equation (3.4b) using the method of separation of variables based on literature [14, 103] by assuming:

$$\psi_{2D}(r,z) = G(r)H(z) \tag{3.19}$$

3.6.1 Internal gate of CSDG MOSFET (0 ≤ r ≤ a)

Replace equation (3.19) into equation (4b), we obtain:

$$\frac{1}{G(r)}\left(\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}G(r)\right)\right)+\frac{1}{H(z)}\left(\frac{dH(z)}{dz^2}\right)=0 \tag{3.20}$$

From equation (3.20), the *G(r)* depends on *r* only, while *H(z)* is independent of *r*. Also, when considering *H(z)*, the *G(r)* is independent of *z*. Hence, the equation has been successfully separated and the both parts are equal to a constant given as:

$$\frac{1}{H(z)}\left(\frac{dH(z)}{dz^2}\right)=\lambda^2 \tag{3.21}$$

and

$$\frac{1}{G(r)}\left(\frac{1}{r}\frac{d}{dr}\left(r\frac{d}{dr}G(r)\right)\right)=\text{-}\lambda^2 \tag{3.22}$$

where λ is the real value separation constant called the eigenvalue, which results in an exponential solution as shown in the general solution of equation (3.23):

$$H_1(z)=A_n e^{(z\lambda_n)}+B_n e^{(\text{-}z\lambda_n)} \tag{3.23}$$

Also, equation (3.22) leads to oscillatory (hyperbolic) solution as given in the parametric form of the general solution of Bessel equation as:

$$G(r)=CJ_0\left(\lambda r\right)+CY_0\left(\lambda r\right) \tag{3.24}$$

where the $J_o(\lambda r)$ and $Y_o(\lambda r)$ are forms of the fundamental set of solutions of the Bessel equation for non-integer, since $J_o(\lambda r)$ and $Y_o(\lambda r)$ are linearly independent. So, to have a finite potential, $C = 0$ in equation (3.24) to ignore the Neumann's function $Y_o(\lambda r)$ [104] which differs at the origin and hence:

$$G(r)=CJ_0\left(\lambda_0 r\right) \tag{3.25}$$

Therefore, the 2D Laplace equation can be obtained by substituting equation (3.23) and (3.25) into equation (3.19) as given:

$$\psi_{2D}(r,z) = G(r)H(z) = \sum_{n=0}^{\infty} [A_n e^{(z\lambda_n)} + B_n e^{(-z\lambda_n)}] J_0(r\lambda_n) \tag{3.26}$$

where λ_n is the eigenvalue which determines the extent of the electric field line penetrating the device. Since the same eigenvalue that appears in the exponential solutions, appears in the hyperbolic solution, so the more rapid the periodic variation the more the decay in accordance with [72]. Hence, the higher orders are ignored in the proposed model's analysis by equating $n = 0$ to obtain the 2D Laplacian equation for the internal gate as:

$$\psi_{2D}(r,z) = \left(A_0 e^{(z\lambda_0)} + B_0 e^{(-z\lambda_0)} \right) J_0(r\lambda_0) \tag{3.27}$$

where the coefficients A_o and B_o are obtained by using the device structure's boundary conditions in equation (3.13) and equation (3.15):

$$A_0 = \left(\frac{(V_{bi} + V_{DS} - \psi_{1D}(a)) - (V_{bi} - \psi_{1D}(a)) e^{-L\lambda_0}}{J_0(a\lambda_0)(e^{L\lambda} - e^{-L\lambda})} \right) \tag{3.28}$$

$$B_0 = \left(\frac{(V_{bi} - \psi_{1D}(a)) e^{L\lambda_0} - (V_{bi} + V_{DS} - \psi_{1D}(a))}{J_0(a\lambda_0)(e^{L\lambda} - e^{-L\lambda})} \right) \tag{3.29}$$

The eigenvalue must verify the Poisson equation at the internal silicon-insulator interfaces for continuity as:

$$\lambda_0 = \left\{ \frac{C_{ox1} J_0\left(\lambda_0 \frac{b-a}{2} \right)}{\varepsilon_{si} J_1\left(\lambda_0 \frac{b-a}{2} \right)} \right\} \tag{3.30}$$

The 2D Laplacian equation for potential distribution of the CSDG MOSFET structure with respect to the eigenvalue has been obtained for the internal gate. In the Laplacian equation, the source and drain electric field effects on the channel have been considered for accurate prediction of SCEs on the device structure.

3.6.2 External gate of CSDG MOSFET (0 ≤ r ≤ b)

The 2D Laplacian equation for the external gate can be obtained in similar order as:

$$\psi_{2D}(r,z) = \left(A_1 e^{(z\lambda_0)} + B_1 e^{(-z\lambda_0)}\right) J_0(r\lambda_0) \tag{3.31}$$

Also, the coefficients A_1 and B_1 can be obtained by using the boundary conditions in equation (3.13) and equation (3.15) as:

$$A_1 = \left(\frac{(V_{bi} + V_{DS} - \psi_{1D}(b)) - (V_{bi} - \psi_{1D}(b))e^{-L\lambda_0}}{J_0(b\lambda_{01})(e^{L\lambda_0} - e^{-L\lambda_0})} \right) \tag{3.32}$$

$$B_1 = \left(\frac{(V_{bi} - \psi_{1D}(b))e^{L\lambda_{01}} - (V_{bi} + V_{DS} - \psi_{1D}(b))}{J_0(b\lambda_{01})(e^{L\lambda} - e^{-L\lambda})} \right) \tag{3.33}$$

In similar manner, the eigenvalue must verify the Poisson equation at the external silicon-insulator interfaces as given:

$$\lambda_{01} = \frac{C_{ox2} J_0\left(\lambda_{01} \frac{b-a}{2}\right)}{\varepsilon_{si} J_1\left(\lambda_{01} \frac{b-a}{2}\right)} \tag{3.34}$$

where the Bessel series function of zero and first order are J_0 and J_1 respectively. By setting the first derivative of equation (3.27) and equation (3.31) at $z = 0$ along the z-axis and, also, by equating the channel potential to zero, the value of the minimum surface potential position at internal and external gates along the channel are obtained as:

$$z_{0\min} = \left(1 \big/ 2l_0 \right) \ln \left(\frac{B_0}{A_0} \right) \tag{3.35}$$

$$z_{01\min} = \left(1 \big/ 2\lambda_{01} \right) \ln \left(\frac{B_1}{A_1} \right) \tag{3.36}$$

The channel potential distribution for the internal and external gate of the CSDG MOSFET structure can be expressed through the equation (3.17), (3.27) and equation (3.18), (3.31) respectively as:

$$\begin{aligned} \psi(r,z) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A a^2}{4\varepsilon_{si}} - \frac{qN_A t^2{}_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox1}} \\ + \left(A_0 e^{(z\lambda_0)} + B_0 e^{(-z\lambda_0)} \right) J_0(a\lambda_0) \end{aligned} \tag{3.37}$$

$$\begin{aligned} \psi(r,z) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t^2{}_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox2}} \\ + \left(A_1 e^{(z\lambda_{01})} + B_1 e^{(-z\lambda_{01})} \right) J_0(b\lambda_{01}) \end{aligned} \tag{3.38}$$

By substituting equation (3.35) and equation (3.36) into equation (3.37) and equation (3.38), the values of minimum surface potential at the internal and external gates in equation (3.39) and equation (3.40), are respectively derived:

$$\begin{aligned} \psi_s(z_{\min}) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A a^2}{4\varepsilon_{si}} - \frac{qN_A t^2{}_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox1}} \\ + \left(A_0 e^{(z_{\min}\lambda_0)} + B_0 e^{(-z_{\min}\lambda_0)} \right) J_0(a\lambda_0) \end{aligned} \tag{3.39}$$

$$\begin{aligned} \psi_s(z_{\min}) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t^2{}_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox2}} \\ + \left(A_0 e^{(z_{\min}\lambda_0)} + B_0 e^{(-z_{\min}\lambda_0)} \right) J_0(b\lambda_{01}) \end{aligned} \tag{3.40}$$

Hence, the surface potential for the internal and external gates of the CSDG MOSFET has been derived. The analysis of the CSDG MOSFET is based on the derived equation.

3.7 Results and Discussions

In this section, the theoretical and numerical simulation results are presented using equation (3.39) and equation (3.40). The list of parameters used for the CSDG MOSFETs are given in Table 3.1.

Table 3.1 The device parameters for simulation.

Parameters	Values
Internal oxide thickness (t_{ox1})	2 nm to 5 nm
External oxide thickness (t_{ox2})	2 nm to 5 nm
Channel length (L)	30 nm
Internal radius (a)	3 nm - 6 nm
External radius (b)	13 nm
Silicon thickness (t_{si})=(b-a)	10 nm
Acceptors ion doping (N_A)	10^{17} cm^{-3}
Work of metal gates (Φ_{MS1}, Φ_{MS2})	4.8 eV
Drain to source voltage (V_{DS})	0.1 V
Band gap (E_g)	1.1ev
Band gap of silicon (E_{gs})	8.8 ev
Permittivity of silicon (ε_{si})	11.8 x 8.854 x 10^{-14} F/cm
Permittivity of gate oxide (ε_{ox})	3.9 x 8.854 x 10^{-14}F/cm
Temperature of operation (T)	300K
Intrinsic Carrier Concentration (n_i)	1.5 x $10^{10}$$cm^{-3}$

The surface potential distribution at both silicon-oxide interfaces are shown in Figure 3.5. It has been observed that at *0 V* and *0.5 V* drain to source bias voltage (V_{DS}), the internal and the external surface potential are approximately identical. However, the external gate shows better accuracy in comparison to device simulation than the internal gate. Also, as the drain voltage increases to *0.5 V*, both surface potentials increase towards the drain end, indicating mutual dependence on the threshold voltage. Inside the CSDG device structure, at V_{DS} value of *0 V* in the subthreshold regime, there exist a zero-built-in potential (ϕ_{bi}) between the *p-type* region (silicon substrate) and the *n-type* region (drain

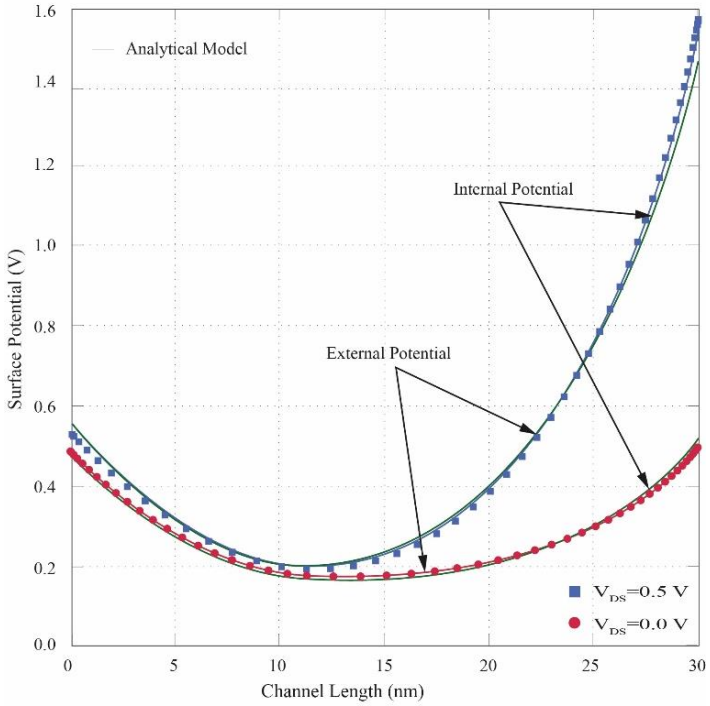


Figure 3.5. Potential distribution of the internal and external CSDG MOSFET by model and numerical simulation at 0 V and 0.5 V bias drain voltage.

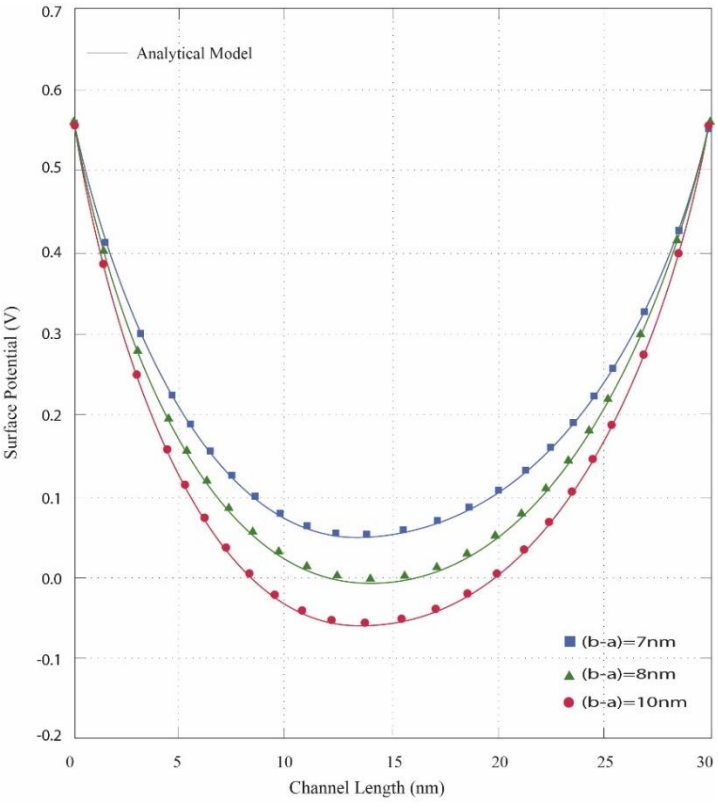


Figure 3.6. Potential distribution for the radii silicon film difference between the external and internal radius of CSDG MOSFET by model and the numerical simulation at different radii silicon film.

and source ends). The built-in potential is the barrier the minority carrier electrons must cross to create a weak inversion. As the V_{DS} value increases to *0.5 V*, the built-in potential at the drain end decreases by allowing more electron flow to the surface, thereby increasing the surface potential at the drain end of the two gates. Hence, the variation in drain-to-source voltage affects the threshold voltage. The model is in good agreement with the numeric simulation.

The potential distribution for the radii difference (silicon film thickness) between the external and the internal radius of the CSDG MOSFET is shown in Figure 3.6. It has been observed that the radii silicon film difference is indirectly proportional to the minimum surface potential. As the radii difference decreases, the minimum surface potential position increases. The controllability of the two gates (internal and external) over the channel increases. Therefore, smaller radii difference enhances the device for better immunity to SCEs. Inside the device, decrease in radii silicon film difference reduces the bulk potential and enhances greater control of the gates. The channel experiences stronger electric field from the two gates to shield the source- and drain-induced field effects. Also, the reduction in radii silicon film difference further immunises the device against radiation effects that are associated with electron-hole pairs in thicker silicon film. The results obtained are in perfect match with numerical simulation.

The surface potential behaviour at various oxide thicknesses is shown in Figure 3.7. The minimum surface potential position increases by pulling upward due to decrease in oxide thickness. This is because as the oxide thickness reduces, the more the vertical electric field penetrates the channel from the internal and external gates, thereby, increasing the gate control over the channel and the effect of threshold degradation is controlled. Hence, thin oxide is preferred to suppress SCEs in CSDG MOSFET. The numerical simulation results obtained are in good agreement with our model.

Practically, beyond 100 *nm* (long channel), at *zero* drain-to-source voltage, the effects from the drain and source on the channel are negligible because of the long channel. The electric field is practically vertical due to effects from the gate voltage only. Also, the channel potential is flattened due to negligible SCEs. However, as the channel length reduces, the gates, drain and source contribute to the electric field in the channel. Hence, the channel potential loses its flatness because of SCEs. The performance of the surface potential at a different channel length of CSDG MOSFET is shown in Figure 3.8. At channel length of 30 *nm*-100 *nm*, the minimum surface potential flattens. This shows

improvement of SCEs due to the coupling of the double surrounding gates. However, at channel length of less than 30 *nm*, the surface potential position rises upward gradually and loses its flatness due to the severe drain and source impacts of the much shorter channel length of less than 30 *nm*. The proposed model is in good agreement with numerical simulation.

The charges are very much inside the bulk of the device structure at *0 V*, and the electric field from the source and drain all contributes to the onset of weak inversion. However, as the gate voltages increase from *0 V* to *0.4 V*, the two gates of the CSDG MOSFETs gain greater control over the channel than the source and drain, provided that the drain voltage is constant. The potential distribution with various gates-to-source voltage at constant *zero* drain-to-source voltage is shown in Figure 3.9. As observed, there is an increase in the minimum surface potential as the gate-to-source voltage increases and flattens out at higher voltage, showing the better immunity to SCEs. As the gate voltage increases, minority carrier electrons migrate toward the surface of the gates of the CSDG MOSFET due to decrease in bulk potential. At the surface, the two gates gain better control of the channel and minimise SCEs. The numerical results obtained agree with the simulated results.

In the long channel, drain and source impacts on the channel are neglected. However, the impact of the drain on the channel becomes significant as the channel length reduces. The bulk potential barrier decreases as the drain voltage increases due to electric field effect on the channel. Moreover, the decrease in bulk potential causes faster rate of channel formation. Furthermore, the surface potential result at various drain-to-source voltage values with zero gate bias is shown in Figure 3.10; as the source-to-drain voltage increases, the surface potential increases at the drain end which indicates that the threshold voltage is inversely dependent on the drain bias. At *0.1 V*, in short channel CSDG MOSFET, the charges from the drain end contribute gradually to the surface channel potential. However, as the drain voltage increases to *0.4 V* irrespective of the *zero* biased gate voltage, the charge sharing from the drain end gains more kinetic energy to cross the bulk barrier potential to the silicon-oxide interface. Hence, the slope rises upward towards the drain end of the device structure as shown in Figure 3.10. The numerical results obtained agree with the results simulated.

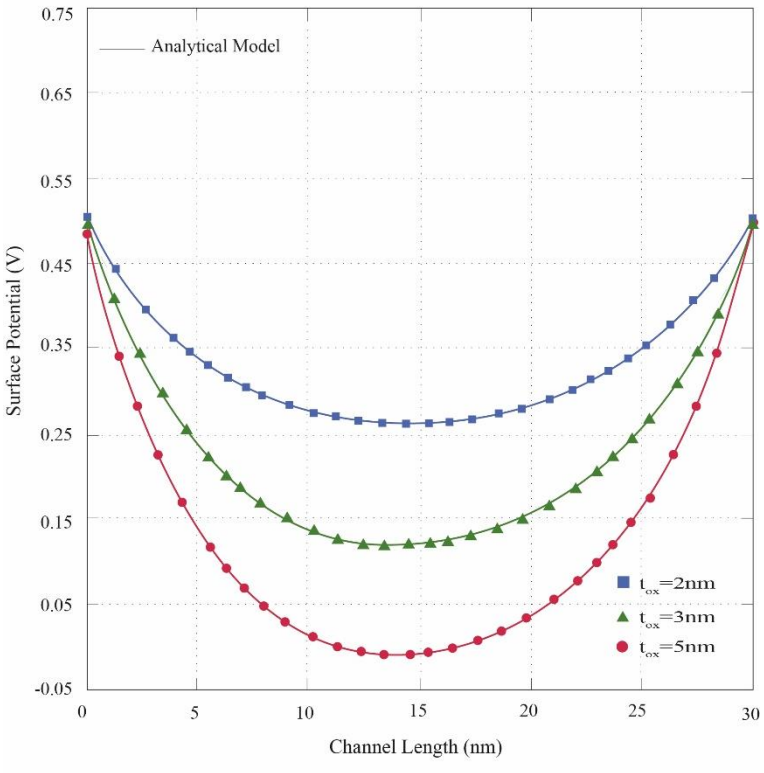


Figure 3.7. Potential distribution of the external gate surface of CSDG MOSFET along the channel length by model and numerical simulation at different oxide thickness

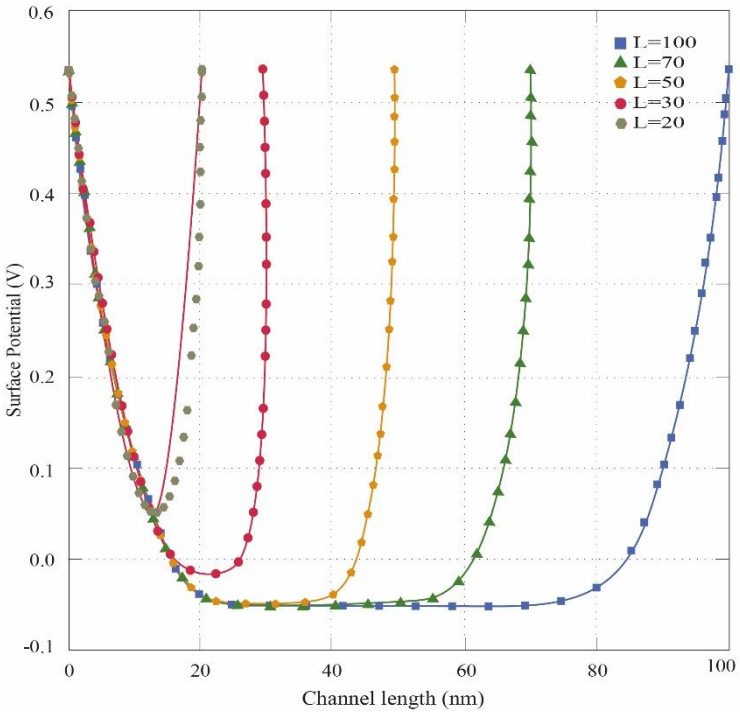


Figure 3.8. Potential distribution of the external surface of CSDG MOSFET along channel length by model and numerical simulation at different channel length.

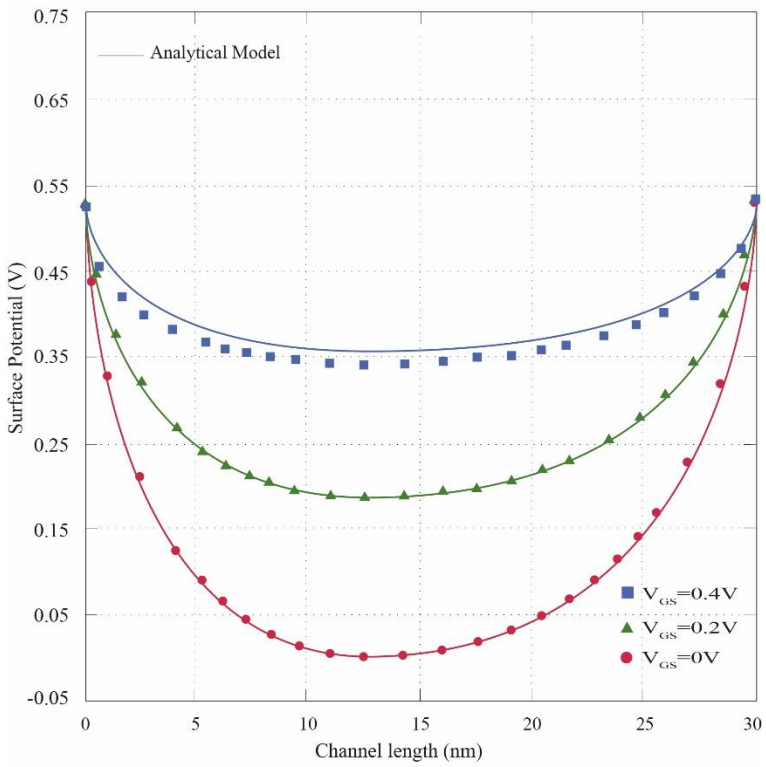


Figure 3.9. Potential distribution of the external surface of CSDG MOSFET along channel length by model and numerical simulation at different gate bias voltage

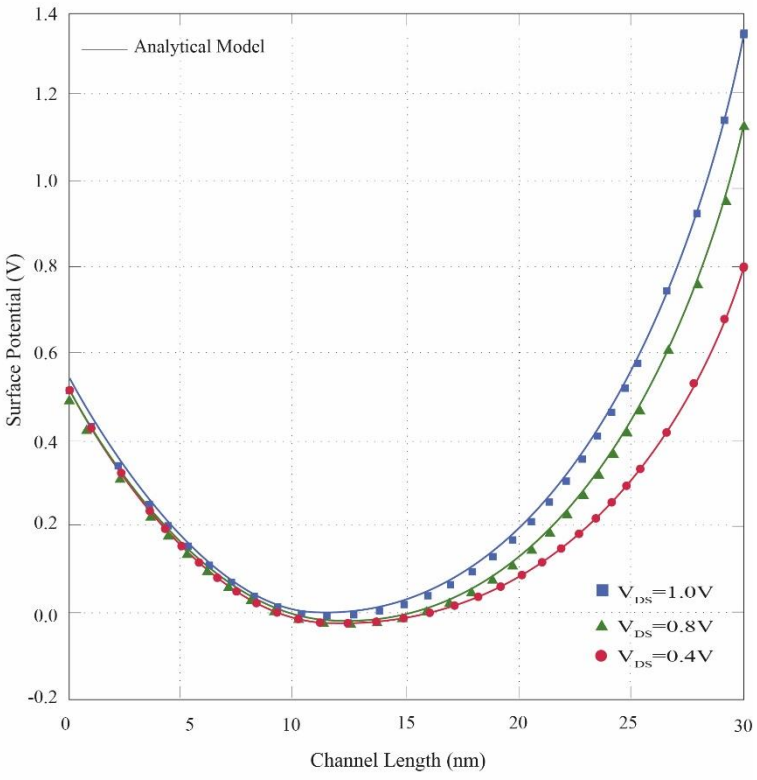


Figure 3.10. Potential distribution of the external surface of CSDG MOSFET along channel length by model and numerical simulation at different drain bias voltage

3.8 Chapter Summary

In this chapter, a simple channel potential model for CSDG MOSFET has been obtained by solving the 2D Poisson equation using the Evanescent-mode approach to observe the performance of the device. Also, the minimum surface potential model has been verified with different parameters to observe the performance of the device structure. It is obvious that as the channel length decreases up 30 *nm*, the device is immune to SCEs due to flatness of the minimum channel potential. Furthermore, the minimum surface potential model increases with decrease in gate oxide, thereby enhancing the gate's controllability over the channel. Moreover, as the radii silicon film difference reduces, gate control over the channel increases. The close-form expression of the model can be extended to model the threshold voltage, subthreshold current, and the subthreshold swing of the proposed CSDG MOSFET structure, as given in the next chapter. Good agreement is observed with numerical simulation.

CHAPTER-4

THRESHOLD VOLTAGE AND SUBTHRESHOLD CHARACTERISTICS

4.1 Introduction

The CSDG MOSFET as a switch requires an external source to be able to determine the *ON-OFF* nature of the device. Since MOSFETs are voltage-controlled devices, so a DC voltage is required to control the CSDG MOSFET. The DC voltage required for the *ON*-switching of the device when a reasonable drain current is achieved is known as the threshold voltage. Also, the subthreshold swing determines the device's behaviour by showing the effect of the change in external gate voltage on the subthreshold current. In an ideal MOSFET, the subthreshold current is zero when the applied gate voltage is less than threshold voltage. However, practically, such behaviour is never obtainable. The ideal subthreshold swing value at room temperature is 60 *mV/dec.*

4.2 Threshold Voltage of CSDG MOSFET

Threshold voltage is defined as the gate voltage at which the minimum surface potential is twice the Fermi potential, $2\phi_f$. So, the minimum surface potential from equation (3.39) and (3.40) is then simplified for both the internal and external gates of CSDG MOSFET by substituting the values of (Z_{min}) from equation (3.35) into equation (3.39) as given:

$$\psi_{s_{\min}}(z_{\min}) = \psi_{1D}(r) + 2J_0(\lambda_0 r)\sqrt{A_m B_m} = 2\phi_f \tag{4.1}$$

where

$$\phi_f = \frac{KT}{q} In\left(\frac{N_a}{n_i}\right)$$

where n_i is the intrinsic carrier concentration, $r=a$ for internal cylinder and $r=b$ for external cylinder, and $m=0$ and $m=1$ for the internal and external coefficient. The values of the parameters have been given in the Chapter 2. The threshold voltage for the proposed CSDG structure is given as

$$V_{TH_{Si}\_CSDG} = V_{TH_L\_CSDG} - V_{TH_i\_CSDG} \tag{4.2}$$

where V_{THL_CSDG} are the threshold voltage for the long channel, assuming the drain and source have no effect on the channel; V_{THi_CSDG} are the threshold voltage roll-off due to drain and source effects with respect to internal or external gate, and V_{THsi_CSDG} is the short channel threshold voltage for the internal and external gate surface potential.

Considering the long channel condition, the threshold voltage for the internal and external gates are given based on equation (3.17) and (3.18) as:

$$\psi_{1D1}(r) = 2\phi_f\Big|_{V_{GS}=V_{TH\_L}} \Rightarrow V_{TH\_L} = 2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A a^2}{4\varepsilon_{si}} + \frac{qN_A t^2{}_{si}}{16\varepsilon_{si}} + \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox1}} \tag{4.3}$$

$$V_{TH\_L} = 2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A b^2}{4\varepsilon_{si}} + \frac{qN_A t^2{}_{si}}{16\varepsilon_{si}} + \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox2}} \tag{4.4}$$

Considering the short channel condition, we included the drain and source effect in the model based on equation (4.1) as given:

$$\psi_{1D1}(r) + 2J_0(\lambda_{01} r)\sqrt{A_{01}B_{01}} = 2\phi_f \tag{4.5}$$

a) Considering the internal gate for the short channel model:

$$\begin{aligned}\psi_S(r = a, z_{\min})\big|_{V_{GS}=\psi_{1D}(a)=V_{th}} &= \psi_{1D}(a) \\ &+ \left(A_1 e^{(z_{\min}\lambda_0)} + B_1 e^{(-z_{\min}\lambda_0)}\right) J_0(a\lambda_0) = 2\phi_f\end{aligned} \tag{4.6}$$

From equation (4.1) we obtain:

$$V_{TH_{a}\_CSDG} + 2J_0(a\lambda_0)\sqrt{A_0 B_0} = 2\phi_f \tag{4.7}$$

The equation (4.7) can be expressed in polynomial form of second order as given:

$$X_1 V_{TH_{a\_CSDG}}^2 + X_2 V_{TH_{a\_CSDG}} + X_3 \tag{4.8}$$

where

$$X_1 = 4a_1 - a_2 - 2 \tag{4.8a}$$

$$X_2 = (2V_{bi} + V_{DS})(2 - 4a_1) \tag{4.8b}$$

$$X_3 = \left[4a_1 \left[\left(V_{bi} (V_{bi} + V_{DS}) \right) \right] - \left(V_{bi} + V_{DS} \right)^2 - 4\phi_f^2 a_2 - V_{DS}^{\ 2} \right] \tag{4.8c}$$

$$\left.\begin{aligned} a_1 &= 2J^2(a\lambda_0)\sinh(L\lambda_0) \\ a_2 &= 4J^2(a\lambda_0)\sinh^2(L\lambda_0) \end{aligned}\right\} \tag{4.8d}$$

Therefore, the threshold voltage roll-off for the internal gate surface potential due to the short channel effect is given as:

$$V_{TH_{a\_CSDG}} = \frac{-X_2 + \sqrt{X_2^{\ 2} - 4X_1X_3}}{2X_1} \tag{4.9}$$

Hence the closed-form expression of the short channel threshold voltage for the internal gate of CSDG MOSFET is given, with the practical assumption of $\lambda_n L >> 1$ [60]:

$$\begin{aligned} V_{TH_{Sa\_CSDG}} = &\left(2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A a^2}{4\varepsilon_{si}} + \frac{qN_A t^2_{si}}{16\varepsilon_{si}} + \frac{qN_A t_{si}^{\ 2} C_{si}}{4\varepsilon_{si} C_{ox1}} \right) \\ &- \left(\frac{-X_2 + \sqrt{X_2^{\ 2} - 4X_1X_3}}{2X_1} \right) \end{aligned} \tag{4.10}$$

b) Considering the external gate for the short channel model:

$$V_{TH_{b\_CSDG}} + 2J_0(b\lambda_0)\sqrt{A_0B_0} = 2\phi_f \tag{4.11}$$

The equation (4.7) can be expressed as a quadratic equation as given:

$$Y_1 V_{TH_{b\_CSDG}}^2 + Y_2 V_{TH_{TH_{b\_CSDG}}} + Y_3 \tag{4.12}$$

where

$$Y_1 = 4b_1 - b_2 - 2 \tag{4.12a}$$

$$Y_2 = (2V_{bi} + V_{DS})(2 - 4b_1) \tag{4.12b}$$

$$Y_3 = \left[4b_1 \left[(V_{bi}(V_{bi} + V_{DS})) \right] - (V_{bi} + V_{DS})^2 - 4\phi_f^2 b_2 - {V_{DS}}^2 \right] \tag{4.12c}$$

$$\left.\begin{aligned} b_1 &= 2{J_0}^2(b\lambda_0)\sinh(L\lambda_0) \\ b_2 &= 4{J_0}^2(b\lambda_0)\sinh^2(L\lambda_0) \end{aligned}\right\} \tag{4.12d}$$

Therefore, the threshold voltage roll-off for the external gate surface potential due the short channel effect is given as:

$$V_{TH_b} = \frac{-Y_2 + \sqrt{{Y_2}^2 - 4Y_1 Y_3}}{2Y_1} \tag{4.13}$$

Likewise, the closed-form expression of the short channel threshold voltage for the external gate of CSDG MOSFET is given as:

$$\begin{aligned} V_{TH_{Sb\_CSDG}} = &\left(2\phi_f + V_{FB} + \psi_{1D}(0) - \frac{qN_A b^2}{4\varepsilon_{si}} + \frac{qN_A {t^2}_{si}}{16\varepsilon_{si}} + \frac{qN_A {t_{si}}^2 C_{si}}{4\varepsilon_{si} C_{ox\text{-}b}} \right) \\ &- \left(\frac{-Y_2 + \sqrt{{Y_2}^2 - 4Y_1 Y_3}}{2Y_1} \right) \end{aligned} \tag{4.14}$$

Therefore, the threshold voltage of the short channel CSDG MOSFET can be determined through the internal gate as shown in equation (4.10) or through the external gate as shown in equation (4.14) respectively.

4.3 Subthreshold Current

The subthreshold current flows from source to drain along the channel length through diffusion mechanism. Hence, the subthreshold current is obtained by integration with respect to the circular area as given [8]:

$$\left.\begin{aligned} I_{Sub} &= q\pi t_{si} D_n \frac{n_m(r,z)}{L} \left[1 - e^{\frac{-V_{DS}}{V_T}} \right] \\ D_n &= \mu V_T \end{aligned}\right\} \tag{4.15}$$

where n_m is known as the electron density at subthreshold regime in relation to classical Boltzmann's equation. It is given in equation (4.16).

$$n_m(r,z) = \frac{n_i^2}{N_A} e^{\left(\frac{\psi(r,z)}{V_T}\right)} \tag{4.16}$$

D_n, V_T, and n_i are the diffusion constant, thermal voltage and intrinsic concentration respectively. By using the equation (4.15), assuming the subthreshold current occurs at the virtual cathode ($z=z_{min}$), the subthreshold current of CSDG MOSFT (I_{CSDG_sub}) is obtained as:

$$I_{CSDG\_sub} = I_a + I_b \tag{4.17}$$

$$I_{CSDG\_sub} = \frac{q\pi t_{si} D_n n_m(r, z_{\min})\left[1 - e^{\frac{-V_{DS}}{V_T}}\right]}{\int_0^l M^{-1}(z)dz} + \frac{q\pi t_{si} D_n n_m(r, z_{\min})\left[1 - e^{\frac{-V_{DS}}{V_T}}\right]}{\int_0^l N^{-1}(z)dz} \tag{4.18}$$

where

$$\left.\begin{aligned} M(z) &= \frac{qn_i^2}{N_A}\int_{\frac{t_{si}}{2}}^{a} f_a(r)dr \\ N(z) &= \frac{qn_i^2}{N_A}\int_{a}^{b} f_b(r)dr \end{aligned}\right\} \tag{4.18a}$$

$$f(r) = e^{\frac{q\psi(r,z_{\min})}{KT}} \tag{4.18b}$$

where $M(z)$ and $N(z)$ can be obtained by integrating the indefinite $f_a(r)$ and $f_b(r)$ through the trapezoidal rule of numerical approach as given [105]:

$$\left.\begin{aligned} M &= \frac{qn_i^2}{N_A} G_a\left[\left(e^{\frac{q\psi_{\min}}{kT}}\right) + \left(\sum_{k=1}^{n-1}\left(e^{\frac{\psi(G_a k, z_{\min})}{KT}}\right) + e^{\frac{q\psi(0,z_{\min})}{KT}}\right)\right] \\ G_a &= \frac{a}{2n} \end{aligned}\right\} \tag{4.19a}$$

$$\left.\begin{aligned} N &= \frac{qn_i^{\,2}}{N_A} G_b \left[\left(e^{\frac{q\psi_{\min}}{kT}} \right) + \left(\sum_{k=1}^{n-1} \left(e^{\frac{\psi(G_b k, z_{0\min})}{KT}} \right) + e^{\frac{q\psi(0, z_{0\min})}{KT}} \right) \right] \\ G_b &= \frac{b}{2n} \end{aligned} \right\} \qquad (4.19b)$$

By equating the partition number, *n=1* to equation (4.19a) and (4.19b) the subthreshold current for CSDG MOSFET can be obtained in equation (4.18).

4.4 Subthreshold Swing

Subthreshold swing (SS) is defined, according to [106], as the change in gate bias voltage required for a change of one decade of subthreshold drain current. Since subthreshold swing is an important device parameter to represent the switching characteristics of the MOS device, its evaluation is necessary, and it is given as [107]:

$$SS = \left[\frac{d \log I_{CSDG\_sub}}{dV_{GS}} \right]^{-1} \qquad (4.20)$$

By substituting equation (4.18) into equation (4.20), the subthreshold swing can be calculated. However, the subthreshold swing is very difficult to obtain using the subthreshold current, due to its complicated dependency on the minimum radius *(r_{min})* of the gate voltage and the numerical integration involved. In a simpler approach [84], the subthreshold current can be related to the minimum surface potential, *ψ_{smin} (r, z_{min})* through the electron concentration at the virtual cathode. This is because, at subthreshold operation, the subthreshold current is dominated by a diffusion process. This leads to a probability of mobile electrons surmounting the source end of the energy barrier. Thus, it can be assumed that the subthreshold current is proportional to the carrier concentration at the virtual cathode, *η_{min} (r, z_{min})* given as [106]:

$$I_{sub} \;\alpha\; n_{\min}(r, z_{\min}) \;\alpha\; e^{\left(\frac{\psi_{\min}}{V_T}\right)} \qquad (4.21)$$

Since, the electron density follows Boltzmann distribution according [108] we can express the SS by substituting equation (4.21) in equation (4.20) as given:

$$SS_{CSDG} = \frac{V_T In10}{\left(\frac{d\psi_{s_{\min}}(r, z_{\min})}{dV_{GS}} \right)} \tag{4.22}$$

where $V_T = \frac{KT}{q}$, and from equation (3.2), the minimum surface potential can be obtained as:

$$\psi(r, z_{\min}) = \psi(r) + \psi(r, z_{\min}) = \psi(r) + 2J_0(r\lambda)\sqrt{A_1 B_1} \tag{4.23}$$

$$\psi_{s_{\min}}(r, Z_{\min}) = (V_{GS} - V_{FB}) - \psi_{1D}(0) + \frac{qN_A b^2}{4\varepsilon_{si}} - \frac{qN_A t^2_{si}}{16\varepsilon_{si}} - \frac{qN_A t_{si}{}^2 C_{si}}{4\varepsilon_{si} C_{ox2}} + 2J_0(b\lambda_0)\sqrt{A_1 B_1} \tag{4.24}$$

$$\frac{d\psi_{s_{\min}}(r, z_{\min})}{dV_{GS}} = \frac{d\psi(r)}{dV_{GS}} + \frac{d\psi(r, z_{\min})}{dV_{GS}} \tag{4.25}$$

Therefore, the subthreshold swing can be obtained using equations (4.22), (4.24) and equation (4.25). The simulation of the close-form expression obtained, and the numerical results are shown in the next section.

4.5 Results and Discussions

In this section, the theoretical and numerical simulation results are presented using equations (4.10), (4.14), (4.18), and equation (4.24) and using the device parameters from table 3.1.

The threshold voltage of the internal and external gate CSDG MOSFET with variation of channel length is shown in Figure 4.1. It has been observed that the decrease in channel length causes a corresponding rapid decrease in the threshold voltage. The phenomenon is called the threshold roll-off which can be determined with either the internal gate or external gate model. Although the threshold voltage between the internal and external gates is almost the same, the external gate has slightly higher threshold voltage than the internal gate due to higher minimum surface potential as shown in Figure 4.1. The external gate is in perfect match with the numerical simulation.

The thin gate oxide of the internal and external structure of the CSDG MOSFET enables the dominance of the vertical electrical fields over the lateral electric field resulting from the drain and source ends. This enables the two gates to have better control of the channels created within the structure. Furthermore, the dominance of the vertical electric field will result in less leakage of current when the device is turned-*OFF*. The variation of threshold voltage with channel length at different oxide thicknesses is shown in Figure 4.2. It is clearly observed that the decrease in channel length results in the decrease in threshold voltage which affects the device performance. We optimised the threshold voltage with different oxide thicknesses. The threshold voltage increases with decrease in gate oxide, hence thin gate oxide tends to provide better gate controllability than the thicker oxide. Also, thin gate oxide reduces SCEs in CSDG MOSFETs. The result is in good agreement with the numerical simulation of the proposed structure.

Also, the thinner radii silicon film difference of the CSDG MOSFET structure enhances the internal and external gate control of the channel carriers over the drain and source ends. The reduction in radii difference further reduces the drain and source sizes, and their impact on the channel is significantly reduced. Hence, the gates have better control of the channel carriers. The variation of threshold voltage with channel length at different radii silicon film thickness is shown in Figure 4.3. It is observed that as the silicon film thickness decreases, the threshold voltage of CSDG MOSFET increases because the drain end loses control of the channel. As a result, the thin silicon film provides better gate controllability leading to low threshold voltage degradation and better suppression of SCEs. The result matches the numerical simulation of the proposed structure.

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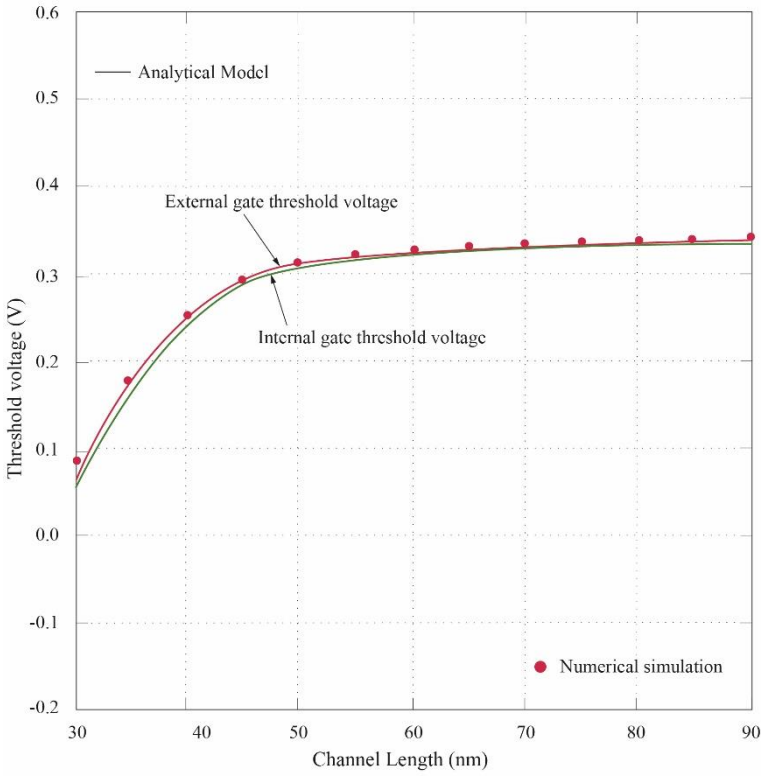


Figure 4.1. Comparison of the internal and external gate threshold voltage versus channel length of CSDG MOSFET by numerical simulation and model.

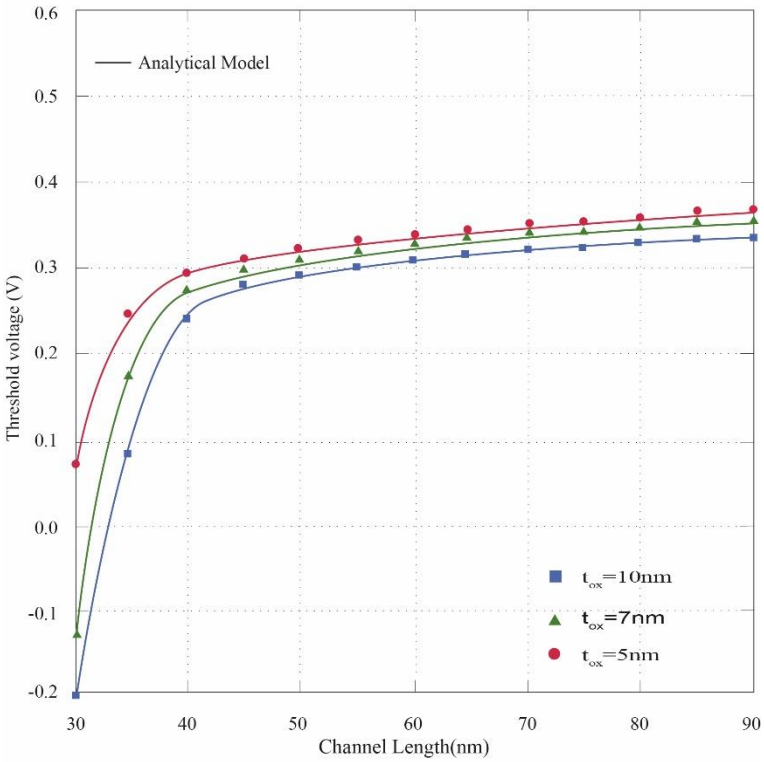


Figure 4.2. Threshold voltage of the external gate of CSDG MOSFET versus channel length by numerical simulation and model with different gate oxide thickness.

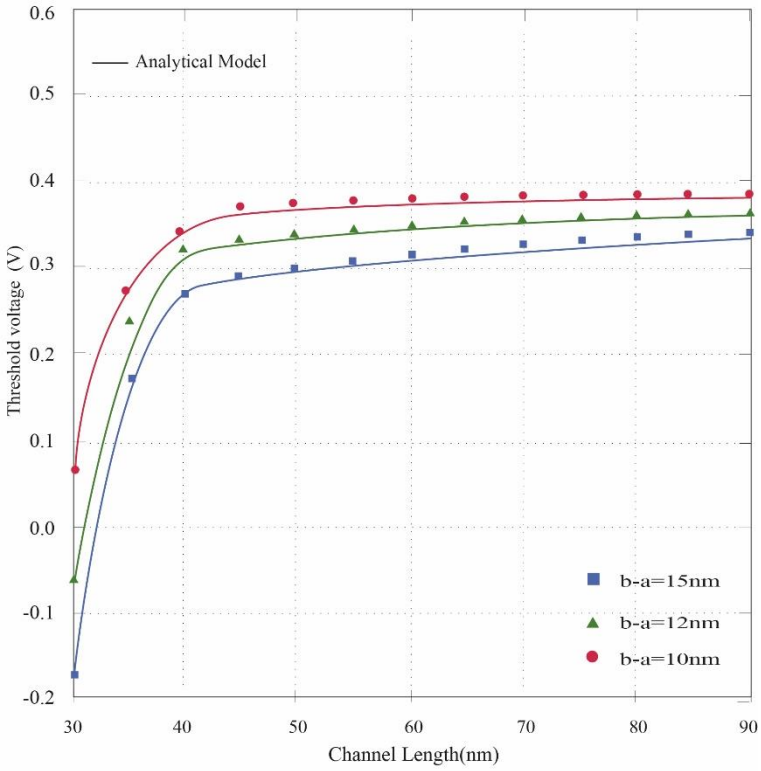


Figure 4.3. Threshold voltage of the external gate of CSDG MOSFET versus channel length by numerical simulation and model with different radii silicon film difference.

CSDG MOSFETs provide higher drain current due to the coupled internal and external gates. These gates increase the average electric field of the structure. This enables rapid acceleration of carriers at the interface towards the drain terminal, resulting in the enhancement of the carrier transportation efficiency for the proposed structure. However, an increase in the drain current causes a slight increase in the subthreshold leakage current, which needs to be minimised at less than 30 *nm* gate length. The subthreshold current versus the gate voltage with a different variation in channel length is shown in Figure 4.4. The channel length is varied from 60 *nm* to 20 *nm*. It is clearly observed that the subthreshold current increases as the channel length decreases with an upward shift. This implies lesser control of the gate over the channel at lower channel length resulting in more current leakage. It should be noted that the model is considered at the subthreshold regime. The slight deviation of the numerical simulation from model towards *0.5 V* of the gate voltage shows the inversion onset phase. The model matches the numerical simulation for the proposed structure within the subthreshold regime.

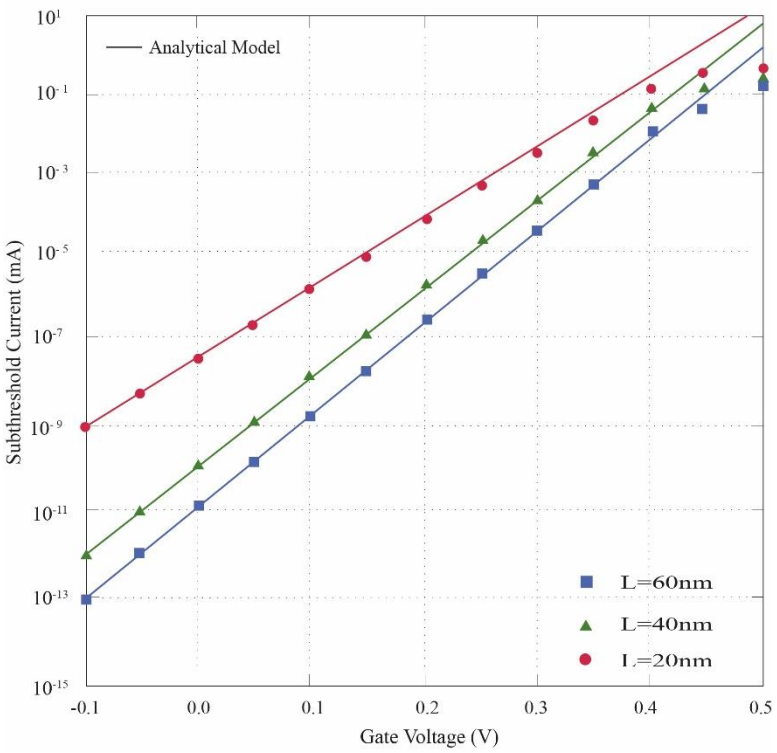


Figure 4.4. Subthreshold current of CSDG MOSFET versus the gate voltage by numerical simulation and model with different channel length.

Furthermore, the presence of the thin gate oxide on the proposed CSDG MOSFET reduces the subthreshold leakage current by enabling greater gate control over the channel and minimal lateral electric field effects. The subthreshold current versus the gate voltage with respect to different variations of the silicon film is shown in Figure 4.5. It is observed that the as the gate-oxide thickness increases, the subthreshold current leakage also increases. The increased gate oxide reduces the gate control over the channel and the leakage due to impacts from the drain is added to the channel. Hence thin oxide is preferred over thicker oxide. But a balance must be maintained to prevent gate-tunnelling. The deviation of the numerical simulation toward 0.5 V shows the onset of the strong inversion. The numerical simulation is in good agreement with the model within the subthreshold regime. Furthermore, the presence of the thin gate oxide on the proposed CSDG MOSFET reduces the subthreshold leakage current by enabling greater gate control over the channel and minimal lateral electric field effects.

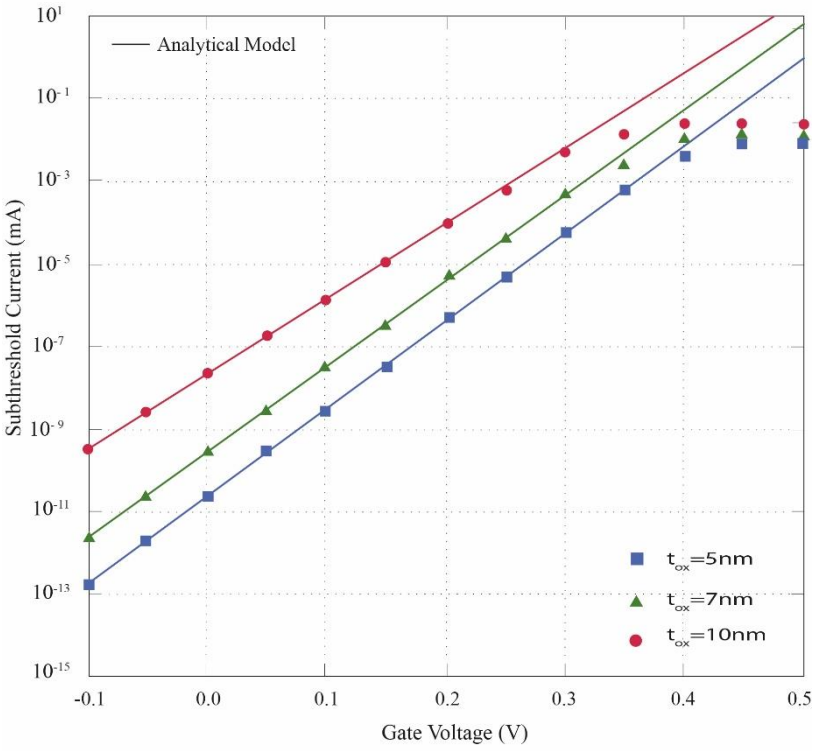


Figure 4.5. Subthreshold current of CSDG MOSFET versus the gate voltage by numerical simulation and model with different gate oxide.

The subthreshold current versus the gate voltage with respect to different variations of the silicon film is shown in Figure 4.5. It is observed that the as the gate-oxide thickness increases, the subthreshold current leakage also increases. The increased gate oxide reduces the gate control over the channel and the leakage due to impacts from the drain is added to the channel. Hence thin oxide is preferred over thicker oxide. But a balance must be maintained to prevent gate-tunnelling. The deviation of the numerical simulation toward 0.5 *V* shows the onset of the strong inversion. The numerical simulation is in good agreement with the model within the subthreshold regime.

Also, the internal and external gates' voltage describes the exponential behaviour of the current in the CSDG MOSFET at subthreshold. This exponential behaviour, known as the subthreshold swing which increases at shorter gate lengths, is minimised in CSDG MOSFET with thin oxide thickness. The smaller subthreshold swing enables better channel control by the gates at micro power application. The subthreshold swing versus channel length for different oxide thickness is presented in Figure 4.6. Subthreshold swing decreases significantly as the oxide thickness decreases because the gates enhance effective channel control. Hence, a thin oxide thickness provides excellent immunity over SCEs. Also, the model matches the numerical simulation of the proposed structure.

Furthermore, the reduction in radii silicon film difference of the CSDG MOSFET enhances the device performance. The subthreshold swing has been minimised by thin radii silicon film. The internal and external gate control over the channel minimises the lateral field effects from the drain end. This results in increase in the threshold voltage. Since the subthreshold swing depends on the gate voltage, increasing the threshold voltage leads to gradual reduction in the subthreshold swing. The subthreshold swing versus channel length at various silicon film thicknesses is shown in Figure 4.7. It is obviously seen that as the channel length decreases, the subthreshold swing increases which is a major problem in scaling at nanometer [level]. This affects the switching characteristics of the of device structure. However, as the radii silicon film thickness decreases, the subthreshold swing decreases. At 10 *nm* radii silicon film thickness, the subthreshold swing decreases below 80 *mV/decades*, enabling faster switching characteristics of the device structure. Hence, thin radii silicon film thickness helps in SCE suppression at reduced channel length. The numerical simulation matches perfectly with the proposed device model.

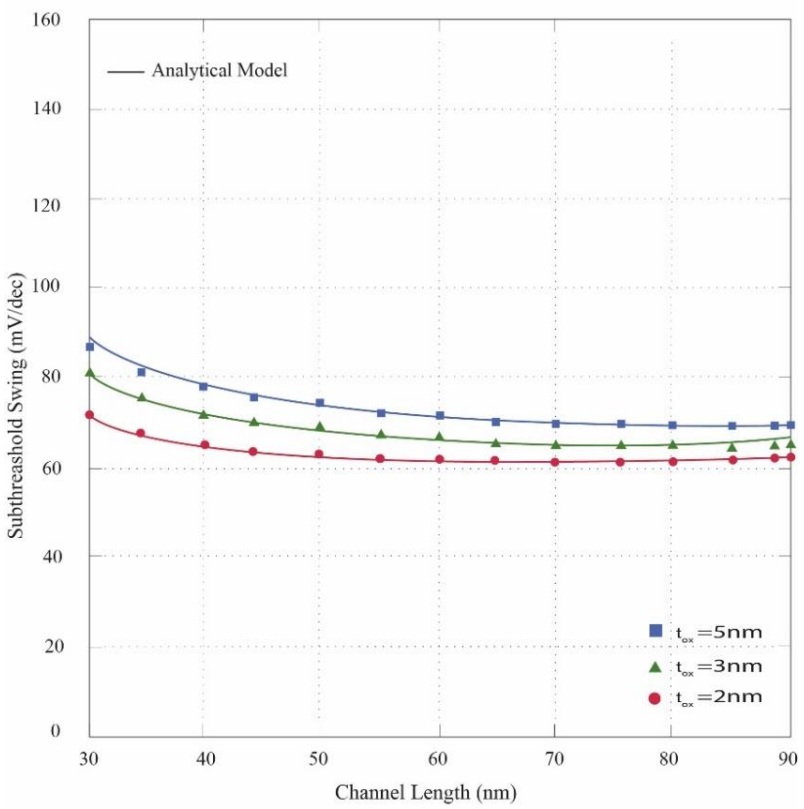


Figure 4.6. Subthreshold swing of CSDG MOSFET versus channel length by device simulator and model with different oxide thickness.

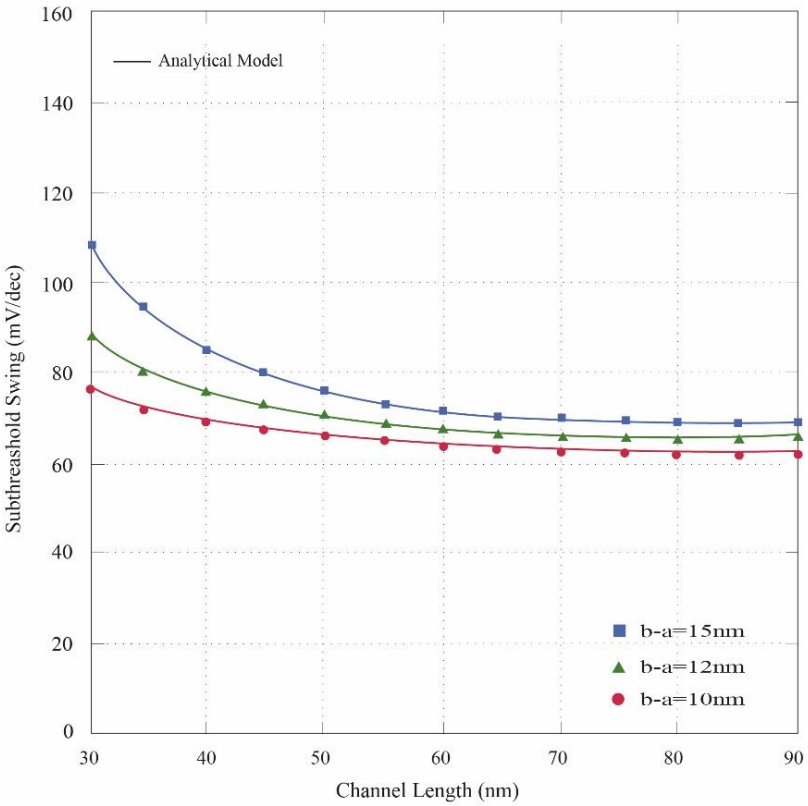


Figure 4.7. Subthreshold swing of CSDG MOSFET versus channel length by device simulator and model with different radii silicon film thickness.

4.6 Chapter Summary

In this chapter, the close-form expression for the threshold voltage, subthreshold current and the subthreshold swing has been obtained using Evanescent-mode approach to observe the device performance. It is found that the internal gate threshold voltage is approximately the same with the external gate, although the external gate matches perfectly with the numerical simulation. The SCEs have been studied with various device parameters like radii silicon film difference, gate-oxide thickness, and the channel length. Results show that the threshold voltage increases with decrease in channel length and an increase in silicon and gate-oxide thickness. Also, the subthreshold current increases with decreases in channel length with an upward shift. The subthreshold swing increases above 60 *mV/decade* at room temperature as the channel length decreases. However, it decreases with a proportional decrease in silicon film or gate-oxide thickness. Furthermore, the models match perfectly with the numerical simulation of the proposed structure.

CHAPTER-5

APPLICATIONS OF CSDG MOSFET

5.1 Introduction

Various home appliances use the small Direct Current (DC) for their operation such as phone chargers, TV and DVD sets, remote control etc. However, the power supplied in homes is Alternating Current (AC), 220/230V 50Hz. In terms of the power consumption, the voltage drops across the conventional diodes are insignificant due to high input voltage. Notwithstanding, at a very low input AC voltage, the voltage drop across the diodes becomes significant. Also, the use of conventional diodes as a bridge rectifier in the telecommunication industry is inapplicable in low-power devices such as a wireless sensor node which requires either battery-bank or self-supportive micro-power electricity for its RF signal transfer and sensing. The micro-power electricity generated through the energy harvested from the environments enables the elimination of the use of batteries for wireless networks and extends their lifetime to infinity, thereby making the method an innovative form of power generation [109, 110]. However, the generated micro-power electricity needs to be converted to DC form through a rectification process for the load utilisation as shown in Figure 5.1. Since the CSDG MOSFET is a low-powered device whose threshold voltage decreases with decrease in gate length to ranges of $0.2V$ to $0.4V$ at nanoscale, the proposed CSDG MOSFET can be utilised as a bridge rectifier for better efficiency.

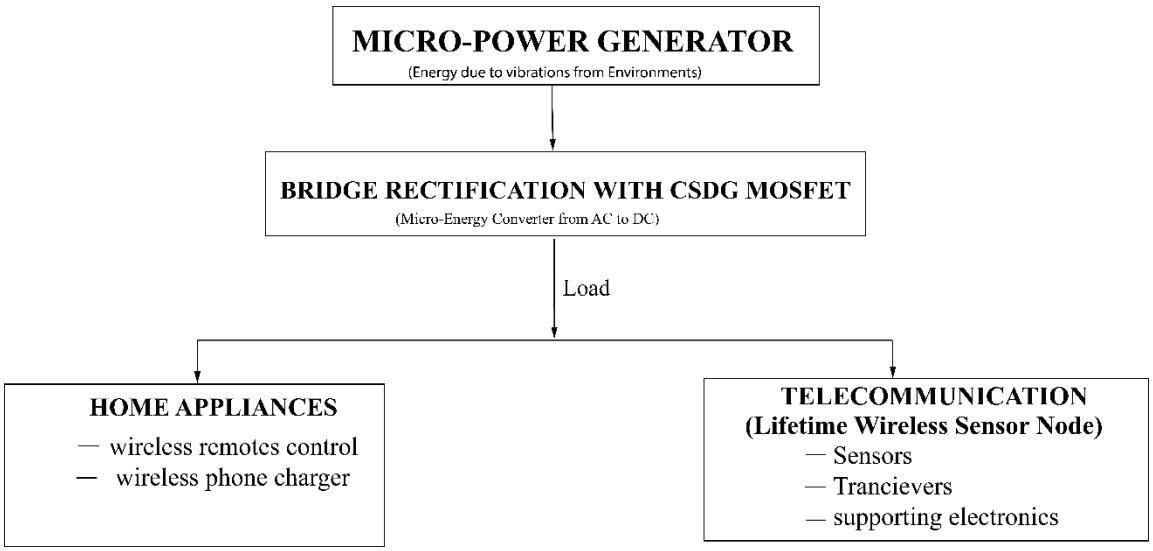


Figure 5.1. Application of CSDG MOSFET as a rectifier for better efficiency.

5.2 Micro Power Generation

Micro power generation is the conversion of energy from the environment into useful electricity. The harvesting of energies is based on two concepts: first, by solar radiation where the solar energy is converted directly to electrical energy in form of direct current (DC); secondly, due to vibration where the kinetic energy (mechanical energy) is converted to electrical energy in form of Alternative Current (AC). Examples of the latter are the energy produced by the human body, thermal gradients, fluid flow, electromagnetic fields, gravitational field action and piezoelectric material which is harvested through microelectromechanical system (MEMS) technology [111]. These two methods of micro power generation have replaced the use of batteries (chemical substances) in our modern micro devices and extend their longevity [112, 113]. Although, the solar power is dependent on batteries at night when there is dim ambient light, limiting its functionality, MEMs pose better prospects; but the AC generated must be converted into DC for electronic use.

5.3 Working of Diode Bridge Rectifier

The bridge rectifier is a circuit that converts the AC to pulsating DC. In the full wave bridge rectifier, four diodes are connected in bridge form to provide full rectification. The circuit diagram is shown in Figure 5.2. In this work the emphasis has been on the full wave bridge rectifier. During the positive half cycle input voltage, the node *A* is made positive with respect to node *B*, so the diodes D_2 and D_4 become forward biased and conduct current through the load R_L and back to node B, while D_1 and D_3 become reverse biased (remains in the *OFF* state). During the negative half cycle of the input voltage, the node *B* is made positive with respect to node *B*. So, D_1 and D_3 become forward biased and conduct current through the load R_L while D_2 and D_4 are reverse biased (remain the *OFF* state). The output frequency is twice the input frequency and a pulsating output voltage is produced at the output with a voltage drop from each of the two-conducting diodes (1.4 V in total) during each phase of the AC supply. This becomes significant when used in a micro power generator.

5.4 Operation of CSDG MOSFET

This CSDG MOSFET follows the three operating modes like traditional MOSFETs [15]:

Cut-off mode: The applied voltage is less than the threshold voltage ($V_{gs} < V_T$) and the device tends to be in the *OFF* state.

Linear mode: The applied voltage at the gate (V_{gs}) is greater than the threshold voltage and drain voltage ($V_{gs} - V_T > V_{ds}$) which leads to the formation of strong inversion channels between the oxide and the *p*-substrate.

Saturation mode: As the drain voltage increases, a saturation region will be reached ($V_{gs} - V_T < V_{ds}$). In this mode, the CSDG MOSFET is fully turned *ON*, and the *ON*-resistance reduces drastically. The CSDG MOSFET operates efficiently under this mode as a rectifier.

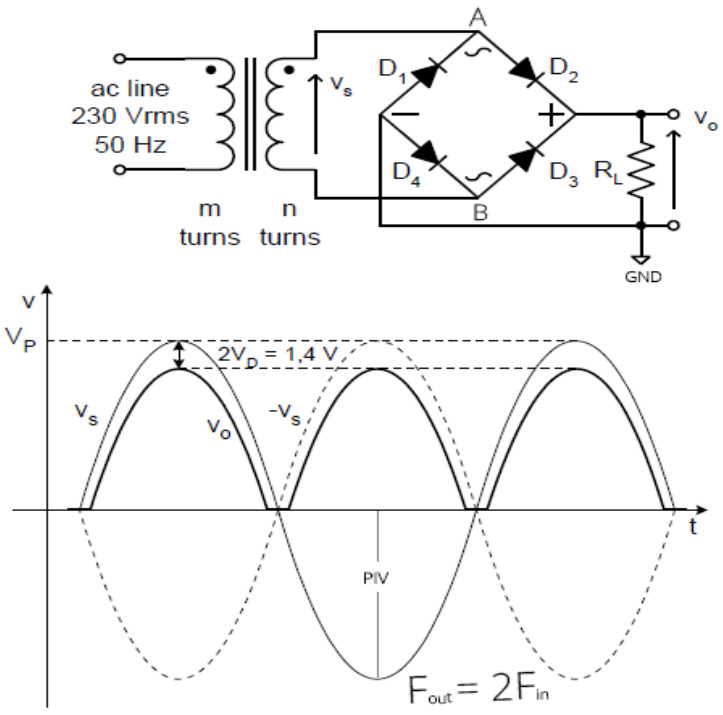
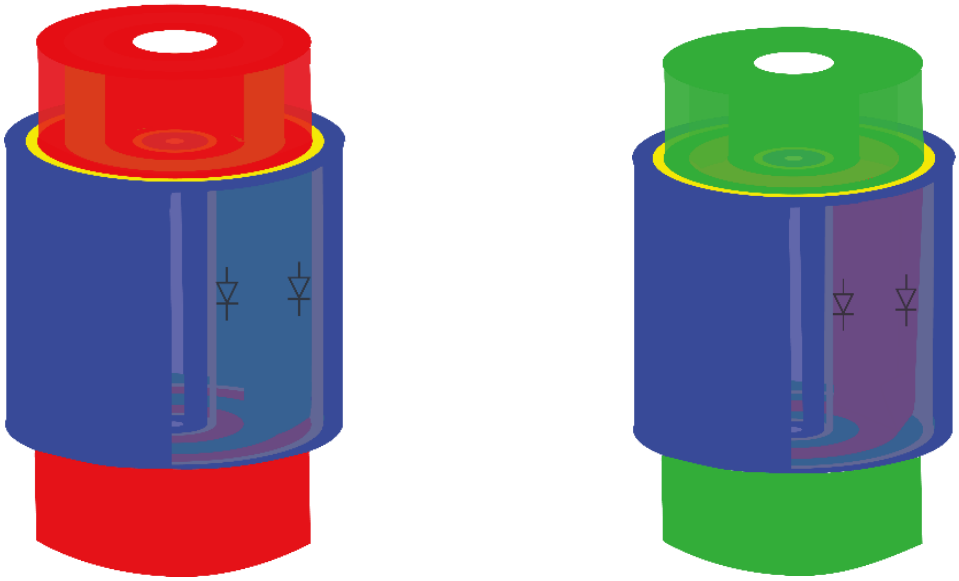


Figure 5.2. Full wave bridge rectifier and its output [114].

5.5 Use of CSDG MOSFET for Bridge Rectifier

The switching techniques in CSDG MOSFET have been used in the design of rectifier circuits. In the switching process, CSDG MOSFET is switched in two possible states: switch-*ON* (conduction of current across it) or switched-*OFF* (no conduction of current). Only two CSDG MOSFETs have been used to replace the four diodes in traditional full wave bridge rectifier. The unused energy, known as energy harvesting, with a low input AC signal from ambient energy, serve as the input voltage to the CSDG MOSFET.



(a) (b)

Figure 5.3. Structure of CSDG MOSFET based on (a) *n*-channel, and (b) *p*-channel

The CSDG MOSFET like the traditional MOSFET has two types, the *n*-channel CSDG MOSFET and the *p*-channel CSDG MOSFET as shown in Figure 5. 3. The *n*-channel can be biased with a positive gate voltage whereas the *p*-channel can be biased with a negative gate voltage. CSDG MOSFET has been modelled as a low-power MOSFET device. When a voltage greater than the threshold voltage is applied to the gate, the CSDG MOSFET is turned *ON*. With the downscale of CMOS technology, the turn *ON* gate voltage lies between 0.2 *V* to 0.4 *V*.

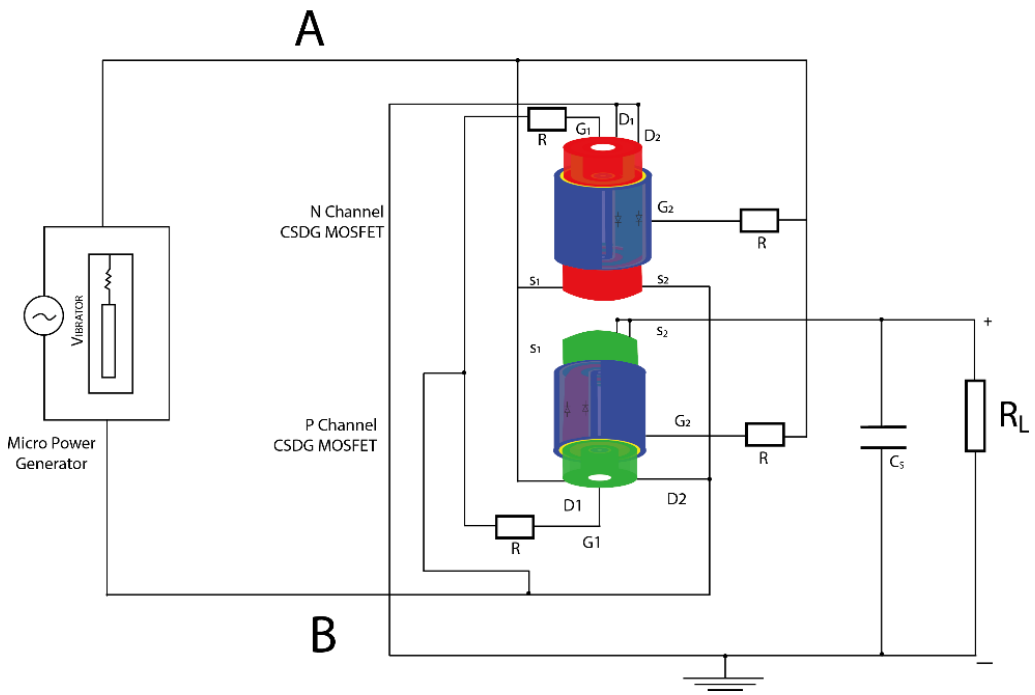


Figure 5.4. Structure of CSDG MOSFET based on (a) *n*-channel, and (b) *p*-channel.

During the positive half cycle, the node *A* is positive with respect to node *B*. Source (S_1) and drain (D_1) terminals of internal CSDG MOSFET of *n*-channel and *p*-channel experience positive voltage while their gates (G_1 of *n*-channel and *p*-channel) are negatively biased. So, an inversion layer channel is created between the drain and source of *p*-channel MOSFET. Hence, S_1 and D_1 of the *p*-channel CSDG MOSFET conduct when the gate voltage is greater than the threshold voltage. This results in low turn-*ON* resistance ($R_{CSDG\text{-}ON}$) between the drain and source, resulting in flow of current from the drain to the source and through the load R_L and D_2 and S_2 of the *p*-channel of CSDG MOSFET, whose gate (G_2) is positively biased and back/returned to *B*.

During the negative phase, the node *B* is positive with respect to the node *A* and the gates (G_2 of *n*-channel and *p*-channel) are negatively biased. So, a conductive channel is created between the drain and source of *p*-channel MOSFET. Hence, D_2 and S_2 of the *p*-channel CSDG MOSFET conduct *B* current through the load R_L and S_1 and D_1 of *n*-channel of CSDG MOSFET and back to *A*. while the D_2 and S_2 of *n*-channel CSDG MOSFET possess a very high turn-*ON* resistance, therefore resisting the flow of current. Therefore, each phase of the alternating current flows through each channel of the gates. Just like the traditional rectifier, the output frequency is twice the input frequency, and the C_s is known as the storage unit of the circuitry. The benefit of this structure is the use of two CSDG

MOSFETs instead of four diodes or four MOSFETs to achieve the direct output voltage from the micro AC voltage current.

5.6 Analysis of the Rectifier Circuits

In this work we have focused on the efficiency and conduction losses analysis with the comparison of diode and CSDG MOSFET based bridge rectifiers [115].

5.6.1 Efficiency Diode based Bridge Rectifier

Efficiency (η_{diode}), the ratio of output to input, is expressed in percentage. So, the efficiency of diode-based full wave bridge rectifier is expressed as:

$$\eta_{diode} = \frac{P_{dc}}{p_{ac}} \times 100\% \tag{5.1}$$

where P_{dc} and P_{ac} are the *DC* output power and *AC* input power respectively. Also, the *AC* power can be expressed as:

$$\left.\begin{aligned} P_{ac} &= P_{rms} + P_{loss} = I_{rms}^2 R_L + I_{rms}^2 r_f \\ I_{rms} &= \frac{I_{dc}}{\sqrt{2}} \end{aligned}\right\} \tag{5.2}$$

where I_{rms}, R_L, and r_f are the root mean square current, the load resistance, and the diode resistance, respectively. The DC power can be expressed as:

$$\left.\begin{aligned} P_{DC} &= I^2{}_{dc} R_L \\ I_{dc} &= \frac{2I_m}{\pi} \end{aligned}\right\} \tag{5.3}$$

Substituting equation (5.2) and (5.3) into equation (5.1) will give the efficiency of approximately 81%, for the diode-based structure.

5.6.2 Efficiency of CSDG MOSFET based Bridge Rectifier

For the clear difference of the efficiency from that of the diode, here symbol (η_{CSDG}) has been used and it can be expressed as:

$$\eta_{CSDG} = \frac{P_{dc}}{p_{ac}} \times 100\% \tag{5.4}$$

where P_{dc} for the CSDG MOSFET output power can be expressed as:

$$P_{dc} = I_{CSDG}^2 R_L \tag{5.5}$$

and P_{ac} for the CSDG MOSFET can be expressed as:

$$\left.\begin{aligned} P_{ac} &= P_{rms} + P_{loss} = I_{rms}^2 R_L + I_{rms}^2 R_{CSDG\text{-}ON} \\ R_{CSDG\text{-}ON} &= \frac{PL}{\pi(b-a)} \end{aligned}\right\} \tag{5.6}$$

where $R_{CSDG\text{-}ON}$ is the turn-*ON* resistance of the CSDG MOSFET, P is the resistivity, L is the device length, b and a are the internal external radius respectively, V_{ds} is the drain-to-source voltage, and I_{ds} is the drain-to-source current. In a bridge rectifier circuit, MOSFETs are forced into conduction in the sinusoidal current input. Thus, in CSDG MOSFET $I_{rms} = I_{CSDG}$

Substituting equation (5.5) and equation (5.6) into equation (5.4) will give the efficiency of CSDG MOSFET which lies between 98% to 99.5% when the CSDG MOSFET is operating in saturation region.

The voltage drop of 1.4 *V* in diode bridge rectifiers becomes obvious in micro-power devices. The CSDG MOSFET tends to have a minimum turn-*ON* resistance when operating at the saturation region. At the saturation region, the CSDG MOSFET acts as an ideal switch with the turn resistance in the order of $m\Omega$ to $\mu\Omega$ [91].

For ideal switch, the current is zero whenever there is an open circuit and the power loss is zero. This implies that the input voltage is equal to the output voltage. When the switch is closed, there is zero voltage across it and the power loss is also zero. Thus, it offers approximately 100% efficiency.

However, the CSDG MOSFET is not ideal − but the power loss is minimal as compared with the diode-based bridge rectifier due to its low turn-*ON* resistance. The minor losses in MOSFETs occur during their switching state (turn-*ON* and turn-*OFF* state), known as the switching losses and conduction losses. They are fully dependent on the turn-*ON* resistor. When the system operates at saturation region, with perfect switching operation mode, we ignore this switching loss. And the conduction loss obeys Ohm's Law in which at saturation point, the turn-*ON* resistance of CSDG MOSFET becomes extremely small and has little or no effect on the channel. This improves the efficiency of the rectifier circuit for wireless home appliances and the telecommunication wireless sensor node.

5.6.3 Conduction Losses of Diode-based Bridge Rectifiers

The average dissipated power in the diode is given by the equation [116]:

$$\left.\begin{aligned} P_{total\_loss,diode} &= P_{loss,diode} + I_{rms}^2 R_L \\ P_{loss,diodes} &= 2V_T I_{(av)} \end{aligned}\right\} \tag{5.7}$$

The voltage drop from the two conducting diodes during each phase is given as $2V_T$. where threshold voltage (V_T) for diodes in the conduction mode is *0.6 V*.

5.6.4 Conduction losses in CSDG MOSFET based Bridge Rectifiers:

The power loss from the conducting CSDG MOSFET during each phase is given by:

$$\left.\begin{aligned} P_{total\_loss,CSDG} &= P_{loss,CSDG} + I_{rms}^2 R_L \\ P_{loss,CSDG} &= I_{CSDG\text{-}ON}^2 R_{CSDS\text{-}ON} \end{aligned}\right\} \tag{5.8}$$

5.7 Results and Discussion

The power loss in diode and CSDG MOSFET are shown in the table below using the conduction losses formula for each device, assuming the average current through the device is 2A. The threshold voltage of diode is $(V_T) = 0.6V$ and the turn on resistance for

traditional MOSFET is between 10 *mΩ* to 20 *mΩ* while that of that of CSDG MOSFET is less than or equal to 5 *mΩ* due to CMOS downscaling of the device. Using these parameters, the results are presented at the table 5.1:

Table 5.1. Comparison of Bridge diode rectifier and Bridge CSDG rectifier

Devices	No of devices	No of conducting components	Formula used for calculation	Power losses in rectifier	Comment
Diode	4	2	$2 \times V_T \times I_{av}$	2.4 W	Though negligible loss, large loss in micro-power devices between 1V to 3V
CSDG MOSFET	2	2	$2 \times R_{DS\text{-}ON} \times I_{av}$	0.02 W	More than 98% percent conserved. Suitable for micro power.

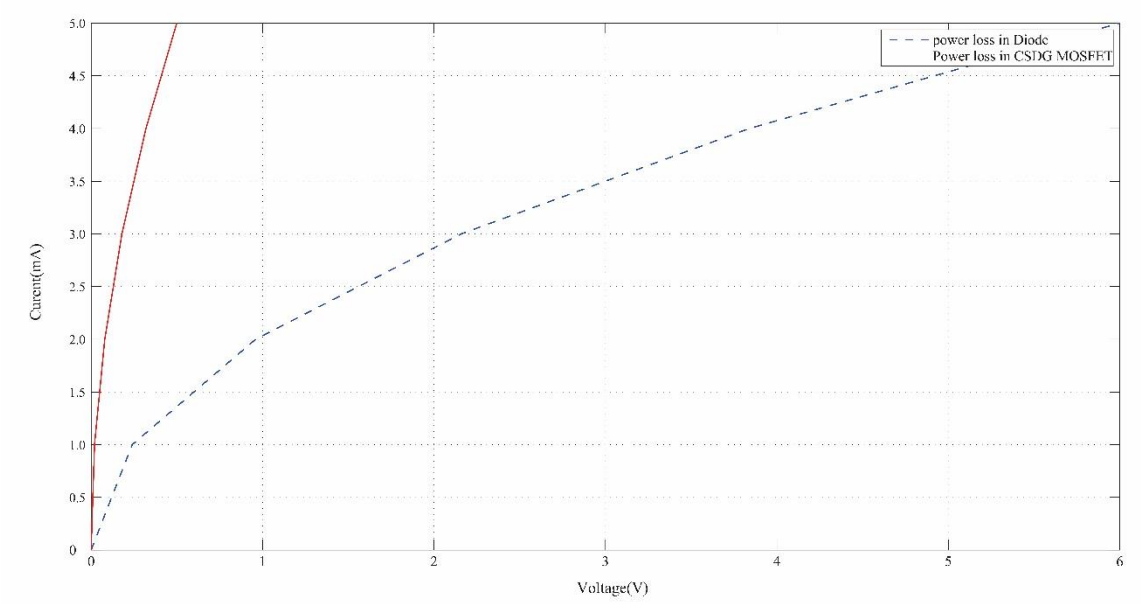


Figure 5.5. Current versus voltage simulation for diode and CSDG MOSEFT.

From the simulation results in Figure 5.5, as the voltage of the device decreases, the power loss in diode tends to be significant, whereas for the CSDG MOSFET it tends toward saturation and the resistance decreases, approaching the *mΩ* order. For this work, the $R_{CSDS\text{-}ON}$ ranges between 10 *mΩ* ~ 20 *mΩ* at saturation region for traditional MOSFET and less than or equal to 5 *mΩ* for CSDG MOSFET at nanoscale [13]. This shows that the

CSDG MOSFET is of better efficiency in rectifier circuits when used in energy harvester systems (micro-power device) than that of diode. Also, the power loss is smaller than that of traditional MOSFET at any given average current since its turn-*ON* resistance is smaller.

5.8 Use of CSDG MOSFETS in Home Appliances

The CSDG MOSFET can be used in electronic appliances through the rectification process to supply direct current to wireless remote control, Bluetooth headsets, calculators and phone chargers. According to researchers from Nokia [117], cell phones could be powered by harvesting the energy emitted from the electromagnetic radiation of wi-fi transmitters, TV masts, and cell phone antennas from the environment. Once this energy is harvested from the environment, a low-power consumption device is needed to convert the generated electricity into useful direct current for home appliances. For this reason, the CSDG MOSFET is used as a bridge rectifier to convert the generated AC into meaningful DC input to the electronic appliances as shown in Figure 5.6, by which the home appliance can be energised with the generated DC. This makes the proposed CSDG MOSFET a promising device for a long-life supply of electricity to electronic gadgets in the nearest future.

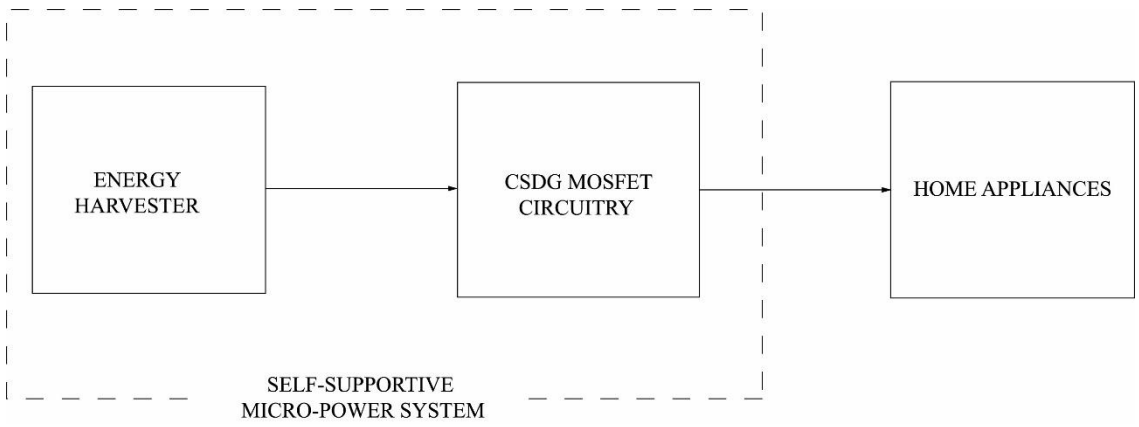


Figure 5.6. Schematic diagram of self-powered home appliances through Energy Harvesting System and CSDG MOSFET.

5.9 Use of CSDG MOSFETS in Wireless Telecommunication

In the wireless telecommunication system, CSDG MOSFET is also applicable in rectifying the harvested energy from MEMS devices to provide a lifetime DC supply to the wireless sensor network as shown in Figure 5.7.

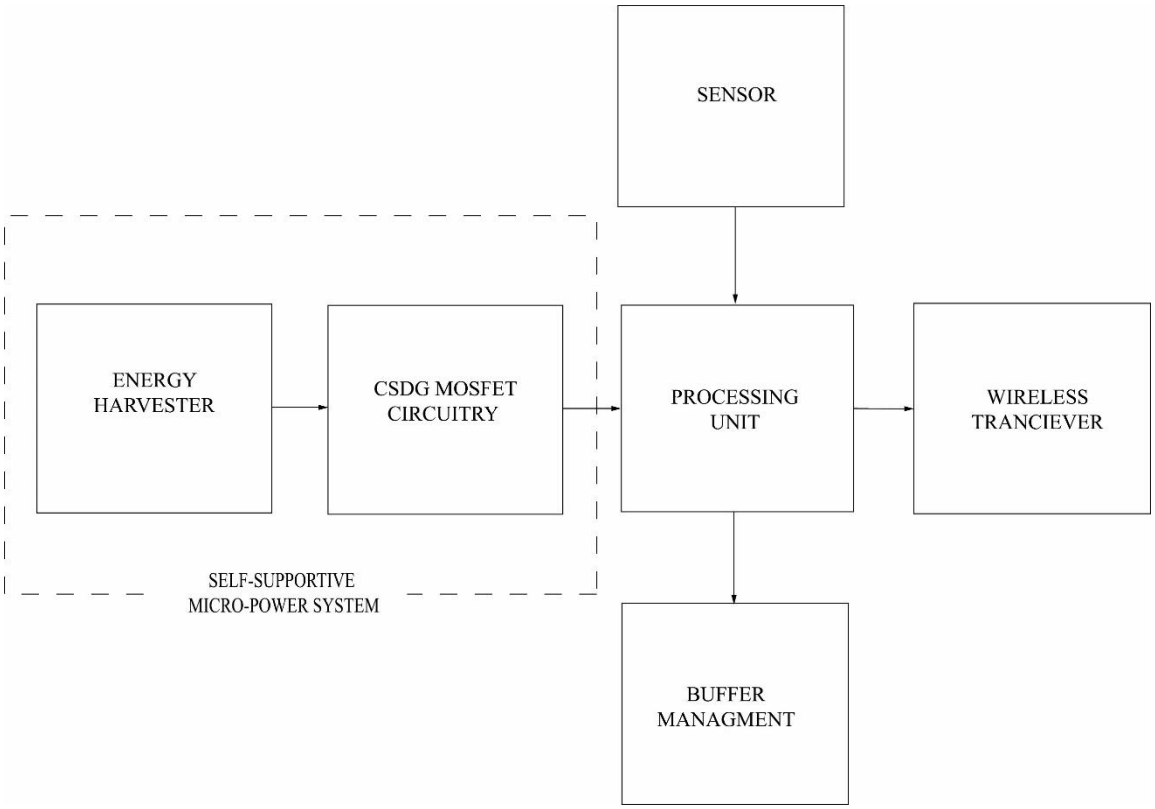


Figure 5.7. Schematic diagram of wireless sensor node with energy harvesting system and CSDG MOSFET for telecommunication technologies.

The arrow line shows the flow of energy and packet data from one unit to another. The power system ensures a lifetime supply of power to the processing unit of the wireless node. The function of the processing unit is to process the incoming data from the sensor and assemble it into packets. The packets are grouped and, based on their priority, some are transmitted through the wireless transceiver while the remainder are relayed to the management buffer. The major role of the buffer management is to store the incoming packets and sequence them for future transmission. Furthermore, the wireless transceiver enables the transmission and reception of data packets in the sensor node. Since this process occurs continually, to ensure continuous supply of energy to the wireless sensor,

we consider replacing the battery with a self-supportive micro power system as shown in Figure 5.7. This can increase the longevity of the wireless node.

5.10 Chapter Summary

This chapter proposes the application of CSDG MOSFET as a bridge rectifier for better efficiency. Also, we applied the circuit with the energy harvester system to further describe a self-supportive micro power system for home appliance and wireless telecommunication sensor node.

CHAPTER-6

CONCLUSIONS AND FUTURE RECOMMENDATIONS

6.1 Conclusions

This research dissertation has presented the theoretical modelling of the channel potential, threshold voltage, subthreshold current and subthreshold swing of CSDG MOSFET using Evanescent-mode analysis to study the device performance with different device parameters like oxide thickness, gate length, radii silicon film difference, and biasing voltage. Moreover, the numerical simulations match the model. Furthermore, the switching characteristics of the CSDG MOSFET were applied to rectify the energy harvested with MEMS from the environment. This enhances circuit efficiency and provides a self-supportive micro-power system for wireless home appliances and telecommunication wireless sensor node.

The modelling of the minimum surface potential was carried out to predict the accuracy of the device characterisation and better performance for the suppression of SCEs. It is observed that the reduction in the oxide thickness and radii difference of the proposed CSDG MOSFET as the channel length decreases improve the device performance and provide better immunity to SCEs. Also, the threshold voltage roll-off which is due to 2D field effect that originated from the source and drain region because of their proximity to the channel can be optimised by decreasing the oxide thickness and radii silicon film difference of the CSDG MOSFET. Furthermore, the behaviour of the DIBL was observed in our model which shows that the threshold voltage does not only depend on the decrease in channel length but also on the drain bias due to the increase in the surface potential at the drain end.

Furthermore, the magnitude of the drain current of CSDG MOSFET at the subthreshold region, known as the subthreshold leakage, can be minimized by decreasing the oxide thickness. Also, it is observed that the decrease in the device channel length increases the subthreshold leakage. However, the coupling of the internal and external gate control over the channel limits the leakage. Also, it is observed that the subthreshold swing is directly proportional to oxide thickness and radii silicon film difference of the CSDG MOSFET. Hence, to control the drain current flow effectively for better switching characteristics, the

oxide thickness and the radii silicon film difference must be decreased moderately. Furthermore, the switching characteristics of the CSDG MOSFET are utilised in the design of the bridge rectifier circuitry for low-power devices.

6.2 Future Recommendations

The analytical model considered in CSDG MOSFET is assumed to have minimum channel length of 30 *nm*. However, at less than 30 *nm* channel length, the quantum mechanical effects become obvious in the CSDG MOSFET. Future research could consider the quantum mechanical effects by solving the Poisson equation and Schrodinger's equation self-consistently. In addition, the influence of direct current, radio frequency (RF) and microwave noise on the nanoscale regime for CSDG MOSFET can also be considered. Also, the small-signal modelling and RF noise modelling of CSDG MOSFET can be considered in the future to observe the behavior of the device. Furthermore, an extensive study of CSDG MOSFET in the application of analogue and RF transmission can be carried out. Moreover, different metal gates like tin metal and molybdenum can be used in place of polysilicon to suppress SCEs.

HFO_2 can be used with the silicon oxide insulator to minimize the current tunneling effect that occurs as the CSDG MOSFET is scaled beyond 30 *nm*. Since, the leakage current depends on the barrier height, addition of HFO_2 increases the barrier height and further prevents the leakage of current. This can be considered in the future to further improve the device performance at less than 30 *nm* channel length and enhance the gate oxide reliability. Also, for RF high-speed applications, vacuum gate dielectric can be used in the future to minimize hot carrier effects due to its low electric field. However, since the vacuum gate dielectric has low *on*-current and transconductance when compared to silicon oxide, adequate channel doping can be implemented with it for better performance of CSDG MOSFET device in the future.

Also, Double Surrounding Gate Material (DSGM) or Triple Surrounding Gate Material (TSGM) can used for both the internal and external structure of the CSDG MOSFETs in the future to further enhance the analogue and digital radio frequency (RF) performance of the device structure. Since the DSGM and TSGM effectively screen the drain and source potential impact on the channel, this method can be used in the future to provide better immunity to short channel effects at nanoscale of less than 30 *nm* and maintain the scaling of the threshold voltage.

Furthermore, the noise characteristics of the device structure, such as the flicker noise, thermal noise and shot noise are more pronounced in the nanotechnology regime. These noise characteristics are yet to be fully exploited in the proposed CSDG MOSFET and can be considered in the future research work to observe the noise behavior of the proposed structure.

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