Improved Parametric Analysis of Cylindrical Surrounding Double-Gate (CSDG) MOSFET

Thesis submitted for the fulfilment of requirements for the degree of

MASTER OF SCIENCE

In

Electronic Engineering

by

OKIKIOLUWA EZEKIEL OYEDEJI

DEPARTMENT OF ELECTRONIC ENGINEERING,
UNIVERSITY OF KWAZULU-NATAL,
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STUDENT NO.: 216074998 **DECEMBER 2018**

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Name of supervisor: Prof. (Dr.) Viranjay M. Srivastava

Signature:

Date: 13 Dec. 2018

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List of Publications

Journal Publication

1. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Thermal Effect and Stability of Cylindrical Surrounding Double-Gate (CSDG) MOSFET," ***International Journal of Engineering and Advanced Technology (IJEAT),*** vol. 8, no. 4C, pp. 23-27, April 2019.

2. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Effect of Radius on various Parameters of Cylindrical Surrounding Double-Gate (CSDG) MOSFET," ***International Journal of Engineering and Technology, UAE (IJET)***, vol. 7, no. 4, pp. 2127-2131, May 2018.

Conference Papers

3. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Cylindrical surrounding double-gate MOSFET based amplifier: A circuit perspective," *International Conference on Intelligent Computing, Instrumentation and Control Technologies (ICICICT 2017),* Kannur, India, 6-7 July 2017, pp. 152-155.

4. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Carrier mobility aspects for cylindrical surrounding double-gate MOSFET," *International Conference on Engineering and Technology (ICET 2016),* Coimbatore, India, 16-17 Dec. 2016, vol. 2, pp. 332-335.

Dedication

To my parent, Mr. and Mrs. Oyedeji.

ACKNOWLEDGEMENTS

My gratitude goes to Prof. (Dr.) Viranjay M. Srivastava for his guidance, support, advice and persistent encouragement during this research work. I appreciate him for his sincerity and fatherly support during the hard times in the course of this research.

Also, to my wonderful parent Mr. & Mrs. Oyedeji and my siblings, Wunmi, Samuel and Pater, without their sincere love, patience, understanding, and spiritual support, this might not be a reality.

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ABSTRACT

Transistors are major components in designing and fabricating high-speed switching devices and micro-electronics. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is popular and highly efficient for designing switches. It has wide applications in microelectronics, nanotechnology and Very Large-Scale Integration (VLSI) design where millions of MOSFETs are fabricated and embedded into a single chip. In these applications, heat becomes a major concern and requires to be addressed.

The Cylindrical Surrounding Double-Gate (CSDG) MOSFET was introduced to overcome this challenge. The device has two scaled channel paths in a cylindrical two-gate structure, which have excellent control on the electrostatic activities that take place along the channel. This help to reduce corner effect and short channel effect and in turn produce higher drain current. This research work explores these advantages to propose a novel structure for an improved CSDG MOSFET.

Firstly, the physical dimensions and structural layout of the improved CDSG MOSFET are highlighted and explained. After that, a parametric analysis of the CDSG MOSFET design has been done. This includes and supported with mathematical analysis and derivation of its operational parameters, namely surface potential, drain current, threshold voltage, transconductance, carrier mobility and capacitive characteristics etc. Thirdly, the thermal effects of this proposed device is analysed at different temperature. Also, the performance of the CDSG MOSFET is analyzed and compared to other existing MOSFET structures.

The results from this analysis show that the improved CDSG MOSFET outperforms other existing MOSFETs. In fact, its power consumption is shown to be lower than those of other compared MOSFETs. A practical application of this device as an amplifier also yields plausible performance in terms of amplification gain and efficiency over a wide range of temperatures.

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GLOSSARY OF ABBREVIATIONS

AC:	Alternating Current
ADG MOSFET:	Asymmetric Double-Gate Metal Oxide Semiconductor Field-Effect Transistor
BJT:	Bipolar Junction Transistor
CSG MOSFET:	Cylindrical Surrounding Gate Metal Oxide Semiconductor Field-Effect Transistor
CSDG MOSFET:	Cylindrical Surrounding Double-Gate Metal Oxide Semiconductor Field Effect Transistor
DC:	Direct Circuit
DG MOSFET:	Double Gate Metal Oxide Semiconductor Field-Effect Transistor
FDSOI:	Fully Depleted Silicon-On-Insulator
FinFET:	Fin Field Effect Transistor
GAA:	Gate-All-Around
GCA:	Gradual Channel Approximation
IC:	Integrated Circuit
MM:	Meyer Model
MOS:	Metal Oxide Semiconductor
MOSFET:	Metal Oxide Semiconductor Field-Effect Transistor
PDSOI:	Partial Depleted Silicon-On-Insulator
RF:	Radio Frequency
SCCM:	Simple Charge Control Model

SCE:	Short Channel Effect
SG MOSFET:	Single-Gate Metal Oxide Semiconductor Field-Effect Transistor
SOA:	Safe Operating Area
SOI:	Silicon-On-Insulator
ULSI:	Ultra Large Scale Integrated
VLSI:	Very Large Scale Integrated
VSM:	Velocity Saturation Model

GLOSSARY OF SYMBOLS

V_{GS}:	Gate-Source Voltage
V_{th}:	Threshold Voltage
V_{DS}:	Drain-Source Voltage
$V_{DS_{SAT}}$:	Drain-Source Voltage at saturation
V_T:	Thermal Voltage
k:	Boltzmann Constant
T:	Temperature
q:	Carrier Charge
g_m:	Transconductance
μ:	Carrier Mobility
Ga_2O_3:	Gallium (III) oxide
GaN:	Gallium nitride
G:	Gate
D:	Drain
S:	Source
I_d:	Drain Current
L:	Channel length
W:	Channel width
H:	Channel height
t_{ox}:	Oxide Thickness
V_{BS}:	Bulk-Source Voltage
n:	number of charges
V_{Gt}:	Overdrive Voltage
E:	Electric field
Q:	Charge densities
Q':	Charge per unit area of the channel
C_{ox}:	Capacitance per unit area of the silicon oxide
β:	Transconductance parameter

q_d:	Depletion Charge Density
q_i:	Inversion Charge Density
V_{FB}:	Flat-band Voltage
ψ_b:	Surface potential quantity that characterize the semiconductor body
ε_s:	Semiconductor Permittivity
ε_{ox}:	Semiconductor-oxide Permittivity
E_s:	Saturation Electric field
ϕ_F:	Fermi potential
W_{dm}:	Maximum Depletion Depth
W_d:	Depletion Depth
ψ:	Surface Potential
$\psi(x)$:	Electrostatic Potential
V:	Electron Quasi-Fermi Potential
n_i:	Intrinsic Carrier Density
ε_{si}:	Permittivity of the silicon
I_{ON}:	Current-ON
q_s:	Charge per unit area
v_d:	Drift velocity
v_s:	Velocity at saturation
$\Delta\varphi$:	Work function
τ:	Transit time
ϕ_t	Thermal Voltage

CHAPTER 1

INTRODUCTION

The Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) is a basic component in the implementation of Very Large Scale Integrated (VLSI) circuits [1, 2]. Due to its simple structure, reduced consumption of power, and economical fabrication, it has attracted applicability in the design of portable electronic devices [3, 4]. Also, its application facilitates the implementation of sophisticated designs that other transistor may not execute with ease [5, 6].

In this chapter, the general background of MOSFET has been examined. The limitations it encountered over the period of usage with how it has revolved in structure and sizes are also discussed. Furthermore, the thermal influences it has on operation and application which are the basis of this thesis are introduced.

1.1. Background of MOSFET

Since the invention of thermionic valve (diode) in 1904 by *Sir John Ambrose Fleming* through inspiration from *Thomas Edison's* work, several inventions have been made to improve this electronic technology. This first invention is cathode-beam relay, used as the earliest amplifier device. The *Audion* is the discovery of transistor on Germanium body in 1947. Transistors was further tested on a pure Silicon with its application on Integrated Circuit (IC) and was widely accepted [7]. In 1962, the MOSFET, a device invented at a research laboratory in New Jersey with its benefits surpassing that of Bipolar Junction Transistor (BJT) was introduced. It has revolutionized and used basically as switching device in electronic appliances.

The MOSFET is a three-terminal device and it is represented by the symbol shown in Fig. 1.1. Since inception, the MOSFET has been based on a Silicon bulk technology, later silicon-on-insulator (SOI) has replaced the bulk technology due to its reliability, increased speed, and low power consumption.

There are four types of MOSFET based on their semiconductor body and on whether they conduct current or not by default, shown in the table 1.1.

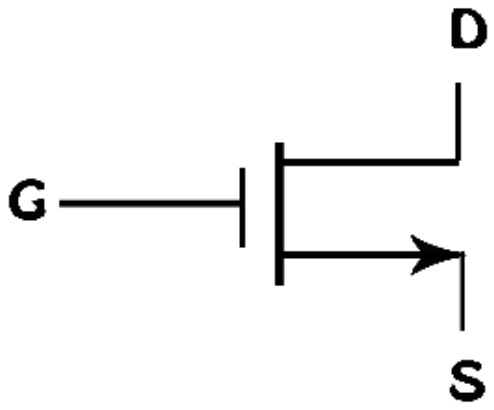
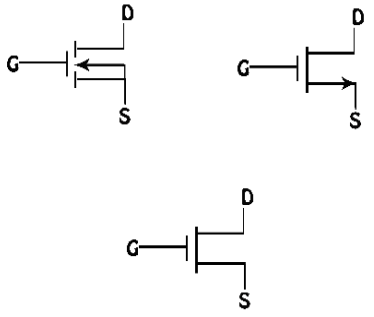
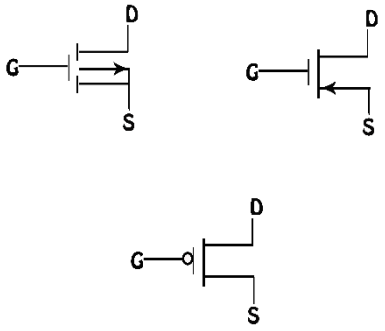
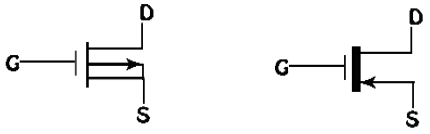


Figure 1.1 Symbol of MOSFET [8].

In *n*-channel MOSFET electrons (the negative charges) are responsible for current flow in the device while *p*-channel MOSFET has holes (the positive charges) as the carrier. In another dimension to these types are the enhancement and depletion modes. The enhancement mode transistors are OFF by default and needs to be biased to '*Enhance*' the flow of current while the depletion mode is ON by default and needs an applied gate voltage to turn the de$_v$ices OFF. In this research work, we will focus on the *n*-channel enhancement MOSFET.

Table 1.1 Symbols of MOSFET types [9]

	n-channel	*p*-channel
Enhancement mode		
Depletion mode		

1.2. Limitations of MOSFET

The introduction of MOSFET in 1960 by *Atalla and Kahng* [10] has been an effective device that all electronic gadgets rely on for their functionality. It aids the use of quite a number of devices on single chip for implementation of great tasks. Few years into its effectiveness, *Gordon Moore* observes that within a year and half, the number of this transistor stuff on an integrated chip increases by a factor of two, which led to the Moore's law [11]. This law has effectively helped in the scaling of the transistor to achieve greater performance and cost reduction. However, this scaling comes with its disadvantages that put a limit on the performance of the devices.

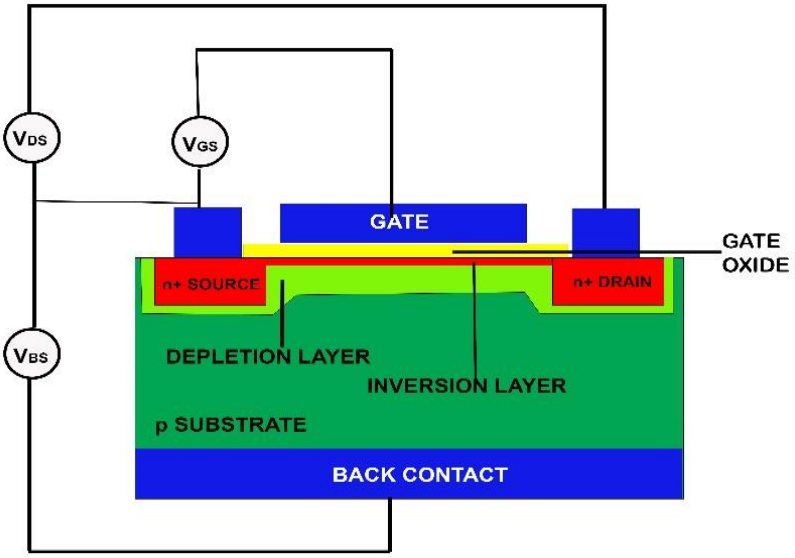


Figure 1.2 *n*-channel enhancement MOSFET [8].

(i) One of the limitations of MOSFET is punch-through. Considering an *n*-channel enhancement MOSFET as shown in Fig. 1.2 with gate voltage less than threshold voltage ($V_{GS}<V_{th}$) and zero drain-source voltage ($V_{DS}= 0$). At this instant, the MOSFET is in its cut-off stage as there exists a high resistance, preventing the movement of electron from the source. However, it seems no current flow at this point but there is a leakage current flow in the drain region due to the reverse biased condition of the drain-body junction. This is because of the proximity of the body with the drain. But as V_{GS} increases beyond

V_{th} and kept constant, the resistance is overcome and a channel formed while the depletion between the drain and it body is increased.

When the V_{DS} increases, the depletion region between the drain and the body is further increases producing an appreciable amount of current flow in the device. However, further increase in the V_{DS} causes more current to flow, to the extent, it becomes relatively impossible for the gate to control the device as the current continues to flow even when the V_{DS} is turned-OFF. This occurrence is called punch-through, while the current flowing when the V_{GS} is turned-OFF is called punch-through current, and this makes the device not to function normally [12]. Considering this limitation in a short-channel device, there will be a major breakdown in the drain-source junctions, thereby causing a distortion in the voltage-current characteristics. This limitation is taken care of in this research work with the application of a Double-Gate (DG) MOSFET characteristics that have an excellent electrostatic control over the conducting channels.

(ii) Another challenge encountered while reducing the device dimension to adapt nanometre scaling is the effect of Electric-field. To balance with the dimensional reduction, the supply voltage is supposed to be reduced. However, this is impossible because the threshold voltage cannot be reduced much due to the thermal voltage ($V_T = kT/q$) characteristics, which make the threshold range at constant value temperature [13]. This implies that with a reduced dimension with same voltage supply, the vertical electric field generated is higher, at the channel and results to the carrier mobility being weakened. This phenomenon is called velocity saturation and it is due to various scattering mechanism and further results to increase in to leakage current which was initially supposed to solve and breakdown of the device.

Also, the required separation between the drain and source is minimum energy of *0.017 eV* at room temperature with the appropriate length separation of *5 nm* according to quantum mechanism to avoid tunnelling. When this scaling is implemented in nanotechnology such that the channel between the drain and source no longer requires the voltage from the gate to control its activities and it became disadvantageous for the transistor to work as a switch, this is one of the major application of the device [14]. This is taken care of by the undoped characteristics of the Cylindrical Surrounding Double-Gate (CSDG) MOSFET.

(iii) Another challenge that MOSFET faced is hot carrier effects. When the device dimension is reduced, (e.g. as the length of channel reduces with constant voltage supply), then it threshold voltage adversely affected. Electric field generated is experienced more at the drain part of the channel. The movement of the electron from the source to the drain witnesses an increase in the kinetic energy which result to impact ionization. This implies that the electron under the influence of greater field effect at the drain acquires more energy to be ejected to other parts with less energy. This might involve the movement of electron to the body, breaking the gate oxide boundary to migrate to the gate or being trapped in the gate oxide resulting to the increase in gate current and shifting of threshold voltage. This obviously causes instability and breakdown of the device [15].

(iv) All these discussed limitations cause temperature instability within the MOSFET and with its environment it is operating with. In the MOSFET, since the device have so many passive electronic components compact together and the operation of the conducting channels with short channel effect, thermal stability is abounding to rise. Also, with the environment, the contact the MOSFET have with the IC board it is mounted upon generate thermal effect which might cause inconsistency in the performance of the MOSFET. This challenge will be reduced with the improved structure proposed in this research work through finding a way to stabilize thermal effect.

1.3. Research Motivation

The application of MOSFET in the design of various contemporary devices, especially in the fabrication of Integrated Circuits (ICs) cannot be over-emphasized. This is due to the possibility of attributes of having more than *100 million* devices stuffed up on a single chip to carry out sophisticated tasks [6, 16]. However, despite the peculiarity and reliability of this device, it is affected by changes in temperature. As the operating temperature increases or reduces beyond or below tolerance, the total energy from the molecular motion of the carrier in MOSFET is affected, causing the required speed and functionality to be unattainable. Moreover, since heat conductivity in Silicon-on-insulator (SOI) MOSFET differs from that of bulk Si MOSFET, so temperature appears to be a difficult parameter to manage [17]. Inability to adequately manage the effect of temperature change often leads to thermal runaway, a phenomenon caused by the

recycling of increased temperature with leakage current, which has unstable consequence on the MOSFET [18]. When the temperature of the MOSFET increases at high voltage supply, the drain saturation current as well as the switching speed reduces [19]. On the other side, exposure of the MOSFET to cryogenic temperatures gives an upgrade on the number of device functionality. This results in the increase of the device transconductance (g_m) and reduction of its series resistance.

This explicates an improved yet dynamic performance. Moreover, the reduction in temperature produces a reduced sub-threshold current and slope that translates to a reduced power consumption [20]. This advantage at lower temperature comes at the cost of reduced reliability and performance of the device. Nevertheless the shortcoming nullifies the advantages and make the thermal effect a concern to manage [21]. In effort to manage the thermal effect and improve the performance of the MOSFET for RF switches, multiple gates transistor was introduced [14, 22, 23]. The multiple gates transistor created have more control over the channel which produces improved current per unit width with low leakage current. The effect of heat with this improvement has however been a challenge that has been discussed with different models and proposals being introduced to overcome it.

Goelet. al. [24, 25] analysed the effect of temperature on threshold voltage (V_{th}) and it mobility (μ) of a MOSFET. It uses the effect of low temperature below *200 K* to expand the depletion region of the transistor to aid the conversion of a Partial Depleted Silicon-On-Insulator (PDSOI) MOSFET to Fully Depleted Silicon-On-Insulator (FDSOI) MOSFET. The application of both SOI MOSFET were used and varied for maximum performance of the MOSFET. On the threshold voltage, it has been observed that it increases due to increase in Fermi potential. Also, the carrier mobility varies due to phonon scattering, but at *77 K* mobility gives an improved value.

Srivastava [26] has analysed the thermal effect in term of resistance for Nano-scaled Double Gate (DG) and Cylindrical Surrounding Double-Gate (CSDG) MOSFET. The model makes use of thermal Ohm's law to compare the thermal resistivity between the DG and CSDG MOSFET. It was discovered that the thermal resistance in the DG is better than that of Single-Gate (SG) MOSFET. Equally, due to the cylindrical structure of CSDG MOSFET, the thermal effect is greatly reduced when compared with DG MOSFET and consequently has great application in RF switch. *Chabak et. al.* [27] have

analysed the effect of temperature when Gallium oxide (Ga_2O_3) is fabricated as the gate dielectric on the Gallium Nitride (GaN).

It was observed that the gate leakage reduced as the temperature increased. Further effect was made to increase the temperature to about $400\ ^0C$, a significant decrease in gate leakage was discovered. This observation was due to the decrease in parasitic resistance of the contact, making its relevant better than conventional MOSFET[28]. *Chou et. al.* [29] also implemented a stability approach to thermal effect by integrating the MOSFET with a controller. With this, the varying temperature could be sensed, and hence helps in protecting the device [30].

With this problem at hand, there is need to develop a better structure in CSDG MOSFET with the sole responsibility of managing the thermal challenge among others. With this motivation, this work considers how to bring about stability in thermal effect using various parameters comparing them for better performance with its trending evolution shown in Figure 1.3. The set objectives for achieving this are listed in the Section 1.4.

1.4. Research Objectives

The objectives of this dissertation are to analyse the improved structure of the CSDG MOSFET and further discuss its thermal effects. Moreover, it also seeks to adopt a minimization technique that suits best for this MOSFET type using its parametric analysis. The research objectives for achieving these analyses are itemized below:

A. To review the trends in the structure of the MOSFET and its multiple gates with the intent of solving the possible challenges attached.

B. To analyse the parameters of the MOSFET at each changing trend.

C. To propose a suitable CSDG MOSFET structure that further minimises the thermal challenges in relation to its parametric analysis.

D. To examine the thermal challenges involved in this novel structure and its effects on the various parameters.

E. To analyse the possible thermal stability involvement in this novel structure.

F. To discuss and layout the advantages of this structure with respect to its application as a RF switch, rectifier, and amplifier.

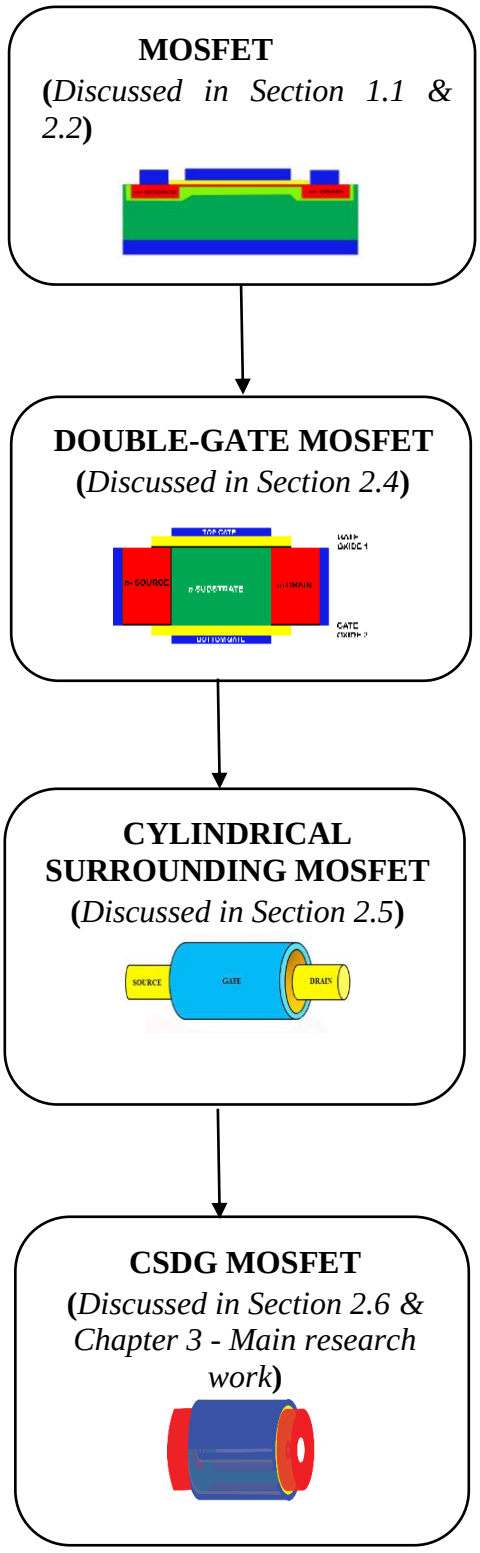


Figure 1.3 Flowchart of MOSFET over time to combat various limitations.

1.5. Organization of Thesis

This research work has been divided into six chapters and each of these chapters is summarised as:

Chapter one deal with the Introduction of MOSFET with its structure and operation. The chapter further discusses the research motivation and objectives with the list of publications.

The **chapter two**, Literature Review explains the overview of the changing trend in MOSFET, that is, the Single-Gate (SG) MOSFET, Double-Gate (DG) MOSFET, Cylindrical Surrounding Gate (CSG) MOSFET and Cylindrical Surrounding Double-Gate (CSDG) MOSFET. Since our research work is based on the CSDG MOSFET, so we introduced the structure with the previous contribution from others and explain the need for a better structure with respect to the existing challenge.

In **chapter three**, the novel structure for the CSDG MOSFET has been introduced. The parameters involved due to the new structure has been examined. The drain current which also play a role in the application property of the device has been analysed. The drift-diffusion components have been used to analyse the drain current of the device through the Pao-Sah integral. Then transconductance has been derived to indicate an improved performance of the proposed design while surface potential among others has been also analysed.

In **chapter four**, the derived parameter formula and models have been analysed to verify their authenticity and compared with other models and their usefulness in various applications. Also, the thermal effect in the structure has been analysed with thermal resistance and thermal noise with possible ways of reducing or eradicating them for better performance in the device.

Applications of the CSDG MOSFET has been examined in **chapter five**. The CSDG MOSFET is applied for an amplifier and RF switch with its efficiency emphasized.

Finally, in **chapter six**, the summary of the research work has been presented. The conclusion and possible work that can be implemented in the future as regard the structure is also listed and suggested.

1.6. List of Publications

1. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Carrier mobility aspects for cylindrical surrounding double-gate MOSFET," *International Conference on Engineering and Technology (ICET 2016),* Coimbatore, India, 16-17 Dec. 2016, vol. 2, pp. 332-335. [*Overlapping chapter 3*].

2. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Cylindrical surrounding double-gate MOSFET based amplifier: A circuit perspective," *International Conference on Intelligent Computing, Instrumentation and Control Technologies (ICICICT 2017),* Kannur, India, 6-7 July 2017, pp. 152-155. [*Overlapping chapter 5*].

3. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Thermal Effect and Stability of Cylindrical Surrounding Double-Gate (CSDG) MOSFET," *International Journal of Engineering and Advanced Technology (IJEAT),* vol. 8, no. 4C, pp. 23-27, April 2019. [*Overlapping chapter 4*].

4. **Okikioluwa E. Oyedeji** and Viranjay M. Srivastava, "Effect of Radius on various Parameters of Cylindrical Surrounding Double-Gate (CSDG) MOSFET," *International Journal of Engineering and Technology, UAE (IJET),* vol. 7, no. 4, pp. 2127-2131, May 2018. [*Overlapping chapter 3*].

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

For the past 40 years, MOSFET size has been shrinking from microscale to nanoscale, which produces a high field activity in the semiconductor material [31]. This is made possible through scaling of the MOSFET device and generating a better result for the production of Very Large Scale Integrated (VLSI) circuit [4].

In this chapter, the MOSFET will be reviewed as researchers have contributed their own quota in improving its operation for suitable use. Also, the parameters involved in making it adequate for VLSI production will be discussed. Furthermore, it also discusses its limitations, and how it has revolved overtime to deal with these limitations through the invention of new structures.

2.2 Structure and Operation of MOSFET

The MOSFET gets its name from its structure and operation. The MOS is Metal on Oxide with a Semiconductor body which explains the structure and operation of the MOSFET as introduced earlier. The structure of a typical *n*-channel enhancement MOSFET with a semiconductor body of *p*-type material serves as the substrate with *n*-type semiconductor at the regions (n^+ source and n^+ drain). A growth of thin layer metal oxide is deposited on the surface of the *p*-type body of thickness less than *50 nm* and length spanning beyond the distance between the drain and the source [32]. This serves as an insulator between the contact and semiconductor body. Above the oxide, there is metal material that forms the gate electrode. Conducting contacts are mounted on the drain, source, and body, so that the device is equipped with four-terminal device namely gate, source, drain and substrate (body).

The substrate which is also known as body is connected to the source hereby making the semiconductor device a three-terminal device of Gate (*G*), Drain (*D*), and Source (*S*) [33].

Consider the *n*-channel enhancement MOSFET in Fig. 2.1, when the gate electrode is unbiased, there exists no connection between the source and drain. The source region and the *p*-type body form a *p*-*n* junction in series connection with the drain, and appear as a *p*-*n* junction with the body. Therefore, no connection exists between the drain and the source due to high resistance ($>100\ G\Omega$) [8, 34]. However, when the source and the drain are grounded with an appreciable amount of positive voltage applied at the gate-source terminal (V_{GS}), the holes (majority carriers) in the *p*-type body are repelled downward, while the electron (majority carriers) are attracted upward toward the metal oxide. The attraction of electrons from the body, coupled with attraction of electrons from the doped n^+ regions produces a pattern below the oxide between the source and the drain. This linear pattern is called the Channel. This *n*-channel is an inverted channel in a *p*-type body, and is referred to as the Inversion Layer. This is formed at a specific value of voltage (about 0.5 to $1.0\ V$) applied at the gate known as Threshold Voltage (V_{th}) [35].

The MOS -Metal gate, Metal oxide insulator and semiconductor substrate- forms a parallel-plate capacitor with the gate as the positive side, the substrate as the negative end of the capacitor due to the accumulation of electrons at the topmost part of the MOS and the gate oxide as the dielectric. Thus, a vertical electric field is formed in the MOS and controls the amount of charges that flow through the channel and likewise, determines the amount of current flow [36, 37]. With the formation of the channel, the application of a low positive voltage (about $10\ mV$) is applied at the drain-source terminal and causes current to flow. Since the channel is formed by the motion of electrons from the source to the drain, current (I_d) therefore flows in the direction opposite to the electrons flow, i.e. from drain to source. Hence, the amount of current flow is dependent on the magnitude of the electron, which also depends on the gate-source voltage (V_{GS}) [38]. When the V_{GS} is increased such that it exceeds the threshold voltage, V_{th}, ($V_{GS} < V_{th}$), effective voltage or overdrive voltage is achieved. Therefore, the drain current (I_D) is dependent on both the overdrive voltage ($V_{GS} - V_{th}$) and drain-source voltage (V_{DS}) [8].

Moreover, as the V_{GS} is kept constant and the drain current increases as electrons travel along the channel from the source to the drain. It is observed that V_{DS} ranges from $0\ V$ to the magnitude of V_{DS} respectively. Likewise, the magnitude of V_{GS} also decreases from the source to the drain, where V_{DS} is at maximum. The V_{GS} is reduced because of

the differences between the two voltages (V_{GS} - V_{th}). Due to this, the channel is distorted, as shown in Fig. 2.1, with its depth at the source is greater than that at the drain [38].

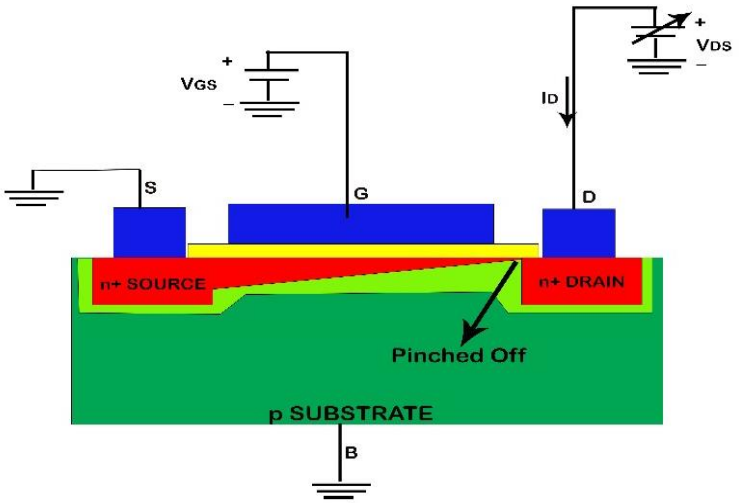


Figure 2.1 A pinched-off enhancement MOSFET with distorted n-channel [8].

As the drain-source voltage (V_{DS}) increases such that V_{GS} - V_{DS} is equal to V_{th}, the channel decreases to almost zero and it is being pinched off. Furthermore, an increase in the V_{DS} can cause breakdown to the device as it experiences more activities at the drain end of the MOSFET.

The pinch-off point explains the various regions in the operation of the MOSFET. The three regions – Saturation, Triode and Cut-off regions- with respect to Figure 2.2 is shown below:

The point beyond the pinched off is known as the Saturation region, which is when the drain-source voltage is greater than or equal to the overdrive voltage, mathematically shown in Eq. (2.1).

$$V_{DS} \geq V_{GS} - V_t \tag{2.1}$$

At this saturation point, current becomes constant even with further increase in the V_{DS}. However, just before saturation point is reached, the drain-source is less than the overdrive voltage. At this point, the MOSFET obeys the Ohm's law of increase in I_D as V_{DS} increases. It is called the Triode or Ohmic region and it is mathematically expressed as:

$$V_{DS} < V_{GS} - V_t \tag{2.2}$$

This is known as the triode region. The cut-off region is at the point when the gate-source voltage is just below threshold and at this point, there is no or fragment current activity in the MOSFET. These region characteristics help the MOSFET to be applicable as a switch.

When the gate voltage (V_{GS}) is applied, the holes in the *p*-type body are repelled and a conducting channel of electrons is formed just below the metal oxide. The coming together of *p*-type body and *n*-type channel beside each other leads to the concept of *p*-*n* junction diode. At this point, diffusion takes place when the holes in the *p*-type moves towards the n-type channel and likewise some electrons in the *n*-type channel diffuse toward the *p*-type part leaving behind negative immobile charges on the p-side and positive immobile charges at the *n*-side respectively. These immobile charges of both positive and negative charges between them form a space charge region where conduction does not take place [39].

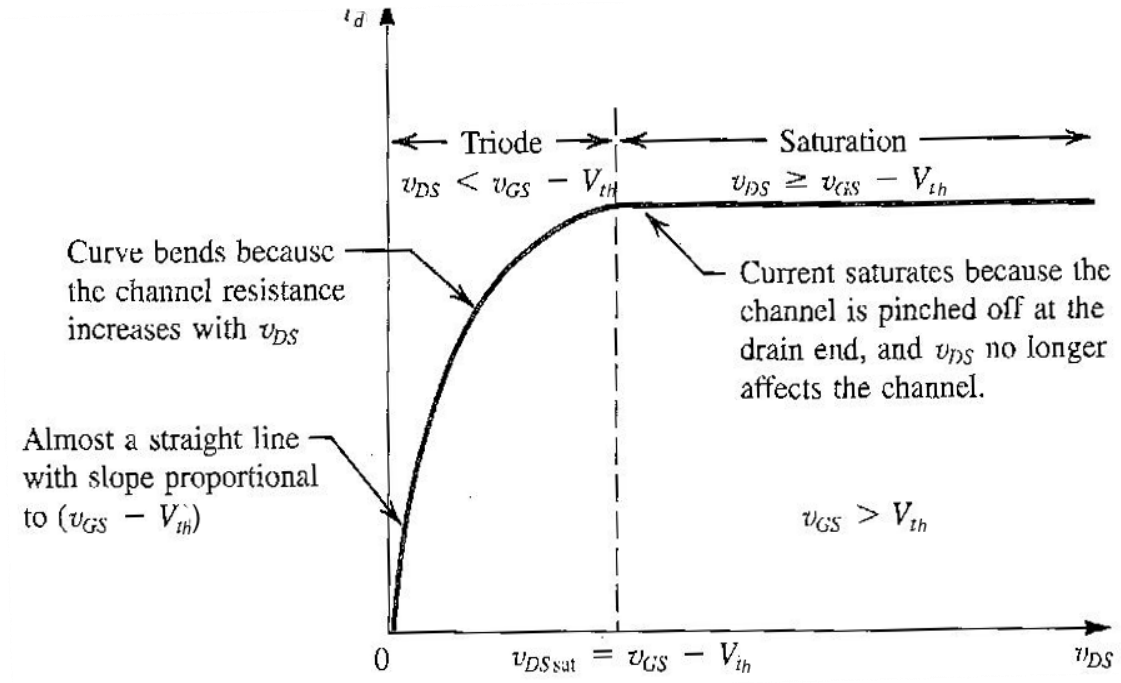


Figure 2.2 The Drain current vs. Drain-Source Voltage showing the regions of conduction [8].

2.3 Parameters of the MOSFET

From the structure of the MOSFET discussed in section 2.1, it is observed that a MOS transistor is synonymous to a MOS capacitor [40]. The gate electrode of the n-channel MOSFET is the positive part of the capacitor, the oxide part as dielectric and

channel, when gate voltage is applied as the negative end of the capacitor. Also, the structure is symmetrical, as one cannot differentiate the source from the drain with unbiased phenomenon, but when the gate voltage is applied to create the channel, the source is seen different from the drain. This is because the source becomes the origin of the electron, while the drain becomes the destination of the electrons.

The channel formed in between the source and the drain has a length represented by L and W is the channel width of the MOSFET as shown in the Figure 2.3. A phenomenon always used for design purpose using these two parameters is the ASPECT RATIO, which is the ratio of the channel width to channel length (W/L). Oxide between the gate and the semiconductor body has thickness represented by t_{ox}, the voltage applied at different part of the terminals are V_{GS}, V_{DS}, V_{BS} representing the gate-source voltage, drain-source voltage and bulk-source voltage respectively. These voltages have the source, which is usually connected with the body and grounded as the reference point, hence often referred to as gate-source voltage (V_{GS}), drain-source voltage (V_{DS}), and bulk-source voltage (V_{BS}).

However, in a biased state of the MOSFET, it is assumed that only current that flows in the device is the drain current (I_d) which is usually a function of $V_{GS,}$ V_{DS}, *and* V_{BS}. Although, when V_{GS} applied is less than the minimum gate voltage called the Threshold Voltage (V_{th}), the current flowing is the leakage current due to depletion charges [4].

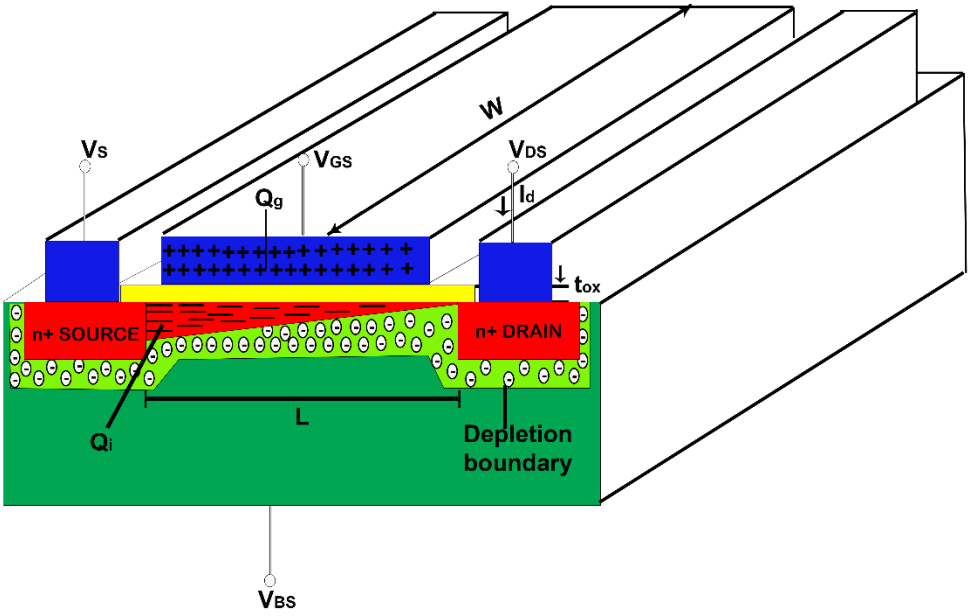


Figure 2.3 A 3-D Operational Description of the biased MOSFET [1].

2.3.1 Drain Current

To explain and increase the drain current in the MOSFET, many models have been introduced to bridge the designer ideas with the manufacturing world. The effectiveness of these models is verified through simulation to check the sustainability at different conditions. These models are based on the Gradual Channel Approximation (GCA), which explains that the electric field generated has two component fields with verification using two-dimensional Poisson's equation and show validity if assumption that the horizontal field component is much less than the vertical field component [41]. However, as saturation is reached the GCA is observed to be invalid. A few of these models are reviewed for proper background insight.

A. Simple Charge Control Model (SCCM)

In this model, GCA is assumed with a constant carrier mobility in a long channel MOSFET. Considering the magnitude of the free charge in the channel given as the product of the number of charges (n) and the carrier charges (q) with the dimension of the channel, the magnitude is given as:

$$|Q| = nq(LWH) \tag{2.3}$$

where L is the length, W is the width and H is the height of the channel in meters, and overdrive voltage ($V_{GS} - V_{th}$) is given as V_{Gt}. In this model, only drift current is considered. Integrating Eq. (2.3) above along the channel length gives:

$$I_d = \mu EW \left| Q' \right| \tag{2.4}$$

where E is the electric field, μ is the carrier mobility and Q' is the charge per unit area of the channel. The drain current for the SCCM is then given as [41]:

$$I_d = \frac{\mu W C_{ox}}{L} * \begin{cases} (V_{Gt} - \frac{V_{Gt}^{\ 2}}{2}) V_{DS} & \textit{Before or on saturation is reached} \\ \\ \frac{V_{Gt}^{\ 2}}{2} & \textit{When saturation is reached} \end{cases} \tag{2.5}$$

The C_{ox} is the capacitance per unit area of the silicon oxide, which is the insulator material used here. Considering the drain current in the model with the current-voltage characteristics that it generates, it becomes easy to find the trans-conductance which is the change in the drain current to the change in the gate-source voltage where the drain-source voltage is kept constant and mathematically given as:

$$g_m = \left.\frac{\Delta I_d}{\Delta V_{GS}}\right|_{V_{DS}} = \begin{cases} \beta V_{DS} & \textit{Before or on saturation} \\ \beta V_{Gt} & \textit{After saturation} \end{cases} \tag{2.6}$$

where β is the transconductance parameter given as $\mu WQ'/L$. One of the shortcomings of this model is that it is applicable mostly for micrometres scale. This shortcoming also influence the introduction of other models to fill in for the open gaps of the model [42].

B. Meyer Model (MM)

The Meyer model considers both the depletion and inversion layer with respect to Gauss' law and assumption that both the semiconductor body with the source are grounded [43]. The charge per unit area in this model is the sum of the depletion charge density (q_d) and the inversion charge density (q_i), that is:

$$q_s = q_d + q_i \tag{2.7}$$

Also in the model, the carrier mobility is assumed to be constant along the channel and on substituting the charge per unit area into Eq. (2.4), the drain current at non-saturation gives:

$$I_d = W\mu C_{ox}\left\{(V_{GS} - V_{FB} - 2\psi_b - \frac{V_{DS}}{2})V_{DS} - \frac{1}{2}\frac{\sqrt{2nq\varepsilon_s}}{3C_{ox}}\left[(V_{DS} + 2\psi_b)^{3/2} - (2\psi_b)^{3/2}\right]\right\} \tag{2.8}$$

where V_{FB} is the flat-band voltage, ψ_b is the quantity that characterizes the semiconductor body, ε_s is the semiconductor permittivity, q is the charge of the electron

and *n* is the concentration of the electron. With the simplicity and almost accurate predictive attribute of this model in simulations, it is still insufficient in predicting correct capacitance in MOS charge pumps, Dynamic memory circuits and capacitance circuit [44].

C. Velocity Saturation Model (VSM)

The previous two models have been introduced with respect to a long channel MOSFET and the assumption that the velocity of the carrier converges when it is almost at pinch-off does not have a proper background explanation. Rather, it is better to describe the drain saturation current with respect to the drift velocity when the vertical electric field generated is high and close to the drain [45], that is the drift velocity is:

$$\upsilon_d = \begin{cases} \mu E & \textit{For low Electric field before saturation} \\ \\ \upsilon_s & \textit{For high Electric field at saturation} \end{cases} \tag{2.9}$$

where the electric field (*E*), *dV/dL* is the vertical electric field in the channel of length *L*, while the υ_s is the velocity at saturation. *Sodini et. al*. [46] proposed a more accurate expression for an n-channel enhancement MOSFET in:

$$\upsilon_d = \begin{cases} \dfrac{\mu E}{1+\dfrac{E}{2E_s}} & \textit{for } E < 2E_s \\ \\ \upsilon_s & \textit{for } E \geq 2E_s \end{cases} \tag{2.10}$$

where E_s is the saturation electric field (υ_s/μ), Eq. (2.9) can be used to derive the voltage-current characteristic for the two previous models (SCCM and MM) as they will have the same non-saturation characteristics but in term of $E_s = E(L)$ with a little idea from SCCM, the VSM was derived to get the drain current at both non-saturation and saturation state [46].

$$I_d = \frac{W\mu C_{ox}}{L} * \begin{cases} V_{Gt}V_{DS} - {V_{DS}}^2/2 & \textit{for on or before saturation is reached} \\ (V_{Gt} - V_{DS_{SAT}})V_L & \textit{for after saturation} \end{cases} \quad (2.11)$$

where

$$V_{DS_{SAT}} = V_{Gt} - V_L\left[\sqrt{1+(V_{Gt}/V_L)^2} - 1\right] \quad (2.12)$$

This model finds its relevance in short channel length because with a parameter of *3 V* threshold voltage *0.08 m^2/Vs* for carrier mobility and saturation velocity below *100 m/s*, the effect of velocity saturation may be negligible for a length of *2.4 µm*, hence making it useful in sub-nanotechnology.

2.3.2 Surface Potential

Taylor [47] analysed the surface potential of the MOSFET by using the charge sharing model with the conduction band edge. The work set boundary for depletion between when the surface potential is zero (flat-band condition) and when the surface potential is doubled Fermi potential ($2\phi_F$). Thus, assumption was made that the surface potential is expected to vary logarithmically along the conducting channel with respect to the gate voltage to determine suitable subthreshold current using the set range. Nevertheless, this analysis was limited as the gate oxide dimension was not considered and the expected logarithmic variation was questionable as the variation was exponential. *Ng et. al.* [48] also analyzed the scalability of the MOSFET considering the SCE. The work gave attention to gate oxide and improved on the variation along the channel length with assumption of Gaussian rule using empirical expression to determine the surface potential among other parameters. But the work did not explain its expression analytically, it seems to be based on the assumptions to improve previous models.

Toyabe et. al. [49] initiated the polynomial potential model that served as background study for many researchers. This model utilizes the 2-D Poisson's equation where the vertical component x is assumed to be zero, and the surface potential is considered with respect to the horizontal component *y*, making it an ordinary differential equation as illustrated in Fig. 2.4.

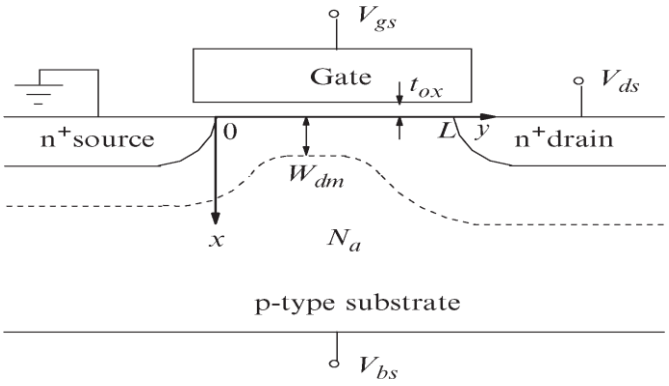


Figure 2.4 Analysis of n-channel MOSFET using polynomial potential model [50].

$$\frac{\partial^2\psi(x)}{\partial x^2}+\frac{\partial^2\psi(y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}N_a \tag{2.13}$$

Taking the boundary to be between $x = 0$, and the maximum depletion depth, W_{dm} and the boundary y to be along the conducting channel, and then it is assumed that:

$$\frac{\partial\psi}{\partial x}(W_{dm},y)=0 \tag{2.14}$$

Considering the boundaries:

$$V_{GS}-V_{FB}-\psi(0,y)=V_{ox}=-t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\partial\psi}{\partial x}(0,y) \tag{2.15}$$

When x = 0, and at x = W_{dm}:

$$\psi(W_{dm},y)=V_{BS} \tag{2.16}$$

Differentiating Eq. (16) w.r.t along vertical axis gives:

$$\frac{\partial\psi}{\partial x}(W_{dm},y)=0 \tag{2.17}$$

Substituting Eq. (14), Eq. (15), and Eq. (16) into Eq. (13) gives

$$\frac{\partial^2 \psi_s}{\partial y^2} - \left[2 / l_{oa} \right]^2 \psi_s = A_0 \tag{2.18}$$

where A_o is a constant constituting V_{BS}, $V_{GS} - V_{FB}$ and qNa/ε_s and l_{oa} is also a constant representing:

$$l_{oa} \sqrt{\frac{2\varepsilon_{si} t_{ox}}{2\varepsilon_{ox} W_{dm} + 3\varepsilon_{si} t_{ox}}} W_{dm} \tag{2.19}$$

From Eq. (2.18), surface potential can be derived as:

$$\psi(y) = (\psi_{bi} - A_1) e^{-2y/l_{oa}} + (\psi_{bi} + V_{DS} - A_1) e^{2(y-L)/l_{oa} + A_1} \tag{2.20}$$

Which satisfies the boundary conditions along the y-axis [51]. However, as comprehensive as the model is, there are some observed limitations. Firstly, the model is assumed to have used the 2-D Poisson equation, but Eq. (2.14) above does not satisfy that. Secondly, the gate-oxide does not have any 2-D Poisson equation. It is because the vertical component in the electric field is assumed as a constant and the derivative of constant is zero, making it a 1-D Poisson equation.

Due to previous attempts to solve the problem of SCE and analyse surface potential in MOSFET, *Ratnakumar et. al.* [52] proposes an analytical model for the 2-D Poisson's equation using the following boundaries.

$$\psi(0, y) = \psi_s(y) \tag{2.21}$$

$$\frac{\partial \psi}{\partial x}(W_d, y) = 0 \tag{2.22}$$

$$\psi(x, 0) = \psi_{bi} \tag{2.23}$$

$$\psi(x, L) = \psi_{bi} + V_{DS} \tag{2.24}$$

Here, the surface potential is assumed to be constant at every point along the conducting channel from y = 0 to y = L [53-56]. Also, the 2-D Poisson equation for surface potential was derived to be:

$$\psi(x,y)=\psi_{s0}\left(1-\frac{x}{W_d}\right)^2+\sum_{n=0}^{\infty}\frac{\sin\left(\frac{(2n+1)\pi x}{2W_d}\right)}{\sinh\left(\frac{(2n+1)\pi L}{2W_d}\right)}* \left[A_n\sinh\left(\frac{(2n+1)\pi(L-y)}{2W_d}\right)+B_n\sinh\left(\frac{(2n+1)\pi y}{2W_d}\right)\right] \tag{2.25}$$

It is observed that some assumptions from the polynomial potential model were integrated into this model. However, this model is limited in its unrealistic assumption of constant boundary conditions for the surface potential. Also, the length of the conducting channel has a long variation in the surface potential [55-57].

2.4 Double-Gate (DG) MOSFET

The need for scaling in MOSFET has brought many advantages, which include smaller dimension as well as improved performance. These advantages are essential properties for usage in Very Large Scale Integrated (VLSI) and Ultra Large Scale Integrated (ULSI) circuit.

Notwithstanding, they come with a great challenge, Short Channel Effects (SCEs). This effect necessitated the need for improving the characteristics and operation of MOSFET, which resulted in a new multi-interface structure Double-Gate Metal Oxide Semiconductor Field-Effect Transistor (DG MOSFET). *Angsuman et. al.* [58] using the proposed DG MOSFET explains the structure and operation of the DG MOSFET.

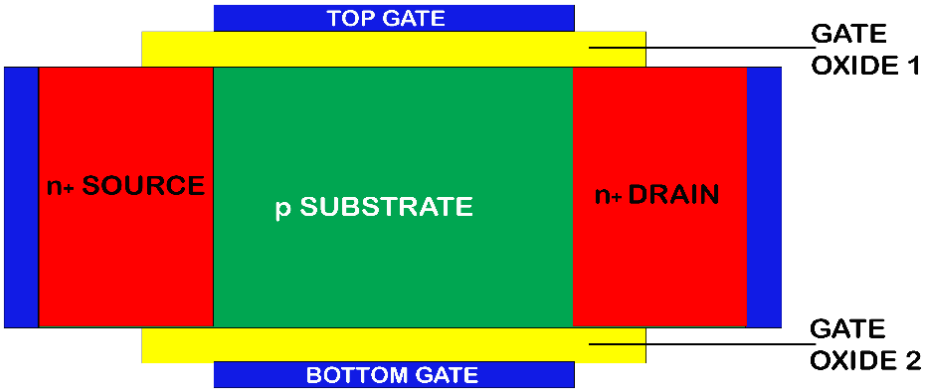


Figure 2.5 An n-channel DG MOSFET [58].

The DG MOSFET is an extension of the SG MOSFET as shown in Fig. 2.5, advanced with the aim of having two conducting channels of small width which is controllable by the two gates at both the upper and lower parts of the substrate. It is best described as a Silicon substrate sandwiched between two gate oxides that serve as an insulator to two gates. This will produce two channels in operation activated by either of the two gates.

The DG MOSFET has more advantages with the scalability enhancement and greater control of the gates in the operation in the channel. Also, the DG MOSFET has higher immunity to the short channel effect; hence, a better application due to its great current drive [58]. The essence of the double-gate is to have full control of the activities in the channel. When voltage is applied independently at the gate, due to the thickness of the silicon substrate, it is observed that two channels are formed close to both sides of the gate. The two channels formed at both the top and the bottom substrate are being separated to show the independence in their activities which gives rise to two separate transistors in which each gate controls the electrostatics activities. With the formation of the two channels, there is a better carrier mobility activities compared with the Single-Gate MOSFET (SG MOSFET) [4].

The DG MOSFET utilises a larger drain/source width rather than the conventional heaving doping of the region, which alters the Si substrate configuration and results to punch through effect [59]. This approach produces a more controlled SCE and increased mobility which makes it applicable for VLSI circuit. This configuration of the DG MOSFET also helps to reduce both the gate leakage and sub-threshold leakage [60]. This is made possible even with greater current drive than the SG MOSFET with the same properties. Also, due to the position of the two gates around the substrate, every part of the channel has reachable control by the gates with a controlled electric field which determines the flow of current in the channel. Hence, it makes the DG MOSFET operate at lower voltage with less power consumption [58, 61]. This configuration has also proven to be characterised with lower threshold voltage but higher transconductance and speed [62, 63].

Frank et. al. [64, 65] utilises Monte-Carlo simulations to observe the operation of the DG MOSFET in the limited scaling behaviour. It was discovered that the DG MOSFET with gate length of *30 nm* have greater performance with higher transconductance characteristics. It was also observed to have better performances in

digital circuitry. *Solomon et. al.* [66] employed the scaling variation in the DG MOSFET and observed the mobility performance of the silicon body ranging from about *10 nm* (*~10 nm*) down to about *5 nm*. In their work, it was discovered that mobility gets better and can be maintained at that range. Fig. 6 above shows the schematic diagram of the DG MOSFET.

However, there are two types to this structures [42]:

A. Symmetric DG MOSFET that possesses identical gate material which controls the channel with equal oxide thickness.

B. Asymmetrical DG MOSFET that has two unequal oxide thickness control by two gates with different flat band and biases.

Both DG MOSFET types are effective but in the symmetrical device, different parameter strength could be derived from both gates which help to improve performance of the transistor as well as reduce power consumption [67].

2.4.1 Symmetric DG MOSFET

The symmetric DG MOSFET has a similar work function attribute of their gates. Also, the uniform channels are active with the same amount of gate voltage. Fig. 2.6 shows the energy band of an undoped symmetrical DG MOSFET both at no voltage applied at the gate and at when the gate voltage is equal to the threshold voltage.

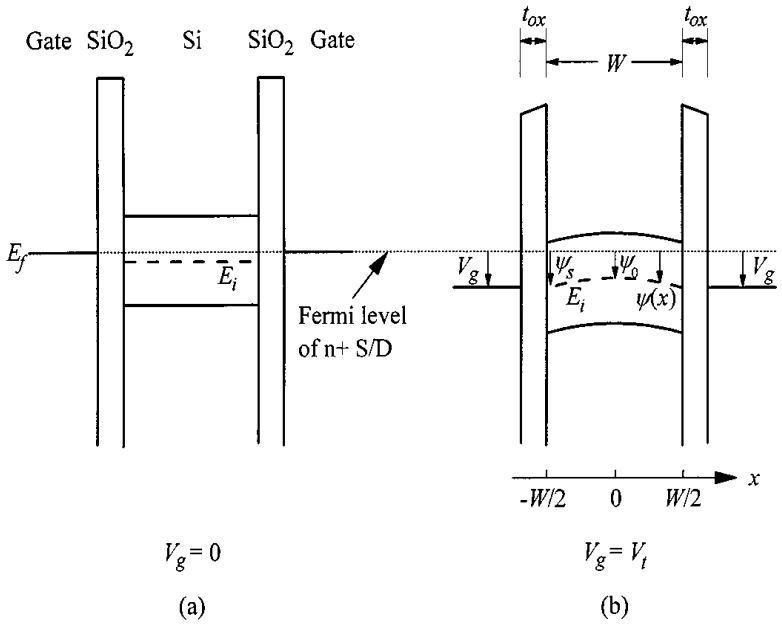


Figure 2.6 Diagram of the Energy band of an undoped, symmetric DG MOSFET at (a) no gate voltage and (b) at threshold voltage [68].

Taur et. al. [68-70] proposed a 1-D analytical solution to a lightly doped or undoped symmetric DG MOSFET using a mobile charge to the Poisson equation. Using Fig. 2.6, the Poisson equation with reference to the mobile charge density is given as:

$$\frac{\partial \psi^2(x)}{\partial x^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q(\psi - V)}{kT}} \tag{2.26}$$

where $\psi(x)$ is the electrostatic potential, V is the electron quasi-Fermi potential, n_i is the intrinsic carrier density, q is the charge and ε_{si} is the permittivity of the Silicon. Double integration of Eq. (2.26) gives:

$$\psi(x) = V - \frac{2kT}{q} In\left[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}\cos\left(\frac{2\beta x}{t_{si}}\right)\right] \tag{2.27}$$

where β represents the boundary conditions, which was further used to derive the current condition using Pao-Sah integration:

$$I_d = \mu\frac{W}{L}\int_0^{V_{DS}} Q_i(V)dV = \mu\frac{W}{L}\int_{\beta_s}^{\beta_d} Q_i(\beta)\frac{dV}{d\beta}d\beta \tag{2.28}$$

The β_s and β_d represent the boundary conditions at zero voltage and at $V = V_{DS}$. The Q_i is known to be equal to $2\varepsilon_{sin}(2kT/q)(2\beta/t_{si})tan\beta$ from Eq. (2.27) using Gauss's law. The drain current then becomes:

$$I_d = \mu\frac{W}{L}\frac{4\varepsilon_{si}}{t_{si}}\left(\frac{2kT}{q}\right)^2\left[\beta\tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\beta^2\tan^2\beta\right]_{\beta_d}^{\beta_s} \tag{2.29}$$

With this formula, the work was able to validate the drain current of the symmetric DG MOSFET at saturation, linear and subthreshold region [71]. This analysis however ignored some physical effects like SCE, quantum effect and mobility model.

2.4.2 Asymmetric DG MOSFET

Its gates have different work function and the gates are biased with different gate voltage. Figure 2.7 shows the energy band diagram of the asymmetric DG MOSFET.

Lu et. al. [71] extended the analysis of *Taur et. al.* [4, 68-70] by considering when the drain voltage is not equal to zero, while applying the quasi-Fermi potential. It was discovered from the analysis that the Poisson equation is similar to that of symmetric, only that there were two boundary conditions due to different oxide interfaces.

$$\varepsilon_{ox}\frac{V_{GS}-\Delta\varphi_1-\psi_{s1}}{t_{ox}}=-\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=\frac{-t_1}{2}}\equiv\varepsilon_{si}E_1 \tag{2.30}$$

$$\varepsilon_{ox}\frac{V_{GS}-\Delta\varphi_2-\psi_{s2}}{t_{ox}}=-\varepsilon_{si}\left.\frac{d\psi}{dx}\right|_{x=\frac{-t_2}{2}}\equiv\varepsilon_{si}E_2 \tag{2.31}$$

The E_1 and E_2 are the electric fields generated at both side of the gates $\Delta\varphi_1$ and $\Delta\varphi_2$ are the work functions of the conducting channels. This generates a surface potential of:

$$\psi(x)=V-\frac{2kT}{q}In\left[\frac{t_{si}}{2\beta}\sqrt{\frac{q^2n_i}{2\varepsilon_{si}kT}}\sin\left(\frac{2\beta x}{t_{si}}+\alpha\right)\right] \tag{2.32}$$

The α and β are the boundaries of the ADG MOSFET. This analysis shortcoming is that the SCE and mobility were not considered.

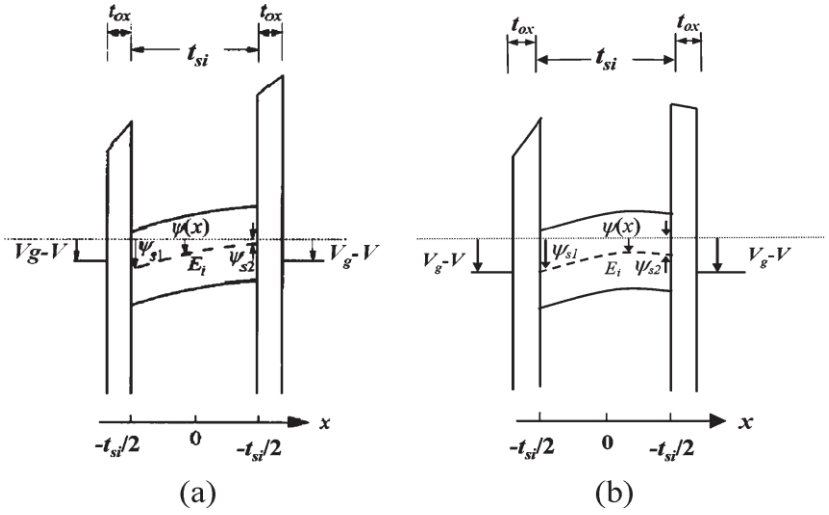


Figure 2.7 Diagram of the Energy band of an asymmetric DG MOSFET at (a) low V_{GS} – V and (b) high V_{GS} –V [71].

2.5 Cylindrical Surrounding Gate (CSG) MOSFET

The DG MOSFET with an undoped drain/source region is an encapsulation of better performance and greater application in nanoscale region. The dynamism of controlling the gate differently to achieve desired goal conveys a great deal of the transistor. The MOSFET is not rigid in its structure as it allows for different topology to achieve greater current and better performance records. However, all these different structures come with different advantages and drawbacks, nevertheless, its usefulness for different purposes cannot be overemphasized. To derive solutions to the challenges of Bulk SG MOSFET explained in section 2.2.2 and achieve higher drain current, different structural dimensions with additional gates, such as FinFET, Gate-All-Around (GAA), Surrounding-Gate MOSFET, among others have been introduced [72]. Yet, a better solution with these limitations as it includes the thermal effect is the Cylindrical Surrounding-Gate MOSFET (CSG); this is the fabrication of a hollowed pole-like Silicon substrate with its controlling gate around it. This structure has promising package of better current drive, reduced subthreshold characteristics and reduced thermal effects. The structural density also makes it useful in VLSI circuits as billions of the structure can be packed for sophisticated functions.

The gates surrounding the substrate body have better electrostatic control of the activity at the channel than ordinary DG MOSFET, and thus SCE is highly reduced. The circumference of the gate round the structure also reduces the body effect in the operation of the MOSFET [73]. Also, the classical SG and DG MOSFET have corner effect due to the several edges in their structures. These edges accommodate parasitic currents which are inexpedient in the operation of the MOSFET.

Hou et. al. [74, 75] have analyzed this corner effect and its distorted effect on achieving better performance not only in classical SG and DG MOSFET but also in GAA MOSFET. However, in the cylindrical structure shown above, corner effects are being overcome while still retaining the characteristics of better current drive, greater electrostatics control of the channel and better application purpose. *Iniguez et. al.* [76] developed a unified charge control model for the CSG MOSFET. This model was based on the charge density at the two ends of the channel (source and drain) to generate a charge current flowing in the channel. *Yu et. al.* [77] also, without using sheet approximation, proposed the Ward-Datton Charge partition method derived from Poisson's equation to get the analytical function of the CSG MOSFET.

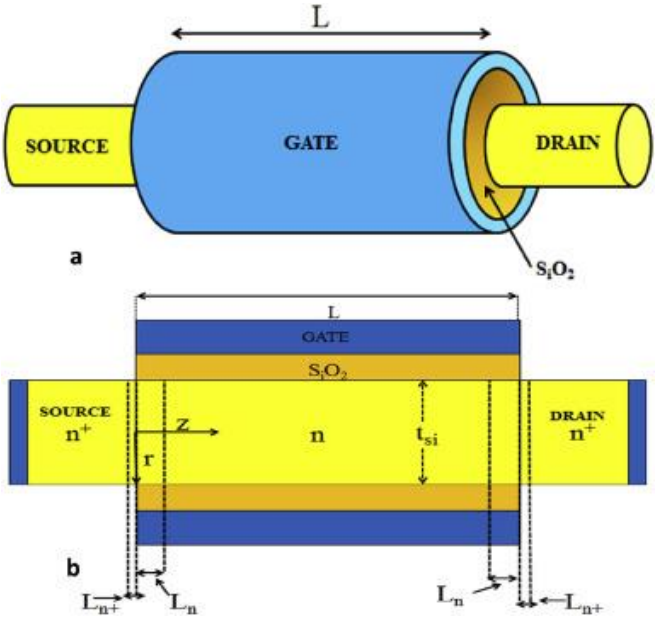


Figure 2.8 A structured Cylindrical Surrounding Gate (CSG) MOSFET [78].

However, all these models are based on highly doped or fairly doped channel. This is because of the lack of dopant atom at the channel gives rise to low mobility of the charge and reduced scattering which result to poor current-ON (I_{ON}) characteristics. These models have been based on high dopant channel in order to reduce SCE and increase current drive, but it has degraded the charge mobility [51]. Attempt to overcome this mobility challenge is decreasing the gate oxide thickness to a very thin layer and this resulted back to the punch-through limitation.

Also, the application of CSG is dependent on compact models as other MOSFET structure (SG and DG) that utilises the charge sheet approximation is not compatible with it at various inversion stages. This shows that more work is needed to be done on the structure, which resulted into a new structure in Cylindrical Surrounding Double-Gate (CSDG) MOSFET as an advancement to CSG and its based on unified charge control model [79].

Gupta and Srimanta [80] further proposed a model for the analysis of surface potential, drain current and threshold voltage for the CSG MOSFET. This model considered some fringing gate capacitance effects after first analysing the core model. The work made assumption on a uniform impact of the charge carrier and a fixed gate-oxide charges on the device, a 2-D Poison equation was analysed with respect to the

vertical axis due to its parabolic potential. With the consideration of the effect of the fringing gate capacitance, the surface potential, drain current as well as threshold voltage were analysed. The drain current was expressed after integrating along the channel of the CSG with consideration with the internal and external boundaries at zero voltage from the source as:

$$I_d = \frac{\pi R^2}{L} q\mu n_i \exp\left(\frac{\psi_s}{V_{th}}\right) V_{th}\left[1-\exp\left(\frac{-V_{DS}}{V_{th}}\right)\right] \tag{2.33}$$

where R and q are the radius of the device and the carrier charge respectively, while μ and n are the carrier mobility and the number of charges. However, in this model, the quantum effect on the devices scaled to radius below *10 nm* is not compatible. Also, there was an assumption of uniform impurity density charge carrier influence along the conducting channel which might not be effective at different inversion regions.

2.6 Cylindrical Surrounding Double-Gate (CSDG) MOSFET

These challenges gave rise to a cylindrical structure but with two gates (CSDG) proposed and developed by *Srivastava et. al.* [81]. This device is proven to have two scaled channel path that reduces parasitic effect in the device [82]. The structural dimension of the device is also of great significance because it has little contact on the board(s) on which it is mounted. This helps to reduce heat and with little effort from heat sink, the device promises to provide long-lasting operations [83]. The structural density also makes it useful in VLSI and ULSI circuits as billions of the structure can be packed for sophisticated functions. That work confirmed that the source to drain capacitance in the CSDG MOSFET is higher than the CSG MOSFET and hence making the drain current operational area larger in CSDG MOSFET. This also makes the stored energy to be almost double the CSG MOSFET and attributes to increased current flow than the SG MOSFET and DG MOSFET. Nevertheless, there is need to improve on the structure not only to overcome SCE, but for increased current drive and better carrier mobility.

Unlike the CSG, the CSDG MOSFET has two gates that control the two channels around the cylindrical substrate. The main idea to the invention is to perfectly control the channel with the application of two thin gate oxide with small width. This approach is to adequately reduce corner effect and SCE and in turn produce higher drain current when

compared with the CSG and the DG MOSFET. In addition, the circular coverage of the gate helps beyond the channel control and also reduces the sub threshold slope [81]. Besides, a similar structure like the CSDG MOSFET is the Gate-All-Around with structure shown in Fig. 2.9.

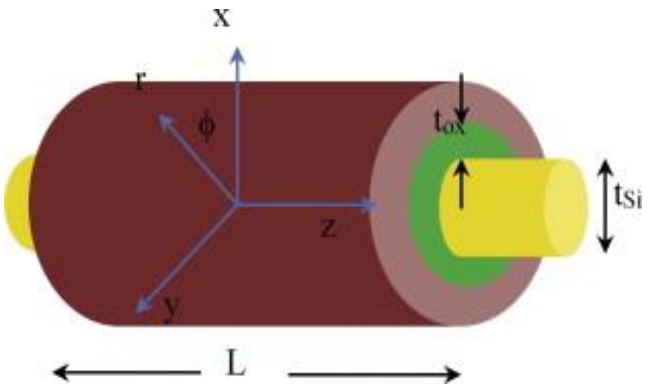


Figure 2.9 A schematic structured of Gate-All-Around (GAA) MOSFET [73].

The GAA is characteristised with uniformly doped conducting channel of about $1x10^{16}\ cm^{-3}$ surrounded by the gate with a protruding drain and source regions. The GAA has a magnificent control over the conducting channel due to the gate around the conducting channel and hence, the reduced SCE.

With this advantage, *Kumar et. al.* [73] have proposed a simple analytical model for the GAA using the cylindrical coordinate of the 2-D Poisson equation to prove that the threshold voltage is more precise than the surface potential. The research work also proposed the mathematical analysis of the potential distribution along the conducting channel as:

$$\psi(z) = A\exp\left[\sqrt{\frac{4}{\lambda}}z\right] + B\exp\left[-\sqrt{\frac{4}{\lambda}}z\right] + \left[V_{GS} - V_{FB} - \frac{\lambda qNa}{4\varepsilon_{si}}\right] \tag{2.34}$$

where λ, A, and B are mathematical representations:

$$\lambda = t_{si}{}^{2}\left[1 + \frac{2\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\right] \tag{2.35}$$

$$A = \left[\frac{\left[V_B - \left(V_{GS} - V_{FB} - \frac{\lambda qNa}{4\varepsilon_{si}} \right) \right] \left[1 - \exp\left(-\sqrt{\frac{4}{\lambda}} z \right) \right] + V_{DS}}{\exp\left(\sqrt{\frac{4}{\lambda}} L \right) - \exp\left(-\sqrt{\frac{4}{\lambda}} L \right)} \right] \tag{2.36}$$

$$B = -\left[\frac{\left[V_B - \left(V_{GS} - V_{FB} - \frac{\lambda qNa}{4\varepsilon_{si}} \right) \right] \left[1 - \exp\left(-\sqrt{\frac{4}{\lambda}} z \right) \right] + V_{DS}}{\exp\left(\sqrt{\frac{4}{\lambda}} L \right) - \exp\left(-\sqrt{\frac{4}{\lambda}} L \right)} \right] \tag{2.37}$$

However, the GAA cannot adequately be utilised in nanotechnology because it has limitation in scalability. This is due to continuous reduction of the gate oxide dimension, and can result into tunnelling and hot-carrier effect. Also, due to a single gate attribute, the GAA has limited lower control over the conducting channel unlike the DG MOSFET.

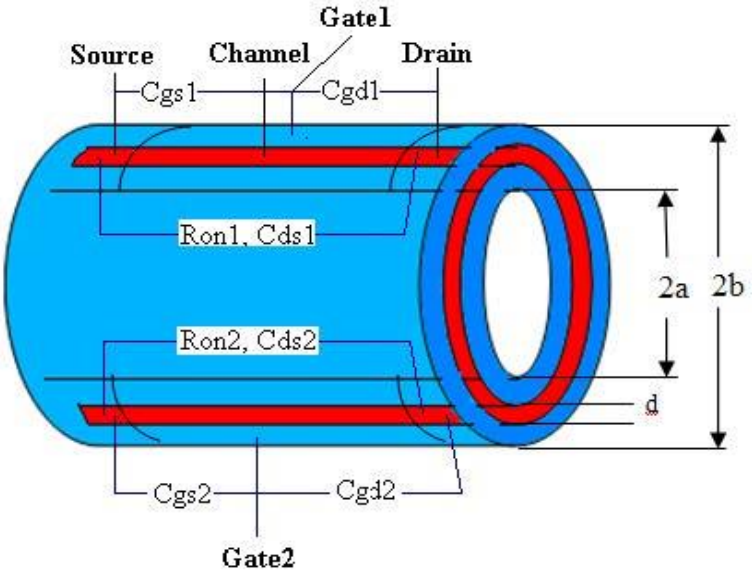


Figure 2.10 Simplified CSDG MOSFET device [81].

However, the CSDG MOSFET makes use of undoped body unlike all other GAA MOSFET. Although, it has been analyzed that doping the channel in a MOSFET can suppress the SCE and reduce the threshold voltage, it also reduces mobility and decrease current drive [81]. The CSDG MOSFET with its undoped body increase mobility of the charge as depletion charges which add to the activities of the electric field is overcome.

Also, the effect of doping is avoided because it causes fluctuation in threshold voltage and operation of the devices.

Srivastava et. al. [84] confirmed that the source to drain capacitance in the CSDG MOSFET is more when compared with the CSG MOSFET and hence making the drain current operational area larger in CSDG MOSFET. This also makes the stored energy to be almost double the CSG MOSFET and attributes to increased current flow than the SG MOSFET and DG MOSFET.

The CSDG is designed by rotating the DG MOSFET in a circular pattern with respect to one of the gate, producing a circular structure. The structure is such that the reference gate is the internal gate while the other gate is the external gate as shown in Figure 2.10.

Verma et. al [85] introduce an improved structure of the CSDG MOSFET in comparison with the CSG MOSFET. The design shown in Fig. 2.11 is characterised by the channel length and radius of *22 nm* and *5 nm*, respectively. This design is different from the previous architectural design and parameter notable due to the removal of the hollow. This modification was employed due to its analysis for future nanotechnology application.

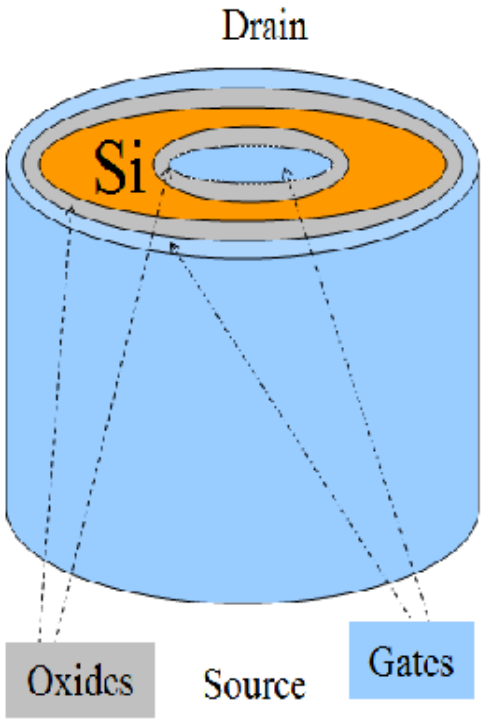


Figure 2.11 The Schematic design of the CSDG MOSFET [85].

Srivastava et. al. [86, 82] have proposed the drain current using Pao-Sah integral for the internal and external regions of the CSDG MOSFET is calculated as:

$$I_d = \mu \frac{2\pi a}{L} \int_0^{V_{DS}} (V) Q_1 dV + \mu \frac{2\pi b}{L} \int_0^{V_{DS}} (V) Q_2 dV \tag{2.38}$$

where Q_1 and Q_2 are the charge densities for the internal and external regions of the CSDG MOSFET. Applying Gauss's law makes the charge density to be expressed as:

$$Q_1 = -C_{ox1}(V_{GS} - \Delta\varphi - \psi_{\text{int}}) \tag{2.39a}$$

$$Q_2 = -C_{ox2}(V_{GS} - \Delta\varphi - \psi_{\text{ext}}) \tag{2.39b}$$

Bairagya et. al. [82] integrated Eqs. (2.32a) and (2.32b) to produce an analytical expression:

$$\begin{aligned} I_d = {} & \mu \frac{2\pi a}{L} \left[\frac{-qn_i^2}{NaE(a)} \right] \left[\frac{kT}{q} \right]^2 \left[e^{\frac{q\psi_{s1}}{kT}} - e^{\frac{q\psi_0}{kT}} \right] \left[1 - e^{\frac{qV_{DS}}{kT}} \right] + \\ & \mu \frac{2\pi b}{L} \left[\frac{-qn_i^2}{NaE(b)} \right] \left[\frac{kT}{q} \right]^2 \left[e^{\frac{q\psi_{s2}}{kT}} - e^{\frac{q\psi_0}{kT}} \right] \left[1 - e^{\frac{qV_{DS}}{kT}} \right] \end{aligned} \tag{2.40}$$

This expression is valid for an asymmetrical form of CSDG MOSFET with different work functions for both internal and external structure. Analysing the surface potential for the CSDG MOSFET by *Sood et. al.* [87] with the assumption of the Gradual Channel Approximation (GCA) is expressed as:

$$\frac{\partial^2 \psi}{\partial r^2} + \frac{1}{r} \frac{\partial \psi}{\partial r} = \frac{q^2 n_i}{\varepsilon_{si} kt} e^{q(\psi - V)/kT} \tag{2.41}$$

where r and q represent the radius of the cylindrical device and the electron charges flowing, V and n_i represent the quasi-Fermi potential and the intrinsic concentration of the silicon. *Sood et. al.* [87] applied transformation for Eq. (2.34) to simplify the equation and was expressed as:

$$\psi(r) = A - \frac{2kT}{q} In\left[1 - \left(\frac{q^2 n_i r^2}{\varepsilon_{si} kt} e^{q(\psi - V)/kT}\right)\right] \tag{2.42}$$

However, there is need for an improved drain current and surface potential analytical expression among other parameters to be considered for the improved structured CSDG MOSFET. These and other parameters will be considered in the next chapter with simulations to verify its authenticity.

2.7 Conclusion

This chapter reviewed the structure and operation of the MOSFET. The way the device get the name from structure and operation, The MOS structure implying Metal Oxide Semiconductor, while its characteristics of utilizing field-effect operation affirms its name. The way the structure affects the operation when it is biased with the MOS - Metal gate, Metal oxide insulator and semiconductor substrate- forming a parallel-plate capacitor with the gate as the positive side, the substrate as the negative end of the capacitor due to the accumulation of electrons at the topmost part of the MOS and the gate oxide as the dielectric. With the formation of the channel, the application of a low positive voltage (about *10 mV*) applied at the drain-source terminal and causes current to flow. Hence, the channel is formed by the motion of electrons from the source to the drain, current (I_d) therefore flows in the direction opposite to the electrons flow, i.e. from drain to source. The amount of current flow is dependent on the magnitude of the electron, which also depends on the gate-source voltage (V_{GS}). But when the V_{GS} is increased such that it exceeds the threshold voltage, V_{th}, ($V_{GS} < V_{th}$), effective voltage or overdrive voltage is achieved. Therefore, the drain current (I_D) is dependent on both the overdrive voltage ($V_{GS} - V_{th}$) and drain-source voltage (V_{DS}). The various regions; saturation, triode and cut-off were explained, as the point beyond the pinched off is known as the Saturation region, the point where the MOSFET obeys ohm's law as Triode region and below that as Cut-off region. Furthermore, the drain current and surface potential was discussed. The SCCM with its assumptions was reviewed to explain the drain current as a parameter of the MOSFET. In addition, the Meyer model analysed the drain current with respect to the depletion and inversion layer. However, one of the shortcomings is that it is not applicable in nanoscale but the assumptions could

be employed to fulfil the aim of this research work. The DG MOSFET was also reviewed as it was introduced to overcome some of the challenges posed by the SG MOSFET. The types of DG MOSFET; symmetric and asymmetrical were discussed and their relevance to a better operation of the device were also discussed. Furthermore, the CSG was discussed as an improvement to better performance with the introduction of the recent structures which this work is based on, CSDG. In summary, the chapter reviewed the different structures of MOSFET with their theories with the intention to propose a new structure to overcome the challenge of MOSFET, of which heat is inclusive. The undoped body characteristics and other features of the structure make the aim of this study worth achieving.

CHAPTER 3
PARAMETRIC ANALYSIS OF CSDG MOSFET

3.1 Introduction

The Double-Gate (DG) MOSFET) have been reviewed in previous chapter and acknowledged to be a better device than the conventional SG MOSFET. This is because of its ability to adequately control the SCE, which restrict the almost perfect operation and performance of the MOSFET. This fact makes this dual-gate MOSFET model to fabricate the CSDG MOSFET that best suit overcoming the challenges of noise, heat and various other challenges facing the nanotechnology devices.

The CSDG MOSFET has the ability of efficient control over the conducting channel even with small dimension of the undoped channel widths due to its double gate. Also, since the larger the conduction width, the larger the threshold voltage [88]. This device operates with low threshold voltage and increased drain current. In addition, due to lack of instability caused by doping effect, this device enjoys the advantage of reduced threshold voltage, increased drain current, and enhanced mobility due to its undoped characteristics and thin gate oxides. Furthermore, the cylindrical structure help to overcome gate alignment and reduces heat effect due to less contact area with the chip. The choice of this improvement requires the analysis of its parameters like drain current, transconductance, surface potential, carrier mobility, and capacitive characteristics. This chapter deals with these parameters including the verification through simulation.

3.2 Structure of the CSDG MOSFET

The CSDG MOSFET is an extension of DG MOSFET. This design is equivalent to two Single-Gate MOSFET arranged back-to-back and rotated with respect to one of the gates as shown in Fig. 3.1. The device is designed such that the internal channel is identical in width and thickness as the external channel and the gates (internal and external), which controls these channels are also alike in dimension. A thick substrate exists between the conducting channels and this helps to separate activity from one to another.

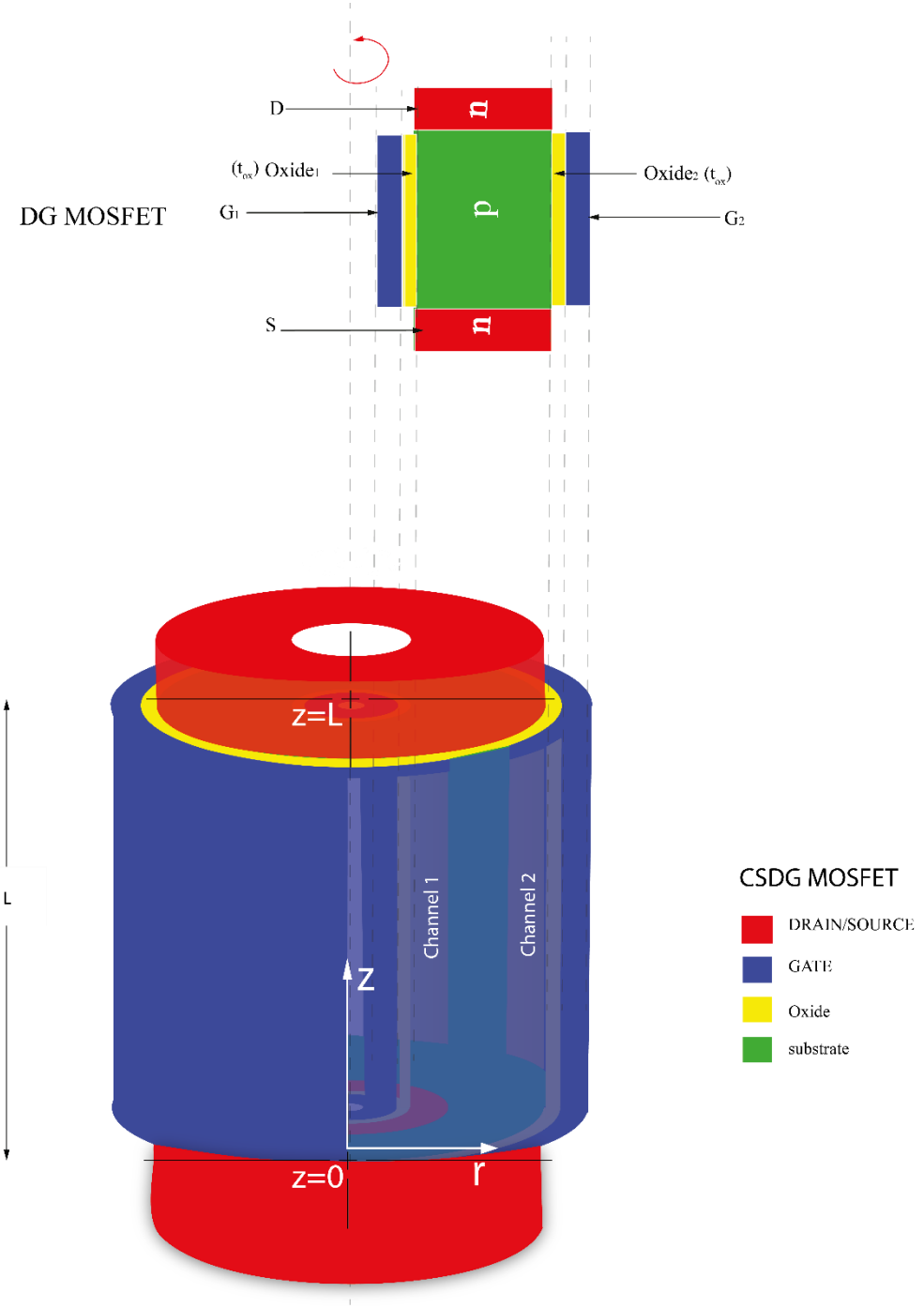


Figure 3.1 Schematic Diagram of the *n*-channel CSDG MOSFET.

This separation also helps to make the activities along the channels independent on the other. The CSDG MOSFET has two gates, $G_1$and G_2, (indicated in blue colour), two drains, D_1 and D_2, (indicated in green colour for *p*-channel and red colour for *n*-channel), the Oxides, $oxide_1$ and $oxide_2$, (indicated in yellow colour), and the *p*-type substrate/body (indicated in red colour for p-channel and green colour for n-channel). The gate, G_1 is formed in the internal part of the cylinder, followed by the thin oxide, $oxide_1$ (to immune the effect of short-channel effect) while the protruding part of the cylinder is the drain and source as shown in Fig. 3.1.

In the *n*-channel enhancement CSDG MOSFET, when suitable positive voltages are applied to the gates $G_1$and G_2, the body which has the majority carrier as holes and minority carrier as electrons, will have the holes repelling from the insulators $oxide_1$ and $oxide_2$ and electrons attracted toward the insulator. Hence creating a channel in which electrons at the *n*-type substrate will be able to move through the source to the drain. Thus, creating *n*-channel in the *p*-type body. This structure has an intruding drain and source region, making the conducting channel of the device capable overcome punch-through effect, velocity saturation, and SCE. A hollow at the centre of the structure makes it effective in limiting thermal effect in the operation of the device. Below is the specification of the novel structure of the CSDG MOSFET.

Table 3.1 Specifications of the novel structure of CSDG MOSFET.

Specification	**Measurement (unit)**
Channel length	*20 nm*
Internal radius	*5 nm*
External radius	*10 nm*
Oxide thickness	*2 nm*
Work function	*4.5 eV*

3.3 Parameters of the CSDG MOSFET

With the introduction of improved cylindrical with undoped-channel device, there is need to analyse its parameter with respect to drain current, transconductance, surface potential, carrier mobility etc. as shown in Fig. 3.2.

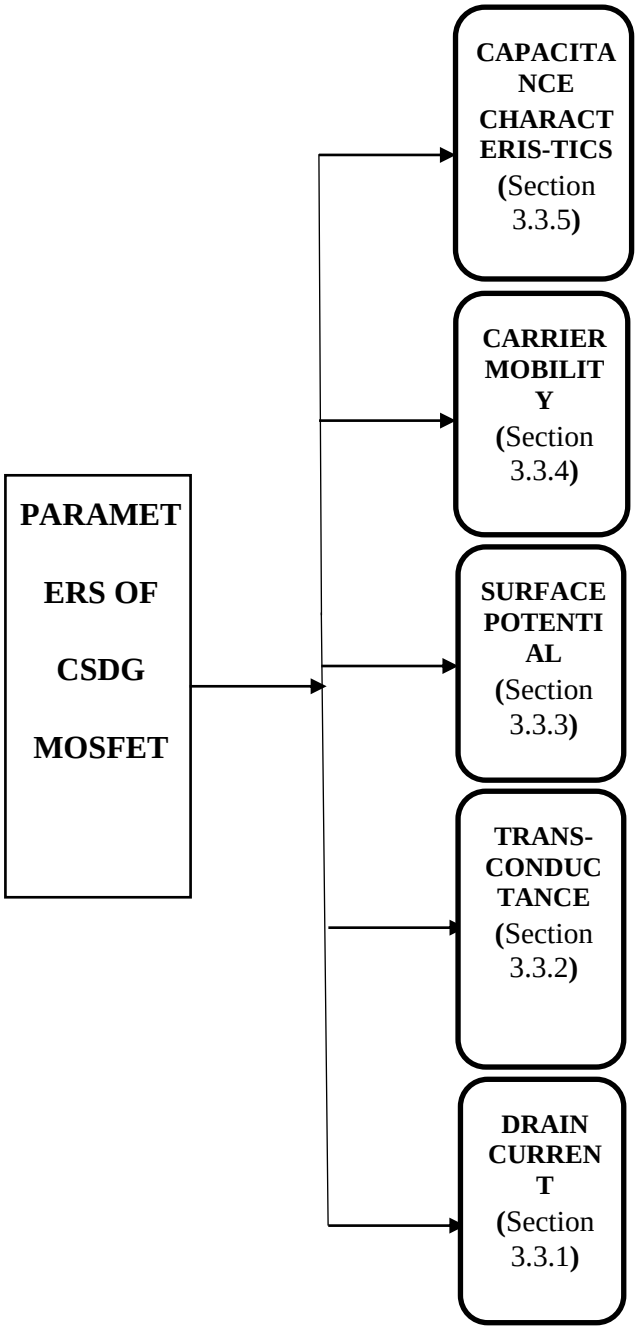


Figure 3.2 Parametric illustration of the CSDG MOSFET.

Although these parameters for different structures of MOSFET have been reviewed in previous chapter, it is necessary to relate their relevance with the improved structure in CSDG MOSFET for better analysis and verify them. In this research work, the verification of analysis is done with the help of a device simulator.

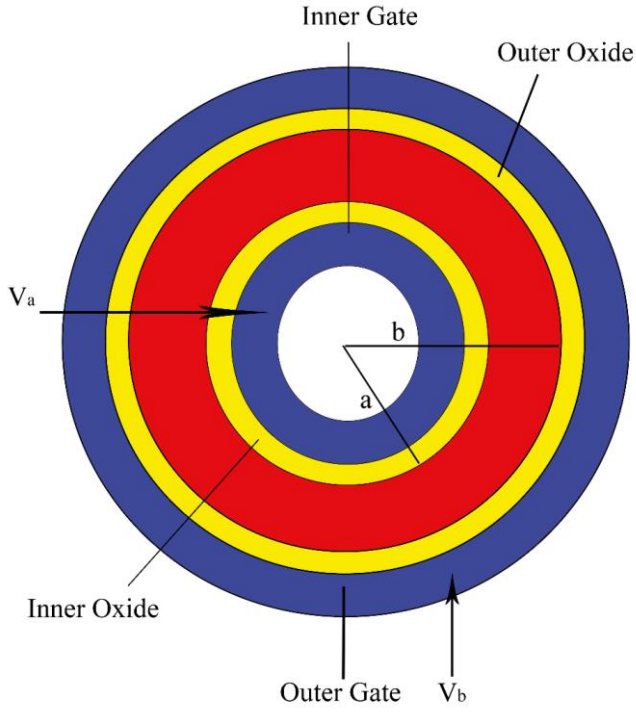


Figure 3.3 Cross Sectional area of the CSDG MOSFET.

Considering the *n*-channel CSDG MOSFET under the influence of electric field generated from applied voltages, V_a and V_b. A 3-D analysis of the MOSFET in *r* and *z*-axis are presented in Fig. 3.1 with the following assumptions put in consideration.

A. The validity of Gradual Channel Approximation (GCA) which explains that the electric field along the y-direction, E_y is much lesser than at x-direction, E_x has been considered in our analysis.
B. It is assumed that the bulk or body charge is uniform in the cylindrical structure, i.e. Q_B is same along the channels.
C. Due to the device type (*n*-channel enhancement CSDG MOSFET) hole current will be negligible as much activity along the channel involved the electron current and its behaviour.
D. The total derived current is assumed to be the same along the channels.

E. The mobility along the channel is known as surface mobility and assumes to be uniform for both channel and is a function of both gate and drain voltage.
F. The conducting channel length of the considered n-channel enhancement CSDG MOSFET is assumed at the range of *20 nm*.

3.3.1 Drain Current

It is important to develop a general drain current equation for a short channel MOSFET. Since the lateral dimension of the considered CSDG MOSFET is more than *10 nm*, quantum mechanical effect will be negligible. To model a drain current equation, the drift-diffusion components has been utilized through the charge-sheet model from Pao-Sah integral. This equation will have some assumptions adequately used to simplify it and use it on other models. Further extension to short-channel device will also be evaluated.

Considering the flow of charges along one of the conducting channels, the current flow can be expressed as:

$$Current(I) = \frac{|Q|}{\tau} \tag{3.1}$$

where $|Q|$ is the magnitude of the charges moving along the conducting channel, and τ is the transit time it takes to move. The Eq. (3.1) assumes that all the electrons flowing from the source (*S*) to drain (*D*) do so with τ. So,

$$\tau = \frac{|Q|}{I} \tag{3.2}$$

The current flow in this CSDG MOSFET is because of two phenomena:

A. Drift velocity of the electron caused by the generated electric field through which drift current is derived.
B. Diffusion currents which is due to the concentration gradient at the conducting channels.

A. Drift Current

The drift current is the motion of the charges due to the presence of electric field in the lateral CSDG MOSFET. When the electric field is generated in one of the conducting channel due to the applied voltage as shown in Fig. 3.3, the charge moves with a velocity w.r.t the intensity of the electric field and such velocity is called drift velocity (v_d). The transit of electron is to travel the length of the conducting channel (L) is given as:

$$\tau = \frac{L}{v_d} \tag{3.3}$$

The magnitude $|Q|$ of the free electron charge is given by the product of the charge (q) with the total number of electrons (which can be represented by the volume of the cylindrical structure) and the concentration of the electron (per unit volume) is:

$$|Q| = nq(\pi a^2 L) \tag{3.4}$$

Substituting Eq. (3.4) into Eq. (3.1), which can be expressed as:

$$I = \frac{nq(\pi a^2 L)}{\tau} \tag{3.5a}$$

Representing the drift velocity in Eq. (3.5a) gives:

$$I = nq(\pi a^2)v_d \tag{3.5b}$$

Considering the top area of the CSDG MOSFET in Fig. 3.3, let the magnitude of the charge per unit area be represented by Q' given as:

$$Q' = nqL \tag{3.6}$$

For a CSDG MOSFET, with generated electric field, the drift velocity is proportional to the carrier mobility expressed as:

$$v_d = \mu_s E \tag{3.7}$$

where μ_s and E are the proportionality constant representing the carrier mobility and the electric field, respectively. Also, the electric field is the voltage applied per length of the considered conducting channel.

$$E = \frac{V}{L} \tag{3.8}$$

where V is the applied voltage at the gate and L is the length of the channel. Substituting Eq. (3.7) into Eq. (3.8) and the result into Eq. (3.5b) gives:

$$v_d = \mu_s \frac{V}{L} \tag{3.9}$$

$$I = \frac{\mu_s Q'(2\pi a)V}{L} \tag{3.10}$$

This equation is verified and in agreement with Ohm's law, where current is proportional to the voltage, and from this equation, the drift current can be expressed as:

$$I_{drift} = \frac{nq\mu_s(2\pi a)V}{L} \tag{3.11}$$

From Eq. (3.11), drift current is proportional to the carrier mobility, radius of the structure and applied voltage and inversely proportional to the length of the conducting channel. This is the drift component of the CSDG MOSFET as part of the model to use in analysing the drain current of the device.

B. Diffusion Current

Diffusion current is the tendency for a charged carrier to move from an area of higher concentration to that of lower concentration due to the random distribution of the electron along the channel and thus result to the flow of electric current. The current is

proportional to the magnitude of the charge (q) and the cross-sectional area of the CSDG MOSFET means:

$$I\alpha\left(-\frac{dn}{dL}\right) \tag{3.12}$$

$$I = Dq(\pi r^2)\left[-\frac{dn}{dL}\right] \tag{3.13}$$

where 'D' is the proportionality (diffusion) constant, which is proportional to the thermal voltage (ϕ_t), given as:

$$D = \mu_s \Phi_t \tag{3.14}$$

And substituting Eq. (3.6) and Eq. (3.14) into Eq. (3.13) with the assumption of the electron tendency to diffuse along the channel length. Diffusion current is expressed as:

$$I_{diff} = \mu_s \Phi_t (2\pi a)\left[-\frac{dQ'}{dL}\right] \tag{3.15}$$

This is valid since the number of electrons are non-uniform along the vertical axis, electrons would have the tendency to diffuse in the r-direction in Fig. 3.1, but we assume that an appropriate external applied vertical electric field prevent that from happening. In other words, we assume that the electrons still move parallel to the z-axis in Fig. 3.1.

Having established the drift and diffusion components for one of the conducting channels which is also applicable to the other channel except for different radius, if the channels are assumed symmetric, we will then derive total current in a channel to be the sum of both drift and diffusion current expressed as:

$$I = I_{drift} + I_{diff} \tag{3.16}$$

w.r.t Eq. (3.10) and Eq. (3.15), considering the whole conducting channel length, the voltage (V) become the potential difference at the surface, (ψ_s) from the source end to the

drain end while with consideration of the negative inversion layer, *-Q'* becomes *Q'*. This implies that these equations become:

$$I_{drift} = \mu_s(-Q')(2\pi a)d\frac{d\psi_s}{dL} \tag{3.17}$$

and

$$I = \mu_s \Phi_t (2\pi a)\frac{dQ'}{dL} \tag{3.18}$$

For one of the channels, substitute Eq. (3.17) and (3.18) into Eq. (3.16), the current becomes:

$$I_{d_1} = \mu_s(-Q')(2\pi a)d\frac{d\psi_s}{dL} + \mu_s \Phi_t (2\pi a)\frac{dQ'}{dL} \tag{3.19}$$

Since, our considerations are along the channel length, we can take the source as the origin, 0 with length at drain as *L* and the potential at the source (ψ_{s0}) and drain (ψ_{sL}) respectively. Also, magnitude of the charge at source and drain as Q'_0 and Q'_L respectively. Using this as boundaries for integrating both side of Eq. (3.19) gives:

$$\int_0^L I_{d_1} dL = (2\pi a)\int_{\psi_{s0}}^{\psi_{sL}} \mu_s(-Q')d\psi_s + \Phi_t(2\pi a)\int_{Q'_0}^{Q'_L} \mu_s dQ' \tag{3.20}$$

$$I_{d_1} = \frac{(2\pi a)}{L}\mu_s\left[\int_{\psi_{s0}}^{\psi_{sL}} (-Q')d\psi_s + \Phi_t(Q'_L - Q'_0)\right] \tag{3.21}$$

Expressing the magnitude of the charge, *Q'* as a function work function between the gate metal and the body (V_{FB}), the capacitance of the oxide (C_{ox}) with consideration of the body effect charge (Q_B) expressed as:

$$Q' = -C_{ox}(V_{GS} - V_{FB} - \psi_s) - Q_B \tag{3.22}$$

$$I_{d_1} = \frac{(2\pi a)}{L}\mu_s C_{ox}\left[\int_{\psi_{s0}}^{\psi_{sL}} ((V_{GS} - V_{FB} - \psi_s) + Q_B)d\psi_s\right] + \frac{(2\pi a)}{L}\mu_s \Phi_t (Q'_L - Q'_0) \quad (3.23)$$

Eq. (3.23) is the drain current drive for one of the conducting channels, but the total drain current is the sum of two conducting channels that make up the device. To achieve this, we assume that the device is symmetric where the internal and external drain current are I_{d_1} and I_{d_2} respectively. Also, the magnitude of the charge per unit area at the source is negligible to achieve the drain current of the CSDG MOSFET is:

$$I_{d_{CSDG}} = I_{d_1} + I_{d_2} \quad (3.24)$$

$$I_{d_{CSDG}} = \frac{2\pi(a+b)}{L}\mu_s\left[2C_{ox}\left(V_{GS} - V_{FB}\right) - C_{ox}\left(\psi_{sL} + \psi_{s0}\right) + 2Q_B + (2\Phi_t C_{ox} - Q_B)\right] \quad (3.25)$$

The application of the drift-diffusion component helps to work with the scaling of the channel length. Analysing the drain current (I_d) with the device simulator varying the drain current to both drain-source voltage and gate-source voltage produce the graphs in Fig. 3.4 and Fig. 3.5 respectively. This analysis is based on the lower voltage that the CSDG MOSFET is characterised with. The threshold voltage is taken as *0.3 V* with channel length of *20 nm*, internal and external radii between *5 nm - 10 nm* and gate-source voltage between *0.5 V - 0.7 V*.

It is noteworthy that Fig. 3.4 produces a steady increment before saturation is reached. Also, as the channel length of the CSDG MOSFET decreases, the drain current increase to further prove the controllability of the dual gate on the activities at the channel, which further cause increase in mobility as the charge carrier have less distance to cover with little or no collision.

It is observed that when a constant V_{GS} at *0.5 V* is applied at the gates of the CSDG MOSFET, the drain current follows the ohmic relationship until pinch off is reached where saturation occur with steady current flow. However, below the threshold voltage, it is observed that little or no significant current flow along the conducting channels. Also, in Fig. 3.5, the V_{DS} is being varied with a range of V_{GS} in which the threshold

voltage also finds its place as the drain current remain insignificantly little but with an increased V_{DS}, the drain current in the CSDG MOSFET increase appreciably.

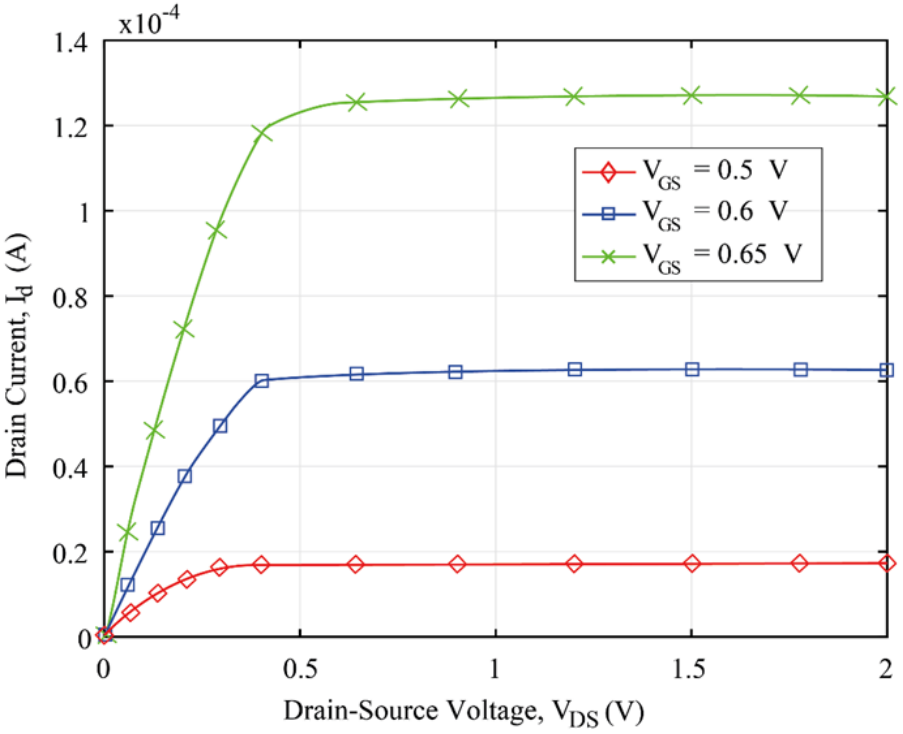


Figure 3.4 Drain current (I_d) with the Drain-Source Voltage (V_{DS}) characteristics of the CSDG MOSFET.

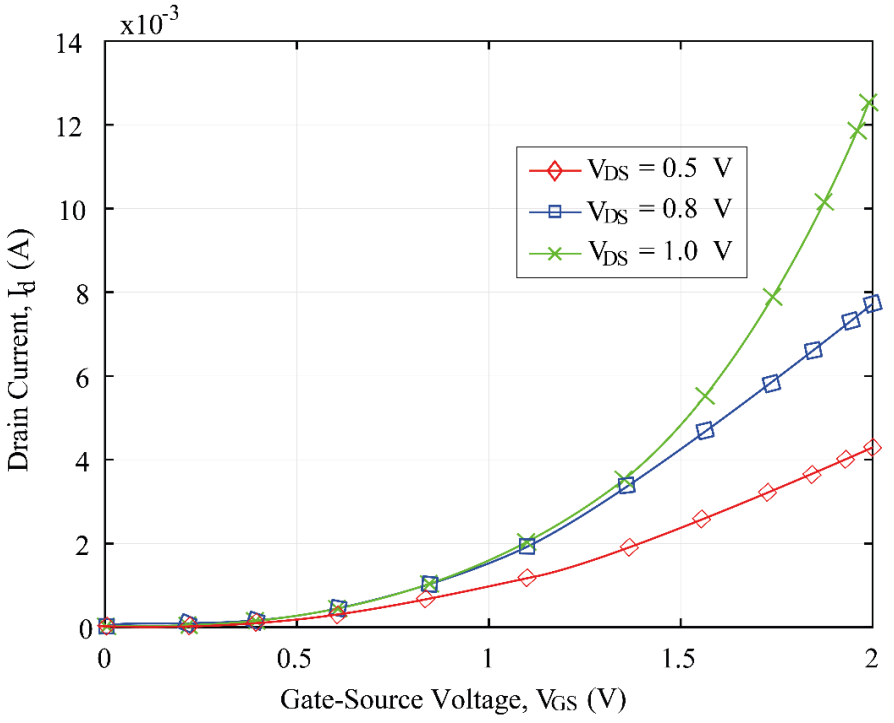


Figure 3.5 Drain current (I_d) with the Gate-Source Voltage (B_S) characteristics of the CSDG MOSFET.

Furthermore, due to the advantage of low threshold voltage, the CSDG MOSFET require a small amount of voltage to activate its activities, this makes the device applicable for low power consumption devices.

3.3.2 Transconductance

The differential change in the drain current with the change in gate-source voltage influenced by the area of the gates explains the transconductance. The efficiency of this device can be measured as the ratio of the output signal to the input signal. The transconductance (g_m) of this device is obtained by differentiating Eq. (3.25) with respect to V_{GS}, while keeping V_{DS} constant. Thus [4]:

$$g_m = \left.\frac{\partial I_d}{\partial V_{GS}}\right|_{V_{DS}} \tag{3.26}$$

This parameter is important because of its dependence on the input signal and it explains the advantage of CSDG MOSFET over other MOSFET types:

$$g_m = \frac{\partial I_d}{\partial \psi_s} . \frac{\partial \psi_s}{\partial V_{GS}} \tag{3.27}$$

The transconductance of this device is obtained by differentiating Eq. (3.25) w.r.t V_{GS}, while keeping V_{DS} and body voltage as a constant. Thus:

$$g_{m_{CSDG}} = \frac{2\pi(a+b)}{V_{GS}L}\mu_s\left[2C_{ox}\left(V_{GS}-V_{FB}\right)-C_{ox}\left(\psi_{sL}+\psi_{s0}\right)+2Q_B+(2\Phi_t C_{ox}-Q_B)\right] \tag{3.28}$$

The efficiency of a device is measured by the ratio of the output signal to that of the input signal. For the CSDG MOSFET in consideration, efficiency is higher due to the Eq. (3.28) and its characteristics. It has been observed from Eq. (3.28) that CSDG MOSFET has a higher transconductance (gain) due to its thin gate oxide, which attribute to higher C_{ox}. Also in the CSDG MOSFET (due to its undoped characteristics) mobility

of electron in the n-channel MOSFET is higher thereby providing higher transconductance.

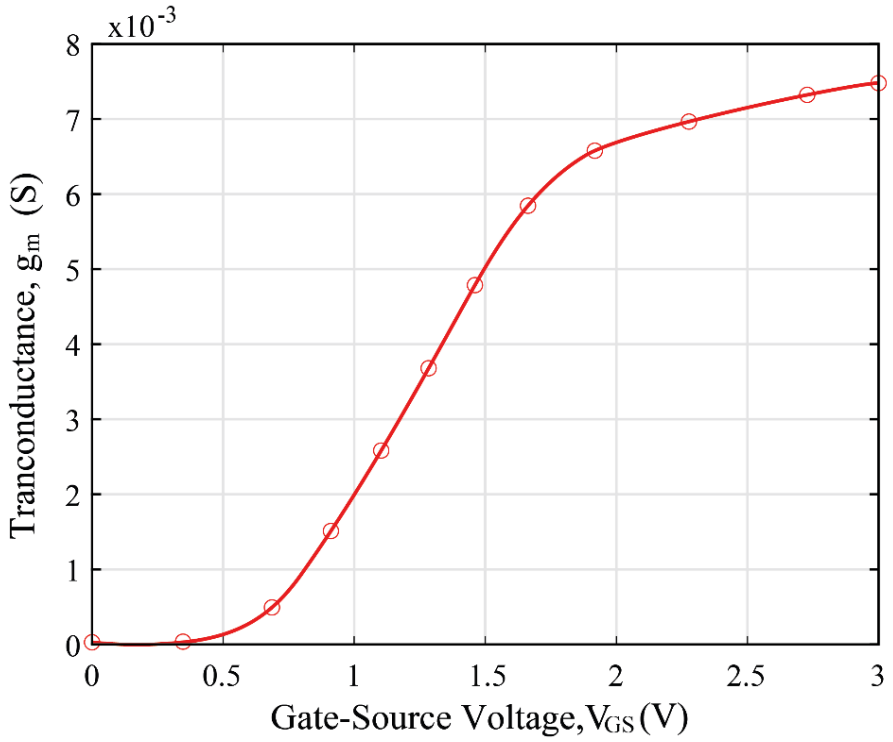


Figure 3.6 Transconductance (g_m) with the Drain Current (I_d) characteristics of the CSDG MOSFET.

In Fig. 3.6, it has been observed that the transconductance is zero below the threshold voltage. *0.3 V*, but as the gate-source voltage increase the transconductance also increase continuously. The sensitivity of the CSDG MOSFET from this analysis is observed to be appreciable as the V_{GS} increases. This characteristics of the CSDG MOSFET can be employed in Radio Frequency Communication systems for better amplification of signals.

3.3.3 Surface Potential

From section 3.3.1, the verified increased drain current affects the mobility of the carrier due to the applied voltages at the channels of the CSDG MOSFET. This fact with the major consideration on the outer structure (Region 1) of the CSDG MOSFET in Fig. (3.7) will be utilized to analyse the surface potential than the inner, this accuracy with the simulation helps to justify the model used in analysing the CSDG MOSFET.

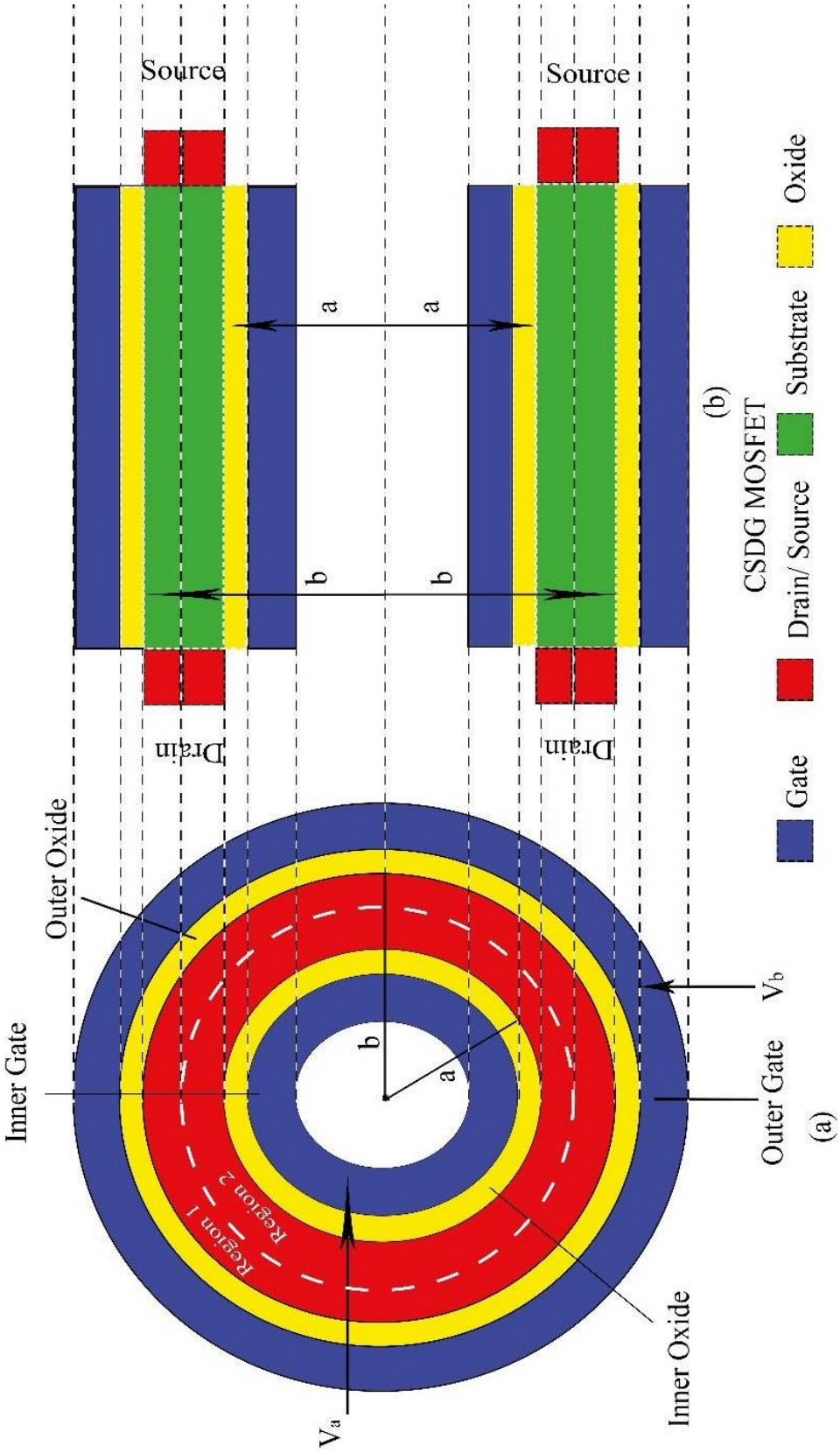


Figure 3.7 2-D cross-schematic diagram of n-channel CSDG MOSFET.

From the coordinate description of the cross-schematic diagram of the CSDG MOSFET in Fig. 3.7, a two-dimensional (2-D) Poisson equation with gradual channel approximation of a cylindrical structure will be used to analyse the surface potential of the CSDG MOSFET, expressed as:

$$\frac{d^2\psi}{db^2}+\frac{1}{b}\frac{d\psi}{db}=\frac{q^2n}{\varepsilon_{si}}e^{q(\psi-V)/kT} \tag{3.29}$$

where ε_{si} and n are the dielectric permittivity of silicon and the number of charges respectively, k and T are the Boltzmann constant and absolute temperature at room temperature respectively, and V and b are the quasi-Fermi potential that ranges from 0 to V_{DS} at different point on the channel and the outer radius of the CSDG MOSFET as shown in Fig. (3.7) respectively. Also, because the channel in consideration is undoped, the hole density for this analysis will be negligible. Applying a less complex approach of variable transformation of different equation to Eq. (3.29) gives:

$$\frac{kT}{q}\frac{d^2w}{db^2}+\frac{kT}{q}\frac{1}{b}\frac{dw}{db}=\frac{q^2n}{\varepsilon_{si}}e^{w} \tag{3.30}$$

where w is the representation of:

$$w=\frac{q(\psi-V)}{kT} \tag{3.31}$$

Evaluating the potential function, ψ with respect to the radius b is expressed as:

$$\psi(\mathrm{b})=2V+\frac{kT}{q}\left[\mathrm{In}\left|\frac{2BA^2\varepsilon_{si}kT}{q^2n}\right|+(\mathrm{A}-2)\,\mathrm{Inb}-2\,\mathrm{In}(\mathrm{b}^A-\mathrm{B})\right] \tag{3.32}$$

where A and B are the integration constant for the boundary conditions while integrating Eq. (3.30). Applying the inversion charge density, Q to Eq. (3.32) to agree with the Gauss's law is expressed as:

$$Q = -C_{ox_2}(V_{GS} - V_{FB} - \psi_s) = \frac{\varepsilon_{si} kT}{q^2}\left[\frac{A-2}{b} - \frac{2Ab^{A-1}}{b^A - B}\right] \tag{3.33}$$

where C_{ox} and V_{FB} are the capacitance of the oxide and gate metal and the body (V_{FB}) respectively. From the analysis of the drain current, the saturation region of operation of the CSDG MOSFET begin to form when the applied voltage, V_{GS} is greater than the threshold voltage. Applying this voltage change while comparing the surface potential and the radius (outer radius considered) of the CSDG MOSFET by simulation produces Fig. 3.8. It is observed that as the radius is increased in its nanoscale, the surface potential is steady but as the applied voltage at the gate exceeds the threshold voltage, the surface potential slightly increases with increased radius.

Also, varying the surface potential and the gate voltage at the different oxide thickness was verified from Eq. 3.33 and it was observed that with the CSDG MOSFET, an increase in applied gate voltage produce an increase in the surface potential of the CSDG MOSFET especially because of reduced oxide thickness. This advantage attribute CSDG MOSFET application in Nanotechnology while retaining its better performance, excellent electrostatic control and greater current drive.

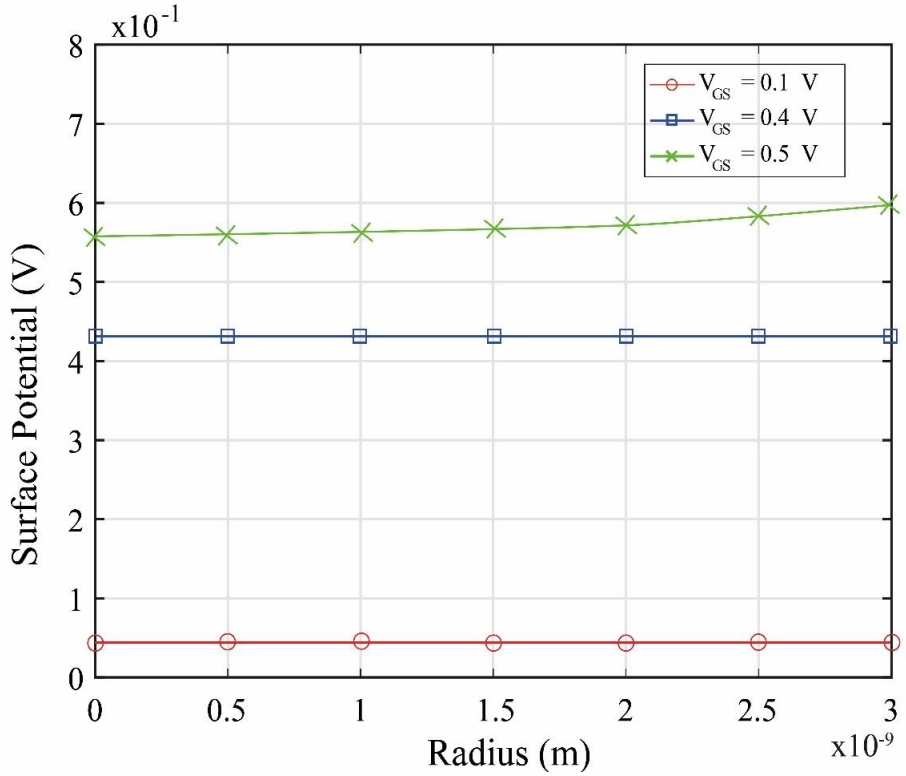


Figure 3.8 Variation of the surface Potential with the outer radius of n-channel CSDG MOSFET.

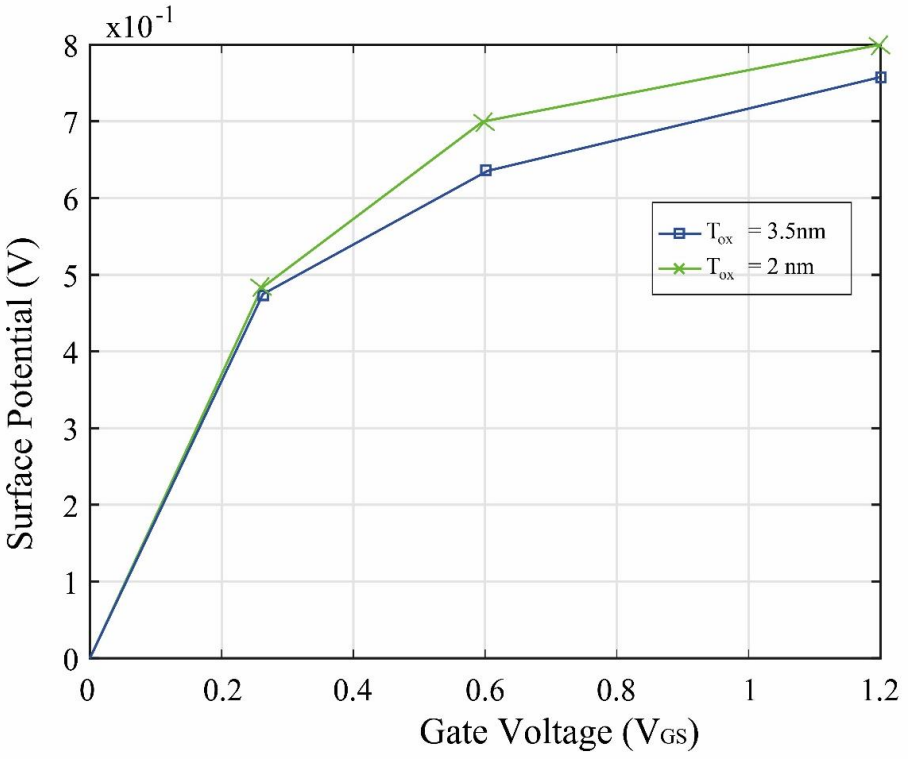


Figure 3.9 Variation of the surface Potential and applied gate voltage at different oxide thickness of n-channel CSDG MOSFET.

3.3.4 Carrier Mobility

From Eq. (3.25) and Eq. (3.28), it has been observed that the carrier mobility strongly affects the drain current and transconductance of the CSDG MOSFET. Mobility is an essential parameter in the modelling of the CSDG MOSFET. It explains how rapidly electrons move along the conducting channel of the cylindrical structure. The movement of the electrons along the channel results into building up of the current due to the diffusion of electrons from region of higher concentration to lower concentration. This movement is in the direction of the electric field generated by the applied voltage.

This concept can be further explained using Gauss's Law, which states that the total electric flux out of a closed system is equal to the charge enclosed by permittivity. For the CSDG MOSFET in consideration, the electric field will be a function of the natural length of the channel, the circumference of the structure and the permittivity of the CSDG MOSFET.

Also, considering two independent gates influencing the activity at the conducting channel, the electric field for the internal cylindrical structure can be expressed as:

$$E_{\text{int}} = \frac{\lambda_a}{2\pi a \varepsilon_0} \tag{3.29a}$$

$$E_{ext} = \frac{\lambda_b}{2\pi a \varepsilon_0} \tag{3.29b}$$

where λ_a and ε_o are the charge per unit length and permittivity, respectively. Then the total electric field for the CSDG MOSFET will be sum of the internal and external electric field given as:

$$E_{CSDG} = E_{\text{int}} + E_{ext} \tag{3.30}$$

$$E = \frac{\lambda(a+b)}{2\pi ab\varepsilon_0} \tag{3.31}$$

where the charge per unit length and permittivity is assumed same for both conducting channels of the CSDG MOSFET.

Furthermore, from Eq. (3.7), the drift velocity is proportional to the electric field applied at the gates of the CSDG MOSFET with mobility as the proportionality constant. The μ, carrier mobility caused by the electric field. However, for a heavily doped MOSFET, the mobility reduces because of energy loss from wider dimension of the conducting channel. That factor is overcome by to the short channel length utility by the CSDG MOSFET. This can be verified from Eq. (3.31), the higher radii of the CSDG MOSFET, the lower the value of electric field. However, with short channel utilized by the CSDG MOSFET, the electric field generated is increased and this affect the drift velocity of the charges as illustrated in Eq. (3.7).

Also, another factor that may influence mobility in charges of the CSDG MOSFET is scattering. Different scattering influencing this MOSFET may be caused by impurity concentration, electric field intensity, temperature changes among others. This scattering tends to lower the electron mobility in *n*-channel CSDG MOSFET and thus affect drain current, transconductance among other parameters. The value of mobility however with its different scattering can be explained using Matthiessen's rule [89] expressed as:

$$\frac{1}{\mu} = \frac{1}{\mu_{coul}} + \frac{1}{\mu_{pho}} + \frac{1}{\mu_{rough}} \tag{3.32}$$

Where μ_{coul}, μ_{pho}, and μ_{rough} are coulomb scattering, phonon scattering and rough surface scattering, respectively. Coulomb scattering is as result of impurity atom doped into the conducting channel which cause interference. But for the CSDG MOSFET with minimal or no doped atom, this scattering is negligible, other scattering are however due to electrical conductivity, interactions between the electrons or the electrons and the surface of the channel. All these factors will be assumed to be constant and not considered to determine how the radii of the device affect and influence carrier mobility in the CSDG MOSFET.

From Eq. (3.31) and Eq. (3.7), considering the drift velocity of the CSDG MOSFET with respect to constant mobility at both radii:

$$\nu_{d_{CSDG}} = \nu_{d_{\text{int}}} + \nu_{d_{ext}} \tag{3.33}$$

$$\nu_{d_{CSDG}} = \mu E_{CSDG} \tag{3.34}$$

$$\nu_{d_{CSDG}} = \mu \frac{\lambda(a+b)}{2\pi ab\varepsilon_0} \tag{3.35}$$

which can equally be expressed proportionally with respect to carrier mobility as:

$$\mu = \frac{2\pi\varepsilon_0}{\lambda}\left[\frac{ab}{a+b}\right]\nu_{d_{CSDG}} \tag{3.36}$$

making $\frac{2\pi\varepsilon_o}{\lambda}$ as a proportionality constant, mobility is expressed as:

$$\mu \propto \left[\frac{ab}{a+b}\right]\nu_{d_{CSDG}} \tag{3.37}$$

From Eq. (3.37), we can relate the carrier mobility to be directly proportional to the product of the radii and inversely proportional to the sum of the two radii with respect to the drift velocity of the charges in the CSDG MOSFET. These radii can be varied one with another to check the mobility.

ANALYSIS OF MOBILITY

Analysing Eq. (3.37) to produce better mobility with respect to each radius '*a*' and '*b*' and drift velocity produce two cases [90].

A. Case 1

Let us apply a fixed internal radius with a varied external radius with range above '*a*' and equal to less than '*b*' where 'b_1' is the varying external radius.

$$a < b_1 \leq b \tag{3.38}$$

Representing external radius, '*b*' with 'b_1' in Eq. (3.37), it is observed that the carrier mobility of the CSDG MOSFET decreases. But using this same fixed internal radius and external radius increased as:

$$b_1 \geq b \tag{3.39}$$

In this variation of case 1, with increased external radius there will be a slight increase in the carrier mobility with respect to total drift velocity. However, this cannot be used as it makes the CSDG MOSFET device larger in dimension in turn making the conducting channel enlarged.

B. Case 2

Varying the internal radius with a fixed external radius with range below and equal to the internal radius.

$$a_1 \leq a \tag{3.40}$$

With this variation, it has been observed that the carrier mobility reduces with respect to the total drift velocity, but if the variation is expressed as:

$$a \leq a_1 < b \tag{3.41}$$

With Eq. (3.41), the mobility is increased and the size of the CSDG MOSFET is retained as the external radius is not reduced. It is observed that carrier mobility increase and the size of the CSDG MOSFET is retained as the external radius is fixed with varying internal gate radius. With this variation, the CSDG MOSFET can control the Si-channel by reducing width to be small.

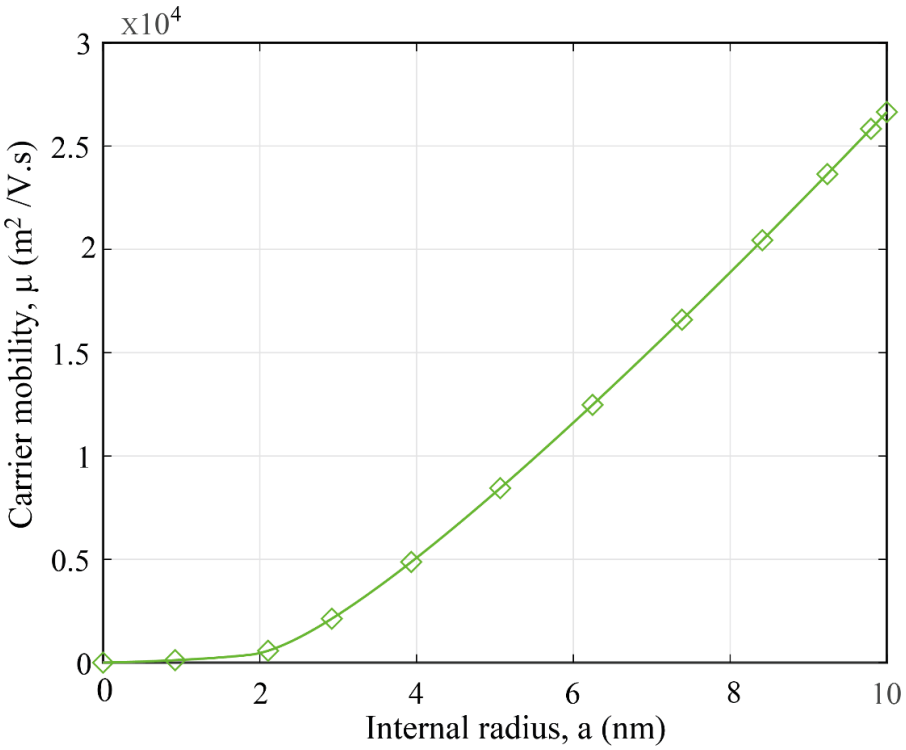


Figure 3.10 Analysing Carrier mobility with the internal radius of the CSDG MOSFET.

In Fig. 3.7, it has been discovered that ranging the internal radius from *0 nm* to *10 nm*, the mobility of the charge increases as the conducting channel is affected. Also, due to less collision along the channel due to lack of dopant, the charge velocity drift increases as the internal radius is increased, which tend to increase the carrier mobility. Although, this increase should not be so much as to sandwich the body of the device where the channels and being form. This is because, the two channels can be influencing

one another but with this analysis of the external gate being *20 nm*, and the internal gate range between *0* to *10 nm*, the CSDG MOSFET will still maintain its better characteristics and increased mobility.

3.3.5 Capacitance Characteristics

In this parameter analysis, Meyer's model [91] has been utilized to explain the six splitting capacitances in the CSDG MOSFET. These capacitances are the gate-source capacitance of the internal radius (C_{GS1}), gate-source capacitance of the external radius (C_{GS2}), gate- drain capacitance of the internal radius (C_{DG1}), gate- drain capacitance of the external radius (C_{DG2}), drain-source capacitance of the internal radius (C_{DS1}), drain-source capacitance of the external radius (C_{DS2}). All these capacitances are derived from the amount of charges generated through the applied gates of the CSDG MOSFET expressed by Meyer [91] as:

$$C_{GS} = \left.\frac{\partial Q_G}{\partial V_{GS}}\right|_{V_{DS}, V_{GD}} \tag{3.42a}$$

$$C_{DS} = \left.\frac{\partial Q_G}{\partial V_{DS}}\right|_{V_{GS}, V_{GD}} \tag{3.42b}$$

$$C_{GD} = \left.\frac{\partial Q_G}{\partial V_{GD}}\right|_{V_{GS}, V_{DS}} \tag{3.42c}$$

From the Eq. (3.42), the capacitance proved to be reciprocal, as C_{GS} is same as C_{SG} and C_{DS} is equal to C_{SD} which further prove Meyers assumption of reciprocal capacitance. Also, the Eq. (3.42) is valid with the assumption that the charges generated along the conducting channel are constant.

However, the considered capacitance is the external part, there exist also some internal part of the CSDG MOSFET that sum up in the total capacitance of the CSDG MOSFET. The internal parts are the gate-oxide capacitance of the first gate, C_{ox1} and the gate-oxide capacitance of the second gate, C_{ox2}. These capacitances can be expressed mathematically as:

$$C_{ox1} = \frac{E_{ox1}}{\left[aIn(1+\frac{t_{ox1}}{a}) \right]} \tag{3.43a}$$

$$C_{ox2} = \frac{E_{ox2}}{\left[bIn(1+\frac{t_{ox2}}{b}) \right]} \tag{3.44b}$$

where E_{ox1} and E_{ox2} are the generated electric field at internal and external gates respectively, t_{ox1} and t_{ox2} are the oxide thickness of both internal and external gates respectively. These oxide capacitances could be different due to different voltages applied at the gates. The capacitances and the drain current of the CSDG MOSFET from the applied voltages at both gates represented in Figure 3.8.

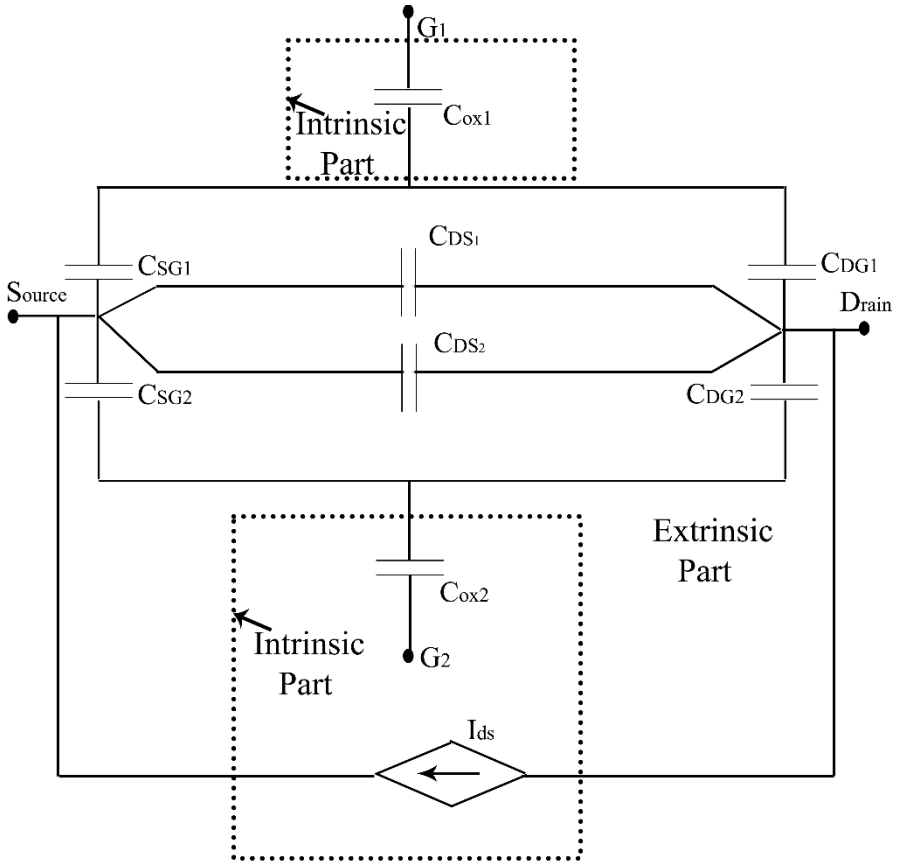


Figure 3.11 Equivalent Capacitive model of the CSDG MOSFET showing the intrinsic and extrinsic parts.

From Fig. 3.8, the total capacitance in series and parallel as drain-source current flow through it is expressed as:

$$C_{CSDG} = C_{ox1} + C_{DS1} + C_{DS2} + C_{ox2} + \frac{C_{SG1}.C_{DG1}}{C_{SG1} + C_{DG1}} + \frac{C_{SG2}.C_{DG2}}{C_{SG2} + C_{DG2}} \tag{3.45}$$

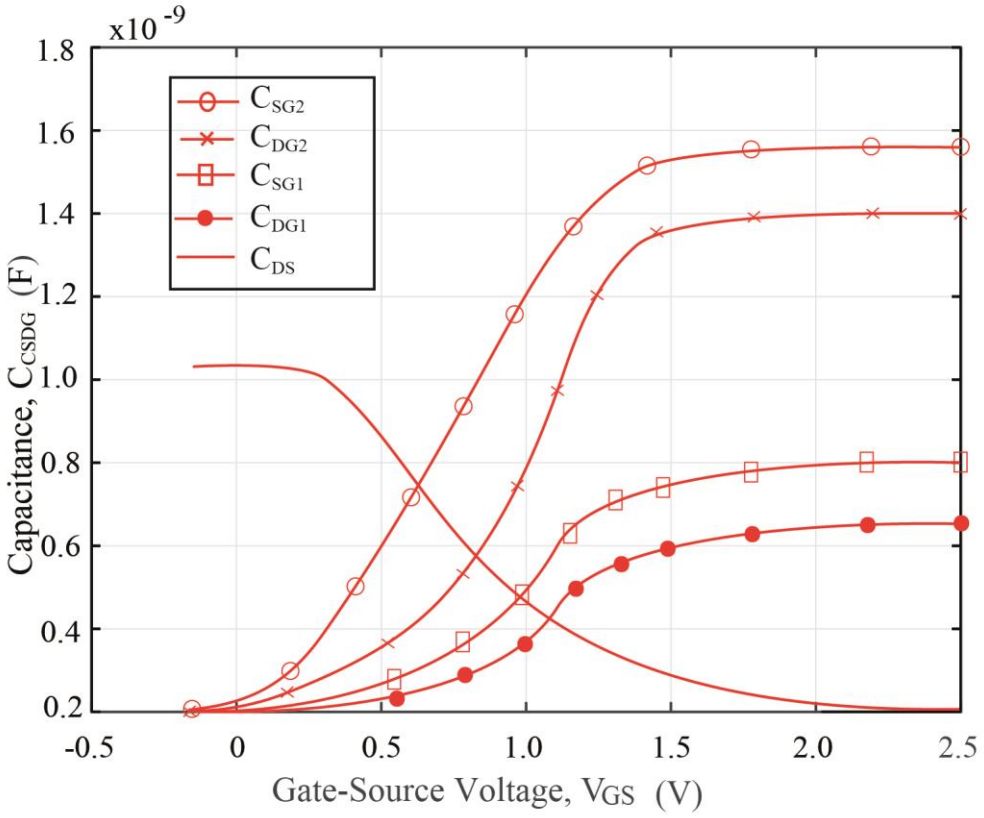


Figure 3.12 Analysing the capacitances in the CSDG MOSFET

In this CSDG MOSFET, the permittivity and the gate-oxide has been considered because of the body on the capacitance and this produce higher stored energy in the devices that almost doubled when compared with other Cylindrical Structured MOSFET with single-gate. This attribute makes the device preferable in application.

Also, considering the internal and external capacitances of the CSDG MOSFET in Fig. 3.12, it was observed that the gate-source capacitance of the external radius of the CSDG MOSFET is higher than that of the internal, likewise the gate-drain capacitance of the external radius is greater than that of internal. This largely due to the increased radius in these part of the devices, which in turn increases the capacitance of the CSDG MOSFET, making it applicable for our daily usage.

3.4 Conclusions

In this chapter, the various parameters of the CSDG MOSFET were analysed and verified. The drain current has been analysed using the drift-diffusion model with the Pao-Sah integral and an increased current drive was derived using the CSDG MOSFET. The sensitivity of the device was also considered with the transconductance parameter. Using the efficiency measure of any device to measure that of the CSDG MOSFET and it was observed that it produces an increased transconductance.

The effect of radius on the carrier mobility through the application of electric field at the two gates of the CSDG MOSFET has been analysed. The variation between the radius and the carrier mobility of the CSDG MOSFET has been derived. It has been observed that to reduce the SCEs caused by fluctuation of carrier mobility, the radius of the CSDG MOSFET can be varied, such that the carrier mobility is increased. This makes carrier transport in CSDG MOSFET easy and useful in nanotechnology devices.

The variation in the radius of CSDG MOSFET is a function of carrier mobility as well as temperature. Although the thermal effect generated in the CSDG MOSFET through this process will be discussed in the next chapter. Furthermore, the intrinsic and extrinsic part of the CSDG MOSFET was also analysed to get an equivalent capacitance characteristic of the CSDG MOSFET. All these attributes of the CSDG MOSFET analysed shows that the device will be of greater benefit in Nanotechnology application.

CHAPTER 4

THERMAL EFFECT ON THE CSDG MOSFET

4.1 Introduction

As peculiar and reliable as the CSDG MOSFET has proven to be, it is discovered that change in temperature have effect on its attributes with other types. This is attributed to the fact that temperature is one of the most important factors hindering the application of MOSFET in VLSI and ULSI designs. When the device is exposed to increased temperature or decreased temperature beyond the normal temperature, the total energy from the molecular motion of the charge carrier in the device is affected and the required speed and functionality becomes unattainable. Inability to adequately manage the effect of temperature change often lead to thermal runaway, caused by the recycling of increased temperature with leakage current. This leads to reduced reliability and damage of the CSDG MOSFET.

When the temperature of any MOSFET increases at high voltage supply, it has been discovered that the drain saturation current as well as switching speed reduces. Also, when the temperature of any MOSFET increases by $10\ ^{0}C$ above $100\ ^{0}C$, the life span of such device reduces by half [19]. On the other side, exposure of the MOSFET to cryogenic temperature gives an upgrade on the number of device functionality. The better functionality includes increased current drive, better voltage gain, reduction of series resistance, and power consumption [20, 92]. However, this comes at the expense of reduced reliability and abnormal performance of the device when used on a long-time operation. This makes the parametric analysis of CSDG MOSFET incomplete work if thermal management has not been analyzed. Therefore, in this chapter the thermal effect on CSDG MOSFET is analysed with the stability to this effect.

The improved CSDG MOSFET in Fig. 3.1 is structured with the understanding of the thermal effect on MOSFET and how to fabricate a structure that best overcome this effect. The cylindrical structure is used to overcome the corner effect from the carrier mobility. Also, with the cylindrical structure, the device has little body contact with the IC board, it might be mounted upon. The external gate of the device has little contact

with the board, and it generates little heat that could be overcome with the help of a heat sink. Likewise, the parameters of the device is carefully considered with the result obtained in chapter 3 are channel lengths = *20 nm*, internal radius = *5 nm*, external radius = *10 nm*, oxide thickness = *2 nm* and work function = *4.5 eV*.

This chapter analyzes the thermal resistance in the CSDG MOSFET to analyse the effect of heat on the drain current, transconductance, and other parameters analysed at the previous chapter along a range of temperature of *0 – 300 K*. This analysis will be verified through numerical simulation to determine the variation between the parameters and temperature. Thereafter, the thermal noise in CSDG MOSFET has been scrutinized with comparison to other MOSFETs types. Finally, the temperature sensitivity of this device will be used to explore how the thermal stability can be ensured in the proposed CSDG MOSFET to affect its reliability and improved performance.

4.2 Thermal Resistance

The CSDG MOSFET in application for microelectronic, nanotechnology and VLSI design shows promising and excellent performance, but the heating effect must be considered. One of the ways to examine this is through the thermal resistance. It is an established fact that there exists a significant amount of resistance along the channels of the *n*-channel enhancement CSDG MOSFET until appreciable voltages are applied to the gates [93]. Also, in the gate electrode, an amount of resistance exists but due to the negligible amount of current, the resistance is not being considered.

Bresson et. al. [94] have analyzed the thermal conductivity in *65-nm* channel length of a SiO_2 buried oxide (BOX) MOSFET. In that research work, high-*k* dielectric materials such as Al_2O_3 and diamond were compared with the default SiO_2. Also, low-*k* dielectric materials, like air was compared with the SiO_2. The thermal conductance was analysed after generating an equivalent thermal resistance circuit, where it was discovered that replacing the conventional BOX with diamond (which is of thermal conductivity *800* $Wm^{-1}k^{-1}$) or manageable with Al_2O_3 and AlN (of *20* $Wm^{-1}k^{-1}$ and *5* $Wm^{-1}k^{-1}$ thermal conductivities respectively). However, this thermal sensitivity comes with an increased short channel effect.

*Zeljk*o [95] modelled a ladder network for the thermal resistance of power MOSFET. This was done to measure the MOSFET's Temperature Sensitive Parameters (TSEP) and Transient Thermal Impedance Curve (TTIC). This was done in switching

circuit device using a power MOSFET. Also, *Paolo et. al.* [96] proposed a model to explain the thermal network using an equivalent thermal resistance circuit, where the MOSFET parameters were evaluated with change in temperature. The model could calculate and analyse the thermal increase but for few parameters such as drain current, transconductance, and carrier mobility, no significant changes was observed with increase temperature.

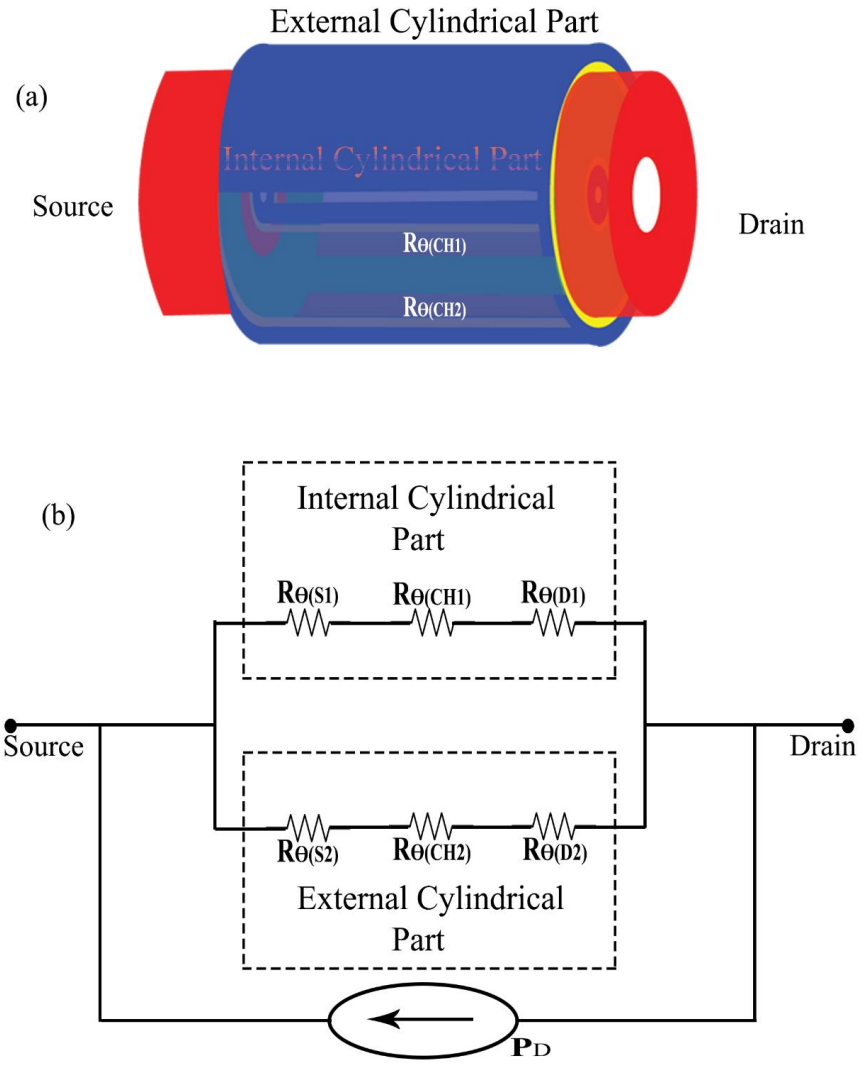


Figure 4.1 Simplified (a) Diagram of n-channel CSDG MOSFET and (b) Equivalent resistive model of the CSDG MOSFET.

These reviewed models and their drawback is used to analyse the equivalent thermal resistance for the CSDG MOSFET. The internal and external cylindrical parts of the CSDG MOSFET was considered with a negligible gate thermal resistance ($R_{\Theta G}$)

along the power of both frames. The equivalent resistance circuit has been modelled with the consideration of a shared resistance of the source and drain along the two channels with no or little consideration of body of the CSDG MOSFET (Fig. 4.1).

The resistances in drain, source and channels are expressed as thermal resistance due to obstruction from heat equilibrium exacted by these junctions (Fig. 4.1). These thermal resistances of drain, source and channels of the internal and external cylindrical parts are in series. Analysing the thermal resistance of the internal and external cylindrical parts is:

$$R_{\theta_{\text{int}}} = R_{\theta_{(\text{S1})}} + R_{\theta_{(\text{CH1})}} + R_{\theta_{(\text{D1})}} \tag{4.1}$$

$$R_{\theta_{\text{ext}}} = R_{\theta_{(\text{S2})}} + R_{\theta_{(\text{CH2})}} + R_{\theta_{(\text{D2})}} \tag{4.2}$$

Since the internal and external cylindrical parts are in parallel, the total thermal resistance in this CSDG MOSFET is expressed as:

$$R_{\theta(CSDG)} = \frac{\left[\left(R_{\theta_{(S1)}} + R_{\theta_{(CH1)}} + R_{\theta_{D1)}}\right)\left(R_{\theta_{(S2)}} + R_{\theta_{(CH2)}} + R_{\theta_{(D2)}}\right)\right]}{\left[\left(R_{\theta_{(S1)}} + R_{\theta_{(CH1)}} + R_{\theta_{(D1)}}\right) + \left(R_{\theta_{(S2)}} + R_{\theta_{(CH2)}} + R_{\theta_{(D2)}}\right)\right]} \tag{4.3}$$

From this analysis, the parallel connection of the CSDG MOSFET helps reduce thermal resistance. It is also observed that the thermal resistance in the CSDG MOSFET below 150 ^{o}C is lower, but when high temperature is attained, the resistance in the device begin to increase, making it inadequate for economical usage. Generally, if the temperature increase is maintained below 150 ^{o}C, the thermal resistance is reduced in the CSDG compared to other reviewed MOSFETs in chapter 2. This will be helpful in the application of the CSDG MOSFET in nanotechnology.

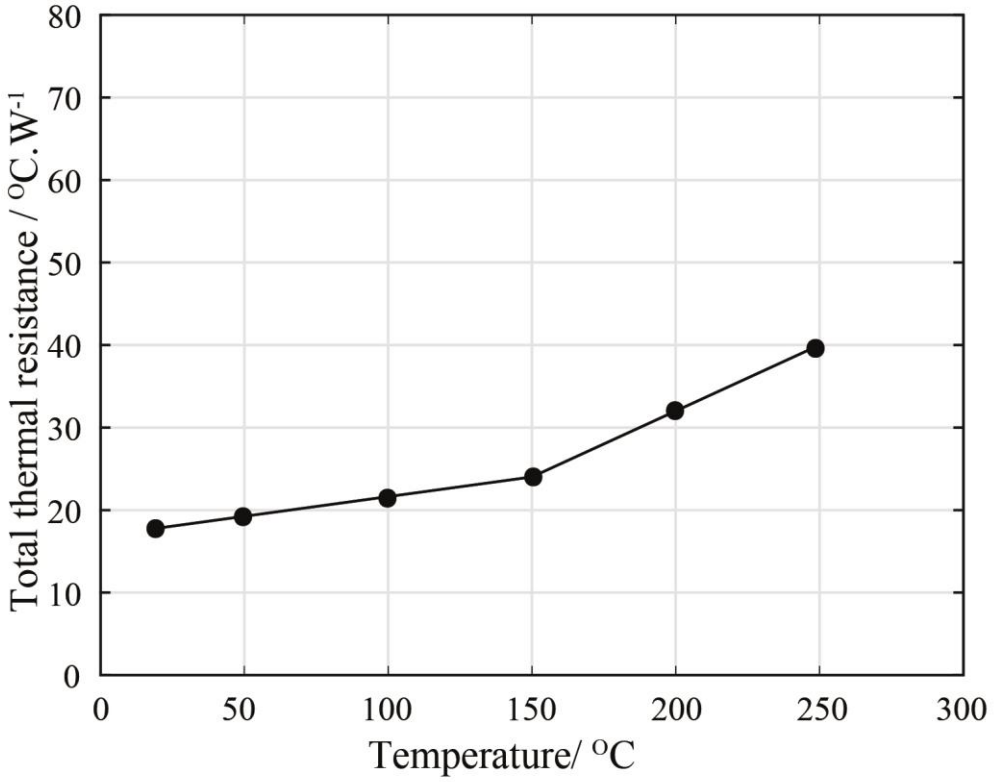


Figure 4.2 Total thermal resistance in the CSDG MOSFET with respect to Temperature change

4.3 Thermal Effect on Parameter of the CSDG MOSFET

Generally, MOSFETs are temperature dependent devices. This implies that temperature is a vital player in the efficiency and performance of the MOSFET. Self-heating in the device affect its proposed environment and in turn affect the performance and reliability of the device. Our improved CSDG MOSFET is modelled with this factor in view. The structure is cylindrical in order to have little contact with the board and generate less heat.

In this section, the CSDG MOSFET is analysed using its parameters such as drain current, transconductance and carrier mobility to determine its temperature dependence. This analysis has been performed using mathematical modelling of its parameters at various temperature range. The impact on these parameters and how it influences the overall performance of the CSDG MOSFET will also be discussed.

4.3.1 Thermal Effect on Drain current

One of the immediate parameter that is affected by temperature change is the drain current. The drain current is assumed to be the monitor for the transistor temperature. This is because an increase in the temperature has a consequential effect on the carrier mobility which in turn affects the drain current. To examine the movement of electron along the channels of the CSDG MOSFET, the drift-diffusion approach comes with the limitation of scattering for previous MOSFET types. But for the CSDG MOSFET, it is established that the channels are undoped and most scattering mechanism are insignificant except for electron-electron collision which is not considered in detail in this work.

When the temperature in MOSFET is increased, the drift current is increased as such that with the application of voltage at both gates of the CSDG MOSFET, electric field is generated along the formed channels which excites the electrons. However, with this increase in temperature, the charge carrier accelerates at an increased speed but with further increase in the temperature, the carrier mobility is reduced. This is due to the increasing collision of the electrons along the cylindrical channels which affect the express movement of the electron from the source to the drain. Recall that drift velocity (ν_d) is proportional to the carrier mobility (μ) expressed as:

$$\nu_d = \mu E \tag{4.4}$$

Such that when the mobility is increased, the drift velocity increases but, with further increased in temperature, the mobility of the carrier charges is constrain due to collision which result to reduced drift velocity. With the cylindrical structure of the CSDG MOSFET considered, the drift current, which is a function of the drift velocity is also affected such that:

$$I_{drift} = \frac{nq\mu 2\pi(a+b)V}{L} \tag{4.5}$$

With the increased temperature, the number of charges (n), the voltage applied (V) and the channel length (L) are kept constant, the mobility (μ) becomes a factor that affect the drift current. When the mobility is appreciable, the drift current is increased and vice versa.

Also, the diffusion current is proportional to the cross-sectional area of the CSDG MOSFET due to the movement of the electrons from higher concentration to lower concentration along the channel. Therefore, diffusion current is:

$$I = Dq\pi(a+b)^2\left[-\frac{dn}{dL}\right] \tag{4.6}$$

where D is the diffusion constant which is the product of the carrier mobility and thermal voltage (Φ_t), that is:

$$D = \mu\Phi_t \tag{4.7}$$

$$\Phi_t = \frac{kT}{q} \tag{4.8}$$

From the Eq. (4.7) and Eq. (4.8), *k* is the Boltzmann constant and *T* is the temperature, the increase in temperature is supposed to bring a logical increase in the diffusion current, but for the electron-electron collision, which tends to obstruct the express movement of electrons when the temperature is increased above tolerance.

The drift-diffusion model is further verified in simulation with *L = 20 nm, a = 5 nm, b = 10 nm,* T_{ox} *= 2 nm,* φ *= 4.5 eV and* V_{GS} *=0.3 V* at different temperature to find the drain current in Fig. 4.2. It has been observed that as the temperature increases, the drain current also increases. This shows the reliability of the CSDG MOSFET at cryogenic temperature. Also, at *100 K*, the drain current of CSDG MOSFET is *2.7 mA*, which is maximum it can go at that temperature. However, as the temperature exceeds *100 K*, irregularity becomes obvious in the performance of the CSDG MOSFET and a decline in the drain current. The CSDG MOSFET produce an optimal performance at about *100 K* but beyond that, the CSDG MOSFET's performance isn't reliable as with other MOSFET types at higher temperature.

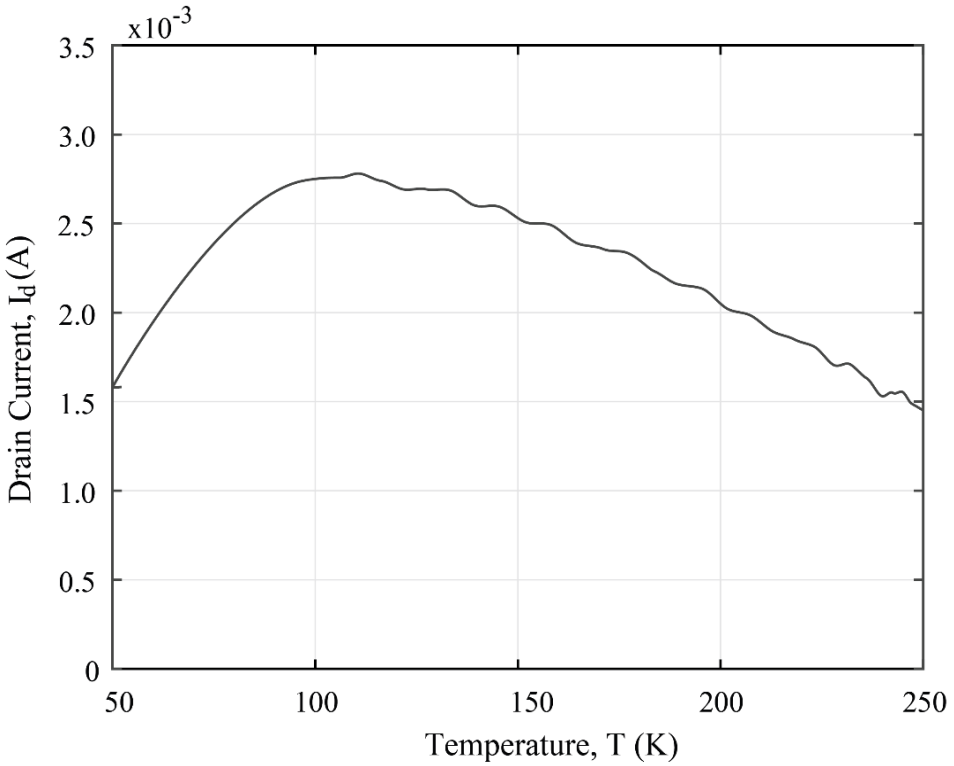


Figure 4.3 The variation of the drain current (I_d) of the CSDG MOSFET with range of temperature (K).

4.3.2 Thermal Effect on Transconductance

Since drain current is known to be the monitor for device temperature, the efficiency of the CSDG MOSFET can be measured w.r.t temperature. From the analysis of the drain current with temperature, the transconductance of the CSDG MOSFET can also be analysed. This is possible because the transconductance is the ratio of the drain current to the gate-source voltage. From the Eq. (4.5) and Eq. (4.6), differentiating the drain current (I_D) with respect to the gate-source voltage (V_{GS}) at a constant drain-source voltage (V_{DS}) explains the transconductance. The transconductance is verified by simulation with the parameters used in section 4.3.1. It is discovered that since the saturation current increases with decreased temperature, so it is expected from transconductance. From Fig. 4.3, it is observed that transconductance is steady with temperature change until little above *100 K*, where it begins to fall gradually. Between *100 K* and *150 K*, the decline isn't too obvious but beyond *150 K*, the decline in the transconductance becomes noticeable. This shows that the effectiveness of the CSDG MOSFET can be measured at temperature less than *100 K*, but above *150 K*, the device becomes not too reliable. However, to avoid this, some precautionary measure will be considered in further sections.

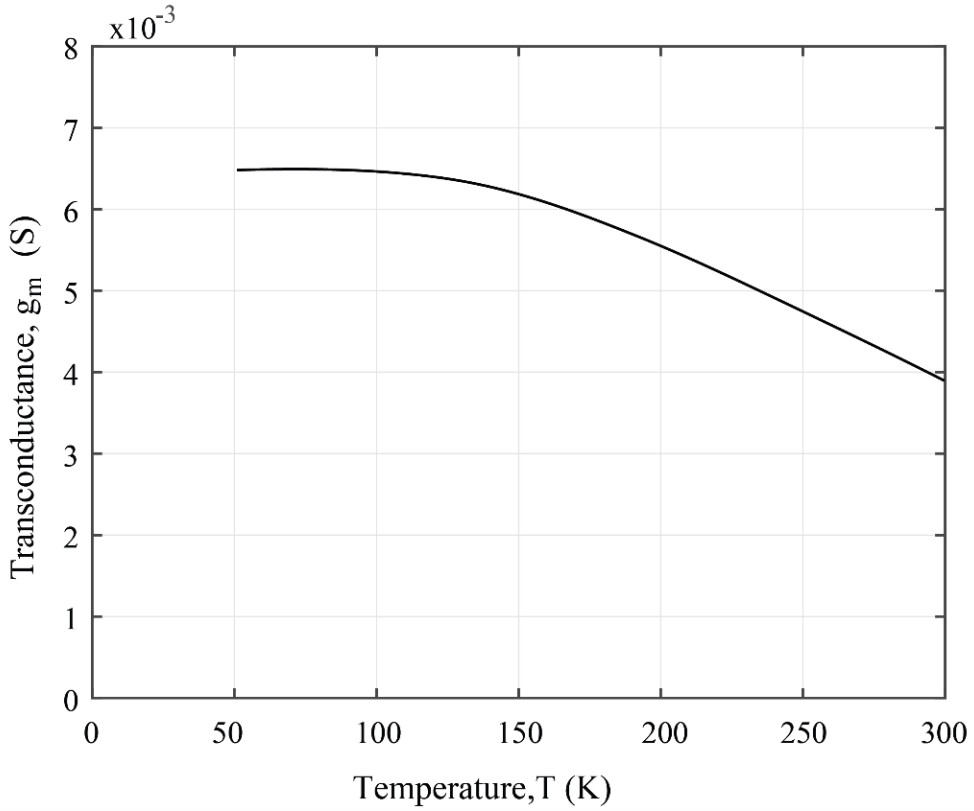


Figure 4.4 Variation of transconductance of the CSDG MOSFET with temperature range to measure effectiveness.

4.3.3 Thermal effect on Carrier Mobility

The carrier mobility is an important parameter of the CSDG MOSFET as it affects all other parameters. It is essential to consider this parameter with respect to temperature. The motion of the electrons along the conducting channels and how it is affected by temperature explains the mobility. As higher the electron motion in the conducting channels of the CSDG MOSFET, efficiency of the device will be better.

Factors that affect the carrier mobility in the CSDG MOSFET are the electric field, scattering mechanism, temperature among others. Electric field is generated from the gate-source voltages (V_{GS}) applied at the two gates of the CSDG MOSFET. Since the CSDG MOSFET is characterized by lower threshold voltage, the applied V_{GS} help the electron mobility to increase until a saturation point is reached where the drain current becomes steady.

In the design of this improved structure, carrier mobility has been considered and it reflects in the undoped property of the conducting channels, and the channel lengths not extensive like previous structure. With the undoped channel length, various scattering

mechanism become negligible due to lack of impurity doping. However, the electron-electron collision is a scattering mechanism to consider.

Also, another factor that affect electron mobility to be considered is the temperature. In the CSDG MOSFET, it has been discovered that at a cryogenic situation, the drift current increase with increase in temperature. This also increases the carrier mobility from the relationship established in Section 3.3.3:

$$E = \frac{\lambda(a+b)}{2\pi ab\varepsilon_0} \tag{4.9}$$

$$\mu = \frac{2\pi\varepsilon_0}{\lambda}\left[\frac{ab}{a+b}\right]v_{d_{CSDG}} \tag{4.10}$$

$$\mu = \frac{2\pi\varepsilon_0}{\lambda T}\left[\frac{ab}{a+b}\right]v_{d_{CSDG}} \tag{4.11}$$

where E and λ are the electric field and electron per unit respectively, a and b are the internal and external radii respectively and ε_0 and v_d are the permittivity and drift velocity, respectively. However, the drift velocity increases until the temperature attains the point where electron to electron collision becomes very significant, making electron mobility to reduce as the temperature increases. This can be verified in Fig. 4.4.

It is observed from Figure 4.4 that the carrier mobility in the CSDG MOSFET is inversely proportional to temperature and as such the carrier mobility increases as the temperature decreases. This can be attributed to the modality in the radius of the device, because as the radius decreases, the electron mobility when temperature rise is increased. This increase in mobility cause collision among the electrons, making mobility to decline and by extension affects other parameters. The CSDG MOSFET possessive an adaptive temperature ability, however the temperature should not be increased beyond $100\ ^0C$ as it affects the reliability of the device and damage the device in the process.

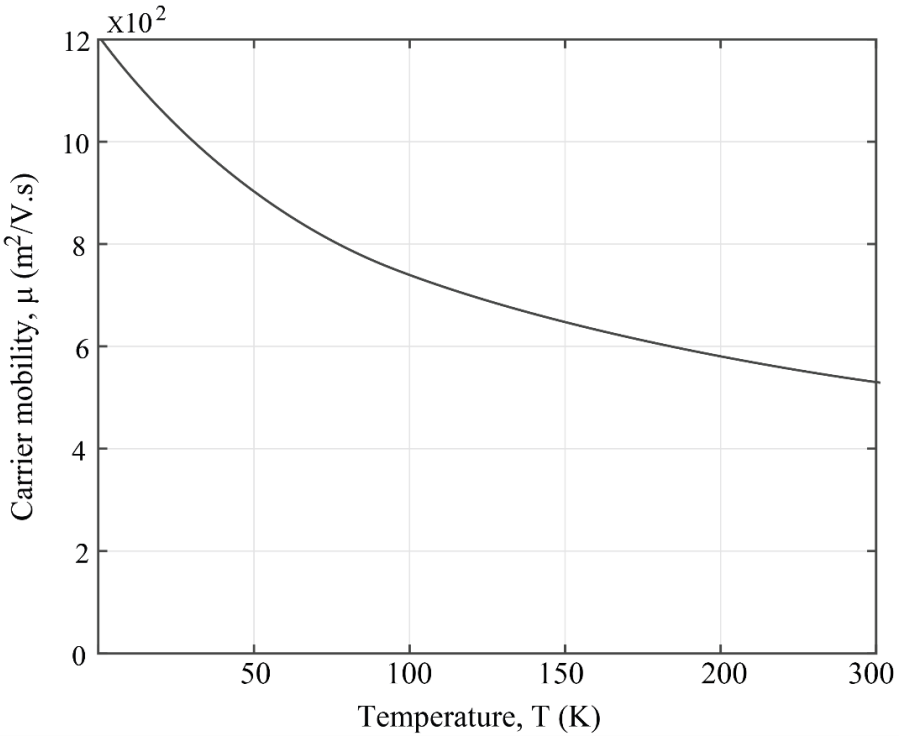


Figure 4.5 The graph of carrier mobility of the CSDG MOSFET against temperature.

4.4 Thermal Stability Model in CSDG MOSFET

Thermal instability is a phenomenon experienced from the application of MOSFET in electronic circuitry. It was discovered that beyond its Safe Operating Area (SOA), the device becomes unstable and unreliable due to the internal and external heat influences on it [97]. Internal heat influences due to the stuffing of many passive devices into a chip and external heat influence due to MOSFET contact with its surrounding and impact of temperature changes experienced.

The CSDG MOSFET has been analyzed with respect to temperature, however it is a necessity to get thermal stability of the device. This MOSFET is made of millions of passive devices stuffed in it. This could also cause internal thermal instability in the device. Also, another cause of instability is the external heat generated from the surrounding of the device.

Ball [98] proposed a way of overcoming the thermal challenges in MOSFET by introducing a monolithic approach by integrating a controller with MOSFET to detect when the device is heated and needed to be protected. This approach is appreciable except that it will substitute for the reliability of the MOSFET. In the novel CSDG

MOSFET, this approach is not applied but an appropriate approach from the architectural fabrication of the device.

The thermal challenge has been combated a bit in the proposed improved CSDG MOSFET structure. To limit the internal heating in the device, a hollow which is determined by the radius of the internal structure analysed in section 3.3.3 is involved. This is fabricated to allow air, a substance of very low thermal conductivity to flow through the device, in turn reducing the effect of the internal heating generated by the device. This is one of the improvements that the previous propose structure did not include.

The external heating is also limited by the cylindrical structure of the CSDG MOSFET, which has little contact with the board it is mounted upon. The part of the device in contact with the board is the external gate and the heat effect of this contact can be eliminated with the involvement of a heat sink on the board it is mounted. Also, to analyse if the circuitry in which the CSDG MOSFET is employed can be functional without the heat sink, the power dissipated can be calculated as:

$$P_{\max} = R_{\theta_{CSDG}} * I^2 \tag{4.12}$$

The maximum power the CSDG MOSFET can dissipate can also be calculated as:

$$P_D = \frac{(T_{\max} - T_{amb})}{R_{\theta_{CSDG}}} \tag{4.13}$$

where T_{max} is the maximum temperature the CSDG MOSFET can adapt to (range of *100 K – 150 K*), $T_{amb.}$ is the ambient temperature (about *25 K*) and $R_{\theta(CSDG)}$ is the thermal resistance of the CSDG MOSFET. The heat sink can be ignored for the CSDG MOSFET when the dissipated Power (P_D) is less than the maximum power dissipated (P_{max}) as illustrated in the equations. However, almost at the Tmax, the stability of the CSDG MOSFET is compromise and cause great havoc to the board it is mounted on, however, this is still temperature accommodative compared to the other MOSFET types in Chapter 2.

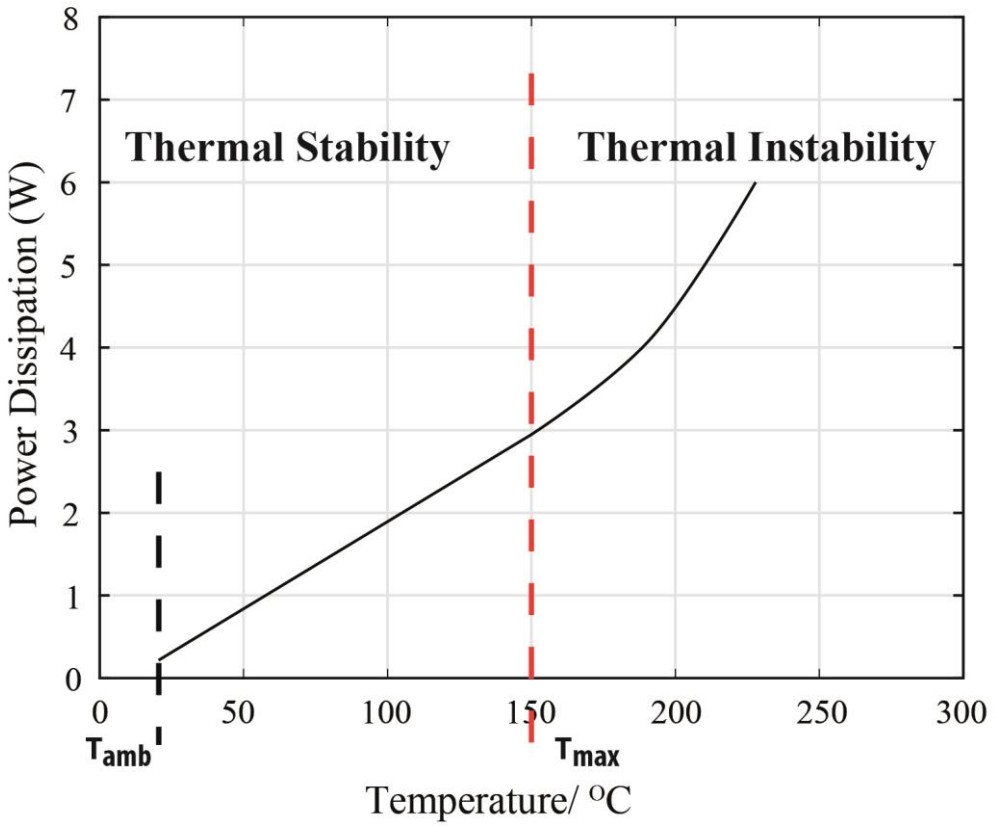


Figure 4.6 Power dissipated in the CSDG MOSFET with respect to Temperature changes.

4.5 Thermal Noise in CSDG MOSFET

Due to the shrinking of the MOSFET to achieve better performance in application, the thermal noise in the device becomes more pronounced. Although, it is always predicted that thermal noise in short-channel MOSFET is higher than that of high-channel MOSFET, this can be true but not with excess factor [99, 100]. With the factor of channel length and rise in temperature in the CSDG MOSFET, the agitation along the channels become noticeable even at zero applied gate-voltages (V_{GS1}=V_{GS2}=0).

Thermal noise in the CSDG MOSFET is expected to be conspicuous due to its nanoscale region of operation and the double channel it possesses. However, a proposed model to reduce the thermal noise in the CSDG MOSFET is being introduced. Observing the charged-based proposal for Power Spectrum Density (PSD) at gradual channel approximation of the thermal noise in MOSFET given as [101]:

$$\delta_{id} = \frac{4kT\mu q}{L^2} \tag{4.14}$$

where T and μ are the temperature and charge carrier mobility along the channel respectively, while Q_{ch} and L are the total charges along the channel and length of the channel. Although Eq. (4.14) above was modelled for long channel MOSFET, but it was discovered that its effect can be used to reduce the short channel effect through increased transconductance value which CSDG MOSFET possesses.

Also, the Eq. (4.14) is valid only if the drift current has little or no effect on the charge transport along the channels of the CSDG MOSFET. However, the diffusive random current has large effect on the transport of the charges causing a significant effect on the thermal noise generated in the CSDG MOSFET. And since the thermal noise is dominant at the linear (Ohmic) region of the CSDG MOSGET, this region will be used to analyse the thermal noise of the device.

Likewise, short channel separations in CSDG MOSFET cannot be possibly seen as a resistance due to degradation of carrier mobility by lateral generation of the electric field [102], because of this condition, the thermal noise will be considered at the gradual channel region. Considering of the channels in the CSDG MOSFET with respect to the dominance of the diffusive random current, the thermal noise can be given as:

$$\delta i_n^{\,2} = 4nq^2 D\Delta f \frac{W}{L} \tag{4.15}$$

where n and D represents the carrier density and diffusion constant respectively and Δf and W represents the band width measurement and width of the channel. Due to the degraded carrier mobility effect, the drain current can be calculated as:

$$I_d = \mu n W q(V) \frac{\partial V}{\partial L} \Bigg/ \left(1 + \frac{\partial V / \partial L}{E_C} \right) \tag{4.16}$$

The E_C is the critical electric field at the point where the carrier velocity will become saturated. The Eq. (4.16) can be integrated with respect to applied voltage along the channels from the source to the drain and the noise of the noise can be expressed as:

$$\Delta I_d = \delta i_n \frac{\mu n W q(V) \Delta V}{L + \frac{V_{DS}}{E_C}} \tag{4.17}$$

From Eq. (4.17), the two channels of the CSDG MOSFET can be expressed as:

$$i_{dn}{}^2 = \sum \left[\Delta I_d \right]^2 \tag{4.18}$$

Substituting Eq. (4.15) and Eq. (4.17) into Eq. (4.18) produces Eq. (4.19) which is expressed as:

$$i_{dn}{}^2 = \sum 4nq^2 D\Delta f \frac{W}{L} . \left[\frac{g_{th} \Delta V^2}{\left(L + \frac{V_{DS}}{E_C} \right)^2} \right] \tag{4.19}$$

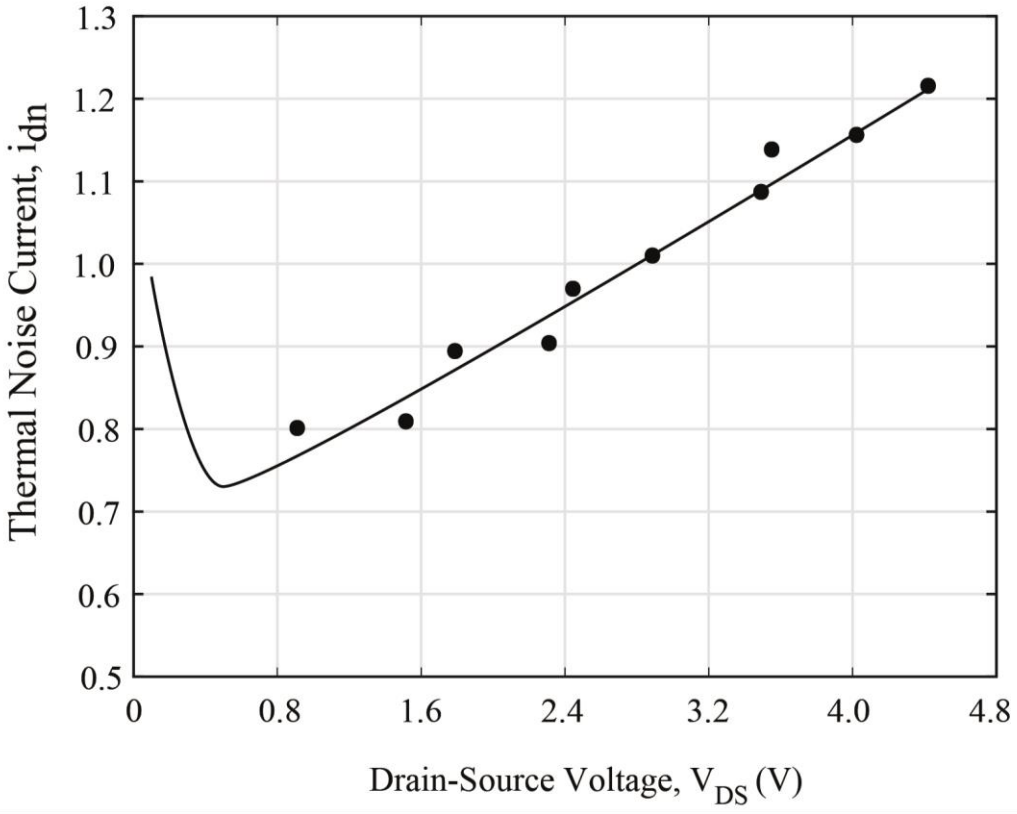


Figure 4.7 Thermal noise current in the CSDG MOSFET with respect to Drain-source Voltage.

where g_{th} represent the product of mobility, number of charges, charges along the channel and width of the channel with respect to the applied voltages, $\mu nWq(V)$ at the gates of the CSDG MOSFET. It has been observed that thermal noise current in CSDG MOSFET is higher due to the carrier heating effect examined with to the gradual channel approximation. This fact helps to appreciate the application of the device in Nanotechnology. Although, thermal noise in MOSFET have been very controversial due to different assumed models and variation, but this research work has been able to develop a physics-based model for drain thermal noise current with carrier heat effect consideration. The resulting model shows the importance of the carrier heat effect at gradual channel region with voltage biasing almost at V_{DS}. This shows a greater and more influential thermal noise drain current at higher applied voltage.

4.6 Conclusion

In this chapter, the effect of heat on the CSDG MOSFET is presented. The CSDG MOSFET was analysed under the influence of temperature change during its utilization. To achieve this, the thermal resistance was first modelled, and a reduced thermal resistance was derived. The thermal effect on the parameters of the CSDG MOSFET was then analyzed with a verification of the suitable temperature that the CSDG MOSFET is best used. The noise generated due to the heat has been a bit complex to analysed, but it was analyzed and some suggested possible ways to stabilize the thermal effect on the CSDG MOSFET explained. The CSDG MOSFET has been an improved device in the nanotechnology and VLSI application and it has the capability to withstand the internal and external heat generated in the process.

CHAPTER 5

APPLICATIONS OF CSDG MOSFET

5.1 Introduction

In the modern electronic devices, there are billions of transistors, resistors and capacitors on a single IC chip that make them work effectively and efficiently. One of these vital components is the MOSFET due to its high input impedance, switching speed, and other advantages [14, 92]. By its high input impedance, it becomes useful for devices with a low current circuit to operate. These parameters make MOSFET essential in VLSI, and microelectronic circuits, where power consumption has been a major challenge [103]. The physical structure of the MOSFET permits the movement of carrier through the channel formed between drain and source. This flow helps in fast switching speed of the MOSFET. The intensity of the channel formed is the amount of voltage applied to gate of the MOSFET [8, 104]. The fabrication of MOSFET on a silicon-body came into existence in the 1960s. Its primary application has been as a switching device and in amplification of electronic signals [105]. However, it has become useful in the digital applications such as the fabrication of logic gates, digital memories and flip-flops etc. [106]. Its relevance as a switch is due to its flexible design and operation. The capacity to accommodate improvement in performance and the design of the gate-insulator with small channel length has enabled it to operate at low voltage. This has therefore made MOSFET a basic cell of electronic devices [84].

This transistor also acts as an amplifier where increase or decrease of the output voltage is needed as per the application requirements. For MOSFET to operate as an amplifier, the gate-source voltage must be greater than threshold voltage to achieve saturation. In this configuration, the input voltage is directly proportional to the drain current.

The dynamics of the MOSFET have been reviewed in Chapter 2 of this work. This led to the earlier discussion on the CSDG MOSFET. The CSDG MOSFET demonstrates a sharp subthreshold, increased current drive, higher switching speed and low leakage current due to Short Channel Length (SCL). The surrounding gate of the CSDG MOSFET helps in controlling short channel effect as voltage applied at each gate affects the formation of the channels. Also, it was discussed in Chapter 3 of this work, the

modelling of a small signal that capacitance exists within the devices due to the fabrication procedure. The various parameters that are important in the fabrication constant for small signal model were also analysed. Firstly, the area of the device due to its structure is less in comparison with other MOSFET types. Secondly, the total resistance in the device is minimal as discussed in Chapter 4, which gives a higher current than the other MOSFET type. Finally, the oxide capacitance was calculated and factors like thickness, radii were considered to derive this. In the present chapter, the CSDG MOSFET is analysed to integrate its advantages in modern domestic and electronic devices to achieve low power consumption, switching speed, high impedance, among others. These are done in the application of the CSDG MOSFET as an amplifier that has been discussed in this chapter.

5.2 CSDG MOSFET as Mixer

The CSDG MOSFET like other transistor types can be used as a switch such that the device is at OFF-state when the input voltage is below the threshold voltage, and ON-state when it is above the threshold voltage. This is made possible by the formation of the conducting channels along the drain and the source. Also, as considered in section 3.3.6 of this research work, there are many capacitors in the CSDG MOSFET, such as the gate-source capacitance of the internal radius (C_{GS1}), gate-source capacitance of the external radius (C_{GS2}), gate- drain capacitance of the internal radius (C_{DG1}), gate- drain capacitance of the external radius (C_{DG2}), drain-source capacitance of the internal radius (C_{DS1}), drain-source capacitance of the external radius (C_{DS2}) that make this switching process possible. Furthermore, this device primarily fits as a switch because of its switching speed ability and setup. The CSDG MOSFET enjoys low threshold voltage characteristics, hence a suitable ON-resistance for low power consumption devices.

The CSDG MOSFET has the advantage of higher switching speed unlike the traditional switches. This is due to its ability to reduce the conduction losses by minimized channel resistance and parasitic capacitance [107]. *Srivastava* [108] have proposed a circuit-level model to establish the switching speed of the CSDG MOSFET. In this analysis, the effect of the parasitic resistance and capacitance was examined. It was discovered that the switching speed of the CSDG MOSFET was derived to be 4.17 kHz which is better when compared with other traditional MOSFETs.

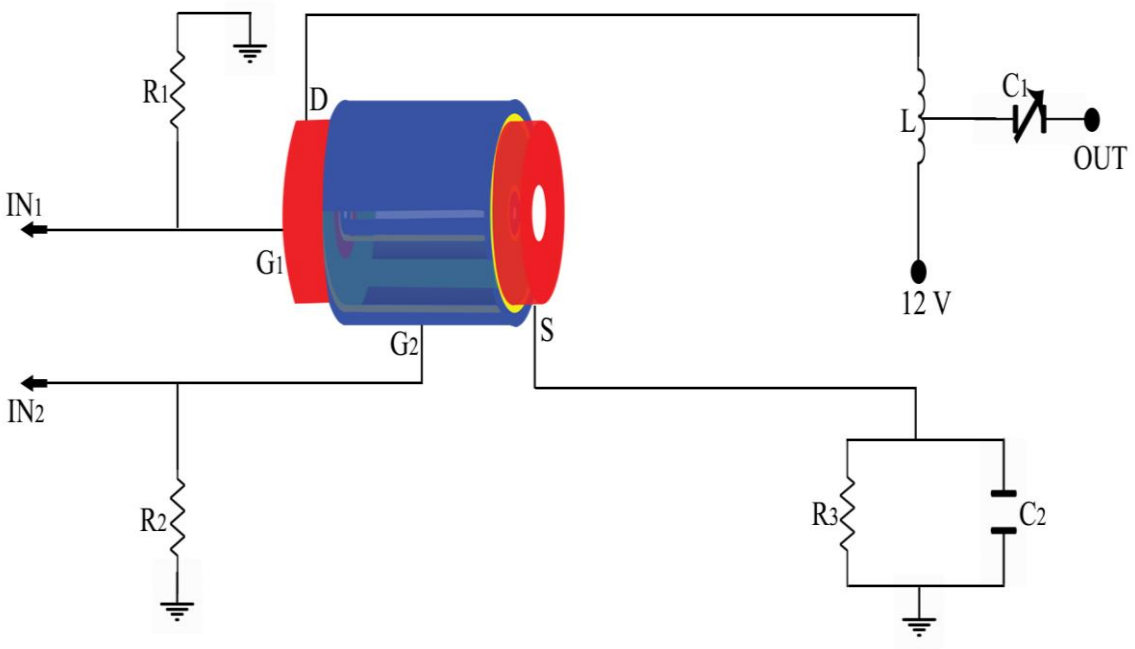


Figure 5.1 Circuit analysis of the CSDG MOSFET as a mixer.

This switching attribute of the CSDG MOSFET in passive mode was employed in a mixer circuit. In Fig. 5.1, the two gates are biased with two signals to produce a desired output. It could be mixed signals of video and audio biased at the two-gate electrode to transmit at a required frequency. To transmit a signal of between *40 – 60 MHz*, two signals of *10 MHz* and *50 MHz* can be biased to the two inputs (*IN1* and *IN2*) as shown in Fig. 5.1. The CSDG MOSFET mix the two signals to produce the require frequency using the inductor (*L*) and variable capacitor (*C1*) to turn the output signals as desired. The resistor (*R3*) and capacitor (*C2*) are to limit the current through the device, as it could destroy the CSDG MOSFET. The CSDG MOSFET is a very useful device in this application because of the intrinsic gate-capacitors that help to prevent adding many capacitors at the gate input.

Also, it was discovered that two of the CSDG MOSFET can be used to replace the convention tetra-diode operation for rectification with reduced power loss. This makes this device usable for domestic appliances that require low power for operation. Examples like the *BriTeq BT-VMS3*, *Roland VR-4HD Mixers*, *Videonics Sound Effects Mixer* can be improved with the application of the CSDG MOSFET to enjoy better current drives, increased switching speed and low power consumption characteristics. Also, capacitance within this device helps in filtering AC signal during amplification. This has been discussed in the following section.

5.3 CSDG MOSFET as Rectifier

Another aspect of application that the CSDG MOSFET can be utilized is as an energy harvesting system. Most harvesting system has low output voltage of about *0.2 V – 0.6 V* [109]. In a successful energy harvesting system, AC/DC converter is an essential circuitry. Since the domestic appliances utilize a DC voltage, but the power generated and distributed is an AC voltage, there is a need to convert this AC voltage to DC voltage. The rectifier is used to do the conversion and conventionally done with the use of a diode.

With the introduction of a MOSFET, it started replacing the conventional diode for rectification. *Mihaiu* [110] proposed an ideal rectifier using multiple MOSFET and diode devices which are supplied with capable voltage to charge the capacitance in the MOSFET. However, these analysis in discovered to have high power consumption and conduction losses which could generate heat and with continuous use damage the devices in the configuration. *Zhong et. al.* [111] also ianalyzed using a self-driven synchronous rectifier to replace the conventional power diode rectifier for a low voltage power consumption application. The analysis could replace the conventional diode rectifier configuration except for the greater power loss of about *50 %* experienced by the configuration and increased component counts as it involved many MOSFETs and diodes among other components.

The switching and structural advantage of the CSDG MOSFET will be utilized to model a rectifier circuit. Instead of the multiple components used in the configuration of the rectifier, the double channel attribute of the CSDG MOSFET and with configuration, two CSDG MOSFET type (n-channel-CSDG MOSFET and p-channel-CSDG MOSFET) will be employed for the two-half cycle rectifier configuration.

A sinusoidal AC signal is applied at points A and B for the two-half cycles of the rectification process as shown in Fig. 5.2. At the positive half cycle, the point A is positive w.r.t. to B and a positive voltage above threshold voltage is applied at the external gates of the two CSDG MOSFET ($_nG_2$ and $_pG_2$), while the internal source of the n-channel-CSDG MOSFET ($_nS_1$) and internal drain of the p-channel-CSDG MOSFET ($_pD_1$) are positive biased respectively. This produces a flow of current in the external channel of the n-channel CSDG MOSFET and internal channel of the p-channel CSDG MOSFET types.

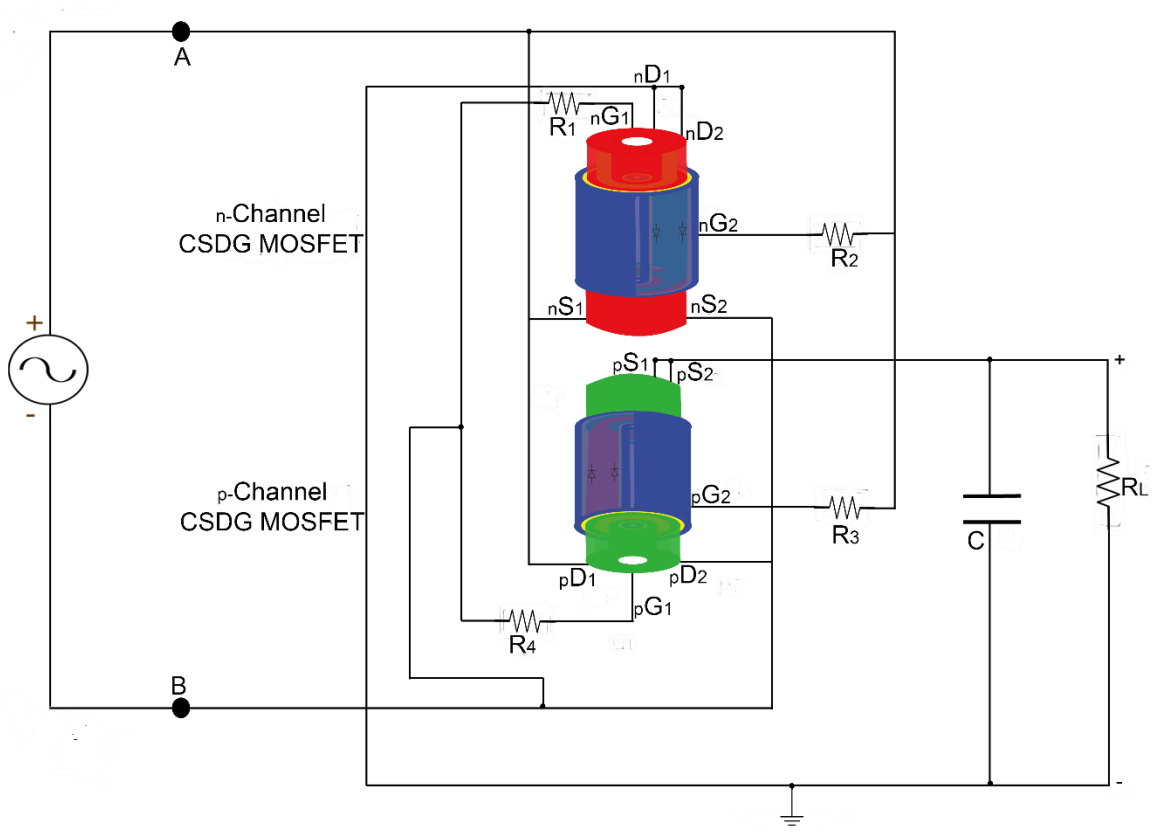


Figure 5.2 Circuit diagram of the CSDG MOSFET bridge rectifier [112].

This is also applicable in the negative-half cycle also, the point B is positive w.r.t. point A, and the internal gates of the two CSDG MOSFET ($_nG_1$ and $_pG_1$) are positively biased with the external source of the n-channel-CSDG MOSFET ($_nS_2$) and external drain of the p-channel-CSDG MOSFET ($_pD_2$) are positive biased respectively. At this point the internal channel of the n-channel CSDG MOSFET and the external of the p-channel CSDG MOSFET allows the flow of current as the resistance is being overcome. This configuration is better than the convention multiple diodes and MOSFETs configuration because of its economical and less compartment of component attributes. For the analysed full-wave rectifier, it can be expressed as:

$$\eta_{CSDG} = \frac{P_{DC}}{P_{AC}} * 100\% \tag{5.1}$$

where

$$P_{DC} = I^2_{CSDG} R_L \tag{5.2}$$

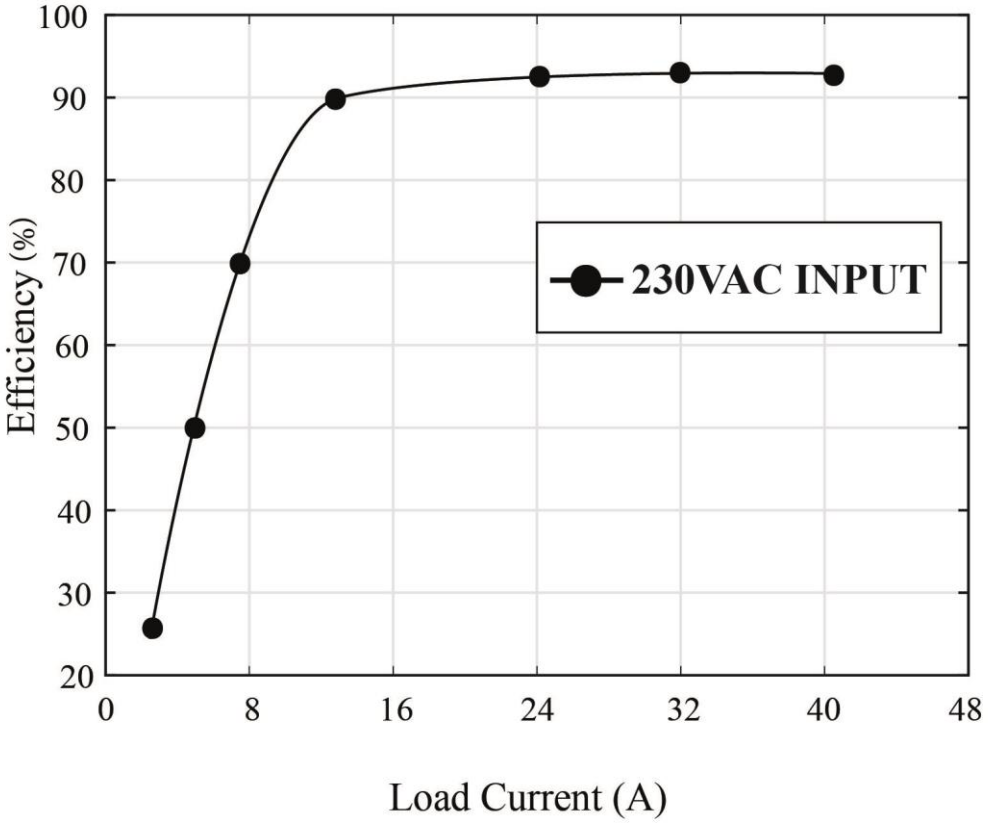


Figure 5.3 Efficiency in the CSDG MOSFET against the Load current.

From Eq. (5.2), it is observed that beyond the mentioned advantage the application of the CSDG MOSFET has in rectification, the rectification ratio is higher than others. Also, as the load current increases, the efficiency tends toward perfection with an applied 130 V AC input. In the equation, the power of the DC voltage is higher due to higher current drive attributed with the CSDG MOSFET. And the device's in-built capacitors help in the filtering process.

5.4 CSDG MOSFET as Amplifier

For a MOSFET to amplify, it must satisfy the saturation condition, which states that the drain voltage must be greater than the subtraction of the threshold voltage from the source-gate voltage ($V_{DS} > V_{GS} - V_{th}$). For the device under consideration, the cylindrical structure and double channel formed in this MOSFET help in minimizing the threshold voltage, also with the reduction of the body effect of the device.

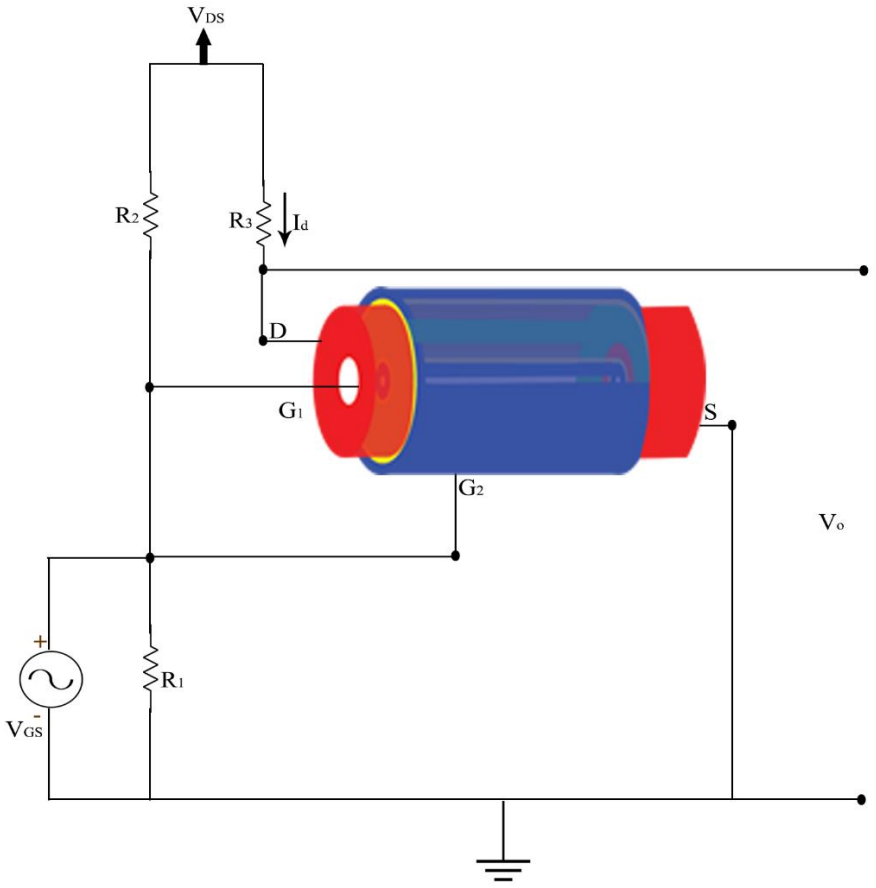


Figure 5.4 Circuit diagram of the CSDG MOSFET based amplifier [93].

In Fig. 5.3, the application for amplification is arranged in a manner where small signal / voltage is applied to both the internal and external gates of the CSDG MOSFET device with the internal and external sources grounded. The output current of the internal structure (I_{D1}) is then added to the output current of external structure (I_{D2}). The total current is converted to voltage to get the output voltage. The amplified voltage then becomes the difference between the product of equivalent drain resistance, which is R_3 in Fig. 5.3 below and total output current from the voltage (V_{DS}) applied at the drains. This output current produces a larger transconductance while output voltage gives a higher voltage gain.

The capacitors found in the CSDG MOSFET with gate-source junction and gate-drain junction helps to filter DC from the output current. The effect of these capacitances is negligible and has not been considered in this process. The mathematical parameters of the CSDG MOSFET have been examined in this section as it relates to amplification and transconductance. These mathematical parameters have been simulated in comparison with CSG MOSFET.

When the small AC signal, V_{GS} is applied at the gates of the CSDG MOSFET, the AC voltage is amplified to produce a large current at the internal drains of this device. The current at each drain is given as:

$$I_{d_1} = \frac{(2\pi a)}{L}\mu_s C_{ox}\left[\int_{\psi_{s0}}^{\psi_{sL}}\left[\left(V_{GS} - V_{FB} - \psi_s\right) + Q_B\right]d\psi_s\right] + \frac{(2\pi a)}{L}\mu_s \Phi_t (Q'_L - Q'_0) \quad (5.3)$$

Eq. (5.3) is the amplified current, but for the whole CSDG MOSFET, the total current will be the sum of the internal amplified current and external amplified. In order get a larger unadulterated output signal, the gate-drain capacitance with large impedance helps to isolate the AC signal from the DC signal. The total output current is given as:

$$I_{d_{CSDG}} = \frac{2\pi(a+b)}{L}\mu_s\left[2C_{ox}\left(V_{GS} - V_{FB}\right) - C_{ox}\left(\psi_{sL} + \psi_{s0}\right) + 2Q_B + (2\Phi_t C_{ox} - Q_B)\right] \quad (5.4)$$

From Eq. (5.4), it has been observed that the total drain current is more when compared to the drain current in the internal cylindrical structure only or DG MOSFET (due to the cylindrical structure of the device). This increase is because of the differences in the internal and external radii. The difference in the radii affects the outcome of the output voltage and can be adjusted to give a better output current. In the equivalent simulation, the internal radius is set to *10 nm*, external radius*20 nm*, and length *20 nm*. The threshold voltage is set to *0.3 V* and the μsC_{ox} is *100 μA/V*^{2}. The gate-source voltage (V_{GS}) of *0.65 V* was applied to the gates of the three devices.

From Fig. 5.4, using the parameters mentioned, it has been observed that as the drain-source voltage (V_{DS}) is increased, the drain current of the three compared devices also increases at the early stage of increment. When the pinch-off is attained, saturation sets in which gives a steady drain current. However, from the variation of the three devices using equal specifications, it is observed that with the same V_{DS} applied to the three types, CSDG MOSFET attained saturation at *1.25 A*. CSDG MOSFET becomes a better device to use for amplification because the ratio of the output voltage to input voltage is higher in CSDG MOSFET than other devices. The advantages of better structure and increased current drive sum up this advantages and help reduced limitations experienced by the other types.

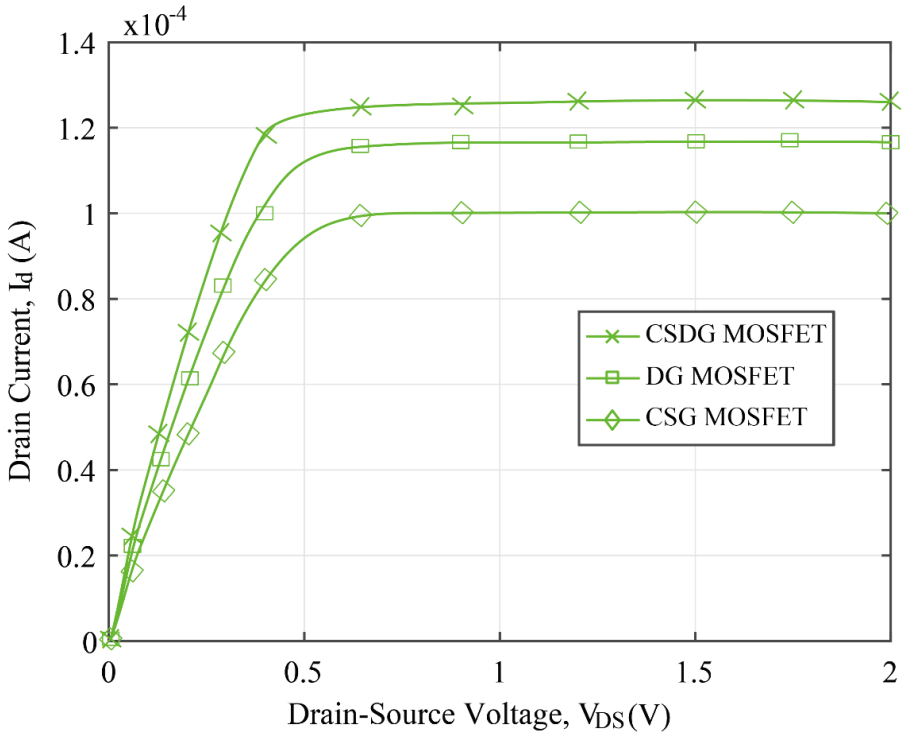


Figure 5.5 Variation of Drain current as a function of Drain-source voltages at equal variables for the CSDG MOSFET. DG MOSFET and CSG MOSFET.

Using Fig. 5.4 in the consideration of the voltage gain in CSDG MOSFET, the resistor R_3 (the drain resistor) is quite important for this voltage gain because it converts the drain current, I_d into voltage. The ratio of the result output voltage, (V_0) to the input voltage (V_{GS}) gives the voltage gain (A_v). Applying transconductance (g_m) of the CSDG MOSFET analysed in chapter 3 to get the voltage gain. Since:

$$g_m = \frac{I_d}{V_{GS}} \tag{5.5}$$

$$V_0 = I_d R_3 \tag{5.6}$$

$$A_v = \frac{V_0}{V_{GS}} = g_m R_3 \tag{5.7}$$

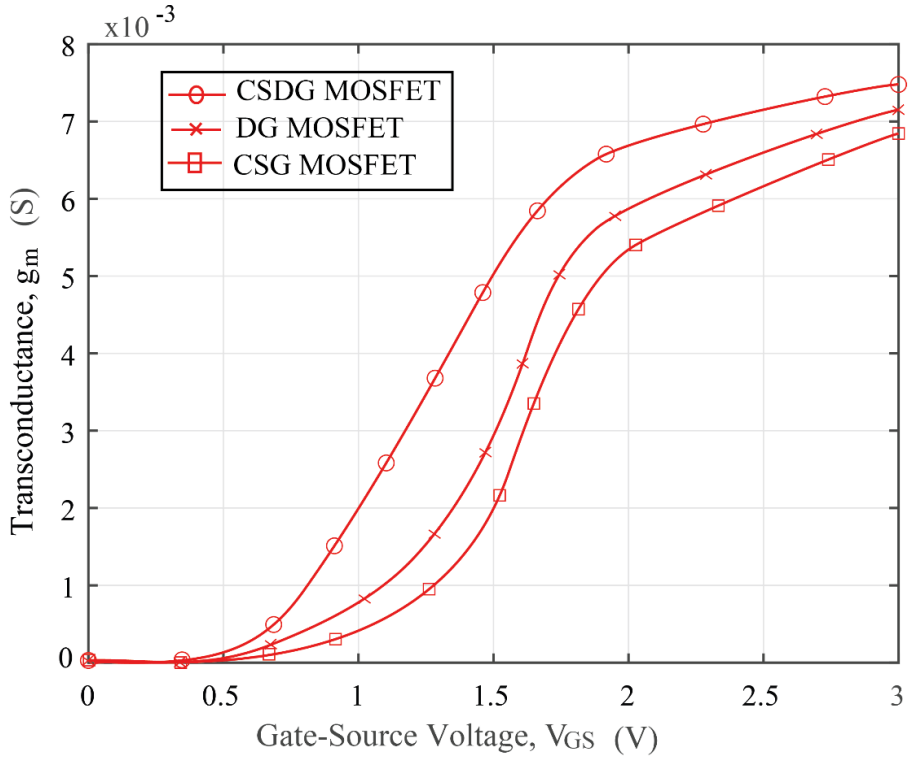


Figure 5.6 Variation of Transconductance as a function of Gate-source voltages at equal variables for the CSDG MOSFET. DG MOSFET and CSG MOSFET.

It is established in Chapter 3 that the sensitivity of the CSDG MOSFET is measured by the Eq. (5.7) varying transconductance (g_m) versus gate-source voltage (V_{GS}).

From Fig. 5.5, it is observed that at *1 V* of the gate-source voltage, the transconductance of CSDG MOSFET is *2 S* unlike the other two compared types. This make the devices applicable for device that requires low voltage input with better output voltage like the cell phones, computers among others. Also, it is observed that as the input drain current increases, the transconductance also increases but due to the dual gate property of the DG MOSFET and CSDG MOSFET, they yield better transconductance than the CSG MOSFET. Also, the CSDG MOSFET due to its cylindrical structure, when voltage applied at a point, it covers the all the region of the gate unlike the DG MOSFET where corner effect hinders the spread of the applied voltage. With this advantage, the value of the drain resistor, R_3 does not matter as it contains sufficient current flow to produce sufficient voltage. This is compensated for in the better transconductance of the CSDG MOSFET, thus resulting to a better amplification.

A single CSDG MOSFET works synonymously and even more than two SG MOSFET cascaded together. It is important to also add that the intrinsic and extrinsic capacitors in the CSDG MOSFET aid the amplification process. Analysing the transconductance with respect to the gate-source voltage is shown in Fig. 5.5 and it is discovered that transconductance in CSDG MOSFET at a given gate-source voltage is more than that of the CSG at the same gate-source voltage. This advantage makes amplification applicable in Radio Frequency switches [84].

5.4 Conclusion

With the advantages stated and the analysis made to evaluate and compare the CSDG MOSFET with other MOSFET-type, it was observed that the CSDG MOSFET is applicable as a switch, rectifier and an amplifier. As an amplifier, output current produces a larger transconductance while output voltage gives a higher voltage gain. With this analysis, the CSDG MOSFET work even better than two conventional SG MOSFET used back-to-back. This was due to the better current drive from the device. It is observed that CSDG MOSFET exemplifies a better application for Nanotechnology, Radio Frequency (RF) communication system among others. This is due to its better current drive, switching speed, better energy storage and amplification analysed in this chapter.

CHAPTER 6

CONCLUSIONS AND FUTURE RECOMMENDATIONS

6.1 CONCLUSIONS

The research work proposes an improved parametric analysis of CSDG MOSFET. This analysis utilizes various models to analyze the parameters of CSDG MOSFET. This analysis was based on the advantages of CSDG MOSFET and how to derive the best use for its application at different thermal range.

The first chapter presents a general introduction of the thesis. The background study of the MOSFET was examined, where the revolution from thermionic valve into a suitable MOSFET device was discovered. Also, the MOSFET was categorized into its mode-types and channel-types with its basic activation modes explained. The MOSFET has encounter its limitations since introduction like the SCE, thermal effect, among others. To overcome these challenges, different solutions have been proposed. But due to the thermal challenges that accompany the device, our research motivation was born on how to design a MOSFET type that best solve the challenges as well as defeat the thermal challenges.

In the second chapter, the structure and operation of the MOSFET with its different regions of operations; saturation, triode and cut-off regions was explained. Then to further get a better understanding into the research work, the various parameters of the MOSFET was analyzed. The Simple Charge Control Model (SCCM), Meyer Model (MM), and Velocity Saturation Model (VSM) approaches were used to explain the drain current of the MOSFET with their shortcoming pointed out, also the surface potential for the MOSFET was also analysed. In a bid to overcome the SCE, among other challenges in MOSFET, the Double-Gate (DG) MOSFET was introduced to have an excellent electrostatic control on the channels in the MOSFET. This became a basis for modification to get the best performance from the MOSFET types. The Cylindrical Single Gate (CSG) MOSFET was also reviewed due to the cylindrical dimension it possess. This review introduces MOSFET structure utilized in this thesis, which is the CSDG MOSFET. The different structures proposed by different researchers were

highlighted and their significance examined. Also, the mathematical analysis of the CSDG MOSFET was analyzed.

The chapter three presented a new structure of the CSDG MOSFET. This structure is an extension of the DG MOSFET with a cylindrical rotation along one of its gates. With this improvement, the parameters of the CSDG MOSFET were discussed. In this discussion, the drain current of the improved CSDG MOSFET was analysed with the drift-diffusion model. The model discussed drift and diffusion components of the CSDG MOSFET to derive a dynamic drain current. The transconductance, which also a follow up from the drain current was explained and verified. One of the essential parameters of the CSDG MOSFET, which is carrier mobility was analysed in this chapter. In the parameter, Gauss's law was use to explain the dynamism that is being enjoyed in the radii of the CSDG MOSFET. The chapter also analyzed the capacitance characteristics in the CSDG MOSFET and the role they play in the effectiveness of the device.

The thermal effect on the CSDG MOSFET was presented in chapter four, the CSDG MOSFET was analysed under the influence of temperature change during its utilization. The thermal resistance was modelled and a reduced thermal resistance was derived. The thermal effect on the parameters of the CSDG MOSFET was then analyzed with a verification of the suitable temperature that the CSDG MOSFET is best used. The noise generated due to the heat was also analyzed and some suggested possible ways to stabilize the thermal effect on the CSDG MOSFET explained.

In the last chapter, the application of the CSDG MOSFET was presented. In this chapter, it was explained that the CSDG MOSFET is applicable as a switch, rectifier and importantly as an amplifier. In its application as an amplifier, it was discovered that the V_{DS} is increased which also cause a greater voltage gain in the device. The CSDG MOSFET was discovered to have better amplification than the DG and CSG MOSFET with better efficiency in its application in the VLSI and nanotechnology designs.

In this research work, we have design a novel CSDG MOSFET was proposed with some enabling models for the parameter of the device. The architecture of this device has been done with the mind-set on how to overcome the challenges of short channel effect, thermal effect, punch-through effect among others discussed in this work. Suitable models have been used for the analysis of the parameters of CSDG MOSFET to get the best from the device. And, its thermal effect has been analysed with a suitable thermal

resistance advantage modelled. Our proposed model is in line with the existing model and has better and improved parameters.

6.2 FUTURE RECOMMENDATIONS

An improved analysis of the new structure CSDG MOSFET has been analyzed and the result shows a good performance especially as it concerns temperature change. However, it is recommended that some different models possibly the ballistic transport using Green's function approach and/or semi-classical approach could be undertaken. The basic for other approach could be easily done since this approach here shows a suitable result. Also, since the CSDG MOSFET type used in this research work is the n-type enhancement type, the p-type enhancement type could also be analysed and compared with the type used in this research work.

Also, in the structural built-up of the device, instead of the silicon oxide used as the gate dielectric, other compounds can be utilized like Hafnium dioxide (HfO_2) and Aluminium oxide (Al_2O_3). The dimension of the gate dielectric could also be varied to get the better of improved reaction in the CSDG MOSFET. Furthermore, this research work was able to review a type of noise (thermal noise), other types of noise like flicker noise, 1/f noise, resistive poly gate noise among others can be review and analyzed.

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