

**MODELLING AND ANALYSIS OF
INVERTER-BASED FACTS DEVICES
FOR POWER SYSTEM DYNAMIC STUDIES**

by

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Submitted in fulfillment of the academic requirements for the degree of Doctor of Philosophy, in the School of Electrical, Electronic and Computer Engineering, University of KwaZulu-Natal, Durban, South Africa.

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I hereby declare that all the material incorporated into this thesis is my own original and unaided work except where specific reference is made by name or in the form of a numbered reference. The work contained herein has not been submitted for a degree at any other university.

Signed: 

F-W Huang

for my family

ABSTRACT

Flexible AC Transmission Systems (FACTS) involves the incorporation of power-electronic controlled devices into ac power transmission systems in order to extend the power-transfer capability of these systems beyond their traditionally accepted boundaries. One particular category of FACTS devices makes use of high-powered voltage source inverters to insert near-sinusoidal ac compensating voltages into the transmission system. This thesis considers this particular category of inverter-based FACTS devices, namely the static synchronous compensator (STATCOM), static synchronous series compensator (SSSC) and unified power flow controller (UPFC).

Although the potential for FACTS devices to enhance the operation of power systems is well known, a device such as a UPFC is itself a complicated subsystem of the overall power system. There is therefore also the possibility that the introduction of such devices could cause adverse interactions with other power system equipment or with existing network resonances. This thesis examines the interactions between inverter-based compensators and a particular form of system resonance, that of subsynchronous resonance between a generator turbine shaft and the electrical transmission network.

The thesis presents a review of the theory of operation of high-power, multi-pulse inverter topologies actually used in transmission-level FACTS devices. Detailed simulation models are developed of both two-level and three-level multi-pulse inverters. With appropriate controls, simulation models of both the SSSC and STATCOM, and a full UPFC are then developed using these detailed inverter models and the results from these simulation models compared against other results from the literature. These comparisons show favourable agreement between the detailed FACTS models developed in the thesis and those used by other researchers. However, the models presented in this thesis include a more detailed representation of the actual power-electronic circuitry and firing controls of inverter-based FACTS devices than is the case with other models used in the literature.

The thesis then examines the issue of whether the introduction of an SSSC to a transmission system could cause subsynchronous resonance (SSR). SSR is a form of dynamic instability that arises when electrical resonances in a series capacitively compensated transmission line interact with the mechanical resonances of a turbo-generator shaft system. The detailed SSSC simulation model developed in the thesis is used to determine the impedance versus frequency

characteristics of a transmission line compensated by an SSSC. The results confirm earlier work by others, this time using more detailed and realistic models, in that the introduction of an SSSC is shown to cause subsynchronous resonance.

The thesis then considers the addition of supplementary damping controllers to the SSSC to reduce subsynchronous oscillations caused both by the SSSC itself as well as by a combination of conventional series capacitors and an SSSC in a representative benchmark study system. The results show that subsynchronous oscillations in the transmission system compensated solely by an SSSC can successfully be damped out using a single-mode supplementary damping controller for a range of values of SSSC series compensation. However, in the case of the transmission system compensated by both conventional series capacitors and an SSSC, the nature of the subsynchronous oscillations is shown to be complex and strongly multi-modal in character. The thesis then proposes an extension to the single-mode supplementary damping controller structure that is better suited to damping the multi-modal resonances caused when an SSSC and conventional series capacitors are used together to compensate a transmission line. The results obtained from this multi-modal controller indicate that it is able to stabilise SSR for a range of compensation values, but that the controller design needs to be adjusted to suit different values of compensation.

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X_L	transmission line reactance
X_q^*	commanded reactance from the SSSC
k	degree of compensation
γ	dead angle
σ	conduction angle
ρ	relative phase angle for the phase shifting trasnsformers

General Symbols

pu	per-unit
$[C]$	transformation matrix C
$[C_I]$	time-varying transformation matrix C_I

CHAPTER ONE

INTRODUCTION

1.1 Flexible AC Transmission Systems (FACTS)

1.1.1 Background

The unprecedented rate of human population growth in the past century demanded increasing amounts of energy for the purpose of farming, manufacturing, transportation and other economic sectors. Since the beginning of the 1990s, the global energy demand surged at an alarming rate, primarily due to the rapid growth of industrializing nations, particularly, China and India [1,2]. A study conducted by the British power company, PowerGen, reported in September 1997 that “Global energy demand is forecast to double by 2020” [2].

In the field of electrical power, due to the issues of cost, environment and right-of-way, the construction of new generation facilities and transmission lines were either put on hold or cancelled in many parts of the world in recent years. But the steep rise in demand for electrical energy simply cannot be ignored: the severe black outs in the Western Cape, South Africa, in early February 2006 served as the most recent reminder of this.

While scientists and engineers strive to find new ways to generate electricity, either from fossil fuels or renewable sources [2,3,4,5], it is equally if not more important to find methods to optimise the utilisation of existing generation plants and transmission systems, together with efforts to promote consumers’ awareness around issues of energy conservation. This research work focuses, in particular, on methods to improve the performance of the transmission part of the power system.

Power flow through an ac transmission line is a function of the line impedance, the magnitude of the sending- and receiving-end voltages, and the phase angle between these two end voltages. AC transmission systems are therefore typically fitted with mechanically switched series and shunt reactive compensators, together with voltage-regulating and phase-shifting transformer tap changers to control the above-mentioned four parameters that influence the transfer of power. In the past, these compensation devices were primarily intended for steady-state control and could

not be adjusted with sufficient speed to control the transient or dynamic behaviour of a transmission system. Therefore transmission systems have often been operated well below their theoretical maximum power transfer capabilities so that the power system is able to recover from the worst-case transient contingencies such as faults, line and generator outages and equipment failures. This implies that transmission resources are considerably under-utilized.

However, if the factors that influence power flow could be controlled under dynamic and transient conditions, then the stability of the power system could be much improved. That implies that the power systems can be operated closer to the theoretical stability limit in order to increase the system utility without jeopardizing the system security. The ideas to be able to use conventional compensation for dynamic and transient control can be dated back to the mid-1960s but could not be implemented in practice due to the absence of suitable power switches [6,7] (i.e. until relatively recently transmission line compensators have been mechanically switched so it was not practically possible to achieve fast control of the amount of compensation).

Semiconductors have been around for the past few decades, but it was the invention of transistors in the late 1940s that changed “semiconductors” from a science jargon to a whole new industry. During the last three decades, major advances have been made in high power semiconductor devices and sophisticated electronic control technologies. The idea of fast and efficient control over the four parameters that affect the power flow in a transmission system can now be implemented and realized by using these solid-state switching devices, which have become more reliable and cost effective.

In 1988, Hingorani [8] introduced the idea of high-speed control over the factors that influence power flow in an ac transmission system, in order to increase availability, operating flexibility and system stability. Hingorani proposed descriptions of two basic practical approaches to implement fast control over the parameters that directly affect ac power transmission (i.e. voltage magnitudes, phase angle and impedance). The first of these approaches was seen as the conventional method, which would integrate solid-state switching devices with existing devices (such as series and shunt capacitors) used for power system control. The second approach would be to implement the control using advanced power electronic circuits that would bear no physical resemblance to the traditional devices they were to replace.

Since Hingorani’s first proposal, the concept of Flexible AC Transmission Systems (FACTS) has been launched and a long-term research initiative has been driven by the Electric Power Research Institute. FACTS has been formally defined as “*alternating current transmission systems incorporating power electronics-based and other static controllers to enhance controllability and*

increase power transfer capability” [9]. Now, like transistors, FACTS is no longer merely a research idea, but an essential concept that is widely accepted in the power industry and utilities around the world [10]. In 1994, to show the importance of the concept, Ramey et al. [11] wrote:

“The recent development of fast... FACTS devices provides a new set of weapons in the arsenal of the transmission planning engineer, particularly for stability limits, where the speed of the electronic devices can be used to great advantage to provide damping and maximize synchronizing torque during transient incidents.”

The importance of FACTS is now being recognized on a worldwide scale and the technology is moving at an increasing pace. Along with advanced control centre technology and overall automation, FACTS represents a new era for transmission systems [9].

1.1.2 Inverter Based Compensators

Since the concept of FACTS was first introduced, various types of FACTS devices have been designed [12]. However this thesis focuses on the second class of FACTS devices envisaged by Hingorani, that is, all power-electronic type FACTS devices with little visual resemblance to conventional compensators. One of these devices is the inverter-based compensator which may be used to replace a conventional series compensator, shunt VAR compensator, phase shifter or all of these at once.

This particular category of FACTS device makes use of high-powered voltage source inverters to insert near-sinusoidal ac compensating voltages into the transmission system. These inverter-based FACTS devices include the Static Synchronous Series Compensator (SSSC), Static Synchronous Compensator (STATCOM) and Unified Power Flow Controller (UPFC), where the UPFC is essentially a combination of the SSSC and STATCOM modules. These devices are capable of controlling a number of different variables in the transmission system that influence power flow and they can do so via fast, continuous control. This thesis will deal with the modelling of all three devices; however, more attention will be paid to the analysis of the SSSC.

A. Static Synchronous Series Compensator (SSSC)

The inverter based series compensator, which is now often termed the SSSC, was first proposed in 1989 by Gyugyi [13]. Fig. 1.1 shows that the SSSC is used to insert, in series into the

transmission line, an ac voltage v_q at the synchronous frequency via a series injection transformer to influence the power flow on the line. The magnitude and angle of this injected voltage is controlled by the SSSC depending on its mode of operation. However, when operating as a stand alone SSSC, the device is restricted to the reactive power domain, where the injected voltage must be in quadrature to the line current.

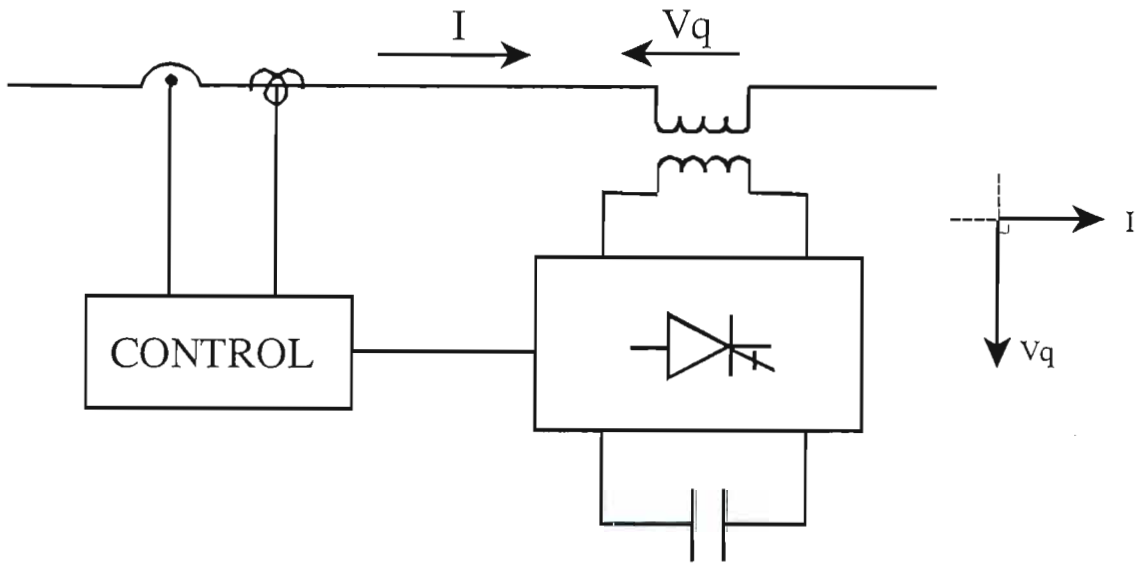


Fig.1.1: Schematic diagram of the SSSC.

Two possible modes of operation are described below [14,15]:

1. Line Impedance Emulation Mode

The SSSC injects an ac voltage that emulates capacitive reactance. The voltage injected into the line is in lagging quadrature with the line current i , thus emulating a *capacitive* reactive voltage drop in series with the transmission line. In practice, the voltage v_q inserted is not in exact quadrature with the transmission line current so that a small amount of real power is supplied by the line to replenish the losses in the inverter. The relationship between the line current phasor I and the injected voltage phasor V_q can be described mathematically by the phasor equation:

$$V_q = kIe^{-j\frac{\pi}{2}} \quad (1.1)$$

where the term k determines the degree of series compensation [16]. Hence, by controlling k , the degree of series compensation can be continuously varied within the rating of the inverter from zero compensation ($k=0$) to some maximum value ($k=k_{max}$). Also, by controlling the

term k , the reactive compensation is specified in a similar manner to a conventional series capacitive reactance [17], where

$$k = \frac{|V_q|}{|I|} = X_q \quad (1.2)$$

From Equation (1.2) the term k becomes analogous to the ohmic magnitude of a series capacitive reactance emulated by the inverter based series compensator [18]. In other words, the traditional capacitor banks are replaced by this inverter based series compensator with $X_q=k$ being, in effect, equivalent to the fundamental-frequency reactance X_c of the conventional series capacitor bank. However, in the case of the inverter-based compensator the magnitude of the compensating reactance is rapidly controllable because the amplitude $|V_q|$ of the inverter output voltage can be changed very rapidly. Note, although the SSSC is intended to emulate a conventional capacitive reactance at the fundamental frequency, throughout this thesis the notation V_q and X_q are used to describe the inserted voltage and emulated capacitive reactance of the SSSC, whereas the notation V_c and X_c are used to describe the voltage and reactance of a conventional series capacitor bank.

Various researchers have given this mode of SSSC operation different names. It is sometimes referred to as the “constant reactance mode” [19], or the “ X_q -controlled SSSC” [20].

This particular mode of operation of the SSSC is the one considered in this thesis.

2. Direct Voltage Injection Mode

This mode of operation [21] provides a controllable series compensating voltage *independent* of the magnitude of the line current, i.e. the injected voltage v_q is *typically* capacitive in nature, but has no direct enforced magnitude relationship with the line current i . For example, the magnitude of this compensating voltage can be used as part of a closed loop control scheme to force the active and reactive power in the transmission line to follow a desired reference value; however the inverter-based compensator does not emulate any specified value of capacitive reactance.

This mode of operation is also referred to as the “constant quadrature voltage mode” [19] or the “ V_q -controlled SSSC” [20].

B. Static Synchronous Compensator (STATCOM)

The second type of inverter-based compensator is the STATCOM, which also used to be referred to as the Advanced Static VAR Compensator (ASVC) [22,23,24] or Static Condenser (STATCON) [17,25]. A STATCOM has similar components to that of an SSSC but it is a shunt device that provides reactive compensation to the transmission system by injecting almost sinusoidal current of variable magnitude at the point of connection, shown in Fig. 1.2.

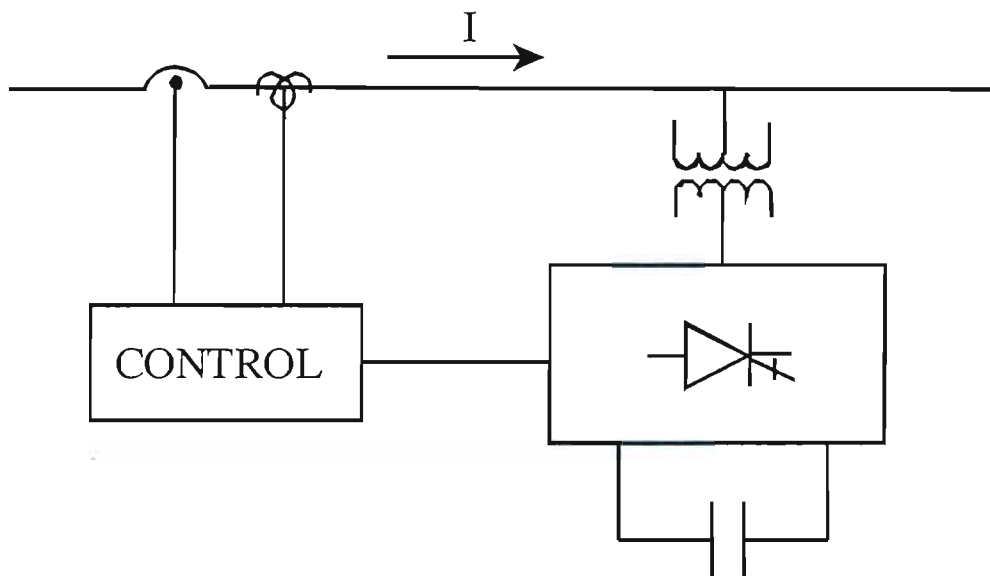


Fig.1.2: Schematic diagram of the STATCOM.

The reactive power exchange is determined by the amplitude difference between the inverter and system AC voltages. The inverter ac voltage is usually controlled by adjusting the magnitude of the dc capacitor voltage. Hence, if the dc capacitor voltage is increased from its nominal value, the STATCOM injects reactive power into the AC system in a similar manner to an over-excited synchronous condenser. On the other hand, if the dc voltage from the capacitor bank is reduced so that the inverter ac voltage is lower than the AC system voltage, then the STATCOM absorbs reactive power like an under-excited synchronous generator. The flow of real power between the AC line and the dc capacitor to replenish the losses in the STATCOM is governed by the phase angle between the inverter and the system AC voltages [11,17,22,26,27].

The reactive compensation control modes are described briefly as follows [14,15]:

1. VAR Control Mode

In this mode of operation, the shunt current injected by the STATCOM is controlled in order that that STATCOM provides a desired reference value of reactive power.

2. Automatic Voltage Control Mode

The transmission line voltage is maintained at a certain reference level by regulating the shunt reactive current injected by the STATCOM.

This thesis considers the detailed modeling of a STATCOM as a part of a larger UPFC model (to be described in the following section), but does not consider the performance of a stand alone STATCOM in ac transmission systems.

C. Unified Power Flow Controller (UPFC)

When either an SSSC or a STATCOM operates as a stand alone device, they are both limited to only work in the reactive power domain due to the fact that they cannot exchange active power with the ac system other than that required to replenish their own internal losses. However, when an SSSC and STATCOM are combined to form a larger device, the UPFC as shown in Fig. 1.3, the restriction is then removed, thus allowing operation within the real power domain [11].

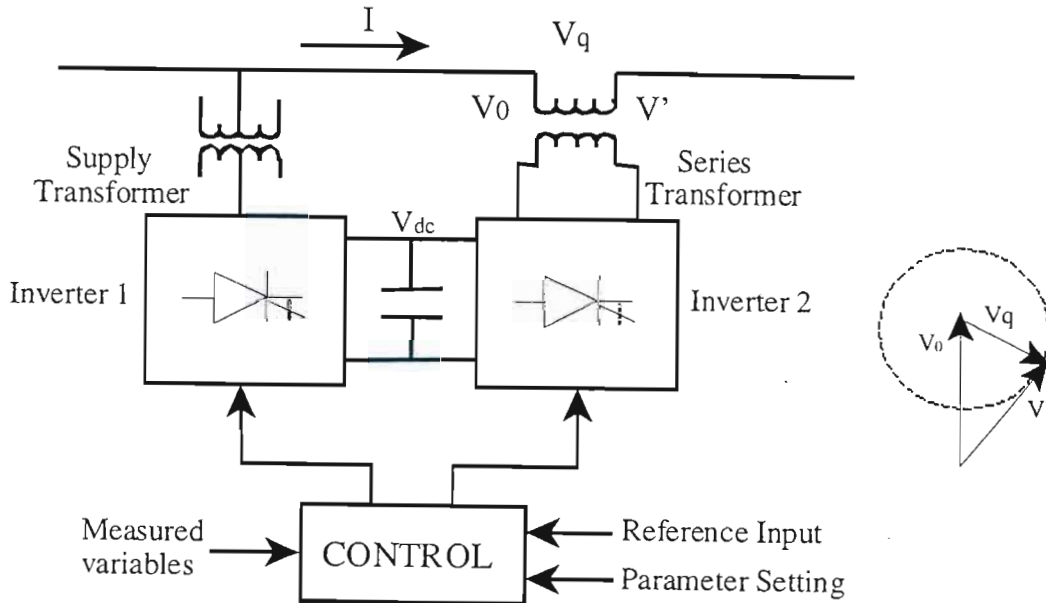


Fig.1.3: Schematic diagram of the UPFC.

The SSSC and STATCOM are connected in such a way that they share a common dc link capacitor – a concept that was first introduced in the Active Power Line Conditioner (APLC) [28,29]. The dc voltage, V_{dc} , of the link capacitor is regulated by the STATCOM which also provides the capability for exchanging shunt reactive current with the line [17]. The net real power absorbed from the line by the UPFC is equal to the losses of the series and shunt inverters and their coupling transformers [14]. The SSSC can now also exchange both real and reactive power with the transmission line. In this arrangement the UPFC can be viewed as an ac-to-ac converter in which the real power is able to pass bi-directionally through the UPFC in either direction via the dc link capacitor; the reactive power, however, is independently generated or absorbed by either the STATCOM or SSSC at its own point of connection to the transmission line [27,30,31].

Apart from being able to operate in the direct voltage injection mode and line impedance emulation mode, the SSSC can be applied to one further application when it is part of a full UPFC [14,15]:

Automatic Power Flow Control Mode

In this mode of operation, the series voltage injected by the SSSC is a two dimensional quantity with both quadrature and in phase components relative to the line current, and it is therefore able to independently control both the real and reactive power flow down the transmission line. Depending on the desired real and reactive power, these components of series injected voltage are automatically and continuously adjusted to respond to any system change. The UPFC is seen by the transmission line as a high impedance power source or sink [14]. It is in this mode that the UPFC yields best advantage over conventional compensating devices as it provides simultaneous, real-time control over all basic power system parameters [26].

Generally speaking, in a UPFC, the STATCOM will be operating in an automatic voltage control mode and the SSSC in the automatic power flow control mode [14]. Ultimately, the use of a UPFC is intended to enhance the power system by allowing maximum real power transmission with minimum reactive power flow [11]. The UPFC is, as reference [32] puts it, “*a unified device combining the advantages of all controllers.*”

1.1.3 Objective

With the advances in power semiconductor technology, the all solid-state implementation of

FACTS devices like inverter based compensators yields many advantages over conventional compensators, these include the reduction in manufacturing cost, equipment sizes and installation labour, also significant improvements in operating flexibility and performance [26]. Although such FACTS devices are intended to enhance the stability of the system and hold many advantages over the conventional power system control methods, due to their complexity, these devices have the potential to cause unfavourable interactions with network or other FACTS devices in the transmission system [33]. The research project described in this thesis has therefore focused on developing detailed simulation models of industry-standard, inverter-based FACTS devices in order to examine whether these devices can cause such unfavourable interactions. By using accurate simulation models at an early stage, it is hoped to be able to identify and overcome any potential hazards before the FACTS devices are introduced in the field.

1.2 Literature Review

1.2.1 General

The previous section gave a broad overview of FACTS and inverter-based compensators. This overview highlighted the issue that FACTS devices are themselves complex subsystems of the power system. The broad objective of the work presented in this thesis is to examine the possibility of adverse interactions between such FACTS devices and the rest of the system, and in particular the development of detailed simulation models of industry-standard FACTS devices so that such interactions can be predicted and avoided.

This section now presents a review of the technical literature in the subject area.

1.2.2 IEEE FACTS Working Group Definitions [9]

In 1997, an IEEE paper was submitted by the FACTS Terms & Definitions Task Force of the FACTS Working Group of the DC and FACTS Subcommittee, entitled "Proposed Terms and Definitions for Flexible AC Transmission System (FACTS)". The aim was to establish appropriate definitions of FACTS related terminology so as to avoid conflicting technical language and ambiguous jargon used worldwide by industries and academic researchers. The three inverter-based FACTS devices are defined as follows:

Static Synchronous Series Compensator (SSSC):

"A static, synchronous generator operated without an external electric energy source as a series compensator whose output voltage is in quadrature with, and controllable independently of, the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the transmitted electric power."

Static Synchronous Compensator (STATCOM):

"A static synchronous generator operated as a shunt-connected static var compensator whose capacitive or inductive output current can be controlled independent of the ac system voltage."

Unified Power Flow Controller (UPFC):

"A combination of static synchronous compensator (STATCOM) and a static synchronous series compensator (SSSC) which are coupled via a common dc link, to allow bi-directional flow of real power between the series output terminals of the SSSC and the shunt output terminals of the STATCOM, and are controlled to provide concurrent real and reactive series line compensation without an external electric energy source. The UPFC, by means of angularly unconstrained series voltage injection, is able to control, concurrently or selectively, the transmission line voltage, impedance, and angle or, alternatively, the real and reactive power flow in the line. The UPFC may also provide independently controllable shunt reactive compensation."

It should be noted that from the definition given to the SSSC, it is clear that the term applies only to the " V_q -controlled SSSC" described in section 1.1.2.A. However this strict definition is often not adhered to in the technical literature [19,20,27,34], and the name SSSC is often also used to describe the " X_q -controlled SSSC" described in section 1.1.2.A. In this thesis the more loose use of the term SSSC to mean "inverter based series compensator" is used. Where it is necessary to distinguish between the two categories of inverter-based compensator (or SSSC) the terms " V_q -controlled SSSC" and " X_q -controlled SSSC" (as defined in 1.1.2.A) are used.

1.2.3 Modeling of Inverter-Based FACTS Devices

The aforementioned objective of this thesis is aimed at developing detailed simulation models of an SSSC, STATCOM and UPFC that can then be used to predict any interactions with the rest of the power system. In order to model such a FACTS device accurately, the following issues need to be considered:

- (i.) inverter technology used in actual (high-power) FACTS devices;

- (ii.) inverter switching strategies typically used in actual FACTS devices;
- (iii.) type of control used in industry-standard applications; and
- (iv.) level of detail of the simulation model that is appropriate.

This section now presents a review of the technical literature and examines each of these issues.

Since the inverter-based FACTS devices can be implemented using various types of static switching power inverter, some important technical factors are considered when selecting the type of inverter to be used in high power FACTS applications: harmonics, switching and conduction losses, state of the art technology, cost, efficiency etc. Two main categories of static inverters are considered in the construction of high power compensators, namely voltage source inverters and current source inverters. Both inverter types may be operated to emulate series capacitance or inductance. However, as [35] points out, it is essential to have extra current snubbers in the current source topologies due to the lack of continuity of the current in the inverter inductors. Therefore, the voltage source inverters may be preferred over the current source inverters. Due to the fact that the mainstream use of inverters has been voltage-sourced since FACTS was introduced, this type will be adopted in this thesis.

Various types of inverter switching strategies that are commonly considered to ensure that the harmonic content of the ac output waveform is sufficiently low are two-level multi-pulse inverters, three-level multi-pulse inverters and pulse-width modulation (PWM) inverters [36]. When assessing the factors mentioned before, multi-pulse inverter configurations are usually considered to be the most practical for high-power utility applications [17,25]: PWM inverters have not been justifiable at high power levels due to higher equipment cost, and because the gate-turn-off thyristors' (GTO) switching losses are unacceptable at the higher switching frequency associated with these inverters [36,37]. However, such judgement may change with time as semiconductor technology improves and more sophisticated inverter topologies are being invented, allowing PWM-type inverter solutions at high power levels [38]. For example, a method has been proposed [39,40,41] which uses phase shifting of the triangular carriers in the sinusoidal pulse width modulation (SPWM) technique to reduce cost, total harmonic distortion (THD), the switching frequency and the switching losses. Reference [23] also employed a technique called the selective harmonic elimination modulation (SHEM) to minimize harmonics and, device stresses and losses. Nevertheless, PWM type of inverters is not considered in this thesis.

Within the multi-pulse inverter category, two types were mentioned, namely, the two-level and the three-level inverters. Two-level inverters have a fixed gain between the dc and ac voltages of the inverter, so that varying the amplitude of the ac output voltage can only be achieved by varying

the amplitude of the dc input voltage. The three-level inverter is more complex but it allows the ac output voltage of the inverter to be varied in two ways: one is the method described for the two-level inverters; the second is by varying the gain between dc and ac voltages without changing the dc voltage. Previously [22], three-level inverters were considered uneconomical for transmission type applications, but subsequently [23,24,27,34] studies have been reported where the three-level type of inverter has been considered. The three-level inverter is also preferred over the two-level due to its flexibility to rapidly vary the ac voltage or to provide a defined zero voltage “notch” to eliminate or reduce some specific harmonics [36]. In short, a three-level inverter may be operated as a two-level inverter, but not vice versa.

Various studies have proposed one typical topology of the single pole three-level inverter [25,23,24,36,42,43]. Reference [25] has actually proposed an n -level inverter topology; that, for $n=3$, reduces to the same topology as references [23,24,36,42,43]. Reference [44] has gone a step further, and proposed three types of transformerless multi-level voltage source inverters, namely, “diode-clamp”, “flying-capacitors” and “cascading-inverters with separate dc sources.” The absence of magnetic coupling transformers in these proposed topologies serves the purpose of overcoming problems of their bulkiness, weight and losses. The “diode-clamp” inverter described in [44] is a further development of those in [25,23,24,36,42,43]. However, the inverter topology described in [25,23,24,36,42,43] will be considered for detailed study in this thesis: this topology appears, based on current technology, to be the most suited to high-power transmission applications.

An SSSC can be operated in different modes, depending on whether or not the device is stand-alone or part of a UPFC. Sen [34] has developed an EMTP simulation model of a stand-alone SSSC based on a two-level, 24-pulse harmonic neutralized voltage source inverter and used this model to study the dynamic performance of the SSSC. Fig. 1.4 shows a diagrammatic representation of the SSSC in an ac transmission system as presented in [34]. This transmission system includes a sending-end voltage source V_s , a receiving-end voltage source V_r , and inductive reactances X_s and X_r . The SSSC consists of a voltage-sourced inverter $VSII$, a special transformer $MC2$ (magnetic adding circuit), a series voltage-injecting transformer $T2$, current and voltage sensors, and a compensation controller.

Soon after [34], Sen [27] developed an EMTP simulation model of a larger UPFC device based on two identical three-level, 24-pulse harmonic neutralized voltage-source inverters and used this model to study the dynamic performance of the UPFC, as shown in Fig. 1.5. The SSSC part of the UPFC is essentially identical to that in [34] but it is now connected to the STATCOM through a common dc link capacitor. The STATCOM consists of a voltage-sourced inverter $VSII$, a

special transformer *MC1* (magnetic adding circuit), a shunt voltage-injecting transformer *TI*, current and voltage sensors, and a compensation controller.

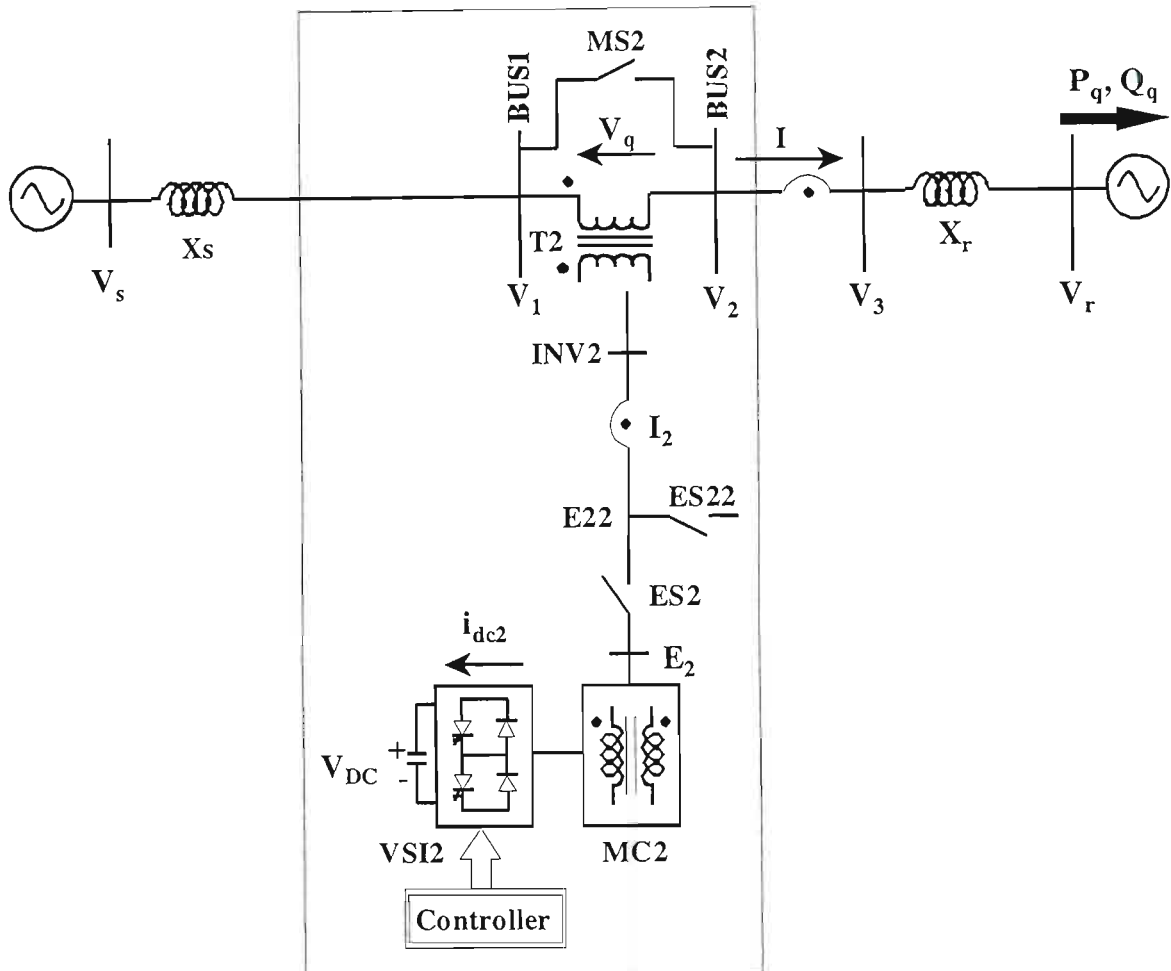


Fig.1.4: Diagram of a Static Synchronous Series Compensator [34].

Since the SSSC in [34] is based on a two-level inverter (fixed gain between inverter dc and ac voltages), the SSSC controls in [34] adjust the magnitude of the ac output voltage by regulating the inverter's dc voltage. Since the SSSC in [27] is based on a three-level inverter (adjustable dc to ac gain), the SSSC controls in [27] adjust the magnitude of the ac output voltage by adjusting the conduction intervals of the GTOs in the inverter; this mode of operation is specifically required in the UPFC, since the magnitude of the dc link voltage shared by the SSSC and STATCOM is set by the STATCOM's controller. In both the aforementioned SSSC and UPFC models originally developed by Sen [34,27] the discontinuous nature of the multi-pulse inverter's ac output waveforms and the SSSC controls are represented in detail, but the actual

power-electronic switching in the inverters is not represented in either case. In most studies on inverter-based FACTS modelling, the mathematical modelling approach taken is to not represent the actual power electronic switches within the inverters; examples of this approach include mathematic modelling of SSSC [20,30,45,46], STATCOM [22], and UPFC [14,31,32,47–54].

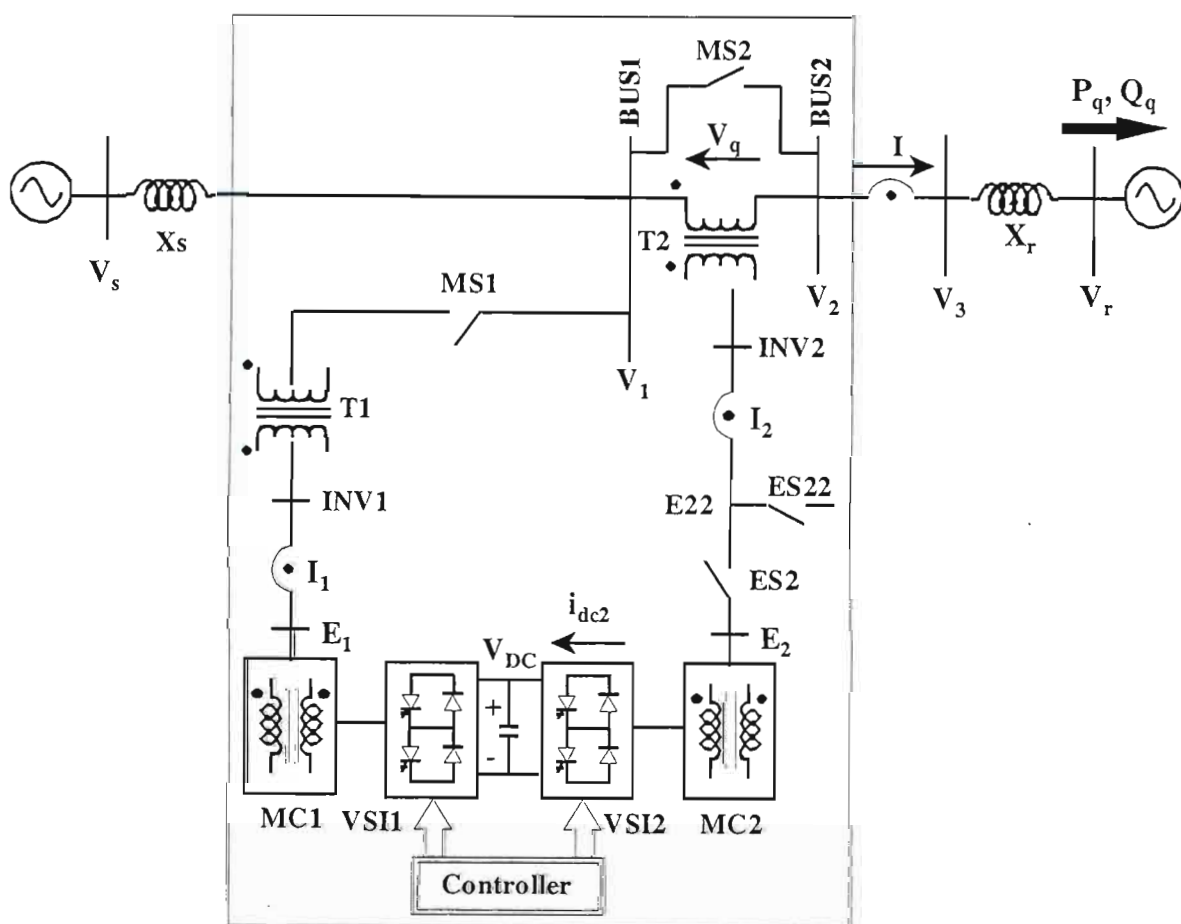


Fig.1.5: Diagram of a Unified Power Flow Controller [27].

Ghosh *et al.* [55] have developed an SSSC model for the power system simulation program PSCAD/EMTDC [56,57] based on a 48-pulse inverter; in this case the simulation model does include the detailed power electronic switching in the inverter, but the inverter considered is only a two-level device. This model is then used for their subsequent studies on the dynamics between SSSC and other compensating devices in the transmission line [58–61]. Reference [62] developed a detailed STATCOM simulation model including power electronics, but assumed a two-level inverter. A detailed UPFC model has been developed based on three-level, 12-pulse inverters which include the inverters' switching topologies [63].

Along the lines of developing detailed power electronic models of the inverter-based FACTS devices, Han *et al.* [42] described an SSSC based on a three-level multi-bridge inverter. Reference [42] proposed an inverter that consisted of six three-level half-bridge modules per phase for the SSSC. These half-bridge modules are the same as the single pole three-level inverter topology mentioned earlier. However, the switching strategy adopted here is pulse width modulation. Subsequently in [43], Han *et al.* considered the three-level switching strategy and also increased the complexity of the inverter developed in [42] to comprise twelve three-level, half-bridge modules per phase; this topology was referred to as a six H-bridge module, and ultimately generated a staircase output waveform of thirteen voltage levels. In regards to module structures, references [42,43] connected each half-bridge module in series with one another, with multiple dc sources, whereas reference [27] connected these modules in parallel with one common dc source. It was claimed by both [42,43] that the system flexibility and operating voltage could be increased by increasing the number of the half-bridge modules connected in series. However, the goal in both [42,43] by Han *et al.* was to propose an SSSC that could be inserted directly onto the transmission line without coupling transformers; since this particular innovation is not an objective in this thesis, only the more standard inverter topologies are considered for study here.

In regards to the type of control mode of the SSSC, references [27,31,42,43,46] have followed the strict definition of the SSSC given in [9], that is the V_q -controlled SSSC. On the other hand, the models described in [55,58,59,60,61] appear to be that of a X_q -controlled SSSC, as the authors specifically designed the SSSC to emulate the behaviour of a series capacitor or inductor. Likewise, [34,64,65] clearly deal with the X_q -controlled SSSC. References [19,20] actually developed both types of SSSC to investigate and compare their characteristics and performances.

In this thesis, detailed models of a stand alone X_q -controlled SSSC and a UPFC have been developed for the simulation package PSCAD/EMTDC. The SSSC model is based on the work of Sen in [34], but the SSSC model presented here is based on a three-level 24-pulse inverter [27,36] and not just a two-level device; hence it can be used in either of the inverter control modes (adjustable inverter dc voltage magnitude or adjustable dc to ac gain across the inverter). The UPFC model is entirely based on the work of Sen in [27]. Both the SSSC and UPFC simulation models developed extend Sen's work from mathematical models developed in EMTP to detailed simulation models that represent the switching actions of each power electronic device within the inverters, their low-level switching controls and coupling transformers. The model of the individual power electronic devices employed in these studies is of a non-ideal (finite resistance) switch, in the open or closed state according to the firing pulses received from the low-level switching controls. Benchmark tests are presented in the thesis to demonstrate that the steady

state and dynamic performances of the stand alone SSSC and UPFC predicted using these PSCAD/EMTDC simulation models agree closely with those described in [36] and [27] respectively.

1.2.4 Subsynchronous Resonance and Related Issues

One of the most inexpensive ways to increase the power flow down an ac transmission line is to insert series capacitors and therefore decrease the total line impedance. However, this seemingly effortless solution of relieving power congestion carried a weighty price tag. In the 1970s, two successive shaft failures occurred at the Mohave plant in South California Edison, U.S.A., after the series capacitor compensation was implemented. These events unveiled the danger of an instability called subsynchronous resonance (SSR) [66,67,68], and a worldwide research effort into the SSR phenomenon and its related topics was launched.

Subsynchronous resonance (SSR) is a form of dynamic instability that arises when electrical resonances in a transmission line compensated with series capacitors interact with the mechanical resonances of a turbine-generator shaft system [69]. This type of instability, as described earlier on, can severely damage the shafts of the turbine-generators and therefore special precautions are required when inserting conventional series capacitors onto transmission lines [66,69].

One of the methods that has been proposed to mitigate the SSR problems is to incorporate inverter-based series compensators onto the transmission line. Various papers [17,21,26] have stated that since inverter-based FACTS series compensators employ no series capacitor they are immune to classical network resonances. This claim is based on the reasoning that series compensation by a synchronous voltage source can be restricted to the fundamental frequency, and with proper implementation should therefore be unable to produce undesired electrical resonances with the transmission network, and therefore *cannot* cause subsynchronous resonance [17]. While Sen in his two papers [27,34] about the inverter-based series compensator did not mention any resonance related topic, Ghosh [55] has claimed that with these FACTS series compensators “*the system operates satisfactorily without any SSR for balanced and unbalanced faults.*”

However, Harley et al. pointed out that due to the fact that the transfer function of the SSSC is of fourth order at least, SSR instability cannot be ruled out [70]. Reference [14] stated that when SSSC is implemented, “*naturally care must be taken in this [line impedance emulation] mode to avoid values of negative resistance or capacitive reactance that would cause resonance or instability.*” References [20] and [33] then demonstrated that the inverter-based form of

compensation does cause a resonant impedance effect similar to that caused by conventional series compensating capacitors and therefore could potentially excite SSR. It was also shown that the subsynchronous frequency at which this resonant minimum occurs in the impedance of an SSSC-compensated line is distinct from that of a conventionally-compensated line; furthermore, the magnitude of the impedance at resonance in the SSSC-compensated line, and hence the extent of the SSR concern, was shown to depend on the tuning of the SSSC's internal controller.

References [58,59] have likewise confirmed that the torsional modes of a generator connected to an SSSC-compensated transmission system can be lightly, or even negatively damped. Indeed, reference [58] also concludes that the SSSC's internal controller design can have an influence on the stability of the torsional modes of neighbouring generators. In [59], this latter issue is considered further: the authors describe a successful study into the design of the SSSC's dc-side capacitor and internal controller to avoid causing negative damping in the torsional modes of a neighbouring generator. Reference [59] also concluded that the increase in conventional capacitor compensation increases the damping of small signal oscillations, whereas the use of an SSSC results in a decrease in small signal stability.

In order to provide positive damping to the SSSC-compensated system, reference [60] introduced a power system stabiliser (PSS) with a speed input signal to improve the system stability. However, it has been shown that, with proper design, the SSSC can nevertheless be used to damp out torsional oscillations caused either by itself [71], or by conventional series capacitors elsewhere in the transmission network [61,65]. These studies have presented the results of successful studies in which an SSSC, together with supplementary damping controls, is used in combination with conventional series capacitors without causing negatively-damped torsional oscillations.

So far in the review, the SSSC that has been used to provide damping in each case is the X_q -controlled form of SSSC; however, with appropriate damping controller, the V_q -controlled SSSC can also be employed to increase power system damping. Nevertheless, it has been shown [19,20] that the X_q -controlled SSSC results in a greater system transient stability limit and provides more natural damping than the V_q -controlled SSSC.

An important consideration when studying the SSR characteristics of new forms of compensation is the nature of the study system itself, particularly when it is desirable to compare the performance of one form of compensation (SSSC) against another (conventional series capacitors) or when it is desirable to compare strategies to investigate SSR using a device such as the SSSC. Also, when drawing conclusions regarding SSR, a range of system conditions needs to be

considered (e.g. different values of series compensation, operating point etc.) rather than drawing conditions based on one value of compensation and one operating point. For this reason, it is important to carry out thorough studies using benchmark study systems developed for such investigation. Much of the detailed research done on SSSCs and SSR has made use of non-benchmark type study systems [15,19,20,34,46,53,65]. While such studies are still of value and interest, it is also important to validate such studies on benchmark systems such as these conducted in [55,58,59,60,61,71]. Other studies have considered detailed resonance issues, but at a single value of series compensation [55,61,65]. In this thesis, the IEEE First Benchmark Model [72] is used as the basis of study and comparison for all detailed SSR investigations, and a range of operating conditions and system variables are considered for analysis, rather than relying on single-condition studies to draw conclusions.

Although a number of research studies have been done into the characteristics, effect and performance of the SSSC on the stability of the power system, little work has been done on the SSR characteristics when a UPFC is connected to a transmission line [52,63], nor has the damping function of the UPFC been fully explored [73]. However, it has been shown [63] that while the operation of STATCOM has no significant effect on the torsional modes of the generator, the SSSC is able to increase the damping of the critical torsional modes by operating in the resistance emulation mode, that is where positive series real voltage is injected onto the line, but that care must still be taken when the SSSC operates in the capacitive reactance emulation mode.

This thesis uses the detailed PSCAD/EMTDC model of the X_q -controlled SSSC to investigate the resonant characteristics of the transmission line impedance in which an SSSC is placed. This same SSSC model is then integrated into the IEEE First Benchmark Model for the study of SSR to investigate the resonant response of the turbo-generator shafts in the presence of a detailed SSSC model. Further studies are presented in this SSSC-compensated First Benchmark Model to investigate the implementation and design of a supplementary damping controller for the SSSC to damp out the electro-mechanical instabilities caused by itself, and those caused by a combination of conventional capacitors and the SSSC operating in the reactance emulation mode.

1.3 Thesis Outline

As described in section 1.1.2, the SSSC, STATCOM and UPFC are based on solid-state voltage-sourced inverters; therefore in Chapter Two, a detailed description of these inverters is presented. The basic 3-level inverter "pole" is first described, then a detailed 3-level, 24-pulse

inverter, including all the power electronics involved in the voltage-sourced inverters and their low-level switching control, is simulated. This chapter also takes a closer look at how the inverter's fundamental and harmonic frequencies behave under different GTO switching angles.

Any investigation based on simulation studies depends heavily on the accuracy of the simulation model. It is therefore essential that the validity of such models be well established before they are used for predictions. Chapter Three presents a detailed SSSC model, including the above described three-level, 24-pulse inverter, phase shifting and series injecting transformers and the associated FACTS device controls. In the studies of Chapter Three, the SSSC is first operated as a two-level (i.e. fixed dc to ac inverter gain) and then as a three-level device (i.e. variable dc to ac inverter gain). The difference between these two modes of control scheme in the SSSC is described in detail. Simulation results obtained from this detailed SSSC model are presented and benchmarked against the results in [34].

Chapter Four presents a detailed UPFC model that employs the three-level, 24-pulse inverter described in Chapter Two. The development of the STATCOM is first described along with its associated controls. After that, the STATCOM is combined with the three-level SSSC described in Chapter Three to form a larger UPFC model. For the purpose of assuring the accuracy of the model, the simulation results obtained from this detailed UPFC model are presented and benchmarked against the results in [27].

Although it is important to run simulations using these detailed models described above as it gives a better idea on how the entire system is performing, large simulation time is required and for some studies, this may not be necessary. Chapter Five, therefore, presents the SSSC, STATCOM and UPFC models that are based on a simplified, continuous-time model of a voltage-sourced inverter; and by doing so, allow the simulation studies to be carried out more rapidly. Once again, the simulation results obtained from these simplified FACTS models are presented and benchmarked against the results in [27, 34] to ensure the accuracy of the simulation models.

Chapter Six presents an investigation into the resonant characteristics of the transmission line impedance in which a two-level SSSC is included. This exercise confirms that an SSSC has the potential to cause subsynchronous resonance. A more detailed case study on SSR is then presented using a combination of the detailed SSSC model and the First Benchmark Model for the study of SSR [72].

Chapter Seven investigates a method of damping out resonant oscillations in a three-level SSSC compensated transmission line. The simulated results show that by providing a supplementary

damping controller designed to add damping at a single torsional mode frequency, SSR stability may be restored. Moreover, it was found that one carefully designed supplementary damping controller is able to stabilise the SSR caused in a transmission system compensated solely by an SSSC over a range of values of SSSC compensation.

In practice, it is likely to be more cost effective to use a combination of conventional series capacitor compensation and an SSSC, such that only part of the series compensation is variable. Chapter Eight, therefore, considers methods of providing damping to a dual-compensated system, that is, a system compensated by both conventional series capacitors and the SSSC. The analyses in the chapter demonstrate that the nature of the resonances in such dual-compensated systems is complex and multi-modal. The chapter therefore proposes an extended, multi-modal supplementary controller for the SSSC that is better suited to damping such resonances. The results presented in the chapter show that this form of supplementary control is able to damp SSR in dual-compensated systems, at least at the values of compensation for which it is designed.

Finally, Chapter Nine presents the conclusions of the thesis and author's suggestions for further work.

1.4 Main Findings and Achievements of the Thesis

The main findings and achievements of the thesis are summarized as follows:

1. Detailed simulation models of the SSSC, STATCOM and UPFC based on an industry-standard, three-level, 24-pulse harmonic neutralized voltage source inverter are designed and benchmarked (Chapter Two, Three and Four);
2. Two control schemes for operating the SSSC are investigated, namely, control over the inverter's dc voltage magnitude and the control of the dc-to-ac gain across the inverter (Chapter Three);
3. Simplified simulation models of the SSSC, STATCOM and UPFC based on continuous-time model of a voltage-sourced inverter are designed and benchmarked (Chapter Five);
4. Re-confirmation, using detailed simulation models in a benchmark study system, that an SSSC can cause SSR (Chapter Six);

5. A detailed study into the performance of a supplementary SSR damping controller in a benchmark study system compensated solely by an SSSC for a range of values of the SSSC compensation (Chapter Seven);
6. A detailed study into the performance of a multi-modal supplementary SSR damping controller, specifically proposed in the thesis to damp subsynchronous resonances in a system compensated by a combination of conventional series capacitors and an SSSC, once again using a benchmark study system for a range of values of compensation (Chapter Eight).

1.5 Research Publications

Some of the findings of this thesis have been presented at national conferences [74,75,76].

Some of the results have also been reported at international conferences [71,77].

Some of the studies conducted have been published in local journal [78] and will be published in an international journal [79].

CHAPTER TWO

THREE-LEVEL MULTI-PULSE INVERTER MODEL

2.1 Introduction

As Chapter One has described, the voltage-sourced inverter is the basic building block of various inverter-based FACTS devices, and it has been shown to have advantages over the current-sourced inverter in regards to cost and performance [36]. Typically, multi-level multi-pulse inverter configurations are preferred over PWM inverters for high-power applications [17,24]. In this thesis a three-level inverter is considered because of its ability to vary its output ac voltage by changing either the amplitude of the dc input voltage, or the dc-to-ac voltage gain across the inverter.

In order to develop a suitable model of the SSSC, STATCOM and UPFC, it is logical first to develop an accurate model of such a voltage-sourced inverter and to analyse its performance before it is used to build these devices. This chapter therefore considers the theory of operation, construction, performance and frequency-domain characteristics of a particular three-level, multi-pulse, voltage-sourced inverter topology. The chapter then describes the development of a detailed model of this inverter topology in the simulation package PSCAD/EMTDC.

Subsequent chapters of the thesis will then describe the development and performance of a stand alone SSSC model (Chapter Three) and a UPFC model (Chapter Four) where the 24-pulse, voltage-sourced inverter developed in this chapter is used as both a two-level inverter (for the stand alone SSSC) and a three-level inverter (for both the stand alone SSSC and the UPFC).

2.2 The Single Pole Three-Level Inverter

2.2.1 Background

As explained in Chapter One, the purpose of an SSSC is to inject an ac voltage of variable magnitude in series with a transmission line. In the case of a stand-alone SSSC, the variation of the ac output voltage can be achieved by varying the dc voltage of the SSSC; in this case the SSSC only requires a two-level inverter (fixed dc to ac gain), although the use of a three-level inverter (variable dc to ac gain) does allow more flexibility and improves performance (at the expense of a more complex and costly inverter topology). However, when an SSSC is combined with a STATCOM to form a UPFC [27], the common dc voltage is controlled by the STATCOM. In this case, there is no option but to use a three-level inverter for the SSSC in order for it to be able to inject a variable ac voltage into the transmission line. This thesis has therefore specifically considered three-level inverters in order that the models developed can be used for the study of SSSCs in either mode of operation, as well as for the study of the UPFC.

In basic terms, a voltage-sourced inverter generates ac voltage from dc voltage. The input dc voltage may be from the rectified output of an ac power supply, from a stiff dc source etc. The dc voltage in the voltage-sourced inverter always has one polarity, but the dc current may flow in either direction. Therefore, power flow can be reversed by the reversal of dc current polarity. Because of this, the inverter valves have to be bi-directional, and are made up of an asymmetric turn-off device (such as a GTO), and a parallel diode connected in reverse. When power flows from the dc side to the ac side, it is regarded as inverter action. On the other hand, when power flows from the ac side to the dc side, it is regarded as rectifier action. In the case of an inverter-based FACTS device, where the dc voltage is obtained from a charged capacitor and not a stiff source, rectifying action is used to charge the capacitor and inverter action to discharge the capacitor as needed to maintain the required dc voltage.

2.2.2 Single-Pole Three-Level Inverter Topology

In Fig. 2.1, one phase-leg or “pole” of a three-level inverter is shown. The topology is taken from [36] as is the nomenclature used in the following descriptions. Each half of the phase leg is split into two series connected valves (1-1' and 1A-1'A in the top half and 4-4' and 4A-4'A in the bottom half). The midpoints between the two valves in each half are connected by the clamping diodes D_1 and D_4 .

As mentioned earlier, the dc current in an inverter-based FACTS device may flow in either direction, so the phase-legs must be able to handle the bi-directional current flow. The turn-off devices handle the inverter action, while their anti-parallel diodes handle any instantaneous rectifier action. Clamping diodes D_1 and D_4 , and turn-off devices 1A and 4A carry the current

during clamping periods: D_1 -1A carries the negative current (current going out to the ac bus) and D_4 -4A carries the positive current (current going into the dc source).

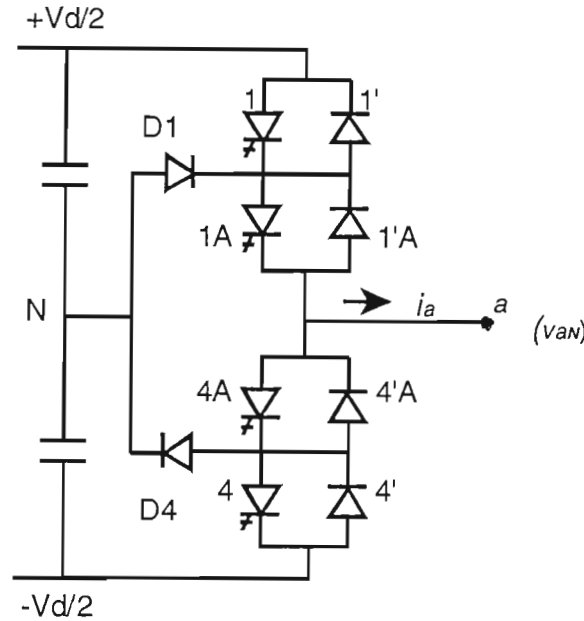


Fig.2.1: One phase-leg of a three-level inverter.

2.2.3 Switching Sequence Of The Single-Pole Three-Level Inverter

Fig. 2.2 shows the switching sequence of one phase-leg of this three-level inverter topology for one cycle of the ac output waveform; Fig. 2.3 shows the output ac voltage of the three-level phase-leg during the same period. The inverter is called three-level because the output has three possible voltage levels (with respect to point N) i.e. $-V_d/2$, 0 and $+V_d/2$. In order to achieve this three-level output the turn-off devices are switched on and off in the manner described as follows.

Step 1. ON: 1A and 4A

OFF: 1 and 4

Together with diodes D_1 and D_4 , 1A and 4A clamp the phase voltage v_a to zero volts with respect to the dc midpoint N regardless of which direction the current is flowing. This period will last for an angle of γ degrees before switching into the next state. Therefore the definition of γ is the “dead” period during which the turn-off devices operate in each quarter cycle and the pole output

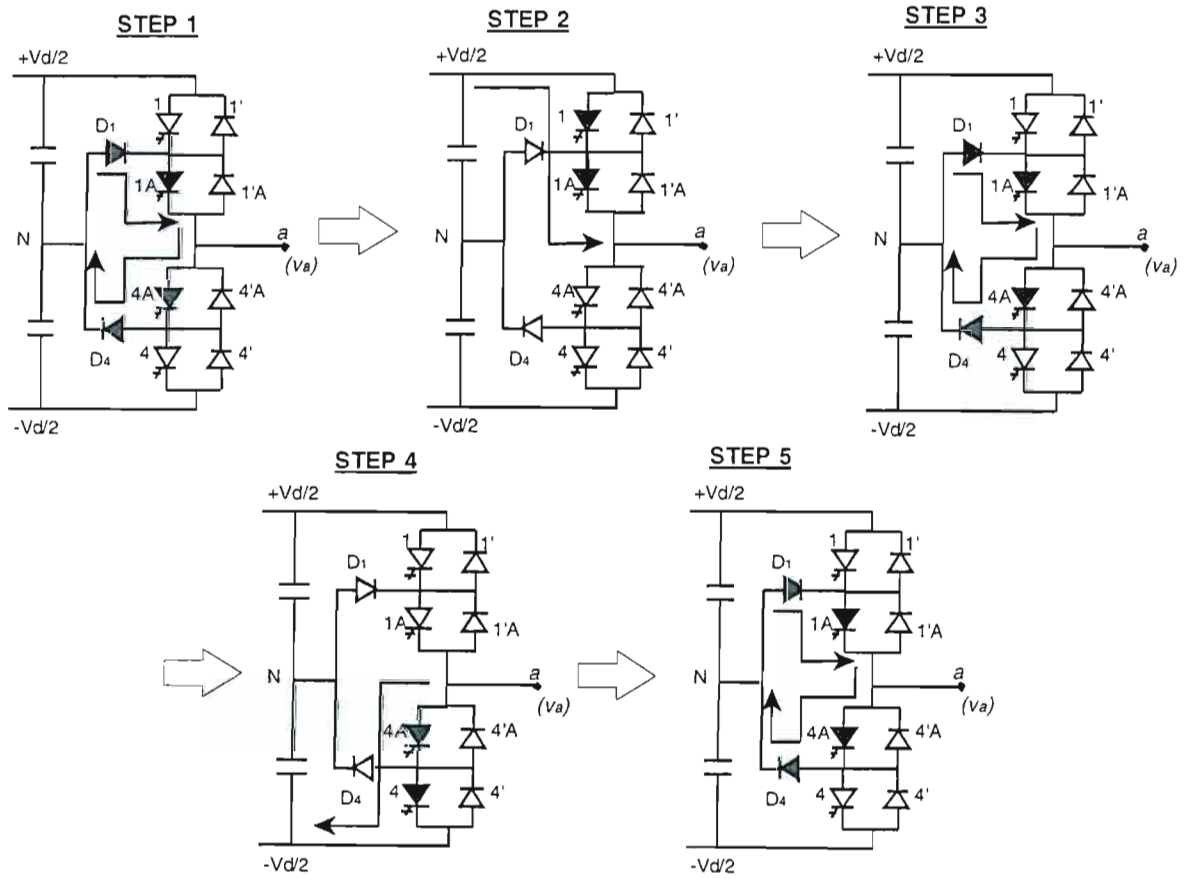


Fig.2.2: Illustration of the switching sequence of one three-level phase-leg for one cycle.

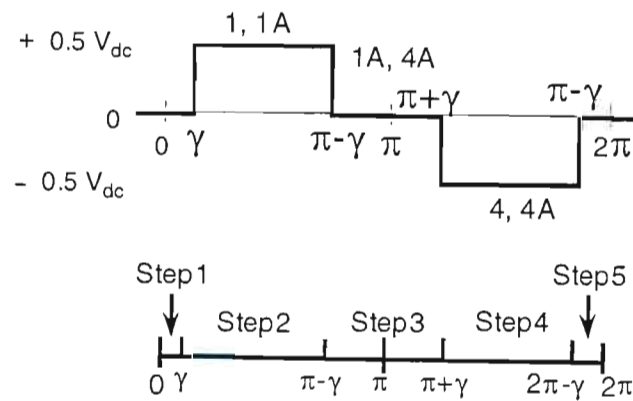


Fig.2.3: Output ac voltage of three-level phase-leg, v_{aN} .

voltage is zero (cf. Fig. 2.3). Note that although there are devices in both top and bottom halves of the leg (1A and 4A) being turned on simultaneously during the dead period of γ degrees, there is no “shoot through” (no short circuit of the dc voltage through the leg) since devices 1 and 4 remain off.

Step 2. ON: 1 and 1A

OFF: 4 and 4A

By turning on both the top half devices 1 and 1A, and turning off both the bottom half devices 4 and 4A, the output voltage v_a is held at $+V_d/2$. This state of the inverter leg is used to produce non-zero voltage during the positive-half cycle of the ac output voltage of duration σ degrees, where $\sigma = 180^\circ - 2\gamma$. (cf. Fig. 2.3.)

Step 3. ON: 1A and 4A

OFF: 1 and 4

The inverter leg is in the same state as described in Step 1. However this state now lasts for 2γ degrees (i.e. γ degrees at the end of the positive half-cycle followed by γ degrees at the beginning of the negative half cycle) (cf. Fig. 2.3).

Step 4. ON: 4 and 4A

OFF: 1 and 1A

By turning on both the bottom half devices 4 and 4A and turning off both the top half devices 1 and 1A the output voltage is held at $-V_d/2$. This state of the inverter is used to produce non-zero voltage during the negative half cycle of the ac output voltage of duration σ degrees. (cf. Fig. 2.3)

Step 5. ON: 1A and 4A

OFF: 1 and 4

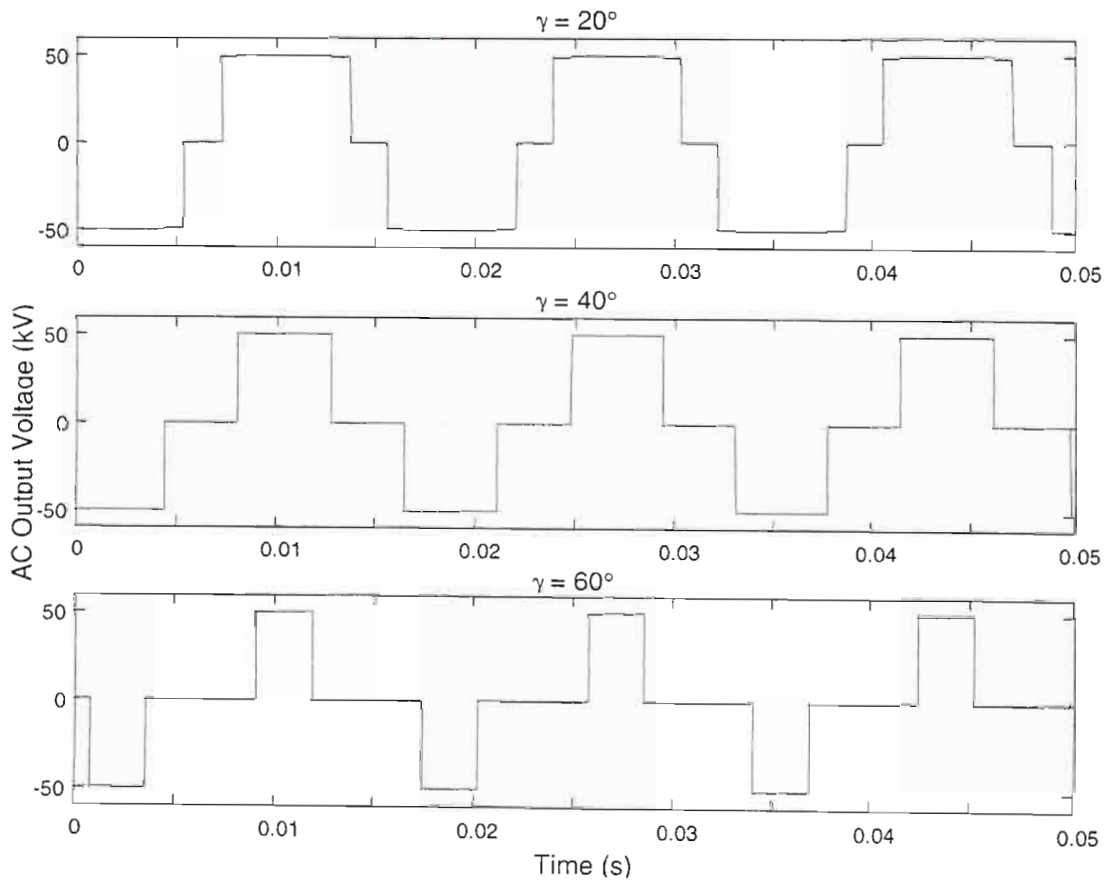
Same state as Step 1 and 3, but now the duration is γ degrees, following which the full cycle of the ac output voltage is complete.

From the above description, it can be seen that in the three-level inverter there is only one turn-on and one turn-off per device per cycle. The turn-off devices 1A and 4A are turned on for 180° during each cycle, devices 1 and 4 are turned on for σ degrees during each cycle, and diodes D_1 and D_4 conduct for 2γ degrees each cycle. The angle γ is a variable and therefore can be controlled to any desirable value in order to vary the effective amplitude of the ac output voltage. The output voltage v_a is made up of $\sigma = 180^\circ - 2\gamma$ square waves. At $\gamma = 0^\circ$, a three-level pole acts as a two-level pole which switches between the two dc levels i.e. $-V_d/2$ and $+V_d/2$.

2.2.4 Time-Domain Simulation Results From PSCAD/EMTDC

A simulation model of the basic three-level inverter leg in Fig. 2.1 has been developed in PSCAD/EMTDC. The two capacitors shown in Fig. 2.1 as dc inputs have been replaced by two identical constant dc voltage sources with amplitudes of +50kV and -50kV in the top and bottom halves of the leg respectively. In later chapters, when the full FACTS device controls around the inverter are considered, the inverter voltage is provided by dc capacitors as shown in Fig. 2.1.

In practical high-power high-voltage inverters a single so-called “valve” as referred to in the previous discussions would not comprise of a single GTO or diode, since a single such device does not have the voltage blocking or current carrying capacity required for such installations. Rather, each valve is in practice made up of several devices in a series string (to obtain the necessary voltage rating) and a number of such strings in parallel (to obtain the necessary current rating).



*Fig.2.4: Simulated output ac voltage waveform v_a from a three-level phase-leg with:
(a) $\gamma = 20^\circ$; (b) $\gamma = 40^\circ$, (c) $\gamma = 60^\circ$*

A firing control scheme for the individual turn-off devices in the inverter leg has been developed as part of the simulation model. This firing control scheme has, as its inputs, the desired value of dead angle γ and the instantaneous phase angle of the fundamental ac sinusoidal voltage that is required at the output of the inverter. In a full FACTS device implementation, the instantaneous angle of the desired ac output voltage is determined by the high-level controls of the FACTS device. However, in the early work of the thesis, before implementing the FACTS device controls, the various inverter models have been tested by generating a desired instantaneous phase angle from a phase locked loop connected to a dummy ac voltage source in the simulation model. This arrangement, together with a description of the inverter firing controls, is shown in more detail in Appendix A.2. Throughout the work of this thesis, the frequency of the ac system is set at 60Hz; this frequency is used for consistency because the SSSC and UPFC models developed in subsequent chapters are compared to published results from the literature [27,34] for a 60Hz ac system.

A number of simulations have been carried out using this model of the inverter leg in Fig. 2.1 in order to test the correctness of the model in PSCAD/EMTDC and to illustrate the effect of the dead angle γ on the ac output voltage. Fig. 2.4 shows a time-domain simulation of the output voltage waveform from the three-level phase-leg with dead-angles $\gamma = 20^\circ, 40^\circ$ and 60° . The results show that as the angle γ is varied, the duration of angle σ changes accordingly. The larger the dead angle γ , the smaller the conduction angle σ , and hence the smaller the average value of the ac output voltage on each half cycle. Ultimately, the ac output voltage will be zero if the dead-angle γ is increased to 90° , since there will then be no conduction pulse at all.

2.2.5 Frequency-Domain Characteristics Of The Single-Pole Three-Level Inverter

The output ac voltage v_a of the three-level inverter leg shown in Fig. 2.3 is a quasi-square wave which contains a positive sequence fundamental component and all the odd harmonic components including the zero sequence third, negative sequence fifth, positive sequence seventh etc. [27]. The amplitude of any odd multiple of the fundamental is defined by

$$V_n = \frac{2}{n\pi} v_d \cos n\gamma \quad (2.1)$$

where γ is the “dead” period during which the turn-off devices operate in each quarter cycle and the pole output voltage is zero, and $n = 2k+1$ for $k = 0,1,2,3$ etc. [27]. Hence the amplitude of the fundamental voltage is given by

$$V_1 = \frac{2}{\pi} v_d \cos \gamma \quad (2.2)$$

Equation (2.2) shows that the ac output voltage of the inverter varies with dead angle γ , i.e. at $\gamma = 0^\circ$ its maximum value is given by

$$V_{1\max} = \frac{2}{\pi} v_d \quad (2.3)$$

while the minimum value of zero occurs at $\gamma = 90^\circ$.

A plot showing the normalized amplitudes of the fundamental and individual harmonic components as a function of γ (calculated using Equation (2.1)) is shown in Fig. 2.5. The fundamental voltage V_1 is shown in per unit of $V_{1\max}$, while the harmonic amplitudes are shown in per unit of the actual fundamental voltage V_1 , as the dead period γ is varied from 0° to 90° . This normalization approach is taken from [36]. From Fig. 2.5, it is clear that the fundamental output

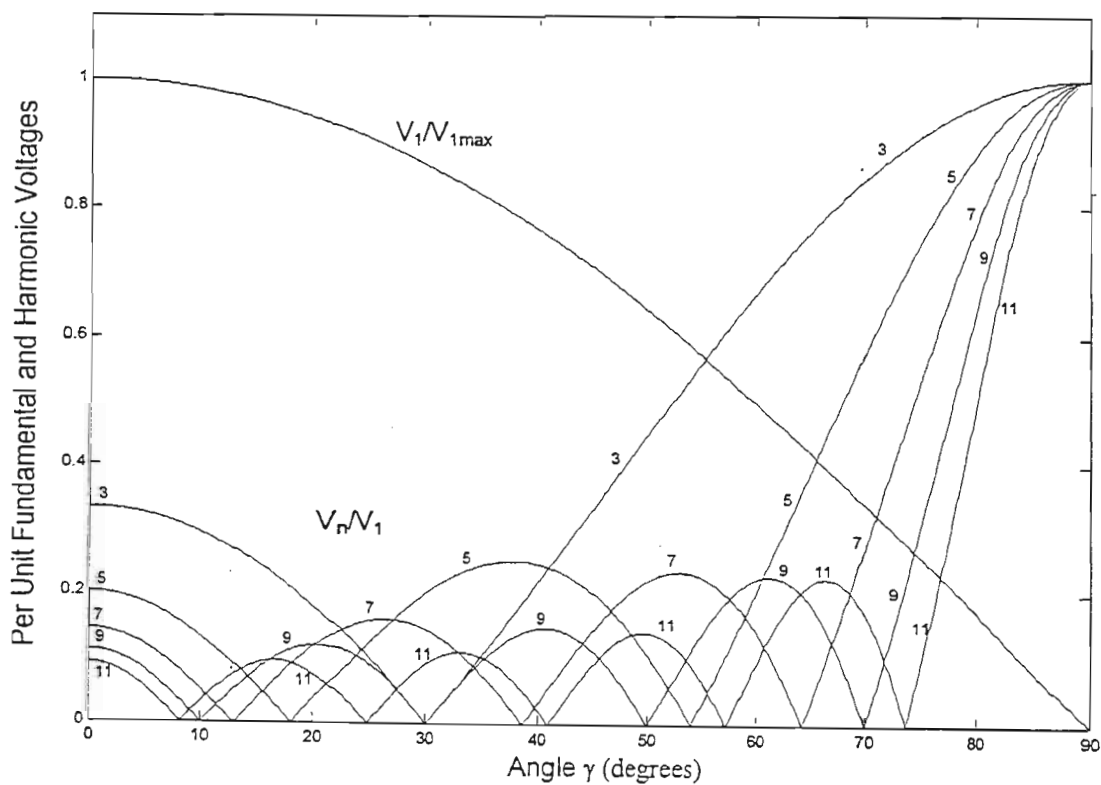


Fig.2.5: Fundamental and harmonic voltages for a three-level inverter pole based on theory [27].

voltage amplitude is 1.0 pu at $\gamma = 0^\circ$, and decreases with increasing dead angle, decreasing to zero at $\gamma = 90^\circ$. However the amplitudes of the harmonics increase and decrease according to Equation (2.1) within the same γ range. In summary, γ can be used to vary the amplitude of the fundamental output voltage but the associated harmonic voltages also change with γ .

2.3 The 6-Pulse Three-Level Inverter

2.3.1 The Topology And Operation Of The 6-Pulse Three-Level Inverter

High-power multi-pulse inverters are made up of a number of square wave inverters of smaller rating, each switched at low frequency (usually the line frequency of 50/60 Hz); a high quality of output ac voltage is then obtained by phase shifting and adding the square wave outputs of each of the smaller inverters to eliminate or reduce some specific, if not all, harmonics produced, in a

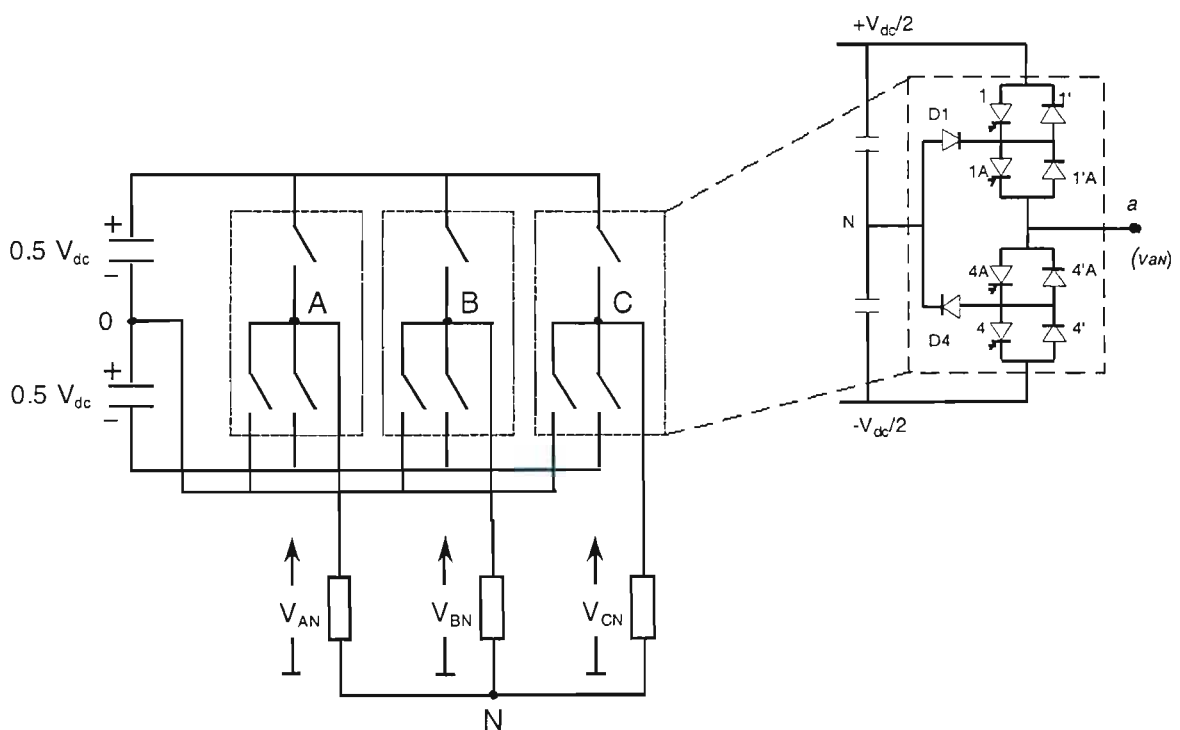


Fig.2.6: A 6-pulse inverter with three-level poles.

process known as harmonic cancellation. This enables a high quality sinusoidal output voltage to be obtained from the multi-pulse inverter as a whole, without the need for high switching frequencies of the individual power electronic devices.

The following sections within this chapter will look at the harmonic content of three different multi-pulse inverters, namely 6-pulse, 12-pulse and 24-pulse inverters. One shall see that the total harmonic distortion (THD) is very much reduced as the pulse number of the inverter increases from six to twelve, and then to twenty-four.

Fig. 2.6 shows three poles A, B and C, which are connected across the same DC capacitor, and the pole outputs are connected to a three-phase load with a neutral point N. The poles A, B and C form a 6-pulse three-level inverter, and are operated so that the pole voltages, v_{AN} , v_{BN} and v_{CN} , are time shifted from one another by one third of the time period of the pole voltage, i.e. the fundamental voltage phasors of each pole are 120° apart. Each pole of the inverter has the same topology as the phase leg described in the previous section. However, the neutral point N of the three-phase load is not connected to the mid-point of the inverter dc capacitor.

2.3.2 Time-Domain Simulation Results From PSCAD/EMTDC

A simulation model of the 6-pulse three-level inverter in Fig. 2.6 has been developed by the author in PSCAD/EMTDC by connecting, in parallel, three of the inverter pole models described in the previous section. These three single-pole, three-level phase legs are connected in parallel to the same dc voltage sources described in section 2.2.4. In addition, a low-level firing control scheme for the individual devices in a three-level 6-pulse inverter has been developed by the author in PSCAD/EMTDC as part of this simulation model. This firing control scheme has as its input the desired value of dead angle γ and the instantaneous phase angle of the fundamental three-phase voltage set required at the output of the 6-pulse inverter. Based on these inputs, the 6-pulse firing controls calculate the instantaneous phase angles required for each pole voltage and hence the firing signals for the individual turn-off devices in the 6-pulse inverter. The full details of the 6-pulse inverter model and its firing controls are shown in Appendix A.3. The inverter ac outputs are connected to a three-phase pure resistive load with a floating neutral. This simulation model was used to generate ac output waveforms of the 6-pulse inverter for a range of values of γ .

Fig. 2.7 shows a time-domain simulation of the phase to neutral voltage waveforms obtained from the 6-pulse inverter model in EMTDC for a dead period of $\gamma = 3.75^\circ$ with a dc capacitor voltage of

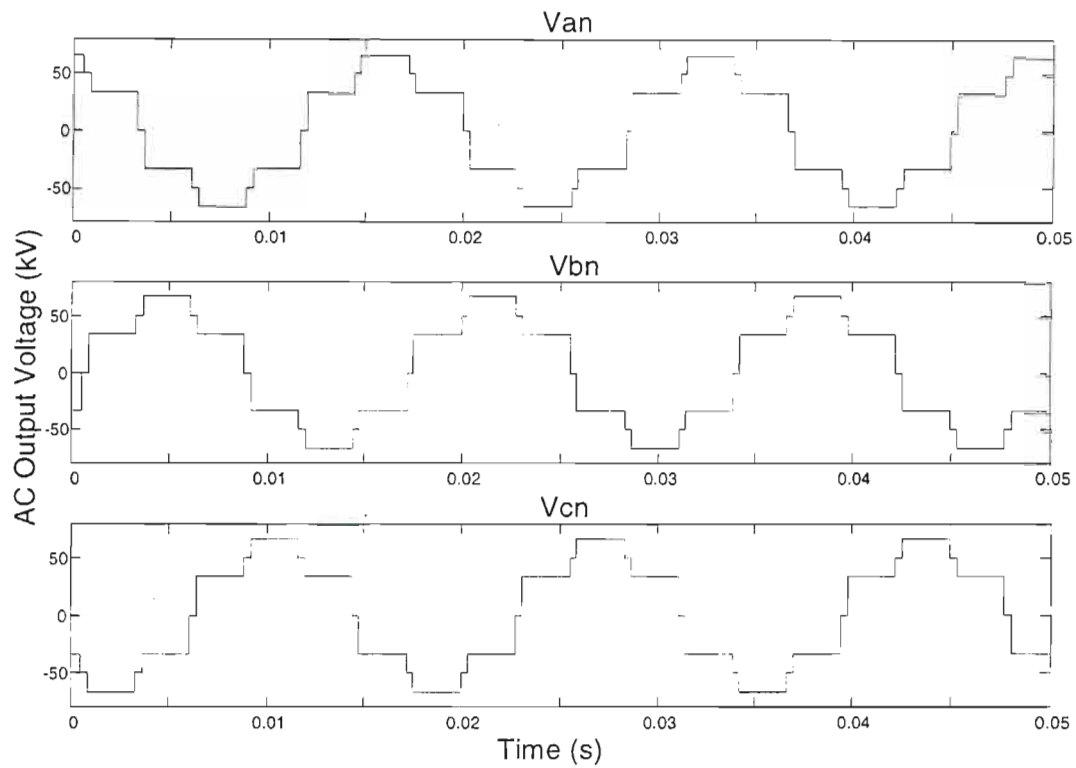


Fig.2.7: Simulated output voltage waveforms from a three-phase, three-level, 6-pulse inverter for $\gamma = 3.75^\circ$.

100 kV. The simulation result shows that the 6-pulse phase to neutral voltages are separated by 120° as expected. Furthermore, the simulation result illustrates that, because the neutral on the ac side of the inverter is not connected to the mid-point (zero volts) of the dc capacitor, the phase to neutral voltages in each pole exhibit seven distinct voltage levels as opposed to the three levels present in the phase to zero voltages shown earlier in Fig. 2.3.

Fig. 2.8 shows a time-domain simulation of the instantaneous and RMS voltages of phase *a* of the 6-pulse inverter in the EMTDC model for three different values of the dead period $\gamma = 20^\circ$, 40° and 60° . The RMS value of the inverter output voltage was determined by passing the instantaneous voltage outputs through an RMS calculation block in the EMTDC program. Earlier, Fig. 2.4 showed that the effect of changing the dead period γ in a single-phase inverter is to change the amount of time that the phase to zero voltage spends at each of the three voltage levels. Fig. 2.8 now shows that, in the three-phase inverter, the effect of changing γ is to change the amount of time that the phase to neutral voltage of each phase spends at each of the seven possible voltage levels. The reason for the presence of seven voltage levels in the three-phase inverter phase voltages can be explained as follows.

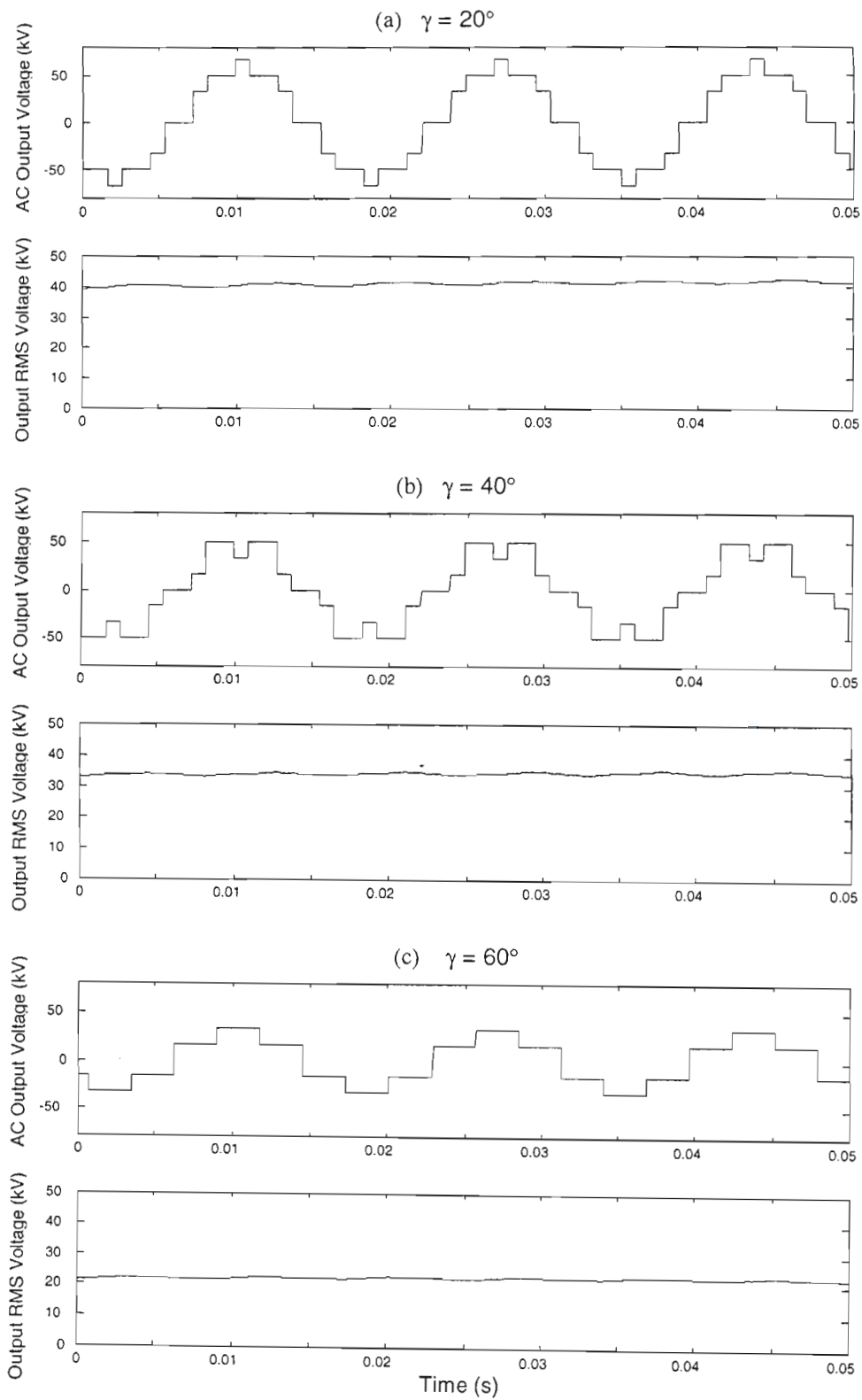


Fig.2.8: Simulated instantaneous and RMS output voltages from a three-phase, three-level, 6-pulse inverter with: (a) $\gamma = 20^\circ$; (b) $\gamma = 40^\circ$; (c) $\gamma = 60^\circ$.

The three-phase load is connected to a neutral that is not connected to the midpoint of the inverter dc voltages i.e. the neutral is not connected to ground. If the neutral were grounded, each inverter output phase voltage (v_{AO} , v_{BO} and v_{CO}) would have three voltage levels and would be similar in appearance to the voltages shown in Fig. 2.4. Since the neutral is left floating, the zero sequence components of each pole current have no return paths to the midpoint of the dc sources, so they are zero. The zero sequence components of each pole voltage, $v_{NO} = (v_{AO} + v_{BO} + v_{CO}) / 3$, appear between the neutral point and the midpoint of the inverter's dc sources. Therefore the load voltage per phase is in effect the *difference* between the phase to ground voltage and the zero sequence voltage component, i.e. $v_{AN} = v_{AO} - v_{NO}$, $v_{BN} = v_{BO} - v_{NO}$, and $v_{CN} = v_{CO} - v_{NO}$ [27], giving rise to the seven voltage levels that appear in the phase to neutral voltages in Fig. 2.8.

By comparing Fig. 2.7 ($\gamma = 3.75^\circ$) and Fig. 2.8(a) ($\gamma = 20^\circ$), it can be seen that at the higher γ value, the “on” time spent in both the maximum and minimum of the seven voltage levels has decreased. When γ is increased further to 40° , as shown in Fig. 2.8(b), the number of voltage levels is still seven but instead of the waveform looking “convex”, as it peaks, it is now “concave”. When γ is further increased to 60° the output voltage spends time in only four of the available seven voltage levels and the maximum and minimum values of the output voltage have also decreased in magnitude when compared to $\gamma = 20^\circ$. Therefore, the RMS value of the output voltage decreases from 39.3kV to 32.8kV to 21.6kV, as γ increases from 20° to 40° to 60° respectively.

2.3.3 The Frequency-Domain Characteristics Of The 6-Pulse Three-Level Inverter

As described in the previous section, because the zero sequence components of each pole current in Fig. 2.6 have no return path to the midpoint of the inverter's dc sources, the zero sequence components of each pole voltage appear between the neutral point and the midpoint of the dc capacitor. Therefore, each phase of the load voltage consists of only a fundamental component and odd harmonic components (n) given by Equations (2.1) and (2.2) where $n = 6k+1$ for $k = 1, 2, 3$ etc. [27].

At $\gamma = 0^\circ$, a three-level pole acts as a two-level pole which switches between positive and negative $v_{DC}/2$; under these conditions the fundamental as well as all the harmonic components have their highest amplitudes and the inverter therefore offers the maximum possible dc to ac utilization. At $\gamma > 0^\circ$, a three-level pole switches from $+v_{DC}/2$ to 0 to $-v_{DC}/2$, which produces improved output waveform quality at the expense of fundamental voltage reduction. For $\gamma > 0^\circ$, the fundamental amplitude decreases monotonically with increasing angle γ , such that the dc to ac gain across the

voltage can be varied by changing the input dc voltage or the angle γ , whereas the ac output voltage of a two-level inverter is strictly a function of the input dc voltage.

A plot showing the normalized amplitudes of the fundamental and individual harmonic components as a function of γ for a 6-pulse inverter (calculated using Equation (2.1)) is shown in Fig. 2.9. The same normalization method described in section 2.2.5 is applied here. The fundamental output voltage amplitude is 1.0 pu at $\gamma = 0^\circ$, and decreases with increasing dead angle, decreasing to zero at $\gamma = 90^\circ$; whereas the normalized harmonic voltages rise and fall throughout the same range of γ .

Fig 2.9 shows that at $\gamma = 0^\circ$, the fundamental as well as all the harmonic components have the highest possible amplitudes¹. At this angle, a three-level pole acts as a two-level pole that switches from $+v_{dc}/2$ to $-v_{dc}/2$ and offers the maximum possible DC to AC utilization. For angles $\gamma > 0^\circ$, the three-level pole is switched between the above-mentioned two states and zero, and thus produces improved output waveform quality but at the expense of reduction in the fundamental voltage.

Fig. 2.9 illustrates that the per unit amplitude of each of the harmonic components initially decreases as γ is increased from zero. Each harmonic component's per unit amplitude decreases to zero at a particular value of γ then successively increases from zero and decreases back to zero as γ is increased towards 90° . Thus, each particular harmonic component has zero amplitude at a few specific values of dead angle, as given by the equation

$$2\gamma = (180^\circ / n) \quad (2.4)$$

where n is the harmonic number [36].

For example, the seventh harmonic is zero when $\gamma = 12.85^\circ$, 38.55° , and again at 51.5° . After its first zero, the n th harmonic amplitude rises again, reaching a peak amplitude at a value of γ given by

$$2\gamma = 2 \times (180^\circ / n) \quad (2.5)$$

1: Note on normalization method – at first glance the amplitudes of the harmonics might appear to be highest at $\gamma = 90^\circ$ in Fig. 2.9. However the harmonic amplitudes are expressed here as per unit of the fundamental magnitude, and the fundamental magnitude decreases with increasing γ . Thus as γ increases the absolute amplitude of the harmonics decreases but their amplitude relative to that of the fundamental alternately increases and decreases.

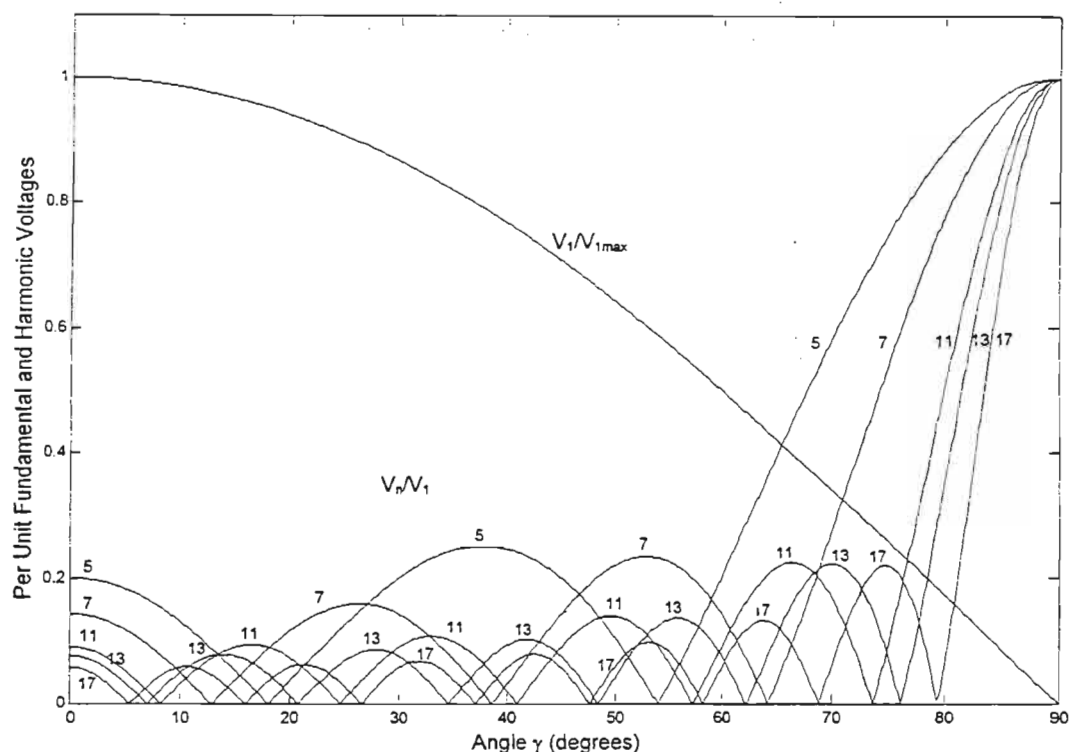


Fig 2.9: Fundamental and harmonic voltages for a 6-pulse three-level inverter based on theory [27].

Because of the zero amplitude of all harmonic voltages at different specific dead angles, there are certain angles where the inverter may be operated to have the same response as a higher pulse-number inverter. For example, in Fig. 2.9, for γ between 13° and 18° , both 5th and 7th harmonics have very small amplitudes, and the inverter almost behaves like a 12-pulse inverter [36]. However, for operation at 18° , the fundamental voltage drops to 0.95 pu which means 5% loss of capacity. Hence there is effectively a compromise between a desired reduction in some specific harmonics and an associated loss in useable output voltage capacity. In many applications, if allowed, a combination of higher pulse inverter, dc voltage control and use of three-level phase-legs are considered [36]. It is important to note that with the split dc capacitor topology of Fig. 2.6, it is essential to ensure that the two capacitors are charged to equal voltages: unequal voltages would result in a generation of even harmonics [36].

The final aspect to consider is the total harmonic distortion (THD) of the 6-pulse three-level inverter. A measure of the harmonic content can be defined [27] as

$$V_{Nh} = \sqrt{\sum V_n^2} \quad (2.6)$$

where V_n is the amplitude of the n th harmonic voltage given by Equation (2.1), and
 $n = 6k \pm 1$ for $k = 1, 2, 3$, etc.

A measure of the total harmonic distortion of the inverter ac voltage is then defined as

$$THD_V = V_{Nh} / V_1 \quad (2.7)$$

where V_1 is the amplitude of the fundamental voltage given by Equation (2.2).

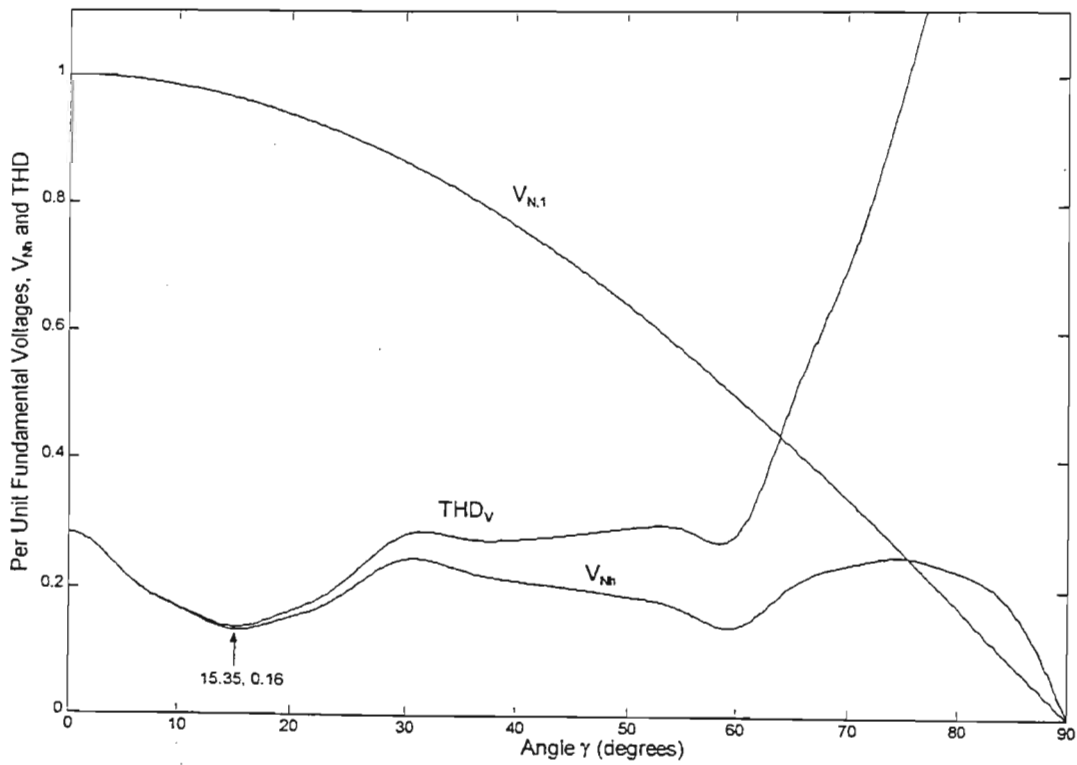


Fig 2.10: Amplitude of fundamental voltage, harmonic content and total harmonic distortion (THD_V) as a function of γ for the 6-pulse inverter, based on theory [27].

Based on the theoretical Equations (2.1), (2.2), (2.6) and (2.7), the amplitude of the fundamental voltage, harmonic content and total harmonic distortion factor of the 6-pulse three-level inverter

as a function of γ are shown in Fig. 2.10. The curves show that at $\gamma = 15.35^\circ$, the fundamental amplitude decreases by 3.57% compared to that obtained from a two-level operation of the poles, i.e. when $\gamma = 0^\circ$. However, at $\gamma = 15.35^\circ$ the harmonic content is reduced to 16% from the value of 31%, obtained from a two-level operation of the inverter, resulting in the smallest THDv. Therefore, angle 15.35° is described as the optimum value of dead angle in the case of the 6-pulse three-level inverter [27].

2.3.4 Frequency-Domain Characteristics From PSCAD/EMTDC Simulation Model

The time domain simulations using the six-pulse inverter model developed for EMTDC were repeated for a range of values of γ from 0° to 90° and Fast Fourier Transform (FFT) analysis used

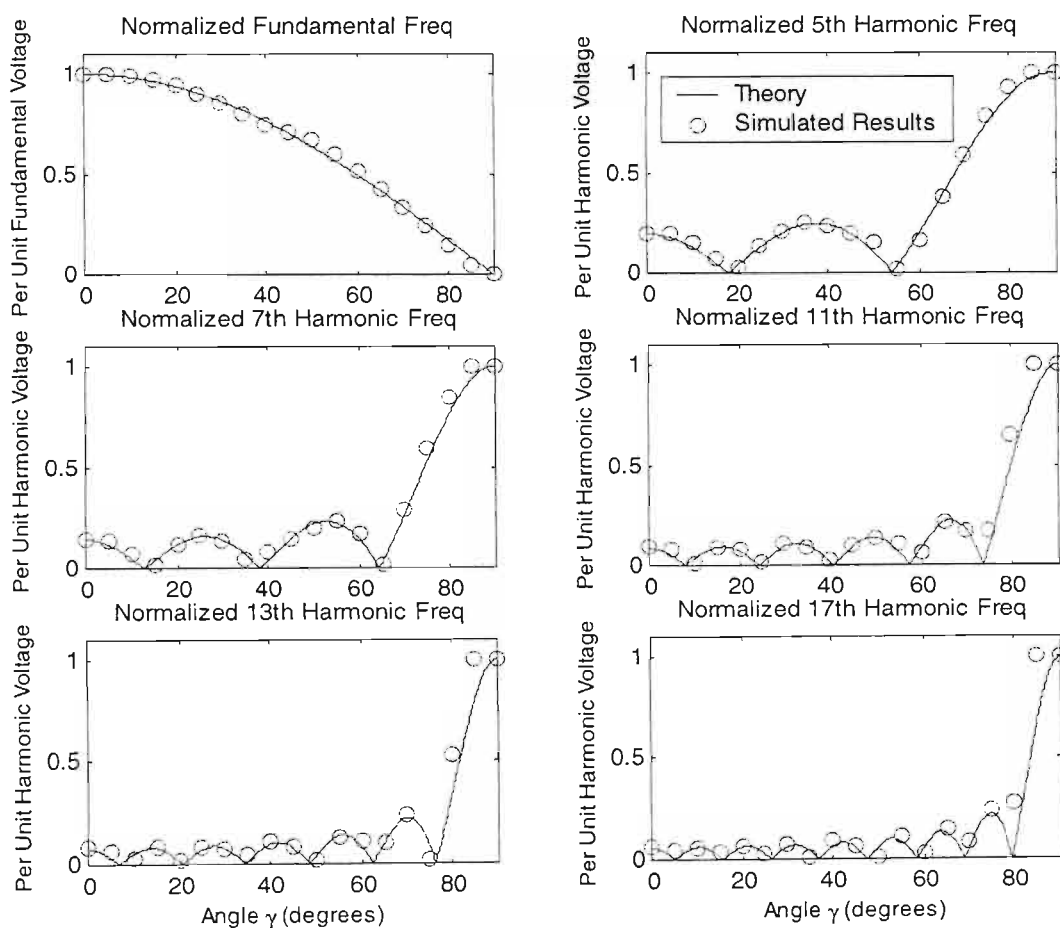


Fig 2.11: Fundamental and harmonic voltages for a 6-pulse inverter: theory vs. EMTDC simulation results.

to determine the amplitude of the ac output voltages (fundamental and harmonics) as functions of γ . The results of these analyses on the outputs of the simulation model are compared with the theoretical behaviour predicted by Equations (2.1), (2.2), (2.6) and (2.7) in Fig. 2.11. Fig. 2.11 shows that the harmonic spectrum of the ac output voltages in the 6-pulse EMTDC inverter model agrees closely with the theory. Fig. 2.11 also illustrates how the amplitude of the fundamental component of the 6-pulse, three-level inverter's ac output voltage could be adjusted by means of the dead period γ .

Fig. 2.12 now compares the harmonic content and total harmonic distortion obtained from the simulation model with that predicted by the theoretical equations for the 6-pulse inverter. The 5th, 7th, 11th, 13th, 17th and 19th harmonics were used to calculate the harmonic content and total harmonic distortion in both the theory and the simulation results of Fig. 2.10 and Fig. 2.12. The

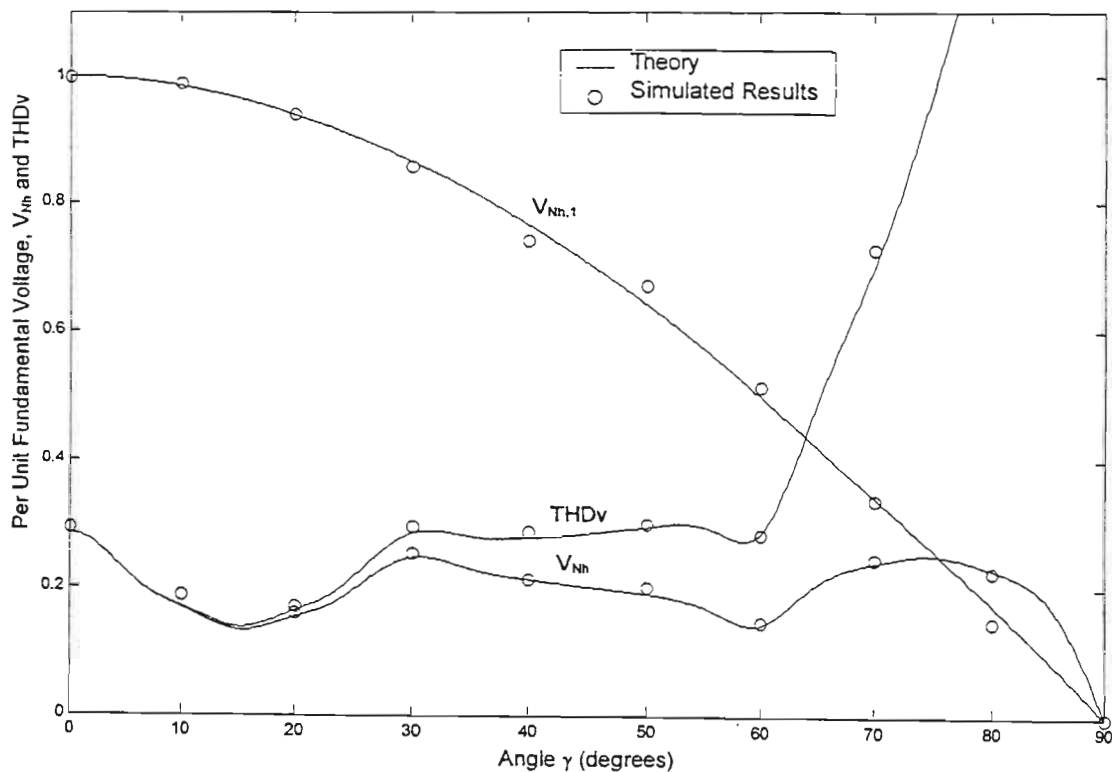


Fig 2.12: Amplitude of Fundamental voltage, Harmonic Content and Total Harmonic Distortion Factor as a function of γ for the 6-pulse inverter: theory vs. EMTDC simulation results.

harmonic distortion present in the simulated inverter voltage waveforms agrees closely with the theoretical values; as γ is increased, the harmonic distortion initially decreases and then increases for values of γ above 15.35° . On the basis of this close agreement and careful checking of time domain wave shapes, it was concluded that the implementation of the 6-pulse inverter model in EMTDC was correct.

2.4 The 12-Pulse Three-Level Inverter

As mentioned in the previous section, improved quality ac voltages can be obtained by phase shifting and adding the quasi-square wave outputs of a number of 6-pulse inverters. This section describes how the outputs of two 6-pulse inverters are combined, using a phase-shifting magnetic circuit, to form a 12-pulse inverter.

2.4.1 The Topology And Operation Of The 12-Pulse Three-Level Inverter

Fig 2.13 shows how two 6-pulse inverters, which are operated from the same DC link capacitor, are connected together to form a 12-pulse inverter. Each of the phase legs A1, B1, C1, D1, E1 and F1 is the same as the pole topology shown earlier in Fig. 2.1; as in the 6-pulse inverter, the neutral of the three-phase load is *not* connected to the midpoint of the capacitors. The expanded view in Fig. 2.13 shows the winding details of the transformers used to combine the output voltages of the two 6-pulse inverters to generate a 12-pulse harmonic neutralized voltage. The ABC 6-pulse inverter voltages are fed to a Y-Y transformer and the DEF 6-pulse inverter voltages are fed to a Δ -Y transformer. The secondary windings of each of these transformers are connected together to form the three-phase output voltages (XYZ) that feed the load. The pole voltage fundamental phasors of DEF inverter, ($V_{D,1}$, $V_{E,1}$, and $V_{F,1}$) are 120° apart, as are the pole voltage fundamental phasors of the ABC inverter ($V_{A,1}$, $V_{B,1}$, and $V_{C,1}$). The displacement angle ρ , between the three phase voltages of two consecutive 6-pulse inverters in a multi-pulse inverter arrangement is $2\pi/6m$, where m is the total number of 6-pulse inverters used [27]; hence, the fundamental voltage phasor set of the DEF inverter lags the fundamental voltage phasor set of the ABC inverter by 30° .

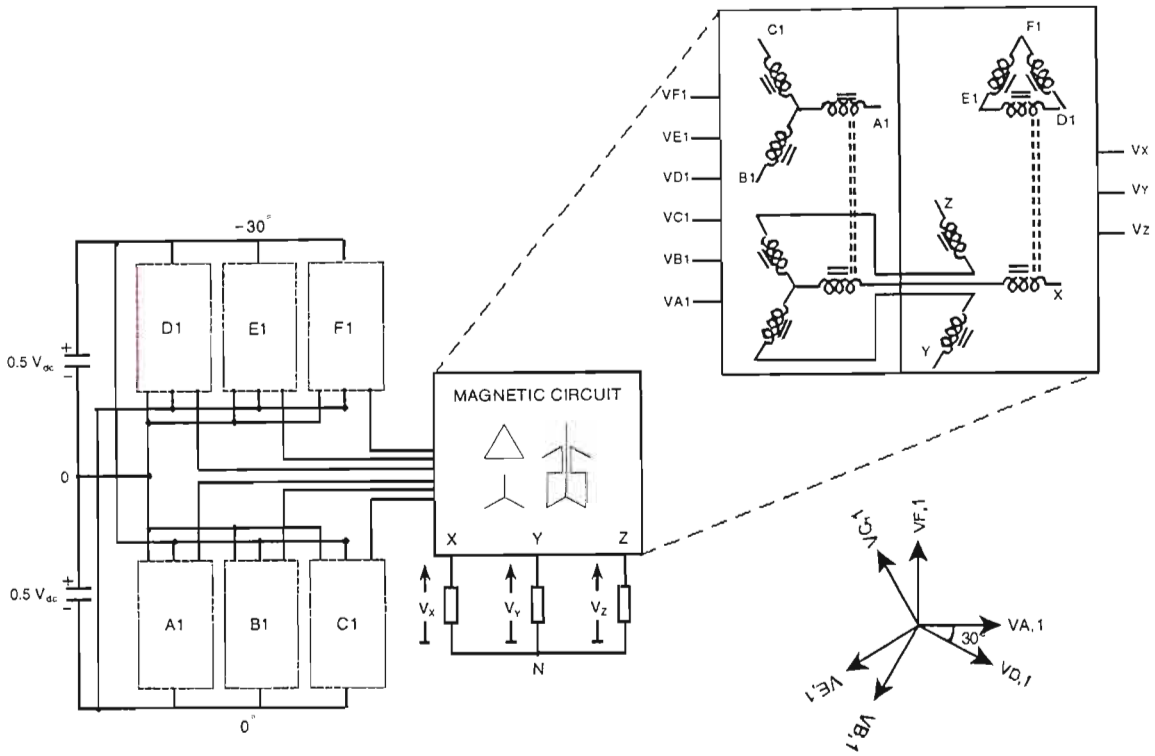


Fig 2.13: A 12-pulse Harmonic Neutralized Inverter Configuration with three-level poles, and a Magnetic Circuit for the 12-pulse Inverter [27].

The final phase angles of the fundamental and harmonics in the output voltages are determined by the phase shifts between individual poles (as determined by the low-level firing controls) and the phase shift that then occurs when these pole voltages are added magnetically (by the phase shifting transformer). This transformer is configured in such a way that if an inverter pole voltage has a relative phase of $-\rho$ (in this case, -30° or $-\pi/6$ radians) then the fundamental and all harmonic components of this voltage get a phase shift of $+\rho$ in the positive direction irrespective of their sequence [27]. Table 2.1 shows, for the first twenty-five harmonic components, the initial and final phase (after the transformer) between the voltages of poles A and D. The output waveforms contain harmonic components such as the negative sequence 5th, positive sequence 7th, negative sequence 11th, positive sequence 13th and so on. The method of calculating the final phase angle is by multiplying the harmonic number by the time shifting angle $-\rho$, then adding the product with the phase shifting angle $+\rho$.

Table 2.1: Phase angles of a 12-pulse inverter phasors.

n	POLE A			POLE D		
	initial phase	transformer phase shift	final phase angle	initial phase	transformer phase shift	final phase angle
5	$-5 \cdot (0)$	0	0	$-5 \cdot (-\pi/6)$	$+\pi/6$	π
7	$+7 \cdot (0)$	0	0	$+7 \cdot (-\pi/6)$	$+\pi/6$	π
11	$-11 \cdot (0)$	0	0	$-11 \cdot (-\pi/6)$	$+\pi/6$	0
13	$+13 \cdot (0)$	0	0	$+13 \cdot (-\pi/6)$	$+\pi/6$	0
17	$-17 \cdot (0)$	0	0	$-17 \cdot (-\pi/6)$	$+\pi/6$	π
19	$+19 \cdot (0)$	0	0	$+19 \cdot (-\pi/6)$	$+\pi/6$	π
23	$-23 \cdot (0)$	0	0	$-23 \cdot (-\pi/6)$	$+\pi/6$	0
25	$+25 \cdot (0)$	0	0	$+25 \cdot (-\pi/6)$	$+\pi/6$	0

2.4.2 Time-Domain Simulation Results From PSCAD/EMTDC

A simulation model of the 12-pulse three-level inverter in Fig. 2.13 has been developed by the author in PSCAD/EMTDC by connecting in parallel two of the 6-pulse inverter models described in the previous section. The two 6-pulse three-level inverters are connected in parallel to the same dc voltage sources described in section 2.2.4. For the purposes of the investigations in this section, the ac output of the 12-pulse inverter was connected to a three-phase pure resistive load with a floating neutral. A low-level firing control scheme for the individual turn-off devices in a three-level 12-pulse inverter has also been developed as part of this simulation model. As with the previous inverter models described, this firing control scheme has, as its inputs, the desired value of dead angle γ and the instantaneous phase angle of the fundamental three-phase ac voltage set required at the output of the inverter. Based on these inputs, the 12-pulse firing controls calculate the instantaneous phase angles required for each pole voltage and hence the firing signals for the individual turn-off devices in each of the six poles of the 12-pulse inverter. The full details of the 12-pulse inverter model and its firing controls are shown in Appendix A.4. In a similar manner to what was done for the 6-pulse inverter, this simulation model was then used to investigate the ac output waveforms of the 12-pulse inverter for a range of values of γ .

Fig. 2.14 shows a time-domain simulation of the instantaneous and RMS voltages of phase a of the 12-pulse inverter in the EMTDC model for three different values of the dead period $\gamma = 20^\circ$,

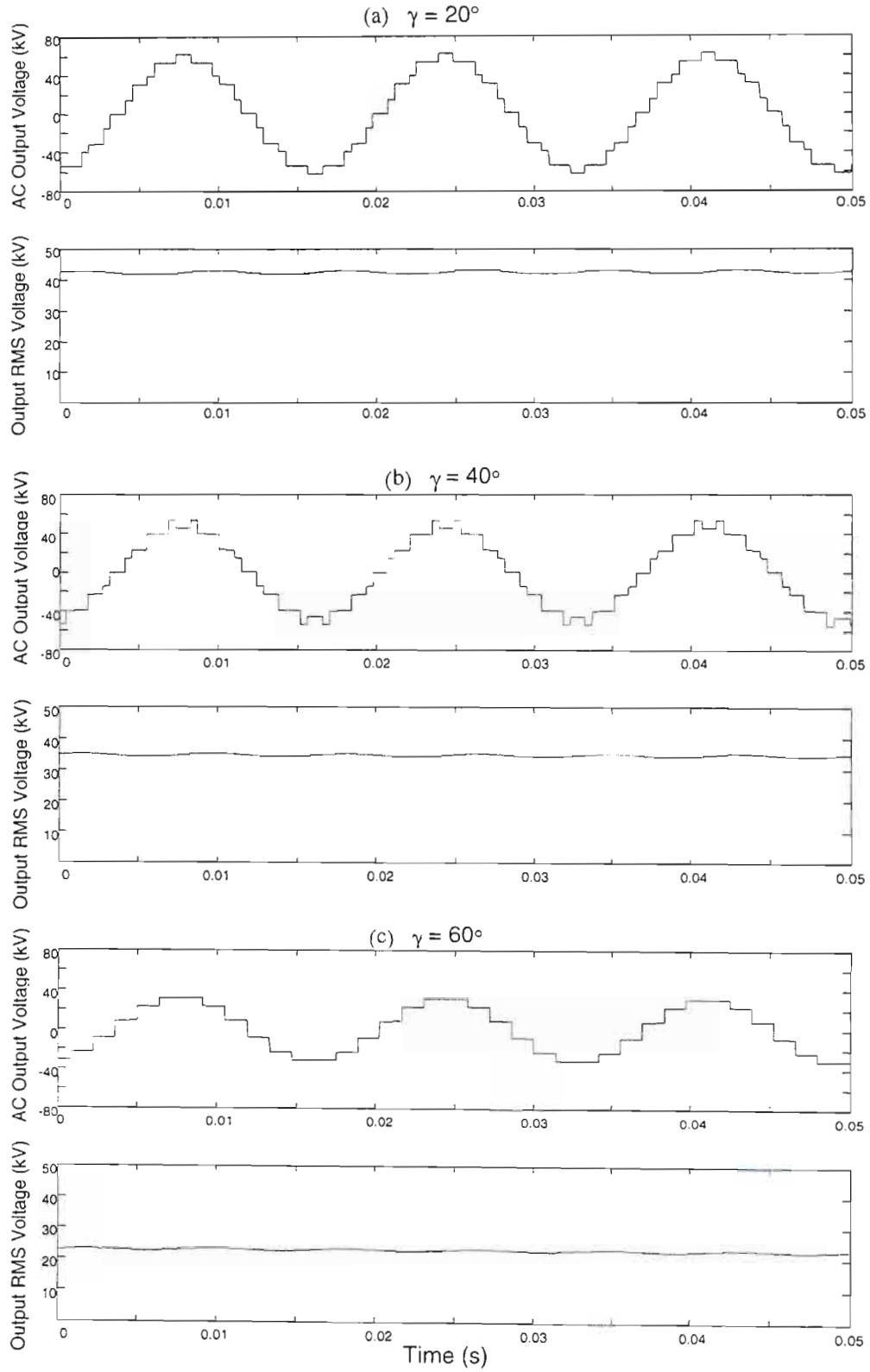


Fig.2.14: Simulated output instantaneous and RMS voltages from a three-phase, three-level, 12-pulse inverter with: (a) $\gamma = 20^\circ$; (b) $\gamma = 40^\circ$; (c) $\gamma = 60^\circ$.

40° and 60° . The simulation result shows that the phase to neutral voltages across each resistive load exhibit eleven distinct voltage levels. Earlier, Fig. 2.8 showed that the effect of changing the dead period γ in a 6-pulse inverter is to change the amount of time that the phase to neutral voltage spends at each of the seven possible voltage levels. Similarly, Fig. 2.14 now shows that, in the 12-pulse inverter, the effect of changing γ is to change the amount of time that the phase to neutral voltage of each phase spends at each of the eleven possible voltage levels.

Besides the fact that the number of inverter pulses has been increased from six to twelve by judicious phase shifting of the two 6-pulse inverters, the issue of zero sequence current described in section 2.3.2 is still accountable for the increased number of voltage levels. In the simulation results of Fig. 2.14, the three-phase load is connected to a neutral that is not connected to the midpoint of the dc sources i.e. the neutral is not connected to ground. If the neutral were grounded, the inverter output voltages (v_{XO} , v_{YO} and v_{ZO}) would have seven voltage levels as shown in the simulation results in Fig. 2.15.

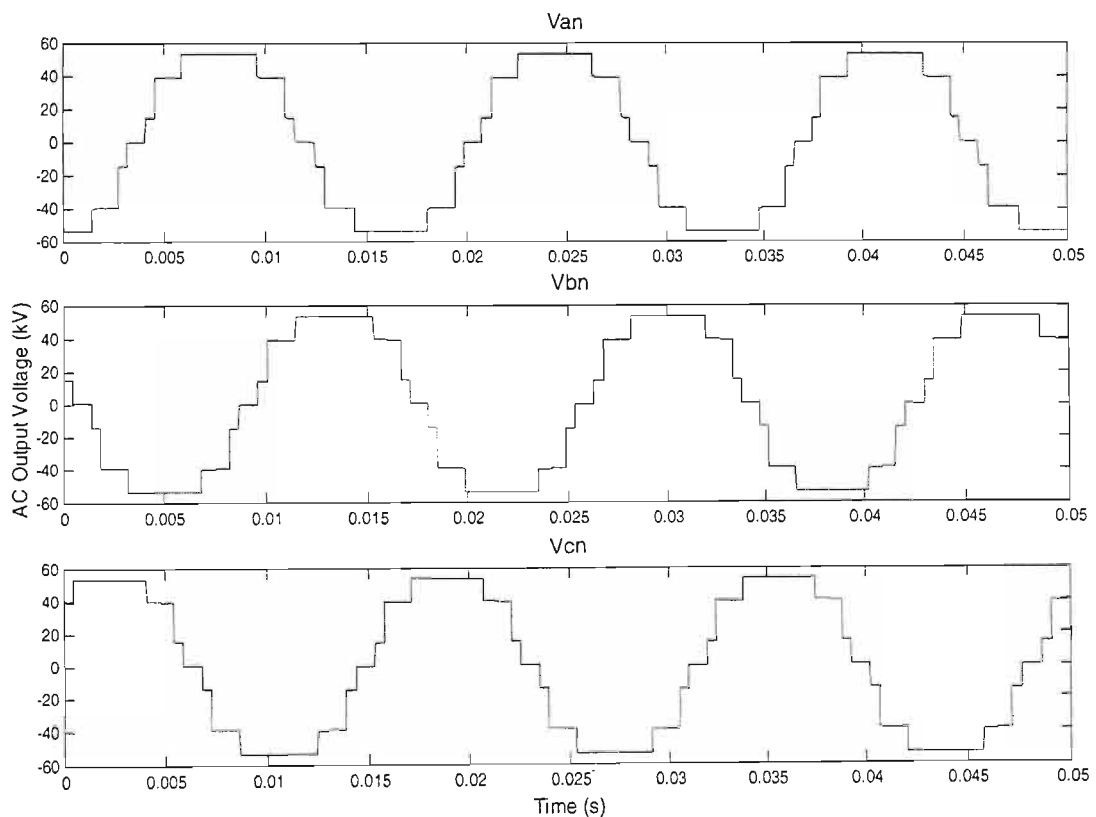


Fig.2.15: Simulated output voltage waveforms from a three-phase, three-level, 12-pulse inverter for $\gamma=20^\circ$ with the three-phase load neutral grounded.

When γ is 40° , as shown in Fig. 2.14(b), the number of voltage levels is still eleven as in the waveform shown in Fig. 2.14(a) (when $\gamma = 20^\circ$) but instead of the waveform looking “convex”, as it peaks, it is now “concave”. When γ is further increased to 60° the output voltages spend time in only six of the possible eleven levels, and the maximum and minimum amplitudes of the voltage waveform have also decreased when compared to $\gamma = 20^\circ$. The RMS voltage waveforms in Fig. 2.14 show that as γ increases, the effective value of the fundamental ac output voltage likewise decreases. The RMS voltage magnitude decreases from 42.7kV to 34.9kV to 22.8kV, as γ increases from 20° to 40° to 60° respectively. Therefore the RMS voltage will be at the highest when $\gamma = 0^\circ$. The RMS voltage would be zero if $\gamma = 90^\circ$, since the conduction period σ would be 0° ($\sigma = 180^\circ - 2\gamma$).

2.4.3 The Frequency-Domain Characteristics Of The 12-Pulse Three-Level Inverter

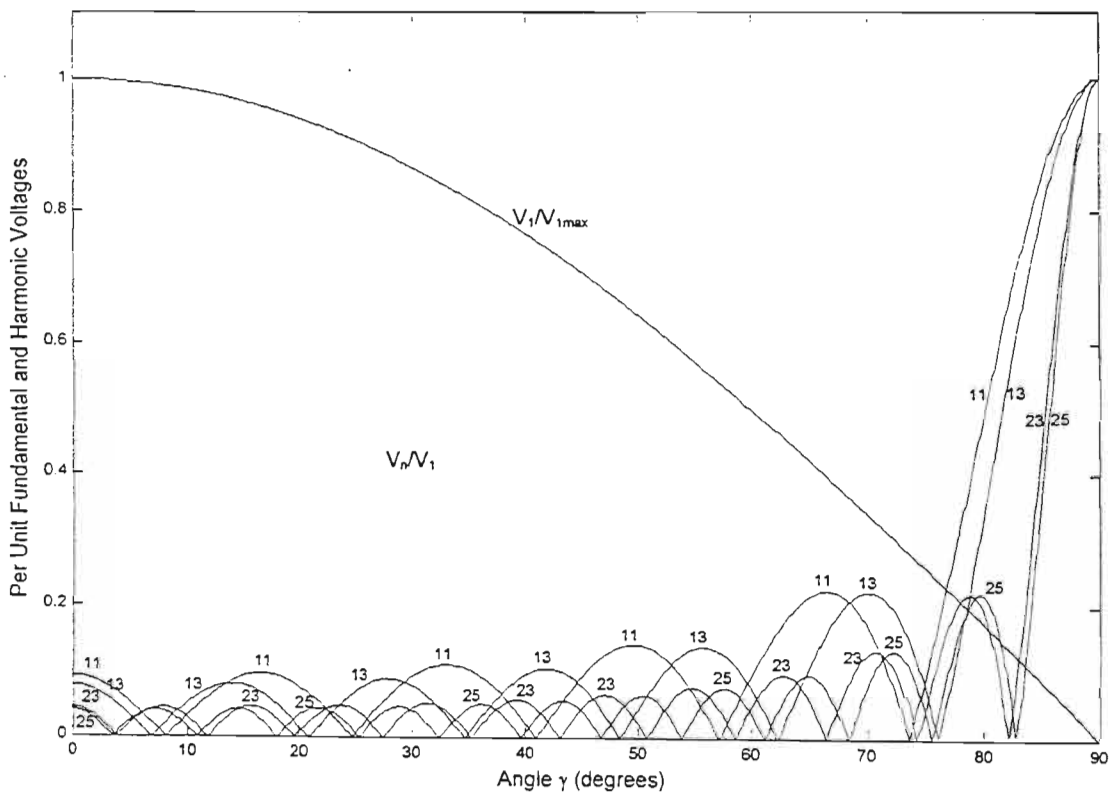


Fig.2.16: Fundamental and harmonic voltages for a 12-pulse three-level inverter based on theory [27].

As explained in the previous section, the pole voltages of each of the 6-pulse inverters in a 12-pulse inverter exhibit a 6-pulse harmonic neutralized waveform with components $n = 6k \pm 1$ for $k = 1, 2, 3$, etc. However, with reference to Fig. 2.13 and Table 2.1, the harmonic components ($n = 6k \pm 1$ for $k = 1, 3, 5$, etc.) of the DEF inverter are in opposite phase with the corresponding harmonic components of the ABC inverter, while the harmonic components ($n = 6k \pm 1$ for $k = 2, 4, 6$, etc.) of the DEF inverter are in phase with the corresponding harmonic components of the ABC inverter. Therefore, when the outputs from each 6-pulse inverter are combined by connecting the corresponding phases in series, a 12-pulse harmonic neutralized waveform is obtained. This 12-pulse output voltage exhibits a fundamental component and odd harmonic components (n) still given by Equations (2.1) and (2.2), but now with $n = 12k \pm 1$ for $k = 1, 2, 3$, etc. [27].

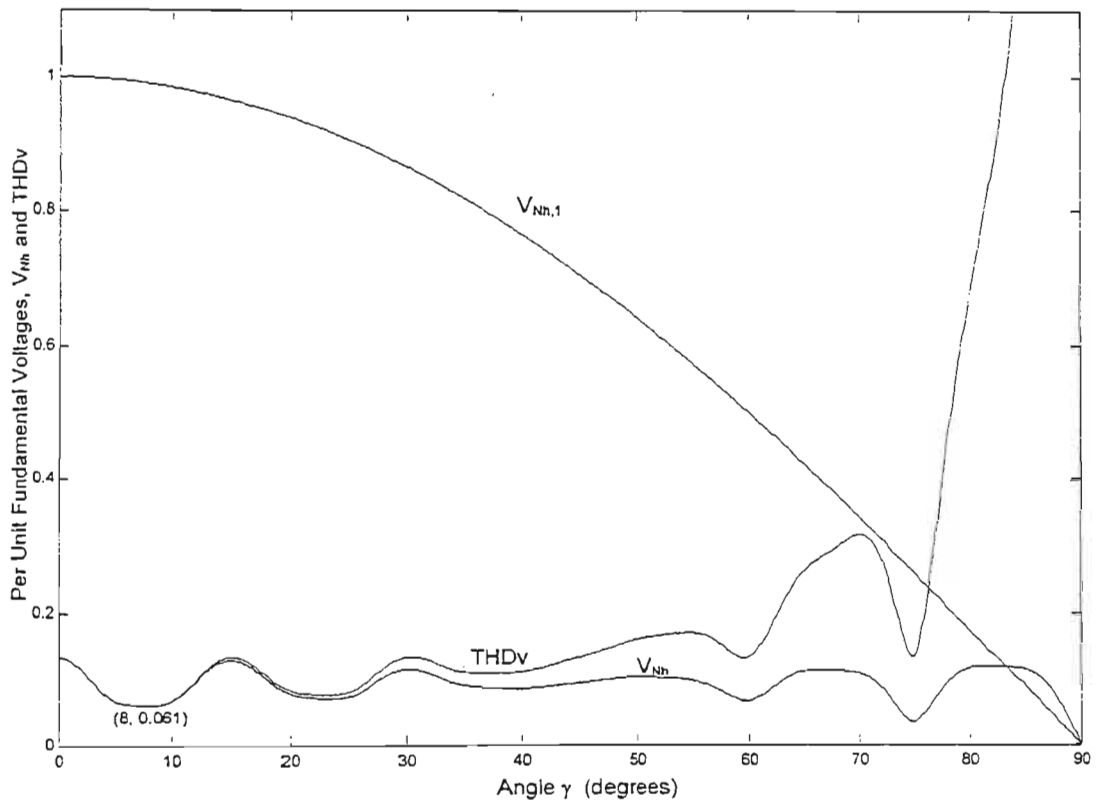


Fig.2.17: Amplitude of fundamental voltage, harmonic content and total harmonic distortion (THDv) as a function of γ for the 12-pulse inverter, based on theory [27].

Fig. 2.16 shows the normalized fundamental and harmonic voltages for a 12-pulse inverter calculated using Equation (2.1). At $\gamma = 0^\circ$, the fundamental and the harmonic components have the highest possible amplitudes. Fig. 2.16 shows that the fundamental amplitude decreases as γ increases from 0° to 90° , while the per unit amplitudes of 11th, 13th, 23rd, and 25th etc. harmonics successively increase and decrease according to Equation (2.1), reaching zero at certain angles of γ , as γ is increased towards 90° .

The theoretical graphs of the harmonic content and total harmonic distortion of the 12-pulse three-level inverter, calculated by using Equations (2.1), (2.2), (2.6) and (2.7), are shown in Fig. 2.17. The curves show that at $\gamma = 0^\circ$ (when the inverter behaves like a two-level device), the harmonic content is approximately 13.29%, which shows a significant reduction when compared to 31% at $\gamma = 0^\circ$ from the 6-pulse inverter. The optimum operating value of dead angle for a 12-pulse inverter is at 8° where the harmonic content is 6.1% and the fundamental amplitude is reduced by about 1%. Compared to the 6-pulse inverter, the 12-pulse inverter shows a lower percentage of harmonic content (6.1% to 16%) and higher fundamental amplitude (99.03% to 96.43%) at the optimum angle (8° to 15.35°).

2.4.4 Frequency-Domain Characteristics From PSCAD/EMTDC Simulation Model

The time domain simulations using the 12-pulse inverter model developed for EMTDC were repeated for a range of values of γ from 0° to 90° and Fast Fourier Transform (FFT) analysis used to determine the amplitude of the ac output voltages (fundamental and harmonics) as functions of γ . Fig. 2.18 illustrates how the amplitude of the fundamental component of the 12-pulse, three-level inverter's ac output voltage could be adjusted by means of the dead period γ . Fig. 2.18 shows that the harmonic spectrum of the ac output voltages in the 12-pulse inverter simulation model agrees well with the theory. It also illustrates that the amplitude of the fundamental component of the 12-pulse three-level inverter's ac output voltage could be adjusted by means of the dead period, γ .

Fig. 2.19 now compares the harmonic content and total harmonic distortion obtained from the simulation model for the 12-pulse inverter with that predicted by the theoretical equations. Since PSCAD allows only a limited number of harmonic frequencies to be calculated simultaneously, only the 11th, 13th, 23rd, 25th harmonics were simulated for the calculation of harmonic content and total harmonic distortion. The theoretical graph shown in both Fig. 2.17 and Fig. 2.19 also used the above-mentioned four harmonics for easy comparison with the simulated results.

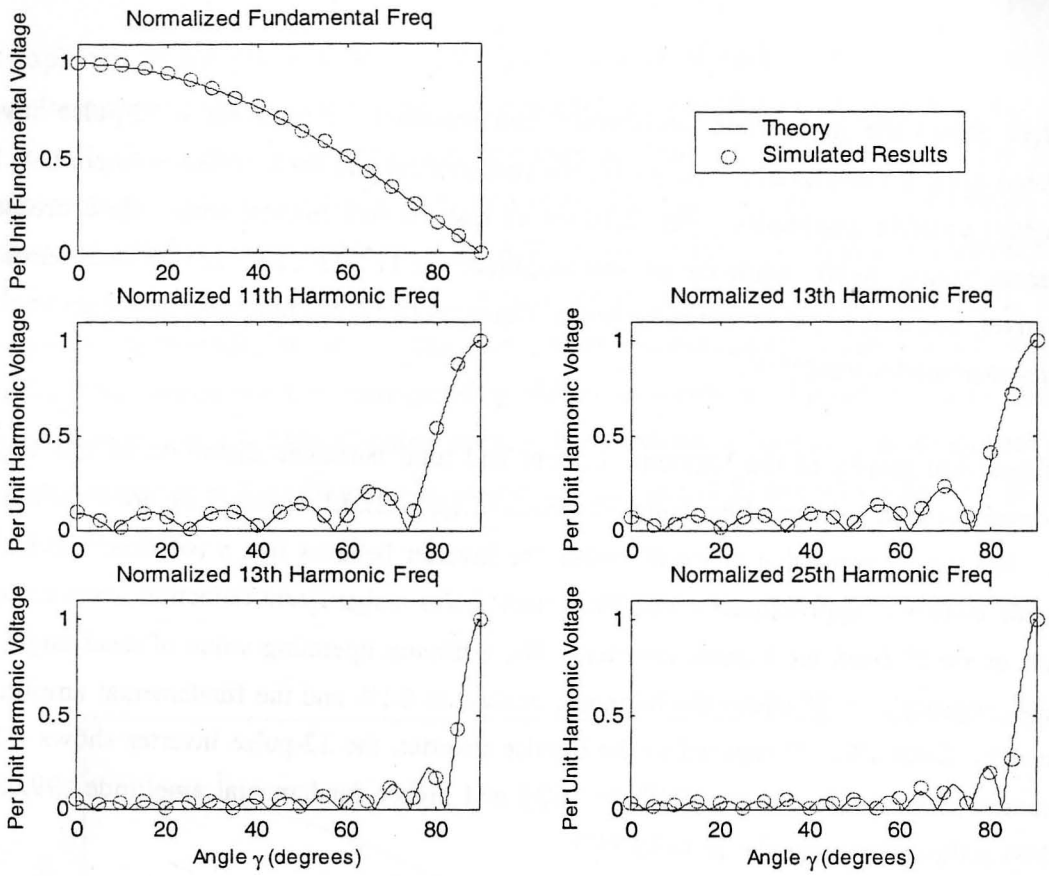


Fig 2.18: Fundamental and harmonic voltages for a 12-pulse inverter from EMTDC simulation.

The harmonic distortion present in the simulated inverter voltage waveforms agrees closely with the theoretical values. On the basis of this close agreement and careful checking of time domain wave shapes, it was concluded that the implementation of the 12-pulse inverter model in EMTDC was correct.

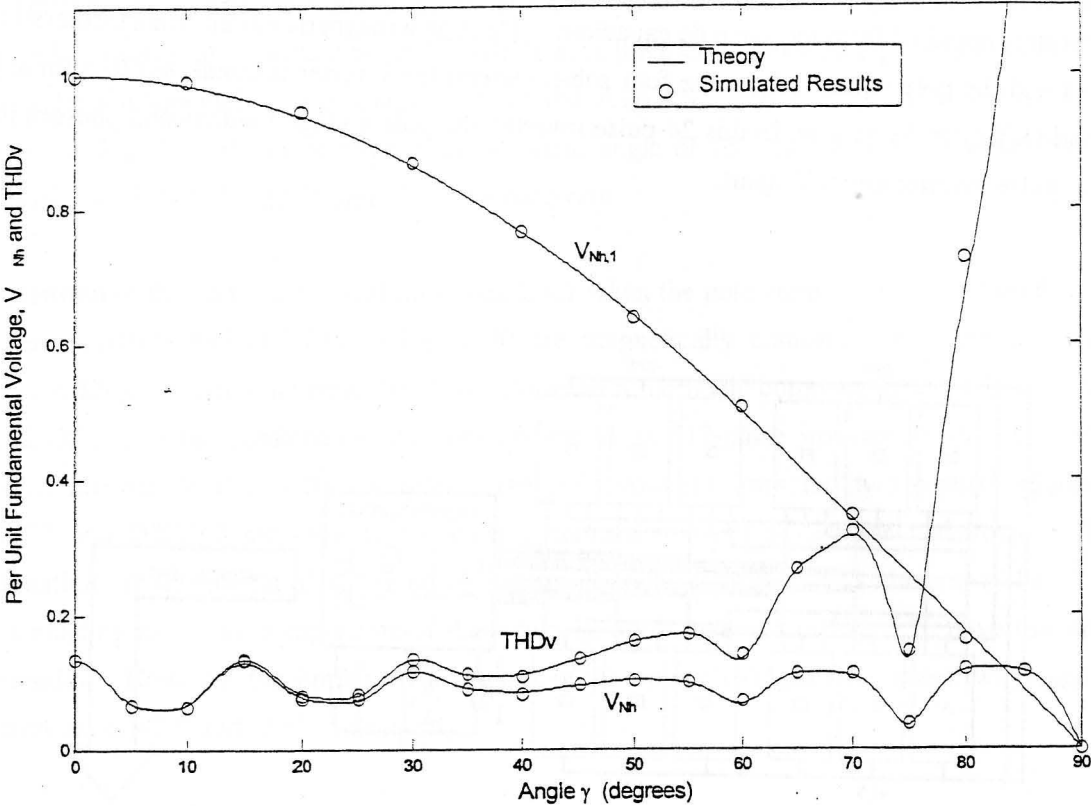


Fig 2.19: Amplitude of Fundamental voltage, Harmonic Content and Total Harmonic Distortion Factor as a function of γ for a 12-pulse inverter: theory vs. the EMTDC simulation results.

2.5 The 24-Pulse Three-Level Inverter

The presence of 12-pulse harmonic components in the inverter output voltage might not be acceptable in many applications [27]. This section therefore considers a 24-pulse harmonic neutralized inverter topology that offers higher quality voltage waveforms than the 12-pulse topology of the previous section. As in the case of the twelve-pulse inverter, the 24-pulse inverter comprises a number of six-pulse inverters connected together, with their outputs being added using special transformers; the result is a new ac output voltage waveform that is a closer approximation to a sine wave than the twelve-pulse inverter waveforms.

2.5.1 The Topology And Operation Of The 24-Pulse Three-Level Inverter

Fig. 2.20 shows a 24-pulse harmonic neutralized inverter, which comprises four six-pulse inverters operated from the same dc capacitor. Through a magnetic circuit (transformers to scale and add the pole voltages from the four sub-inverters) the inverter is connected to a three-phase load (XYZ) on its ac side. In this 24-pulse inverter, the pole voltage fundamental phasors in each six-pulse inverter are 120° apart.

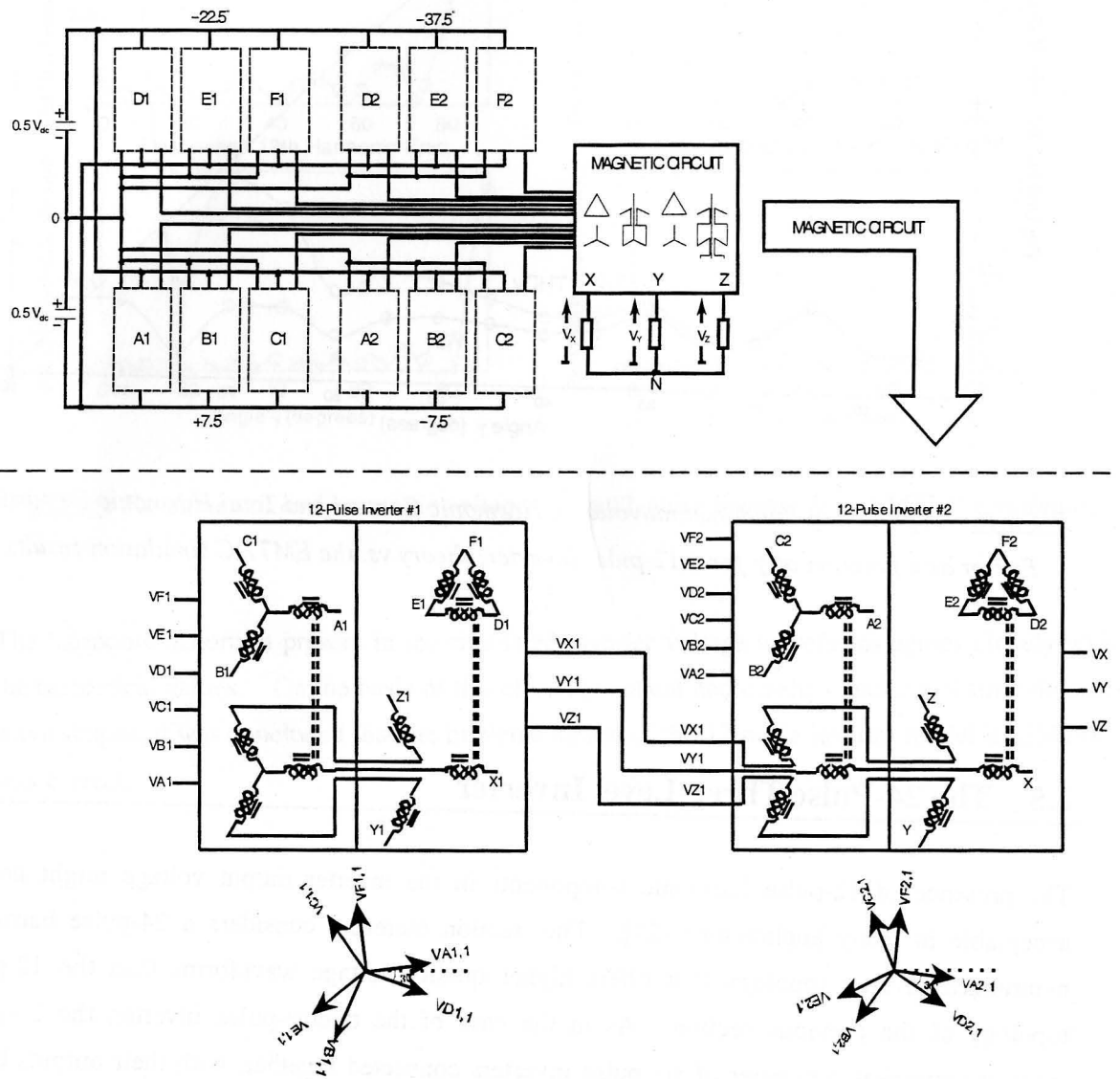


Fig 2.20: A 24-pulse Harmonic Neutralized Inverter Configuration with 3-level poles, and a Magnetic Circuit for the 24-pulse Inverter [27].

As explained previously, the displacement angle between consecutive 6-pulse inverters in a multi-pulse inverter arrangement is $2\pi/6m$, where m is the total number of 6-pulse inverters used [27]. The fundamental voltage phasor sets of the A1B1C1, A2B2C2, D1E1F1 and D2E2F2 inverters in Fig. 2.18 therefore have a displacement angle of 15° , and they are time shifted by angles of $+7.5^\circ$, -7.5° , -22.5° and -37.5° respectively.

By extension of the earlier argument in section 2.4.1 when the pole voltages from the two 6-pulse inverters A1B1C1 and D1E1F1 in Fig. 2.20 are magnetically combined, the output voltage exhibits a 12-pulse harmonic neutralized waveform with harmonic components $n = 12k \pm 1$ for $k = 1, 2, 3$, etc. This combination can be thought of as “12-pulse inverter 1” in the overall 24-pulse inverter of Fig. 2.20. Similarly, the pole voltages from the two 6-pulse inverters A2B2C2 and D2E2F2 are also magnetically combined to form a 12-pulse waveform. This combination can be thought of as “12-pulse inverter 2” in the overall 24-pulse inverter of Fig. 2.20. Corresponding harmonic components of these two 12-pulse inverters in Fig. 2.20 have the same magnitudes. However, the fundamental phasors of the output voltages from these two 12-pulse inverters are at $+7.5^\circ$ and -7.5° respectively.

2.5.2 Time-Domain Simulation Results From PSCAD/EMTDC

A simulation model of the 24-pulse three-level inverter in Fig. 2.20 has been developed by the author in PSCAD/EMTDC by connecting together four of the 6-pulse inverter models described in section 2.2. Once again, as part of this simulation model, a low-level firing control scheme for the individual devices of a 24-pulse inverter has been developed. The four 6-pulse three-level inverters of the 24-pulse inverter model are connected in parallel to the same dc voltage sources described in section 2.2.4. The twelve outputs of the 6-pulse inverters are connected to phase shifting transformers to complete the 24-pulse three-level inverter. The ac outputs of this 24-pulse inverter were then connected to a three-phase pure resistive load with a floating neutral. The full details of the 24-pulse inverter model and its firing controls are shown in Appendix A.5. In a similar manner to the investigations of the 6-pulse and 12-pulse inverters, this simulation model was used to generate the ac output waveforms of the 24-pulse inverter for a range of values of γ .

Fig. 2.21 shows a time-domain simulation of the instantaneous and RMS voltages of phase a of the 24-pulse inverter in the EMTDC model for three different values of the dead period $\gamma = 20^\circ$, 40° and 60° . The simulation result shows that the phase to neutral voltages across the resistive load exhibit twenty-one distinct voltage levels. Fig. 2.21 shows that, in the 24-pulse three-phase

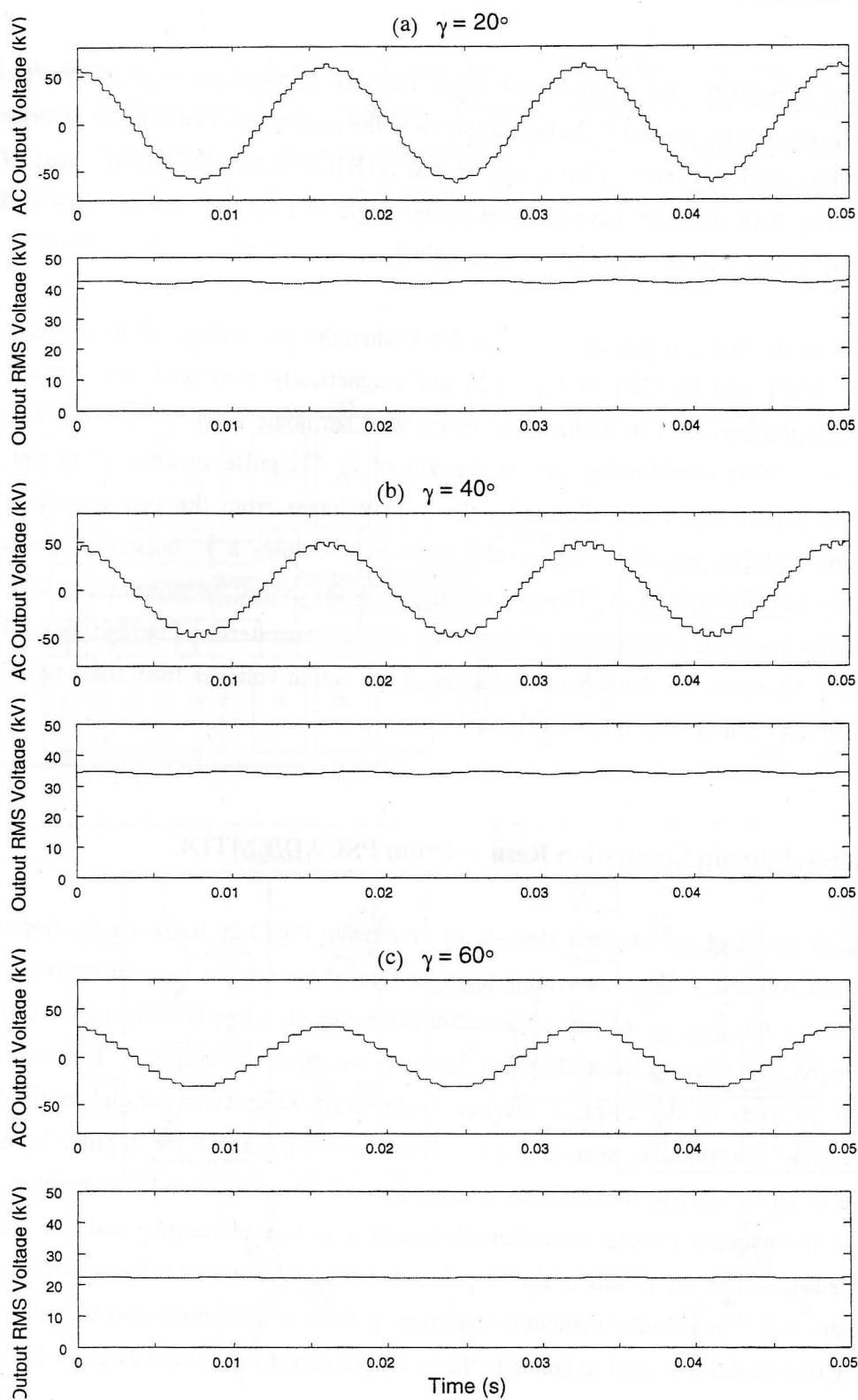


Fig.2.21: Simulated output instantaneous and RMS voltages from a three-phase, three-level, 24-pulse inverter with: (a) $\gamma = 20^\circ$; (b) $\gamma = 40^\circ$; (c) $\gamma = 60^\circ$.

inverter, the effect of changing γ is to change the amount of time that the phase to neutral voltage of each phase spends at each of these twenty-one possible voltage levels.

As with the 6-pulse and 12-pulse inverter configurations, the number of levels in the ac output voltages of the 24-pulse inverter depends on the connection of the load neutral. This is illustrated in Fig. 2.22 which shows that the 24-pulse inverter output is reduced to thirteen voltage levels when the neutral of the load is connected to the midpoint of the two capacitors.

Fig 2.21 (b) and (c) show that for the 24-pulse inverter, as with the 6-pulse and 12-pulse inverters, an increase in dead angle γ results in a decrease in the amplitude of the fundamental output voltage.

The RMS value of the voltage magnitude in Fig. 2.21 decreases from 58kV to 49.7kV to 31.1kV, as γ increases from 20° to 40° to 60° respectively. However, by comparison with the 6-pulse and

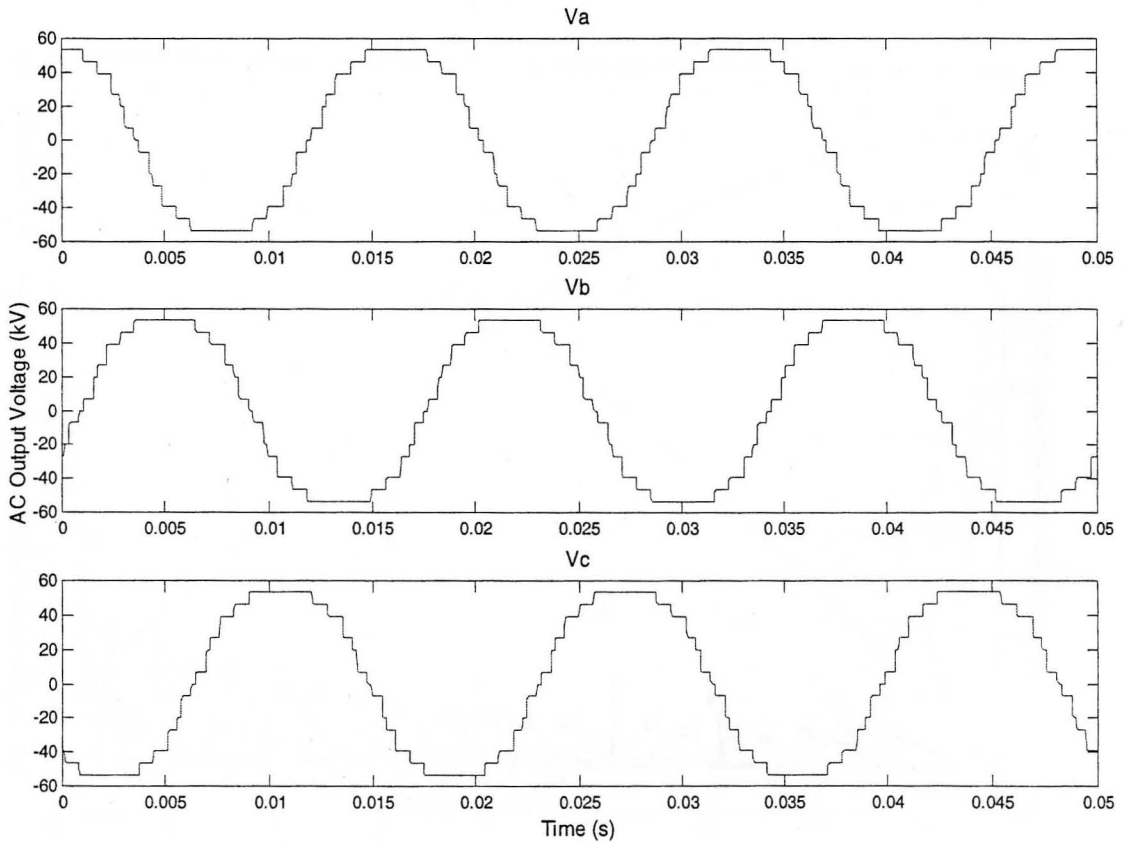


Fig.2.22: Simulated output voltage waveforms from a three-phase, three-level, 24-pulse inverter for $\gamma=20^\circ$ with the three-phase load neutral grounded.

12-pulse inverter waveforms shown earlier, it can immediately be seen (simply by observation of the time domain waveforms in Fig. 2.21) that the quality of the near-sinusoidal voltages of the 24-pulse inverter remains very high even at increased values of γ . This is further confirmed in the following section.

2.5.3 The Frequency-Domain Characteristics Of The 24-Pulse Three-Level Inverter

The resultant output voltage of the 24-pulse inverter exhibits a fundamental component and odd harmonic components, each of which has an amplitude of

$$V_{x,n} = \frac{2}{n\pi} v_{DC} \cos\left(\frac{n\pi}{24}\right) \cos n\gamma \quad (2.8)$$

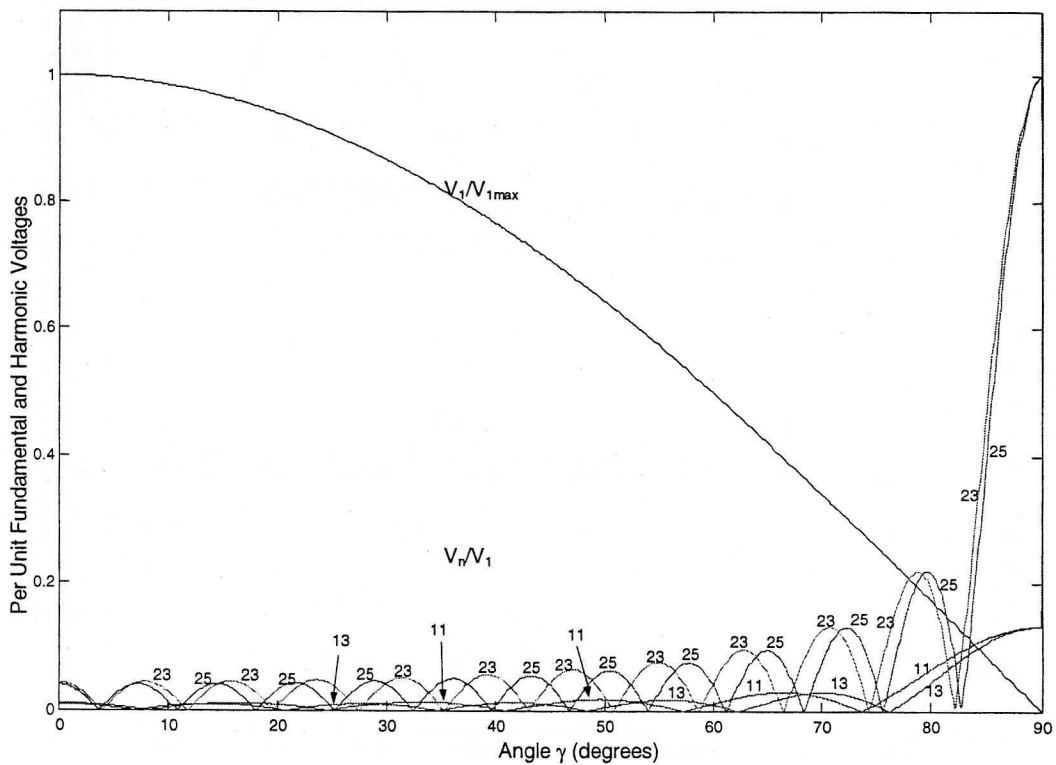


Fig.2.23: Fundamental and harmonic voltages for a 24-pulse inverter based on theory [27].

where $n = 1$ and $12k \pm 1$ for $k = 1, 2, 3$, etc. [27] The amplitude of any odd harmonic component (n) normalized to the fundamental component is

$$\frac{V_{X,n}}{V_{X,1}} = \frac{\cos(n\pi/24) \cos n\gamma}{n \cos(\pi/24) \cos \gamma} \quad (2.9)$$

where $n = 12k \pm 1$ for $k = 1, 2, 3$, etc. [27].

Fig. 2.23 shows the fundamental and harmonic voltages as a function of γ for the 24-pulse three-level inverter based on Equations (2.8) and (2.9). As with the 6-pulse and 12-pulse inverters, the fundamental amplitude decreases as γ increases from 0° to 90° . The per unit amplitude of the harmonic components shown in Fig. 2.23 illustrate that each of these harmonic components initially decreases as γ increases; each harmonic component's amplitude then reaches zero at a specific value of γ , and then successively increases from and decreases to zero as γ approaches 90° .

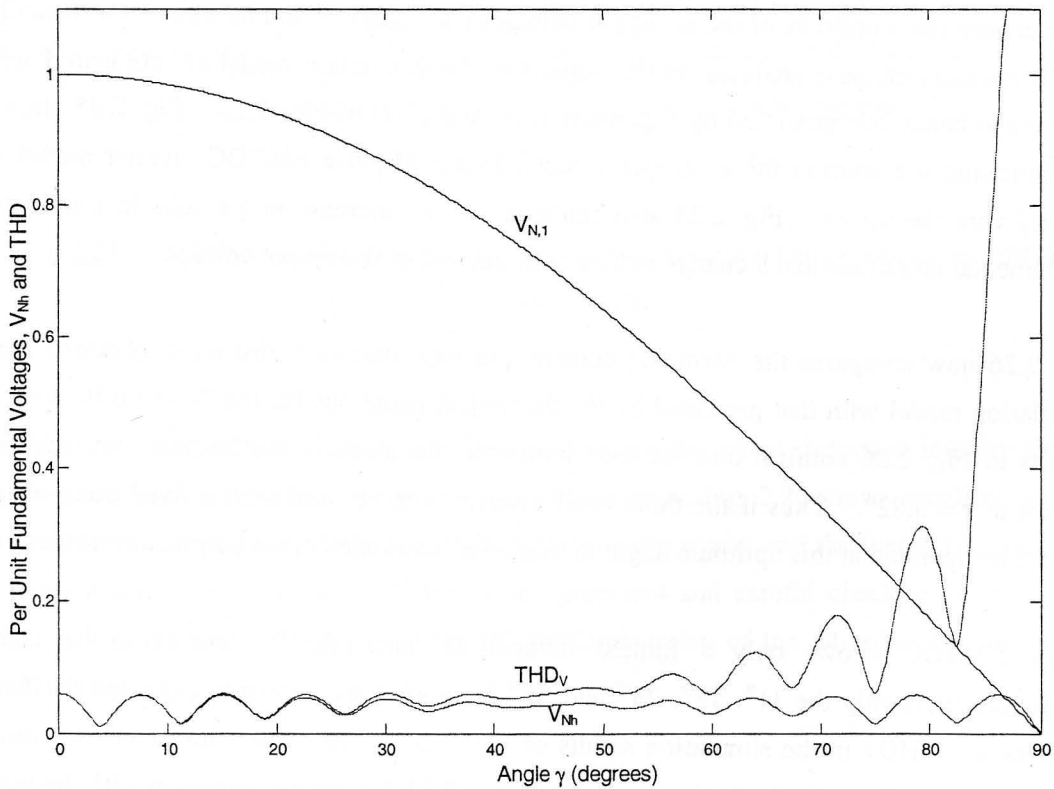


Fig.2.24: Normalized harmonic components of output voltages from a 24-pulse inverter based on theory [27].

Fig. 2.24 shows the normalized harmonic content and the total harmonic distortion of the output voltages from a 24-pulse harmonic-neutralized inverter as a function of harmonic order (n) as calculated using the above Equations (2.6), (2.7), (2.8) and (2.9). Fig. 2.24 shows that at $\gamma_{\text{optimum}} = 3.82^\circ$, the fundamental amplitude decreases by 0.21% from that obtained from a two-level operation of the poles, and that the harmonic content is reduced from 6.11% when $\gamma = 0^\circ$, to 1.19% at this optimum value of dead angle. At the optimum angle, the 24-pulse inverter has the smallest THDv when compared to the 6-pulse and 12-pulse inverters. Fig. 2.24 also confirms what was observed in the time domain waveforms of Fig. 2.21: in the case of the 24-pulse inverter the total harmonic distortion of the ac output waveform remains very low (below 10%) for values of γ as high as 60° . By comparison, the 12-pulse inverter has a total harmonic distortion of 6.1% even at its optimum value of γ .

2.5.4 Frequency-Domain Simulation Results From PSCAD/EMTDC

The time domain simulations using the 24-pulse inverter model developed for EMTDC were repeated for a range of values of γ from 0° to 90° and Fast Fourier Transform (FFT) analysis used to determine the amplitude of the ac output voltages (fundamental and harmonics) as functions of γ . The results of these analyses on the outputs of the simulation model are compared with the theoretical behaviour predicted by Equations (2.8) and (2.9) in Fig. 2.25. Fig. 2.25 shows that the harmonic spectrum of the ac output voltages in the 24-pulse EMTDC inverter model agrees closely with the theory. Fig. 2.25 also confirms that an increase in γ results in a reduction of fundamental amplitude and a change in harmonic content of the output voltages.

Fig. 2.26 now compares the harmonic content and total harmonic distortion obtained from the simulation model with that predicted by the theoretical equations for the 24-pulse inverter. The results in Fig. 2.26 confirm that the total harmonic distortion in the 24-pulse inverter is at its lowest at $\gamma = 3.82^\circ$. Thus if the three-level inverter is to be used with a fixed dc to ac gain, it should be operated at this optimum angle to minimise harmonics in the output waveforms.

Since EMTDC allows only a limited number of harmonic frequencies to be calculated simultaneously, only the 11th, 13th, 23rd and 25th harmonics were used to calculate the harmonic content and THDv in the simulation results of Fig. 2.26. The same number of harmonics was also used in the theoretical calculation shown in Fig. 2.24 for close comparison with the simulated results. The harmonic distortion present in the simulated inverter voltage waveforms agrees

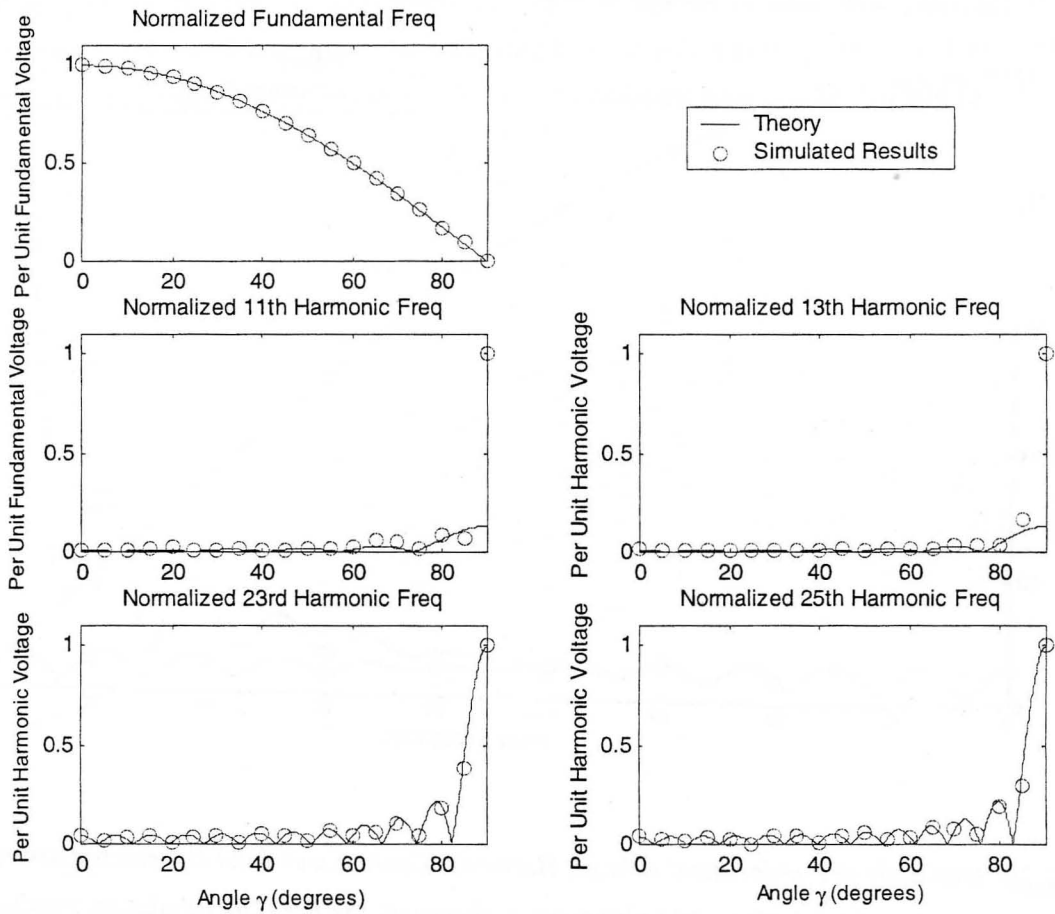


Fig.2.25: Fundamental and harmonic voltages for a 24-pulse inverter: theory vs. EMTDC simulated results.

closely with the theoretical values; as γ is increased, the harmonic distortion initially decreases and then increases for values of γ above 3.82° . Once again, Fig. 2.26 shows excellent agreement between the results obtained from the EMTDC simulation model and the theory of a three-level, 24-pulse inverter. On the basis of this close agreement and careful checking of time domain wave shapes, it was then concluded that the implementation of the 24-pulse inverter model in EMTDC was correct.

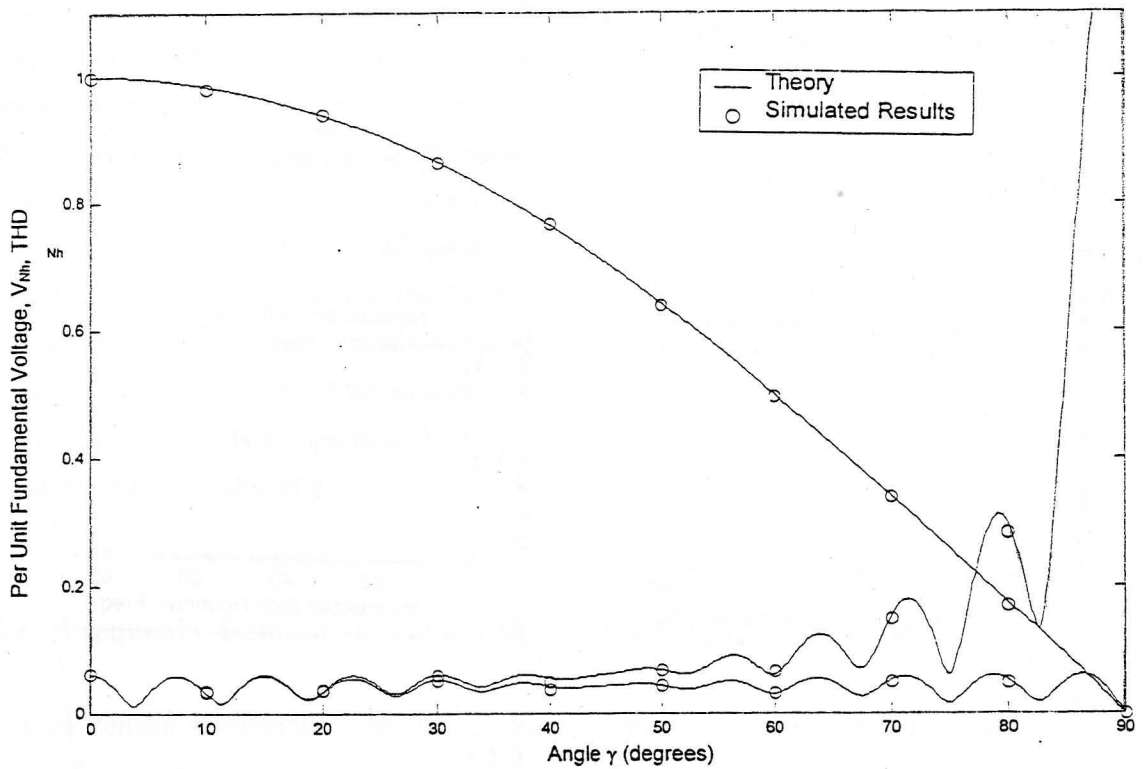


Fig 2.26: Amplitude of Fundamental voltage, Harmonic Content and Total Harmonic Distortion Factor as a function of γ for a 24-pulse inverter: theory vs. the EMTDC simulation results.

2.6 Conclusion

This chapter has investigated three different types of three-level voltage-sourced inverters, namely, the 6-pulse, 12-pulse and the 24-pulse three-level inverters. The chapter has described the development of detailed simulation models of each of these types of inverters, in the simulation package PSCAD/EMTDC. The simulation models developed in each case include detailed low-level firing controls for the power-electronic devices in the inverter. The 6-pulse and the 12-pulse inverter models were developed as intermediate steps towards the final goal of a model of a 24-pulse three-level inverter, which has sufficiently high quality output voltages for FACTS applications. The time-domain and frequency-domain results obtained from these inverter simulation models have been compared against theory and have shown excellent agreement.

This chapter has therefore demonstrated that the 24-pulse three-level inverter model that has been developed for EMTDC is sufficiently accurate for use in the modelling and analysis of an inverter-based FACTS device. The following chapter will describe how this inverter is used to implement a model of a stand alone SSSC in the simulation package PSCAD/EMTDC.

CHAPTER THREE

THE 24-PULSE INVERTER BASED SSSC

3.1 Introduction

Chapter One described conceptually how a voltage-sourced inverter can be used to construct an SSSC, either as part of a larger UPFC or as a single stand-alone device. Chapter Two then focused solely on the detailed development and operation of multi-pulse three-level inverters, where the 24-pulse inverter was shown to have a high quality, near-sinusoidal output voltage that is suitable for the construction of an inverter-based FACTS device. The previous chapter has also explained that by varying the dead angle, γ , the inverter dc-to-ac gain is varied, and can therefore be used to control the inverter ac output voltage. With the dead angle set to zero, the inverter acts as a two-level device where the output voltage from each pole switches between the positive and negative $v_{DC}/2$.

The aim of this chapter is to develop a detailed model of an SSSC suitable for accurate studies into how an SSSC might interact with rest of the transmission system. The approach in this thesis is to consider, as far as possible, standard implementations of the SSSC in the analysis. For this reason, the previous chapter developed a detailed simulation model of a 24-pulse three-level inverter typical of those actually used in transmission FACTS applications. This chapter now considers the development of detailed SSSC controls for this 24-pulse inverter. As with the inverter model itself, the emphasis here is on implementing standard SSSC controls actually used in transmission applications.

Although the model developed in Chapter Two is of a three-level inverter, the SSSC controls developed in the first part of this chapter operate this inverter only in two-level mode: the SSSC controller implemented in the first part is taken from [34], in which the inverter considered was a two-level device. Then, the second part of this chapter considers the extension of this SSSC controller [34] to exploit the full three-level capability of the inverter model developed in Chapter Two. The first part of this chapter also focuses on further demonstrating the correctness of the inverter model and of the SSSC controls developed for it, presenting simulation results to benchmark the performance of the SSSC model developed here against the results presented in [34].

3.2 The 24-Pulse Two-Level Inverter Based SSSC

3.2.1 Introduction

As mentioned in Chapter One, an SSSC is a voltage source inverter that injects a near-sinusoidal voltage, of variable and controllable magnitude in series with the transmission line. This injected voltage emulates either an inductive or capacitive reactance in series with the transmission line; by controlling the size of this emulated reactance, the SSSC is then able to influence the electric power flow in the line.

An SSSC can be operated in different modes, depending on whether or not the device is stand-alone or part of a UPFC (STATCOM and SSSC combined). In [34], Sen developed a mathematical model of a stand-alone, 24-pulse, two-level-inverter based SSSC to investigate the characteristics of such a device. Because the inverter is a two-level device, the dc-to-ac gain across the inverter is fixed and the magnitude of the ac output voltage is adjusted by controlling the inverter's dc voltage. On the other hand, Sen *et al.* developed an UPFC model in [27] where the SSSC and STATCOM are based on a 24-pulse three-level inverter. In the latter case, since the dc voltage between the SSSC and the STATCOM is controlled by the STATCOM's controller, the ac output voltage of the SSSC is varied by varying the dead angle γ , and therefore the gain across the three-level inverter of the SSSC. However, like most of the literature that focuses on SSSC, references [27] and [34] have not included the actual inverter power electronics when developing the simulation models. References [55,58,59,60,61], on the other hand, have described an SSSC model for PSCAD/EMTDC based on a 48-pulse inverter; in this case the simulation model does include the power electronic switches in the inverter, but the inverter considered is only a two-level device. Han *et al.* [42] have also developed a detailed power electronics model of SSSC, however the model is based on a three-level multi-bridge pulse width modulation inverter. Subsequently, Han *et al.* [43] developed a multi-bridge inverter-based SSSC using a three-level switching scheme, but the main focus of that study was to illustrate the injection of the compensating voltage directly into the transmission line without coupling transformers.

This section presents a detailed model of an SSSC that has been developed for the simulation package PSCAD/EMTDC. The SSSC controller used in the model is based on the work in [34], but extends this work in two ways: the SSSC model presented here is based on a three-level 24-pulse inverter topology taken from [27] (as described in Chapter Two) and can therefore be used in either of the two control modes (stand-alone SSSC or as part of a UPFC); the SSSC model presented here represents the actual power electronic devices within the SSSC inverter and their

low-level switching controls. Although the SSSC presented here is based on a three-level inverter, for the purposes of this first part of the chapter, the inverter is operated as a two-level device (i.e. dead angle $\gamma = 0^\circ$).

3.2.2 The SSSC And Transmission System Layout

Fig. 3.1 shows a single-line, diagrammatic representation of an SSSC in an ac transmission system similar to that studied in [34]; the system structure and parameters used in this chapter are the same as those in [34] in order to demonstrate the correctness of the SSSC model presented here. The transmission system in Fig. 3.1 includes a sending-end voltage source V_s and a receiving-end voltage source V_r , separated by some transmission angle, as well as inductive reactances X_s and X_r .

The SSSC itself comprises a voltage-sourced inverter and a coupling transformer that is used to insert the ac output voltage of the inverter in series with the transmission line. The magnitude and phase of this inserted ac compensating voltage are determined by the high-level SSSC controls.

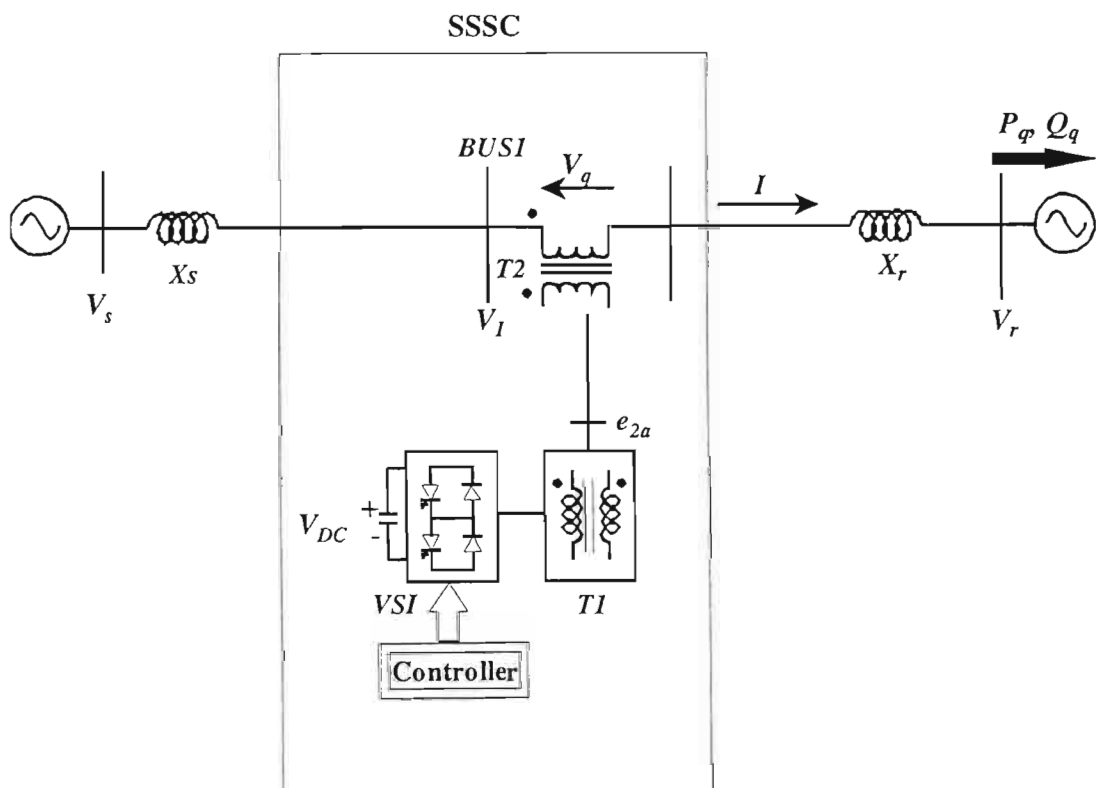


Fig.3.1: Diagram of the system used to compare the performance of the SSSC against that predicted in [34].

In this chapter, the SSSC consists of a three-level, 24-pulse harmonic neutralized voltage source inverter VSI, a phase-shifting transformer $T1$ (magnetic adding circuit), a series voltage-injecting transformer $T2$, current and voltage sensors, and a compensation controller. The power circuit, which consists of the 24-pulse three-level inverter and a magnetic adding circuit are described in Chapter Two. The following section describes in detail the SSSC control scheme used to vary the ac output voltage that is series injected into the transmission line.

3.2.3 The SSSC Controller

The three control requirements of an SSSC can be described as follows:

1. Angle Control: The compensating voltage vector V_q , injected in series with the transmission line by an SSSC must lag the line current vector I by 90° if the SSSC is operated in the capacitive mode; V_q must lead I by 90° in the inductive mode of operation.
2. Magnitude Control: The magnitude of the compensating voltage vector must be proportional to the magnitude of the line current vector,

$$V_q = kIe^{-j\frac{\pi}{2}} \quad (3.1)$$

where k is the degree of series compensation.

3. DC Voltage Regulator: The dc voltage on the inverter's storage capacitor (i.e. the inverter's voltage source) must be regulated to the required value by shifting a small component of the compensating voltage vector in phase with the line current vector in order to replenish the losses in the inverter. However, this third requirement only applies to a stand-alone SSSC, where there is no front-end converter or auxiliary source to supply the dc side of the inverter.

Fig. 3.2 shows the high-level control block diagram of a stand-alone, two-level inverter-based SSSC developed by Sen [34], where the magnitude of the ac output voltage from the SSSC is varied by controlling the magnitude of the inverter's dc capacitor voltage. Given the three control requirements of an SSSC described above, Fig. 3.2 is dissected into three corresponding sub-sections, namely, angle control, magnitude control and dc voltage regulator. The output of this high-level controller then provides the input for the gate pattern logic i.e. the low-level

controls which determine the firing signals for each turn-off device within the inverter. Each of the three sub-sections of the high-level SSSC controller is described in detail as follows.

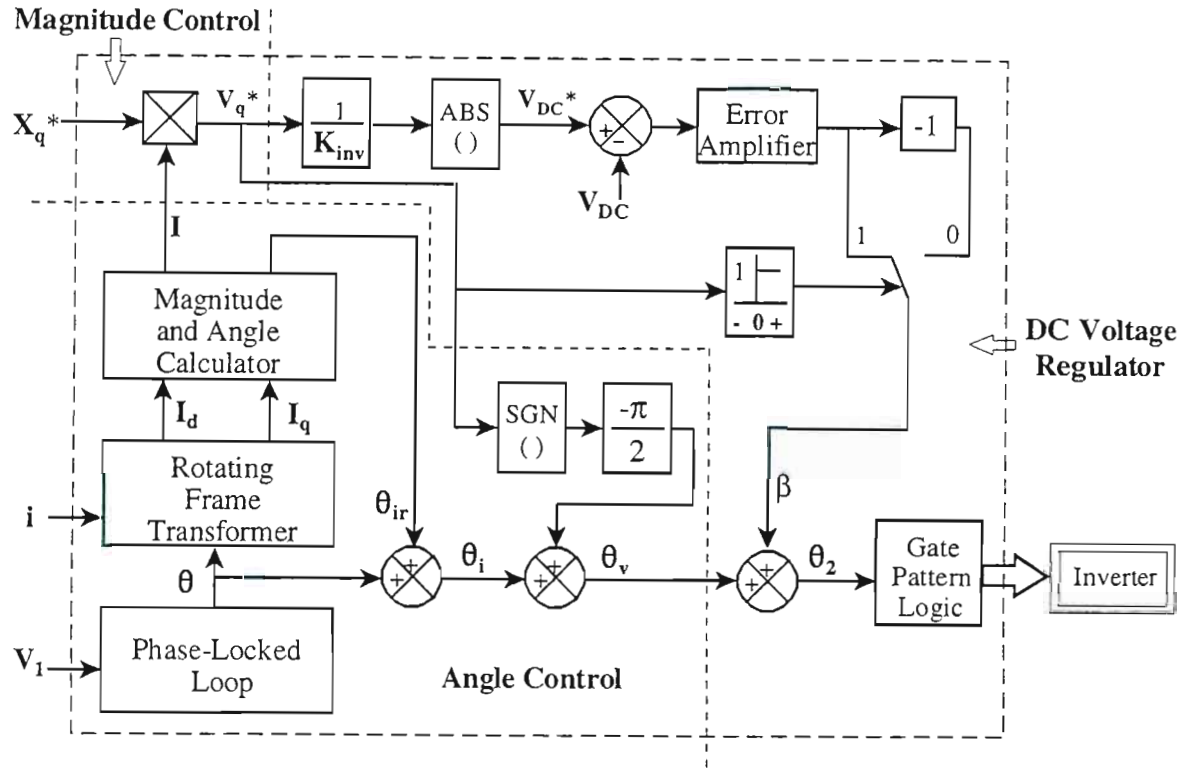


Fig.3.2: Control block diagram of a stand-alone two-level inverter based SSSC [34].

3.2.3.1 Angle Control Of Injected Voltage

The approach taken in [34] to ensure that V_q is inserted at the correct angle relative to I is to determine the exact angle θ_i of the transmission line current vector with respect to a synchronously rotating coordinate frame; the correct angle θ_v for quadrature of the injected voltage is then obtained by subtracting 90° from the angle of the current vector, i.e. $\theta_v = \theta_i - 90^\circ$. In the case of emulating an inductive reactance, the angle θ_v is calculated by adding 90° to the angle of the current vector, so that $\theta_v = \theta_i + 90^\circ$.

Phase Locking of the Injected Voltage Vector V_q

The synchronously rotating coordinate referred to above is established as follows, where the full theory is described in [22].

Firstly, the instantaneous phase-to-neutral voltages v_{1a} , v_{1b} , and v_{1c} at the SSSC bus (bus 1 in Fig. 3.1) are measured and converted to per unit. These instantaneous a , b , and c voltages are converted to their ds and qs components in a stationary d-q coordinate frame using the transformation matrix $[C]$ defined in [22] viz.:

$$\begin{bmatrix} v_{1ds} \\ v_{1qs} \\ 0 \end{bmatrix} = \underbrace{\frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}}_{[C]} \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} \quad (3.2)$$

Such that, in long hand, v_{1ds} and v_{1qs} can be written in the following expressions:

$$v_{1ds} = \frac{2}{3}v_{1a} - \frac{1}{3}v_{1b} - \frac{1}{3}v_{1c} \quad (3.3)$$

and

$$v_{1qs} = \frac{1}{\sqrt{3}}v_{1b} - \frac{1}{\sqrt{3}}v_{1c} \quad (3.4)$$

Equations (3.3) and (3.4) give the stationary d-q axis components of the instantaneous bus voltage v_1 in terms of its phase-to-neutral a-b-c components. Assuming

$$v_{1a} + v_{1b} + v_{1c} \equiv 0$$

such that

$$v_{1b} = -v_{1a} - v_{1c} \quad (3.5)$$

then Equations (3.3) and (3.4) reduce to

$$v_{lds} = v_{la} \quad (3.6)$$

$$v_{lqs} = -\frac{1}{\sqrt{3}}v_{la} - \frac{2}{\sqrt{3}}v_{lc} \quad (3.7)$$

Equations (3.6) and (3.7) give the stationary d-q axis components of v_l in terms of two phase-neutral voltage measurements (v_{la} and v_{lc}) at bus 1.

Next, it is desirable to find the components of v_l in a new d-q coordinate frame which

- (i.) rotates at exactly the system frequency (i.e. synchronously rotating) and;
- (ii.) is positioned such that there is no (zero) component of the voltage vector V_l along its q-axis.

The objective of finding such a coordinate frame is likewise twofold: firstly, the line current vector will always appear stationary in such a frame; secondly, the d-axis component of line current in such a frame is, by definition, the real (active) component of line current whilst the q-axis component of the line current in such a frame is, by definition, the reactive component of line current.

The instantaneous a-b-c values of the transmission line variables are transformed into the d and q coordinates of this synchronously rotating coordinate frame using the time-varying transformation matrix $[C_l]$ defined in [22] as

$$\begin{bmatrix} |v| \\ 0 \\ 0 \end{bmatrix} = \underbrace{\frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}}_{[C_l]} \begin{bmatrix} v_{la} \\ v_{lb} \\ v_{lc} \end{bmatrix} \quad (3.8)$$

where the instantaneous angle θ in matrix $[C_I]$ is defined as

$$\theta = \tan^{-1} \left(\frac{v_{qs}}{v_{ds}} \right) \quad (3.9)$$

where v_{ds} and v_{qs} are the instantaneous coordinates of the SSSC bus 1 voltage in the stationary d-q coordinate frame. In practice, in the SSSC controls, the angle θ is obtained from the output of a phase locked loop [22] rather than by using Equations (3.6), (3.7) and (3.9), since v_{ds} is zero twice per ac cycle, resulting in divide by zero errors twice per cycle. Also, the use of a phase locked loop to determine θ allows the controller to ride through temporary faults in the transmission

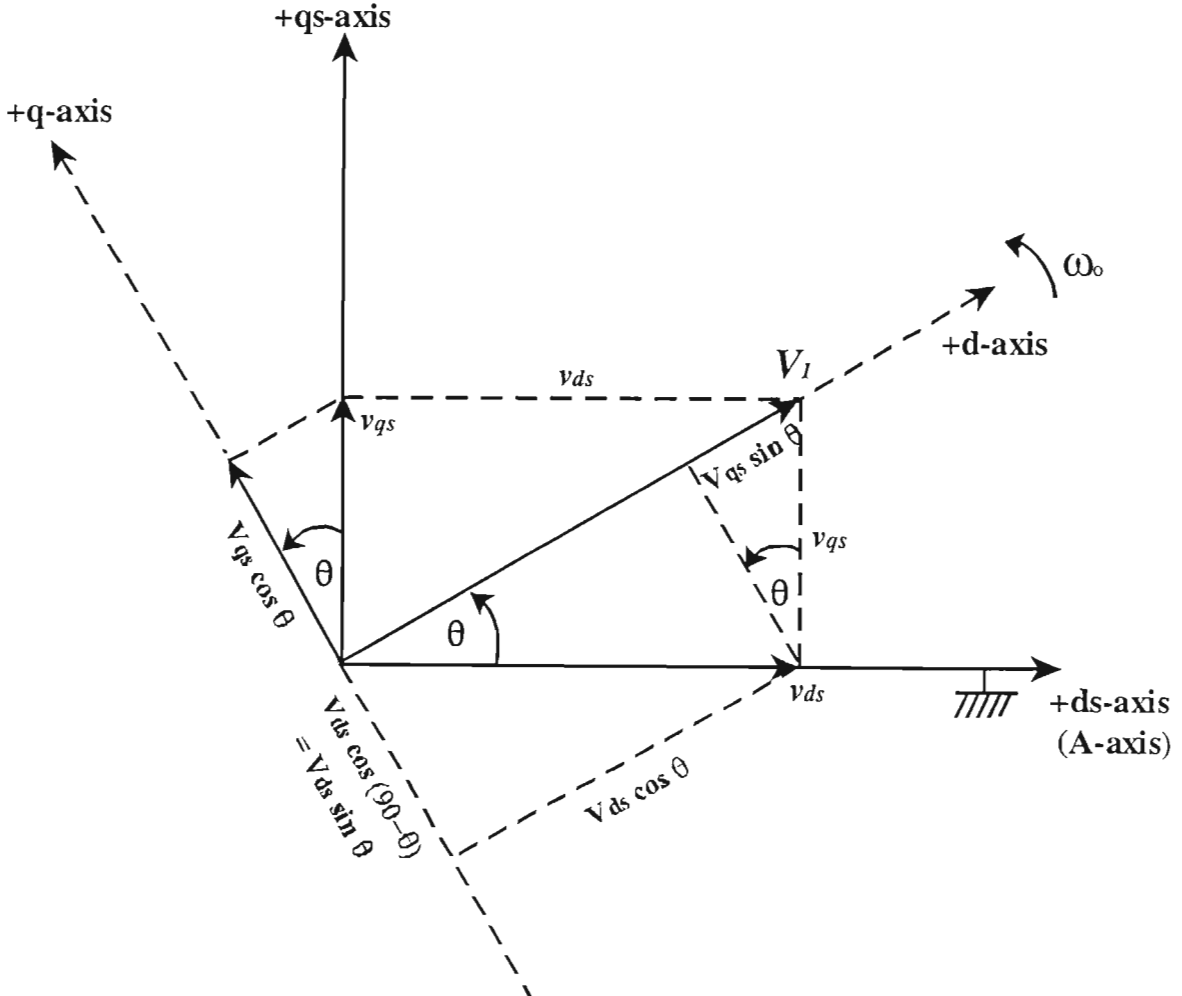


Fig.3.3: Relationship between the stationary (ds, qs) and synchronous (d,q) coordinate frames in the SSSC controller [22].

system. The manner in which the phase locked loop (PLL) determines the correct value of θ for the transformation in Equation (3.8) is explained shortly. However, for the time being, if one assumes that the PLL can drive θ to the correct value, then Fig. 3.3 shows the relationship between ds-qs and d-q coordinate frames.

In Fig. 3.3 the bus 1 voltage vector V_I rotates at the synchronous frequency, ω_o , and axes ds, qs are stationary; the components v_{Ids} and v_{Iqs} therefore vary sinusoidally with time. However, in the case of the d-q frame, the axes rotate at exactly the same frequency ω_o as does vector V_I (this is ensured by action of the phase locked loop as will be explained later.) Hence components v_{Id} and v_{Iq} are dc or “stationary” variables. From Fig. 3.3 and based on simple trigonometry, the synchronous frame components v_{Id} and v_{Iq} of vector V_I can be written in terms of its stationary frame components v_{Ids} and v_{Iqs} as:

$$v_{Id} = v_{Ids} \cos \theta + v_{Iqs} \sin \theta \quad (3.10)$$

and

$$v_{Iq} = v_{Iqs} \cos \theta - v_{Ids} \sin \theta \quad (3.11)$$

If the values of v_{Id} and v_{Iq} are obtained from the instantaneous a-b-c variables v_{Ia} , v_{Ib} and v_{Ic} using Equation (3.8), and θ is obtained from v_{Ids} and v_{Iqs} using Equations (3.6), (3.7) and (3.9), then the transformation matrix $[C_I]$ ensures that the d axis of the synchronous coordinate frame lies directly along the voltage vector V_I , so that V_I has no q-axis component in the synchronously rotating d-q coordinate frame. This observation is used to position the d-q axes using a phase locked loop within the SSSC controls as explained in the following sub-section.

The Phase Locked Loop (PLL)

Equations (3.10) and (3.11) have shown how v_{Id} and v_{Iq} can be obtained from v_{Ids} and v_{Iqs} if the correct transformation angle θ is known at every instant. In practice [22], the angle θ in the SSSC controls is obtained from the output of a phase locked loop. If the angle θ output by this PLL is incorrect, then the components v_{Id} and v_{Iq} of vector V_I in the synchronous coordinate frame will also be incorrect; in particular the component v_{Iq} will *not* be zero. Fig. 3.4 illustrates how this observation is used to synchronize the phase locked loop to ensure the correct value of θ is maintained. In the diagram, the correct value of the transformation angle (by definition the instantaneous angle between the +ds-axis and the vector V_I) is labelled θ^* whereas the actual angle output by the PLL is assumed to be some incorrect value θ . By using this PLL angle the d- and q-axes are incorrectly located, with the error in their angular position being given by $\theta_e = \theta^* -$

θ . Fig. 3.4 shows that this error in the positioning of the d- and q-axes results in a non-zero component of $v_{Iq} = |V_I| \sin \theta_e$. Therefore, instead of measuring the angle error θ_e itself and using it as the error input to a PLL to advance θ , this error θ_e is detected by v_{Iq} . For small values of error angle θ_e , $\sin \theta_e$ is approximately equal to θ_e and hence

$$v_{Iq} \approx |V_I| * \theta_e = \text{PLL}_{(\text{error})} \quad (3.12)$$

Equation (3.12) shows that the non-zero value of v_{Iq} obtained is a direct measurement of the error θ_e in the angle θ that was used to calculate v_{Id} and v_{Iq} in the first place (with a scale factor of $|V_I|$ between v_{Iq} and θ_e). Fig. 3.4 shows the situation for a positive error θ_e but it can just as easily be seen diagrammatically that Equation (3.12) holds for negative errors in θ where d-axis is ahead of vector V_I .

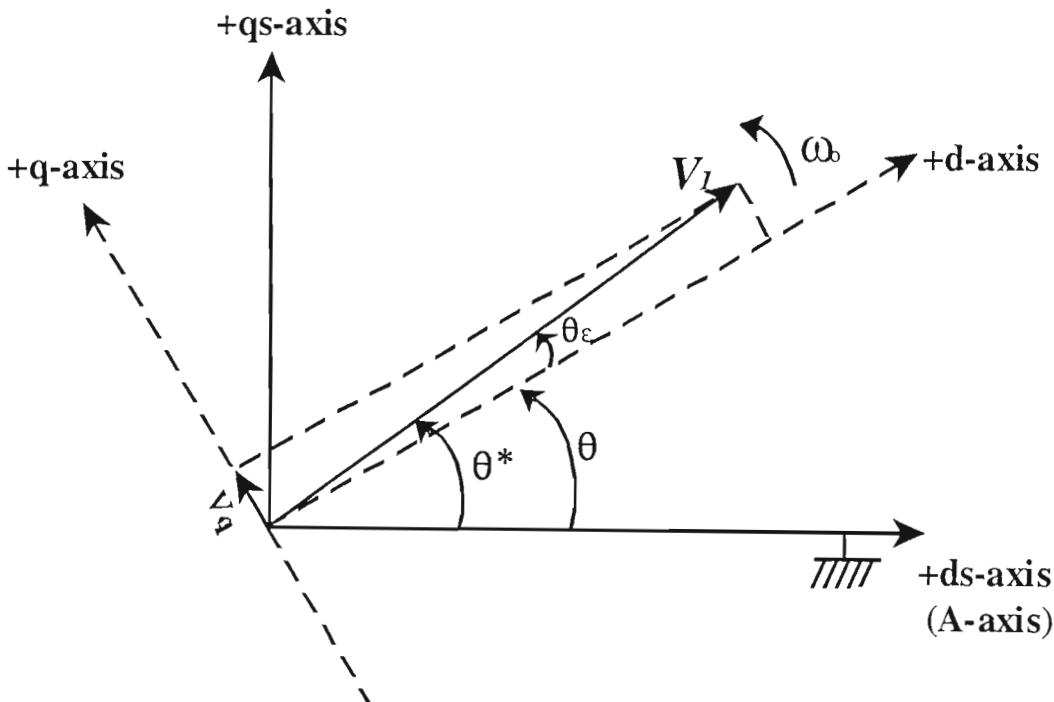


Fig.3.4: Example illustrating the d-axis not correctly aligned with the vector V_I .

In summary, if d-axis is ahead of vector V_I (i.e. the correct angle θ^* is smaller than the actual angle θ), θ_e is negative and v_{Iq} is negative; hence the $\text{PLL}_{(\text{error})}$ is negative. The $\text{PLL}_{(\text{error})}$ then drives the output of the PLL (i.e. θ itself) lower until θ is correct and θ_e and v_{Iq} become zero. On the other hand, if d-axis is behind vector V_I (i.e. the correct angle θ^* is larger than the actual angle

θ , like the example shown above), θ_e is positive and v_{Iq} is positive; hence the $PLL_{(error)}$ is positive. The $PLL_{(error)}$ then drives the PLL output angle θ higher until θ is correct and θ_e and v_{Iq} become zero.

Thus, with any “assumed” starting value for angle θ and a phase locked loop driven by whatever component of v_{Iq} arises, the angle θ at the output of the PLL will be driven to the correct value to hold $v_{Iq} = 0$ and hence the d-axis synchronous with, and aligned along vector V_I .

Line Current I in the d-q Frame

The Angle Control sub-section of the full SSSC control scheme shown in Fig. 3.2 is now shown in more detail in Fig. 3.5, based on the equations and explanations described above.

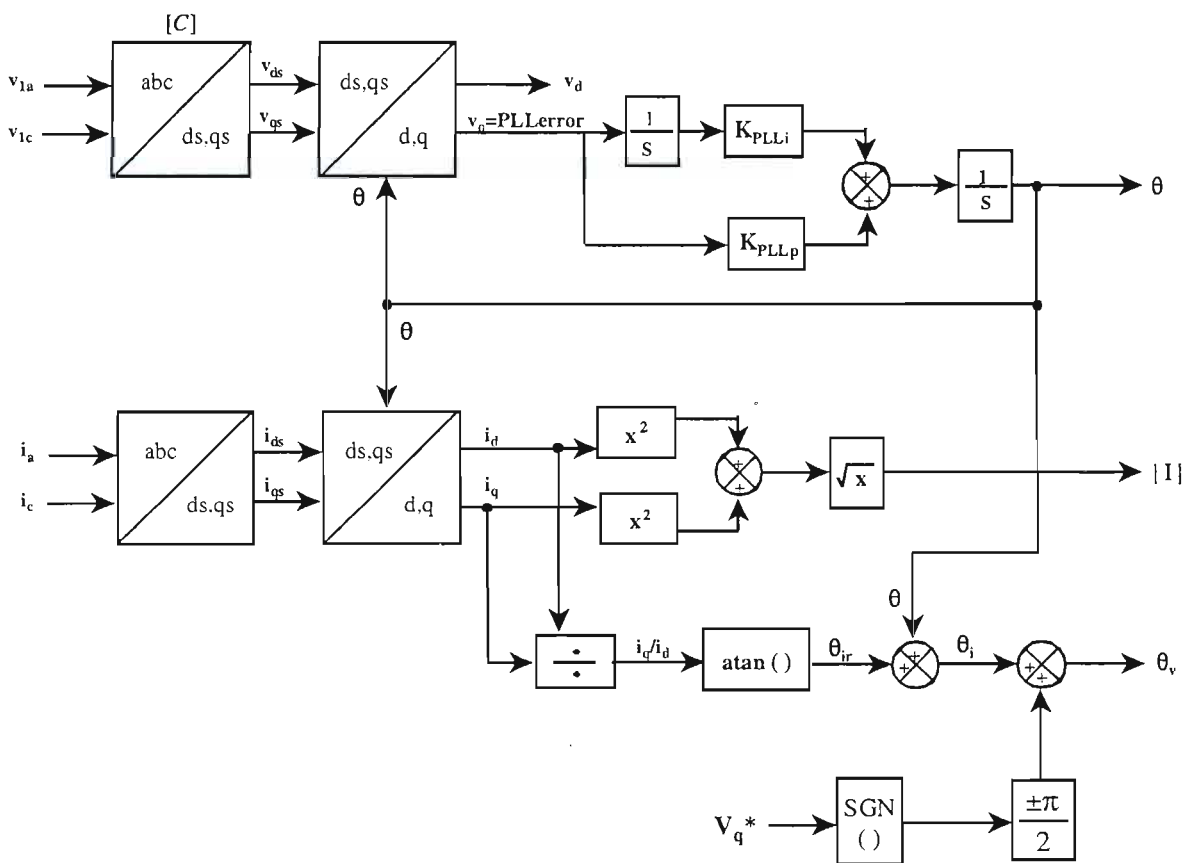


Fig.3.5: An expanded and detailed diagram of the Angle Control sub-section from Fig. 3.2 .

With the correct value of θ obtained from the above-mentioned phase locked loop, this angle and the same set of transforms is used to calculate the magnitude and the angle of the transmission

line current vector \mathbf{I} in the synchronous d-q frame using the instantaneous measurements of i_a and i_c such that

$$i_{ds} = i_a \quad (3.13)$$

$$i_{qs} = -\frac{1}{\sqrt{3}}i_a - \frac{2}{\sqrt{3}}i_c \quad (3.14)$$

and

$$i_d = i_{ds} \cos \theta + i_{qs} \sin \theta \quad (3.15)$$

$$i_q = i_{qs} \cos \theta - i_{ds} \sin \theta \quad (3.16)$$

From i_d and i_q , the magnitude of the transmission line current vector can be calculated:

$$|\mathbf{I}| = \sqrt{i_d^2 + i_q^2} \quad (3.17)$$

The angle θ_{ir} of this current vector relative to the synchronously rotating coordinate frame is then calculated as:

$$\theta_{ir} = \tan^{-1} \left(\frac{i_q}{i_d} \right) \quad (3.18)$$

and subsequently the actual angle θ_i of the line current vector in stationary coordinates, measured from the position of a space vector that lies along the phase a axis at time $t = 0$:

$$\theta_i = \theta_{ir} + \theta \quad (3.19)$$

Now the required angle θ_v of a voltage vector to be injected in series with the line is obtained such that this voltage vector will be exactly 90° ahead of or behind the line current vector, i.e.

$$\theta_v = \theta_i \pm 90^\circ \quad (3.20)$$

If 90° is subtracted from θ_i , the required angle θ_v of a voltage vector will be 90° behind the line current vector, i.e.

$$\theta_v = \theta_i - 90^\circ \quad (3.21)$$

which essentially means that the SSSC is emulating a capacitive reactance. Alternatively, if an inductive reactive voltage drop is desired, then 90° is added to θ_i , i.e.

$$\theta_v = \theta_i + 90^\circ \quad (3.22)$$

where the positive or the negative sign is decided by which mode (capacitive or inductive) the SSSC is required to operate in.

3.2.3.2 Amplitude Of The Compensating Voltage

The second requirement of the SSSC controller is such that the *amplitude* of the ac compensating voltage V_q^* required from the SSSC's inverter is determined by multiplying the magnitude of the line current vector I (as determined in the previous section) by the compensating reactance demand X_q^* in per unit, i.e.

$$V_q^* = |I| \times X_q^* \quad (3.23)$$

The sub-section of the full SSSC controller responsible for calculating the required magnitude of V_q^* is shown in the original control block diagram in Fig. 3.2. The required *sign* of V_q^* is determined from the sign of the compensating reactance demand, i.e. at the input to the SSSC controls, X_q^* is positive if the SSSC is to emulate a capacitive reactance and negative if the SSSC is to emulate an inductive reactance.

3.2.3.3 Inverter DC Voltage Regulator

The SSSC controller considered in this chapter assumes a fixed dc-to-ac gain across the inverter, so the demanded value of ac voltage V_q^* in turn determines (after accounting for the inverter's constant dc-to-ac gain K_{inv}) the demanded inverter dc voltage V_{dc}^* sent to the input of the voltage regulator. Even if the demanded value of the ac compensating voltage V_q^* did not change over time, due to the losses within the inverter and the transformers, the inverter dc voltage would gradually discharge if no energy were drawn from the transmission system, so a voltage regulator would still be required to main V_{dc} .

In order to charge and discharge the inverter dc capacitor as necessary, the voltage regulator must enable active energy (either positive or negative) to be exchanged with the transmission line. The regulator does this by moving the phase of the injected voltage V_q slightly away from perfect quadrature with the line current so that there is a small component of V_q in phase with I , and hence a small component of active power at the interface between the SSSC and the transmission line.

An expanded and detailed diagram of the DC Voltage Regulator sub-section of the SSSC controller in Fig. 3.2 is now shown in Fig. 3.6. In Fig. 3.6 the demanded value V_{dc}^* is compared to the actual dc voltage V_{dc} and the error is used to drive a PI controller. The output β^* from this PI controller determines the angular phase offset applied to the injected ac voltage v_q (away from quadrature). However the *sign* of the angle β required to generate the required active power at the ac terminals of the SSSC depends on the mode of operation (capacitive or inductive) of the SSSC (the reason for this is explained shortly). Thus the sign of β^* is altered according to the sign of X_q^* (which is positive for capacitive mode and negative for inductive mode) in order to yield the correct final phase offset β . This phase offset β is added to θ_v (the angle of v_q required for exact quadrature) to form the required angle θ_2 of the ac voltages at the output of the SSSC.

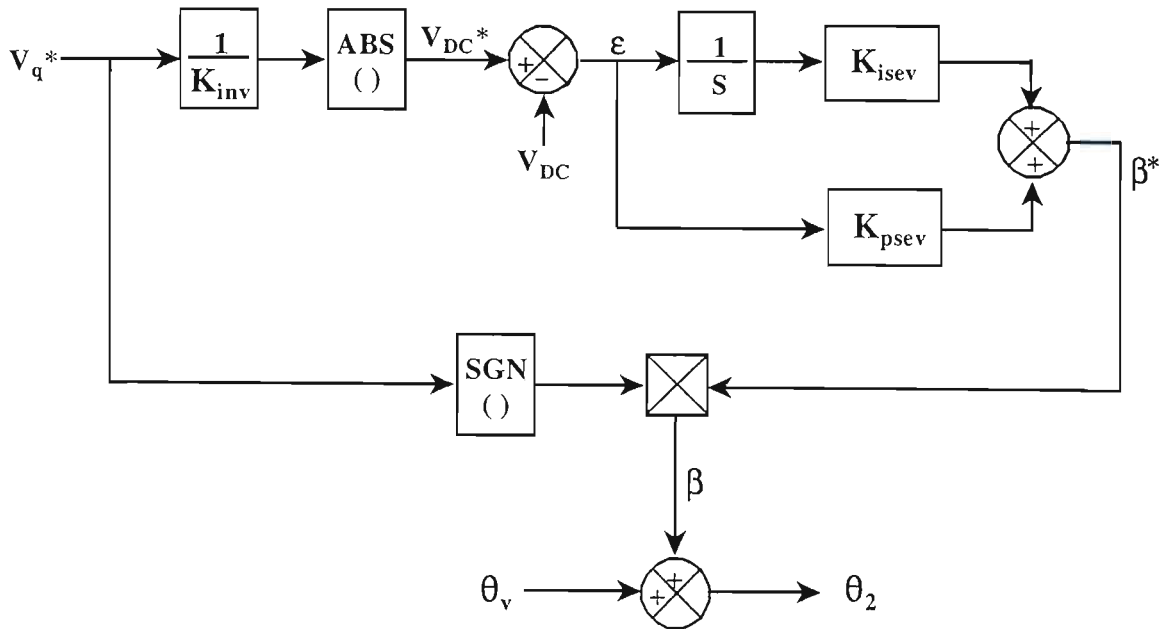


Fig.3.6: An Expanded and Detailed Diagram of DC Voltage Regulator sub-section from Fig. 3.2 .

The reason that the sign of β^* has to be changed from capacitive to inductive mode of SSSC operation can be explained as follows. Recall that in the control block diagram of Fig. 3.6 the final phase offset β is always added to the phase θ_v of v_q . Now consider the situation where the inverter dc voltage is too low (positive error ϵ) such that a positive component of the active power is required at the ac terminals of the SSSC. Fig. 3.7 illustrates that in capacitive mode of operation a positive value of β would need to be added to the quadrature phase angle of v_q whereas in inductive mode a positive value of β would need to be subtracted from the quadrature phase angle of v_q . Hence, for the same positive error ϵ in the dc voltage of the SSSC and hence a positive β^* at the output of the regulator, the actual value of required phase offset β to be added to the phase of v_q is positive for capacitive mode and negative for inductive mode. It can be shown that this correction of the phase offset to be added to the angle of v_q also holds for negative values of voltage regulator error ϵ . This concludes the description of the dc voltage regulator and the overall high-level SSSC control.

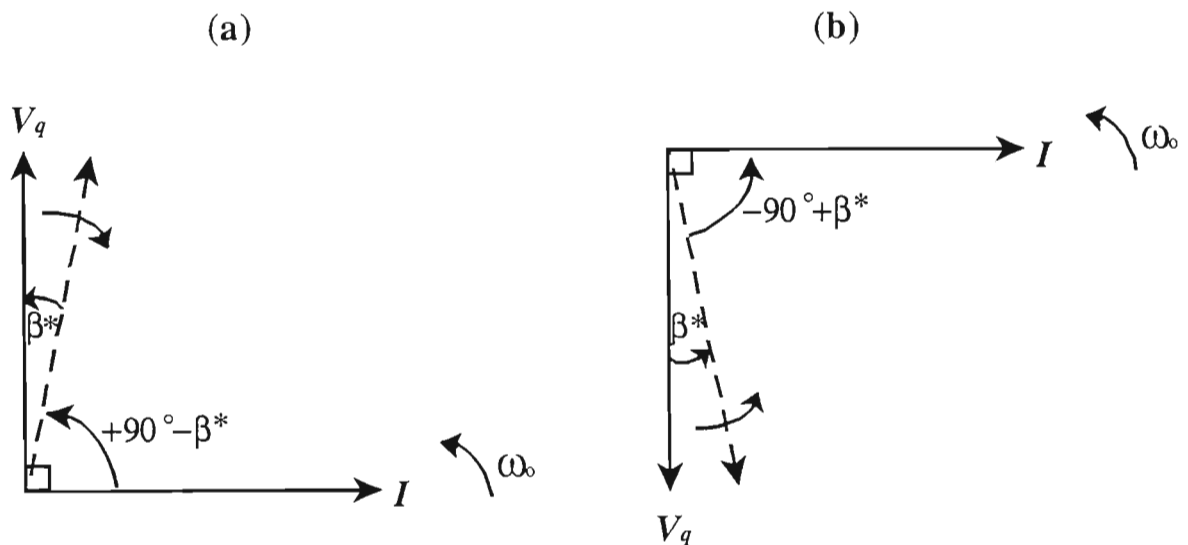


Fig.3.7: Desired position of SSSC's vector v_q to create positive active power at the ac terminals: (a) inductive mode;(b) capacitive mode.

3.3 Two-Level SSSC Simulation Model In PSCAD/EMTDC

A detailed simulation model of the two-level-inverter based SSSC described in the previous section has been developed in the simulation package PSCAD/EMTDC. This SSSC simulation model comprises four main sub-modules:

- (i.) the series compensated transmission line and the coupling transformers that are used to inject the ac compensating voltages from the SSSC onto the line;
- (ii.) the 24-pulse three-level inverter together with phase-shifting and adding transformers developed in Chapter Two (in this particular SSSC implementation the inverter is operated as a two-level device with γ fixed at 0°);
- (iii.) the high-level SSSC controls described in the previous section.
- (iv.) the low-level inverter firing controls situated between the output of the high-level SSSC controls and the inverter itself.

Although the high-level SSSC controller in this model is based on that in [34], the SSSC model here is more detailed than those in [27,34] since all the inverter's power electronics and firing controls are represented as well as the phase shifting and adding transformers actually present in a multi-pulse inverter arrangement. This PSCAD/EMTDC model has been used to simulate the dynamic performance of the SSSC in the same study system that was considered in reference [34]. The predictions of the PSCAD/EMTDC model are then directly compared to those of the EMTP model used by Sen in [34] (the details of Sen's EMTP code was provided as an appendix in [34] and this code has been used to reproduce Sen's results in the EMTP program). The parameters for the transmission line system, transformers, inverter dc-to-ac gain and dc link voltages, PI controller gains etc. are taken from [34] and listed in Appendix B.1. The full details of the SSSC simulation model with all its components in PSCAD/EMTDC are shown in Appendix B.2.

The following section compares some of the SSSC time domain results produced by the PSCAD/EMTDC model developed in this thesis with the results from the EMTP model in [34].

3.4 Two-Level SSSC Benchmark Results

The PSCAD/EMTDC simulation model of the SSSC described above has been used to recreate the results presented in [34]. The left hand side of Fig. 3.8 shows the dynamic response of the SSSC to changes in commanded compensating reactance X_q^* as simulated using the EMTP model of Sen [34], whereas the right hand side of Fig. 3.8 shows the simulated results of the SSSC to the same changes in X_q^* using the detailed PSCAD/EMTDC model presented in this chapter. In each case the sending and receiving end voltages in the transmission line are kept at constant magnitude and the transmission angle (phase between V_s and V_r) remains fixed. The SSSC is then used to alter the magnitude of the line current (and hence the active and reactive power transfer down the line) by changing the commanded compensating reactance (both the size and nature – inductive or capacitive – of X_q^*).

At time $t = 0$ in Fig. 3.8, $X_q^* = 0$ and the inverter injects zero volts into the line, with its dc capacitor voltage, V_{DC} , likewise zero; the transmission line is thus operating with no series reactive compensation. At $t = 50\text{ms}$, the desired reactance X_q^* is stepped up to 0.15 pu inductive (i.e. $X_q^* = -0.15$). Immediately, the line current i_a and both the active (P_q) and reactive (Q_q) powers at the receiving end decrease because of the increased net reactance between the sending and receiving ends of the transmission line. The inverter output voltage, e_{2a} , of phase a leads the line current, i_a , by almost 90° , and therefore mimics the desired inductive characteristic. When X_q^* is increased to 0.3 pu inductive at $t = 175\text{ms}$, the magnitudes of inverter dc voltage and ac injected voltage increase accordingly. However, the magnitude of the line current, i_a , and the receiving end powers P_q and Q_q decrease even more due to the further increase in net inductive reactance of the line.

At $t = 300\text{ ms}$, the commanded reactance X_q^* is step-changed to 0.1 pu capacitive (i.e. $X_q^* = +0.1$). The net reactance of the line is now lower than its uncompensated value and therefore the line current, active power and reactive power increase; the inverter output voltage, e_{2a} , of phase a now lags the line current, i_a , by almost 90° . Both the dc voltage and the injected ac voltage magnitudes decrease with the reduced magnitude of X_q^* . When X_q^* is increased to 0.15 pu capacitive at $t = 450\text{ms}$, the inverter dc voltage, the injected ac voltage, line current and the power flow in the transmission line all increase in magnitude due to this higher degree of compensation.

Fig. 3.9 shows the current i_a and the inverter output voltage e_{2a} from time $t = 250\text{ms}$ to $t = 350\text{ms}$. During this time period (specifically at time $t = 300\text{ms}$) the commanded reactance is changed from inductive to capacitive. Fig. 3.9 shows the rapid change in the phase of the compensating voltage e_{2a} relative to the line current i_a : when the commanded reactance is inductive, the inverter

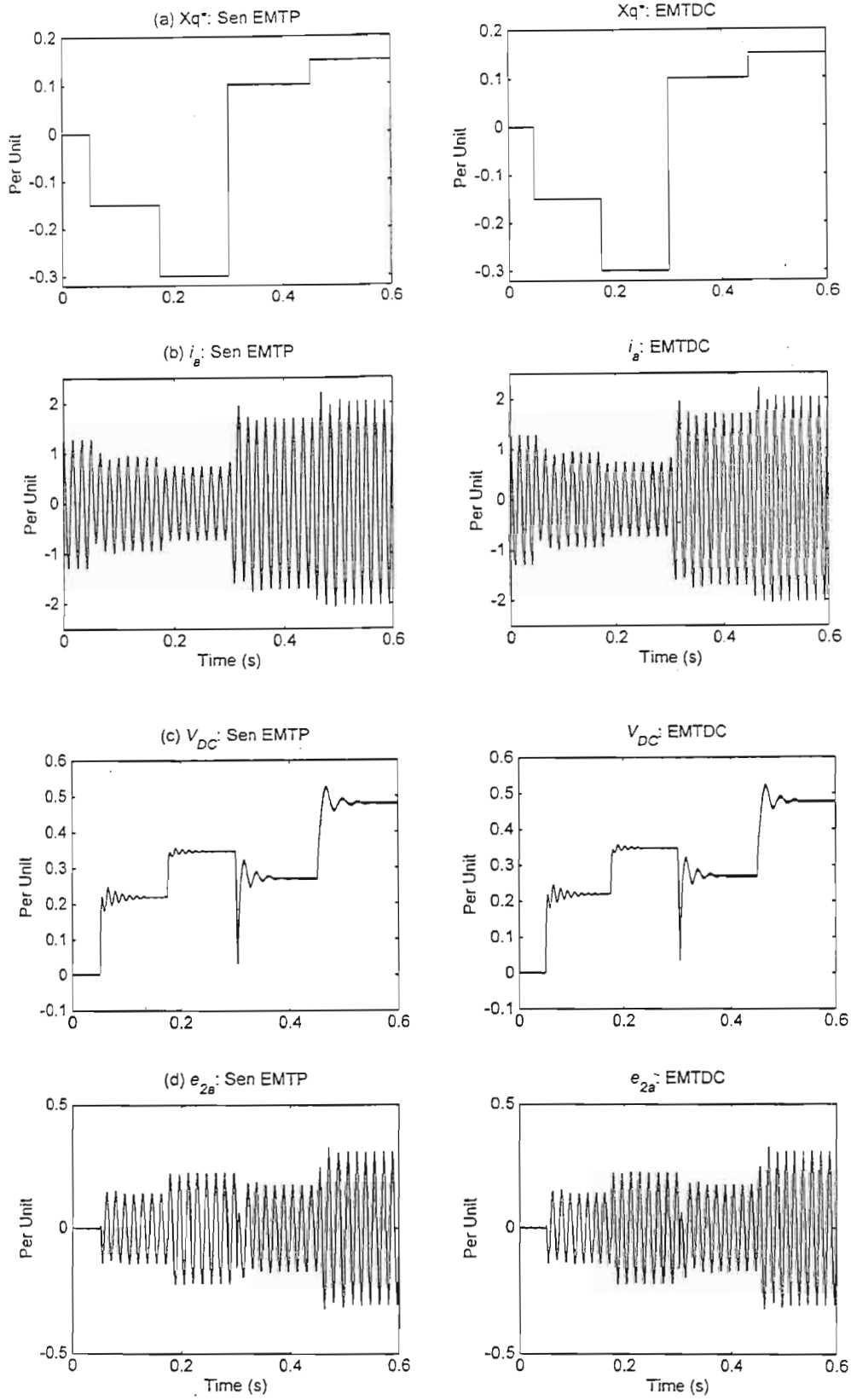


Fig.3.8: Performance of an SSSC with a 24-Pulse Two-Level Inverter Operating in Inductive and Capacitive Modes, as modelled in EMTP [34] and PSCAD/EMTDC: (a) X_q^ ; (b) i_g ; (c) V_{DC} ; (d) e_{2a} .*

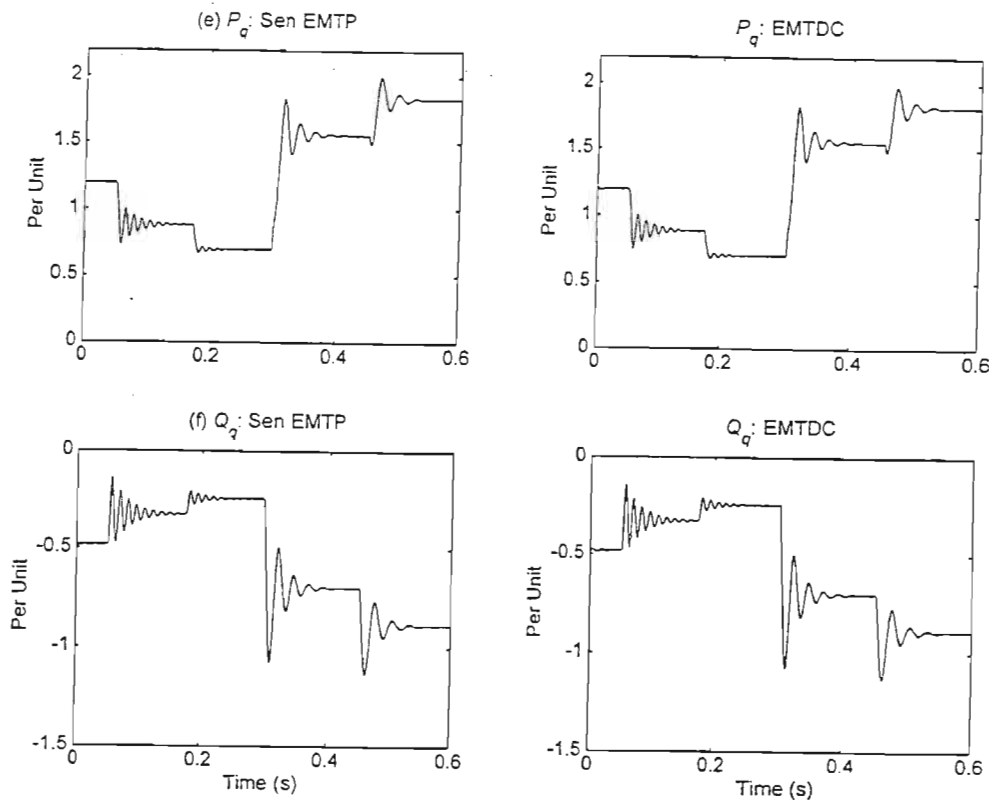


Fig.3.8 (continued): Performance of an SSSC with a 24-Pulse Two-Level Inverter Operating in Inductive and Capacitive Modes, as modelled in EMTP [34] and PSCAD/EMTDC: (e) P_q ; (f) Q_q .

output voltage, e_{2a} , of phase a leads the line current, i_a , by almost 90° . On the other hand, when the commanded reactance is capacitive, the inverter output voltage, e_{2a} , of phase a lags the line current, i_a , by almost 90° . This illustrates the correctness of the control scheme where it is able to differentiate between the capacitive and the inductive reactance demand, thus subtract or add 90° to the current vector and therefore output the correct phase.

A close comparison between the results in Fig. 3.8 has shown that the response predicted by Sen's EMTP model in [34] and that predicted by the detailed PSCAD/EMTDC model of this thesis are virtually identical, thus confirming the correctness of the latter model. Fig. 3.10 illustrates this close agreement for one particular system variable: the transmission line current i_a predicted by each of the models is plotted on the same axes in Fig. 3.10 for comparison.

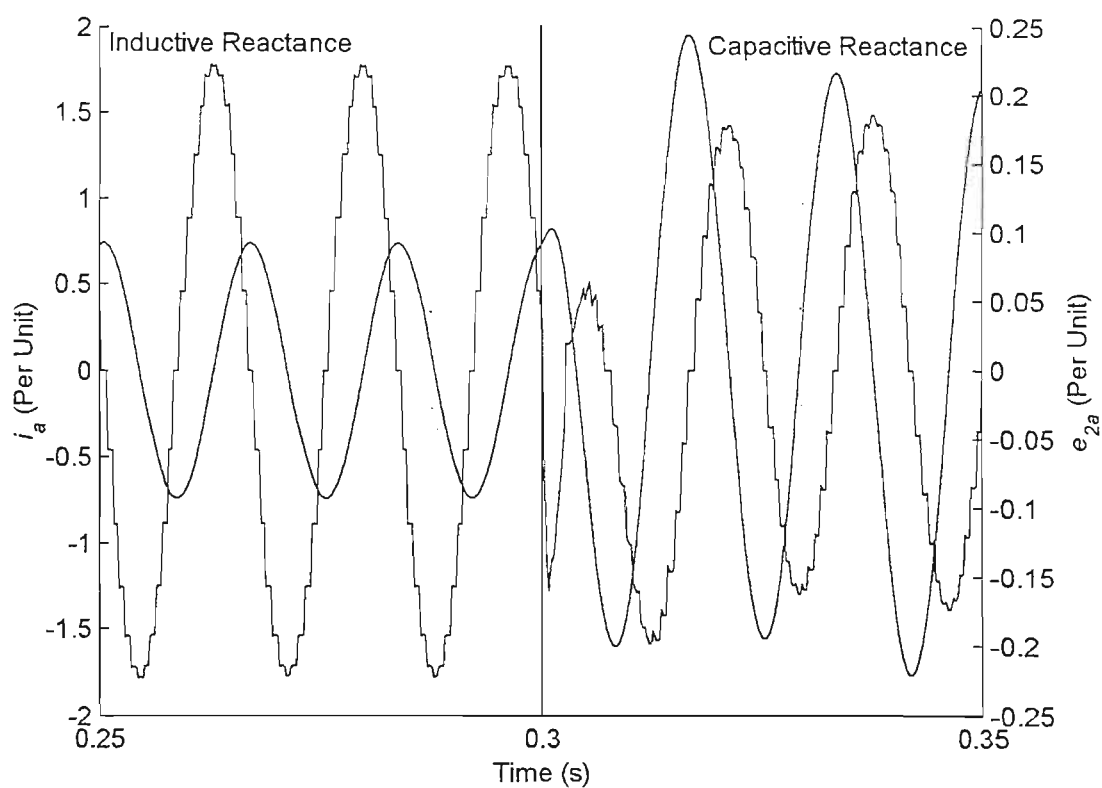


Fig.3.9: Phase relationship between the line current i_a and the inverter output voltage e_{2a} .

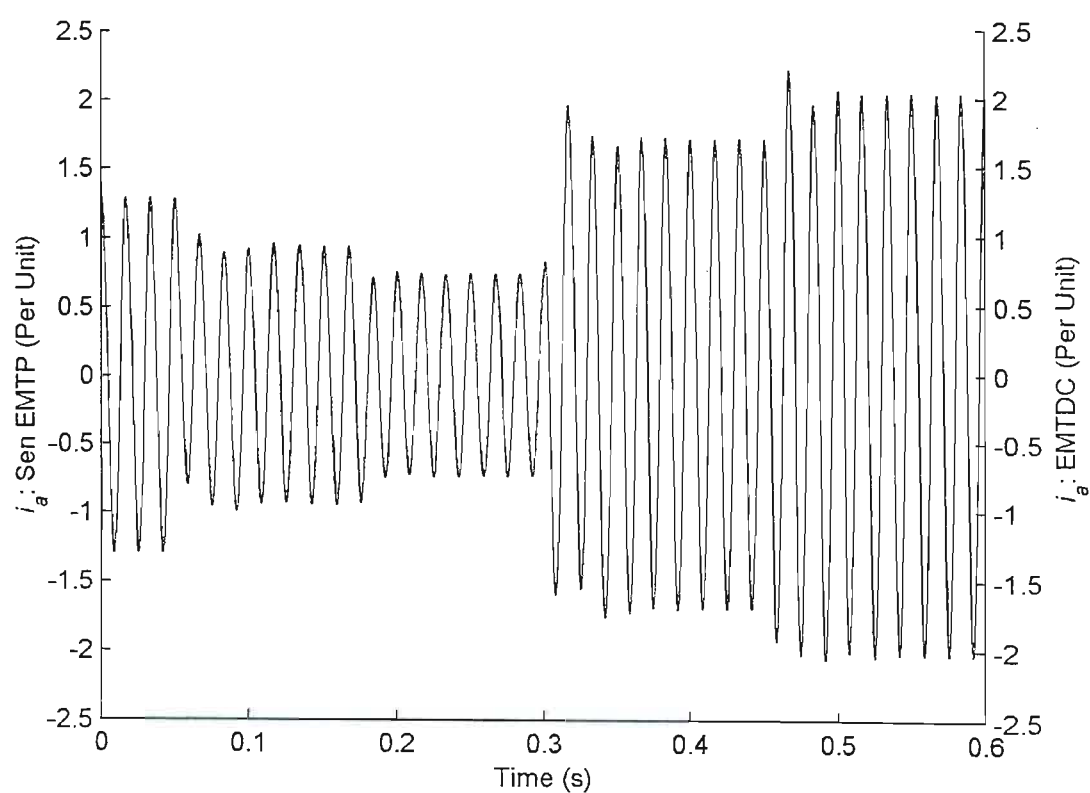


Fig.3.10: The line current, i_a : EMTP [34] vs. PSCAD/EMTDC.

3.5 The 24-Pulse Three-Level Inverter Based SSSC

3.5.1 Introduction

As previously mentioned, an SSSC can be operated either as a stand-alone device or as part of a UPFC where the SSSC is combined with a STATCOM. Since the SSSC has no control over the dc link capacitor voltage when operated as a part of the UPFC, a different type of control needs to be implemented in order for the SSSC to supply the required variable ac output voltage and function satisfactorily. In addition to a different high-level controller, a three-level inverter is required in order to achieve this mode of operation. As Chapter Two explained, by varying the width of each turn-off device's on-pulse, a three-level inverter's dc-to-ac gain is changed and therefore the output ac voltage amplitude can be controlled independently of the inverter dc voltage.

Among the papers that have considered variable dc to ac gain converters and modelled the actual power electronics, some have considered their application to the advanced static VAR compensator (ASVC) or STATCOM [23,24,25], and some have considered their application to the SSSC, but along with the method of pulse width modulation [42,43]. Reference [27] by Sen *et al.*, however, did model a 24-pulse three-level inverter-based SSSC as a part of an UPFC, but did not represent the actual power electronic switches and the associated low-level switching control scheme in the simulation model. In addition, although the SSSC model in [27] is for a three-level inverter, it needs to be adapted to allow operation of the SSSC as a stand alone three-level device since when an SSSC is part of a UPFC (as in [27]) it is not required to maintain its own dc voltage – rather, this is done by STATCOM.

This section of the chapter now presents an adaptation of the three-level SSSC model described in [27] and the two-level SSSC model described in [34] to develop a control scheme for a stand alone three-level SSSC that can operate with a fixed dc voltage, thus exploiting the full flexibility of a three-level inverter. Such a control scheme could be of use when operating just the SSSC module of a full UPFC on its own which is sometimes the case [15,53], although it would also be possible to operate such an SSSC by reverting to the two-level controls described in the first part of the chapter. However, as described later in the thesis, the flexibility of the three-level stand alone SSSC can be exploited for supplementary damping control applications whereas the two-level SSSC is not as suited to such applications.

When simulating and testing the three-level stand alone SSSC in the remainder of this chapter, the layout of the SSSC and the transmission system remains the same as that shown in Fig. 3.1. The

system structure and parameters, with the exception of some aspects of the SSSC high-level controller are the same as those in [34] in order to demonstrate the correctness of the SSSC model later in the chapter. The following section describes the modified control scheme for the three-level stand alone SSSC used to vary the inverter's ac output voltages to meet the commanded compensating reactance by adjusting the dead angle, γ .

3.5.2 Stand-Alone Three-Level SSSC Controller

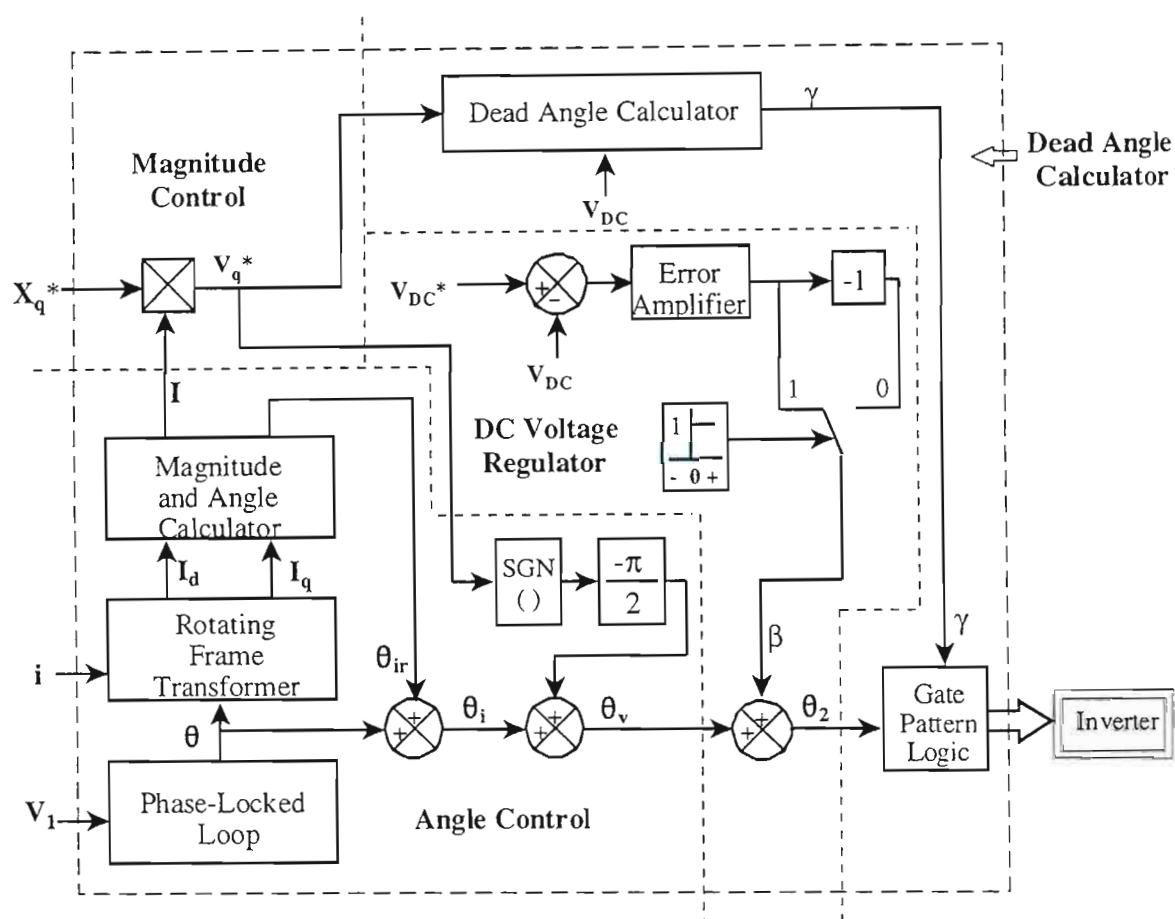


Fig.3.11: Control block diagram of a stand-alone three-level inverter-based SSSC.

Fig. 3.11 shows the high-level control block diagram of the stand-alone three-level inverter-based SSSC developed for this thesis, where the ac output voltage from the SSSC is varied by controlling the inverter's dc-to-ac gain. The diagram is once again broken down into three sub-sections according to the three control requirements of the SSSC. The synchronization of the SSSC to the bus 1 voltage and the calculation of the desired angle θ_v of the injected voltages for exact quadrature (the section labelled Angle Control in Fig. 3.11) is the same as in the

two-level SSSC controller in section 3.2. However, the subsections of the controller responsible for magnitude control and dc voltage regulation are now modified from those in the two-level SSSC controller, as explained shortly. As in the two-level SSSC controller, the final output of the high-level controls is the angle sent to the inverter's low-level firing controls, which determine the firing signals for each turn-off device within the inverter. The specific implementations of the magnitude control and dc voltage regulator in the stand-alone three-level SSSC are now explained in more detail.

3.5.2.1 Magnitude Of The Desired DC Voltage

The first important change to the dc voltage regulator from the two-level SSSC in section 3.2 is the input to the voltage regulator: in the three-level, stand-alone SSSC the desired value of the dc voltage is set by the reference input V_{dc}^* which is no longer a function of the desired ac compensating voltage V_q^* . The value of this reference input is determined by the operator and can be adjusted from time to time to suit the operating conditions in the transmission system. Despite this change in the way its input is determined, the operation of the regulator itself remains the same: any error between V_{dc}^* and V_{dc} is passed through the error amplifier (PI controller) to determine the offset angle β to be added or subtracted from the angle of the injected voltages as needed to charge or discharge V_{dc} under capacitive or inductive mode.

Although the reference value of the inverter dc voltage in this three-level stand-alone SSSC is now decoupled from the commanded value of ac compensating voltage V_q^* in the controller, its value cannot be chosen *completely* independently of V_q^* . Recall that for a given dc voltage there is a maximum ac output voltage in a three-level inverter. The magnitude of the ac compensating voltage V_q^* required at the output of the inverter will vary depending on the range of desired magnitude of reactance X_q^* and the magnitude of the current I flowing in the transmission line. Therefore for a given value of X_q^* the dc voltage needs to be sufficient to supply the required V_q^* at the largest value of line current envisaged. In practice, there is a maximum rating of V_{dc} (based on the two physical dc capacitors used in the inverter) and of V_q^* (based on the rating of the injecting transformers). Therefore, there would be a maximum value of V_{dc} that the controller can ask for based on the actual ratings of the equipment used in practice (for both types of stand-alone SSSC: two-level and three-level.)

Recall also (as discussed in Chapter Two) that at low values of ac compensating voltage (relative to the dc voltage), the dead angle γ is closer to 90° and the amplitudes of harmonics increase. Hence as ac conditions in the line change, the value of V_{dc}^* may have to be increased in order to

accommodate larger commanded values of V_q^* or decreased to improve the harmonic performance at lower commanded values of V_q^* . Once V_{dc}^* is so set, V_q^* can then vary independently of the inverter dc voltage provided the angle γ remains in the range $0^\circ \leq \gamma \leq 90^\circ$.

In the stand-alone three-level SSSC, it is therefore crucial that the operator has some idea about the desired range of compensating reactance and the transmission line current in order to appropriately select the necessary magnitude of dc capacitor voltage within the inverter.

3.5.2.2 Magnitude Control

With respect to the desired ac compensating voltage V_q^* , the control objectives in the three-level SSSC are the same as in the two-level SSSC described in section 3.2, and hence V_q^* is calculated in the same way i.e. $|V_q^*| = |I| \times X_q^*$. However, now that the magnitude of the SSSC output voltage is varied using the dead-angle of the inverter, an extra stage in the magnitude controls is required to determine the correct value of γ based on the desired value of V_q^* and the actual value of the inverter's dc voltage (as determined by the set point V_{dc}^*).

The relationship between the magnitude of the compensating voltage vector and the dead angle, γ , for a 24-pulse three-level inverter is defined [27] as

$$V_q = \frac{2}{\pi} v_{DC} \cos\left(\frac{\pi}{24}\right) \cos \gamma \quad (3.24)$$

Since the desired output is the dead angle, by changing the subject of the formula, Equation (3.24) becomes

$$\gamma = \cos^{-1} \left(\frac{V_q \pi}{2v_{DC} \cos\left(\frac{\pi}{24}\right)} \right) \quad (3.25)$$

Therefore, depending on the desired inverter ac voltage output (i.e. the commanded value of V_q^*) and the actual value of V_{dc} , the controller will determine the correct value of γ based on Equation (3.25). This calculation of γ from V_q^* and V_{dc} using Equation (3.25) is shown as the Dead Angle Calculator block in Fig. 3.11, although the value of V_{dc} used in the calculation is not shown explicitly in Fig. 3.11.

In the two-level SSSC controller described in section 3.2, the final angle sent to the low-level firing controls is $\theta_v + \beta = \theta_2$. This angle θ_2 is the phase angle of the system-frequency ac voltages that will appear at the output of the inverter; this phase angle θ_2 of the system-frequency ac voltages is also an output of the stand-alone three-level SSSC as shown in Fig. 3.11. However, in the three-level SSSC the required dead angle γ for the inverter is an additional output to the low-level firing controls. (In the SSSC controls of section 3.2, γ is not an output of the SSSC controller since the SSSC controls are intended for a two-level inverter in which there is no capability for dead angle control.)

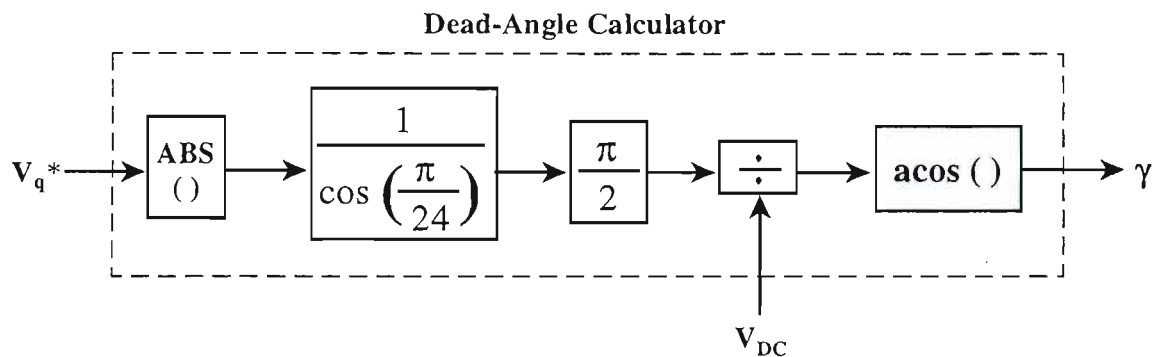


Fig.3.12: An Expanded and Detailed Diagram of Dead Angle Calculator sub-block from Fig. 3.11.

3.6 Benchmark Results For The Stand-alone Three-Level SSSC In PSCAD/EMTDC

A detailed simulation model of the stand-alone three-level SSSC has been developed in the simulation package PSCAD/EMTDC, including the detailed model of the three-level inverter itself that was described in Chapter Two.

In this section, in order to ensure the correctness of the PSCAD/EMTDC model, the performance of the stand-alone three-level SSSC for dynamic changes in X_q^* is benchmarked against the performance of the two-level SSSC in EMTD for the same changes in X_q^* , where the same system and X_q^* values are used as those considered in section 3.2. The dc capacitor voltage is chosen to be 60kV for this particular study, which is sufficient for the maximum compensating voltage required when the size of the capacitive reactance X_q^* is 0.15 pu (the maximum value of X_q^* considered in this study).

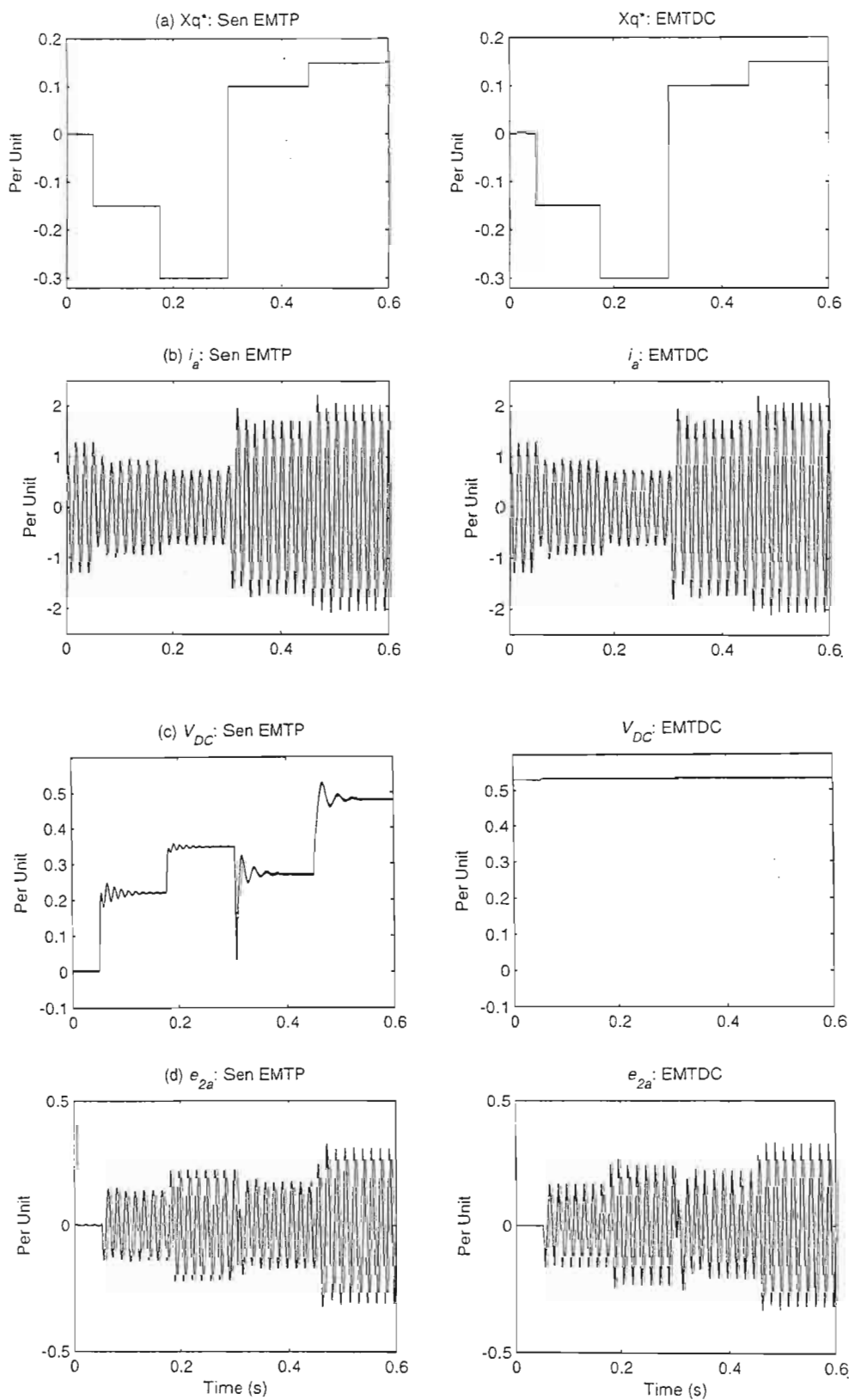


Fig.3.13: Performance of a two-level SSSC as modelled in EMTP [34] and a stand-alone three-level SSSC as modelled in PSCAD/EMTDC: (a) X_q^ ; (b) i_a ; (c) V_{DC} ; (d) e_{2a} .*

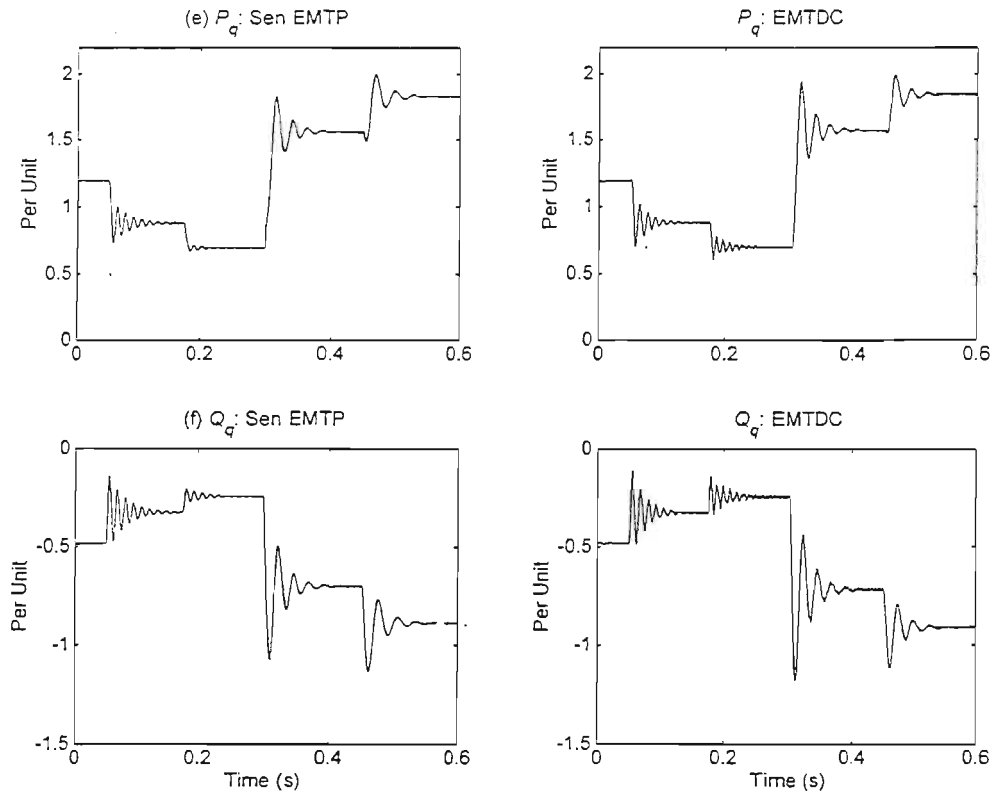


Fig.3.13 (continued): Performance of a two-level SSSC as modelled in EMTP [34] and a stand-alone three-level SSSC as modelled in PSCAD/EMTDC: (e) P_q ; (f) Q_q .

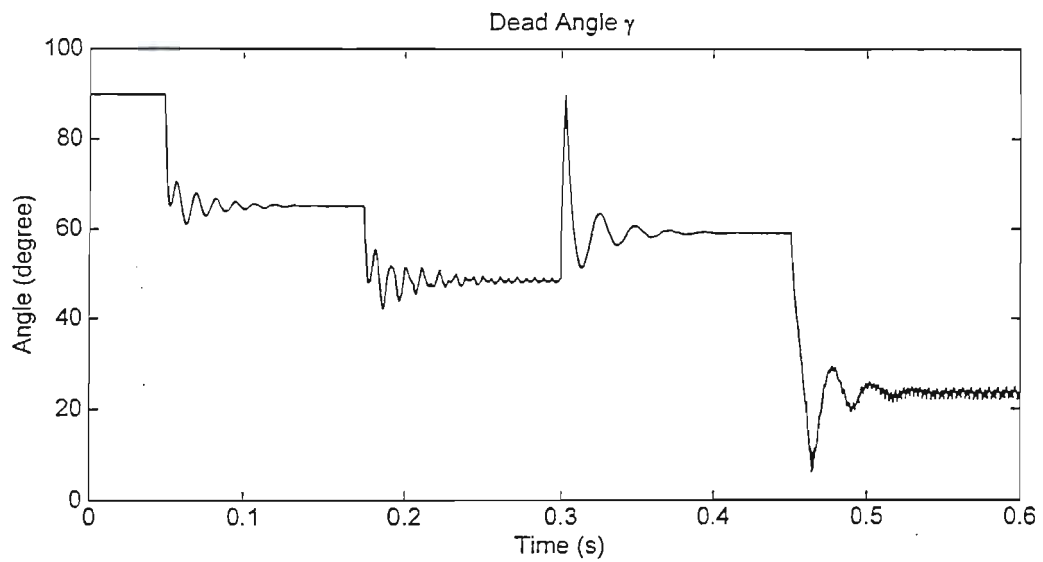


Fig.3.14: Variation of the dead angle γ in the stand-alone three-level SSSC as modelled in PSCAD/EMTDC.

The left hand side of Fig. 3.13 shows the dynamic response of the two-level SSSC to changes in commanded compensating reactance X_q^* as simulated using the EMTP model of Sen [34], whereas the right hand side of Fig. 3.13 shows the simulated results of the stand-alone three-level SSSC to the same changes in X_q^* using the detailed PSCAD/EMTDC model presented in this chapter. As in section 3.2, in each case the sending and receiving end voltages in the transmission line are kept at constant magnitude and the transmission angle (phase between V_s and V_r) remains fixed. The SSSC is then used to alter the magnitude of the line current by changing both the size and nature of the commanded compensating reactance.

At time $t = 0$ in Fig. 3.13, $X_q^* = 0$ and the inverter injects zero volts into the line, with its dc capacitor voltage, V_{DC} , likewise zero in the case of the two-level SSSC considered by Sen (left-hand side of Fig. 3.13(c)). On the other hand, the dc voltage is set at 60kV (0.53 pu) for the γ -controlled SSSC shown on the right-hand side of Fig. 3.13(c) throughout the entire analysis. Because of this non-zero dc voltage, the dead angle γ is adjusted to 90° (i.e. zero on-pulse for the turn-off devices in the inverter), in order to achieve zero ac output voltage in the case of the γ -controlled SSSC when $X_q^* = 0$. The transmission line is thus initially operating with no series reactive compensation in the case of both SSSC models in Fig. 3.13. (Fig. 3.14 shows the value of γ in the three-level SSSC at each stage during the transient response shown in Fig. 3.13.)

At $t = 50\text{ms}$, the desired reactance X_q^* is stepped up to 0.15 pu inductive (i.e. $X_q^* = -0.15$). Immediately, the line current i_a and both the active (P_q) and reactive (Q_q) powers at the receiving end decrease because of the increase in net reactance between the sending and receiving ends of the transmission line. The inverter output voltage, e_{2a} , of phase a leads the line current, i_a , by almost 90° , and therefore mimics the desired inductive characteristic. When X_q^* is increased to 0.3 pu inductive at $t = 175\text{ms}$, the magnitudes of inverter dc voltage and ac injected voltage increase accordingly in the case of the two-level SSSC. For the three-level SSSC, γ decreases from 65.2° to approximately 48.5° thus increasing the width of the on-pulse of each turn-off device and therefore increasing the fundamental magnitude of the compensating voltage.

At $t = 300\text{ ms}$, the commanded reactance X_q^* is step-changed to 0.1 pu capacitive (i.e. $X_q^* = +0.1$). Due to this step change from a negative to a positive value, X_q^* momentarily passes through zero which results in γ shooting up to almost 90° then settling to approximately 59° . The net reactance of the line is now lower than its uncompensated value and therefore the line current, active power and reactive power increase; the inverter output voltage, e_{2a} , of phase a now lags the line current, i_a , by almost 90° . The injected ac voltage magnitude decreases with the reduced magnitude of X_q^* . When X_q^* is increased to 0.15 pu capacitive at $t = 450\text{ms}$, the injected ac

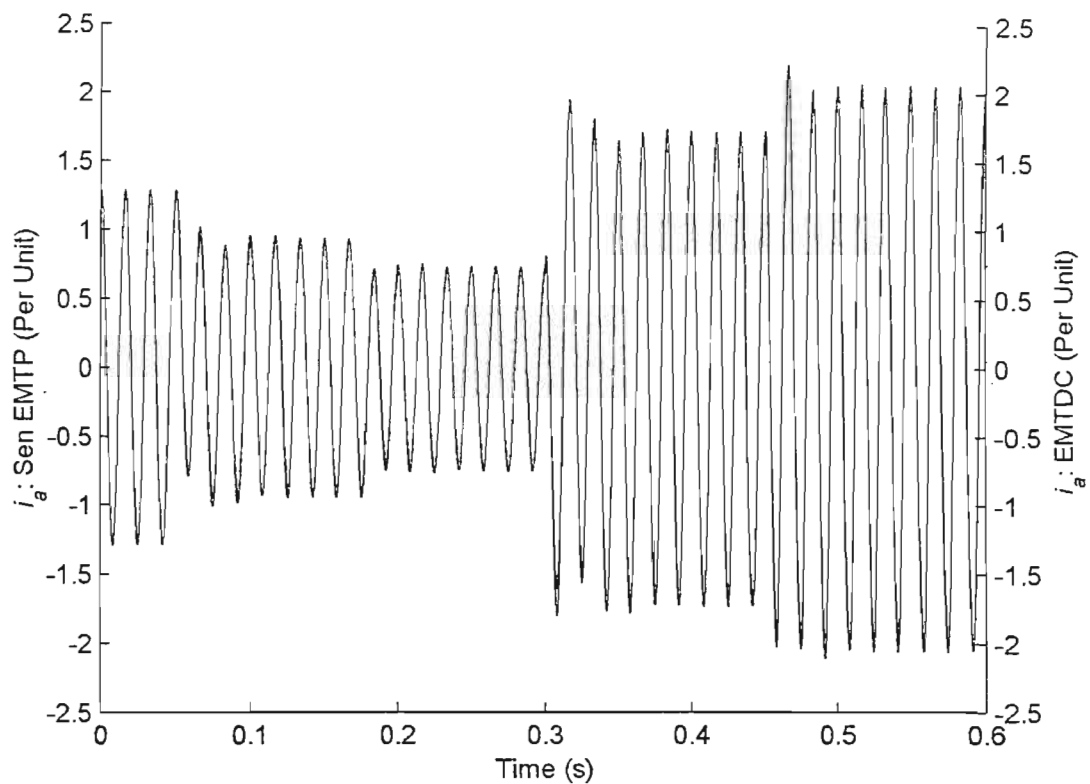


Fig.3.15: The line current, i_a : two-level SSSC in EMTP [34] vs. three-level SSSC in PSCAD/EMTDC.

voltage, line current and the power flow in the transmission line all increase in magnitude due to this higher degree of compensation.

In the simulation results shown in Fig. 3.13, both forms of compensator (three-level and two-level SSSC) are commanded to provide the same dynamically-varying compensating reactance to the same transmission system. Thus, despite the differences in internal control approach in the two SSSCs, the ac performance in the line should be the same in each case. One transmission variable, the line current i_a , is chosen to demonstrate this. Fig. 3.15 shows this same variable from the three-level SSSC case and the two-level SSSC case plotted on the same axes. Fig. 3.15 confirms that the steady state and dynamic performance of the ac line variables is virtually identical as the two forms of SSSC compensation are used to vary the effective reactance of the line.

Recall that in the case of the two-level SSSC, there is no change in the dead angle of the inverter, so the variable magnitude of ac compensating voltage is achieved by varying the dc voltage of the inverter. However, in the case of the three-level SSSC, the inverter dc voltage V_{dc} is fixed at 60kV (0.53 pu) and the dead angle γ is varied to change the magnitude of the ac compensating voltages. This section has thus confirmed that despite this difference in control approach, the three-level stand-alone SSSC developed in this chapter is able to provide the same dynamic variation of compensating reactance X_q as the stand-alone two-level SSSC of Sen, but with a fixed dc voltage.

3.7 The Effect Of Small Changes In Inverter DC Voltage On The Performance Of The Three-Level SSSC

3.7.1 Introduction

The previous section demonstrated the method of varying the ac output compensating voltage in the three-level SSSC without changing its dc capacitor voltage. When this type of SSSC is operated as a stand-alone device, the output compensating voltage is essentially controlled by varying the angle γ , and the dc capacitor voltage is regulated to stay at some desired value. As discussed previously, in practice, it may be necessary to adjust the set point of V_{dc} by means of the input V_{dc}^* to suit different transmission line conditions. When such adjustments are made, the compensating voltages injected into the transmission line must temporarily move away from near-quadrature with the line currents in order to allow the exchange of active power with the line needed to charge or discharge the inverter's dc capacitor as required. However, during such changes to the set point on the dc side of the SSSC there should be minimum disruption to the ac compensation of the line.

This section therefore now considers only the three-level SSSC but examines the effect on the transmission line when compensation is kept fixed (i.e. fixed X_q^*) but changes are made in the set point of the dc voltage regulator.

3.7.2 Time Domain Response Following Step Changes In V_{dc}^* ($X_q^* = 0.15$ pu) - First Case Study: Values Of γ Out Of Range

The aim of this study is to show the time domain response from the dead angle calculator of the SSSC when the set point of the inverter's dc capacitor voltage is stepped down to a value that is too low to be able to support the ac voltage magnitude V_q associated with the required reactance (i.e. X_q^*) demand. In practice, set point changes are unlikely to be made in a step fashion but rather by gradual ramping of the input from one set point to another. However, step changes are used in this study to observe the worst-case transient response. This study once again considers the three-level SSSC in the same transmission system considered by Sen in [34].

Fig. 3.16 shows the response of the three-level SSSC to such step changes; three system variables are shown, namely the desired dc voltage V_{dc}^* , the actual measured dc voltage V_{dc} and the inverter dead angle γ . At time $t = 0$ ms, the required compensating reactance X_q^* is 0.15 pu capacitive (i.e. $X_q^* = +0.15$ pu), the dc voltage is set at 60kV (0.53 pu) and γ is controlled to stay at 23.5° by the dead angle calculator. At $t = 50$ ms, the desired dc voltage V_{dc}^* is stepped down to 48kV (0.426 pu) i.e. a 20% decrease from the original dc value of 60kV. The voltage regulator rapidly reduces V_{dc} to try and meet the new commanded value, and in order to maintain the required magnitude of ac compensating voltage at this reduced value of inverter dc voltage, the dead angle calculator reduces the value of γ . However, because the magnitude of ac compensating voltage V_q required is greater than can be supported by the inverter at this new value of V_{dc} , the angle γ reaches the lowest possible value ($\gamma = 0^\circ$) at which time the angle γ and inverter dc voltage enter a limit cycle. An expanded view of γ from 50ms to 150ms is shown in Fig. 3.16 (d) where the dead angle calculator within the controller outputs undefined values of γ (i.e. the value within the arc-cosine in Equation (3.25) is larger than 1). The actual dc voltage is also affected as a result of such fluctuation as shown in Fig. 3.16 (b).

From $t = 150$ ms to $t = 250$ ms, V_{dc}^* is stepped back from an invalid operating point (where the system was in a limit cycle) to the original valid operating point where the system was originally at steady state i.e. $V_{dc}^* = 60$ kV. Despite the fact that the system was in a limit cycle, when it is stepped back to a valid V_{dc}^* it does recover (even after γ momentarily goes into the limit immediately after this step change of V_{dc}^*), although the system does take a long time to settle to a steady value of γ . When V_{dc} is stepped up further to 72kV (0.639 pu) at $t = 250$ ms, i.e. a 20% increase from the initial dc value, the dead angle calculator increases the value of γ to 39.5° to maintain the required V_q^* . This shows that this particular increased dc voltage level also lies within the range of the dead angle calculator.

This study has shown that in the three-level SSSC, when the dc capacitor voltage set point value determined by the voltage regulator is not large enough, the output from the dead angle calculator

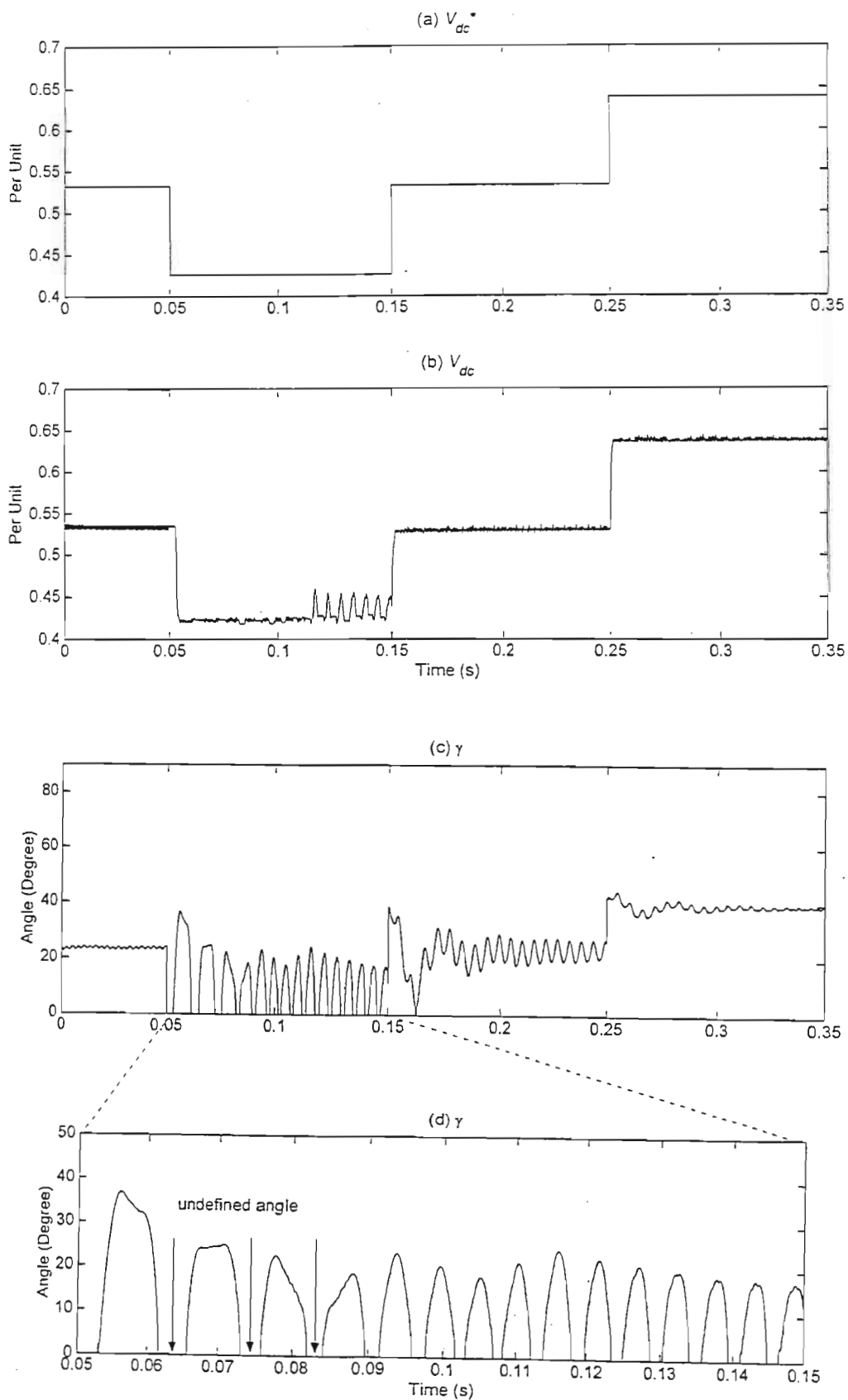


Fig.3.16: Time domain response of the three-level SSSC following step change in V_{dc}^* :

(a) V_{dc}^* ; (b) V_{dc} ; (c) γ ; (d) expanded view of γ from 0.05s to 0.15s.

may be briefly undefined during a transient or, in a worse case scenario, the inverter dc voltage may not even be sufficient to supply the required ac compensating voltage during steady state. It is therefore essential for the operator to adjust the desired dc voltage to a suitable level to ensure acceptable operation of the three-level SSSC. The study has also shown that the system recovers satisfactorily by increasing the dc voltage after the dead angle γ enters a limit cycle for this particular case study. It is also noted that the actual dc voltage is properly regulated to follow closely the desired dc voltage, except during the limit cycle.

The next subsection considers the performance of the three-level SSSC and the response of the transmission system with the same required compensating reactance of $X_q^* = 0.15\text{pu}$ capacitive, but with the desired dc voltage magnitudes V_{dc}^* increased with respect to the ones chosen in this particular study to avoid the problem of limit cycle.

3.7.3 Time Domain Response Following Step Changes In V_{dc}^* ($X_q^* = 0.15\text{ pu}$) - Second Case Study: Values Of γ Within Range

This subsection once again considers the time domain response of the SSSC and the transmission line when subjected to deliberate changes in the desired dc voltage V_{dc}^* . The *changes* in V_{dc}^* are of the same percentage magnitude as in the previous section, but the initial magnitude of the dc voltage, and each subsequent magnitude of V_{dc} , is increased by 18kV. (This overall increase in V_{dc} of 30% is done to ensure that the dc voltage values all lie within the dead angle calculator limits throughout the transient investigation.) Fig. 3.17 shows the response of the three-level SSSC and the transmission system following these changes in the amplitude of the inverter dc voltage.

As in the previous section, when time $t = 0\text{ ms}$, in Fig. 3.17, the required compensating reactance X_q^* is 0.15 pu capacitive (i.e. $X_q^* = +0.15\text{pu}$), but now the dc voltage is set at 78kV (0.692 pu) and γ is controlled to stay at 44.2° by the dead angle calculator. At $t = 50\text{ms}$, the desired dc voltage V_{dc}^* is stepped down to 66kV (0.586 pu). The dead angle γ decreases and settles to around 33° to maintain the required fundamental magnitude of the ac compensating voltage V_q^* injected into the line. This decrease in γ corresponds to an increase in the width of the on-pulse of each turn-off device, which causes a change in the *shape* of the ac compensating voltage waveform, e_{2a} . The decrease in V_{dc}^* , on the other hand, decreases the *peak amplitude* of the ac compensating voltage waveform, e_{2a} , as shown in Fig. 3.17(d). However, the combination of reduced peak and increased width of on-pulse of the ac waveform ensures that its *fundamental* magnitude remains constant at steady state as required. The line current i_a and both the active

(P_q) and reactive (Q_q) powers are almost unchanged despite some small fluctuations immediately after the step change in V_{dc}^* . This confirms that the required steady-state compensation provided by the three-level SSSC is unaffected by the change in the value of V_{dc} . At $t = 150\text{ms}$, V_{dc}^* is stepped back up to 78kV and γ returns to 44.2° in steady state.

When V_{dc}^* is stepped up further to 90kV (0.798pu) at $t = 250\text{ms}$, γ increases to 51.7° . This increase in the desired dc voltage increases the peak amplitude of the ac compensating voltage e_{2u} .

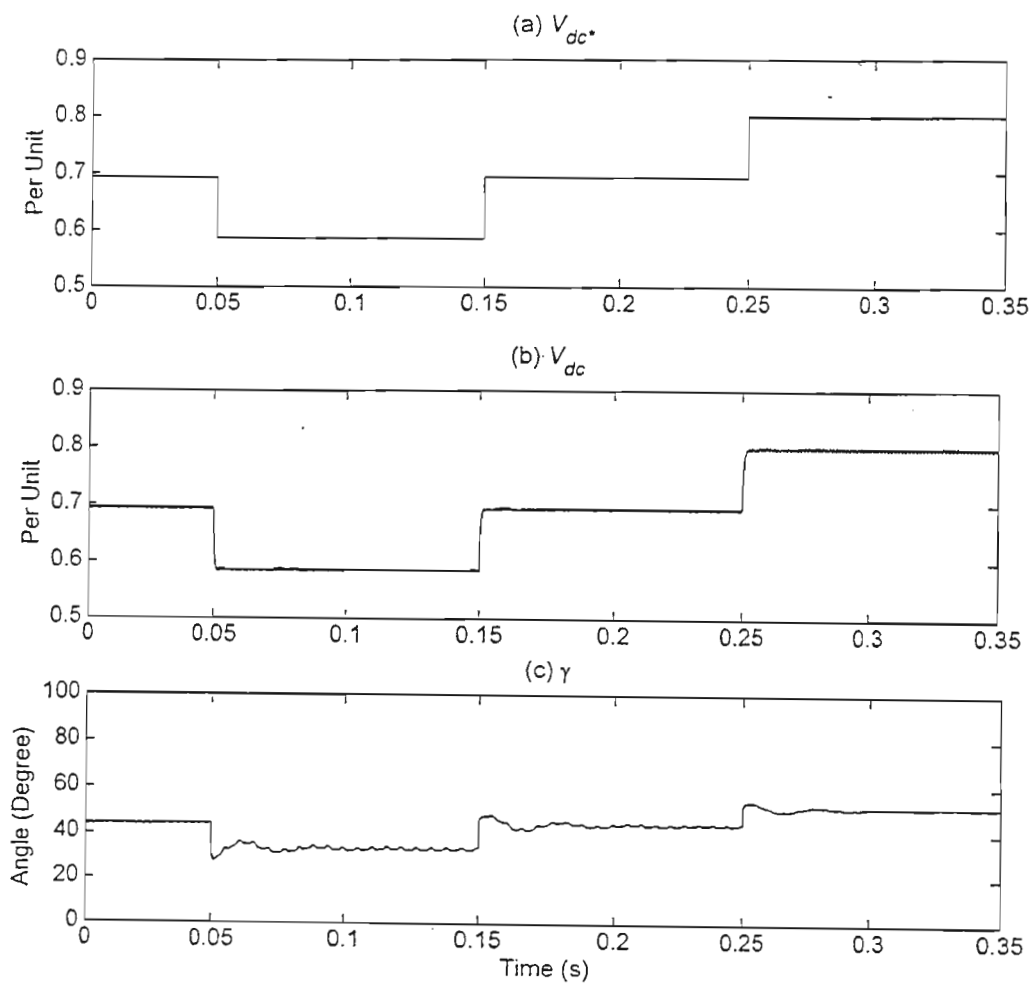


Fig.3.17: Time domain response of the three-level SSSC and the transmission system following step changes in V_{dc}^ : (a) V_{dc}^* ; (b) V_{dc} ; (c) γ .*

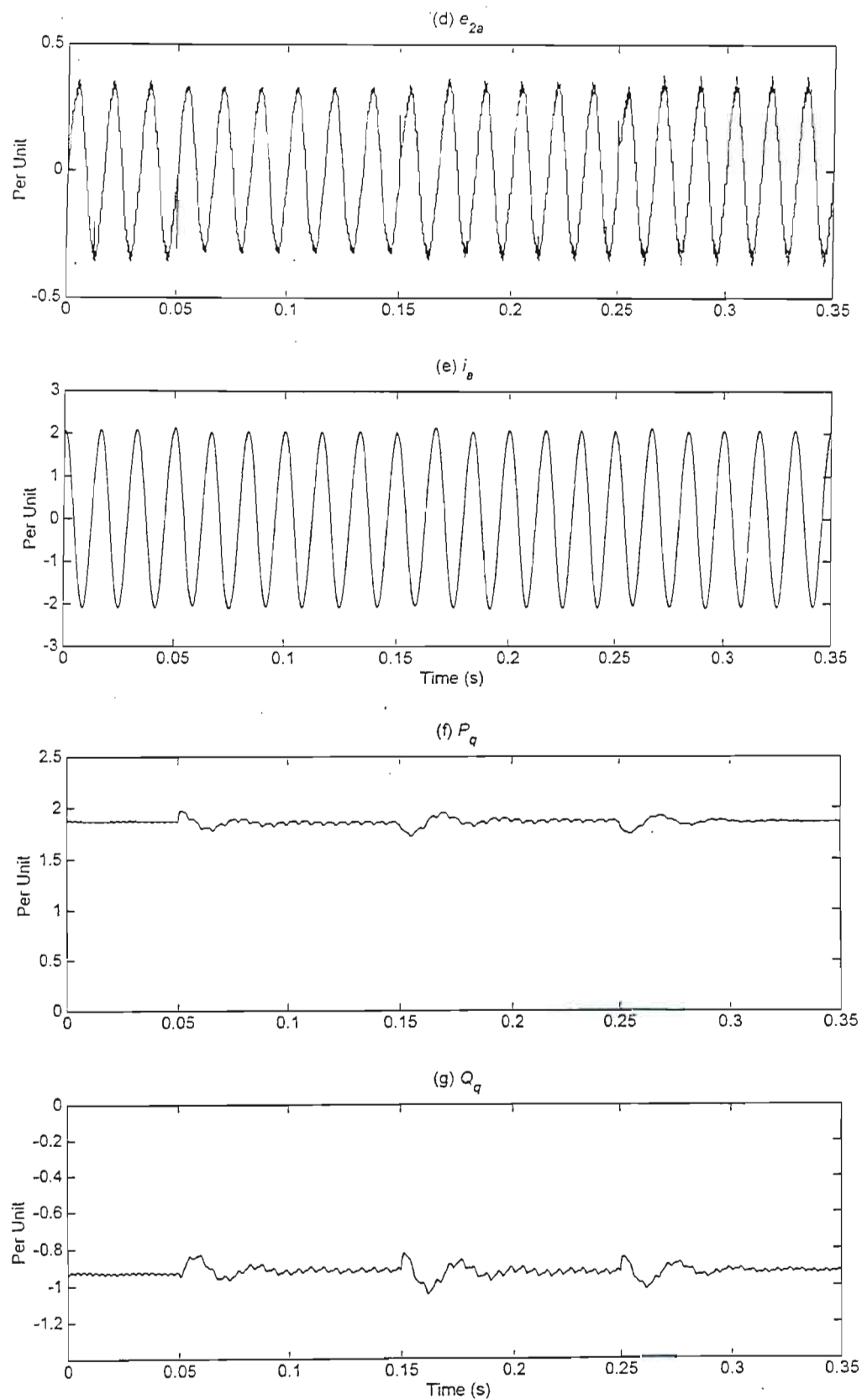


Fig.3.17 (continued): Time domain response of the three-level SSSC and the transmission system following step changes in V_{dc}^ : (d) e_{2a} ; (e) i_a ; (f) P_q ; (g) Q_q*

The resulting increase in γ means a decrease in the width of the on-pulse of each turn-off device, and therefore a change in the shape of e_{2a} as shown in Fig. 3.17(d). The line current i_a and both the active (P_q) and reactive (Q_q) powers still remain unchanged during steady state, confirming once again that the steady-state compensation is unaffected by the change in V_{dc} .

It is noted that during each change of V_{dc}^* , there are transient periods before variables settle to their steady state values. As previously explained, this is due to the exchange of active power at the interface between the SSSC and the transmission line, in order to charge or discharge the inverter dc capacitor to the new desired voltage levels. However, during steady state these changes in the dc voltage do not change the variables on the ac side of the SSSC i.e. the ac characteristics of the transmission line remain unaffected by V_{dc} , provided that the chosen set point V_{dc}^* is within the range of dead angle calculator. Therefore, within limit, the dc voltage may be controlled to vary the dead angle γ and therefore adjust the total harmonic distortion (THD) to appropriate levels. The topic of varying dc voltage in regards to THD is to be investigated in the next section.

3.8 The Effect Of Small Changes In Inverter DC Voltage On The Total Harmonic Distortion (THD) Of The Three-Level SSSC

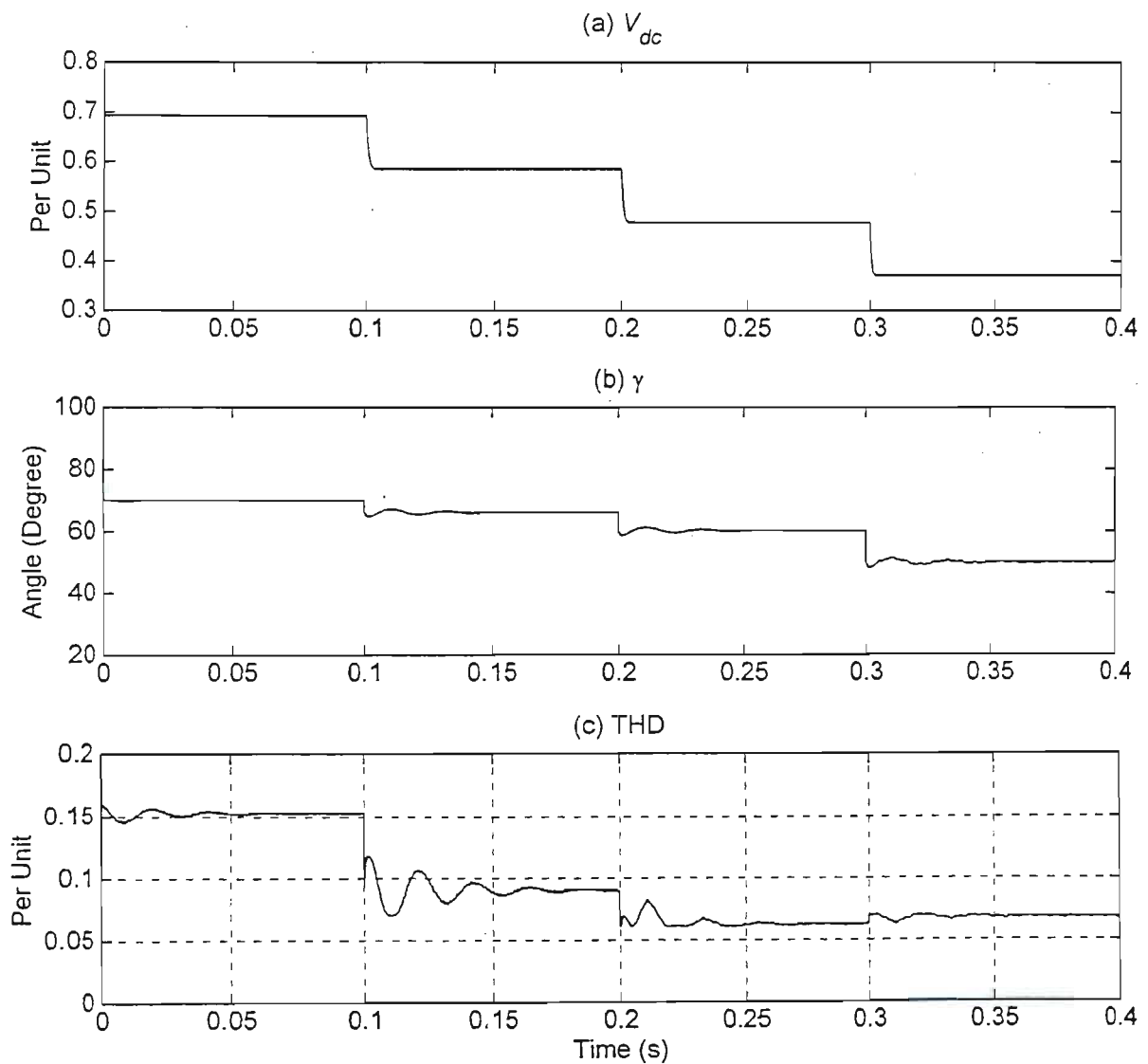
3.8.1 Introduction

The previous section has demonstrated that with a decrease in dc capacitor voltage in the three-level SSSC, γ decreases accordingly. In Chapter Two, under Section 2.5 describing the performance of a 24-pulse three-level inverter, it was shown that the THD of the ac output waveform remains below 10% for values of γ between 0° and 60° . Although the 24-pulse three-level inverter offers this considerably low THD for a wide range of γ values, depending on the amplitudes of the required line reactance X_q^* and the transmission line current, γ may be forced into the region above 60° . It is then desirable to lower V_{dc}^* to bring down the value of γ , and hence the THD.

3.8.2 Time Domain Response Following Step Changes In V_{dc}^* ($X_q^*=0.9$ pu)

This subsection now once again considers the time domain response of the SSSC to deliberate step changes in the desired dc voltage V_{dc}^* . However, the focus of this study is to show the

effect on the total harmonic distortion of manipulating the dc voltage with constant required reactance. Fig. 3.18 shows the response of the three-level SSSC by means of two system variables, the dc voltage V_{dc} and the dead angle γ ; the graph of THD is plotted in Fig. 3.18 (c). For the purpose of referencing, Fig. 3.19 shows the theoretical THD curve and the THD results from the simulation.



*Fig.3.18: Time domain response of the three-level SSSC following changes in V_{dc} *: (a) V_{dc} ; (b) γ ; (c) THD.*

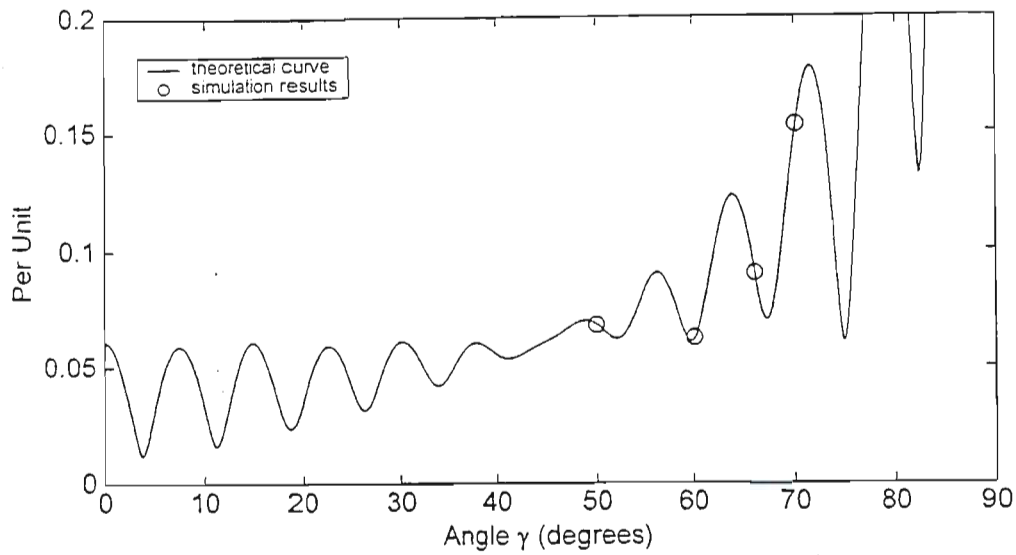


Fig.3.19: THD for a 24-Pulse three-level inverter: theory vs. PSCAD/EMTDC simulation.

When $t = 0$ ms, the dc voltage is set at 78kV (0.69 pu) and for the purpose of this study, X_q^* remains fixed at 0.09 pu capacitive i.e. $X_q^* = +0.09$ pu. Under such conditions, the dead angle γ is at 70.08° and the THD is 0.153 pu as shown in Fig. 3.18 (c). When V_{dc}^* is decreased to 66kV (0.585 pu) at $t = 100$ ms, γ decreases to about 66.2° at steady state and therefore the THD decreases to 0.09 pu (i.e. the THD is less than 10%). At $t = 200$ ms, V_{dc}^* is decreased further down to 54kV (0.479 pu) i.e. another 12kV drop. The dead angle γ reduces to 60.2° during steady state and the corresponding THD decreases to 0.0625 pu. At $t = 300$ ms, V_{dc}^* is again decreased by another 12kV to 42kV (0.372 pu). The dead angle γ is now reduced to 50° and even though the THD now rises to 0.068 pu, it still remains below 10%. These calculated values of THD during the simulation correspond to the theory as shown in Fig. 3.19.

This study has shown that by intentionally changing the dc voltage, the THD of the ac compensating voltages in the three-level SSSC may be lowered, thereby allowing a “cleaner” voltage to be injected into the transmission line. Depending on different transmission line operating conditions, the dc voltage of the γ -controlled SSSC may be programmed or manually changed to adjust the dead angle in order to decrease the amount of harmonics injected on to the transmission line.

3.9 Conclusion

Detailed models of both a two-level and a three-level static synchronous series compensator have been developed in the simulation package PSCAD/EMTDC. In the case of the two-level SSSC model, the ac output voltage is controlled solely by varying the inverter dc voltage by means of a voltage regulator in the high-level controller. In the case of the three-level SSSC model, the output voltage is controlled by varying the dead angle γ and the dc voltage is also made adjustable. In both cases, the inverter's power electronics and associated transformers are represented in detail using the model described in Chapter Two.

The results from the two-level SSSC model developed in PSCAD/EMTDC have been shown to be virtually identical to those simulated in EMTP by Sen [34], and therefore confirm the correctness of the more detailed SSSC model developed in PSCAD/EMTDC. When this SSSC was simulated under conditions of constant dc voltage and variable γ (and therefore variable dc-to-ac gain across the inverter), the results showed the ac performance of the compensator to be almost identical to that of the two-level SSSC simulated in EMTP by Sen [34], and therefore validate the accuracy of the SSSC model developed in PSCAD/EMTDC.

Various studies were conducted to investigate the behaviour of the three-level SSSC when experiencing changes or disturbances in the dc capacitor voltage. In order to show the effect of the real limits within the dead angle calculator in the three-level SSSC, the first study investigated a case where the desired dc voltage of the inverter is lowered to a level where it is insufficient to support the necessary ac compensating voltage to be injected into the line. It was shown that the dead angle calculator then outputs undefined values of γ . In the second study, the magnitude of dc voltages used was chosen to lie within the bounds of the dead angle calculator. It was then shown that, provided the bounds of γ are not exceeded, when the magnitude of the inverter dc voltage is changed, the SSSC controller automatically adjusts the dead angle γ to continue providing the correct emulated reactance at steady state. Also, with each variation in the dc voltage, there is a momentary exchange of active power between the three-level SSSC and the transmission line immediately after the step changes in desired dc voltage V_{dc}^* ; otherwise, the ac side of the SSSC experiences no noticeable change during steady state. Finally, the third study also demonstrated the flexibility of the three-level SSSC: by adjusting the desired dc voltage appropriately, the total harmonic content of the injected compensating voltages can be maintained at acceptable levels as operating conditions in the transmission line change.

The benchmarked results of the two-level SSSC and the three-level SSSC models presented in this chapter have been shown to be correct and therefore the PSCAD/EMTDC models of these

devices can be used to analyse their characteristics and performance in other applications later in the thesis. The following chapter first describes the development of a STATCOM simulation model, again using the same 24-pulse, three-level inverter topology of Chapter Two, followed by the combination of this STATCOM model with the SSSC model described in this chapter to form a larger UPFC model.

CHAPTER FOUR

THE 24-PULSE STATCOM AND UPFC

4.1 Introduction

The previous chapter described the detailed development of two SSSC models based on the 24-pulse, three-level voltage-sourced inverters developed in Chapter Two, each with their own set of high level controls. The first SSSC model presented had the inverter gain fixed (with the dead angle fixed at $\gamma = 0^\circ$) and the output ac voltage was controlled by adjusting the dc capacitor voltage. The second SSSC exploited the full functionality of the three-level inverter by changing the gain across the inverter (by varying the dead angle, γ) in order to control the output ac voltage.

This chapter now extends the modelling study to the two other inverter-based FACTS devices and is therefore divided into two major sections:

1. Static Synchronous Compensator (STATCOM)

The Static Synchronous Compensator (STATCOM) was often referred to as the Static Condenser (STATCON) [11,17,47] or Advanced Static VAR Compensator (ASVC) [22,23,24,25] before the FACTS Working Group standardized the terms and definitions [9] used in the field of FACTS technology in 1997. The STATCOM is a shunt device that provides reactive compensation to the transmission line by injecting almost sinusoidal current of variable magnitude at the point of connection.

2. Unified Power Flow Controller (UPFC)

The concept of the Unified Power Flow Controller (UPFC) was first introduced in the early 1990s with major contribution by Dr Gyugyi [17,26,30]. Since then, the UPFC has been hailed as *“the most versatile and complex power electronic equipment that has emerged for the control and optimization of power flow in electrical power transmission systems”* [14]. When the STATCOM and the SSSC are operated independently of one another, they are restricted to work only in the reactive power domain because these devices do not generally have external sources of power, nor do they exchange active power with the ac transmission system, except to replenish their internal losses. However, when the STATCOM and SSSC are connected via a common dc capacitor to form a UPFC, the device is now able to operate

in the real power domain. This is due to the fact that the dc link capacitor voltage is regulated by the STATCOM which allows the SSSC to inject ac voltages in series with the line at any angle with respect to the line current i.e. the exchanged power at the SSSC's ac terminals can be both real and reactive. The total real power absorbed by the UPFC is equal to the losses in the STATCOM and SSSC inverters and associated transformers.

Most modelling studies of inverter-based FACTS devices have taken a simplified approach, where the actual power electronics and associated firing controls are not represented; examples of this mathematical modelling approach in STATCOM and UPFC studies include references [22,38] and [14,27,31,32,47–54,73] respectively. Although [27] likewise ignores the actual inverter power electronics, the discontinuous nature of the inverter's ac output waveforms are represented in detail. Other modelling studies have, however, represented the detailed power electronics: references [23,24,25] all developed STATCOM models based on multi-level inverters but incorporated PWM, FFM (Fundamental Frequency Modulation) or SHEM (Selective Harmonic Elimination Modulation) switching techniques; reference [62] developed a detailed STATCOM simulation model but assumed a two-level inverter; reference [63] developed a detailed UPFC model but it is based on three-level, 12-pulse inverters.

By developing detailed models of these inverter-based FACTS devices, accurate studies on their interactions with the rest of the electrical network may be carried out. Therefore, in this chapter, the detailed model of a 24-pulse, three-level inverter developed in Chapter Two will again be used as the basis for developing both STATCOM and UPFC simulation models. Although the three-level inverter will be employed in the model of the STATCOM, the inverter will however be used as a two-level device by setting the dead angle $\gamma = 0^\circ$, since the output ac voltage of a STATCOM is normally adjusted by varying its dc capacitor voltage. In the case of the SSSC functioning as a part of a larger UPFC, it will exploit the inverter's full three-level capability. This is necessary because, as explained previously, the SSSC can not adjust its output ac voltage by varying the dc capacitor voltage within a UPFC, as this common dc voltage is now controlled by the STATCOM.

This chapter presents detailed models of a STATCOM and a UPFC that have been developed for the simulation package PSCAD/EMTDC. The focus of the chapter is on implementing standard STATCOM and UPFC controls actually used in transmission-level applications. Both the STATCOM and UPFC high level controllers implemented in this chapter are taken from reference [27] and therefore the EMTP simulation results from [27] will be used for the purpose of benchmarking. The STATCOM and UPFC models developed here are an extension of the work

in [27] by presenting the actual power electronic devices within the STATCOM and UPFC inverters and their low-level firing controls.

4.2 The 24-Pulse Two-Level STATCOM

4.2.1 Introduction

The primary function of a STATCOM is to control the amplitude of the transmission line's ac voltage at the point of connection [26], by providing controllable shunt reactive compensation to the transmission system. The STATCOM itself comprises a voltage-sourced inverter, a magnetic adding circuit and a coupling transformer that is used to supply or absorb the ac current in shunt with the transmission line. The reactive current flowing in and out of the STATCOM is determined by the difference in amplitude between the transmission line voltage and that of the voltage-sourced inverter, coupled via the transformer's leakage reactance. As long as the inverter output voltage is kept in phase with the line voltage, this current will always be in quadrature with the system voltage because of the reactive coupling [24]. The magnitude and the direction of this shunt current are dependent on the inverter's ac output voltage: when the inverter's output voltage is higher than the transmission line voltage, shunt current is injected into the line and reactive power is generated by the STATCOM, i.e. the STATCOM operates in capacitive mode; when the inverter's output voltage is lower than the transmission line voltage, shunt current flows into the STATCOM and reactive power is absorbed by the STATCOM, i.e. the STATCOM operates in inductive mode. Since the inverter's output voltage amplitude is controlled by adjusting the dc capacitor voltage, active power must temporarily be exchanged at the STATCOM terminals to either charge or discharge the dc capacitor in order to adjust the reactive output of the STATCOM.

Fig. 4.1 shows a single-line, diagrammatic representation of a STATCOM in an ac transmission system similar to that studied in [27]; the system structure and parameters used in this chapter are the same as those in [27] in order to demonstrate the correctness of the STATCOM model presented here. The transmission system in Fig. 4.1 includes a sending-end voltage source V_s and a receiving-end voltage source V_r separated by some transmission angle, as well as inductive reactances X_s and X_r .

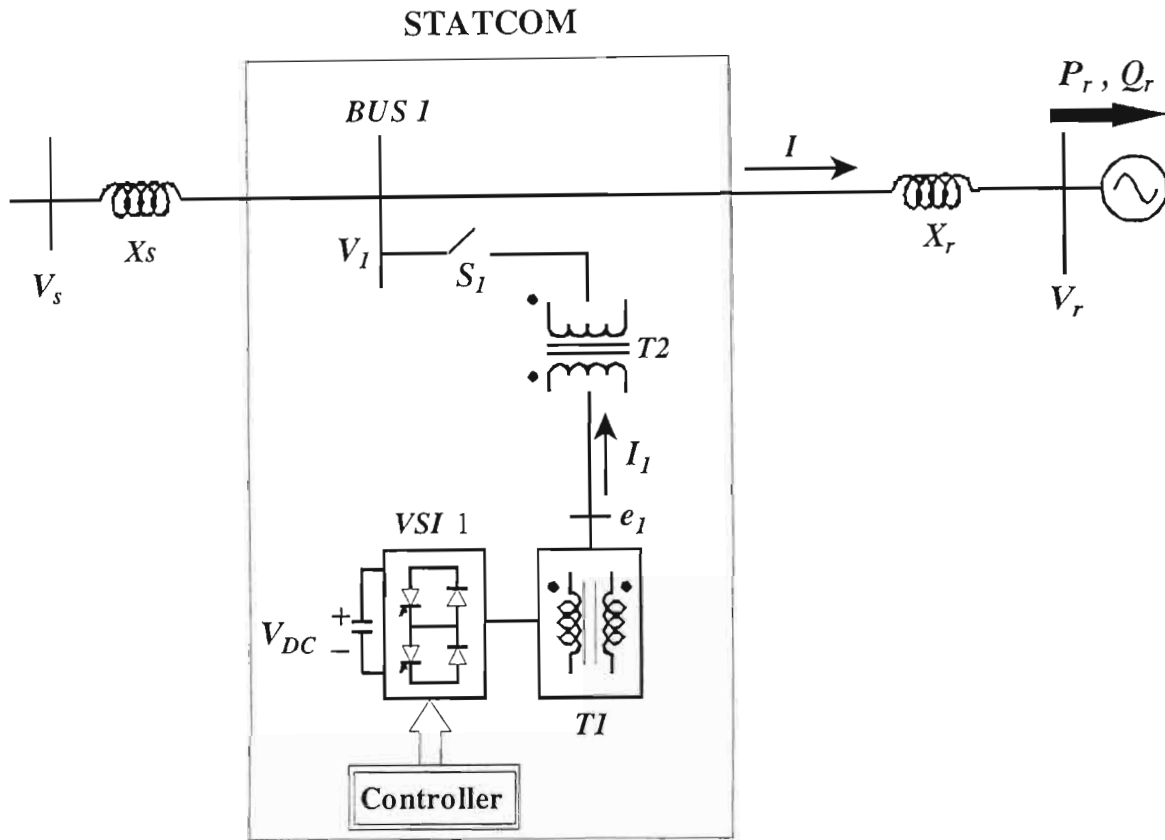


Fig.4.1: Diagram of the system used to compare the performance of the detailed STATCOM model against that predicted in [27].

In this thesis, the STATCOM consists of a three-level, 24-pulse harmonic neutralized voltage source inverter VSI1, a phase-shifting transformer $T1$ (magnetic adding circuit), a coupling transformer $T2$, current and voltage sensors, and a compensation controller. The power circuit, which consists of the 24-pulse three-level inverter and a magnetic adding circuit are described in Chapter Two. The following section describes in detail the STATCOM control scheme used to vary the ac output current that is injected in shunt with the transmission line.

4.2.2 The STATCOM Controller

The two control requirements of a STATCOM can be described as follows:

1. Phase Control: In order to ensure that the shunt current flowing in and out of the STATCOM is always in quadrature with the line voltage via the reactive coupling, the inverter's output ac voltage is required to be in phase with the system voltage.

2. **Magnitude Control:** The magnitude of the quadrature current injected by the STATCOM is a function of the inverter's output ac voltage which is dependent on the dc capacitor voltage. The charging and discharging of the dc capacitor requires exchange of active power between the transmission line and STATCOM. This active power exchange is made possible by slightly shifting the angle of the inverter ac voltages so that they are no longer perfectly in phase with those of the transmission line. The sign of this phase shift between the inverter and transmission line voltages determines whether the dc capacitor voltage charges up or discharges.

Fig. 4.2 shows the high-level control block diagram of a stand-alone, two-level inverter-based STATCOM developed by Sen [27], where the magnitude of the ac output voltage from the inverter is varied by controlling the magnitude of the inverter's dc capacitor voltage. Given the two control requirements of the STATCOM described above, Fig. 4.2 is made up of two corresponding sub-sections, namely, phase control and magnitude control. The output of this high-level controller then provides the input for the gate pattern logic i.e. the low-level controls which determine the firing signals for each switching device within the inverter. Each of the two sub-sections of the high-level SSSC controller is described as follows.

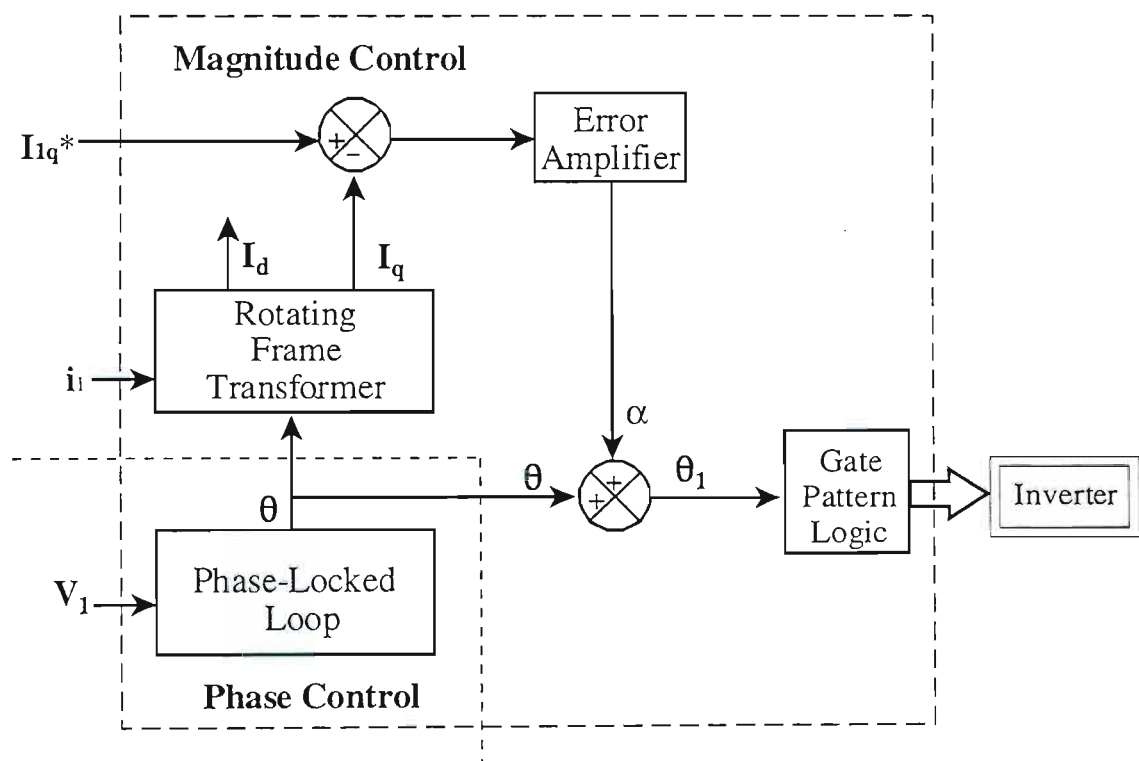


Fig.4.2: Control block diagram of a stand-alone two-level inverter based STATCOM [27].

4.2.2.1 Phase Control

The phase control of the inverter's output ac voltage is achieved by means of a phase locked loop, whose principle of operation was explained in detail in Chapter Three (section 3.2.3.1) and will thus only be briefly described here. The instantaneous phase-to-neutral voltages v_{1a} and v_{1c} at the STATCOM terminals are measured and converted into their ds and qs components in a stationary two-axis coordinate frame using the transformation matrix $[C]$. These ds and qs components are then transformed into the d and q axis coordinates of a synchronously rotating coordinate frame using the time-varying transformation matrix $[C_I]$. The voltage v_q is used as the error signal to the phase locked loop. By maintaining $v_q = 0$, the phase locked loop ensures that its output angle θ is synchronized to the phase of the transmission line voltage v_{1a} . Hence, in the STATCOM, the *steady-state* angle of the phase a inverter voltage is equal to this phase-locked angle θ so as to ensure that the STATCOM's ac voltages are in phase with the transmission line ac voltages. This form of synchronization also ensures that the transmission line ac voltage vector lies exactly along the d -axis of the synchronously rotating coordinate frame.

The Phase Control sub-section of the full STATCOM control scheme shown in Fig. 4.2 is now shown in more detail in Fig. 4.3, based on the explanations described above.

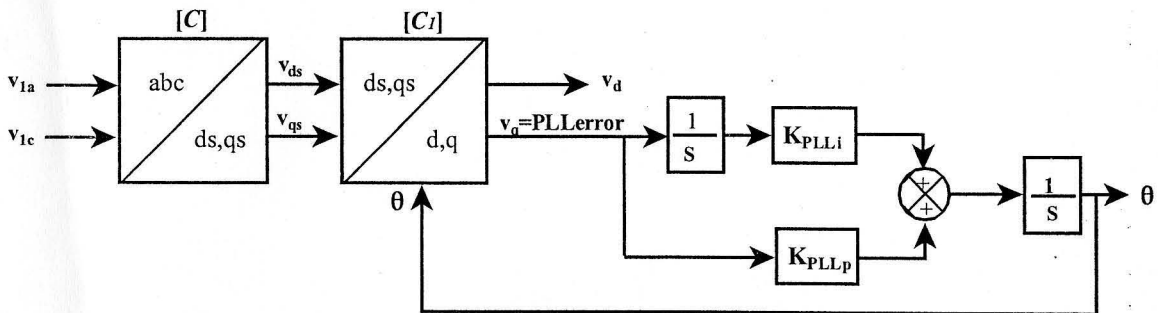


Fig.4.3: An expanded diagram of the Phase Control sub-section from Fig. 4.2.

4.2.2.2 Magnitude Control

As described above, the magnitude of the STATCOM's ac output voltage, and hence the reactive power it generates or absorbs is controlled by adjusting the magnitude of the inverter's dc voltage. The transfer of active power into the STATCOM to change its dc voltage is achieved by temporarily adding an offset phase angle α to the steady state angle θ of the STATCOM's ac output voltages. The particular control loops used to adjust the magnitude of the STATCOM's dc (and hence ac) voltages via this angle α depend on the mode of operation of the STATCOM.

For example, the STATCOM can be configured to regulate the magnitude of the transmission line voltage directly, or simply to provide a set-point value of reactive current injection into the transmission line. This latter mode of operation of the STATCOM is considered here, and the associated magnitude control loops shown in Fig. 4.4. The operation of this magnitude control is outlined below.

The coordinate transforms $[C]$ and $[C_I]$ discussed earlier are used to convert the measured shunt currents i_a and i_c at the ac output of the STATCOM into currents i_d and i_q in the synchronously rotating dq coordinate frame. Because the d axis of this coordinate frame is phase-locked to, and aligned with, the transmission line voltage vector, the q axis STATCOM current in this coordinate frame is, by definition, the reactive current at the output of the STATCOM. Fig. 4.4 shows that this measured q-axis (reactive) current output i_{lq} from the STATCOM is compared to a reference input I_{lq}^* , which represents the desired reactive current injection from the STATCOM, with a negative sign of I_{lq}^* representing *output* of reactive power from the STATCOM (STATCOM in capacitive mode); the error between I_{lq}^* and i_{lq} is used to drive a PI controller whose output is the temporary phase offset α to be added to the instantaneous angle θ to form the required angle θ_1 of the STATCOM's ac output voltages.

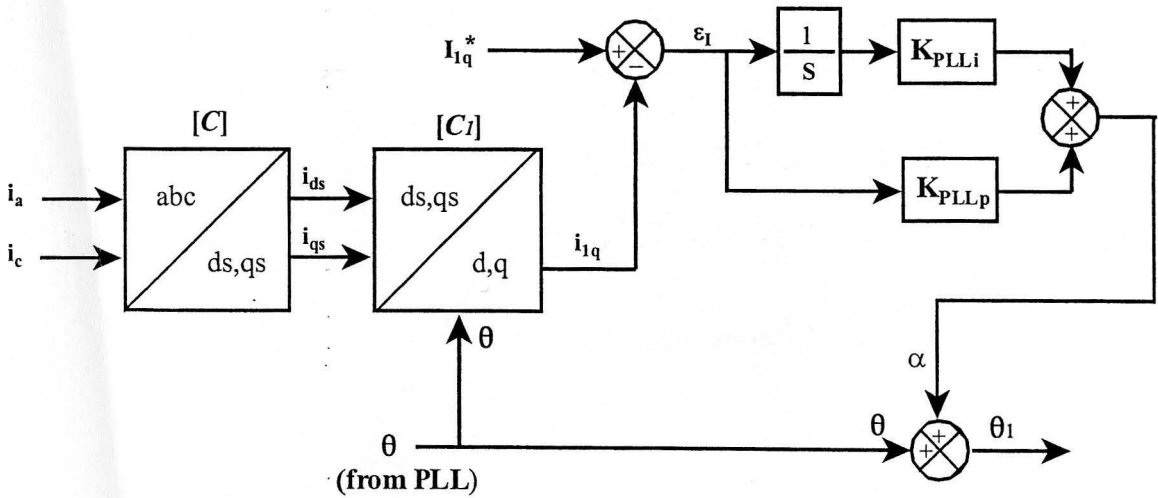


Fig.4.4: An Expanded and Detailed Diagram of Magnitude Control sub-section from Fig. 4.2.

Consider the situation when the magnitude of the capacitive reactive current i_{lq} output at the STATCOM terminals is less than the magnitude of capacitive current commanded at the controller input I_{lq}^* , (i.e. I_{lq}^* is more negative than i_{lq}) such that the error ϵ_l in the PI controller is negative. In this case the PI controller creates a negative offset angle α , retarding the phase of the STATCOM ac voltages relative to the transmission line voltages, thus admitting positive real

power into the STATCOM to charge up its dc voltage. As the dc voltage charges up, the STATCOM's ac voltages increase in magnitude relative to the transmission line voltages, thus increasing the size of the capacitive reactive current output from the STATCOM towards the reference value I_{lq}^* . When the STATCOM ac voltages reach the correct amplitude (relative to the line voltages) to generate the commanded value of reactive current I_{lq}^* , the error ε_l and phase offset α return to zero and the STATCOM ac voltages return to being in phase with the transmission line voltages.

Similarly, if the magnitude of the capacitive reactive current i_{lq} is larger than the commanded value I_{lq}^* (i.e. I_{lq}^* is less negative than i_{lq}), the resulting positive error ε_l in the PI controller adds a positive phase offset α to the STATCOM ac voltages, advancing them relative to the line ac voltages, resulting in negative real power into the STATCOM (i.e. flow of real power out of the STATCOM to discharge its dc voltage). As the ac voltages of the STATCOM decrease in magnitude relative to the line voltages the reactive current output from the STATCOM decreases back towards the reference value I_{lq}^* .

4.2.3 STATCOM Simulation Model In PSCAD/EMTDC

A detailed simulation model of the two-level inverter based STATCOM described in the previous section has been developed in the simulation package PSCAD/EMTDC. This STATCOM simulation model comprises four main sub-modules:

- (i.) the transmission line and the coupling transformers that are used to allow current to flow in or out of STATCOM;
- (ii.) the 24-pulse three-level inverter together with phase-shifting and adding transformers developed in Chapter Two (in the STATCOM application the inverter is operated as a two-level device with γ fixed at 0°);
- (iii.) the high-level STATCOM controls described in the previous section.
- (iv.) the low-level inverter firing controls situated between the output of the high-level STATCOM controls and the inverter itself.

Although the high-level STATCOM controller in this model is based on that in [27], the STATCOM model here is more detailed than [27] since all the inverter's power electronics and

firing controls are represented as well as the phase shifting and adding transformers actually present in a multi-pulse inverter arrangement. This PSCAD/EMTDC model has been used to simulate the dynamic performance of the STATCOM in the same study system that was considered in reference [27]. The predictions of the PSCAD/EMTDC model are then directly compared to those of the EMTP model used by Sen in [27] (the details of Sen's EMTP code was provided as an appendix in [27] and this code has been used to reproduce Sen's results using the EMTP program). The parameters for the study system are taken from [27] and listed in Appendix D.1. The full details of the STATCOM simulation model with all its components in PSCAD/EMTDC are shown in Appendix D.2.

The following section compares some of the STATCOM time domain results produced by the PSCAD/EMTDC simulation model developed in this thesis with the results from the EMTP model in [27].

4.2.4 Two-Level STATCOM Benchmark Results

The left hand side of Fig. 4.5(a) to (g) shows the dynamic response of the STATCOM to changes in commanded quadrature current I_{iq}^* as simulated using the EMTP model of Sen [27], whereas the right hand side of Fig. 4.5(a) to (g) shows the simulated results of the STATCOM to the same changes in I_{iq}^* using the detailed PSCAD/EMTDC model presented in this chapter. Fig. 4.5(h) shows the simulated results of the inverter voltage, e_{ia} , the line voltage, V_{ia} , and the phase a shunt current, I_{ia} , from the PSCAD/EMTDC simulation study in more detail.

In each case the sending and receiving end voltages in the transmission line are kept at constant magnitude and the transmission angle (phase between V_s and V_r) remains fixed. The STATCOM is then used to vary the magnitude of the bus 1 voltage (c.f. Fig. 4.1) by changing the commanded quadrature component of the inverter current I_{iq}^* .

From the time $t = 0$ to $t = 50\text{ms}$ in Fig. 4.5, switch S1 remains open so that the STATCOM is disconnected from the transmission system. With the dc capacitor pre-charged, the inverter's output voltage is controlled to be in phase with the system voltage. At $t = 50\text{ms}$, S1 closes and the commanded quadrature current is set to $I_{iq}^* = 0$. Zero reactive current from the STATCOM requires the magnitudes of the inverter voltage, e_{ia} , and the system voltage, V_{ia} , to be the same, as shown in Fig. 4.5(h). At $t = 125\text{ms}$, the desired quadrature current I_{iq}^* is stepped from zero to 1 pu capacitive (i.e. $I_{iq}^* = -1$). Fig. 4.5(g) and (c) show that at $t = 125\text{ms}$ the angle α is temporarily made negative in order to retard the STATCOM voltage relative to the transmission

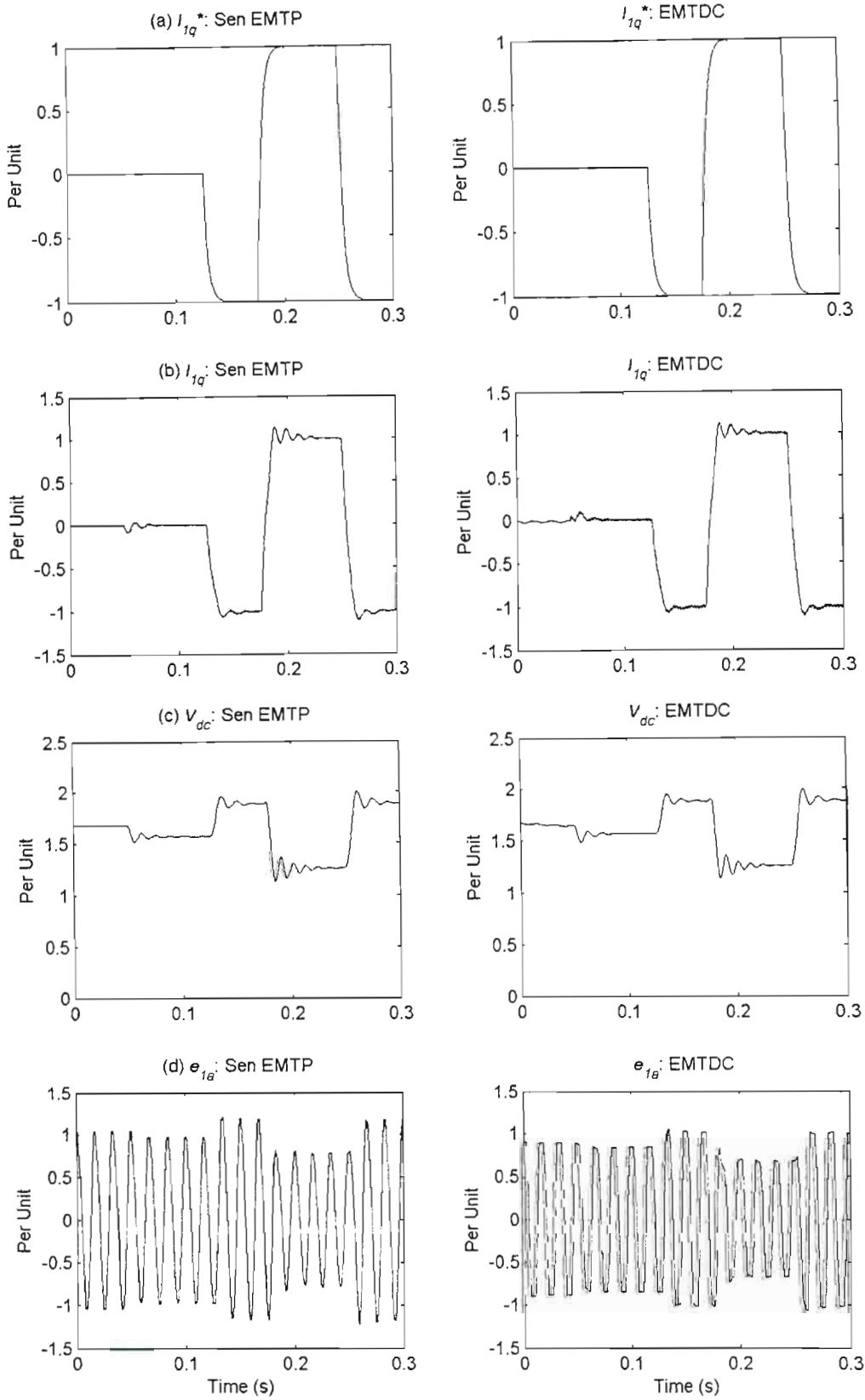


Fig.4.5: Performance of a STATCOM with a 24-pulse two-level inverter operating in inductive and capacitive modes, as modelled in EMTD [27] and PSCAD/EMTDC: (a) I_{dq}^ ; (b) I_q ; (c) V_{dc} ; (d) e_{id} .*

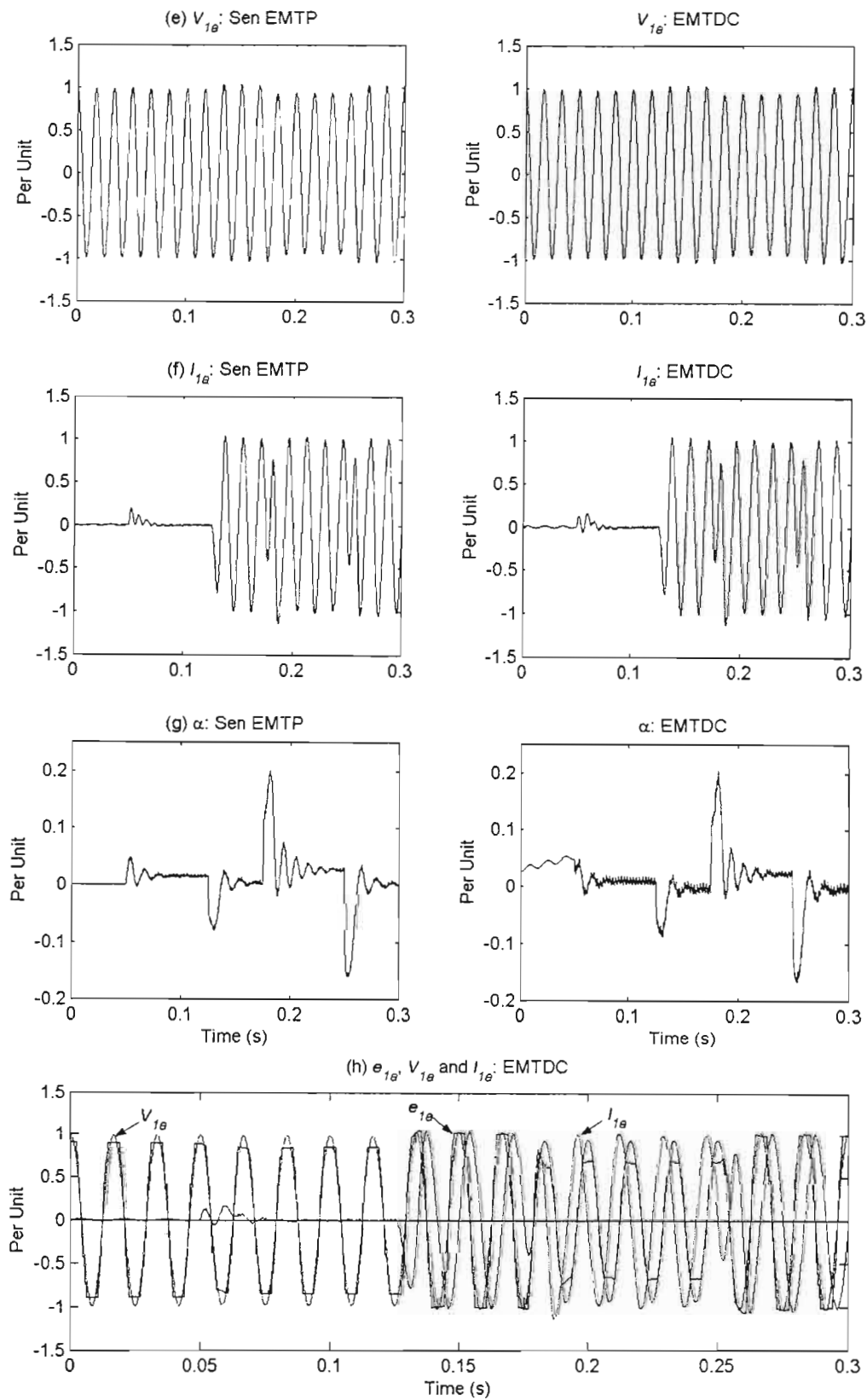


Fig.4.5 (continued): Performance of a STATCOM with a 24-pulse two-level inverter operating in inductive and capacitive modes, as modelled in EMTD [27] and PSCAD/EMTDC: (e) V_{1a} ; (f) I_{1a} ; (g) α ; and (h) e_{1a} , V_{1a} , and I_{1a} from the PSCAD/EMTDC simulation only.

line voltage so as to charge up the dc voltage. Fig. 4.5(h) shows that as a result of the increase in V_{DC} at $t = 125\text{ms}$, the STATCOM ac voltage e_{1a} is now larger in magnitude than the line voltage V_{1a} and the STATCOM ac current i_{1a} lags the STATCOM ac voltage e_{1a} by 90° , confirming the capacitive nature of the output in response to the negative value of I_{1q}^* . When I_{1q}^* is stepped to 1 pu inductive (i.e. $I_{1q}^* = +1$) at $t = 175\text{ms}$, the dc capacitor voltage, V_{DC} , decreases so that the inverter voltage, e_{1a} , is now lower than the system voltage, V_{1a} . In this inductive mode, the STATCOM ac current i_{1a} now leads the STATCOM ac voltage e_{1a} by 90° . At $t = 250\text{ ms}$, the commanded quadrature current I_{1q}^* is stepped back to 1 pu capacitive (i.e. $I_{1q}^* = -1$).

A close comparison between the results in Fig. 4.5 has shown that the response predicted by Sen's EMTP model in [27] and that predicted by the detailed PSCAD/EMTDC model of this thesis are virtually identical, thus confirming the correctness of the latter model. Fig. 4.6 illustrates this close agreement for one particular system variable: the transmission line voltage V_{1a} at bus 1 predicted by each of the models during a step change in STATCOM operating conditions is plotted on the same axes in Fig. 4.6 for comparison.

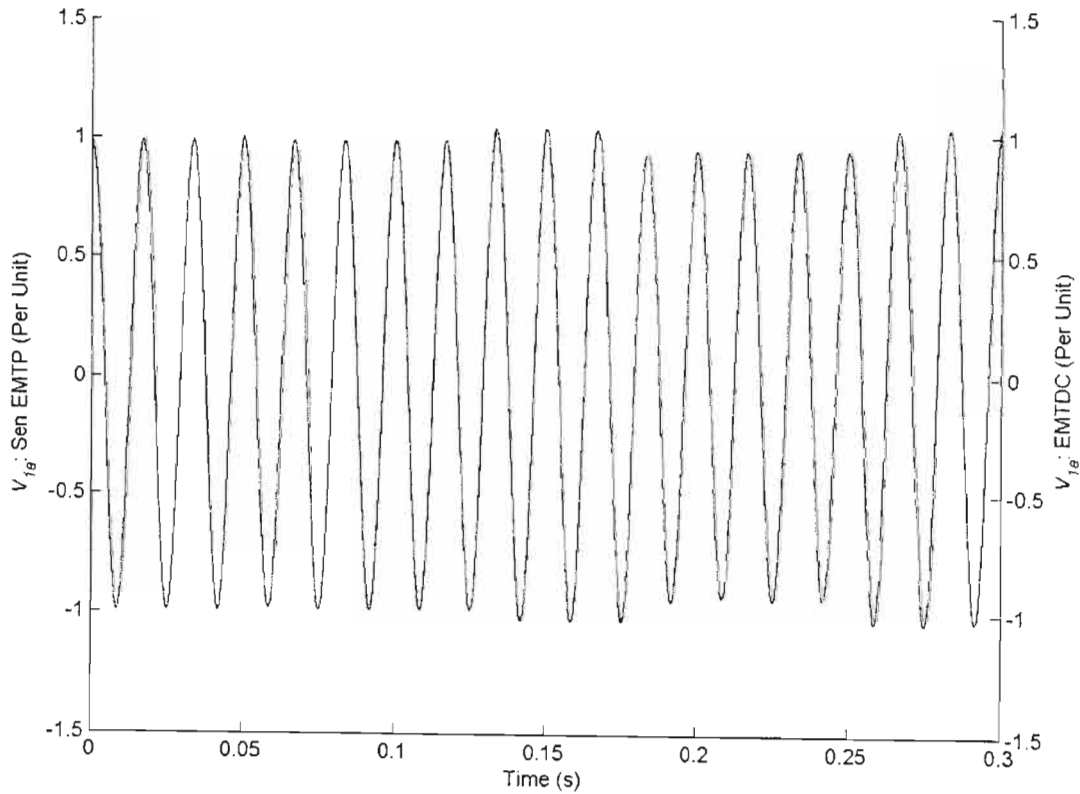


Fig.4.6: The line voltage, V_{1a} : EMTP [27] vs. PSCAD/EMTDC.

4.3 The UPFC

4.3.1 Introduction

A Unified Power Flow Controller is a combination of two inverter-based FACTS devices, namely a STATCOM and an SSSC, sharing a common dc link capacitor such that the arrangement is essentially an AC to AC power converter whose input and output variables can be independently controlled [26]. With such a set-up, the SSSC part of the UPFC can operate in various modes, including voltage injection mode, phase shifter emulation mode, line impedance emulation mode and automatic power flow control mode. Essentially, the SSSC can inject a voltage into the transmission line that is two-dimensional in nature, i.e. the voltage vector can be adjusted to be at any angle with respect to the line current so that all three transmission line parameters influencing power flow (voltage, impedance and phase angle) can be controlled. In the automatic power flow control mode, for example, the injected voltage can be controlled to maintain a desired active and reactive power flow in the transmission system [14]. The fundamental function of the STATCOM, when part of the UPFC, is to regulate the dc capacitor voltage depending on the active power requirement from the SSSC, so that the net active power absorbed by the UPFC is equal to the sum of the inverter and transformer losses. However, should it be required, the STATCOM is also able to control the voltage magnitude at its connection point in the transmission line by exchanging reactive current with the line.

The SSSC itself comprises a voltage-sourced inverter and a coupling transformer that is used to insert the ac output voltage of the inverter in series with the transmission line. The magnitude and phase of this inserted ac compensating voltage are determined by the high-level SSSC controls. The STATCOM comprises a voltage-sourced inverter, a magnetic adding circuit and a coupling transformer that is used to supply or absorb the ac current in shunt with the transmission line. Since the two voltage-sourced inverters are linked by a dc capacitor whose voltage is solely controlled by the STATCOM, the magnitude of the ac output voltage from SSSC is adjusted by varying the gain across its three-level inverter; this is done through changing the dead angle γ .

Fig. 4.7 shows a single-line, diagrammatic representation of a UPFC in an ac transmission system similar to that studied in [27]; the system structure and parameters used in this chapter are the same as those in [27] in order to demonstrate the correctness of the UPFC model presented here. The transmission system in Fig. 4.7 includes a sending-end voltage source V_s and a receiving-end voltage source V_r , separated by some transmission angle, as well as inductive reactances X_s and X_r .

In this section, the STATCOM part of the UPFC consists of a three-level, 24-pulse harmonic neutralized voltage source inverter VSI1, a phase-shifting transformer $T1$ (magnetic adding circuit), a coupling transformer $T2$, current and voltage sensors, and a compensation controller. The SSSC part of the UPFC consists of a three-level, 24-pulse harmonic neutralized voltage source inverter VSI2, a phase-shifting transformer $T3$ (magnetic adding circuit), a series voltage-injecting transformer $T4$, current and voltage sensors, and a compensation controller. The power circuits, which consist of the 24-pulse three-level inverters and magnetic adding circuits are described in Chapter Two. The following section describes in detail the particular control scheme used for the SSSC when it forms part of a UPFC.

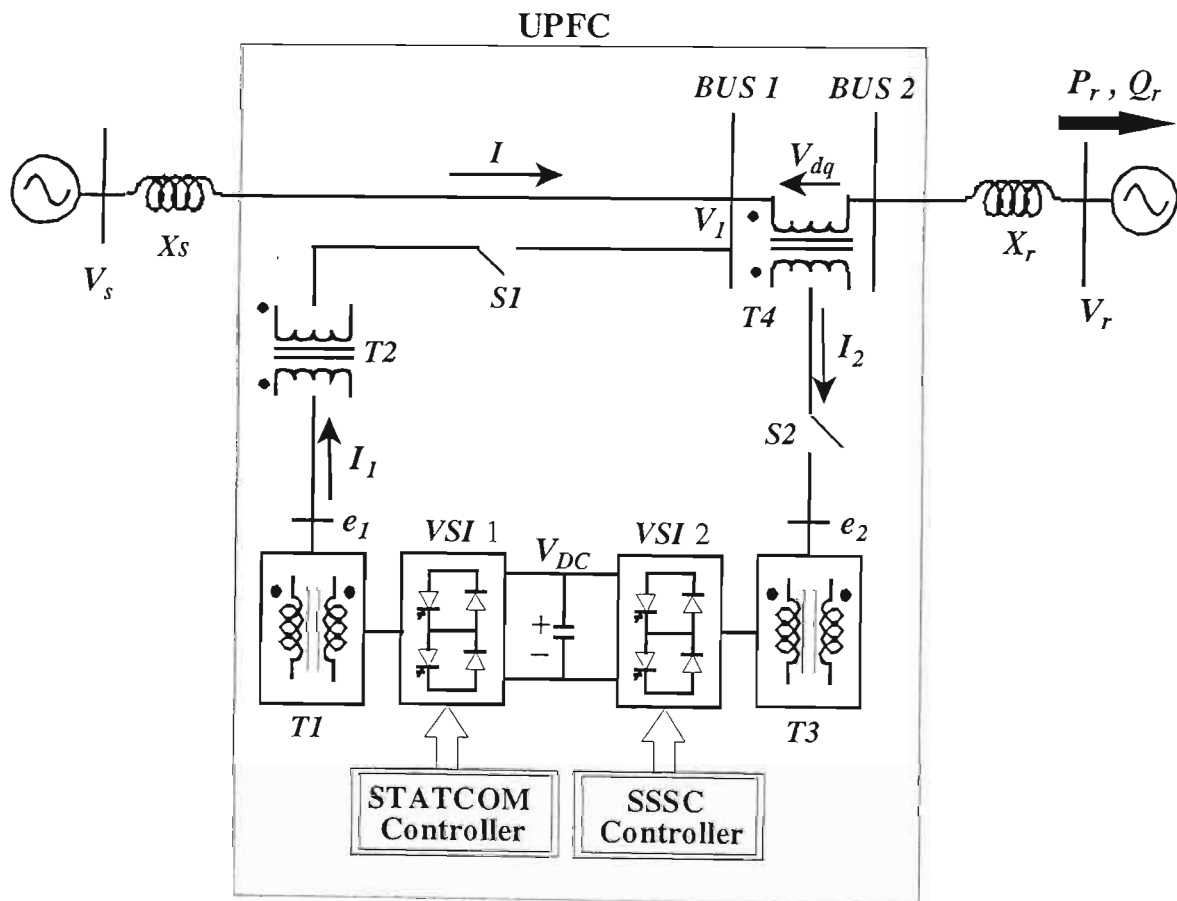


Fig.4.7: Diagram of the system used to compare the performance of the UPFC against that predicted in [27].

4.3.2 The UPFC Controller

When a STATCOM is operating as a part of a larger UPFC, the high level STATCOM controls remain exactly the same as those for a stand-alone STATCOM, as described in section 4.2.2. However, as stated earlier, the high-level controls for a stand-alone SSSC must be modified when the SSSC forms part of a UPFC. When an SSSC operates as a stand-alone device additional control is required to regulate the dc capacitor voltage. This control requirement is no longer necessary for the SSSC when it forms part of a UPFC, since the dc capacitor voltage is now controlled by the STATCOM.

Fig. 4.8 shows the high-level control block diagram of a three-level inverter-based SSSC that forms part of a UPFC, as developed by Sen [27], where the magnitude of the ac output voltage from the inverter is varied by controlling the gain across the inverter. Although the SSSC may be operated in various modes as described earlier, it is operated in the *voltage injection mode* in [27], which allows the series injected voltage vector to be at any magnitude and phase commanded by the reference inputs [14]. The high level control therefore differs from that in the stand-alone SSSC, described in Chapter Three, where the device was designed to operate in the *line impedance emulation mode*, such that the injected voltage vector is restricted to be in quadrature with the line current.

Since the SSSC as a part of a UPFC is operated in the voltage injection mode in [27], there are two reference inputs to the high-level controls, namely the desired magnitude and phase of the series injected voltage. These reference inputs to the SSSC are defined as β (phase of the SSSC's ac voltage relative to the transmission line voltage vector V_l) and V_{dq}^* (magnitude of the SSSC's injected ac voltage in per unit). Consequently, the two control requirements of an SSSC in this mode of operation can be described as follows:

1. Phase Control: In order to apply any phase shift β to the series injected voltage, the system phase angle needs to be first tracked and locked by the SSSC control.
2. Magnitude Control: The magnitude of the series injected voltage is determined by varying the gain across the inverter i.e. changing the dead angle γ .

Given the two control requirements of an SSSC described above, Fig. 4.8 is once again dissected into two corresponding sub-sections, namely, phase control and magnitude control. The output of this high-level controller then provides the input for the gate pattern logic i.e. the low-level controls which determine the firing signals for each switching device within the inverter. Each of the two sub-sections of the high-level SSSC controller is described as follows.

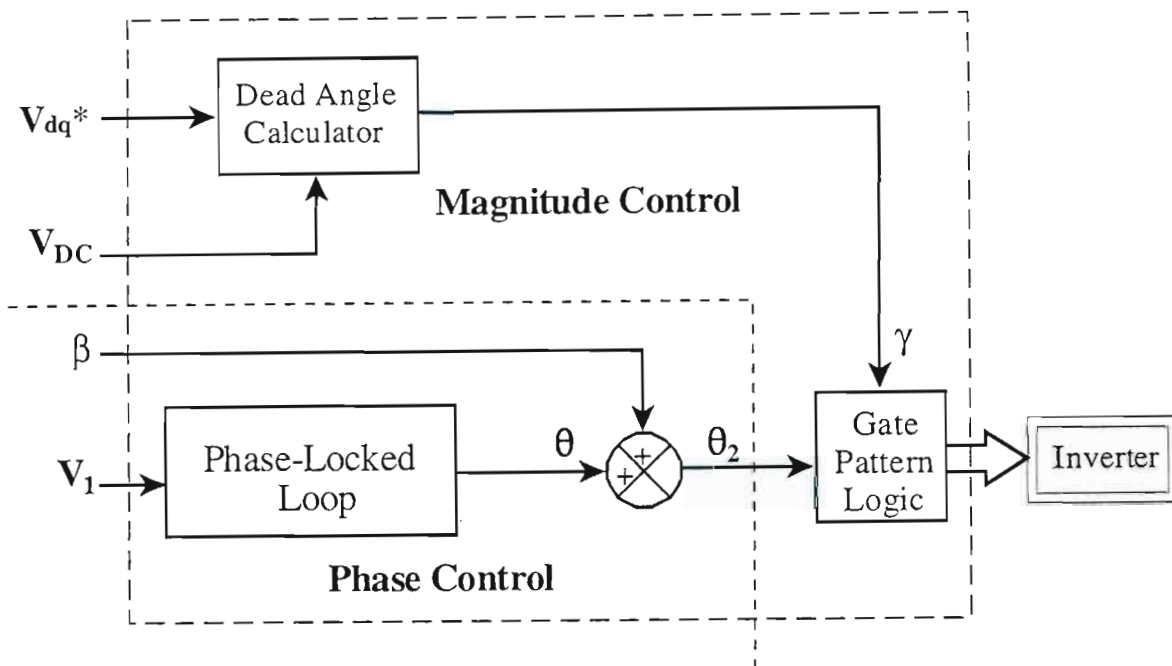


Fig.4.8: Control block diagram of three-level inverter based SSSC as a part of a UPFC [27].

4.3.2.1 Phase Control

A phase locked loop is employed to ensure that the series injected voltage vector is in synchronism with the transmission line voltages, and can be adjusted in phase relative to these voltages. The mechanism behind the phase locked loop will not be repeated here as it was explained in detail in Chapter Three and briefly reviewed in section 4.2.2.1 of this chapter. The commanded relative phase angle, β , at the input to the SSSC controls is simply added onto the instantaneous phase angle θ at the output of the phase locked loop to give the final angle θ_2 of the SSSC's injected ac voltage vector. Fig. 4.9 shows a more detailed version of the phase control sub-section of the full SSSC control scheme shown in Fig. 4.8. In practice, the phase angle θ is obtained from the same phase locked loop used for the STATCOM controls, that is the SSSC and STATCOM controls are synchronised to the same transmission line voltage using a single phase locked loop.

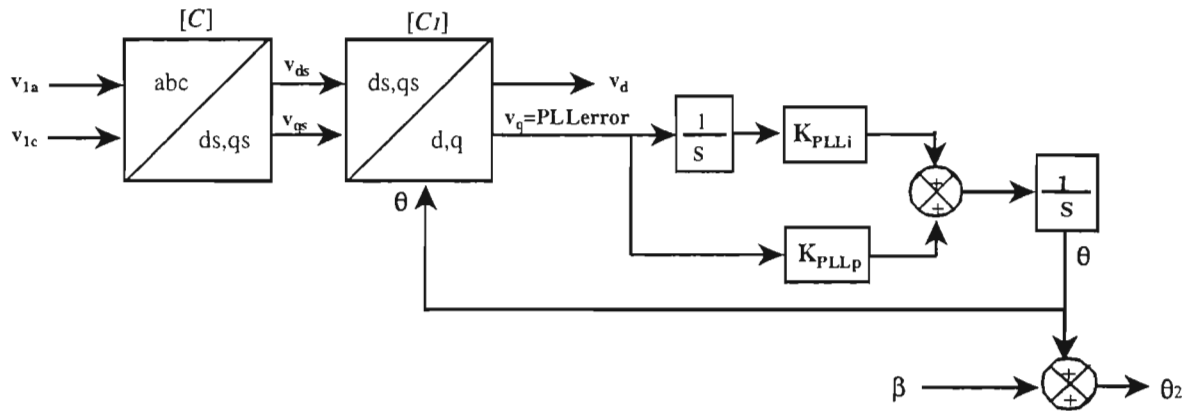


Fig.4.9: An expanded diagram of the Phase Control sub-section from Fig. 4.8.

4.3.2.2 Magnitude Control

With respect to the desired ac compensating voltage V_{dq}^* , the magnitude control in the SSSC as a part of the UPFC is similar to the stand-alone three-level SSSC described in section 3.5.2.2 of Chapter Three. The only difference in the implementation is that the desired ac compensating voltage, V_{dq}^* , is an independent input to the control system in the UPFC, whereas the desired compensating voltage V_q^* in the stand-alone SSSC is a function of the desired compensating reactance to be emulated. Apart from that, the magnitude of the SSSC output voltage is still varied using the dead-angle of the inverter, so the magnitude control is required to determine the correct value of γ based on the desired value of V_{dq}^* and the actual value of the inverter's dc voltage (as determined by the STATCOM).

The relationship between the magnitude of the compensating voltage vector and the dead angle, γ , for a 24-pulse three-level inverter is defined [27] as

$$V_{dq} = \frac{2}{\pi} v_{DC} \cos\left(\frac{\pi}{24}\right) \cos \gamma \quad (4.1)$$

Since the desired output is the dead angle, by changing the subject of the formula, Equation (4.1) becomes

$$\gamma = \cos^{-1} \left(\frac{V_{dq} \pi}{2v_{DC} \cos\left(\frac{\pi}{24}\right)} \right) \quad (4.2)$$

Therefore, depending on the desired inverter ac voltage output (i.e. the commanded value of V_{dq}^*) and the actual value of V_{dc} , the controller will determine the correct value of γ based on Equation (4.2). This calculation of γ from V_{dq}^* and V_{dc} using Equation (4.2) is shown as the Dead Angle Calculator block in Fig. 4.10. The dead angle γ , is then directly output to the low level firing controls of the SSSC's inverter.

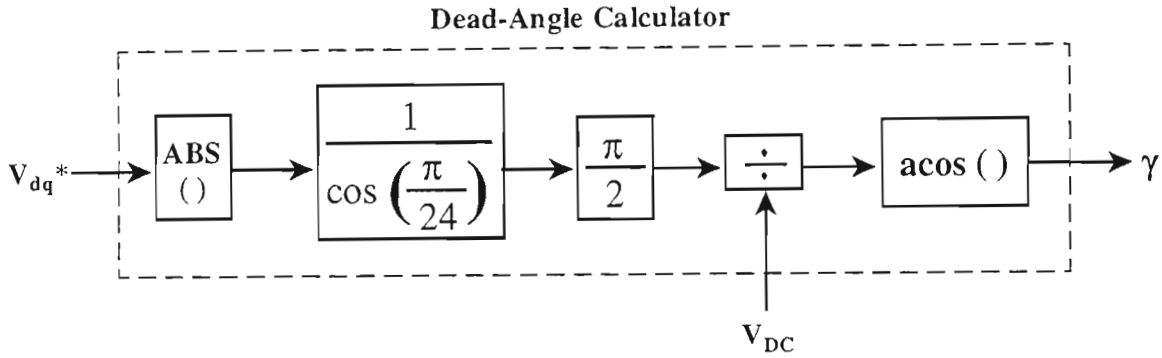


Fig.4.10: An expanded and detailed diagram of the dead angle calculator sub-block from Fig. 4.8.

4.3.3 UPFC Simulation Model In PSCAD/EMTDC

A detailed simulation model of the three-level inverter based UPFC described in the previous section has been developed in the simulation package PSCAD/EMTDC. This UPFC simulation model comprises seven main sub-modules:

- (i.) the transmission line and the coupling transformers that allow the exchange of voltages and currents with the UPFC;
- (ii.) the 24-pulse three-level inverter together with phase-shifting and adding transformers developed in Chapter Two for the SSSC implementation;
- (iii.) the 24-pulse three-level inverter together with phase-shifting and adding transformers for the STATCOM implementation where the inverter is operated as a two-level device with γ fixed at 0° ;
- (iv.) the high-level SSSC controls described in the previous section;
- (v.) the high-level STATCOM controls described in section 4.2.2;

- (vi.) the low-level inverter firing controls situated between the output of the high-level SSSC controls and the SSSC inverter;
- (vii.) the low-level inverter firing controls situated between the output of the high-level STATCOM controls and the STATCOM inverter.

Although the high-level UPFC controller in this model is based on that in [27], the UPFC model here is more detailed than [27] since all the inverter's power electronics and firing controls are represented as well as the phase shifting and adding transformers actually present in a multi-pulse inverter arrangement. This PSCAD/EMTDC model has been used to simulate the dynamic performance of the UPFC in the same study system that was considered in reference [27]. The predictions of the PSCAD/EMTDC model are then directly compared to those of the EMTP model used by Sen in [27]. The parameters for the study system are once again taken from [27], and are listed in Appendix E.1. The full details of the UPFC simulation model with all its components in PSCAD/EMTDC are shown in Appendix E.2. However, Table 4.1 shows the actual ratings of the main plant in this UPFC of [27], which are taken from those of an actual UPFC installation [15].

Table 4.1: UPFC main component ratings [15]

Component	Ratings	
Series Inverter	$\pm 160\text{MVA}$	$ V_{ac} = 0.16 \text{ pu}$
Shunt Inverter	$\pm 160\text{MVA}$	
Individual GTOs	4000A	4500V
Transmission System Voltage	138kV rms line-to-line	

4.3.4 UPFC Benchmark Results

The left hand side of Fig. 4.11 shows the dynamic response of the UPFC to changes in commanded series injection voltage V_{dq}^* and relative angle β , as simulated using the EMTP model of Sen [27], whereas the right hand side of Fig. 4.11 shows the simulated results of the UPFC to the same changes using the detailed PSCAD/EMTDC model presented in this chapter. Fig. 4.12 (a) shows the simulated results of STATCOM inverter's voltage, e_{1a} , phase a of the line voltage, V_{1a} , and the phase a shunt current, I_{1a} , in EMTDC; Fig. 4.12 (b) shows the simulated results of SSSC inverter output voltage, e_{2a} , phase a of the voltage across the series coupling transformer reactance, V_{J2a} , and the phase a line current, I_a , in EMTDC

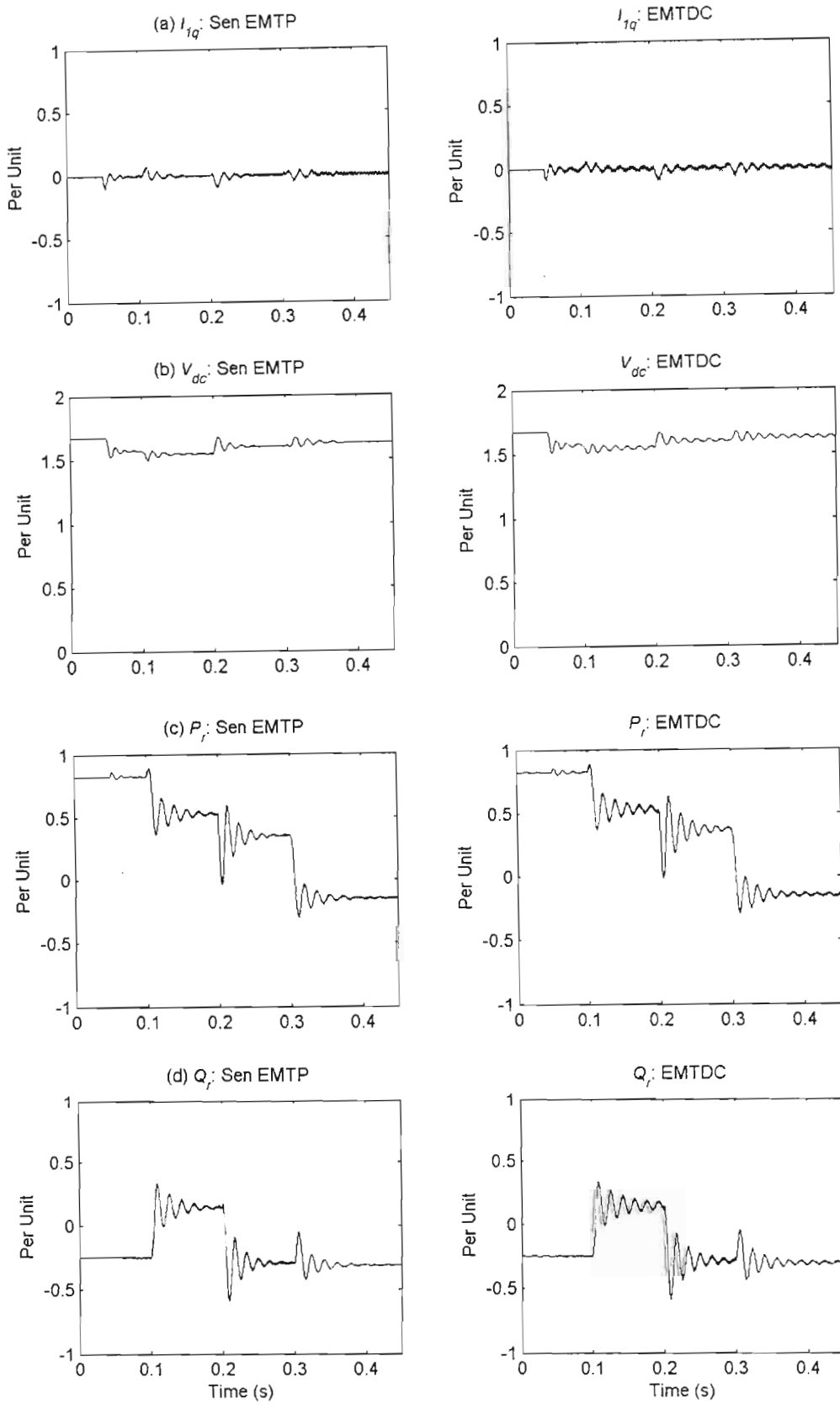


Fig.4.11: Performance of a UPFC with a 24-pulse three-level inverter, as modelled in EMTDP [27] and PSCAD/EMTDC: (a) I_{1q} ; (b) V_{DC} ; (c) P_r ; (d) Q_r .

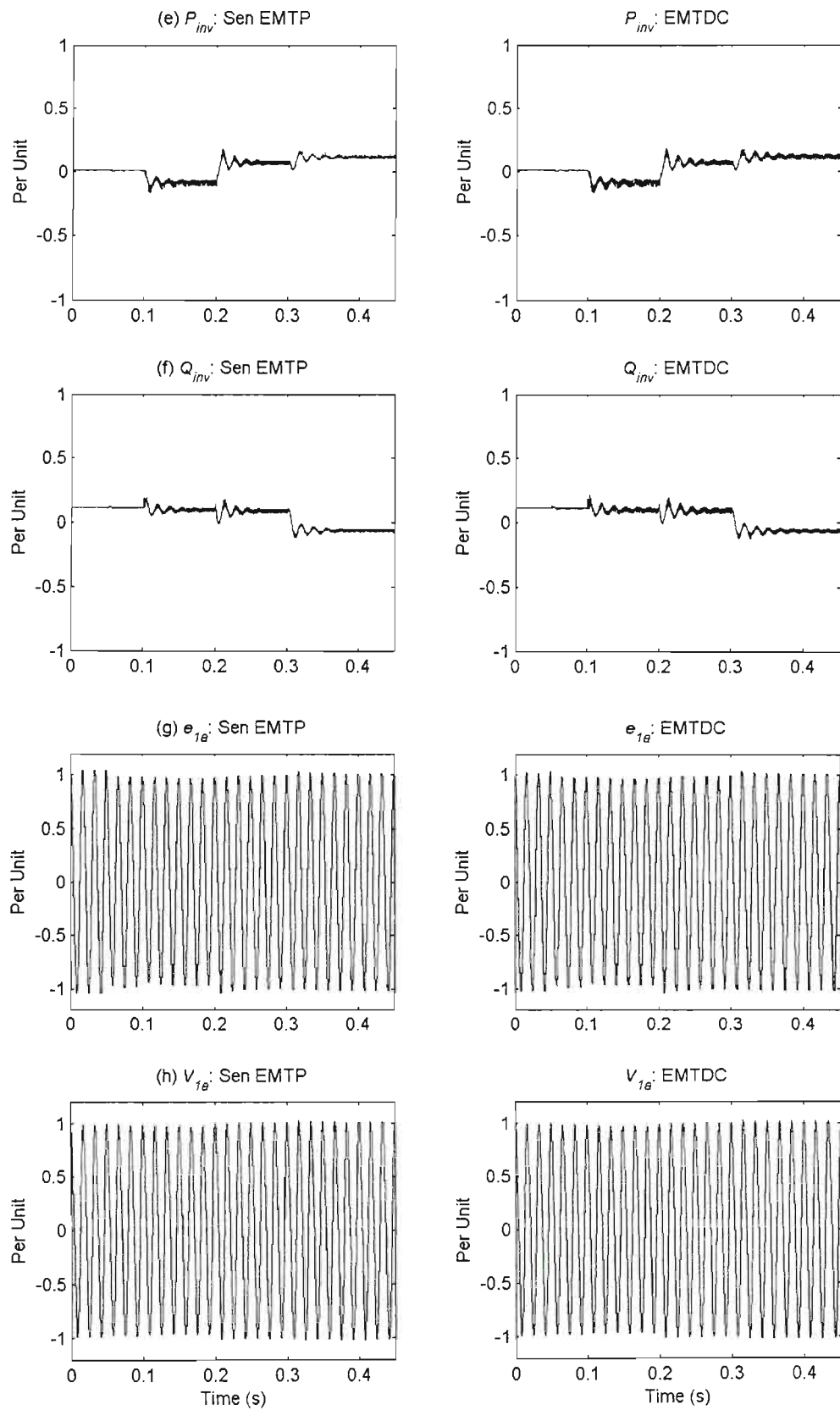


Fig.4.11 (continued): Performance of a UPFC with a 24-pulse three-level inverter, as modelled in EMTP [27] and PSCAD/EMTDC: (e) P_{INV} ; (f) Q_{INV} ; (g) e_{1a} ; (h) V_{1a} .

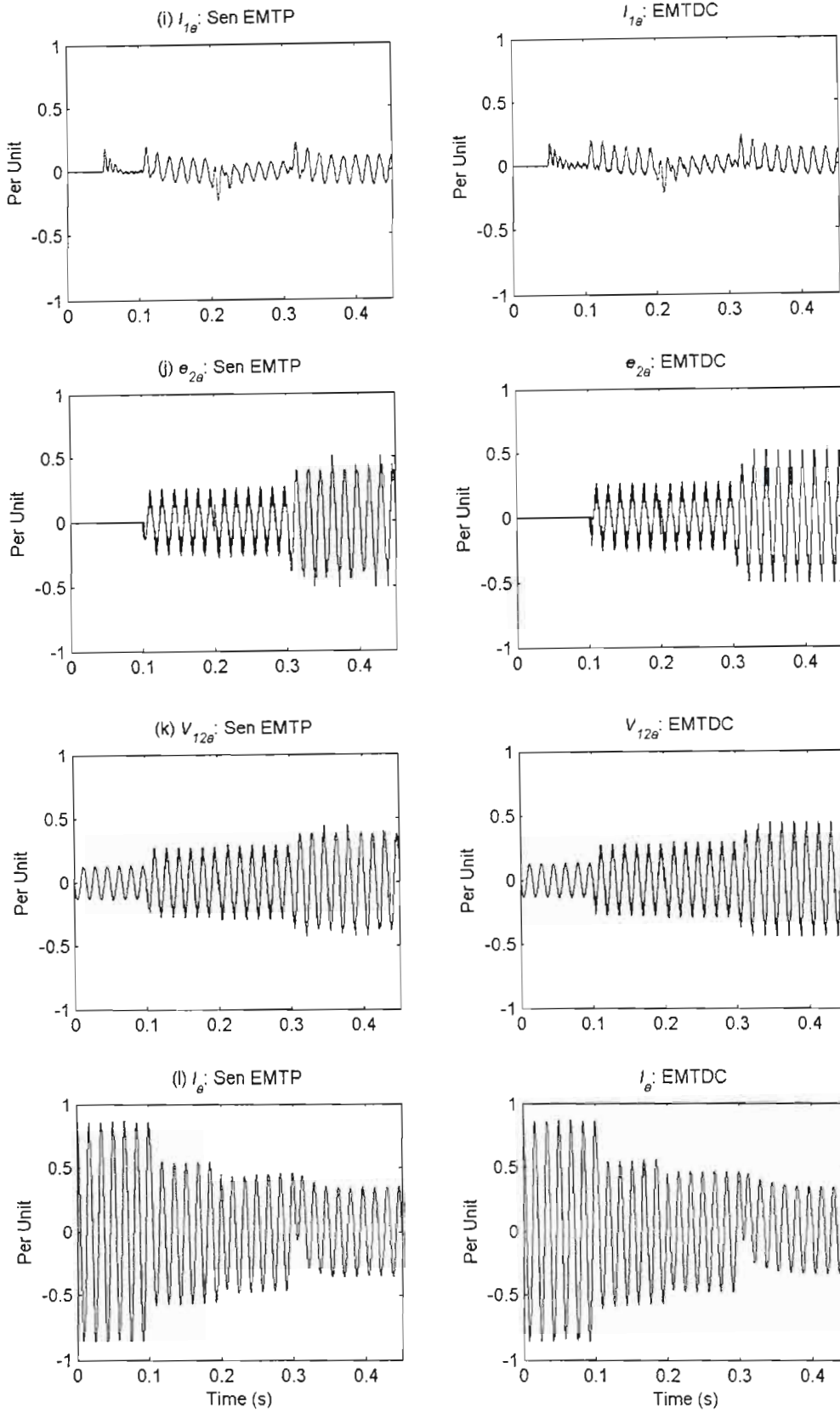


Fig.4.11 (continued): Performance of a UPFC with a 24-pulse three-level inverter, as modelled in EMTP [27] and PSCAD/EMTDC: (i) I_{1a} ; (j) e_{2a} ; (k) V_{12a} ; (l) I_a .

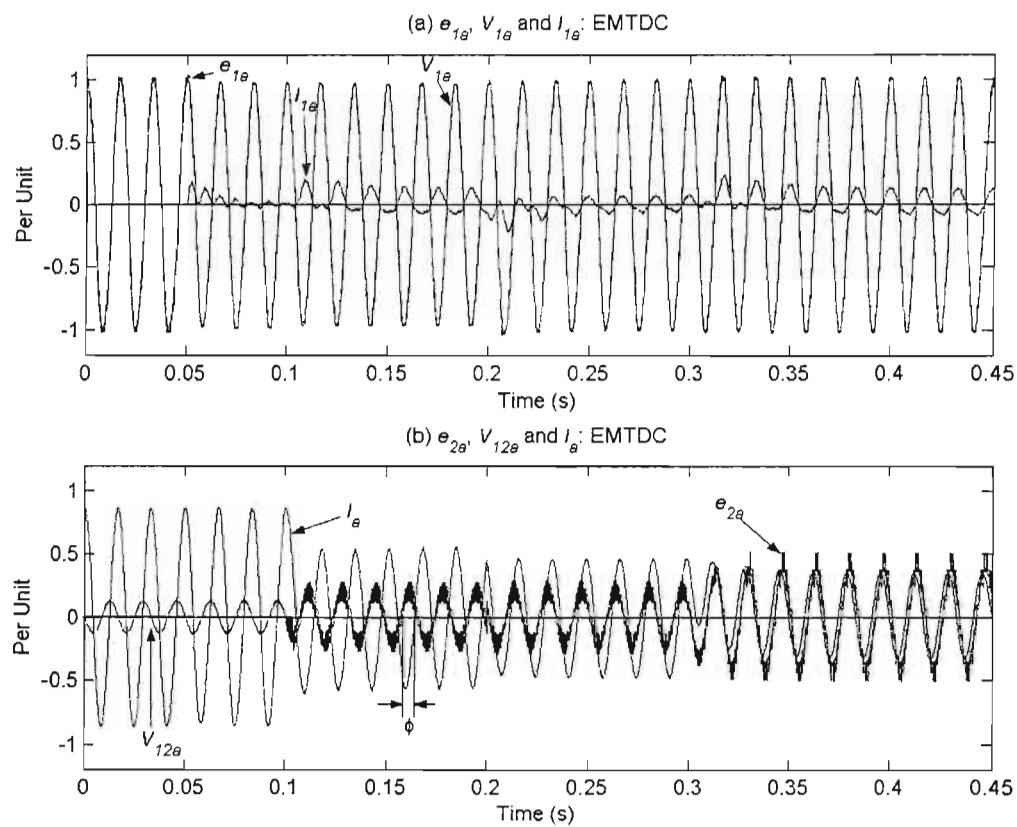


Fig.4.12: Performance of a UPFC with a 24-pulse three-level inverter, as modelled in PSCAD/EMTDC: (a) e_{1a} , V_{1a} , I_a ; (b) e_{2a} , V_{12a} , I_a .

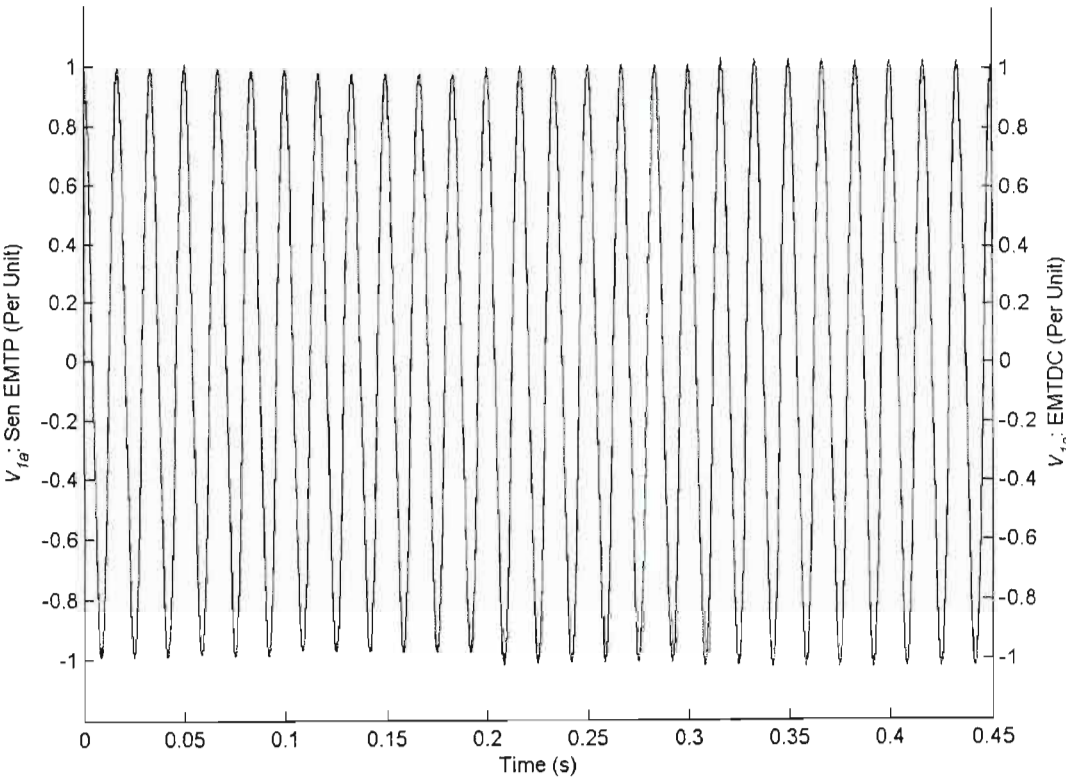


Fig.4.13: The line voltage, V_{1a} : EMTP [27] vs. PSCAD/EMTDC.

In each case the sending and receiving end voltages in the transmission line are kept at constant magnitude and the transmission angle (phase between V_s and V_r) remains fixed. The UPFC is then used to vary the active and reactive power flow in the line by changing the commanded series injection voltage V_{dq}^* and relative angle β . The commanded quadrature shunt current, I_{lq}^* , remains zero throughout this study; in other words, the STATCOM is not injecting or absorbing reactive current from the line.

From the time $t = 0$ to $t = 50\text{ms}$ in Fig. 4.11, switch S1 remains open so that the STATCOM is disconnected from the transmission system; switch S2 is closed but the SSSC does not inject any voltage; due to the inductance of the transformer $T4$, reactive power is exchanged at the point of connection; the dc capacitor is pre-charged before $t = 0$.

At $t = 50\text{ms}$, S1 closes and the commanded quadrature current is set to $I_{lq}^* = 0$. As a result of this command, the magnitudes of the STATCOM inverter voltage, e_{la} , and the system voltage, V_{la} , are same, as shown in Fig. 4.12(a). This is achieved, as shown in Fig. 4.5, by allowing active power to be transferred between the STATCOM and the line and as a result the dc capacitor voltage, V_{DC} , settles into a new steady state value.

At $t = 100\text{ms}$, the desired series injection voltage V_{dq}^* is set to 0.2 pu and the commanded relative angle is set to $\beta = 120^\circ$ leading. The dc capacitor voltage settles to a new magnitude keeping the STATCOM output voltage, e_{la} , the same magnitude as the line voltage, V_{la} . This new set of reference inputs causes the series injection voltage, e_{2a} , to lead the line current, I_a , by an angle ϕ , as shown in Fig. 4.12(b) meaning that the injected voltage vector is in the inductive domain. The reactive power, Q_{INV} , at the point of SSSC connection remains positive as shown in Fig. 4.11(f). Furthermore, because the angle ϕ is larger than 90° , the SSSC is also emulating a negative resistance, requiring active power to be injected in series with the line, such that P_{INV} is now negative as shown in Fig. 4.11(e), and the source of this active power flow is from bus 1, through the STATCOM. This is evident in Fig. 4.12(a) which shows that the STATCOM output voltage, e_{la} , is almost 180° out of phase with the shunt current, I_{la} , so that active power may be absorbed at the STATCOM terminals. Fig. 4.11(c) shows that the active power, P_r , at the receiving end of the line decreases. Fig. 4.11(d) shows that the reactive power, Q_r , that flows to the receiving end of the line is now inductive.

With the injected voltage magnitude V_{dq}^* kept constant at 0.2 pu, the desired relative angle β is now stepped down to 60° at $t = 200\text{ms}$. The series injected voltage, e_{2a} , still leads the line current, I_a , at this new operating point, which means that the injecting voltage vector remains in the inductive domain. The reactive power, Q_{INV} , at the point of SSSC connection stays positive

as shown in Fig. 4.11(f). However, the angle ϕ is now smaller than 90° , which means that the SSSC is emulating a positive resistance. This requires active power to be absorbed from the line by the SSSC such that, P_{INV} is now positive as shown in Fig. 4.11(e), and this real power flows to bus 1 via the STATCOM. This can be seen in Fig. 4.12(a) which shows that the STATCOM output voltage, e_{1a} , is now in phase with the shunt current, I_{1a} , so that active power is released from the UPFC. This new β setting further decreases the real power, P_r , transferred down to the receiving end of the line as shown in Fig. 4.11(c), and the reactive power, Q_r , that flows to the receiving end of the line is now capacitive.

At $t = 300$ ms, the relative angle β is maintained at 60° while the injected voltage magnitude V_{dq}^* is stepped up to 0.4 pu. The effect of this new setting is that the series injected voltage, e_{2a} , now lags the line current, I_a , as shown in Fig. 4.12(b), which suggests that SSSC is partially emulating a capacitive reactance. The reactive power, Q_{INV} , at the point of SSSC connection is now negative as shown in Fig. 4.11(f). With the angle ϕ still smaller than 90° , the SSSC is still emulating a positive resistance and therefore absorbs active power from the line. P_{INV} has increased due to the increase in the injected voltage magnitude. Fig. 4.12(a) also shows that more shunt current, I_{1a} , is flowing out to the line. With this new V_{dq}^* setting the direction of the active power flow in the transmission line itself now reverses as shown in Fig. 4.11(c), while the reactive power, Q_r , remains capacitive.

A close comparison between the results in Fig. 4.11 has shown that the response predicted by Sen's EMTP model in [27] and that predicted by the detailed PSCAD/EMTDC model developed in this thesis are virtually identical, thus confirming the correctness of the latter model. Fig. 4.13 illustrates this close agreement for one particular system variable: the transmission line voltage V_{1a} at bus 1 predicted by each of the models is plotted on the same axes in Fig. 4.13 for comparison.

4.4 Conclusion

A detailed model of both a stand-alone, two-level static synchronous compensator and a three-level unified power flow controller have been developed in the simulation package PSCAD/EMTDC. In the two-level STATCOM model, the inverter output voltage is controlled by varying the inverter dc voltage. The desired shunt current that flows between the STATCOM and the transmission line will determine the inverter's output voltage magnitude in relation to the line voltage. This will in turn influence the reactive power being exchanged at the point of

connection. In the three-level inverter based UPFC model, the STATCOM is operated as a two-level device (with $\gamma = 0^\circ$) and has the sole control over the dc link capacitor voltage. The SSSC as a part of the UPFC is then allowed to inject a voltage that is a two-dimensional vector quantity [14]; in other words, it is able to not only influence the reactive power in the line but also the active power depending on the mode of operation. The magnitude of this series injection voltage is controlled by varying the dead angle γ , thus varying the inverter gain. In both simulation models, the inverter's power electronics and associated transformers are represented in detail using the model described in Chapter Two.

The results from the stand-alone STATCOM model and the UPFC model developed in PSCAD/EMTDC have been shown to be virtually identical to those simulated in EMTP by Sen [27], and therefore confirm the correctness of the more detailed STATCOM and UPFC models developed in PSCAD/EMTDC.

Since the benchmarked results of the stand-alone STATCOM and the UPFC models presented in this chapter have been shown to be correct, the PSCAD/EMTDC models of these devices can be used to analyse their characteristics and interactions with other plant in the power system in future work. The following chapter will describe the development of SSSC, STATCOM and UPFC simulation models using a simplified, continuous-time model of the inverter.

CHAPTER FIVE

CONTINUOUS-TIME MODEL OF INVERTER-BASED FACTS DEVICES FOR PSCAD/EMTDC

5.1 Introduction

Chapter Three and Chapter Four described the detailed modelling of three inverter based FACTS devices, namely, the SSSC, STATCOM and UPFC, based on the 24-pulse, three-level voltage-sourced inverters developed in Chapter Two in the simulation package PSCAD/EMTDC. The 24-pulse, three-level inverter model developed includes actual power electronics and associated low-level firing controls, and it has been shown to output high quality, near-sinusoidal voltages suitable for high-power FACTS applications.

Although in some cases it is necessary to use highly detailed models as in [78] to predict interactions between the SSSC and the rest of the system, these models are nevertheless cumbersome and require a large amount of simulation time. A simplified, continuous-time model of a voltage-sourced inverter has therefore been developed to allow simulation studies on FACTS devices to be carried out more rapidly. One of the attractions of this modelling approach is that it will allow for more rapid analysis and debugging of high-level control schemes that are present in these inverter-based FACTS devices, at least in the initial development phase. In addition, for detailed analysis of issues like SSR, this continuous-time representation of the inverter allows the FACTS device model to be linearised about a particular steady state operating point so that eigenvalue analysis can be done. In the case of some FACTS device studies, it may even be possible to avoid using detailed inverter models without suffering too much loss in accuracy.

This chapter therefore presents a simplified, continuous-time model of a voltage-sourced inverter that has been developed for the simulation package PSCAD/EMTDC. This simplified inverter model is then used for the development of SSSC, STATCOM and UPFC models. In a similar manner to Chapter Three and Chapter Four, the high level controls for the SSSC are taken from reference [34], and the high level controls for the STATCOM and UPFC are taken from reference [27]. For the purpose of benchmarking, the SSSC, STATCOM and UPFC models based on the

simplified inverter representation described in this chapter will be compared to those based on the detailed multi-level inverter models presented in Chapter Three and Chapter Four.

5.2 Continuous-Time Model of Voltage-Sourced Inverter

The basic building block of an inverter-based FACTS device is the voltage-sourced inverter shown schematically in Fig. 5.1.

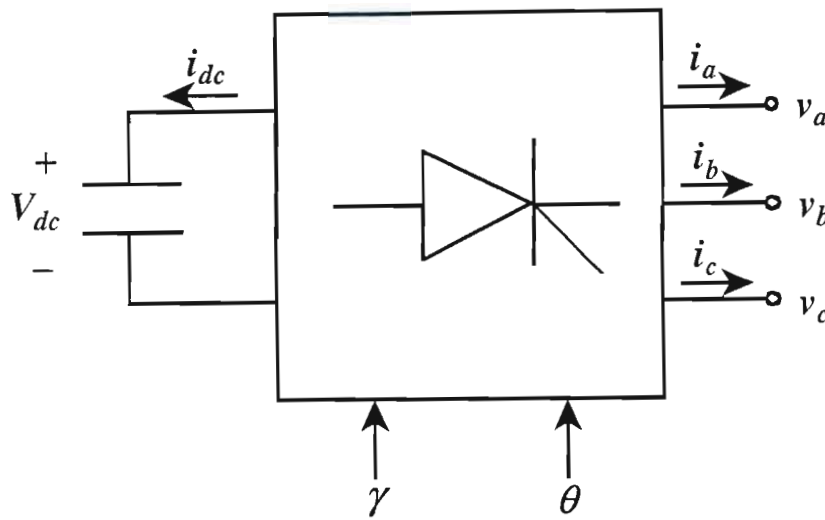


Fig. 5.1: Voltage-sourced inverter.

In transmission FACTS devices such as the SSSC, STATCOM and UPFC, the inverter itself is typically a multi-pulse square wave inverter. The inverter converts a dc voltage, V_{dc} , at its input to instantaneous three-phase voltages, v_a , v_b and v_c at its output; the instantaneous angle of the three-phase voltage set is determined by the control input θ to the inverter. In addition, depending on the type of FACTS device, the inverter may be a two-level device (i.e. fixed dc-to-ac voltage gain) or a three-level device (variable dc-to-ac voltage gain). In the case of a three-level inverter, there is a further control input, namely the dead angle, γ , that is used to adjust the dc-to-ac inverter gain. When the dead angle $\gamma = 0^\circ$, the three-level inverter resembles a two-level inverter.

For the purpose of consistency, the simplified inverter model considered in this chapter is also a three-level, 24-pulse device for which the gain K_{INV} between the dc input voltage and the fundamental component of the ac output voltage is a function of γ given by [27] as

$$K_{INV} = \frac{|v_{abc}|}{V_{dc}} = \frac{2}{\pi} \cos\left(\frac{\pi}{24}\right) \cos \gamma \quad (5.1)$$

In Chapter Two, a model was developed in PSCAD/EMTDC of a three-level, 24-pulse voltage-sourced inverter with the power electronic switches and low-level firing controls of the inverter represented in detail. However, this model of the inverter can be greatly simplified by neglecting the non-fundamental frequency components in the ac output voltages and assuming that the inverter is an ideal dc to ac voltage gain, K_{INV} , with K_{INV} being a function of the control input γ as shown in equation (5.1). With this approach it is possible to neglect all the power electronic devices in the inverter as well as their low-level firing control circuits, thus greatly reducing the computational burden in the simulation.

However, if the actual power-electronic circuit connecting the ac and dc sides of the inverter is neglected, it is necessary to describe the energy transfer process across the inverter by means of an equivalent model.

When considering the ac side of the inverter, as mentioned, the inverter outputs instantaneous voltages v_a , v_b and v_c that are determined by the control inputs γ and θ , the dc voltage V_{dc} at its input, and the gain K_{INV} . Thus, in the continuous-time equivalent model, the output ac voltage equations of the inverter are given by

$$v_a = K_{INV} * V_{dc} * \sin \theta \quad (5.2)$$

$$v_a = K_{INV} * V_{dc} * \sin\left(\theta - \frac{2\pi}{3}\right) \quad (5.3)$$

$$v_a = K_{INV} * V_{dc} * \sin\left(\theta + \frac{2\pi}{3}\right) \quad (5.4)$$

On the dc side of the inverter, the dc voltage V_{dc} may (depending on the application) be supplied from a charged capacitor, a battery, or from the dc voltage of another inverter. In any case, it is necessary to model the charging and discharging characteristics on the dc side of the inverter. At any instant in time, the instantaneous active power P_i at the ac terminals of the inverter is given by

$$P_i = v_a * i_a + v_b * i_b + v_c * i_c \quad (5.5)$$

where i_a , i_b and i_c are the instantaneous currents flowing in the three ac output phases of the inverter.

Assuming the inverter to be an ideal, lossless device, this active power P_i (either positive or negative) must be supplied instantaneously from the energy storage device providing the input voltage V_{dc} to the inverter. In the continuous-time equivalent model of the inverter, this energy transfer from the dc side of the inverter is represented as a current injection I_{dc} into the dc terminals of the inverter. At each instant in time this current injection I_{dc} is calculated as

$$I_{dc} = \frac{P_i}{V_{dc}} \quad (5.6)$$

where V_{dc} is the instantaneous voltage at the dc terminals of the inverter.

The next section will now describe the implementation of this continuous-time inverter model in the simulation package PSCAD/EMTDC by using the equations for the 24-pulse, three-level inverter shown in this section.

5.3 Continuous-Time Inverter Model In PSCAD/EMTDC

This thesis, in its entirety, has developed all its inverter-based FACTS device models in the simulation package PSCAD/EMTDC. The PSCAD/EMTDC software program was originally developed for studying HVDC systems. However, over the years many models and capabilities have been added and at present PSCAD/EMTDC is now a versatile tool to study AC as well as DC power systems problems [56]. PSCAD/EMTDC comprises two modules: the EMTDC computing engine itself and the PSCAD design environment in which the power system to be simulated is constructed graphically from a block diagram library of pre-coded components and models; the parameters of each model are entered by the user in the PSCAD environment via dialogue boxes that are associated with each component's block diagram.

PSCAD/EMTDC, however, also offers the facility for users to design their own customized components in the form of user-defined models written in FORTRAN code. Introducing a new, user-defined model to the program requires three main development steps.

1. Designing a PSCAD functional block diagram representation, together with the necessary parameter dialogue boxes, for the new model; these will then appear in the block diagram component library;
2. Carrying out the necessary programming within PSCAD to allow interfacing of the new component's functional block diagram to the model itself in the EMTDC computing engine;
3. Programming the necessary equations of the model in a subroutine that will be called by the EMTDC computing engine at each time step during a simulation.

Within a user-defined component in PSCAD, it is possible to define programmable current and voltage sources to supply the electrical output terminals of the model, with the equations for these current and voltage sources then written in FORTRAN code. It is also possible to define, as inputs to the user-defined model, either control variables or electrical measurements (voltages and currents) from an external network. Similarly, the user-defined models are able to supply the external circuit with control variables and electrical measurements as outputs if so desired.

The user-defined continuous-time inverter model of a three-level, 24-pulse voltage sourced inverter is defined to have eight electrical terminals and two control input terminals as shown schematically in Fig. 5.2.

At the dc electrical terminals the voltage V_{dc} applied to the inverter is measured as an input to the model while at the AC terminals the currents i_a , i_b and i_c in the inverter's three-phases are also measured as inputs. Finally, the variables γ and θ , from a high-level inverter controller are imported as control inputs to the user-defined model.

The facility that allows users to design their own customized components in PSCAD/EMTDC, as previously mentioned, is a program within PSCAD/EMTDC called the Component Wizard [80]. The continuous-time inverter model described in the previous section has been developed as a user-defined model in PSCAD/EMTDC by using this program. The Component Wizard aided in creating a continuous-time inverter functional block whose property is divided into three main sections, namely, the Graphics, Parameter and SectionsNode sections. The Graphics section allows the user to create the visual graphics of the new component; a simplified inverter functional block similar to that in Fig. 5.2 is created in this section. The Parameter section allows the user to enter any required parameters related to the functionality of the component. This particular section is left blank as it is not a design requirement for the simplified inverter model. The SectionsNode section holds all the necessary code for the designed component that to be calculated by the EMTDC simulation engine at each time step. The code for current

injection, I_{dc} , which is responsible for representing the charging and discharging characteristics of the dc capacitor, is placed in this particular section (i.e. equations (5.5) and (5.6)). The necessary parameters and variables are then passed in between the SectionsNode section and a separate subroutine that contains the code for the ac voltage sources (based on the equations (5.1), (5.2), (5.3), and (5.4)). The subroutine is then called by the EMTDC computing engine for simulation. At each simulation step, these equations (coded in FORTRAN) are solved and used to calculate the correct electrical values of the inverter model, namely, v_a , v_b and v_c and I_{dc} . Finally, the user-defined voltage and current sources in the inverter model are updated with these calculated values of v_a , v_b and v_c and I_{dc} and these are passed to the main EMTDC solution of whatever external electrical network is connected to the user-defined inverter model (on both its dc and ac sides).

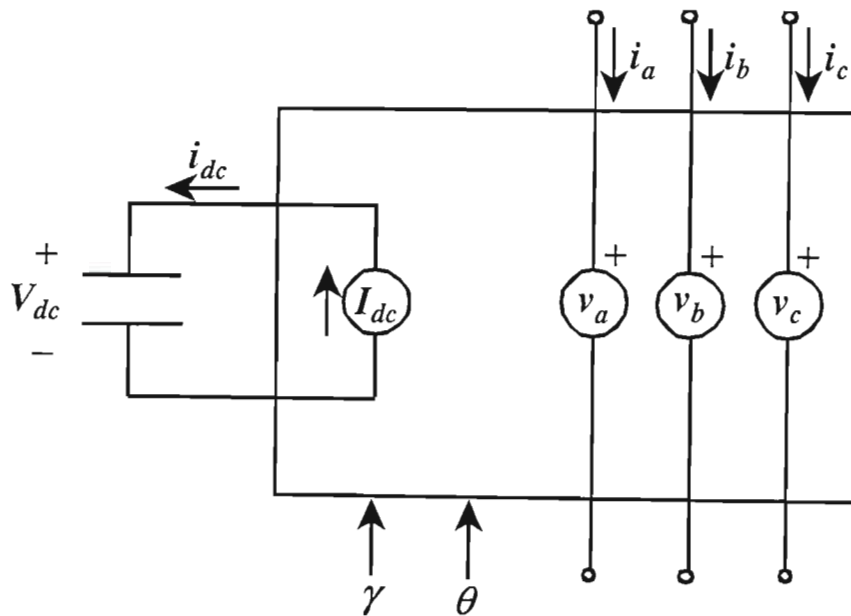


Fig. 5.2: Schematic representation of the continuous-time inverter model developed in PSCAD/EMTDC.

The full details of the design of the continuous-time inverter model with all its components and embedded code in PSCAD/EMTDC are shown in Appendix F.1.

The following section compares some of the SSSC, STATCOM and UPFC time domain results produced by the simplified PSCAD/EMTDC model developed in this chapter with the results from the detailed models in Chapter Three and Chapter Four. Appendix F.2 then also presents a more detailed performance study of the SSSC, using the simplified model, to determine if the SSSC's characteristics at subsynchronous frequencies are retained in the simplified model.

5.4 Continuous-Time Inverter-Based FACTS Devices: Benchmark Results

For the purpose of showing the correctness of the continuous-time inverter model, it was used to construct SSSC, STATCOM and UPFC simulation models; the results generated using these simplified FACTS device models were then compared to the results obtained from similar studies obtained using the detailed inverter model already shown in Chapter Three and Chapter Four. The high-level control of these inverter-based FACTS devices and system layout was in each case the same for the simplified model studies as those described in the previous two chapters. In the case of the simplified SSSC model, only the two-level SSSC controls will be considered in this section.

5.4.1 SSSC

Fig. 5.3 shows a comparison of the dynamic performance of an SSSC obtained using the simplified inverter model of this chapter and the detailed inverter model of Chapter Three. The simulation study is similar to that shown in Figs. 3.9 and 3.10 of Chapter Three.

Figs. 5.3(a) and (b) show the dynamic response of the SSSC output ac voltage, e_{2a} , and the phase a line current, i_a , respectively. The SSSC is initially operating at steady state with $X_q^* = 0.3$ pu inductive, which has resulted in e_{2a} leading i_a by almost 90° . At $t = 300$ ms, the commanded reactance X_q^* is adjusted to 0.1pu capacitive, such that the inverter output voltage, e_{2a} , now lags the line current, i_a , by almost 90° ; since the total line reactance is now lower than the uncompensated value, the current increases in magnitude as expected.

In Fig. 5.3(a) the ac output voltage of the detailed SSSC model shows a 24-pulse quasi harmonic neutralized waveform obtained from combining output voltages of four 6-pulse inverters by means of a magnetic adding circuit. This stair-cased waveform exhibits voltages of fundamental and odd harmonic components. By contrast, the simplified SSSC model outputs the voltage of only the fundamental component. However, Fig. 5.3(a) nevertheless shows that this fundamental component of the SSSC voltage corresponds closely to the output voltage of the detailed SSSC model both at steady state and under dynamic conditions.

Fig. 5.3(b) shows the behaviour of the transmission line current predicted using the two SSSC models: the two currents are virtually identical, further confirming the correctness of the simplified SSSC model.

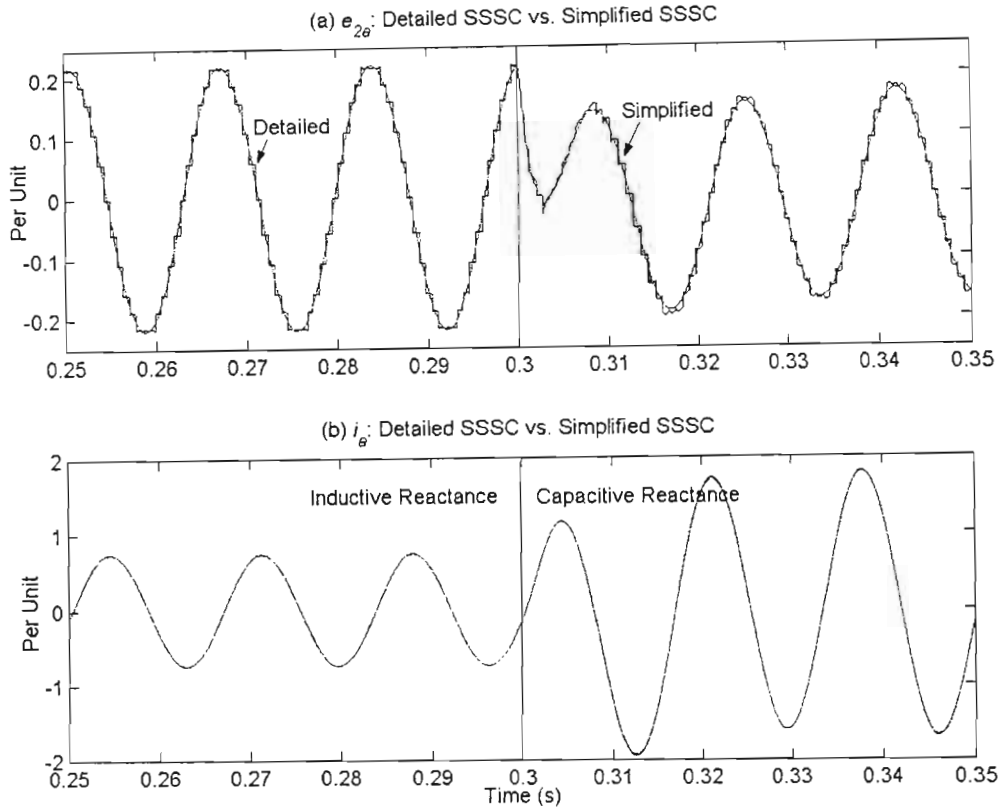


Fig. 5.3: Performance of both the detailed and simplified SSSC models operating in Inductive and Capacitive modes as simulated in PSCAD/EMTDC: (a) $e_{2\theta}$; (b) i_{θ} .

5.4.2 STATCOM

Fig. 5.4(a) shows a comparison of the dynamic performance of a STATCOM obtained using the simplified inverter model of this chapter and the detailed inverter model of Chapter Four. The simulation study is similar to that shown in Fig. 4.5(h) of Chapter Four.

Fig. 5.4(a) shows the dynamic response of the simplified STATCOM output ac voltage, e_{1a} , the line voltage, V_{1a} , and the phase a shunt current, I_{1a} , simulated in PSCAD/EMTDC. Before time $t = 175\text{ms}$, the commanded quadrature component of the inverter current, I_{1q}^* , is 1 pu capacitive and this has resulted in the magnitude of the STATCOM output voltage, e_{1a} exceeding that of the line voltage, V_{1a} . At $t = 175\text{ms}$, the commanded quadrature current, I_{1q}^* , is adjusted to 1 pu inductive, so that the inverter output voltage, e_{1a} , is now lower than the system voltage, V_{1a} .

Fig. 5.4(b) shows the behaviour of the transmission line voltage at the point of STATCOM

connection predicted using the two STATCOM models: the two voltages are virtually identical, further confirming the correctness of the simplified STACOM model.

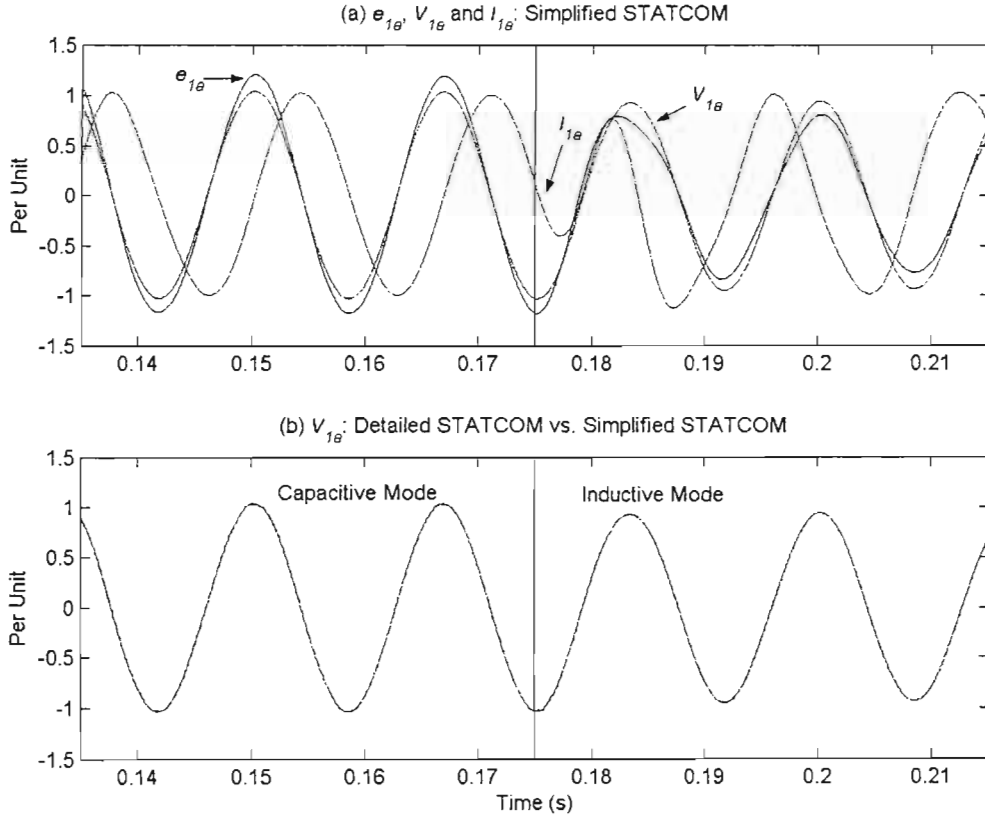


Fig. 5.4: (a) Performance of simplified STATCOM model operating in Inductive and Capacitive modes as simulated in PSCAD/EMTDC: e_{1a} , V_{1a} and I_{1a} .

(b) Performance of line voltage, V_{1a} , in both the detailed and simplified STATCOM models operating in Inductive and Capacitive modes.

5.4.3 UPFC

Fig. 5.5 shows a comparison of the dynamic performance of a UPFC obtained using the simplified inverter model of this chapter and the detailed inverter model of Chapter Four. The simulation study is similar to that shown in Fig. 4.12 of Chapter Four.

Before time $t = 200\text{ms}$, the commanded series injection voltage V_{dq}^* is set to 0.2 pu and the commanded relative angle is set to $\beta = 120^\circ$ leading. The STATCOM output voltage, e_{1a} , is at the same magnitude as the line voltage, V_{1a} . This set of reference inputs causes the series

injection voltage, e_{2a} , to lead the line current, I_a , by an angle ϕ , shown in Fig. 5.5(b), meaning that the injected voltage vector is in the inductive domain. Also, because the angle ϕ is larger than 90° , the SSSC is emulating a negative resistance. The active power is injected in series with the line by delivering real power from the STATCOM terminals through the dc link capacitor. Because of this, the STATCOM output voltage, e_{1a} , is almost 180° out of phase with the shunt current, I_{1a} , so that active power may be absorbed at the STATCOM terminals.

At $t = 200\text{ms}$, the injected voltage magnitude V_{dq}^* is kept constant at 0.2 pu, but the commanded relative angle β is now stepped down to 60° . The magnitude of the STATCOM output voltage, e_{1a} , remains the same as the line voltage, V_{1a} . The series injection voltage, e_{2a} , is still leading the line current, I_a , which means that the injected voltage vector remains in the inductive domain. However, the angle ϕ is now smaller than 90° , which means that the SSSC is emulating a positive resistance. This requires active power to be absorbed from the line by the SSSC, and this real power flows to the point of STATCOM connection. This is evident in Fig. 5.5(a) which shows that the STATCOM output voltage, e_{1a} , is now in phase with the shunt current, I_{1a} .

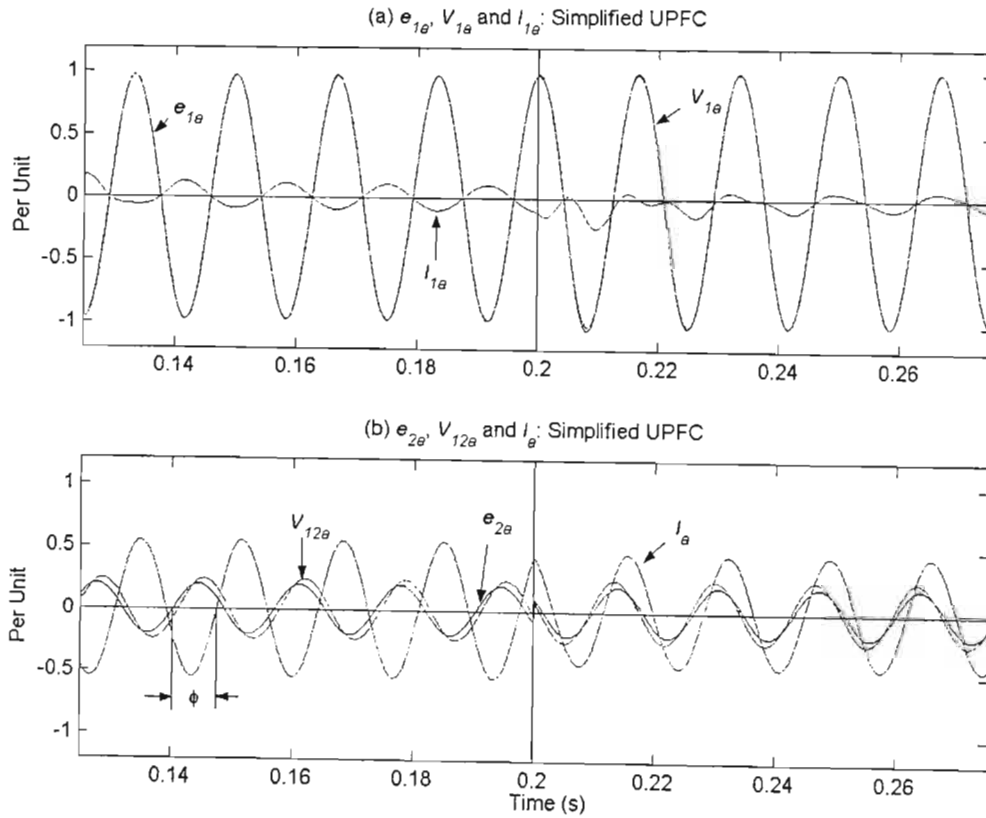


Fig. 5.5: Performance of simplified UPFC model operating in Voltage Injection mode as simulated in PSCAD/EMTDC: (a) e_{1a} , V_{1a} and I_{1a} ; (b) e_{2a} , V_{12a} and I_a .

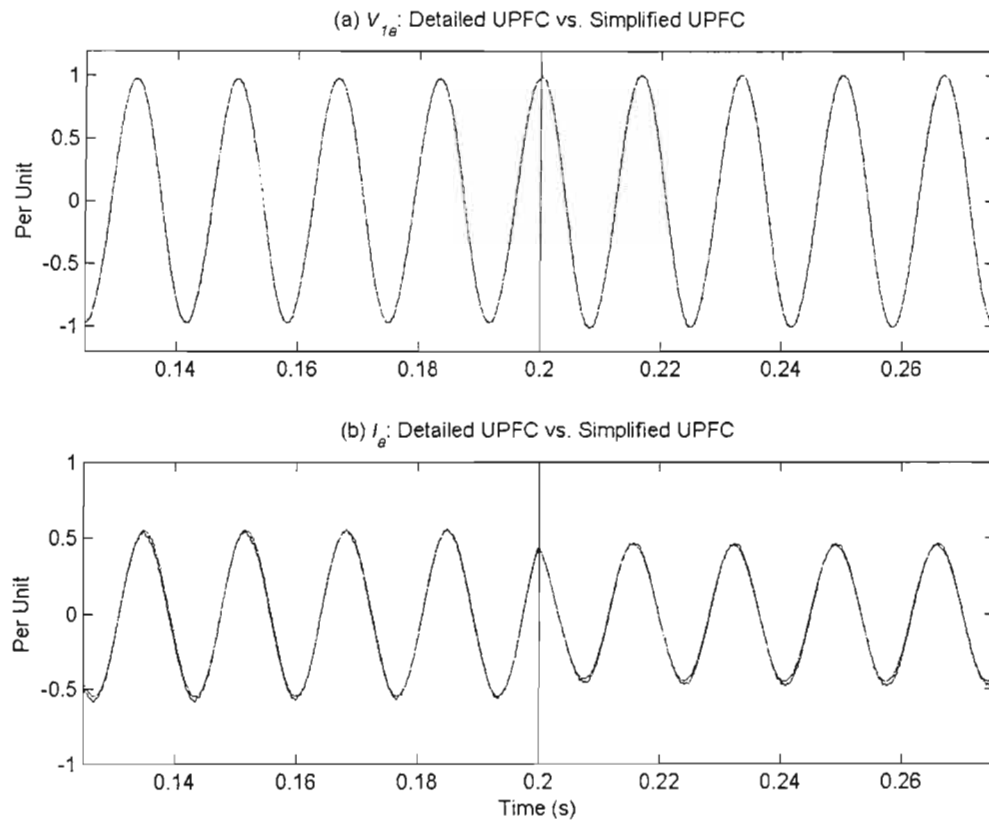


Fig. 5.6: Performance of both the detailed and simplified UPFC models operating in Voltage Injection mode as simulated in PSCAD/EMTDC: (a) V_{la} ; (b) I_a .

Fig. 5.6 presents a close-up view of part of the same dynamic response test shown in Fig. 5.5, generated for the purpose of close comparison between the detailed UPFC model and the simplified continuous-time UPFC model presented in this section. Fig. 5.6(a) and (b) show the behaviour of the transmission line voltage, V_{la} , at the point of STATCOM connection and the line current, I_a , respectively. The predicted results using the two UPFC models have been shown to be virtually identical, further confirming the correctness of the simplified UPFC model.

5.5 Conclusion

This chapter has presented a continuous-time model of a voltage-source inverter developed for the simulation package PSCAD/EMTDC. This simplified inverter model is aimed to output a continuous-time waveform that exhibits only the fundamental frequency component of the actual inverter voltages. The magnitude of this output voltage is based on the measured dc capacitor

voltage and the required dead angle γ . This chapter has also described the process used to design such an inverter model in PSCAD/EMTDC.

This continuous-time inverter model was then used to develop simplified SSSC, STATCOM and UPFC models, the results of which have been shown to be very similar to those obtained from the detailed models in Chapter Three and Chapter Four, and therefore validate the accuracy of these simplified inverter-based FACTS models. Simplified, continuous-time models of FACTS devices such as those presented in this chapter can also be linearised and used for eigenvalue analysis. However, the main focus of the investigations in this thesis has been to develop detailed models of FACTS devices based on the actual power-electronic topologies typically used in practice in high-powered FACTS applications. Thus, when conducting the analyses in the rest of the thesis, the full detailed FACTS device models are used. However, the continuous-time models presented and benchmarked in this chapter could form the basis on which to develop linearised models of the FACTS devices for future eigenvalue studies.

There are two aspects to the study of inverter-based FACTS devices in this thesis, namely mathematical modelling and performance analysis of these devices. Chapter Two described the design of a detailed 24-pulse, three-level inverter model which includes the actual representation of power electronics and associated low-level firing controls. Chapter Three described the modelling of a two-level and three-level SSSC based on the voltage-sourced inverter model developed in Chapter Two. Chapter Four similarly described the development of detailed simulation models of two other inverter-based FACTS devices, namely, the STATCOM and UPFC. Finally, Chapter Five has presented the development of a continuous-time inverter model used to derive simplified SSSC, STATCOM and UPFC models: the end of this chapter therefore concludes the mathematical modelling aspects of the thesis.

The next chapter marks the beginning of the performance analysis of inverter-based FACTS devices in the thesis, and specifically considers the frequency-domain impedance characteristics of a transmission line compensated with a two-level SSSC, and examines the possibility of this form of compensation giving rise to harmful resonances.

CHAPTER SIX

RESONANT CHARACTERISTICS OF THE ELECTRICAL COMPENSATION PROVIDED BY A TWO-LEVEL SSSC

6.1 Introduction

Chapter Three of this thesis described the development of two detailed SSSC models, each incorporating the same 24-pulse three-level inverter, but with different control schemes. In the first part of Chapter Three, the gain across the inverter is fixed (by setting $\gamma = 0^\circ$) and the output ac compensating voltage is varied by adjusting the inverter dc voltage; in the second part, the dc voltage is kept fixed at some desired value and the output ac voltage is varied by changing the dead angle γ and therefore the inverter gain. Both SSSC models have been benchmarked against known results from the literature. Chapter Three then demonstrated that with the three-level SSSC, the inverter dc voltage might be adjusted by the operator to vary the dead angle γ , and therefore minimize the total harmonic content that is injected into the transmission system.

Although the two SSSC models have been shown to perform correctly under various steady state operating conditions at the transmission line frequency of 60Hz, the characteristics of the SSSC's compensating reactance have not yet been considered at other frequencies. The frequency-domain characteristics of the SSSC are of interest due to concern for whether or not an SSSC has the potential to excite subsynchronous resonance (SSR). It is commonly known that when a conventional dielectric capacitor is used to compensate an RL transmission line to reduce its series reactance, the transmission line becomes a resonant RLC network. An SSSC, on the other hand, replaces a physical capacitor by injecting ac voltages that emulate the behaviour of capacitive reactance in series with the line. The answer to whether or not this, too, constitutes a resonant RLC network requires a detailed examination of the electrical impedance characteristics of the compensator in the frequency domain.

This chapter therefore investigates the resonant characteristics of the compensation provided by the *two-level* SSSC developed in Chapter Three. These investigations include examining the impedance versus frequency characteristics of a transmission line compensated with the SSSC for different ohmic reactance settings of the SSSC, and comparing these with the characteristics of

conventionally compensated lines. The investigations also include an examination of the performance of the SSSC in a benchmark system for the study of SSR [72]. It is hoped that these studies can provide a clearer understanding of the behaviour of the SSSC as an equivalent impedance element in the transmission line, and therefore identify the possible risk of SSR.

6.2 Subsynchronous Resonance (SSR)

6.2.1 Introduction

When series capacitance is inserted into a transmission line to increase the power transfer capability, it forms a resonant circuit with the line resistance and inductance which resonates at its natural electrical frequency after a change in system variables. Under such conditions, the interaction between a turbine-generator and a series compensated transmission line may lead to a form of dynamic instability called subsynchronous resonance (SSR) [18]. SSR has been formally defined by the IEEE Subsynchronous Resonance Working Group [81] as *"...encompassing the oscillatory attributes of electrical and mechanical variables associated with turbine-generators when coupled to a series capacitor compensated transmission system..."*.

In the presence of SSR the turbine shafts are subjected to large amplitude torque oscillations. These torque oscillations not only have the potential to cause shaft fatigue and shorten the life of the turbine, they can also cause shaft failure as illustrated by two famous incidents at Mohave Power Station in Nevada, U.S.A. [82]. It is therefore important to understand the effect that an SSSC will have on the transmission system before actual implementation of such a device, even though no physical capacitors are placed in series with the transmission line.

6.2.2 Mechanisms Of SSR

As previously described, when a conventional capacitor is used to compensate an RL transmission line to reduce its series reactance, the transmission line becomes a resonant RLC network. The line therefore exhibits a resonant minimum in its impedance at a natural frequency f_{er} given as

$$f_{er} = f_0 \sqrt{\frac{X_c}{X_L}} = \frac{1}{2\pi\sqrt{LC}} \quad (6.1)$$

where

f_0 is the synchronous frequency of the system;

$X_L = 2\pi f_0 L$ is the inductive reactance of the line at the system frequency; and

$X_c = \frac{1}{2\pi f_0 C}$ is the capacitive reactance inserted in series with the line at the system frequency.

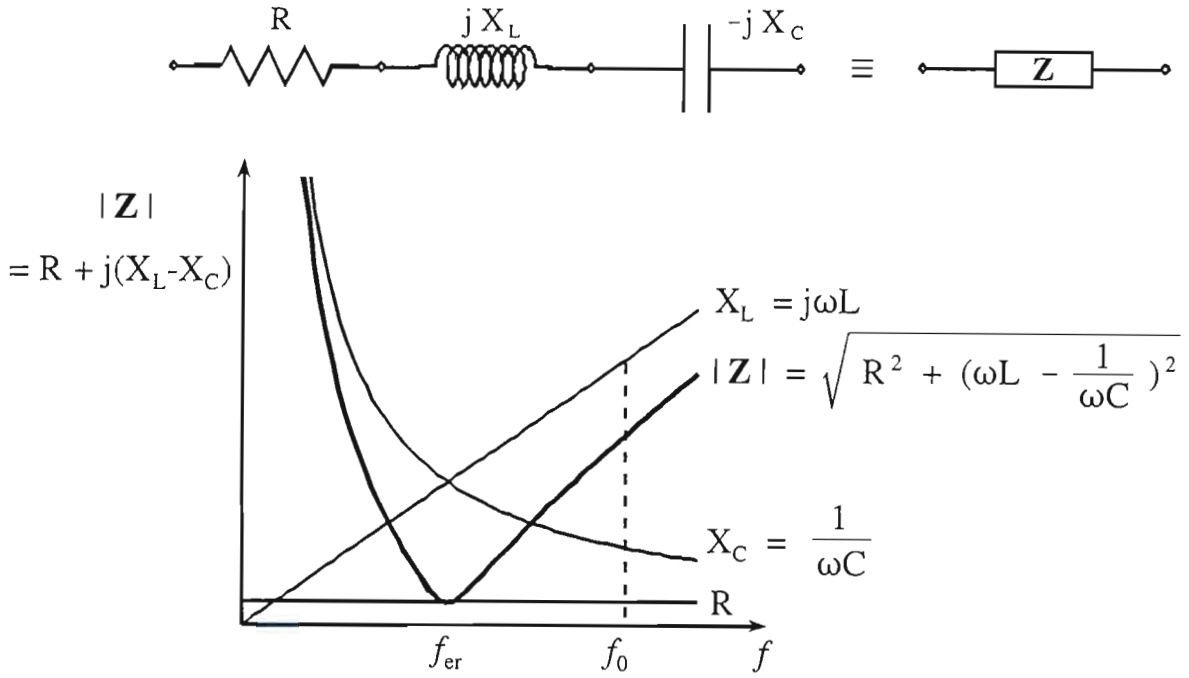


Fig.6.1: Conventional RLC line impedance elements as a function of frequency [18].

Fig. 6.1 shows the total magnitude of the RLC line impedance as a function of frequency. Because the inductive reactance X_L increases and capacitive reactance X_C decreases with increasing frequency, there is always one impedance minimum and this minimum value occurs at the natural frequency of oscillation f_{er} (as shown in Equation (6.1)), where the inductive and capacitive reactances are equal and cancel each other out ($X_{TOTAL} = X_L - X_C = 0$) leaving a small resistance in the transmission line to limit the resonant frequency current flow. In practice, the compensation ratio $\frac{X_C}{X_L}$ is always less than unity, therefore the resonant frequency, which is dependent on the level of compensation of the line inductance, is lower than the system frequency f_0 , i.e. f_{er} is subsynchronous [18].

There are two mechanisms through which SSR can manifest itself, namely, the induction generator effect and torsional interaction. The *induction generator effect* is predominantly an electrical resonance, which occurs when the compensation ratio is high and the effective system resistance is too low at the natural frequency f_{er} , resulting in the flow of subsynchronous current becoming self-sustaining. The second mechanism, *torsional interaction*, is a form of self-excitation that occurs due to the interaction between the electrical system and mechanical dynamics of a turbine-generator. This particular mechanism can only occur in a generator with a multi-inertia shaft. In such a turbine-generator system, the turbine stages are connected by torsionally flexible shafts so that there are a number of natural torsional oscillatory modes. Each of these torsional modes has a distinct mechanical natural frequency of oscillation f_n . When the series compensated transmission line possesses an electrical resonance f_{er} , it results in air-gap fluxes in the generator at complementary frequencies of $f_0 \pm f_{er}$. The electrical and mechanical systems will interact when the subsynchronous complementary frequency $f_0 - f_{er}$ is close to one of the mechanical resonant modes. This interaction can result in oscillations that become self-excited and the subsynchronous currents are large. In the case where the damping of torsional modes in a turbine-generator is exceptionally low, a phenomenon called shaft torque amplification may occur. This further effect of SSR is capable of producing shaft torques of much larger amplitudes following a system disturbance than those developed in uncompensated transmission lines.

In both mechanisms, the existence of physical capacitors is instrumental in introducing an electrical resonance in the transmission line and hence causing SSR. The question remains whether an inverter-based series compensator like the SSSC is able to cause a similar electrical resonance in transmission line. The following subsection reviews the literature concerning this matter.

6.2.3 Literature Review

This section now presents a review of the technical literature and examines the issue of whether or not the inverter-based series compensator is also a candidate for causing electrical resonance in the transmission line and therefore SSR.

Since the solid-state, inverter-based series capacitive compensator was first introduced by Gyugyi [13] to replace conventional capacitors by injecting a controllable synchronous ac voltage in series with the transmission line, various papers [16,26] have stated that these series compensators are immune to network resonances because no physical capacitors are placed on to the

transmission line. It was claimed that since the inverter-based series compensator injects the required quadrature voltage into the line only at the system frequency, it therefore exhibits a theoretically zero impedance at all other frequencies. Hence, with proper implementation, it *cannot cause subsynchronous resonance* because of the absence of the transmission line impedance minimum. Subsequently, Gyugyi mentioned in [17] that the “*series compensation by a synchronous voltage source that can be restricted to the fundamental frequency is superior to that obtained with series capacitive compensation in that it is, with proper implementation, unable to produce undesired electrical resonances with the transmission network, and for this reason it cannot cause subsynchronous resonance.*” Later on, Gyugyi *et al.* [21] reiterated that the SSSC’s claimed immunity to classical network resonances is one of its advantages. However, no impedance characteristics of the inverter-based series compensator compensated transmission line or any relevant results were presented to validate the above statement.

References [35,83] by Ooi *et al.* proposed a method of controlling a single inverter to act as an advanced series compensator but the magnitude of compensating reactance injected into the line could not be controlled. Ooi *et al.* [35,83] considered the potential of transmission line resonance and proposed the inclusion of a notch filter feedback circuit to the series compensator so that it, as an active filter, removes all low order frequencies in the transmission line. However, again, no frequency domain analysis on the transmission line impedance was shown in both papers and therefore such a solution to the problem of SSR has still not been fully evaluated.

While Sen did not include any resonance related topic in his two papers [27,34] on the development of the two-level SSSC and UPFC respectively, Ghosh [55] on the other hand, stated that with these FACTS series compensators “*the system operates satisfactorily without any SSR for balanced and unbalanced faults.*” Despite the unanimous agreement in such claims, little detailed analysis of the resonant characteristics of the inverter-based series compensator has been presented in each case.

Nevertheless, it has been demonstrated [18,20,33] by analysis of transmission line impedance in the frequency domain that an inverter-based series compensator causes a similar resonant impedance effect to that caused by conventional series compensating capacitors, and therefore “*has the potential to cause SSR*”. However, the subsynchronous frequency at which the resonant minimum occurs in the impedance of the SSSC-compensation is different from that compensated by the conventional capacitors. Reference [33] also stated that even though the inverter-based series compensator can potentially excite SSR, it is “*inherently more SSR stable than conventional series compensating capacitors.*”

Reference [77] by the author described a frequency-domain impedance characteristic study on the two-level SSSC when used to compensate a transmission system based on that in [34]. The conclusion drawn in [77] in regards to SSR is in agreement with [18,33]: the SSSC was shown to cause a resonant minimum in the transmission line impedance similar to that caused by conventional series compensating capacitors, and is therefore “*prone to subsynchronous resonance.*”

The above review shows not a disagreement in the field of SSR, but rather a development in the closer understanding of one aspect of the behaviour of the inverter-based series compensators. The following section furthers the analysis on a two-level SSSC in the frequency domain to investigate the resonant characteristics of such a device when placed in series with the transmission line of a benchmark SSR study system.

6.3 The Impedance Versus Frequency Characteristics Of The SSSC In The Transmission Line Of The IEEE First Benchmark Model

6.3.1 Introduction

Since the IEEE First Benchmark Model [72] was first developed in 1977, it has been used for comparison in computational results for various simulation programs. The simplicity and the accuracy of the simulation model itself also invites researchers to perform tests and analysis on the transmission line resonances and the machine shaft dynamics. It was therefore decided to take advantage of the benchmark model to study the resonant characteristics of an SSSC. The electrical network of the First Benchmark Model is shown in Fig. 6.2: the sending-end of the transmission line consists of a multi-inertia synchronous generator, and the receiving-end is connected to an infinite bus behind system reactance X_r . The transmission line itself includes line resistance R_L , inductive reactance X_L , and a compensating capacitive reactance X_C . A temporary three-phase fault to ground with fault reactance X_F is applied immediately after the series compensation.

The aim of this section is to analyse the impedance versus frequency characteristics of the transmission line itself in the IEEE First Benchmark Model compensated with the two-level SSSC. In order to do so, the IEEE First Benchmark Model that is already present as an example case in the simulation package PSCAD/EMTDC is modified for this particular study. Because the focus of this part of the investigation is to identify the resonant impedance minimum of the compensated transmission line (either by the conventional capacitors or the SSSC), the

synchronous machine at the sending-end of the line is initially replaced with a grounded three-phase ac source with the same voltage amplitude and frequency. This simplified version of the full benchmark model is used to analyse the different resonant responses in the frequency domain of conventional capacitor compensation and inverter-based SSSC compensation. The detailed PSCAD/EMTDC simulation models employed in this section are shown in Appendix G.2.

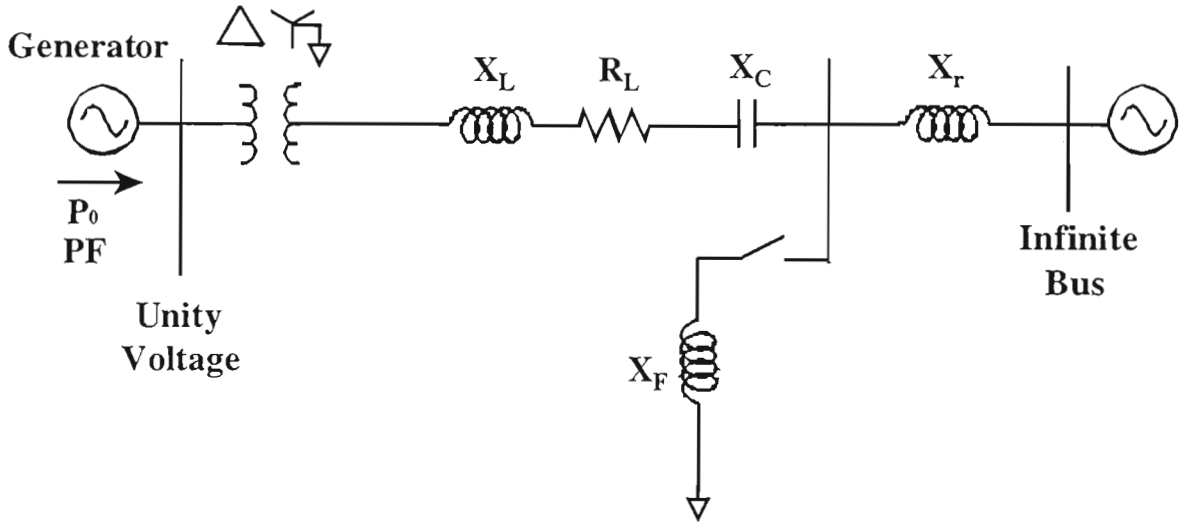


Fig.6.2: IEEE First Benchmark network for subsynchronous resonance study [72].

6.3.2 Simulated Frequency Response Test Methodology

The simulated frequency response test described in this section is adapted from [18,33]. The reason such an approach is required is that, when the series compensation is provided by a complex power-electronic device such as the SSSC, it is no longer possible to predict the frequency response using linear circuit theory analysis as would be the case when using conventional capacitors. The main steps that were taken in order to investigate the resonant characteristics of the line compensated with the SSSC are described below:

- (1) A small subsynchronous voltage source $V_{ss\ abc}$ of 5% of the sending-end voltage amplitude is inserted into each phase at the sending end of the transmission line as shown in Fig. 6.3. The frequency of the subsynchronous voltage $V_{ss\ abc}$ is set to some subsynchronous value ω_{ss} (i.e. $\omega_{ss} < \omega_0$) at which the impedance characteristics of the line are to be determined.
- (2) With the combination of synchronous and subsynchronous forcing voltages, the steady-state response of the transmission line variables was obtained from the time-domain simulation of the system shown in Fig. 6.3.

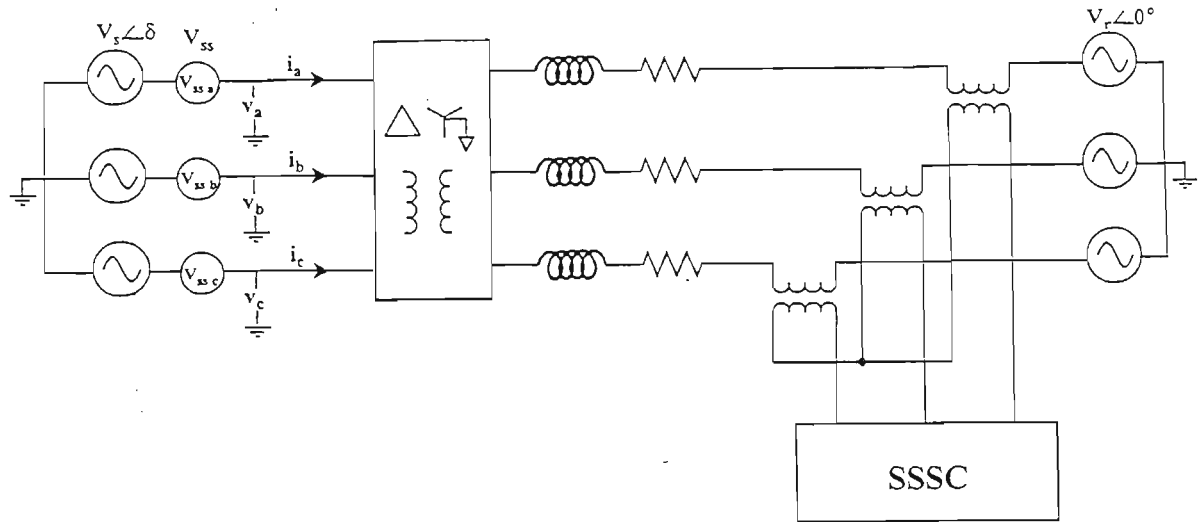


Fig.6.3: Diagram of the simulated frequency response tests as performed on the transmission line of the IEEE Benchmark Model transmission line containing a detailed model of the SSSC in PSCAD/EMTDC.

(3) A 1024-point, Fast Fourier Transform (FFT) analysis is then carried out on the time domain results to extract the magnitude and phase relationship between the phase a voltage v_a at the sending-end of the line and the phase a current i_a in the line to determine the impedance Z_{line} at the preset subsynchronous frequency ω_{ss} of the voltage $V_{ss abc}$.

(4) By repeating the procedure from (1) to (3) for a range of values of subsynchronous frequency the net impedance of the line as a function of frequency was obtained over the rest of the frequency domain.

Same steps are taken to investigate the resonant characteristics of the line compensated with the conventional capacitors, but with the SSSC replaced with capacitors in Fig. 6.3.

6.3.3 Conventional Capacitor Compensation Versus SSSC Compensation

In order to obtain confidence that the above-described frequency response test is the correct procedure to investigate the resonant impedance characteristics, these steps are followed for numerous values of subsynchronous frequencies between 0 Hz and 60 Hz in order to obtain the phase a impedance characteristics for the conventional capacitor compensated IEEE First Benchmark Model transmission line. The results of this simulation analysis at the IEEE First Benchmark Model default compensating reactance of $X_c = 0.3707$ pu are shown in Fig. 6.4.

These simulated results are then compared to the theoretical impedance curve calculated based on Equation (6.1). Fig. 6.4 shows that the frequency-domain impedance predicted by the PSCAD/EMTDC simulation agrees closely with the theory, thus confirming the correctness of the test method. This testing method can therefore also be employed to investigate the resonant impedance characteristics of the line when compensated with the SSSC.

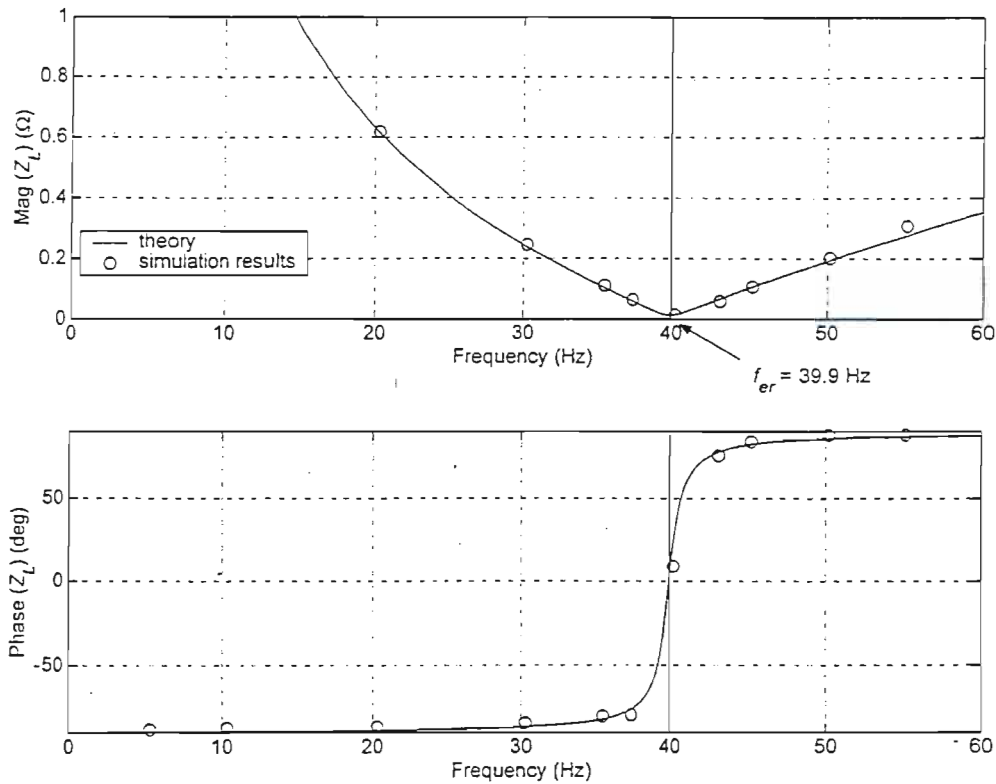


Fig.6.4: Magnitude and phase of the total impedance Z of the conventional capacitor compensated IEEE First Benchmark Model transmission line at $X_C = 0.3707$ pu, as obtained from simulated frequency response tests and from theoretical calculation.

As mentioned previously, the aim of this section is to illustrate the similarities and differences in resonant characteristics between the conventional capacitor compensated and SSSC compensated transmission line. Therefore the phase a resonant impedance characteristics in the frequency domain for the transmission line compensated by the conventional capacitor are again shown in Fig. 6.5(a) (these results are duplicates of Fig. 6.4), but now the impedance results for the transmission line compensated by the SSSC are also shown for at the same compensation ratio shown in Fig. 6.5(b).

As shown in Fig. 6.5, it is clear that both the conventional capacitor compensated and SSSC compensated transmission lines exhibit a resonant minimum and zero phase in their impedances, but at different resonant frequencies, f_{er} . From the PSCAD/EMTDC simulation results, the line compensated with the conventional capacitor resonates at 39.9 Hz whereas the line compensated with the SSSC resonates at a lower frequency of 30.5 Hz. Although both types of series compensation have a similar effect, the SSSC compensation does not follow the same theoretical equation for the resonant frequency (i.e. Equation (6.1)) as the conventional capacitor compensation.

Despite the difference in resonant frequency, Fig. 6.5 illustrates that for both types of series compensation, the capacitive reactance provided by the compensator is greater than the inductive reactance of the line at frequencies below the resonant frequency and therefore the transmission

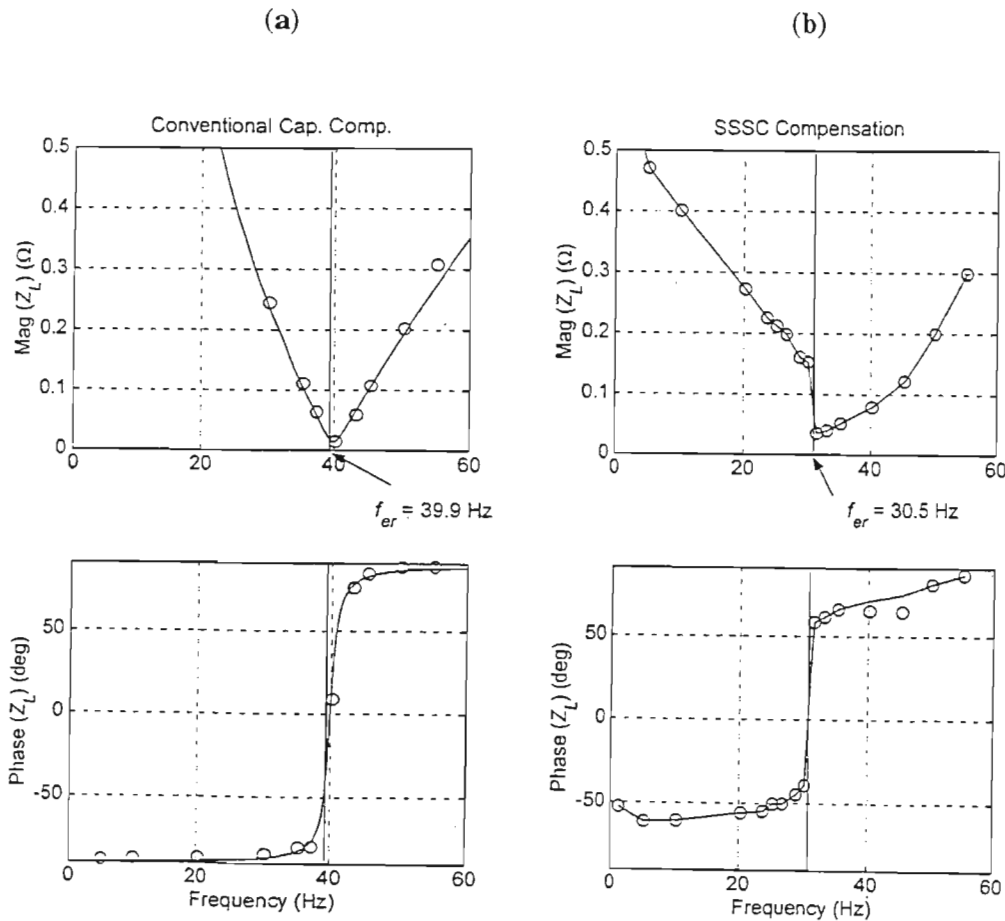


Fig.6.5: (a) Magnitude and phase of the total impedance Z of the conventional capacitor compensated IEEE First Benchmark Model transmission line at $X_C = 0.3707$ pu, as obtained from simulated frequency response tests; (b) total impedance Z of the same transmission line compensated by the SSSC at $X_q^ = 0.3707$ pu.*

line is net capacitive: the voltage *lags* the current by 90° and the impedance phase angle is between 0° and -90° . The phase for the SSSC compensated line, however, stays at around -55° and does not reach as low as -90° like the conventional capacitor line. Similarly, for both forms of compensation, at frequencies above the resonant frequency, the transmission line inductive reactance exceeds the capacitive reactance of the compensator and the line is net inductive: the voltage *leads* the current and the impedance phase angle is between 0° and $+90^\circ$. At their respective resonant frequencies, however, the capacitive reactance provided by either type of compensation exactly cancels the line inductive reactance such that the net line impedance is purely resistive and exhibits a resonant minimum in both cases.

This frequency response of the SSSC compensated transmission line in the First Benchmark Model is consistent with the findings of [18,33,77]. Subsequent to these findings, other researchers have also verified the same findings using analytical techniques [20], further validating both the results and the use of the simulated frequency response techniques employed here. Like the conventional RLC line, the SSSC compensated transmission line has a resonant minimum because it acts as a capacitive reactance over the entire frequency domain and not *only* at the synchronous frequency of the transmission system. Therefore, it has the potential to excite subsynchronous resonance.

6.3.4 SSSC Compensation For Different Values Of Compensating Reactance X_q^*

This subsection now examines the net impedance of the SSSC compensated transmission line as a function of frequency for a range of different values of commanded compensating reactance X_q^* . The purpose of this study is to identify the trend of the resonant impedance characteristic of the transmission line compensated by the SSSC when X_q^* is varied. The same frequency response test procedure described in subsection 6.3.2 is followed in this investigation as in the previous subsection.

Fig. 6.6 shows the graphs of the frequency-domain impedance characteristics of the SSSC compensated transmission line for values of commanded capacitive compensating reactance X_q^* of 0.178 pu, 0.275 pu and 0.3707 pu (Figs. 6.6(a), 6.6(b) and 6.6(c) respectively), as well as a commanded inductive reactance of 0.178 pu (Fig. 6.6(d)).

As in the previous section, Fig 6.6 shows that for each different value of compensating reactance provided by the SSSC, the line exhibits a resonant minimum in its impedance at a subsynchronous frequency, and the impedance at this frequency is small and purely resistive. It can also be seen

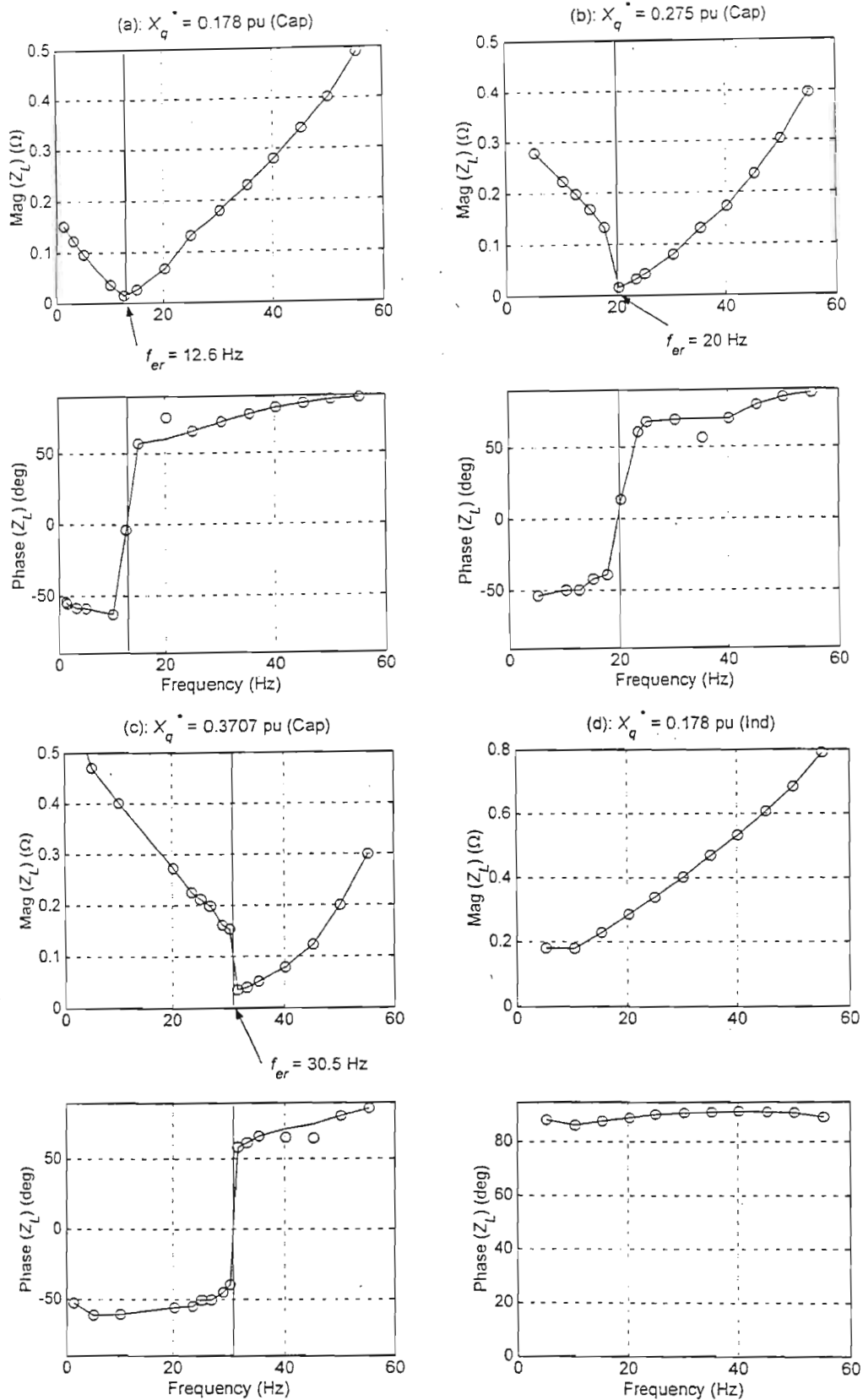


Fig.6.6: Magnitude and phase of the total impedance Z of the SSSC compensated IEEE First Benchmark Model transmission line at (a) $X_C = 0.178$ pu; (b) $X_C = 0.275$ pu; (c) $X_C = 0.3707$ pu; (d) $X_L = 0.178$ pu, as obtained from simulated frequency response tests.

on those three plots that consider capacitive values of X_q^* (Figs. 6.6(a), 6.6(b) and 6.6(c)) that the natural frequency f_{er} increases with the increase in the commanded capacitive compensating reactance X_q^* . The phase of the total transmission line impedance shifts from -90° to $+90^\circ$ as the frequency of the subsynchronous forcing voltage increases. This indicates that the impedance of the line ranges from being predominantly capacitive to purely resistive at the resonant frequency where the phase crosses zero degrees, to being predominantly inductive as the frequency increases above f_{er} .

The results in Fig. 6.6(d) show that when the SSSC is used to provide an inductive reactance in series with the line, there is no resonant minimum in the line impedance. Instead, both the magnitude and the phase of the line impedance increase with the increase in frequency of the subsynchronous forcing voltage, with the phase remaining close to $+90^\circ$ and never reaching zero degrees. This behaviour is consistent with the frequency domain characteristics of an RL line.

The results presented in this section have confirmed the findings in [18,33], that the SSSC causes a resonant impedance effect similar to that caused by conventional capacitors. These results have also shown that the resonant frequency of the SSSC compensated line increases as the commanded value of capacitive compensating reactance increases. Therefore when the SSSC is used to provide a certain amount of capacitive compensation in a transmission line sourced by a multi-inertia synchronous machine, there is a risk that the resulting electrical resonant frequency may by chance interact with one of the turbine's mechanical natural modes and cause SSR. The following section investigates precisely that, where the SSSC is put into the original IEEE First Benchmark Model in place of the conventional capacitors.

6.4 The IEEE First Benchmark Model: Conventional Capacitor Compensation Versus SSSC Compensation

6.4.1 Introduction

The previous section has investigated the resonant characteristics of a transmission line compensated with an SSSC and has shown that the SSSC causes a similar resonant effect to that caused by conventional capacitors. This section now examines the effect this electrical resonance caused by the SSSC has on a multi-inertia synchronous machine, once again by making use of the IEEE First Benchmark Model. The turbine-shaft system modelled in the First Benchmark Model consists of six turbine-generator stages and the associated interconnecting

torsional shafts. This detailed mechanical model of the shaft of the multi-inertia turbine has five natural torsional oscillatory modes, and associated with each of these oscillatory modes is a distinct mechanical natural frequency, f_n , each of which is shown in Table 6.1. As seen in the previous section, the SSSC will cause an electrical resonance in the line whose frequency f_{er} depends on the magnitude of compensation. As explained previously, an electrical resonance in the line results in a component of air gap flux at a subsynchronous complimentary frequency $f_o - f_{er}$. If this complementary frequency coincides with one of mechanical natural frequencies of the shaft shown in the table, then there is a risk of torsional interaction and SSR.

Table 6.1: Turbo-generator shaft modes in the IEEE First Benchmark Model

Modes	Mode Frequency, f_n
Mode 1	15.71 Hz
Mode 2	20.005 Hz
Mode 3	25.55 Hz
Mode 4	32.285 Hz
Mode 5	47.46 Hz

The aim of this study is to investigate the resonant interactions between the transmission line and the machine shaft dynamics. In order to do so, the subsynchronous ac sources are removed, and the three-phase ac source used in the previous study to examine the resonant characteristics of the SSSC in the IEEE First Benchmark Model transmission line is replaced with the original synchronous machine model and turbine shaft model used in the First Benchmark Model for the study of subsynchronous resonance [72]. The detailed simulation model used in this study is shown in Appendix G.3. The following subsection presents some predicted results of the interactions between the electrical and the mechanical system when the transmission line is compensated either with the SSSC or conventional capacitors at different compensation levels.

6.4.2 Time Domain Simulation Results From PSCAD/EMTDC

The previous study has shown that the SSSC and the conventional capacitor compensated transmission line both exhibit resonant impedance minima, but at different natural frequencies. Moreover, the resonant frequency is dependent on the level of compensation, as it increases with the increase in the commanded compensating capacitive reactance X_q^* . This study therefore

considers the same three values of compensating capacitive reactance used in the previous section, which are 0.178 pu, 0.275 pu, and 0.3707 pu, to show the possible interaction between their respective natural frequencies and the mechanical shaft modes. At each value of compensation, the results of both SSSC and conventional capacitor compensation are shown for the purpose of comparison. Based on [72], each case considered shows four selected system variables from the PSCAD/EMTDC simulation, namely, the phase *a* machine current, the electrical torque, the LPA–LPB turbine shaft torque and the GEN–EXC shaft torque.

In the case of both the conventional capacitor compensated and SSSC compensated transmission lines, the system is initially operating at steady state; a three-phase fault of duration 0.075 seconds is then applied at the receiving end of the line at time $t = 0.1$ seconds as shown in Fig. 5.2. The fault duration of 0.075 seconds represents the time for a circuit breaker to interrupt the fault; the particular value of 0.075 seconds is that used in [72]. The results are shown as follows.

$$X_q^* = 0.178 \text{ pu}$$

At the commanded capacitive reactance of 0.178 pu, the SSSC and the conventional capacitor cause different natural frequencies, f_{er} . The value of f_{er} at this value of X_q^* for each form of compensation has been predicted in the previous section. These predicted values of f_{er} , together with the associated subsynchronous complimentary frequency, are shown below:

Conventional Capacitor:	$f_{er} = 27.715 \text{ Hz}$	$f_o - f_{er} = 32.285 \text{ Hz}$
SSSC:	$f_{er} = 12.8 \text{ Hz}$	$f_o - f_{er} = 47.2 \text{ Hz}$

With reference to Table 6.1, it can be seen that the complimentary frequency of the conventional capacitor matches the Mode 4 mechanical frequency of 32.285 Hz, whereas the complimentary frequency of the SSSC comes very close to the Mode 5 mechanical frequency of 47.46 Hz.

Fig 6.7(a) and Fig 6.8(a) show graphs of the phase *a* machine current for conventional capacitor compensation and SSSC compensation respectively. After the three-phase fault has been applied at 0.1s, machine currents for both forms of compensation increase in amplitude then begin to decrease back to steady state after the fault has been cleared. Whereas the SSSC compensated machine current settles quickly to steady state and is predominantly 60 Hz, it is obvious that the capacitor compensated machine current is less damped and contains more than just the system frequency.

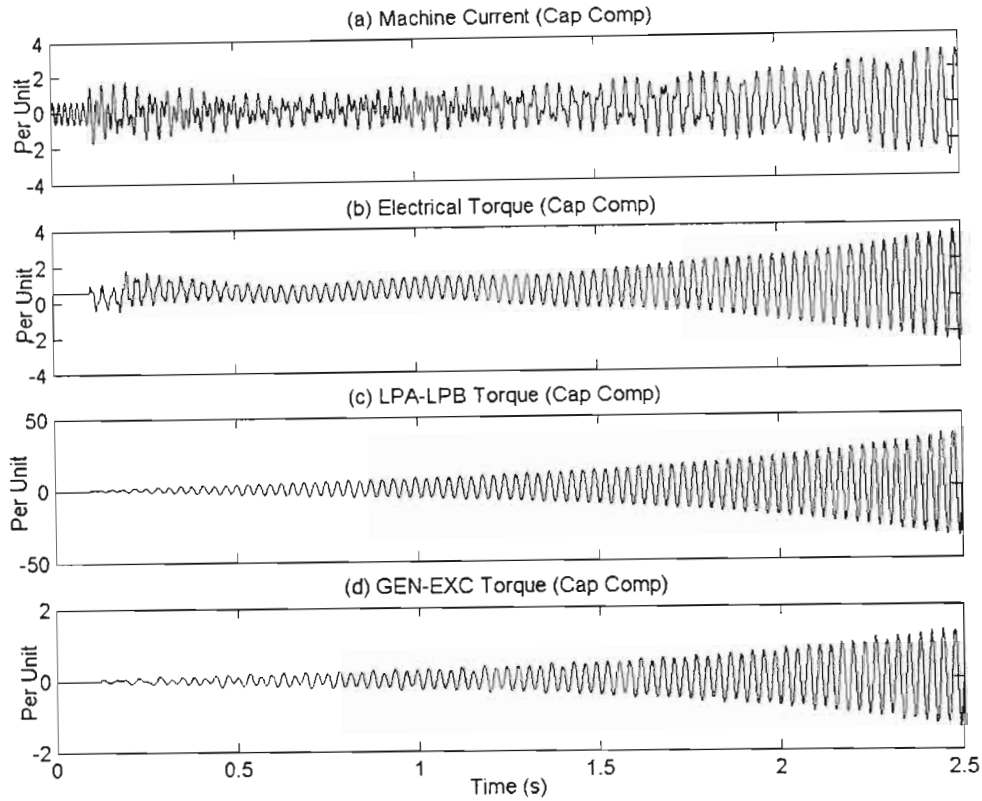


Fig.6.7: Machine response curves for the conventional capacitor compensated transmission system at $X_q^ = 0.178$ pu in the IEEE First Benchmark Model.*

Figs. 6.7(b), (c) and (d) show that in the case of the conventionally compensated system, following the disturbance the electrical torque, LPA-LPB and GEN-EXC shaft torques all exhibit large negatively damped oscillations. In the case of the LPA-LPB shaft torque, these oscillations are predominantly at the frequency of Mode 4 (32.3Hz), while in the case of the GEN-EXC shaft torque the oscillations comprise both the Mode 4 and Mode 5 frequencies (mixture of 32.3Hz and 47.5Hz).

On the other hand, electrical torque of the SSSC compensated system, shown in Fig. 6.8(b), exhibits relatively small oscillations immediately after the disturbance, but these are well damped and rapidly return to steady state. In Fig. 6.8(c) and (d), the LPA-LPB and GEN-EXC shaft torques clearly show no destabilization of the system by the SSSC at this value of compensation, despite the electrical system being closely tuned to the frequency of Mode 5.

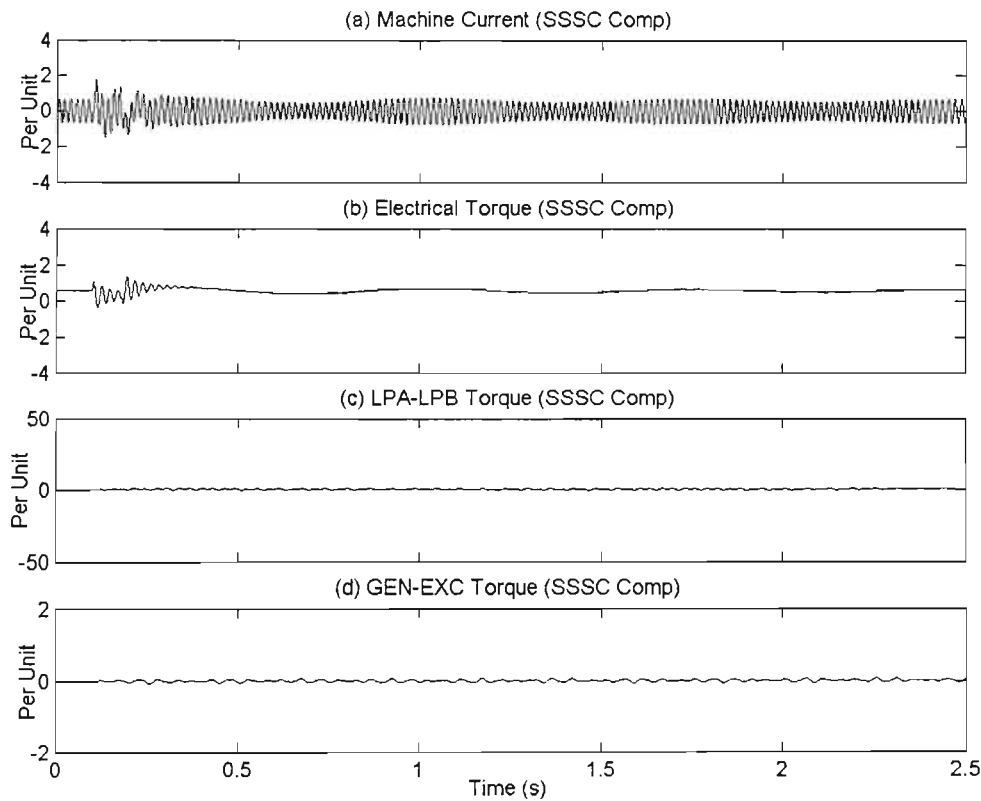


Fig.6.8: Machine response curves for the SSSC compensated transmission system at $X_q^ = 0.178$ pu in the IEEE First Benchmark Model.*

$X_q^* = 0.275$ pu

At the capacitive reactance value of 0.275 pu, the value of f_{er} for each form of compensation has been predicted in the previous section. These predicted values of f_{er} , together with the associated subsynchronous complimentary frequency, are shown below:

Conventional Capacitor:	$f_{er} = 34.45$ Hz	$f_o - f_{er} = 25.55$ Hz
SSSC:	$f_{er} = 19.76$ Hz	$f_o - f_{er} = 40.24$ Hz

With reference to Table 6.1, the complimentary frequency of the system compensated with conventional capacitors matches the Mode 3 mechanical frequency of 25.55 Hz, whereas the complimentary frequency of system compensated with the SSSC is half way between Mode 4 and Mode 5.

Fig 6.9(a) and Fig 6.10(a) show graphs of the phase *a* machine current for conventional capacitor compensation and SSSC compensation respectively. After the fault has been applied at 0.1s, machine currents for both forms of compensation once again increase in amplitude then begin to decrease after the fault has been cleared. Whereas the SSSC compensated machine current settles more quickly to steady state, it is clear that in the case of both forms of compensation the line currents contain more than just the system frequency.

The electrical torque shown in Fig 6.9(b) shows large sustained oscillations in the capacitor compensated system with a frequency of 26Hz, which is the Mode 3 frequency. The oscillations in electrical torque of the SSSC compensated system, shown in Fig. 6.10(b), are more damped and occur at a frequency of 40Hz, which is the predicted complimentary frequency of the SSSC compensation.

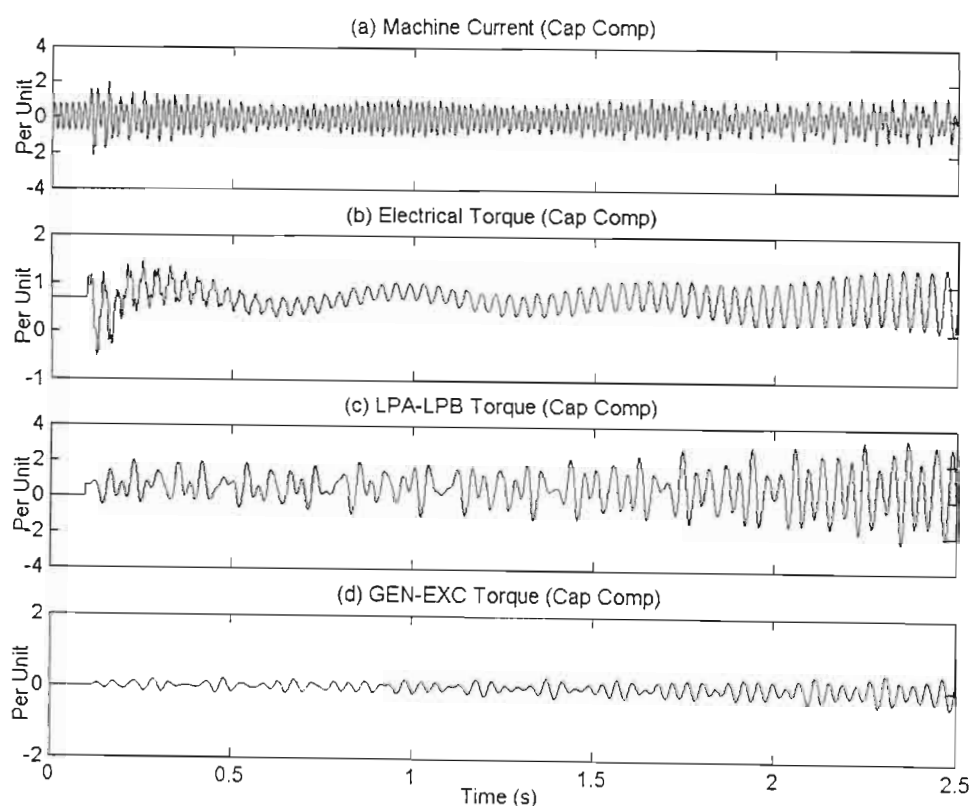


Fig.6.9: Machine response curves for the conventional capacitor compensated transmission system at $X_q^ = 0.275$ pu in the IEEE First Benchmark Model.*

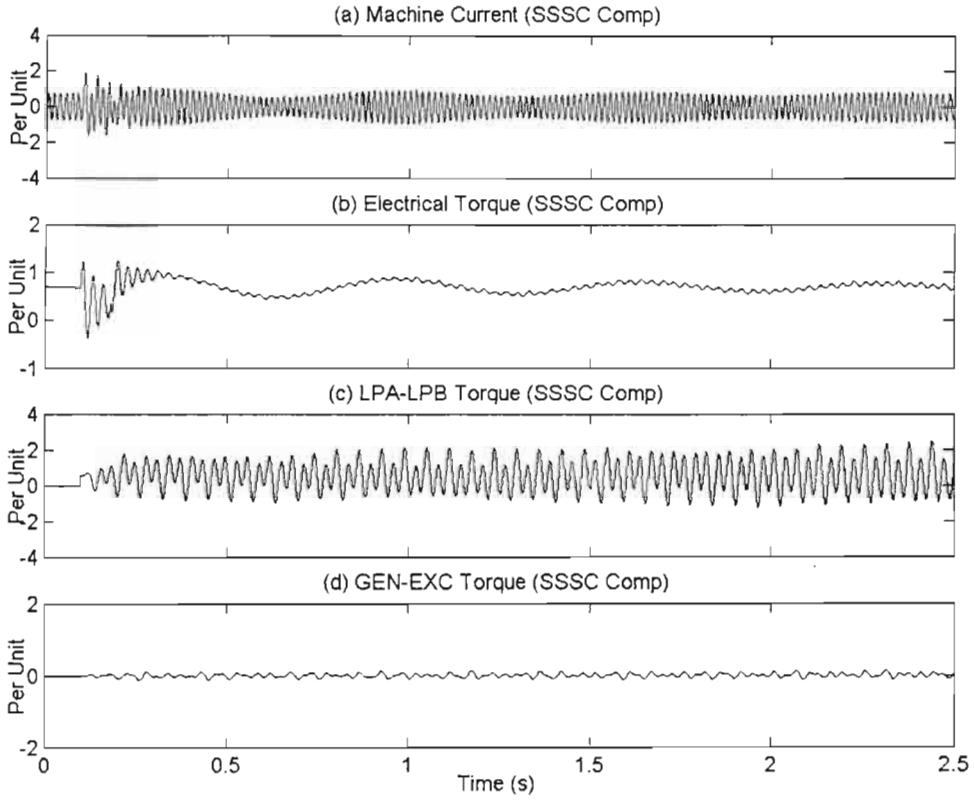


Fig.6.10: Machine response curves for the SSSC compensated transmission system at $X_q^ = 0.275$ pu in the IEEE First Benchmark Model.*

Figs. 6.9(c) and (d) show that in the case of the conventionally compensated system, following the disturbance the LPA-LPB and GEN-EXC shaft torques both exhibit negatively damped oscillations. These growing oscillations confirm the instability of Mode 3 for this value of conventional compensation. Figs. 6.10(c) and (d) show that in the case of the SSSC compensation there are oscillations at the frequency of both Mode 4 (32.2Hz) and Mode 5 (47.5Hz) in the LPA-LPB and GEN-EXC shaft torques respectively. From the results of Fig 6.10(c) in particular, it is clear that the SSSC is causing strong torsional interaction with Modes 4 and 5 of the shaft and that the system is close to instability (i.e. mechanical failure) as a result. Even without mechanical instability, the large poorly damped torques are undesirable as they would contribute to shaft fatigue and reduction in life of the equipment.

Overall, the torque oscillations in the conventionally compensated system are larger than in the case of the SSSC compensated system. Thus, the SSSC form of compensation gives rise to significantly less destabilization at this value of compensation, and this destabilization manifests itself in a distinct torsional mode from that of conventional series compensation. Conventional compensation results in a predominantly Mode 3 oscillations, while SSSC

compensation results in a combination of Mode 4 and Mode 5 oscillations. This phenomenon of exciting two modes at once is well known [82] and is due to the fact that one of the modes is highly susceptible to torsional interactions.

$$X_q^* = 0.3707 \text{ pu}$$

At the capacitive reactance value of 0.3707 pu, the value of f_{er} for each form of compensation has been predicted in the previous section. These predicted values of f_{er} , together with the associated subsynchronous complimentary frequency, are shown below:

Conventional Capacitor:	$f_{er} = 39.994 \text{ Hz}$	$f_o - f_{er} = 20.006 \text{ Hz}$
SSSC:	$f_{er} = 30.5 \text{ Hz}$	$f_o - f_{er} = 29.5 \text{ Hz}$

This particular commanded compensating capacitive reactance of 0.3707 pu is the value selected for the time domain subsynchronous resonance study published in the IEEE First Benchmark Model [72]. This compensation level is specifically chosen (for conventional compensation) to have a resonant frequency at 39.994Hz and therefore excites the second torsional frequency of 20.006Hz. With reference to Table 6.1, the resonant frequency of the SSSC at this value of compensating reactance is at 30.5Hz and therefore the complimentary frequency in the case of SSSC compensation is between Mode 3 and Mode 4, but closer to the latter mode at 29.5Hz.

Fig 6.11(a) and Fig 6.12(a) show graphs of the phase *a* machine current for conventional capacitor compensation and SSSC compensation respectively. After the three-phase fault has been applied, machine currents for both forms of compensation increase in amplitude then begin to decrease after the fault has been cleared. However, the peak-to-peak amplitude of machine current for the capacitor compensated system is noticeably higher than the previous two sets of studies with different compensating reactances X_q^* , but similar to the previous two studies in that it contains more than the system frequency. On the other hand, the SSSC compensated machine current settles quickly to steady state and is predominantly 60Hz.

The electrical torque shown in Fig 6.11(b) shows large sustained oscillations in the capacitor compensated system, again noticeably higher in amplitude than the previous two studies. The electrical torque of the SSSC compensated system, shown in Fig. 6.12(b), also exhibits fairly large oscillations compared to the previous two values of compensation, but these are well damped and rapidly return to steady state.

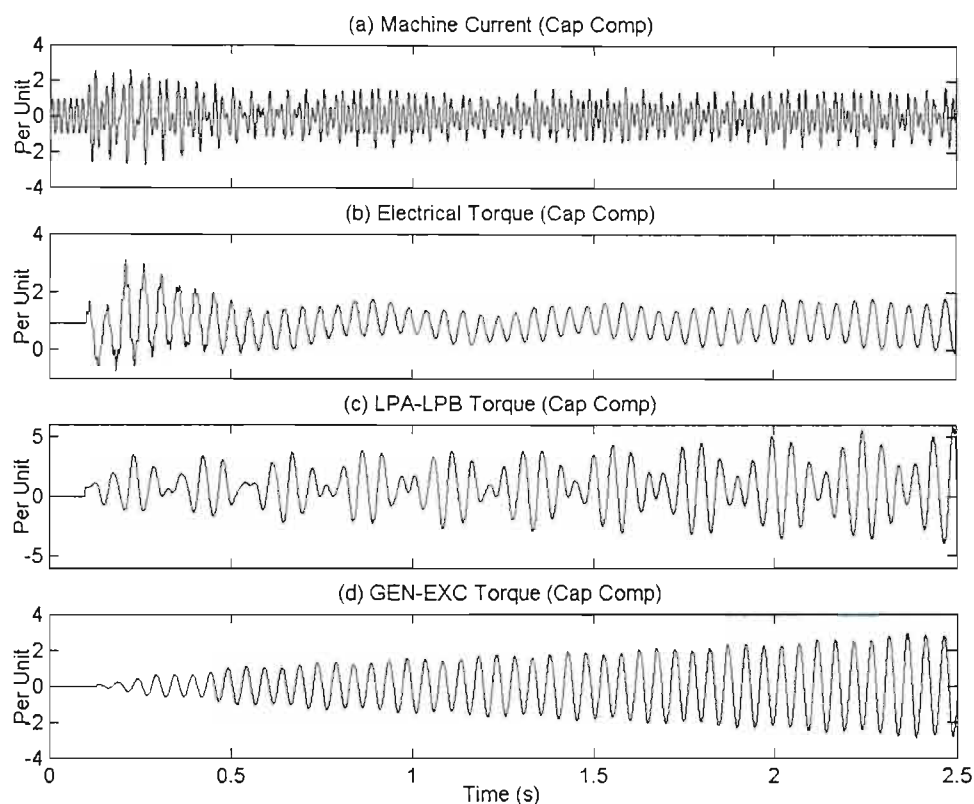


Fig.6.11: Machine response curves for the conventional capacitor compensated transmission system at $X_q^ = 0.3707$ pu in the IEEE First Benchmark Model.*

Figs. 6.11(c) and (d) show that in the case of conventionally compensated system, the LPA-LPB and GEN-EXC shaft torques both exhibit large negatively damped oscillations following the disturbance. The oscillations in both of these shaft torques are predominantly at the frequency of Mode 2 (20Hz) as predicted. These shaft torque amplitudes are much larger than the previous study, especially the LPA-LPB torque. The amplitude of the oscillations of the GEN-EXC torque shown in Fig. 6.11(d) increases with time and therefore suggests instability in Mode 2 at this value of conventional capacitor compensation.

In the case of SSSC compensated system, Fig. 6.12(c) shows that there are oscillations at the frequency of Mode 4 (32Hz) in the LPA-LPB shaft torque, whereas Fig. 6.12(d) shows a frequency of 20Hz, which suggests a small excitation of Mode 2. This shows that with this particular SSSC compensation, a combination of modes is excited. However, in the case of SSSC compensation, the oscillations persist for several cycles but they are not as large and are not as negatively damped as in the case of conventional capacitor compensation. Nevertheless, the oscillations of the LPA-LPB shaft torque show clearly that torsional interaction is taking place.

These results confirm that at the same value of synchronous frequency compensating reactance, the SSSC and conventional series capacitor interact with the mechanical shaft of the turbine at quite distinct subsynchronous frequencies.

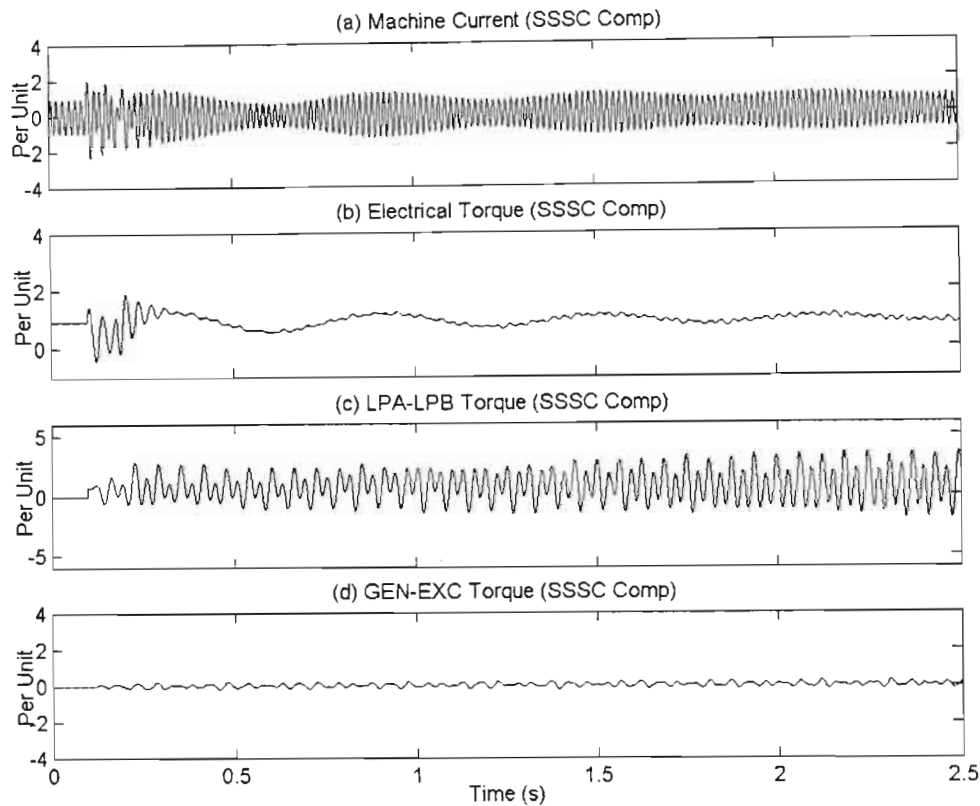


Fig.6.12: Machine response curves for the SSSC compensated transmission system at $X_q^ = 0.3707$ pu in the IEEE First Benchmark Model.*

The above investigation has presented three sets of SSR studies of SSSC and conventional capacitor compensated transmission lines with different commanded capacitive compensation reactance values. It is observed that since resonance occurs at different frequencies for the SSSC and conventional capacitors at the same compensation level, one form of compensation may excite a specific mechanical shaft mode while the other can excite another mode, a combination of modes or miss out on all modes. Although close tuning of the subsynchronous electrical complementary frequency is a necessary condition for destabilization of a torsional mode, it is not on its own a sufficient condition: certain torsional modes of a turbine shaft are less susceptible to torsional interaction and destabilization by electrical resonances than other modes because of torsional properties other than their mode frequency [84]. In the case of this study system, there is no instability in Mode 5 for SSSC compensation of $X_q^* = 0.178$ pu despite the electrical

resonance caused by the SSSC, since this resonance coincides with a torsional mode that is not susceptible to torsional interaction. Therefore, instead of showing only one operating condition for the SSR studies in order to rule out the possibility of SSR (as shown in [55]), it is crucial to check a range of compensation values. Also, even at values of compensation where the SSSC does not cause large persistent oscillations, the shaft torque oscillations can still be poorly damped and therefore of concern. Hence, these results show that this form of compensation *can* cause torsional interaction, even if it may destabilize torsional modes to a lesser degree than conventional capacitors. This finding is in agreement with conclusions drawn in reference [33].

6.5 Conclusion

This chapter began by introducing the two different mechanisms that cause subsynchronous resonance, then presented a review of the field of inverter-based series compensators and SSR. It has commonly been claimed, that these inverter-based series compensators do not cause SSR because their compensating voltages can be restricted to the fundamental frequency. Subsequently [18,33], it has been shown otherwise by examining the electrical impedance characteristics of an inverter-based series compensator in the frequency domain.

This chapter extends the previous work by examining the impedance versus frequency characteristics of a transmission line compensated with a two-level SSSC using the detailed model developed in Chapter Three. The chapter has also considered the compensation characteristics of a two-level SSSC in the IEEE First Benchmark Model for the study of SSR, once again using the detailed model of the SSSC developed in Chapter Three. Similar to the findings in [18,33] the SSSC was found to cause a resonant minimum in the line impedance at a subsynchronous natural frequency, at which frequency the line impedance is purely resistive: i.e. the SSSC acts as a capacitive reactance not only at the fundamental frequency but over the *entire* frequency spectrum. It was therefore concluded that the SSSC is likely to cause SSR in susceptible neighbouring generators. Furthermore, it has been shown that for the same compensating capacitive reactance, the resonant frequency of the SSSC is somewhat lower than that of conventional capacitors. It was also then demonstrated that with the increase in the compensating capacitive reactance, the resonant frequency caused by the SSSC increases.

The detailed examination of the two-level SSSC in the IEEE First Benchmark Model confirmed the above conclusions. The results showed that this form of compensation can result in no destabilization, or significantly reduced destabilization of the torsional modes of a particular

system when compared directly with the same degree of conventional series capacitor compensation. However, it also showed that, in a similar manner to the conventional capacitor compensation, the electrical resonant frequency caused by the SSSC may excite one or more mechanical torsional modes. This interaction may result in large, poorly-damped, or even self-excited oscillations. With insufficient damping of the torsional modes, shaft torque amplification may occur which will give rise to large turbine-generator shaft torques.

Despite the advantages SSSC has over conventional capacitor compensation, (e.g. fast control and response, the ability to emulate both inductive and capacitive reactances, and the ability to damp power oscillations by coordinated modulation of compensating reactance etc.) it nevertheless also has the potential to excite SSR. Close attention should therefore be paid when using such devices so to avoid undesired resonances.

The investigations conducted in this chapter have considered a range of values of compensation X_q^* provided by the SSSC, but at each such value considered, the SSSC's commanded compensating reactance was kept constant during the time frame of the study. The following chapter now considers whether supplementary modulation of the SSSC's compensating reactance can be used to mitigate the resonances it causes when introduced in a transmission line.

CHAPTER SEVEN

SUPPLEMENTARY DAMPING CONTROLLER FOR AN SSSC-COMPENSATED TRANSMISSION LINE

7.1 Introduction

By carrying out frequency scanning tests on the detailed *two-level* SSSC compensated transmission line model developed in Chapter Three, the previous chapter showed that the SSSC exhibits a resonant minimum in the line impedance at a subsynchronous frequency. This is therefore a serious concern when an SSSC is used in a real electrical network as it has the potential threat of exciting SSR. Chapter Six also demonstrated that although the destabilization of torsional modes for SSSC compensation may not always be as severe as with conventional series capacitor compensation, SSR could still result should there be insufficient damping in the system.

Jowder and Ooi have proposed [65] an SSSC fitted with supplementary controls to damp out subsynchronous oscillations caused by other conventional compensating capacitors in the transmission system. However, although the simulation results presented in [65] confirm that the proposed modulated reactance control of the SSSC was able to stabilize SSR in the studied system, the model of the SSSC used in [65] did not include the detailed power electronics and low-level firing controls of the SSSC's inverter. Although the SSSC in [65] is described as three-level, it is represented in the mathematical model as a dynamically-variable ideal voltage source. Furthermore, although the torsional properties of the studied turbine generator were represented in detail in [65], the study system itself was not a benchmark system because of the particular focus of that work [65]. Finally, the system studied in [65] considered only one value of compensation provided by the SSSC, as it was used as an SSR damper rather than a variable compensator.

Other research [64] has shown that the dynamically-adjustable series compensation provided by an SSSC can, in practice, be used to add significant damping to the electromechanical oscillations of a nearby generator in the power system. However, the scheme in [64] was designed to add damping to a relatively low-frequency inertial swing mode of the generator, whereas the torsional oscillations associated with SSR can be significantly higher in frequency, and can even be quite

close to the system frequency itself in some instances. Furthermore, while the findings in [64] were confirmed by laboratory measurements, the SSSC in that study employed a pulse-width modulated inverter; in practice, a transmission-voltage SSSC would typically use multi-level, multi-pulse square wave inverter technology.

Due to the fact that the output ac voltage from the inverter needs to respond rapidly to the modulated reactance control described in the above applications, the two-level SSSC is not considered for this aspect of the work. The reason being is that the output ac voltage from the two-level SSSC is varied by changing the inverter's dc capacitor voltage, and the relatively slow charging and discharging time of the capacitor is therefore not suited for this type of damping control. The *three-level* SSSC is ideal for such application as the amplitude of its output ac voltage is independent of the inverter's dc capacitor voltage, and is changed by varying the inverter's dc-to-ac gain within the high-level SSSC controls.

This chapter now considers whether the supplementary damping control scheme proposed in [65] can still provide acceptable damping of SSR when the SSSC and its inverter are represented in detail, that is with the SSSC's high-level controls, low-level firing controls and its full 24-pulse, three-level voltage source inverter topology represented in the system study. Furthermore, this work further extends that of [65] by considering the performance of the proposed damping control system in a benchmark study system [72], and for a *range of values* of compensation provided by the SSSC.

Before designing the supplementary damping controller, it is necessary to first examine the resonant characteristics of the three-level SSSC. The following section investigates the performance of the three-level SSSC in the IEEE First Benchmark system [72].

7.2 Resonant Characteristics Of Three-Level SSSC

The study conducted in the previous chapter examined the resonant interactions between the transmission line and the generator shaft dynamics in the IEEE First Benchmark Model when the line was compensated with a two-level SSSC. In this section, the same investigation will be carried out on a three-level SSSC compensated transmission line, once again, using the IEEE First Benchmark Model. For the purpose of convenient referencing, the five torsional modes of the multi-inertia turbine and their associated mechanical natural frequencies, f_n , are again shown in Table 7.1.

This study once again considers the same three values of compensating capacitive reactance, X_q^* , used in the previous chapter, which are 0.178 pu, 0.275 pu, and 0.3707 pu, in order to investigate a range of operating points.

Table 7.1: Turbo-generator shaft modes in the IEEE First Benchmark Model

Mode	Mode Frequency, f_n
Mode 1	15.71 Hz
Mode 2	20.005 Hz
Mode 3	25.55 Hz
Mode 4	32.285 Hz
Mode 5	47.46 Hz

As in the studies of Chapter 6, the system is initially operating at steady state; a three-phase fault of duration 0.075 seconds is then applied at the receiving-end of the transmission line at $t = 0.1$ seconds. The results of four system variables from the PSCAD/EMTDC simulation, namely, generator speed, the electrical torque, the LPA–LPB turbine shaft torque and the GEN–EXC shaft torque are shown as follows.

$X_q^* = 0.178$ pu

In the previous chapter, at a commanded capacitive reactance of $X_q^* = 0.178$ pu, the resonant frequency, f_{er} , in the transmission line caused by the two-level SSSC is 12.8 Hz and the associated subsynchronous complementary frequency, $f_o - f_{er}$, is 47.2 Hz. With reference to Table 7.1, the complementary frequency of 47.2 Hz is very close to the Mode 5 mechanical natural frequency of 47.46 Hz.

Fig 7.1 shows the simulated results of the three-level SSSC-compensated line to the short circuit disturbance at $X_q^* = 0.178$ pu. The results shown in Fig. 7.1 indicate no noticeable destabilization of the system compensated by the three-level SSSC at this value of compensation. With the exception of the electrical torque, shown in Fig. 7.1 (b), the mechanical system variables exhibit torsional oscillations after the three-phase fault has been cleared, but these are not negatively damped and they are of small amplitude.

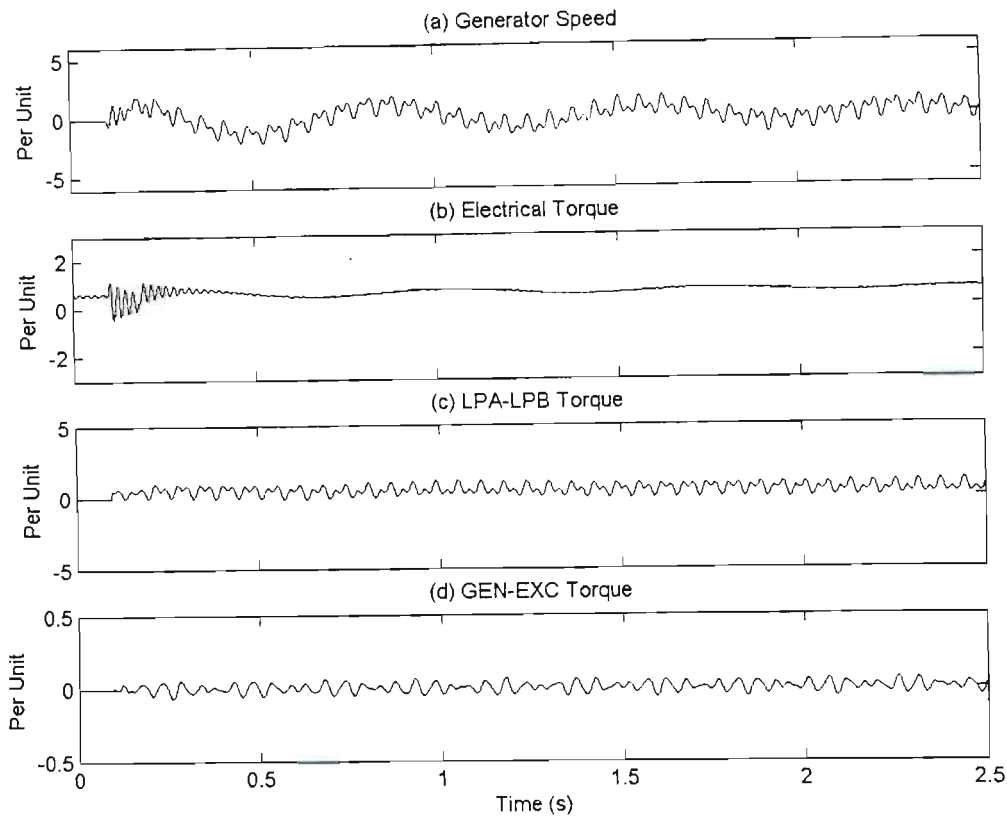


Fig.7.1: Simulated response of the IEEE First Benchmark Model to a short circuit fault for the three-level SSSC compensated transmission system at $X_q^ = 0.178$ pu.*

$$X_q^* = 0.275 \text{ pu}$$

As predicted in the previous chapter, the resonant frequency, f_{er} , in the transmission line caused by an SSSC at a commanded capacitive reactance of $X_q^* = 0.275$ pu is 19.76 Hz, and the associated subsynchronous complementary frequency, $f_o - f_{er}$, is 40.24 Hz. With reference to Table 7.1, the complementary frequency of the system at this value of compensation is half way between the mechanical natural frequencies of Mode 4 and Mode 5.

Fig 7.2 shows the simulated results of the three-level SSSC-compensated line to the short circuit disturbance at $X_q^* = 0.275$ pu. The results in Fig. 7.2 show that at this value of compensation the torsional oscillations in the mechanical system variables are now of concern: although the oscillations are not noticeably negatively damped, they are larger in amplitude than is the case in Fig. 7.1 and are sustained; such oscillations would in all likelihood reduce the life of the turbine shaft if allowed to persist in this manner. A close analysis of these oscillations (not

shown here) has shown the presence of both the Mode 1 (15.71 Hz) and Mode 4 (32.3 Hz) mechanical natural frequencies.

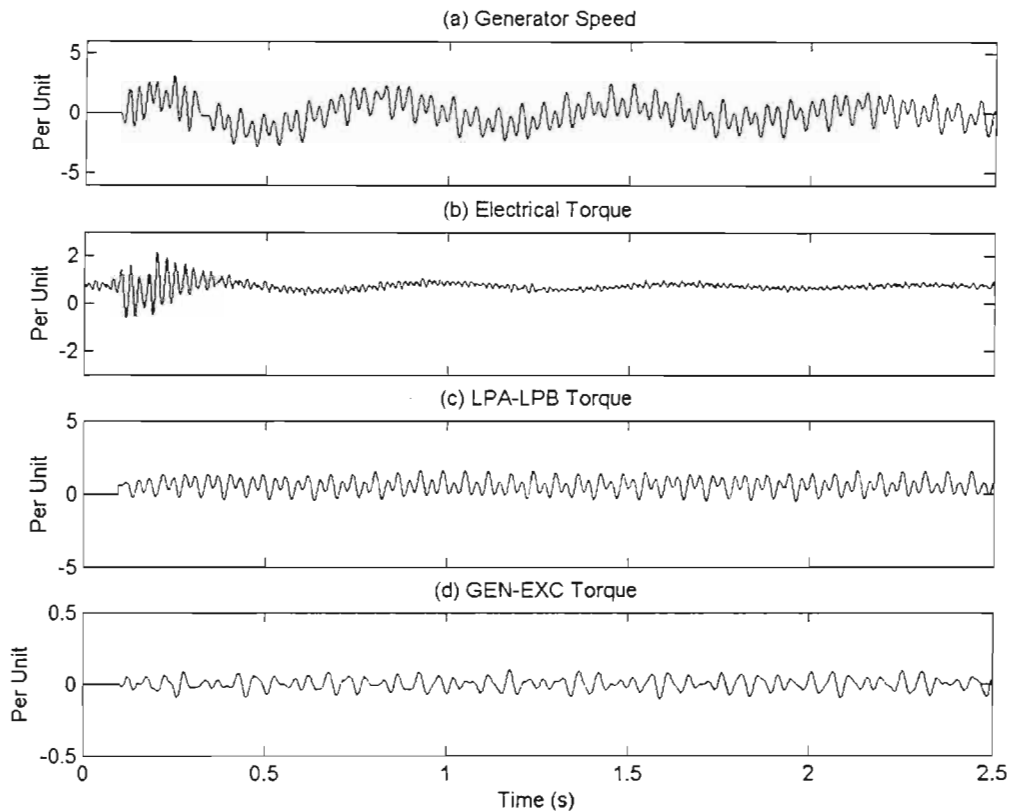


Fig.7.2: Simulated response of the IEEE First Benchmark Model to a short circuit fault for the three-level SSSC compensated transmission system at $X_q^ = 0.275$ pu.*

$$X_q^* = 0.3707 \text{ pu}$$

As predicted in the previous chapter, the resonant frequency, f_{er} , in the transmission line caused by an SSSC at a commanded capacitive reactance of $X_q^* = 0.3707$ pu is 30.5 Hz and the associated subsynchronous complementary frequency, $f_o - f_{er}$, is 29.5 Hz. With reference to Table 7.1, the complementary frequency of the system at this value of compensation lies in between the mechanical natural frequencies of Mode 3 and Mode 4, but is closer to that of Mode 4.

Fig 7.3 shows the simulated results of the three-level SSSC-compensated line to the short circuit disturbance at $X_q^* = 0.3707$ pu. The results in Fig. 7.3 show that at this value of compensation

the system is clearly experiencing negatively damped torsional oscillations. A careful frequency-domain analysis of these results (not shown here) has shown that the mechanical system oscillations are once again multi-modal in character, comprising oscillations at both the Mode 1 and Mode 4 frequencies, but that the Mode 4 frequency is predominant. Thus, at a value of $X_q^* = 0.3707$ pu the three-level SSSC results in significant destabilization of the Mode 4 torsional mode as well as provoking noticeable oscillations in Mode 1.

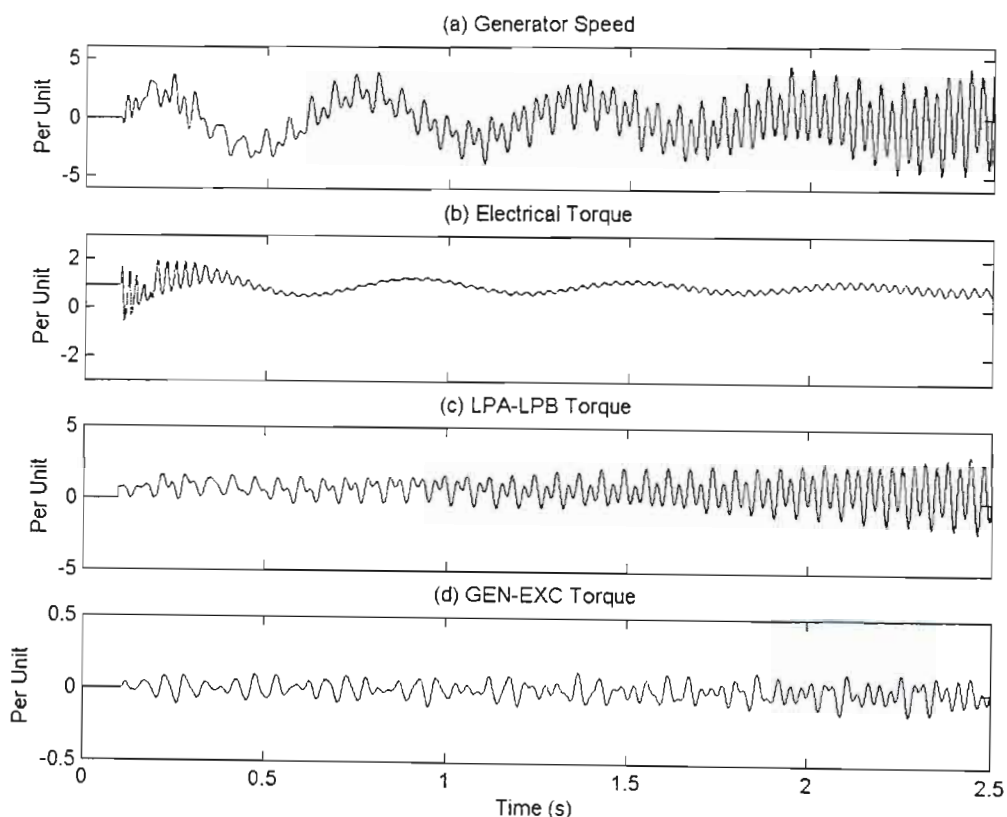


Fig.7.3: Simulated response of the IEEE First Benchmark Model to a short circuit fault for the three-level SSSC compensated transmission system at $X_q^ = 0.3707$ pu.*

The previous three simulation studies have considered the responses of the three-level SSSC compensated transmission system following a three-phase fault, with different commanded compensating capacitive reactance values. The results are in agreement with the conclusions drawn in Chapter Six:

1. Due to the different susceptibility of the torsional modes of a turbine shaft to torsional interaction, it is possible that the close tuning of the subsynchronous electrical

complementary frequency to that of a particular mechanical mode may not, in fact, affect that mode but instead interact with the other modes.

2. Although at some compensation levels the SSSC does not cause instability in the electro-mechanical system, it is evident that it still excites shaft torque oscillations. While this is true in some cases, at other compensation levels, the SSSC clearly causes large negatively damped oscillations following a disturbance. Therefore, in the SSR study, it is paramount to examine the resonant characteristics of a compensating device by investigating a range of compensation values.

In the previous three studies it has been shown that, at all of the compensating reactance values considered, the Mode 4 frequency of 32.3 Hz is present in the response of the mechanical system variables following a disturbance, and that it is often the dominant frequency. It is therefore sensible to try and damp out the response of this highly susceptible mode in order to provide stability to the electro-mechanical system. The following section will describe the design of a supplementary controller for the three-level SSSC to damp out Mode 4's torsional oscillations.

7.3 Supplementary Damping Controller

It has been shown in the previous chapter that when an SSSC is used to provide a fixed degree of series compensation to a transmission line (i.e. constant X_q) there is a subsynchronous resonant minimum in the line impedance similar in characteristic to that caused by conventional dielectric series capacitor compensation, and that for this reason an SSSC can give rise to SSR. If a generator feeding such a transmission system has a multi-inertia turbine shaft, subsynchronous frequency components will be present in the generator voltages due to torsional oscillations of its shaft, and these in turn will give rise to subsynchronous components of transmission line current. If these subsynchronous components of transmission line current coincide with the frequency of a resonant minimum in the line impedance, they can result in large components of air gap torque in the generator which may be phased to sustain the original torsional oscillations, resulting in unstable SSR. Since the SSSC has the capability to dynamically control its own ac output voltages, the possibility exists that its output voltages could be controlled in a supplementary fashion (i.e. over and above the normal SSSC controls) to counter the flow of subsynchronous frequency currents in the line.

7.3.1 Design Philosophy

One proposed method [65] to carry out supplementary damping control is shown in Fig. 7.4 where the supplementary controller is similar in structure to a power system stabilizer (PSS). In the implementation in this thesis of the idea proposed in [65], the input to the supplementary SSSC controller is the generator rotor's speed deviation, $\Delta\omega$, which is passed through two lead compensators and a gain block to form an output ΔX_q which modulates the commanded compensating reactance of the SSSC around some set point X_{q0} .

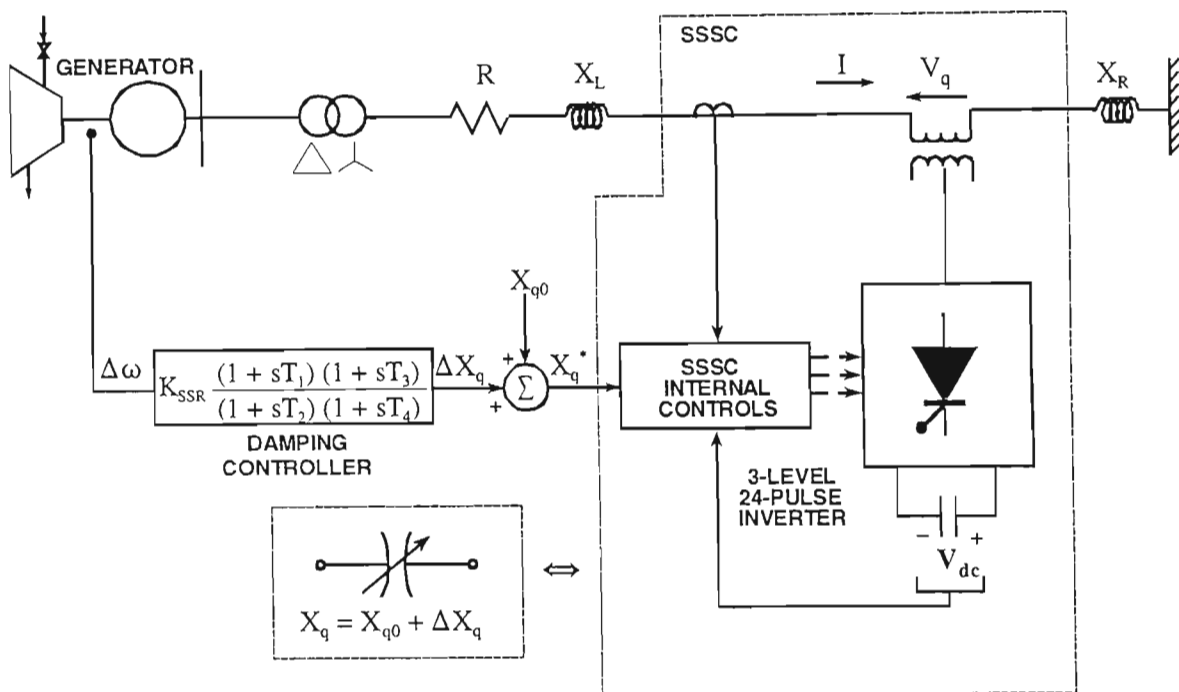


Fig.7.4: Three-level SSSC with supplementary damping controls in the IEEE First Benchmark Model transmission system.

The approach used in this thesis to design the SSSC's supplementary controls is similar to that used in PSS design: the intention is to modulate ΔX_q in such a way as to produce a positive component of damping torque in the air gap of the generator in order to dissipate the energy of any torsional oscillations caused by interaction between the generator and resonances in the line impedance. In other words, if the generator rotor's speed oscillates at some subsynchronous frequency due to torsional motion, the damping controller should command a modulation ΔX_q in the SSSC's compensating reactance in such a way as to produce a component of torque deviation ΔT_e in the air gap of the generator that is *in phase* with the original subsynchronous oscillation in speed (such a torque deviation is then, by definition, a pure damping torque at that frequency).

7.3.2 Design Procedure

Having established the resonant characteristics of the SSSC-compensated benchmark system without any supplementary damping controls in section 7.2, it was concluded that the torsional mode that is most significantly affected by torsional interaction with the SSSC, at all values of X_q^* , is Mode 4, although the severity of instability in this mode increases at higher compensation levels. A study was then conducted to determine if sufficient damping could be added to the Mode 4 oscillations via supplementary damping control using the SSSC. This section now focuses on the design of such a damping controller for the specific value of SSSC compensating capacitive reactance of $X_q^* = 0.3707$ pu, which corresponds to the worst-case instability in Mode 4 in the analyses of the previous section.

In order to implement the SSSC supplementary damping control based on the approach described above, three basic design steps, using the full PSCAD/EMTDC system simulation model, were employed:

1. First, a small-amplitude sinusoidal test modulation signal at the torsional frequency of interest (in this case, the Mode 4 frequency of 32.285 Hz) was injected at the input ΔX_q to the SSSC as shown in Fig. 7.5. The phase lag between this ΔX_q signal and the resulting oscillations ΔT_e in generator electrical torque were then measured. During this part of the test the inertia constant of the generator in the IEEE First Benchmark Model was temporarily set to a very large value in order to prevent the steady-state oscillations in the electrical torque from influencing the speed and rotor angle of the generator – this artificial decoupling technique is the same as that often used when measuring the phase response of a generator for power system stabilizer design purposes.
2. After the open-loop phase lag between the controller input ΔX_q and electrical torque ΔT_e had thus been measured at the frequency of interest, a suitable compensator was then designed to provide phase lead to counteract this phase lag (in other words, the values of time constants T_1 to T_4 in the supplementary damping controller of Fig. 7.4 were so designed). The details of the lead compensator design method are described in Appendix H.
3. Finally, the closed-loop supplementary damping control scheme shown in Fig. 7.4 was then implemented using this lead compensator design on the IEEE First Benchmark Model for the design value of SSSC compensation of $X_q^* = 0.3707$, and its performance evaluated for a range of values of damping controller gain K_{SSR} .

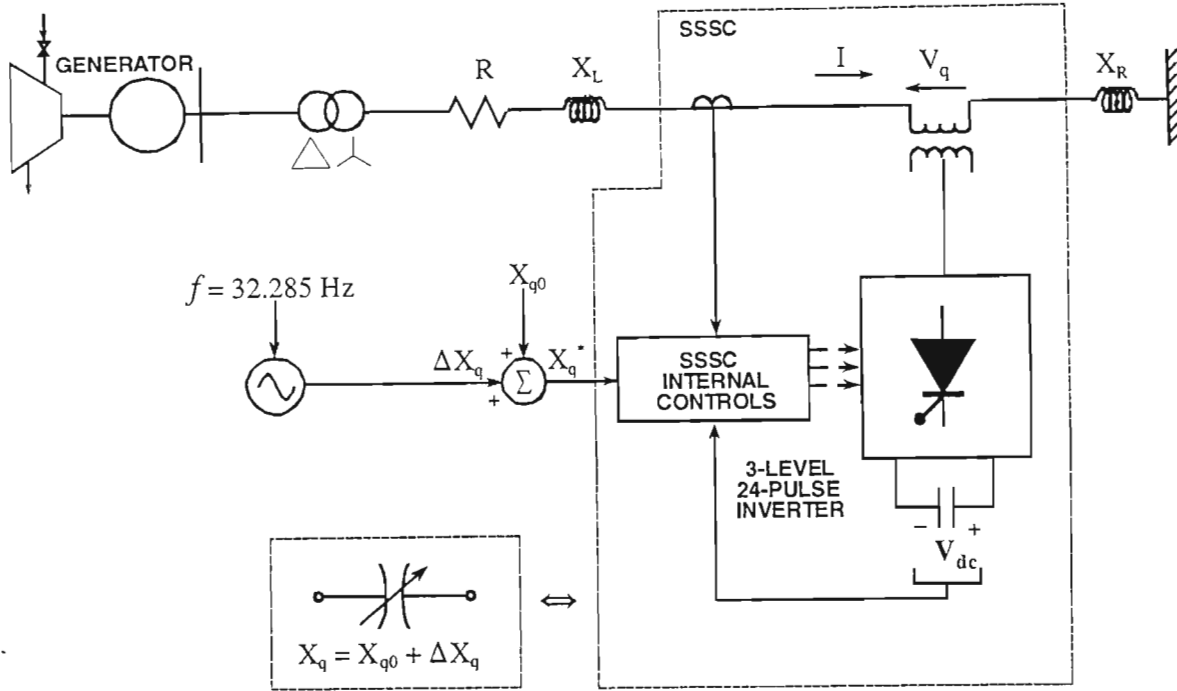


Fig.7.5: The first step of the SSSC supplementary damping controller design where a small-amplitude sinusoidal test modulation signal is injected into the input of ΔX_q .

7.3.3 Performance Of SSR Damping Control

With the SSSC supplementary damping controller having been designed to damp out Mode 4 oscillations, this section now compares the SSR characteristics of the SSSC, with and without supplementary damping controls, and for different gains of this damping controller.

Fig. 7.6 shows the SSR characteristics of the First Benchmark Model when the SSSC is providing a set-point value of compensation $X_{q0} = 0.3707\text{pu}$, but compares the situation when there are no supplementary controls ($K_{SSR} = 0$) to that when the supplementary controls are activated with a gain $K_{SSR} = 0.1$. As has already been seen in Fig. 7.3, the SSSC compensated system is unstable with no supplementary controls. However, Fig. 7.6 now shows that with the damping controls added, the Mode 4 torsional oscillations in the mechanical shaft and electrical torque are clearly more positively damped. Furthermore, the oscillations in the generator speed deviation, LPA-LPB and GEN-EXC torques, shown in Fig. 7.6(b) (e) and (f) respectively, now clearly contain predominately the Mode 1 frequency of 15.71 Hz with significantly less influence from the Mode 4 frequency. Fig. 7.6(a) also illustrates how this has been achieved: the commanded value of X_q^* at the input to the SSSC is modulated in sympathy with the oscillations in the

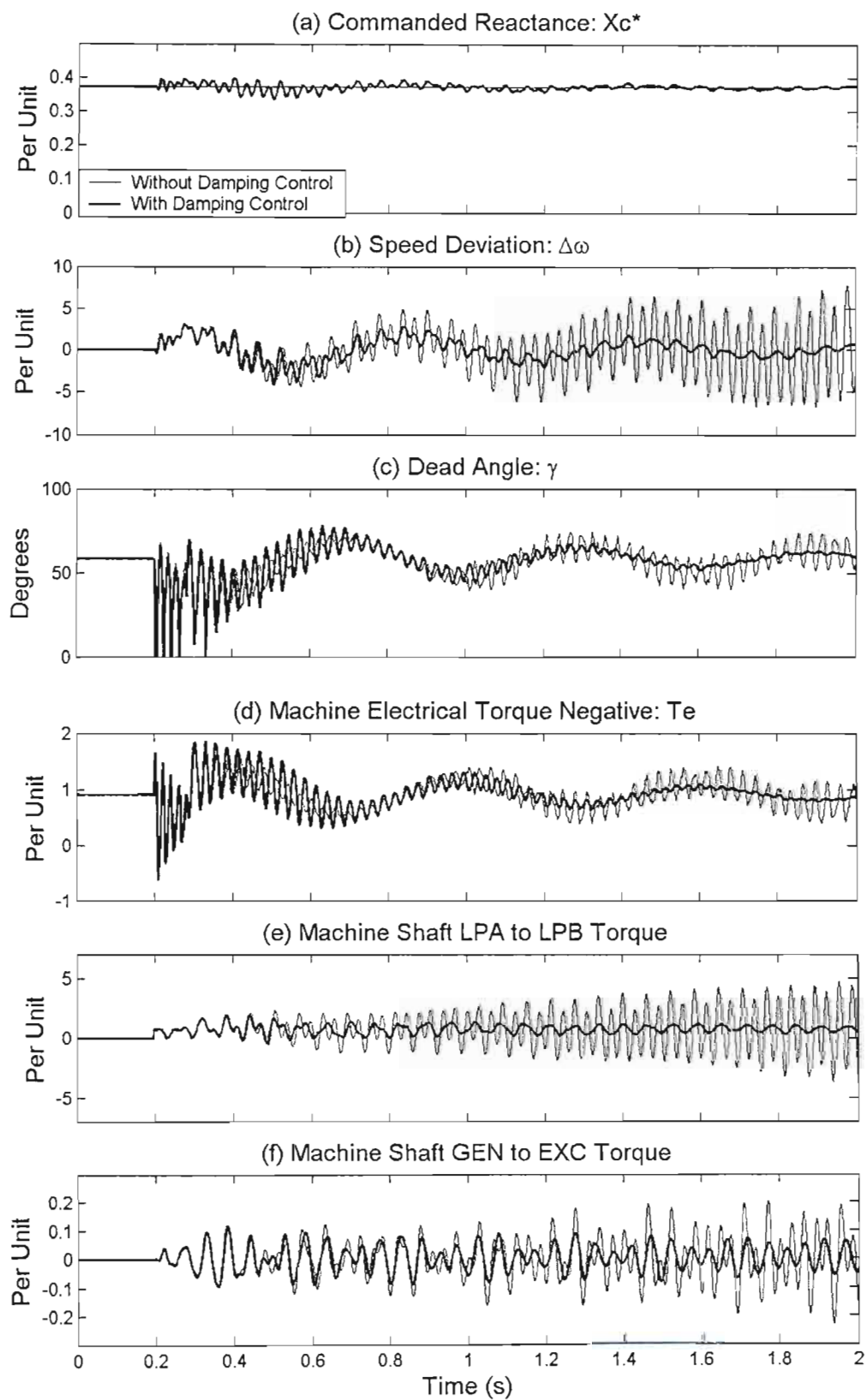


Fig. 7.6: Performance of the SSSC compensated IEEE Benchmark Model transmission system with no damping control and with damping control and $K_{SSR} = 0.1$; $X_{q0} = 0.3707$ pu.

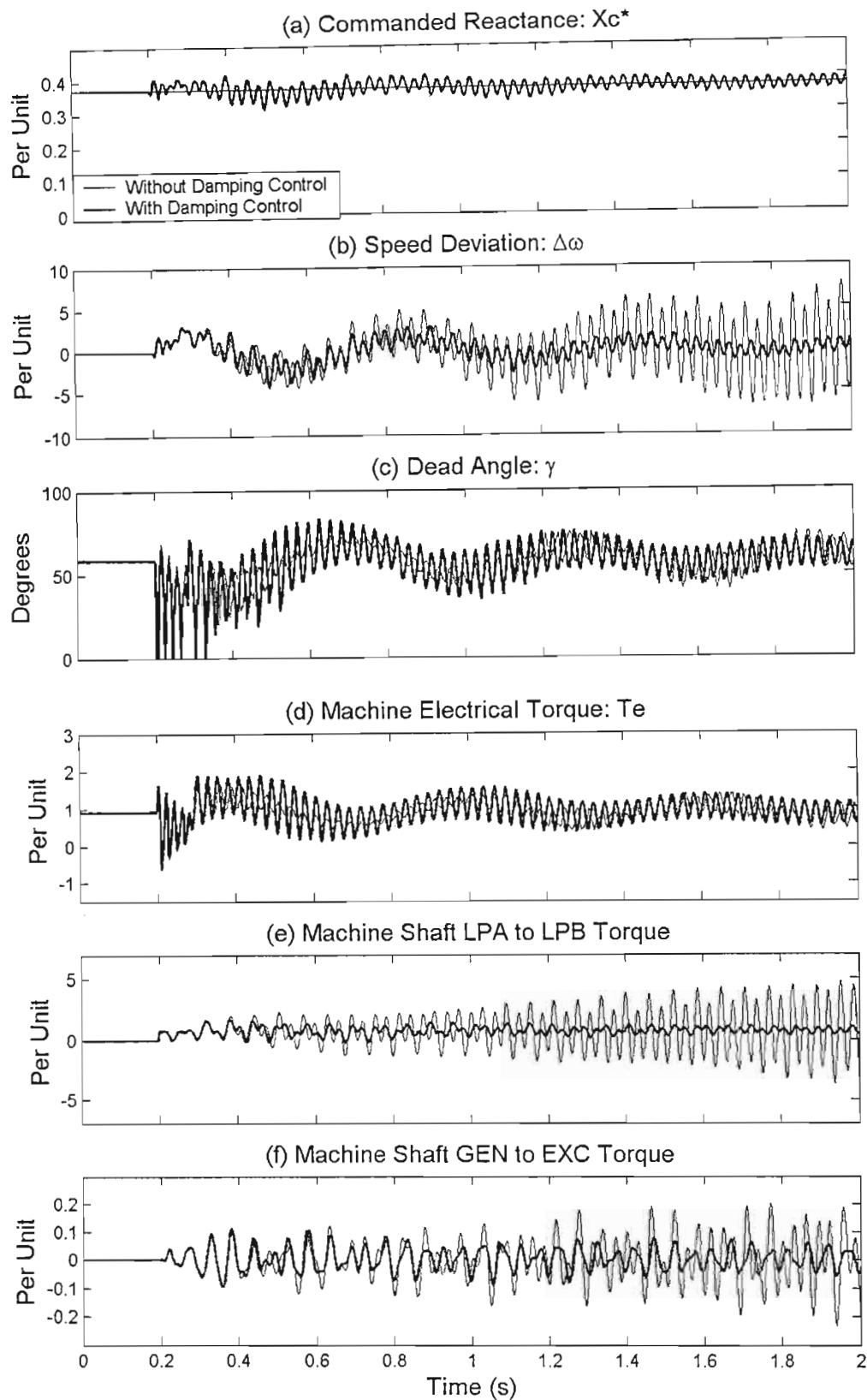


Fig. 7.7: Performance of the SSSC compensated IEEE Benchmark Model transmission system with no damping control and with damping control and $K_{SSR} = 0.15$; $X_{q0} = 0.3707$ pu.

generator's speed deviation; the resulting modulation in the inverter's dead angle γ is also shown in Fig. 7.6 (c).

Although there is a clear stabilizing influence from the damping controller evident in Fig. 7.6, the torsional oscillations still persist for several seconds after the disturbance even with the damping controller activated. Fig. 7.7 therefore considers whether further improvement in the damping of the torsional oscillations can be obtained by increasing the supplementary controller's gain K_{SSR} .

Fig. 7.7 now shows the SSR characteristics for $X_{q0} = 0.3707$ pu but compares the fixed SSSC compensation ($K_{SSR} = 0$) to modulated compensation with $K_{SSR} = 0.15$. The results show that there is in fact further reduction in the amplitude of the Mode 1 (15 Hz) shaft torsional oscillations at the increased value of gain (c.f. Fig. 7.6); however, this comes at the expense of larger excursions in the compensating reactance and generator electrical torque during, and after the application of the fault in the transmission line. Also, there appears to be a less-damped higher frequency mode present in the speed deviation signal in Fig. 7.7 that is not as evident in Fig. 7.6. Thus, while in principle it is possible to add significant damping to the torsional oscillations using the SSSC's supplementary controller, careful consideration would be required to apply appropriate limits to the magnitude of ΔX_q commanded at the output of such controls.

7.4 Performance Of The Damping Controller At Different Values Of X_q

The previous section considered the performance of a supplementary controller that was designed to damp out Mode 4 torsional oscillations at a specific value of SSSC compensation of $X_q^* = 0.3707$. It was shown that with proper supplementary damping control using the controller structure proposed in [65], the three-level SSSC can successfully damp a single torsional mode in a benchmark study system using a realistic representation of the SSSC's inverter.

This section investigates whether or not the same supplementary controller designed for the specific value of SSSC compensating reactance of $X_q^* = 0.3707$ can still be employed to provide damping to the system when the SSSC's compensating reactance is changed to values different from that at which the damping controller was designed. This is an important consideration, since the whole point of an SSSC is to provide compensating reactance whose value can be adjusted; although [65] considered different degrees of compensation, this was achieved by studying a combination of different values of *conventional* series compensation with a *single* value of SSSC compensation.

It was shown in section 7.2 that for lower values of compensation, such as $X_q^* = 0.178$ pu, the damping of the torsional modes in the study system was not of concern. Thus, in the following studies, the values of compensation chosen for further study are $X_q^* = 0.245$ pu, $X_q^* = 0.315$ pu and $X_q^* = 0.385$ pu; these values span the range of compensating reactances for which torsional oscillations were shown to be a concern in Fig. 7.2 and Fig. 7.3 earlier.

As in the previous simulation studies, the response of the system at each of these values of X_q^* to a three-phase fault of duration 0.075 seconds was considered. The responses of four system variables from the PSCAD/EMTDC simulation, namely, generator speed, the electrical torque, the LPA–LPB turbine shaft torque and the GEN–EXC shaft torque with no damping controller, and with damping control and gain $K_{SSR} = 0.1$ are shown in each study.

This section now compares the SSR characteristics of the SSSC form of compensation with and without supplementary damping controls, and for different values of compensating reactance, when the supplementary controller has been designed to damp out Mode 4 oscillations at a specific value of $X_q^* = 0.3707$ pu. (Note: when examining the variables in the following plots, the oscillations may appear to exhibit higher amplitudes than in previous plots; however, this is simply because the scales on the plots have been adjusted from those used previously in the chapter.)

Fig. 7.8 shows the SSR characteristics of the First Benchmark Model when the SSSC is providing compensation of $X_q^* = 0.245$ pu. Fig. 7.8 also compares the situation when there are no supplementary controls ($K_{SSR} = 0$) to that when the supplementary controls are activated with a gain of $K_{SSR} = 0.1$. It is clear that the system does not exhibit negative damping even when the supplementary damping controls are disabled. However, with the supplementary damping controls enabled, there are noticeable (but not pronounced) improvements in the damping of all four system variables.

In Fig. 7.9, when the SSSC is providing a compensating reactance of $X_q^* = 0.315$ pu, there is a gradual increase in the amplitudes of the oscillations in all the variables when there is no supplementary damping control; this is particularly evident in the generator speed and LPA–LPB torque, as shown in Fig. 7.9 (a) and (c). Once again, with the supplementary damping controls activated, the damping of all the system variables is noticeably improved, to the extent that the system is no longer negatively damped at this value of X_q^* with supplementary damping control.

When the SSSC is providing a compensating reactance of $X_q^* = 0.385$ pu, with no supplementary controls, it is obvious that the system is extremely negatively damped from the post-fault response

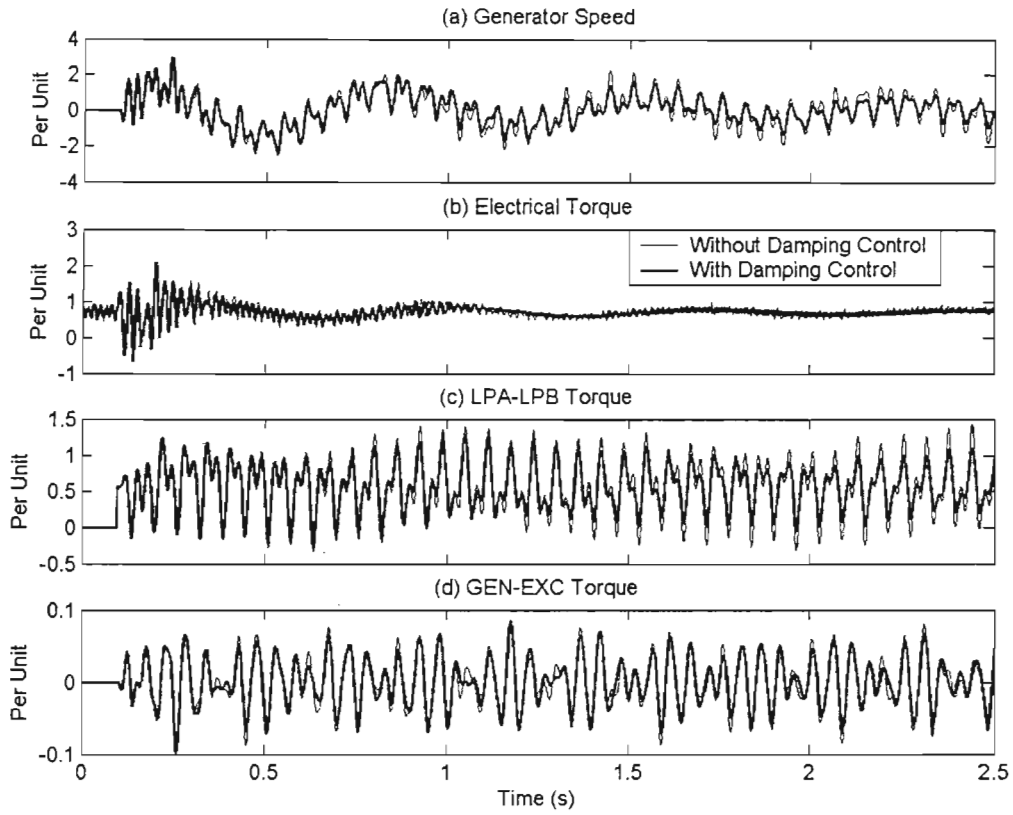


Fig. 7.8: Performance of the SSSC compensated IEEE Benchmark Model transmission system at $X_{q0} = 0.245$ pu with no supplementary damping control and with damping control and gain $K_{SSR} = 0.1$.

shown in Fig. 7.10. However, when the supplementary control is activated at this value of X_q^* , all system variables are once again positively damped and the stability is restored. It should be noted that in Fig. 7.10 (and in some of the other results shown in this chapter) the amplitudes of the generator electrical torques during, and immediately after the fault are significant when the SSSC's supplementary damping controls are activated. However, it should also be noted that in this time period the controller is responding to large excursions in the system variables which it should not, ideally, be trying to influence. Ideally, a small signal damping controller such as this should have its output limited in some manner to prevent such impact on the system during large-signal transients, whilst still allowing it to positively influence the small signal behaviour of the system once the large-signal response is over.

The above investigation has presented three sets of SSR studies of the three-level SSSC with different commanded capacitive compensation reactance values. The investigations compared

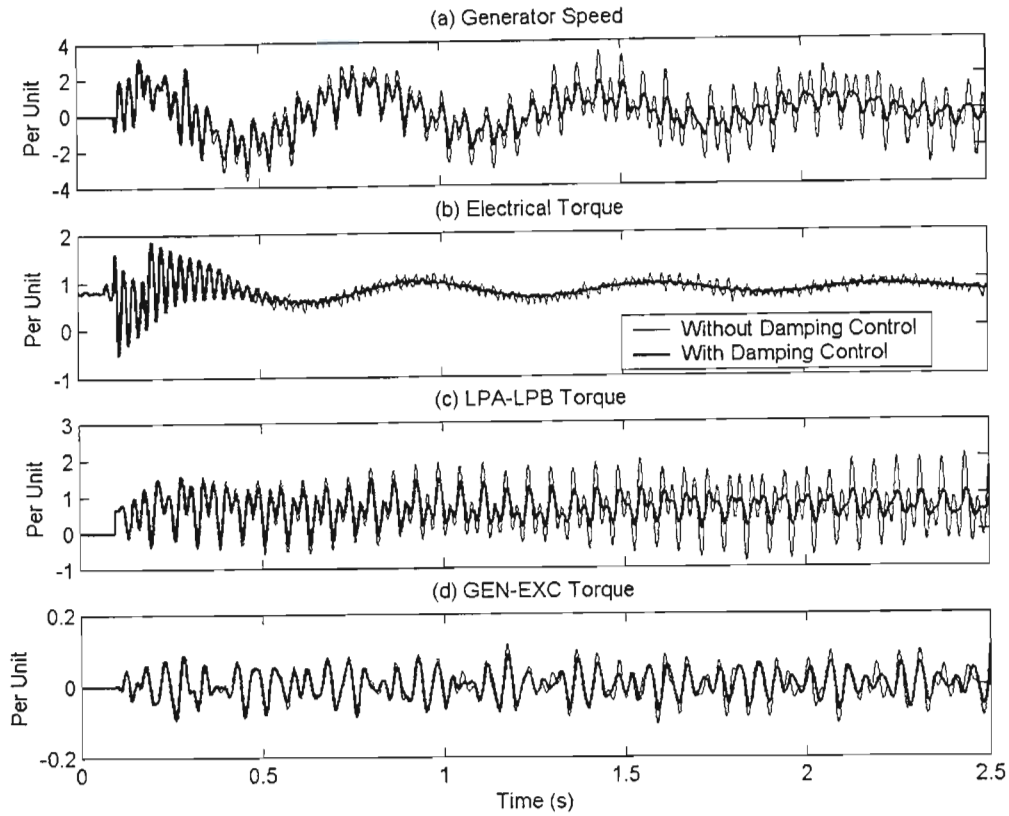


Fig. 7.9: Performance of the SSSC compensated IEEE Benchmark Model transmission system at $X_{q0} = 0.315$ pu with no supplementary damping control and with damping control and gain $K_{SSR} = 0.1$.

the response of the system when no supplementary damping control is provided, to that when the supplementary damping controller designed in section 7.3 is activated. It is observed that the supplementary controller designed for a single value of compensating reactance of $X_q^* = 0.3707$ pu still provides positive damping to the system when the value of X_q^* is changed from the design value. Although this fixed-design supplementary controller did not provide significant damping to the system for lower values of X_q^* , it did not negatively affect the stability of the system at those values of X_q^* . Furthermore, the supplementary damping controller was shown to be able to stabilize negatively-damped torsional oscillations in the First Benchmark Model for values of X_q^* other than that for which it was designed. Thus it can be concluded that the SSSC, with a single, fixed design of supplementary damping controller, could be used over a range of compensation values in the First Benchmark Model. However, the results have also shown that further refinement of the supplementary damping controller is required to limit its output under larger signal conditions, particularly at large values of X_q^* .

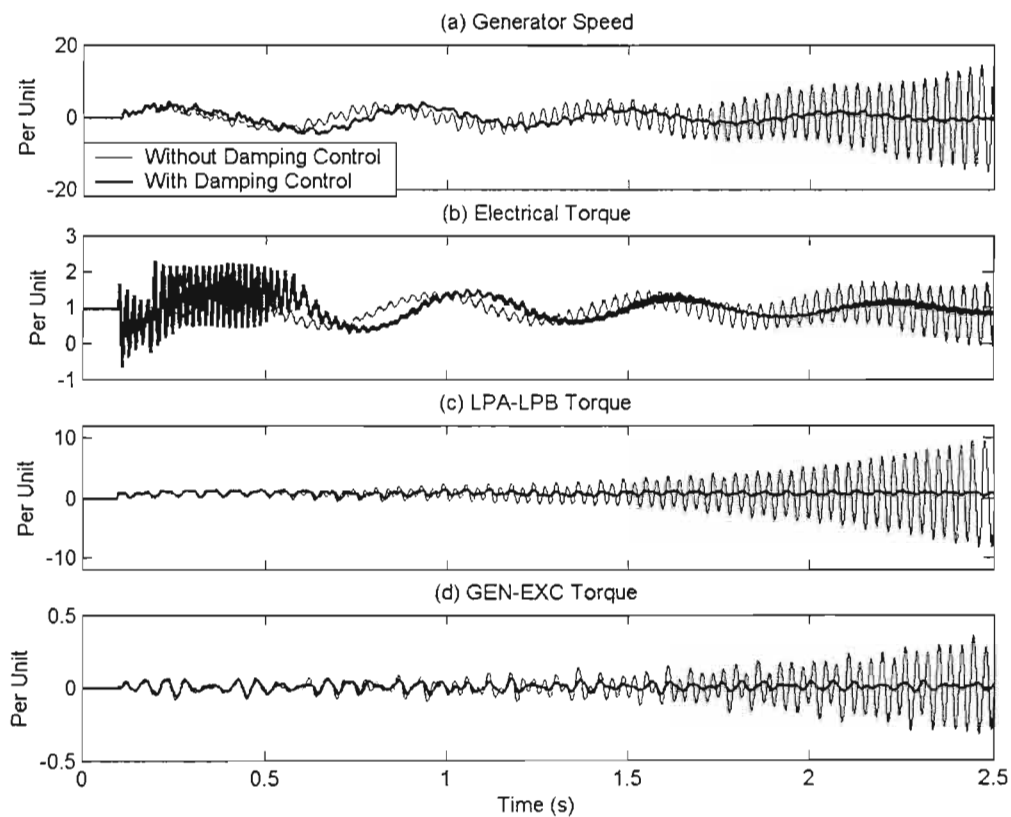


Fig. 7.10: Performance of the SSSC compensated IEEE Benchmark Model transmission system at $X_{q0} = 0.385$ pu with no supplementary damping control and with damping control and gain $K_{SSR} = 0.1$.

7.5 Conclusion

This chapter began by confirming the characteristics of a three-level SSSC in the IEEE First Benchmark Model, using the detailed model of the SSSC developed in Chapter Three. It was found that, like the two-level SSSC, the electrical resonant frequency caused by the three-level SSSC may excite one or more mechanical torsional modes and instability may be the result of such interaction. Furthermore, even when the SSSC does not cause large persistent oscillations, it still excites the shaft torque oscillations to some extent.

After establishing the resonant behaviour of the three-level SSSC, the chapter described the design and implementation of a supplementary damping controller for this SSSC based on the idea proposed in reference [65]. This study has focused on designing a supplementary controller

to damp out the Mode 4 torsional oscillations in the IEEE First Benchmark Model for a specific value of the compensating reactance of the SSSC of $X_q^* = 0.3707$ pu. The design showed promising results as the supplementary controller successfully damped the Mode 4 oscillations and stabilized the system at its design operating point.

The chapter then considered the performance of this fixed-design supplementary controller for the SSSC at values of SSSC compensation other than that at which the controller design was originally carried out. The results of these studies have shown that a single-design supplementary damping controller, added to the SSSC, can allow it to operate over a range of values of series compensating reactance without causing SSR; furthermore, the damping controller does not negatively impact on the system damping for values of SSSC compensation that are already stable without supplementary control. Thus it can be concluded that a carefully-considered, single-design damping controller added to a conventional SSSC can extend the operating ranging over which the device can be used without causing SSR, when the SSSC is the only form of compensation (i.e. the only source of resonance) in the transmission line. This finding differs from, and adds to, that of [65] in that the results in [65] used the SSSC at a single value of compensation purely to damp SSR caused primarily by conventional capacitors. The studies in this chapter show that the idea proposed in [65] can also be used to extend the safe variable-compensation operating range of the SSSC itself in systems where SSR is a concern and where only SSSC compensation is to be used. Furthermore, the results presented have represented the SSSC's power electronics in detail and considered a known SSR benchmark study system for analysis, adding further weight to the findings of [65].

The results of this chapter have shown that, with the aid of a supplementary controller, the three-level SSSC is able to damp out unwanted oscillations caused by the SSSC itself. However, it may be desirable, for economic reasons, to include a combination of SSSC and conventional series compensation in a transmission line, in cases where only a fraction of line compensation needs to be controllable. The following chapter therefore considers the resonant characteristics of the SSSC when combined with conventional series capacitors.

CHAPTER EIGHT

SUPPLEMENTARY DAMPING CONTROL FOR A CONVENTIONAL CAPACITOR AND SSSC COMPENSATED LINE

8.1 Introduction

When the concept of the SSSC was first proposed, it was intended to replace a dielectric capacitor by injecting an ac voltage that was almost in quadrature with the line current. It was thought that the SSSC would be immune to SSR and therefore, with its fast response to control commands, this more sophisticated form of compensation would be ideal in practice. However, Chapter Six has confirmed the work of others in showing that this is not the case, as the SSSC shows similar resonant characteristics to conventional capacitors, and the possibility of SSR is therefore inescapable. Hence, the previous chapter considered the SSSC not only as a compensator but also as a “suppressor of incipient SSR instability” [65]. Chapter Seven showed that with appropriate design, a supplementary controller added to the three-level SSSC was successful in damping out system resonances caused by the SSSC itself for a range of compensating values, X_q^* .

Although the flexibility and capability of an SSSC remains highly attractive, due to cost, more affordable conventional capacitors are likely to make up large portions of the total series capacitive compensation in transmission lines. This chapter now considers a transmission system compensated by a combination of the SSSC and conventional series capacitors. The aim is to examine, in more detail than in [65], whether or not the supplementary damping controller for the SSSC is sufficient to damp out subsynchronous oscillations caused by both the SSSC itself and the conventional capacitors.

As described in Chapter Seven, Jowder and Ooi [65] examined the performance of a radial power system compensated by a combination of SSSC and dielectric capacitors. The SSSC was fitted with supplementary controls to damp out subsynchronous oscillations caused by itself and the conventional series compensating capacitors in the transmission system. As previously

mentioned, although their supplementary controller was able to stabilize some oscillatory modes of the studied system, the model of the SSSC used did not include the detailed power electronics and low-level firing controls of the SSSC's inverter. Also, although the torsional properties of the studied turbine generator were represented in detail, the study system itself was not a benchmark system because of the particular focus of that work [65].

Reference [61] also presented a detailed study into the torsional interactions of a transmission system compensated by both an SSSC and conventional capacitors. In this work, the SSSC employed a 48-step, two-level harmonic neutralized inverter model where the detailed power electronics were represented. Also, the system used for SSR analysis was the IEEE First Benchmark Model. This study also found that with an auxiliary damping controller, the SSSC could stabilize unstable torsional modes caused by the conventional capacitors *alone* at *one* chosen operating point; the authors of [61] reached this conclusion because their study was done under the assumption that an SSSC *does not* resonate with the line inductance.

This chapter now considers whether the supplementary control scheme proposed in [65] can still provide acceptable damping of SSR when the transmission system is compensated by both the three-level SSSC and conventional series capacitors for a range of compensating reactance values. However, in order to extend the findings of both [61] and [65], the system in this chapter considers a *range* of values series compensation provided by *both* the SSSC's compensating reactance X_q and the conventional series capacitors. The SSSC model used in this chapter again includes a detailed representation of the SSSC's high-level controls, low-level firing controls and its full 24-pulse, three-level voltage source inverter topology. Furthermore, this work considers the performance of the proposed damping control system in a benchmark study system [72].

Before designing the SSSC's supplementary damping controller, it is necessary to first examine the resonant characteristics of the combination of conventional series capacitors and the SSSC over the range of compensation of interest. The following section investigates these characteristics for three particular combinations of SSSC and conventional series compensation in the IEEE First Benchmark system [72].

8.2 Resonant Characteristics Of The Dual-Compensated System

Before attempting to apply supplementary control to damp out subsynchronous oscillations, this section first examines the resonant interactions between the transmission line and the generator

shaft dynamics when the line is compensated with both conventional series capacitors and a three-level SSSC; this combined form of series compensation is hereafter referred to as dual-compensation. As in the previous chapter, all the investigations make use of the detailed PSCAD/EMTDC model of the SSSC and the system under investigation is the IEEE First Benchmark Model.

Since an infinite number of possible combinations of conventional compensation (X_c) and SSSC compensation (X_q) could have been considered for the analyses in this chapter, some method of deciding upon a manageable number of interesting scenarios was required. The approach adopted was to consider three case studies: in two of these cases, a value of conventional series compensating reactance was chosen that, on its own (i.e. without added SSSC compensation), would result in a resonant frequency in the transmission line tuned exactly to one particular torsional mode in the IEEE First Benchmark Model; in the third case, a value of conventional series reactance was chosen that on its own would result in a resonant frequency tuned *between* two torsional modes in the IEEE First Benchmark Model. Finally, in all three cases, the amount of additional SSSC compensating reactance, X_q , was chosen such that the *total* compensation $X_c + X_q$ would add up to 0.3707 pu. This value of total series compensation corresponds to that required to cause a resonant frequency in the line exactly tuned to Mode 2 when all the compensation is conventional. A summary of the three case studies, and the associated values of X_c and X_q^* , is shown in Table 8.1.

Table 8.1: Capacitor and SSSC compensating reactance values for the three case studies considered in the IEEE First Benchmark Model.

Case Study	X_c (pu)	X_q^* (pu)	$X_c + X_q^*$ (pu)
1	0.178	0.1927	0.3707
2	0.224	0.1467	0.3707
3	0.275	0.0957	0.3707

As in previous chapters, when conducting simulation studies for each of these cases, the system initially operates at steady state; a three-phase fault of duration 0.075 seconds is then applied at the receiving-end of the transmission line at $t = 0.1$ seconds. In each case, time-domain results are shown to predict the response of four system variables from the PSCAD/EMTDC simulation, namely, generator speed deviation, the electrical torque, LPA–LPB turbine shaft torque and the GEN–EXC shaft torque. In addition, the frequency spectrum of each of these variables is determined, by performing Fast Fourier Transform analysis on the time domain results, in order to be able to better understand the resonant interactions occurring in each case.

8.2.1 Case 1 – Without Supplementary Damping Control

In this case study, the individual compensating reactances of the conventional capacitor and SSSC are $X_c = 0.178$ pu and $X_q^* = 0.1927$ pu respectively, adding up to a total capacitive reactance of 0.3707 pu. Recall that in Chapter Six, it was shown that for $X_c = 0.178$ pu of conventional compensating capacitance (with no SSSC), the subsynchronous complementary frequency of the transmission line exactly matches the Mode 4 mechanical frequency of 32.285 Hz. Similarly, recall that when the transmission line is compensated solely by conventional capacitors, this total value of compensating reactance of 0.3707 pu is exactly tuned to the Mode 2 torsional frequency of 20.005 Hz.

Fig. 8.1 shows the time-domain response of the selected system variables following the disturbance for the combination of conventional and SSSC compensation in Case 1. The system is clearly unstable as the generator speed, electrical torque and mechanical shaft torques all exhibit large, negatively damped oscillations. The frequency-domain results in Fig. 8.2

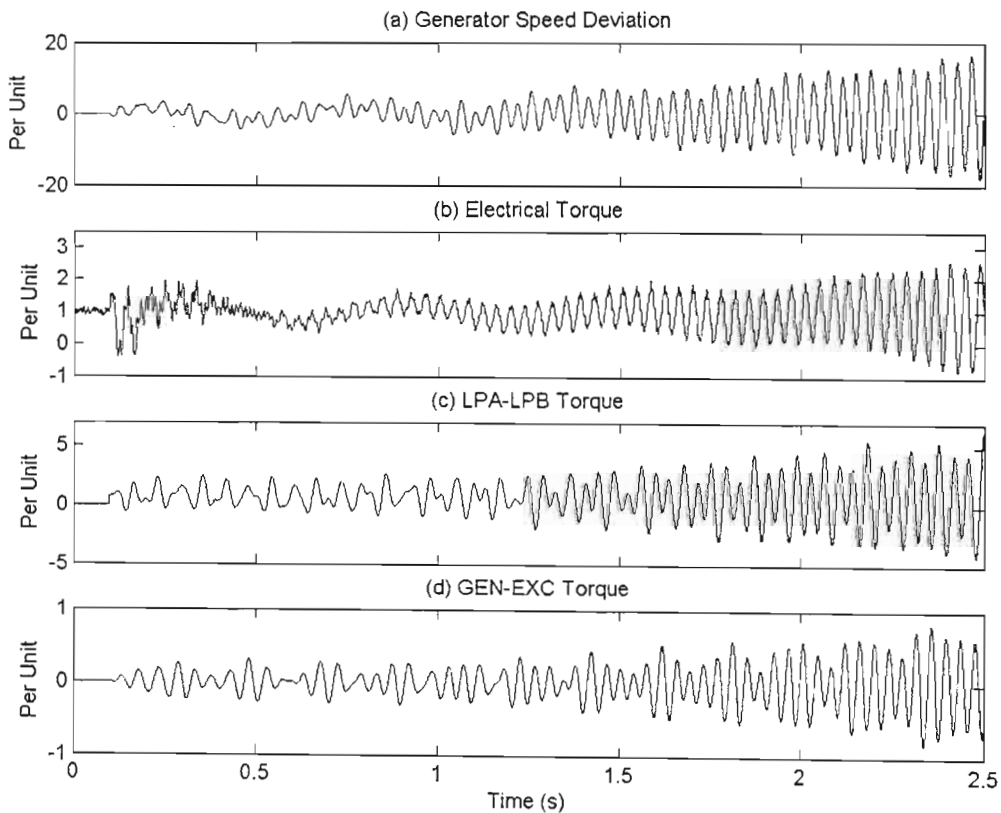


Fig.8.1: Time domain simulation results for the Case 1 dual-compensated system with no supplementary damping control.

give a clearer indication of the specific mode frequencies present in the unstable response. The FFT results in Fig. 8.2 show that the predominant subsynchronous frequency present in all of the variables' response is clearly that of Mode 3 (25.55 Hz). Although the dominance of Mode 3 seems to overshadow other modes, the effect of Mode 1 and Mode 4 is still present in both the generator speed deviation and the LPA-LPB torque, as well as Mode 2 being present in the GEN-EXC torque.

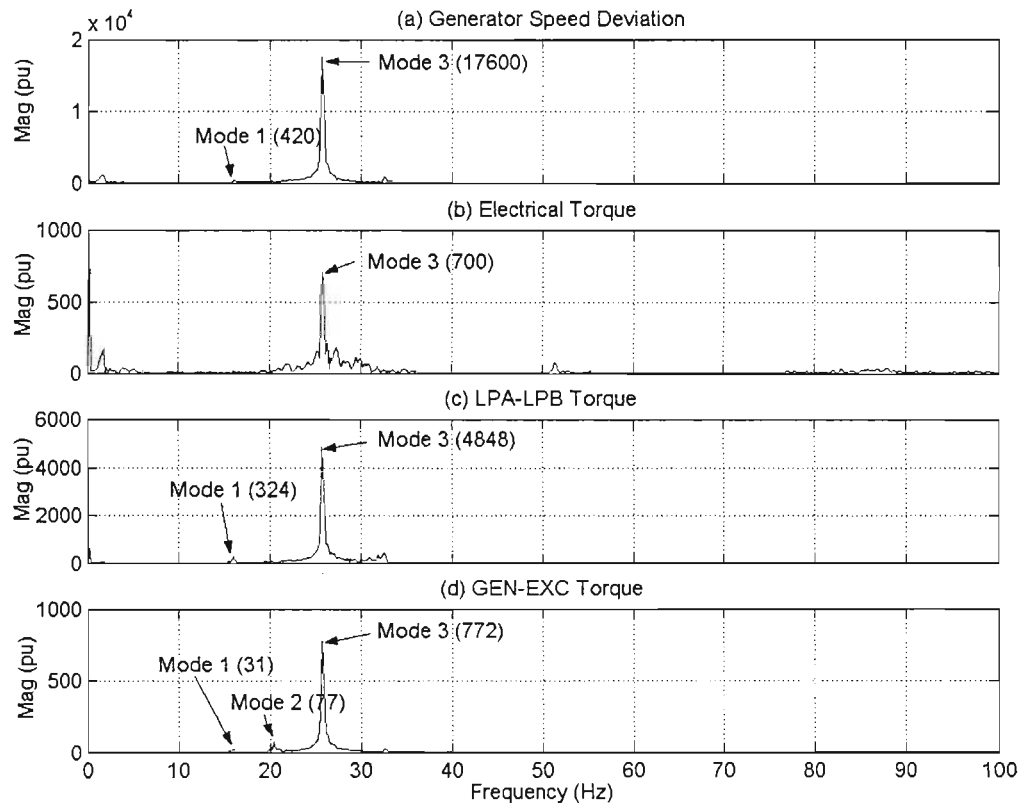


Fig.8.2: FFTs of the time-domain responses shown in Fig. 8.1.

Interestingly, the frequency of Mode 4 (32.285 Hz) is not the dominant mode in this case study, despite the fact that, without the SSSC, the conventional compensation level in this case would be exactly tuned to Mode 4. Thus, the effect of adding SSSC compensation to the conventional compensation appears to be a complex resonant condition that is distinct from the interaction that occurs between the conventional capacitors and the generator shaft modes without the SSSC present.

8.2.2 Case 2 – Without Supplementary Damping Control

In this case study, the individual compensating reactances of the conventional capacitor and SSSC are $X_c = 0.224$ pu and $X_q = 0.1467$ pu, respectively. The complementary frequency of a system compensated solely with $X_c = 0.224$ pu of conventional capacitance falls half way between the Mode 3 and Mode 4 frequencies.

Fig. 8.3 shows the time-domain response of the selected system variables following the disturbance for the combination of conventional and SSSC compensation in Case 2. The response of the system for this combination of SSSC and conventional compensation is not negatively damped as in Case 1 (c.f. Fig. 8.1), but the oscillations are nevertheless of considerable amplitude and are sustained, and are therefore clearly of concern. The FFTs of each variable in Fig. 8.3 are shown in Fig. 8.4. The FFTs of generator speed and electrical torque show that the predominant frequency component present in the response of these variables is that of Mode 3 (25.55 Hz). However, the response of the LPA–LPB torque also shows significant components of Mode 1 and 4 whilst the GEN–EXC torque, as was observed in Case 1, shows Mode 2 being the dominant frequency.

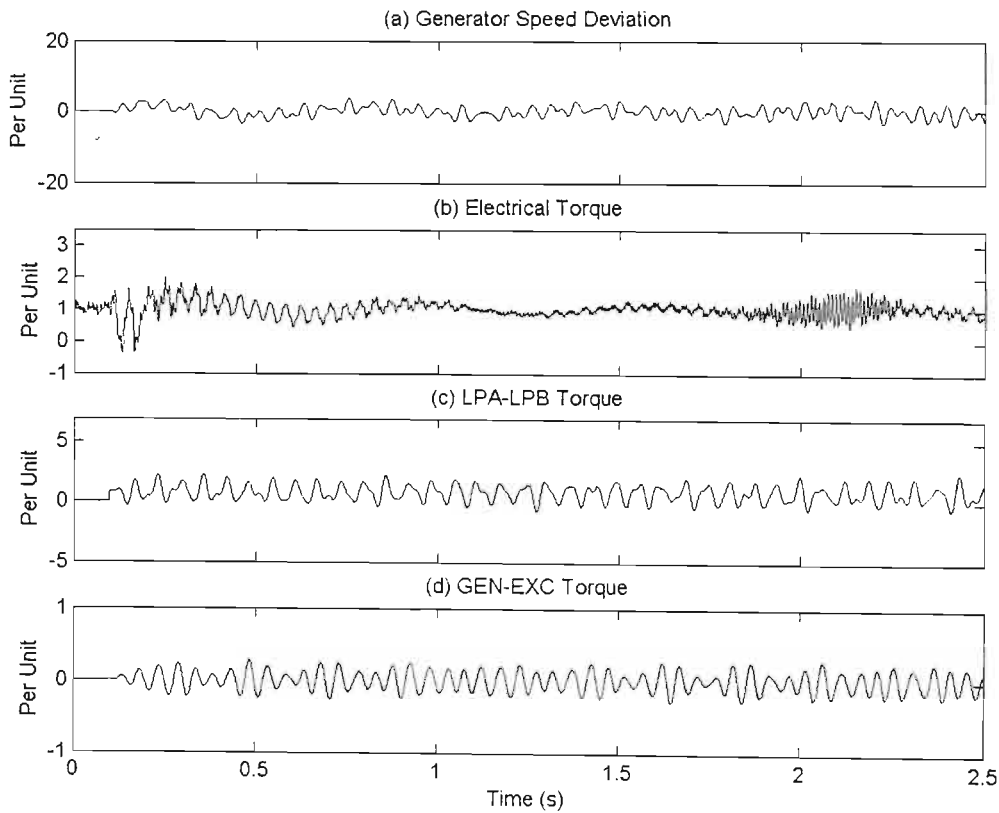


Fig.8.3: Time domain simulation results for the Case 2 dual-compensated system with no supplementary damping control.

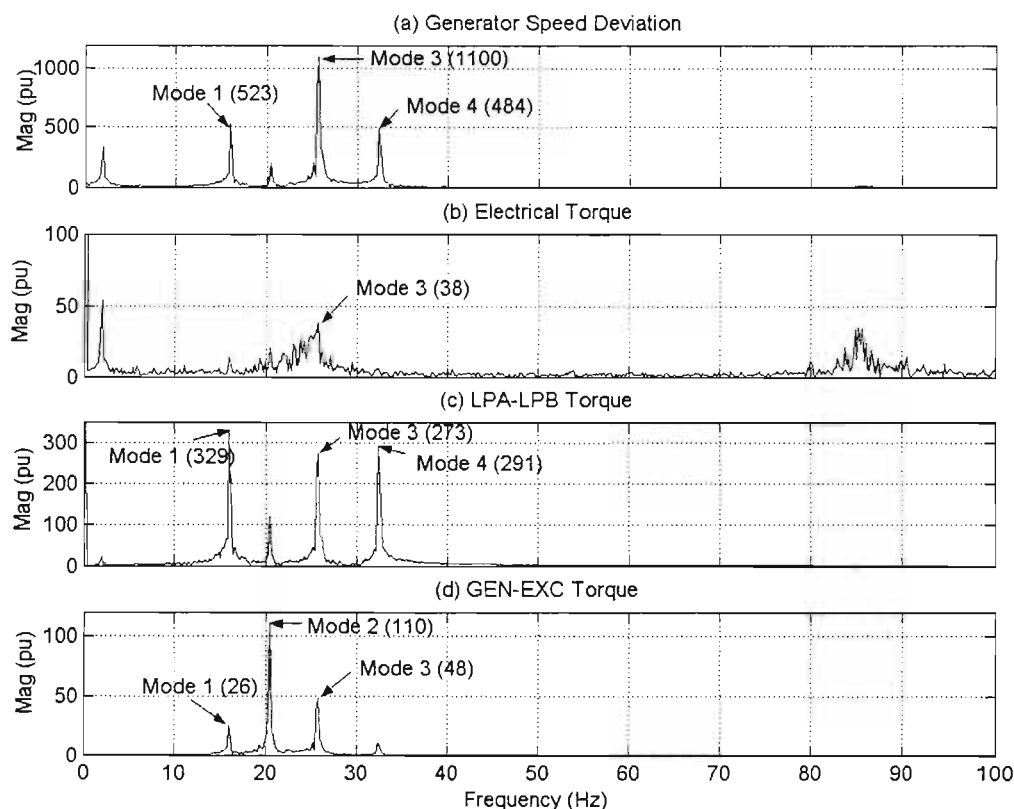


Fig.8.4: FFTs of the time-domain responses shown in Fig. 8.3.

In a transmission line compensated solely by conventional capacitors, it is expected that at this value of compensation of $X_c = 0.224$ pu the system should be relatively stable (at least in comparison with Case 1 and 3) since the natural frequency of the transmission line is not exactly tuned to any particular torsional mode. The results of Figs 8.3 and 8.4 show that for this particular case, the extra SSSC reactance inserted into the line to enhance the power flow does not have a significant destabilising effect on the system, but that the combined conventional and SSSC compensated system once again exhibits a complex, multi-modal response in which the amplitudes of the torsional oscillations following a disturbance are of concern.

8.2.3 Case 3 – Without Supplementary Damping

In this case study, the compensating reactances of the conventional capacitor and SSSC are $X_c = 0.275$ pu and $X_g = 0.0957$ pu, respectively. Recall that in Chapter Six, it was shown that for $X_c = 0.275$ pu of conventional reactance, the subsynchronous complementary frequency of the transmission line exactly matches the Mode 3 mechanical frequency of 25.55 Hz.

Fig. 8.5 shows the time-domain response of the selected system variables following the disturbance for the combination of conventional and SSSC compensation in Case 3. The FFTs of each variable in Fig. 8.5 are shown in Fig. 8.6. The results in Fig. 8.5 show that for this case the system is clearly once again negatively damped, with the oscillations in the LPA-LPB and GEN-EXC mechanical torques, in particular, noticeably increasing in amplitude with time. Also of note is the high-frequency behaviour evident in the response of the electrical torque in Fig. 8.5(b). The FFT results in Fig. 8.6(b) show that these oscillations in the electrical torque are in fact at a supersynchronous frequency of 90 Hz. The FFT results in Fig. 8.6 show that, with the exception of the GEN-EXC mechanical torque, the predominant subsynchronous frequency present in all of the variables' responses is that of Mode 1 (15.71 Hz). As in both previous cases, Fig. 8.6 shows that the predominant frequency present in the response of the GEN-EXC torque for this case is again that of Mode 2, although the Mode 1 frequency is also strongly evident in the GEN-EXC torque as well for this case.

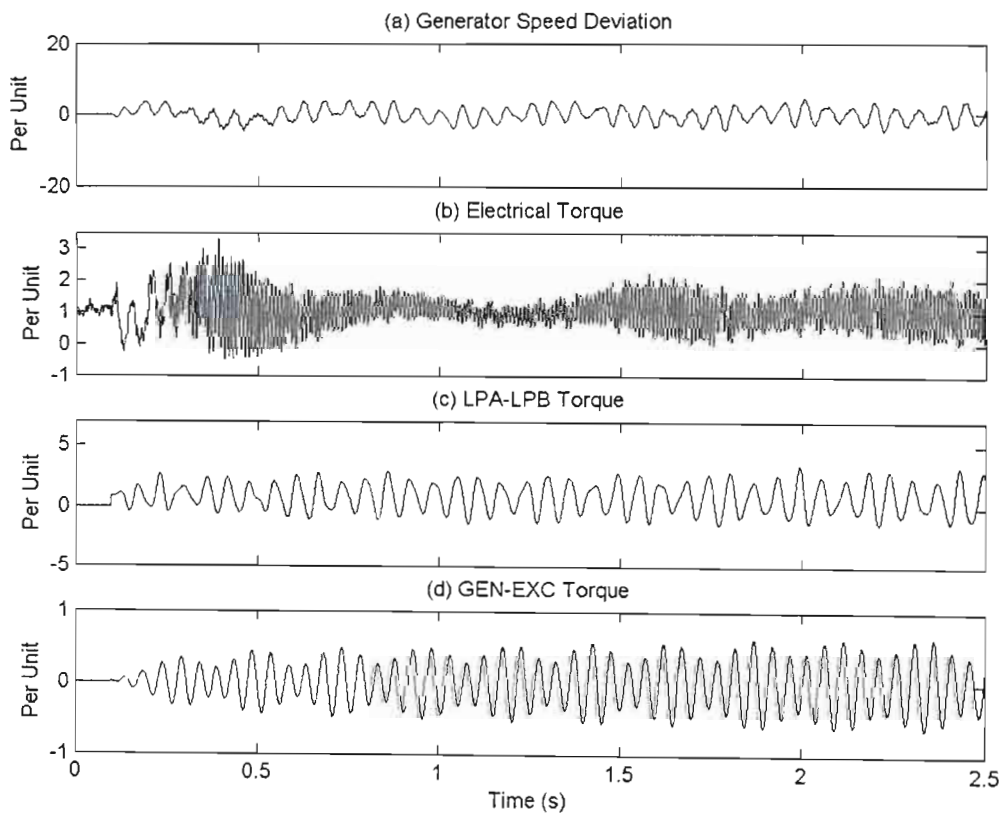


Fig.8.5: Time domain simulation results for the Case 3 dual-compensated system with no supplementary damping control.

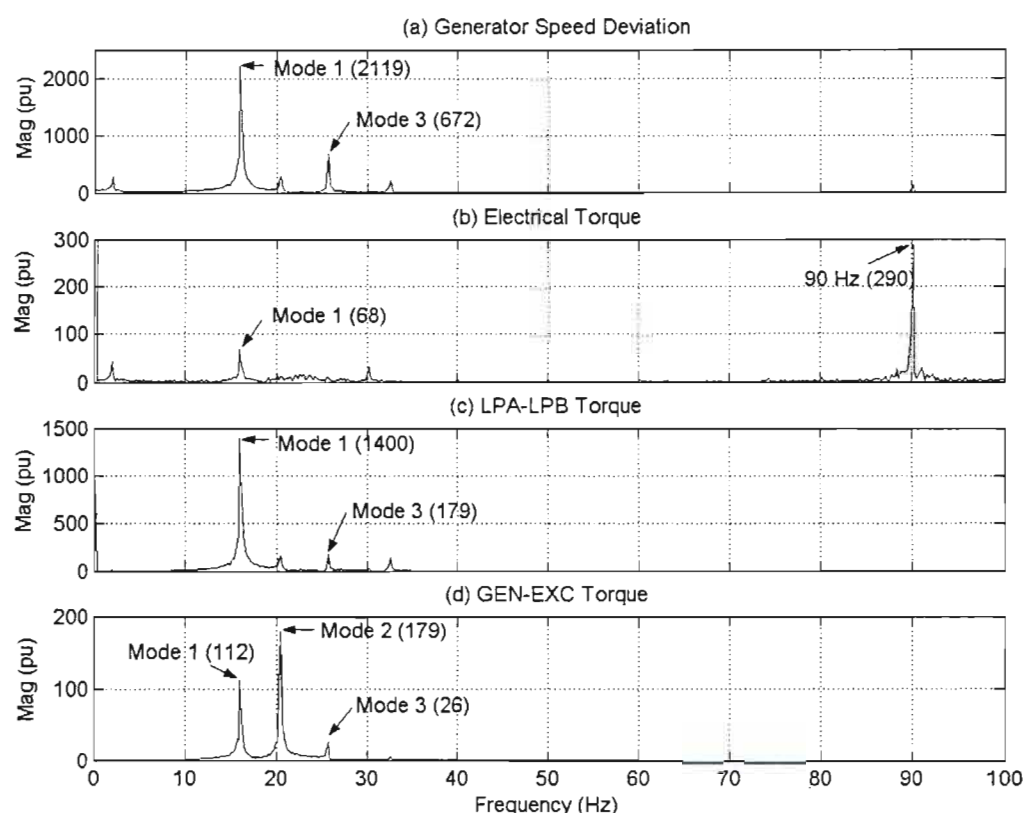


Fig.8.6: FFTs of the time-domain responses shown in Fig. 8.5.

In a transmission line compensated solely by conventional capacitors at this value of compensation of $X_c = 0.275$ pu the complementary frequency of the transmission line is exactly tuned to the Mode 3 mechanical frequency of 25.55 Hz. However, with the added capacitive reactance provided by the SSSC, the Mode 3 frequency now no longer dominates in the system oscillations; instead, it is now Mode 1 that is being strongly destabilized. Thus, as in Case 1, where the conventional compensation was, on its own, also exactly tuned to destabilise a particular mode, the additional of the SSSC has noticeably altered the resonant interactions between the conventional capacitors and the generator shaft modes.

In a transmission line compensated solely with conventional series capacitors, as shown in Chapter Six, the torsional modes that will be destabilised by a certain value of capacitive reactance are predictable. Similarly, Chapter Six showed that in a transmission line compensated solely by an SSSC, the resonant frequency in the transmission line is also relatively easy to predict and explain. However, the results in this section demonstrate that the resonant characteristics that are observed when SSSC compensation is added in series with conventional series capacitors are complex, and noticeably different from those associated with the resonances caused by the series capacitors acting alone. In particular, one distinct characteristic of dual-compensation is that the resonance is no longer dominated by one mode alone, but rather that

strong, multi-modal resonances are typically observed. This is distinct from the multi-modal resonances that may occur in conventionally compensated radial systems, where the electrical resonance in the line may be tuned to a value close to two torsional modes and destabilize them both to some extent. However, the series combination of conventional and SSSC compensation appears, rather, to destabilize multiple modes over a wide frequency range. The reason for this phenomenon is not fully understood, but could be examined by conducting impedance versus frequency scans for the dual compensated system similar to those carried out in Chapter Six. Furthermore, it can be observed that the subsynchronous characteristics of the dual-compensated system are highly dependent on the relative magnitudes of the different forms of compensation that make up the total compensating reactance.

Now that the particular resonant characteristics of the three dual-compensation cases chosen for study have been established, the following section considers the design of supplementary damping controllers for the SSSC, using the approach described in Chapter Seven, for each of these three cases.

8.3 Supplementary Control With A Single Damping Controller

The previous section has demonstrated the nature of the multi-modal resonances created when dual-compensation was employed in the transmission line of the IEEE First Benchmark Model. The previous chapter showed that a single supplementary controller applied to the SSSC could damp out *all* resonances caused by the SSSC itself (in the absence of conventional compensation). This section therefore examines whether a single supplementary damping controller can achieve a similar result, in providing positive damping and restoring stability to all modes, when applied to the system with the dual-compensation approach. The design of the supplementary controllers in each of the studies presented in this section follows the same philosophy described in Chapter Seven. For each damping controller design considered in this section, the behaviour of the system after the addition of the controller is demonstrated by showing the time-domain response of the generator speed deviation to the same disturbance considered in the previous section's studies; the FFT of this speed deviation response is also shown for each controller design to compare the ability of each controller design to reduce the amplitude of the modal oscillations of interest.

8.3.1 Case 1 – With Single-Mode Damping Controllers

The results in section 8.2.1 showed that the combination of X_c and X_q^* in Case 1, with no

supplementary damping control, gives rise to unstable SSR, and that the dominant mode in the unstable response was Mode 3, but with Mode 1 and 4 also present. This section considers whether this case can be stabilised first by adding a single supplementary damping controller designed for Mode 1, and then by adding a single controller designed for Mode 3. Figs. 8.7(a) and (b) show the response following the addition of a supplementary controller designed to add damping at the single frequency of Mode 1; Figs. 8.7(c) and (d) show the response following the addition of a supplementary controller designed to add damping at the single frequency of Mode 3. Each of these results should be compared to those shown in Figs. 8.1 and 8.2, which show the behaviour of the same Case 1 with no supplementary control.

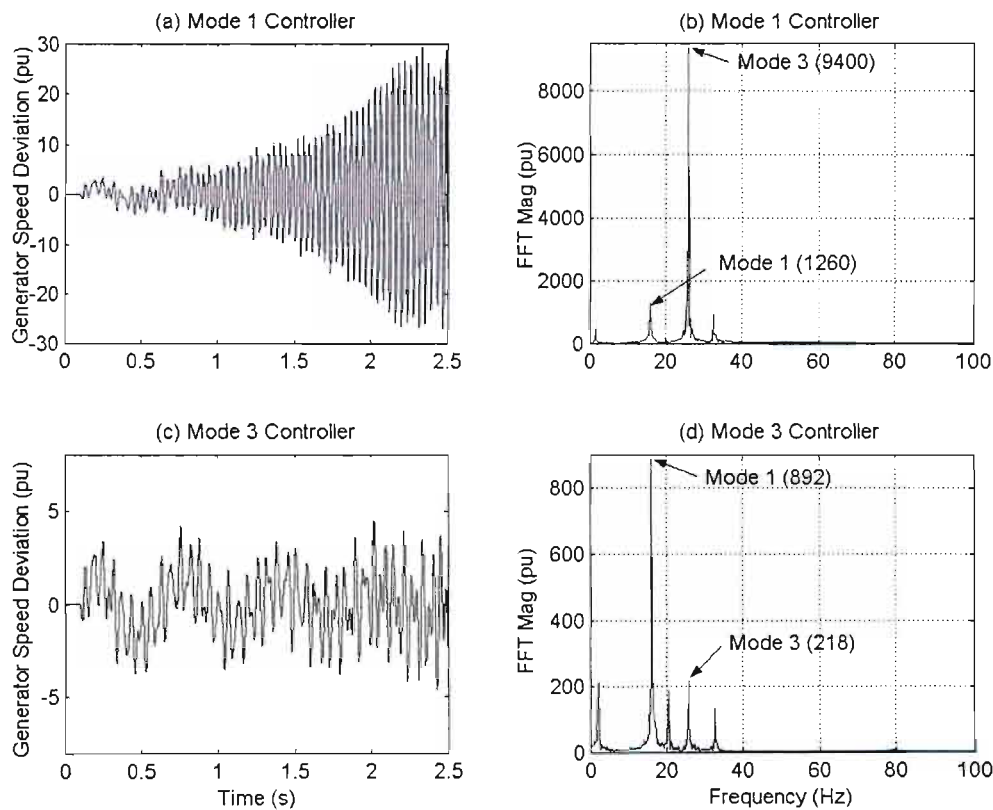


Fig.8.7: Time-domain responses, and FFTs, of the generator speed deviation for Case 1 after the addition of separate, single-mode damping controllers at each of the frequencies of Mode 1 and 3.

The results in Figs. 8.7 (a) and (b) show that the addition of the supplementary damping controller designed for Mode 1 does not provide damping to the very mode for which it was designed; instead, it destabilises this mode (the amplitude of the FFT at the frequency of Mode 1 (15.71 Hz) in Fig. 8.7(b) is three times larger than that shown in Fig. 8.2(a)). Ironically, this Mode 1 damping controller has reduced the presence of other modes in the response, with its effect most evident on Mode 3. However, the overall damping provided is not sufficient to restore the system to stability with Mode 3 remaining dominant. Note, the rate of growth of

the amplitude of the oscillations in generator speed deviation in Fig. 8.7(a) is clearly worse than that in the uncontrolled study of Fig. 8.1 (a); however, the FFT analysis indicates that this deterioration is as a result of the destabilization of Mode 1, despite the reduced content of, but still unstable, Mode 3 oscillations present in the response.

Figs. 8.7(c) and (d) show that the controller designed to add damping at the frequency of Mode 3 has in fact successfully done so (the amplitude of the FFT at the frequency of Mode 3 (25.55 Hz) in Fig. 8.7(d) is considerably reduced from that in Fig. 8.2(a)). However, comparison of the Mode 1 frequency peaks in the FFTs of Figs. 8.7(d) and 8.2(a) show that the Mode 3 damping controller has had a negative impact on the Mode 1 oscillations compared to the original response. (A close analysis of the magnitudes of the FFTs at the Mode 1 frequency of 15.71Hz in Fig. 8.7(d) and 8.2(a) shows that amplitude of Mode 1 has more than doubled after the Mode 3 controller has been applied). The time-domain behaviour of the generator speed deviation in Fig. 8.7(c), when compared with that in Fig. 8.1(a), has clearly improved, but still exhibits the negatively damped oscillatory components associated with the Mode 1 frequency that were present in Fig. 8.1(a), but which were swamped by the more negatively damped Mode 3 oscillations prior to the introduction of the Mode 3 damping controller to the SSSC.

Table 8.2: Comparative amplitudes of the FFTs of generator speed deviation at each mode frequency with, and without, single-mode damping controllers – Case 1.

Mode	No Damping Controller	Mode 1 Damping Controller	Mode 3 Damping Controller
1 (15.71 Hz)	420	1260	892
2 (20.005 Hz)	300	112	185
3 (25.55 Hz)	17600	9400	218
4 (32.285 Hz)	1000	934	133

The impact of the two single-mode damping controllers can be seen at a glance in Table 8.2 which shows the changes in the magnitudes of the FFTs of the generator speed deviation, at each mode frequency, following the addition of each of the single-mode controllers. In one case, the single-mode controller significantly destabilises the mode that it was meant to damp out (Mode 1); however, the amplitudes of all other torsional components decrease as a result of the application of the controller. In the other case of the single-mode controller (Mode3), the amplitude of the torsional component associated with the frequency at which the controller was designed is successfully reduced, but the amplitude of the torsional components at another frequency is increased by the introduction of the controller. Thus it appears, at least in this

case, that the addition of a single-mode supplementary damping controller does not provide the stability needed for all modes.

8.3.2 Case 2 – With Single-Mode Damping Controllers

The results in section 8.2.2 showed that the combination of X_c and X_q^* in Case 2, with no supplementary damping control, gives rise to sustained, but not negatively damped, oscillations in the generator speed deviation dominated by Mode 3, but with a strong component of Mode 1 also evident. This section therefore considers whether the damping of the torsional oscillations can be improved for this case, by adding either a single damping controller designed for Mode 1, or a single damping controller designed for Mode 3.

Figs. 8.8(a) and (b) show the response following the addition of a supplementary controller designed to add damping at the single frequency of Mode 1; Figs. 8.8(c) and (d) show the response following the addition of a supplementary controller designed to add damping at the single frequency of Mode 3. Each of these results should be compared to those shown in Figs. 8.3 and 8.4, which show the behaviour of the same Case 2 with no supplementary control. The

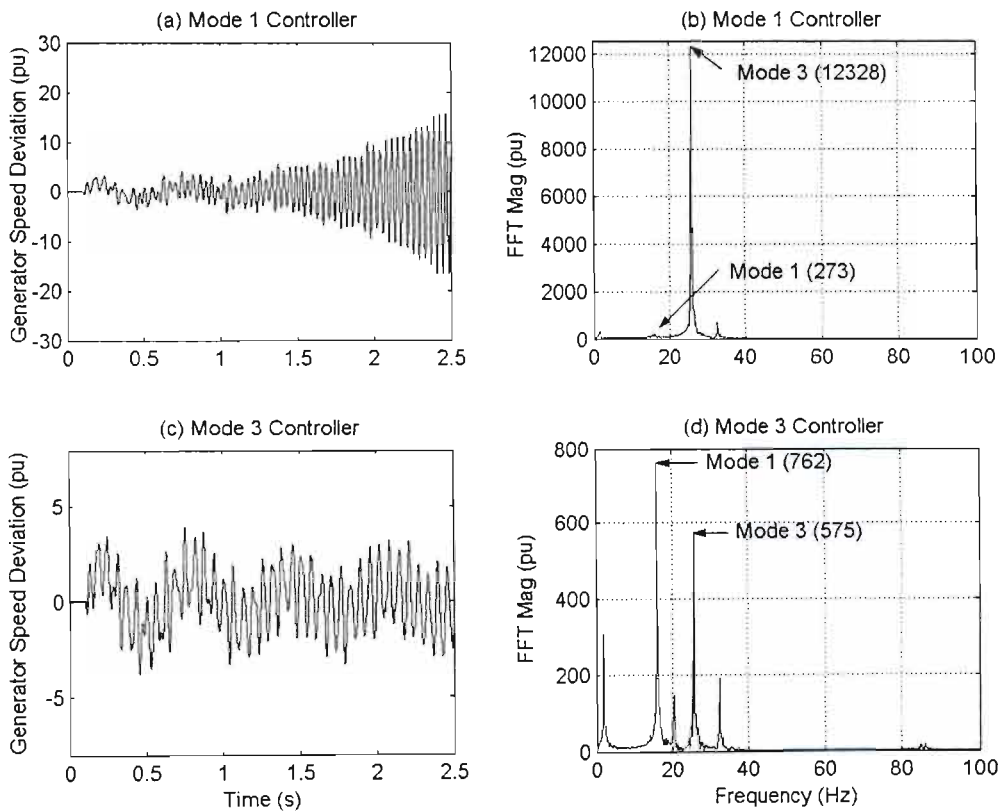


Fig.8.8: Time-domain responses, and FFTs, of the generator speed deviation for Case 2 after the addition of separate, single-mode damping controllers at each of the frequencies of Mode 1 and 3.

results in Figs. 8.8(a) and (b) clearly show that the addition of the supplementary damping controller designed for Mode 1 has in fact significantly destabilised Mode 3. (A close analysis of the magnitudes of the FFTs at the Mode 1 frequency of 15.71 Hz in Fig. 8.8(b) and 8.4(a) shows that, despite this destabilising of Mode 3, the controller has reduced the amplitude of the Mode 1 oscillations.) Conversely, Figs. 8.8(c) and (d) show that the controller designed to add damping at the frequency of Mode 3 has in fact successfully done so (the amplitude of the FFT peak at the frequency of Mode 3 (25.55 Hz) in Fig. 8.8(d) is reduced to almost half of that shown in Fig. 8.4(a)). However, a comparison of the Mode 1 frequency in the FFTs of Figs. 8.8(d) and 8.4(a) shows that the Mode 3 damping controller has had a relatively small, but negative impact on the Mode 1 oscillations compared with the original response. The time-domain behaviour of the generator speed deviation in Fig. 8.8(c) still exhibits sustained oscillations similar to those shown in Fig. 8.3(a).

Table 8.3 shows the changes in the magnitudes of the FFTs of the generator speed deviation, at each mode frequency, following the addition of each of the single-mode controllers. In the case of each single-mode controller, the amplitude of the torsional component associated with the frequency at which the controller was designed is successfully reduced, but the amplitude of the torsional components associated with at least one other frequency is increased by the introduction of the controller. Thus it appears, in this case, that the addition of a single-mode supplementary damping controller does not provide the stability needed for all modes.

Table 8.3: Comparative amplitudes of the FFTs of generator speed deviation at each mode frequency with, and without, single-mode damping controllers – Case 2.

Mode	No Damping Controller	Mode 1 Damping Controller	Mode 3 Damping Controller
1 (15.71 Hz)	523	273	762
2 (20.005 Hz)	200	130	145
3 (25.55 Hz)	1100	12328	575
4 (32.285 Hz)	484	720	192

8.3.3 Case 3 – With Single-Mode Damping Controllers

The results in section 8.2.3 showed that the combination of X_c and X_q^* in Case 3, with no supplementary damping control, gives rise to negatively damped SSR dominated by Mode 1, but with Mode 2 also present. This section therefore considers whether this case can be

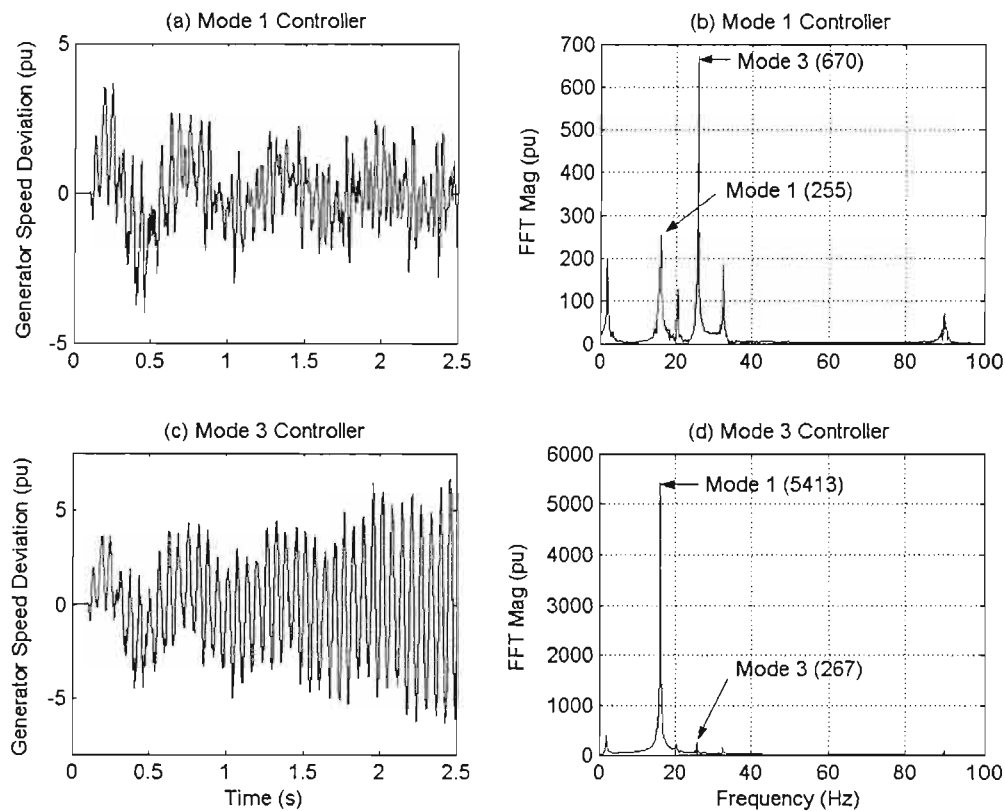


Fig.8.9: Time-domain responses, and FFTs, of the generator speed deviation for Case 3 after the addition of separate, single-mode damping controllers at each of the frequencies of Mode 1 and 3.

Table 8.4: Comparative amplitudes of the FFTs of generator speed deviation at each mode frequency with, and without, single-mode damping controllers – Case 3.

Mode	No Damping Controller	Mode 1 Damping Controller	Mode 3 Damping Controller
1 (15.71 Hz)	2219	255	5413
2 (20.005 Hz)	287	127	260
3 (25.55 Hz)	672	670	267
4 (32.285 Hz)	220	187	150

stabilised by adding a single-mode damping controller designed for first Mode 1, and then (for consistency with the two previous cases) for Mode 3.

Figs. 8.9(a) and (b) show the response following addition of the Mode 1 supplementary damping controller whilst Figs. 8.9(c) and (d) show the response following addition of the

Mode 3 supplementary damping controller. Table 8.4 summarises the impact on the mode frequency components as a result of introducing each single-mode controller.

The results show that for this case, the addition of the single, Mode 1 supplementary damping controller reduces the amplitudes of the FFT peaks at all mode frequencies and results in a stable response of the generator speed deviation that has a considerably reduced amplitude of torsional oscillation (Fig. 8.9(a)) compared with the case with no damping controller in Fig. 8.5(a). However, the results also show that adding a single Mode 3 controller in this case significantly destabilises Mode 1, resulting in a negatively damped response in the generator speed deviation.

The results of this case, as well as those of the previous two cases, have shown that in general it is not possible to design a single-mode supplementary damping controller for the SSSC that will either stabilise, or at least not *destabilise*, other torsional modes when the SSSC is in series with conventional capacitors. On the contrary, it has been shown that a single-mode damping controller added to the SSSC is actually likely to significantly destabilise other modes when conventional series capacitors are also present. Thus the addition of, and design of, a supplementary SSSC damping controller is clearly a more complex issue in the presence of conventional series compensation, than when the SSSC is the only compensator in the line (c.f. Chapter Seven).

8.4 Supplementary Control With A Multi-Modal Damping Controller

The previous section has shown that it is generally not possible to stabilise SSR in a system comprising conventional series capacitors and an SSSC, with a supplementary damping controller designed for a single mode frequency. Furthermore, the results showed that not all single-mode damping controllers considered were even able to add damping to the mode for which they were designed, and that even when they are able to do so, they typically destabilise other modes, often to a considerable extent.

This section therefore considers an extension of the idea originally proposed in [65] that is more suited to damping the more complex, multi-modal torsional responses found in the presence of dual-compensated systems. The idea for this extended approach arose from the findings of the previous section. Specifically, the findings of the previous section show that in the presence of conventional series capacitors, an SSSC supplementary damping controller must be able to achieve two goals:

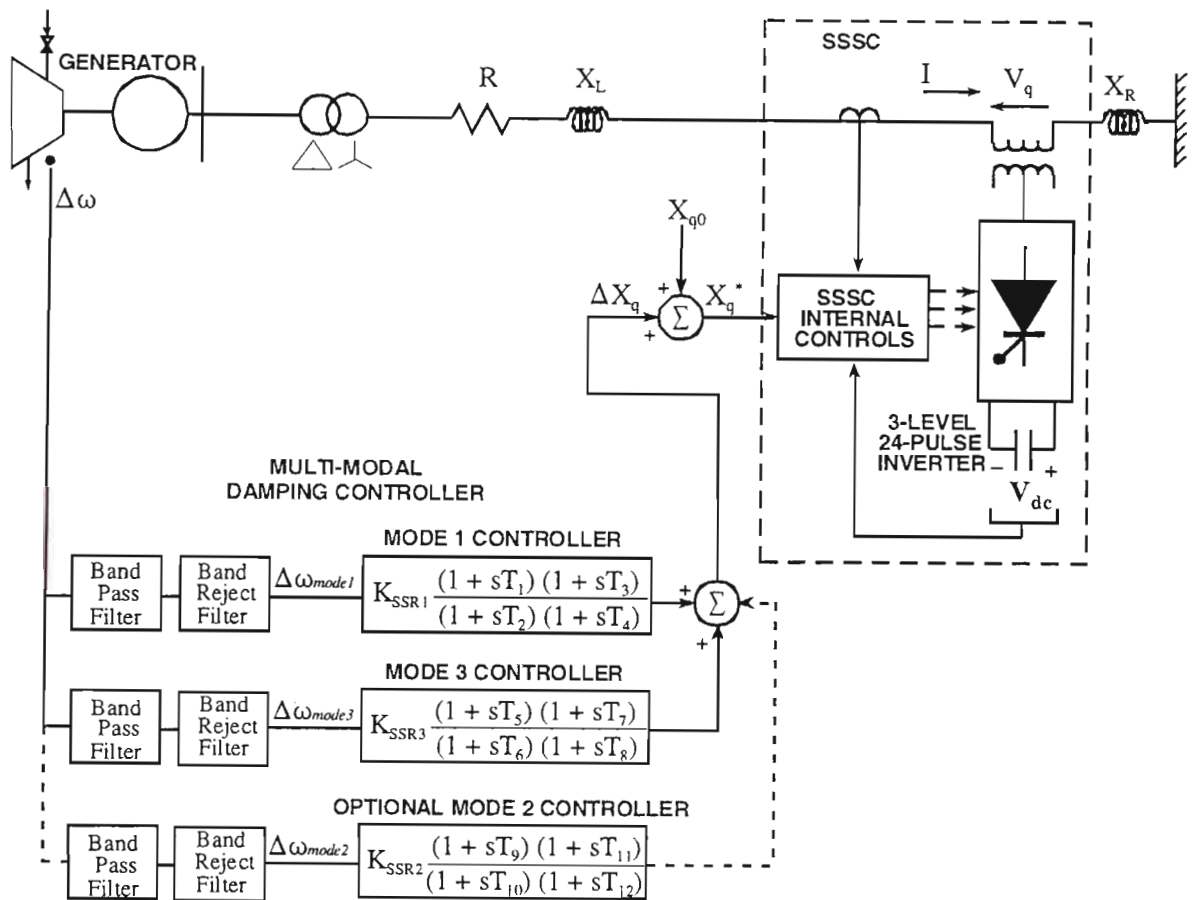


Fig.8.10: Three-level SSSC with multi-modal supplementary damping controls in the IEEE First Benchmark Model transmission system.

- (i) it needs to be designed to damp out more than one mode, i.e. the controller must be multi-modal; and
- (ii) each mode controller must be designed to add damping to its mode whilst minimising its adverse impact on other modes.

Fig. 8.10 shows a diagram of this extended supplementary damping controller. Essentially, the approach taken was to combine a number of individually-designed, single-mode damping controllers at distinct mode frequencies into one multi-mode damping controller. In order for each single-mode damping controller to damp out its specific torsional mode frequency, filters are used on the generator speed deviation at the input to each single-mode controller to allow (within the limits of the filters) only the mode frequency of interest to pass through to that single-mode controller. The output from the filters, $\Delta\omega_{mode\ i}$, is then fed into the single-mode supplementary SSSC controller, which consists of lead compensators and a gain block, to form its own output

modulation. Depending on the number of single-mode controllers required, the output modulations from all of these single-mode controllers will be added to form an output ΔX_q , which is then added onto the desired capacitive reactance of the SSSC around some set point, X_{q0} .

8.4.1 Design Procedure

From the resonant characteristics of the three dual-compensated cases without any supplementary damping controls considered in section 8.2, it was observed that Mode 1 and Mode 3 were generally the two dominant modes in the post-disturbance responses of the system for all the cases considered. The aim of the multi-modal controller design considered in this section was therefore to damp out these two specific modes and, by so doing, to ensure stability of the dual-compensated IEEE First Benchmark System for the three cases considered. This section now describes the particular design steps taken to arrive at such a multi-modal damping controller.

The six steps involved in the design of the multi-modal supplementary damping controller are outlined as follows.

1. The design of each single-mode controller within the multi-mode controller starts with design of its input filter parameters. Each mode controller has a band-pass filter (centred on the frequency of the mode to be damped) in series with a band reject filter (centred on the frequency of one other dominant mode whose frequency is to be filtered out from the input signal to that single-mode controller). The parameters of the two-filters were designed under open-loop conditions by adjusting their gains and damping ratios to get the best combination of attenuation of the mode-frequency to be filtered out, and amplification of the mode frequency to be passed through to that mode controller.
2. Using the same procedure described in Chapter Seven, the open-loop phase characteristics were measured at the frequency of interest for each single-mode controller in turn: i.e. a sinusoidal test signal was applied at the ΔX_q input of the SSSC and the phase lag measured from this input to the output $\Delta \omega_{mode\ i}$ of that single-mode controller's filter.
3. A suitable lead compensator was then designed (using parameters T_1 to T_4) for each single-mode controller to compensate for the phase lag measured in step 2 at the frequency of interest.

4. The first of the single-mode damping controller loops was then closed, and its gain K_{SSR_x} determined experimentally with the other single-mode controllers left open loop. The approach adopted was to consider a range of values for K_{SSR_i} and to select the value that resulted in the best compromise between improved damping of the mode to be controlled (based on inspection of time-domain and FFT results) and minimised destabilisation of the other dominant mode (again based on inspection of time-domain and FFT results).
5. Step 4 was repeated for the second single-mode damping controller (i.e. the second single-mode controller loop was closed and its gain K_{SSR_i} determined experimentally with the first single-mode controller left open-loop.)
6. The two single-mode damping controllers, with their gains K_{SSR_i} determined in Step 4 and 5, were connected in closed-loop together to form a multi-modal damping controller design whose performance could then be evaluated relative to that of the dual-compensated system with no supplementary controls.

The approach just described is that used to design a two-mode damping controller, but an additional mode damping controller loop can be added, and a similar design procedure followed, to arrive at a three-mode damping controller; this latter approach is considered later in the chapter.

8.4.2 Performance Of Multi-Modal Damping Control

This section now examines the performance of multi-modal damping controllers designed for each of the three cases of dual-compensation described earlier in the chapter. When considering Case 1, the results obtained during the intermediate design steps (i.e. the performance of the individual mode controllers) are shown for completeness. When considering Cases 2 and 3, only the performance of the full multi-modal controller is considered.

Once again, in the simulation results to be shown, the electrical system is initially operating at steady state; a three-phase fault of duration 0.075 seconds is then applied at the receiving-end of the transmission line at $t = 0.1$ seconds. Time and frequency domain results are presented for three system variables from the simulation, namely, generator speed deviation, the LPA-LPB turbine shaft torque, and GEN-EXC shaft torque.

Case 1 – Multi-Modal Damping Controller Applied To Case 1

The results in section 8.2 showed that the dual-compensated system in Case 1 ($X_c = 0.178$ pu and $X_q^* = 0.1927$ pu) is unstable with no supplementary damping control on the SSSC, and that Mode 3 is dominant in the unstable system response, but with Mode 1 and 4 also present. The results in section 8.3 then showed that attempts to damp either Mode 1 or Mode 3 in Case 1 with a single-mode controller resulted in destabilization, either in the mode of interest or in the other dominant mode. This section therefore considers the performance of a two-mode supplementary controller for Case 1, with the individual mode controllers designed to damp Mode 1 and 3 respectively.

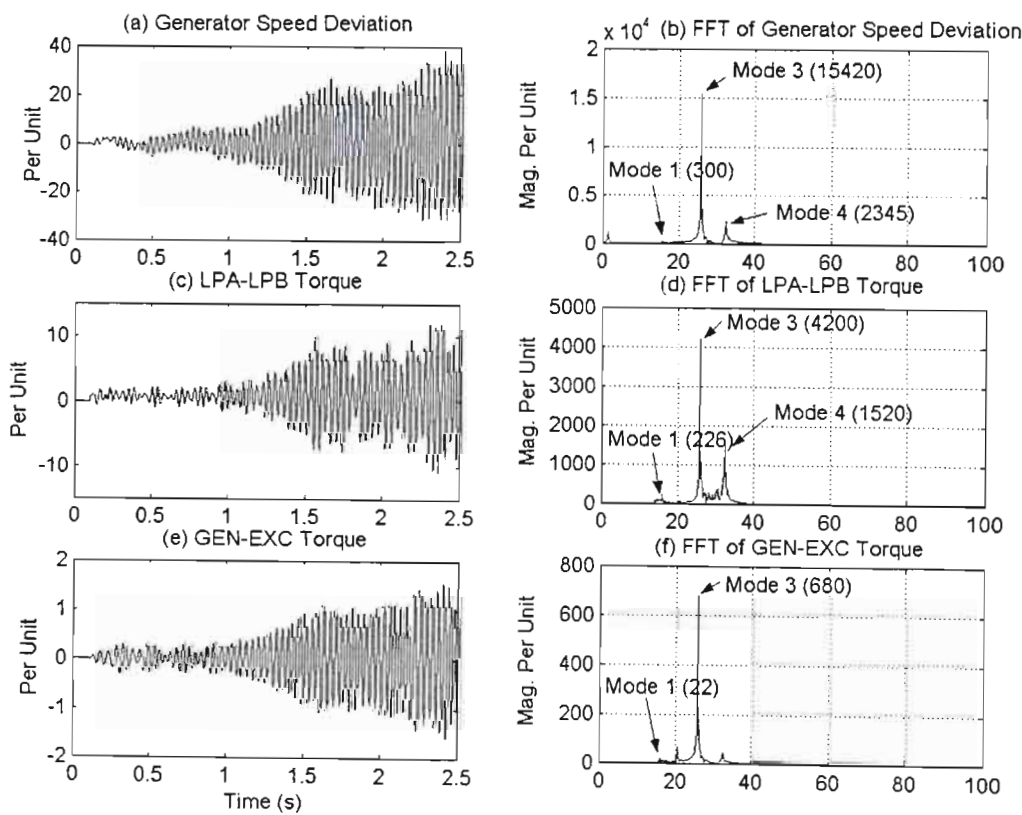


Fig.8.11: Time-domain response and frequency-domain characteristics for Case 1: Mode 1 controller active ($K_{SSR1} = 0.67$) with Mode 3 controller open loop.

Fig. 8.11 shows the time domain response and frequency domain characteristics when only the Mode 1 damping loop of this multi-modal controller is closed, with gain $K_{SSR1} = 0.67$. A comparison of the amplitudes of the FFT peaks in Fig. 8.2(a), (c) and (d) with those in Fig. 8.11(b), (d) and (f) show that with this particular gain and with pre-filtering on its input signal,

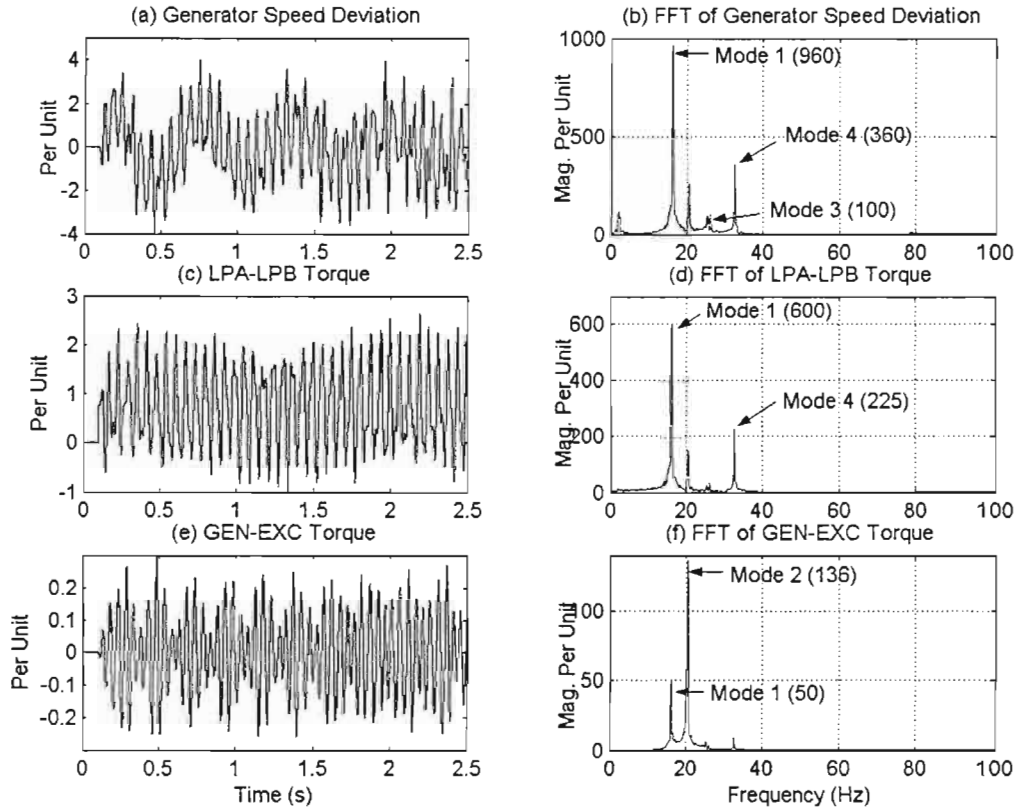


Fig.8.12: Time-domain response and frequency-domain characteristics for Case 1: Mode 3 controller active ($K_{SSR3} = 0.06$) with Mode 1 controller open loop.

the single-mode damping controller is now able to provide damping to all the modes, including the mode for which it was designed. However, the system remains unstable, with the Mode 3 frequency being the dominant frequency in the response (i.e. the stabilisation is incomplete).

Fig. 8.12 shows the time domain response and frequency domain characteristics when only the Mode 3 damping loop of this multi-modal controller is closed, with gain $K_{SSR3} = 0.06$. Once again, comparison of the FFT peaks in Fig. 8.2 with those in Fig. 8.12 shows that this single-mode damping control loop is able to reduce the amplitude of its own mode frequency but in this case it still increases the amplitude of the frequency component of the other dominant mode.

Fig. 8.13 shows the time domain response and frequency domain characteristics obtained when both the Mode 1 and Mode 3 loops of the multi-modal controller are closed together with gains $K_{SSR1} = 0.67$ and $K_{SSR3} = 0.06$. The results in Fig. 8.13 confirm that the two loops of the

multi-mode damping controller, when working together, are able to stabilise both Mode 1 and Mode 3: the time domain results show that all the variables are now positively damped, whilst the FFTs confirm that the presence of both the Mode 1 and Mode 3 frequency components in the system variables has been significantly reduced in comparison with the FFT peaks in the uncontrolled Case 1 response shown in Fig. 8.2

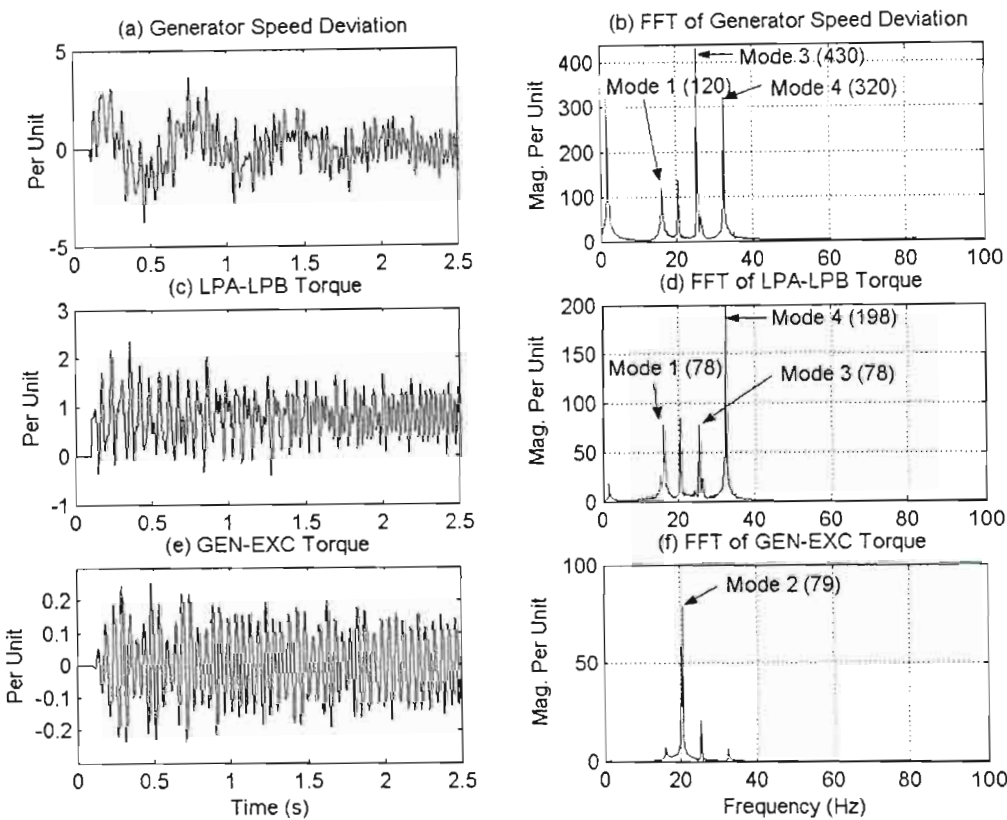


Fig.8.13: Time-domain response and frequency-domain characteristics for Case 1: Mode 1 and Mode 3 loops of the multi-modal damping controller activated; $K_{SSR1} = 0.67$, $K_{SSR3} = 0.06$.

In order to gauge the degree of improvement in the SSR characteristics as a result of the addition of the multi-modal damping controller to the SSSC in Case 1, Fig. 8.14 compares the response with this supplementary controller active to that obtained with no supplementary damping control on the SSSC at all.

The results indicate clearly that a significant amount of damping has been added to the torsional oscillations in the generator speed deviation and LPA-LPB torque; the GEN-EXC torque also exhibits a noticeable, although less significant, improvement in damping. The results confirm that, for Case 1, it is possible to stabilise the torsional oscillations by means of a carefully-designed multi-modal supplementary damping controller acting on Modes 1 and 3 of the First Benchmark Model.

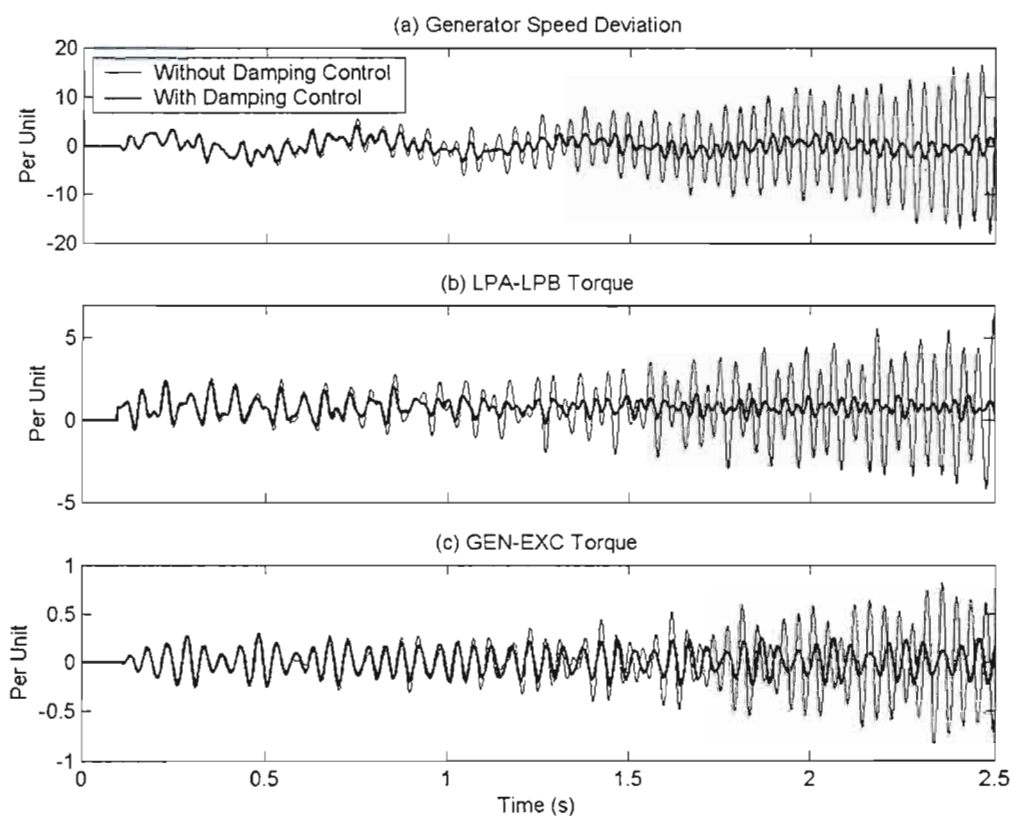


Fig.8.14: Comparison of time-domain responses of Case 1 with and without the multi-modal supplementary damping controller ($K_{SSR1} = 0.67$, $K_{SSR3} = 0.06$) active.

Case 2 – Multi-Modal Damping Controller Applied To Case 2

The results in section 8.2 showed that the dual-compensated system in Case 2 ($X_c = 0.224$ pu and $X_q = 0.1467$ pu) is fairly stable with no supplementary damping control on the SSSC, with Modes 1 and 3 dominating the system response. The results in section 8.3 then showed that attempts to damp either of these dominant modes in Case 2 with a single-mode controller results in destabilization of the other dominant mode. This section therefore considers the performance of a two-mode supplementary controller for Case 2, with the individual mode controllers designed to damp Mode 1 and 3 respectively.

Fig. 8.15 shows the time domain response and frequency domain characteristics obtained when both the Mode 1 and Mode 3 loops of the multi-modal controller are closed together with gains $K_{SSR1} = 0.6$ and $K_{SSR3} = 0.07$ for Case 2. The results in Fig. 8.15 confirm that the two loops of the multi-mode damping controller, when working together, are able to provide positive

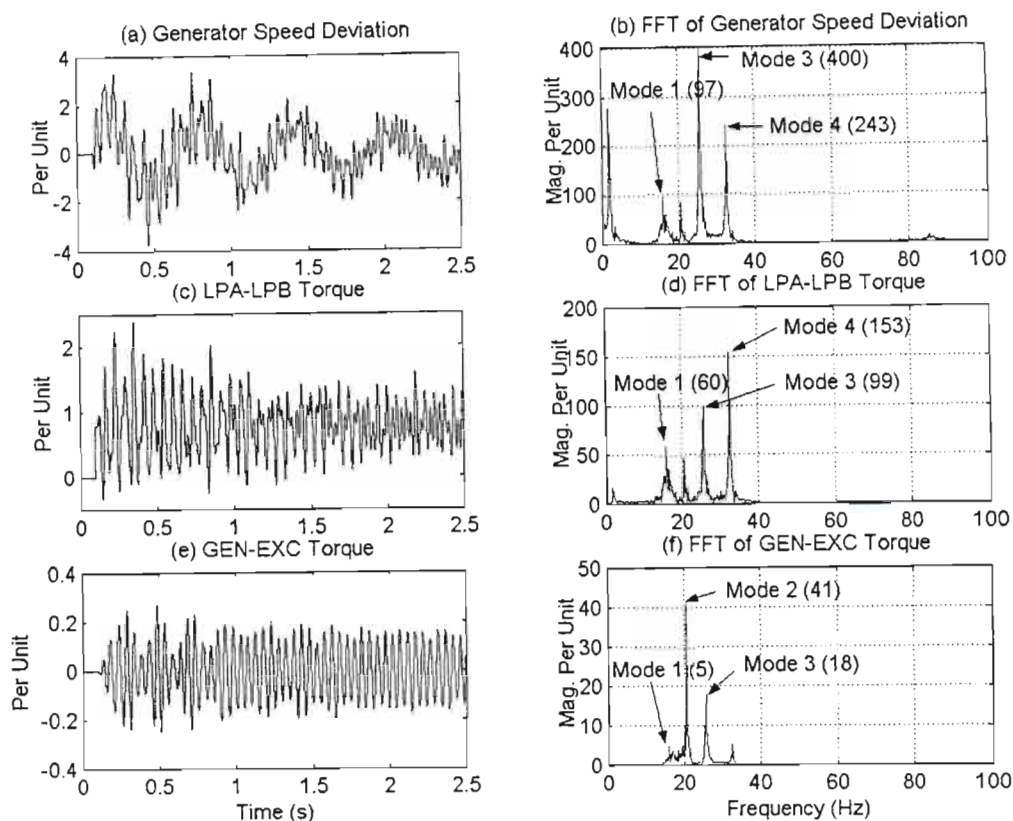


Fig.8.15: Time-domain response and frequency-domain characteristics for Case 2: Mode 1 and Mode 3 loops of the multi-modal damping controller activated; $K_{SSR1} = 0.6$, $K_{SSR3} = 0.07$.

damping to both Mode 1 and Mode 3: the time domain results show that all the variables are now positively damped, whilst the FFTs confirm that the presence of both the Mode 1 and Mode 3 frequency components in the system variables has been significantly reduced from those evident in the response of the uncontrolled Case 2 results shown in Fig. 8.4.

In order to show the improvement in the SSR characteristics as a result of the addition of the multi-modal damping controller in Case 2, Fig. 8.16 compares the response with this supplementary controller active to that obtained with no supplementary damping control on the SSSC at all. The results clearly indicate that a significant amount of damping has been added to the torsional oscillations in the generator speed deviation and LPA-LPB torque; the GEN-EXC torque also exhibits a noticeable, although less significant, improvement in damping. The results confirm that, for Case 2, it is possible to provide positive damping to the torsional oscillations by means of a carefully-designed multi-modal supplementary damping controller acting on Modes 1 and 3 of the First Benchmark Model.

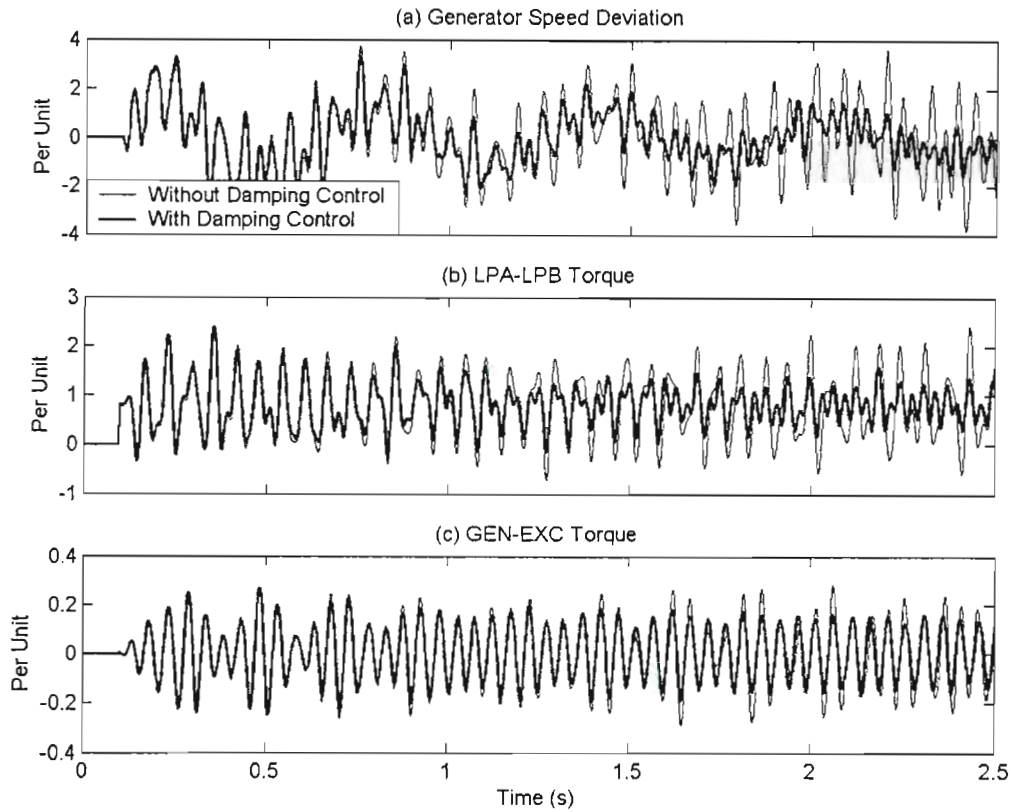


Fig.8.16: Comparison of time-domain responses of Case 2 with and without the multi-modal supplementary damping controller ($K_{SSR1} = 0.6$, $K_{SSR3} = 0.07$) active.

Case 3 – Multi-Modal Damping Controller Applied To Case 3

The results in section 8.2 showed that the dual-compensated system in Case 3 ($X_c = 0.275$ pu and $X_q = 0.0957$ pu) is unstable with no supplementary damping control on the SSSC, and that Modes 1 and 3 are dominant in the unstable system response (particularly Mode 1). The results in section 8.3 then showed that by damping Mode 1 with a single-mode controller, the system response was no longer unstable, but still exhibited sustained oscillations. However, the attempts to damp Mode 3 with a single-mode controller resulted in destabilization of Mode 1.

As in the previous two cases, a two-mode supplementary controller was considered for Case 3, with the individual mode controllers designed to damp Modes 1 and 3 respectively. It was hoped that by employing this two-mode supplementary controller, positive damping would be provided to all modes and thus restore the system stability. However, it was found that although Modes 1 and 3 were duly suppressed as expected by this two-mode controller, Mode 2

remained predominant in the GEN-EXC torque (the variable that has been shown to be most affected by this particular mode), and in fact the GEN-EXC torque remained unstable with growing oscillations.

Since Mode 2 was instrumental in the unstable response of the GEN-EXC torque, a two-mode supplementary controller was then designed instead to damp out the Mode 1 and Mode 2 frequencies. This resulted in a slightly better performance than the first attempt to damp the Mode 1 and 3 frequencies with a two-mode controller. However, only partial stabilization was achieved by this controller design.

Consequently, this study considered a three-mode supplementary damping controller design to simultaneously stabilize Modes 1, 2 and 3 for Case 3 in particular. This section now investigates the performance of this three-mode supplementary controller for Case 3, with the individual mode controllers designed to damp Modes 1, 2 and 3.

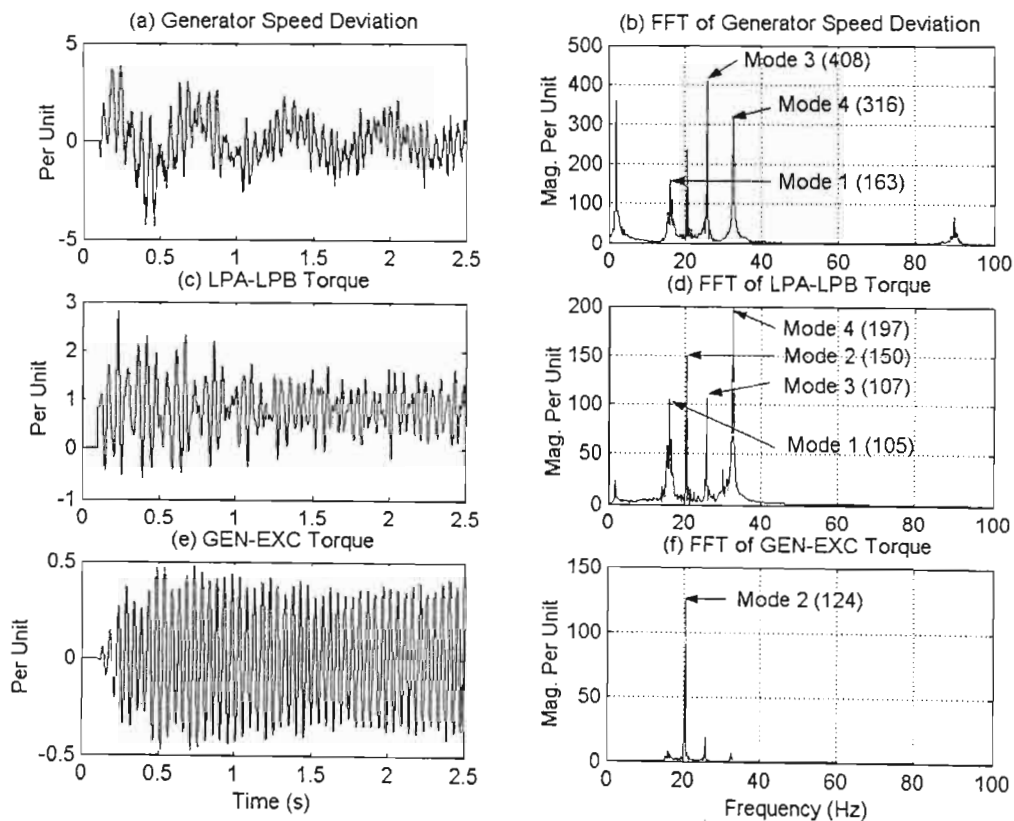


Fig.8.17: Time-domain response and frequency-domain characteristics for Case 3: Mode 1, Mode 2 and Mode 3 loops of the multi-modal damping controller activated;

$$K_{SSR1} = 0.7, K_{SSR2} = 0.3 \text{ and } K_{SSR3} = 0.05.$$

Fig. 8.17 shows the time domain response and frequency domain characteristics obtained when both the Mode 1, Mode 2 and Mode 3 loops of the multi-modal controller designed for Case 3 are closed together with gains $K_{SSR1} = 0.7$, $K_{SSR2} = 0.3$ and $K_{SSR3} = 0.05$. The results in Fig. 8.17 show that the three loops of the multi-mode damping controller, when working together, are able to provide positive damping to all modes of interest, particularly Mode 1 and Mode 3: the time domain results show that the generator speed deviation and LPA-LPB torque are both positively damped; however, although no longer unstable, the GEN-EXC torque oscillations are still sustained. The FFTs in Fig. 8.7 confirm that the presence of both the Mode 1 and Mode 3 frequency components in the system variables has been significantly reduced from those in Fig. 8.16, and although the Mode 2 frequency component has also been reduced, the extent of this reduction is, however, not dramatic.

In order to show the improvement in the SSR characteristics as a result of the addition of the multi-modal damping controller in Case 3, Fig. 8.18 compares the response with this supplementary controller active, to that obtained with no supplementary damping control on the SSSC at all. As in both previous cases, the results indicate that a significant amount of

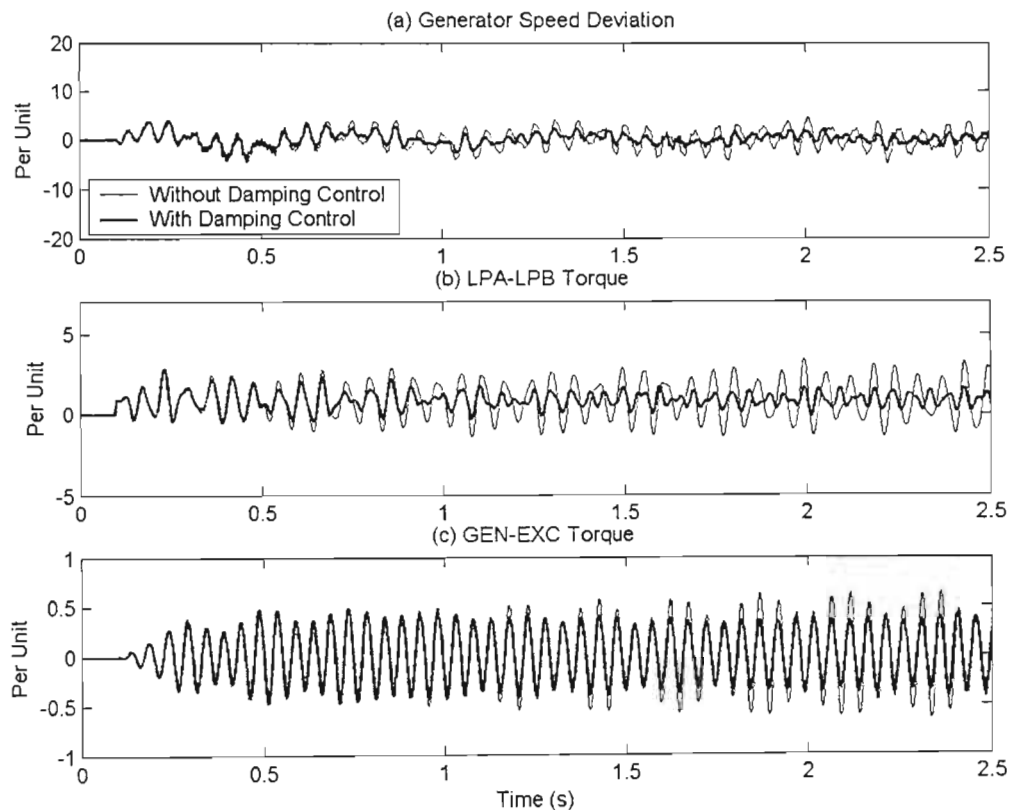


Fig.8.18: Comparison of time-domain responses of Case 3 with and without the multi-modal supplementary damping controller ($K_{SSR1} = 0.7$, $K_{SSR2} = 0.3$ and $K_{SSR3} = 0.05$) active.

damping has been added to the torsional oscillations in the generator speed deviation and LPA-LPB torque; the GEN-EXC torque again exhibits a noticeable, although less significant, improvement in damping. The results confirm that, for Case 3, it is possible to provide positive damping to the torsional oscillations by means of a carefully-designed multi-modal supplementary damping controller acting on Modes 1, 2 and 3 of the First Benchmark Model.

Although the performance of the three-mode supplementary controller applied to Case 3 offers marginally better performance than that of the two-mode controller, the dominant characteristics of Mode 2 in the GEN-EXC torque remains a concern in this case study as this particular mode could not be damped to the same extent as Modes 1 and 3. However, the issue is not a problem of getting the multi-modal damping controllers to work together, but rather, Mode 2 appears not to be very susceptible to this method of SSSC supplementary damping, since it is possible to add damping to this mode, but not to stabilize it to the extent of other modes.

This section has considered the design and application of multi-modal supplementary damping controllers to the three dual-compensated case studies considered in the IEEE First Benchmark Model. The design philosophy and design approach used in the multi-modal controller was outlined in detail and, in Case 1, the results of intermediate design steps shown for completeness. The results have shown that it is possible to successfully damp out the strong multi-modal response evident in dual-compensated systems, at least for the three cases considered for detailed study here. However, in the results presented in this section, each of the three dual-compensated cases has required its own unique, custom-designed, multi-modal damping controller to completely stabilise the system; in Case 3 in particular, an additional mode controller had to be added to the multi-modal controller structure that was not required in Cases 1 and 2.

The next section of the chapter therefore investigates whether it is possible to stabilise SSR in one dual-compensated case example with a multi-modal supplementary damping controller designed for a different dual-compensation case example.

8.5 Performance Of Multi-Modal Damping Controller At Other Values Of Compensation

The previous section showed the promising performance of multi-modal supplementary damping controllers in stabilising SSR in a system comprising conventional series capacitors and an SSSC. The next part of this dual-compensated system study is to consider whether it is possible, instead

of designing a separate multi-modal controller for each combination of conventional series capacitor and SSSC values ($X_c + X_q$), for a more generally applicable supplementary controller to rather be found and used for every combination of series compensating reactance values. This section therefore investigates whether or not it is possible to obtain such an ideal supplementary controller, that would provide the necessary system damping for all dual-compensated cases, or, at worst, does not further destabilise the overall system for dual-compensation values other than that for which it was designed.

The approach adopted for this study is to consider the performance of a multi-modal supplementary damping controller designed for one dual-compensated case example (i.e. one combination of X_c and X_q) when applied to a different dual-compensated case example in the same study system. Each step in this approach is therefore referred to as a “cross-case” damping study. Each such study to be presented in this section will again consider one of the three dual-compensation cases used throughout the chapter.

Once again, in all simulation studies the electrical system is initially operating at steady state; a three-phase fault of duration 0.075 seconds is then applied at the receiving-end of the transmission line at $t = 0.1$ seconds. Time and frequency domain results are presented for three system variables from the simulation, namely, generator speed deviation, LPA–LPB turbine shaft torque, and GEN–EXC shaft torque.

8.5.1 Cross-Case Damping Study Using The Multi-Modal Supplementary Controller Designed For Case 1 Dual-Compensated System

In this section, the multi-modal supplementary controller designed for the Case 1 dual-compensated system ($X_c = 0.178$ pu and $X_q^* = 0.1927$ pu) is applied to the Case 2 and Case 3 dual-compensated systems.

Multi-Modal Damping Controller Applied To The Case 2 Dual-Compensated System

The results in section 8.2 showed that the dual-compensated system in Case 2 ($X_c = 0.224$ pu and $X_q^* = 0.1467$ pu) is fairly stable with no supplementary damping control on the SSSC, with Modes 1 and 3 dominating the system response.

Fig. 8.19 shows the time domain response and frequency domain characteristics obtained when

the multi-modal controller that was specifically designed for the Case 1 dual-compensated system to damp out Mode 1 and Mode 3 with gains $K_{SSR1} = 0.67$ and $K_{SSR3} = 0.06$, is now applied to Case 2. The results in Fig. 8.19 show that this particular multi-mode supplementary controller, when applied to the Case 2 dual-compensated system, is able to provide positive damping to all modes, with the improvement in Mode 1 and Mode 3 particularly noticeable: the time domain results show that the generator speed deviation and LPA-LPB torque are now positively damped; the GEN-EXC torque is not as well damped as the other two variables with its oscillations remaining sustained. The FFTs in Fig. 8.19 confirm that the presence of both the Mode 1 and Mode 3 frequency components in the system variables has been significantly reduced from those in the uncontrolled Case 2 example shown in Fig. 8.4. The slight reduction in the amplitude of the Mode 2 peak from that shown in Fig. 8.4 is not sufficient to significantly positively damp the GEN-EXC torque oscillations.

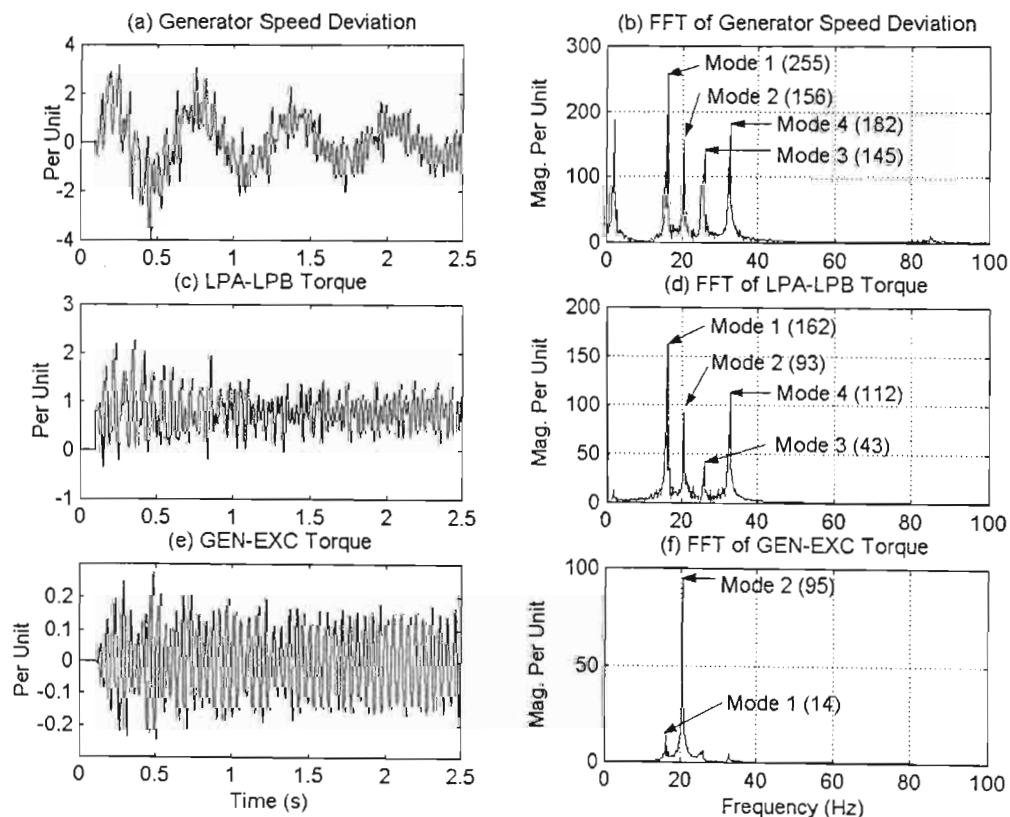


Fig.8.19: Time-domain response and frequency-domain characteristics for Case 2 dual-compensated system: Mode 1 and Mode 3 loops of the multi-modal damping controller designed for Case 1 dual-compensated system activated; $K_{SSR1} = 0.67$, $K_{SSR3} = 0.06$.

Multi-Modal Damping Controller Applied To The Case 3 Dual-Compensated System

The results in section 8.2 showed that the dual-compensated system in Case 3 ($X_c = 0.275$ pu and $X_q = 0.0957$ pu) is unstable with no supplementary damping control on the SSSC, and that Modes 1 and 3 are dominant in the unstable system response (particularly Mode 1).

Fig. 8.20 shows the time domain response and frequency domain characteristics obtained when the multi-modal controller that was specifically designed for the Case 1 dual-compensated system to damp out Mode 1 and Mode 3, with gains $K_{SSR1} = 0.67$ and $K_{SSR3} = 0.06$, is now applied to Case 3. The results in Fig. 8.20 show that this particular multi-mode supplementary controller, when applied to the Case 3 dual-compensated system, is unable to fully restore the system stability: the time domain results show that the generator speed deviation, the LPA-LPB torque and GEN-EXC torque all exhibit slightly negatively damped oscillations. However, the amplitudes of all of these variables' oscillations have decreased compared to those exhibited in Case 3 with no supplementary controller (c.f. Fig. 8.5). The FFTs in Fig. 8.20 confirm that

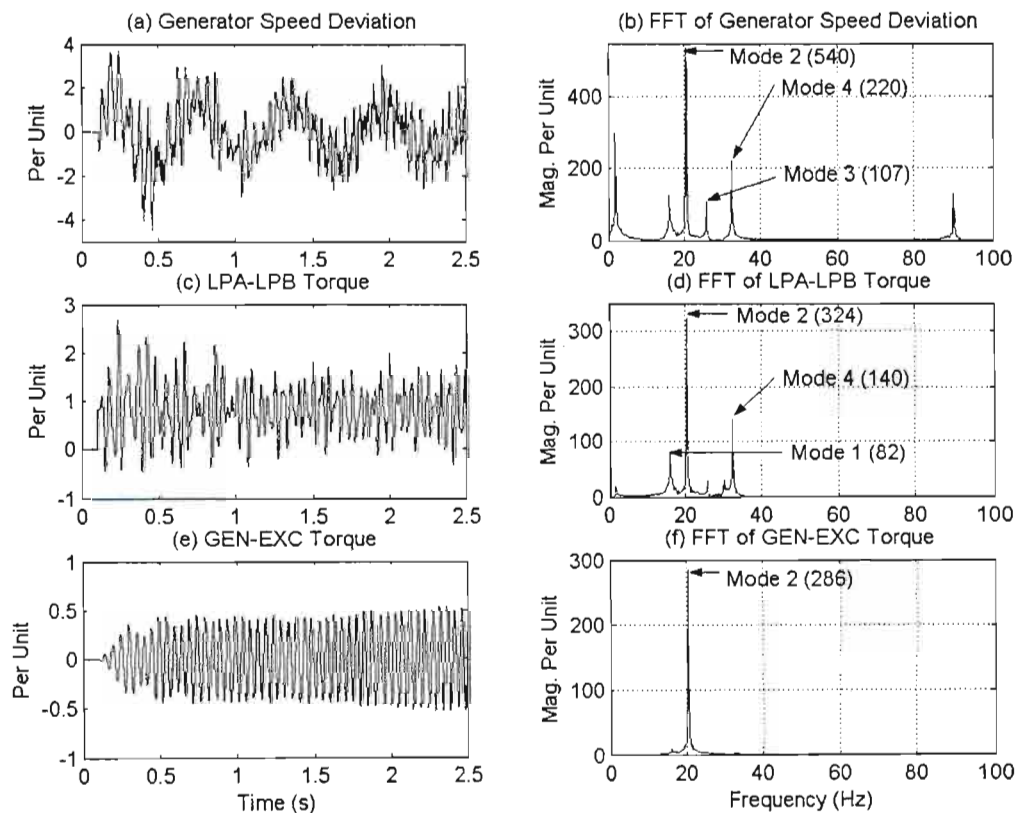


Fig.8.20: Time-domain response and frequency-domain characteristics for Case 3 dual-compensated system: Mode 1 and Mode 3 loops of the multi-modal damping controller designed for Case 1 dual-compensated system activated; $K_{SSR1} = 0.67$, $K_{SSR3} = 0.06$.

the presence of both the Mode 1 and Mode 3 frequency components in the system variables has been significantly reduced from those seen in the uncontrolled case shown in Fig. 8.6; however, this comes at the expense of significant amplitude increase in the Mode 2 FFT peaks from those in Fig. 8.6.

This set of studies has considered the use of a multi-modal supplementary damping controller designed for the Case 1 dual-compensated system, applied to the Case 2 and Case 3 dual-compensated systems. The results have shown that this supplementary controller performs fairly well in the Case 2 dual-compensated system as it offers damping to all modes in the system variables. For the Case 3 dual-compensated system, the supplementary controller was able to provide damping to those modes that the controller was designed to damp out in the other case example; however, this controller has further destabilised Mode 2 in the Case 3 example, and the overall system remains unstable.

8.5.2 Cross-Case Damping Study Using The Multi-Modal Supplementary Controller Designed For Case 2 Dual-Compensated System

In this section, the multi-modal supplementary controller designed for the Case 2 dual-compensated system ($X_c = 0.224$ pu and $X_q^* = 0.1467$ pu) is applied to the Case 1 and Case 3 dual-compensated systems.

Multi-Modal Damping Controller Applied To The Case 1 Dual-Compensated System

The results in section 8.2 showed that the dual-compensated system in Case 1 ($X_c = 0.178$ pu and $X_q^* = 0.1927$ pu) is unstable with no supplementary damping control on the SSSC, and that Mode 3 is dominant in the unstable system response, but with Mode 1 and 4 also present.

Fig. 8.21 shows the time domain response and frequency domain characteristics obtained when the multi-modal controller that was specifically designed for the Case 2 dual-compensated system to damp out Mode 1 and Mode 3, with gains $K_{SSR1} = 0.6$ and $K_{SSR3} = 0.07$ is now applied to Case 1. The results in Fig. 8.21 show that this particular multi-mode supplementary controller, when applied to the Case 1 dual-compensated system, fails to restore the overall system stability: the time domain results show that the generator speed deviation and GEN-EXC torque are still negatively damped, although the amplitudes of these oscillations have been reduced considerably from those in the uncontrolled Case 1 study of Fig. 8.1. The FFTs in Fig. 8.21 confirm that the presence of both the Mode 1 and Mode 3 frequency

components in the system variables has been significantly reduced (particularly Mode 3) from those seen in Fig. 8.2, even though it is not sufficient to bring the system back to stability.

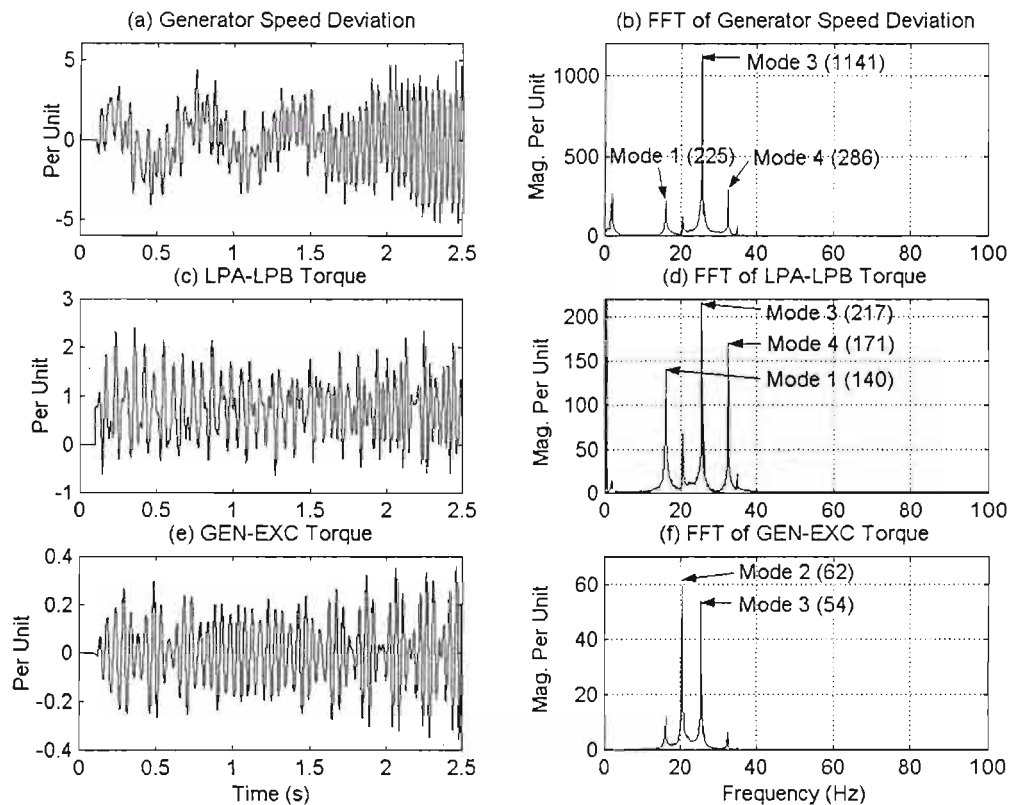


Fig.8.21: Time-domain response and frequency-domain characteristics for Case 1 dual-compensated system: Mode 1 and Mode 3 loops of the multi-modal damping controller designed for Case 2 dual-compensated system activated; $K_{SSR1} = 0.6$, $K_{SSR3} = 0.07$.

Multi-Modal Damping Controller Applied To The Case 3 Dual-Compensated System

The results in section 8.2 showed that the dual-compensated system in Case 3 ($X_c = 0.275$ pu and $X_q = 0.0957$ pu) is unstable with no supplementary damping control on the SSSC, and that Modes 1 and 3 are dominant in the unstable system response (particularly Mode 1).

Fig. 8.22 shows the time domain response and frequency domain characteristics obtained when the multi-modal controller that was specifically designed for the Case 2 dual-compensated system to damp out Mode 1 and Mode 3, with gains $K_{SSR1} = 0.6$ and $K_{SSR3} = 0.07$, is now applied to Case 3. The results in Fig. 8.22 show that this particular multi-mode supplementary controller, when applied to the Case 3 dual-compensated system, is unable to fully restore the system stability: the time domain results show that the generator speed deviation, LPA-LPB

torque, and GEN-EXC torque all exhibit slightly negatively damped oscillations, however, the FFTs in Fig. 8.22 confirm that the presence of both the Mode 1 and Mode 3 frequency components in the system variables has been significantly reduced from the uncontrolled Case 3 example (c.f. Fig. 8.6); however, this comes at the expense of amplitude increase in the Mode 2 and Mode 4 peaks. Clearly, the behaviour of the system shown in Fig. 8.22 indicates that the system could not be operated at this level of dual compensation, even with the improved damping obtained with the controller: the response of the system is clearly unstable and would therefore result in shaft damage.

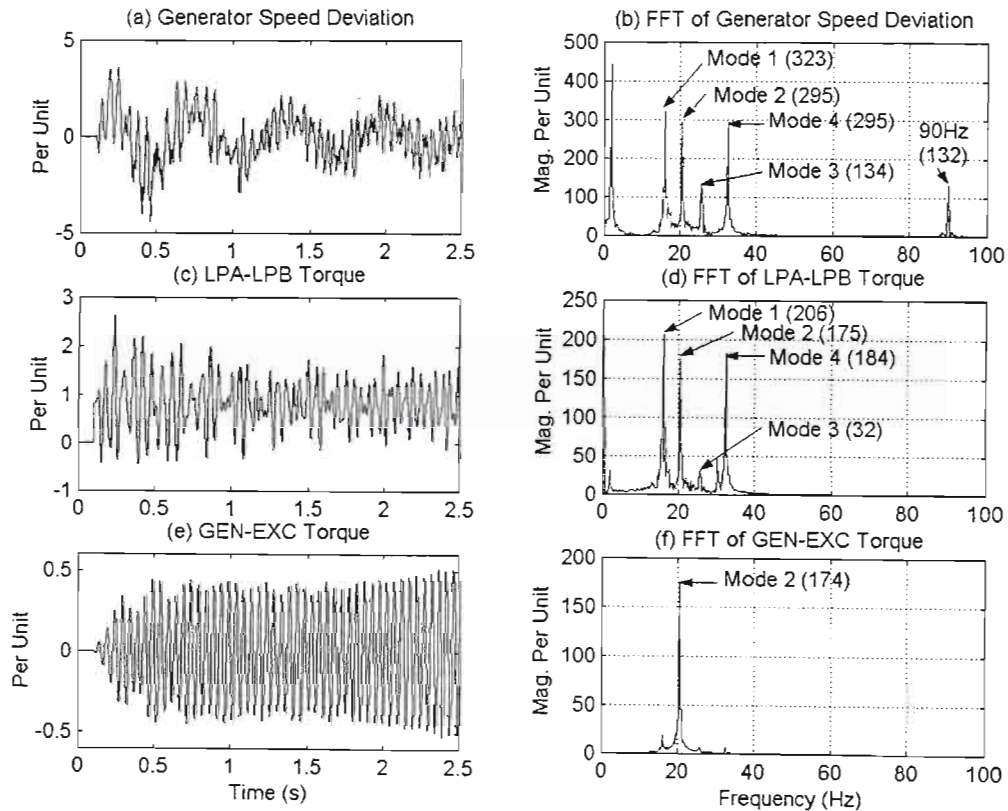


Fig.8.22: Time-domain response and frequency-domain characteristics for Case 3 dual-compensated system: Mode 1 and Mode 3 loops of the multi-modal damping controller designed for Case 2 dual-compensated system activated; $K_{SSR1} = 0.6$, $K_{SSR3} = 0.07$.

This set of studies has considered the use of a multi-modal supplementary damping controller designed for the Case 2 dual-compensated system, applied to the Case 1 and Case 3 dual-compensated systems. It was found that in both cases, such a supplementary controller was able to provide positive damping to Modes 1 and 3 to quite a large extent, but not to a sufficient degree to restore the system stability. Also, for the Case 3 dual-compensated system, the supplementary controller designed for Case 2 has negatively influenced the system by further destabilising Mode 2 and Mode 4.

8.5.3 Cross-Case Damping Study Using The Multi-Modal Supplementary Controller Designed For Case 3 Dual-Compensated System

In this section, the multi-modal supplementary controller designed for the Case 3 dual-compensated system ($X_c = 0.275$ pu and $X_g = 0.0957$ pu) is applied to the Case 1 and Case 2 dual-compensated systems.

Multi-Modal Damping Controller Applied To The Case 1 Dual-Compensated System

The results in section 8.2 showed that the dual-compensated system in Case 1 ($X_c = 0.178$ pu and $X_g^* = 0.1927$ pu) is unstable with no supplementary damping control on the SSSC, and that Mode 3 is dominant in the unstable system response, but with Modes 1 and 4 also present.

Fig. 8.23 shows the time domain response and frequency domain characteristics obtained when the multi-modal controller that was specifically designed for the Case 3 dual-compensated system to damp out Mode 1, Mode 2 and Mode 3, with gains $K_{SSR1} = 0.7$, $K_{SSR2} = 0.3$ and $K_{SSR3} =$

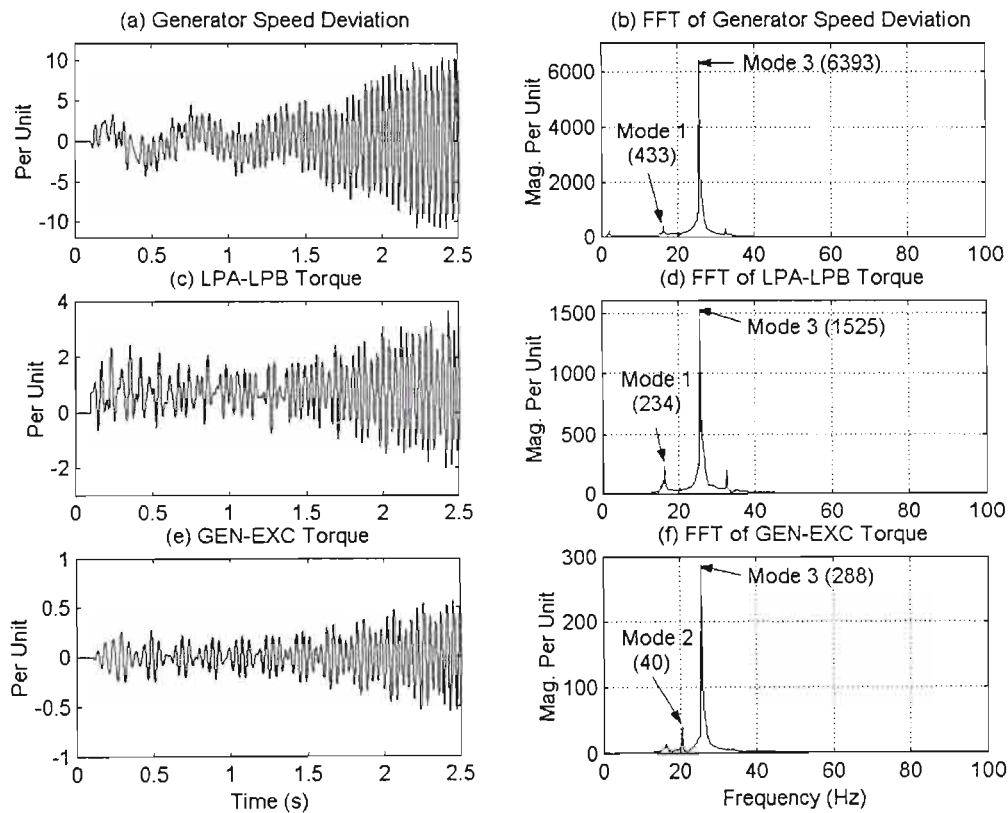


Fig.8.23: Time-domain response and frequency-domain characteristics for Case 1 dual-compensated system: Mode 1 and Mode 3 loops of the multi-modal damping controller designed for Case 3 dual-compensated system activated; $K_{SSR1} = 0.7$, $K_{SSR2} = 0.3$ and $K_{SSR3} = 0.05$.

0.05, is now applied to Case 1. The results in Fig. 8.23 show that this particular multi-mode supplementary controller, when applied to the Case 1 dual-compensated system, fails to restore the overall system stability: the time domain results show that all the system variables are still negatively damped, although the amplitudes of these oscillations have been reduced considerably from those in the uncontrolled Case 1 example shown in Fig. 8.1. The FFTs in Fig. 8.23 show that the presence of the Mode 2 and Mode 3 frequency components in the system variables has been significantly reduced compared to those in Fig. 8.2, even though this reduction is not sufficient to bring the system back to stability. On the other hand, the amplitudes of the Mode 1 frequency components in all the system variables remain almost at the same level as those in Fig. 8.2 when the system was not provided with a supplementary controller.

Multi-Modal Damping Controller Applied To The Case 2 Dual-Compensated System

The results in section 8.2 showed that the dual-compensated system in Case 2 ($X_c = 0.224$ pu and $X_g^* = 0.1467$ pu) is fairly stable with no supplementary damping control on the SSSC, with Modes 1 and 3 dominating the system response.

Fig. 8.24 shows the time domain response and frequency domain characteristics obtained when the multi-modal controller that was specifically designed for the Case 3 dual-compensated system to damp out Mode 1, Mode 2 and Mode 3, with gains $K_{SSR1} = 0.7$, $K_{SSR2} = 0.3$ and $K_{SSR3} = 0.05$, is now applied to Case 2. The results in Fig. 8.24 show that this particular multi-mode supplementary controller, when applied to the Case 2 dual-compensated system, is able to provide positive damping to all modes: the time domain results show that all the system variables are now positively damped. The FFTs in Fig. 8.24 confirm that the presence of both the Mode 1 and Mode 3 frequency components in the system variables has been significantly reduced from the uncontrolled Case 2 example shown in Fig. 8.4.

This set of studies has considered the use of a multi-modal supplementary damping controller designed for the Case 3 dual-compensated system, applied to the Case 1 and Case 2 dual-compensated systems. The results have shown that for the Case 1 dual-compensated system, the supplementary controller was not able to provide damping to all the modes that the controller was designed to damp out in the other case example, and the system remains unstable. On the other hand, the results from the Case 2 dual-compensated system have shown that such a supplementary controller performs fairly well, as it provides sufficient damping to stabilise all modes in the system.

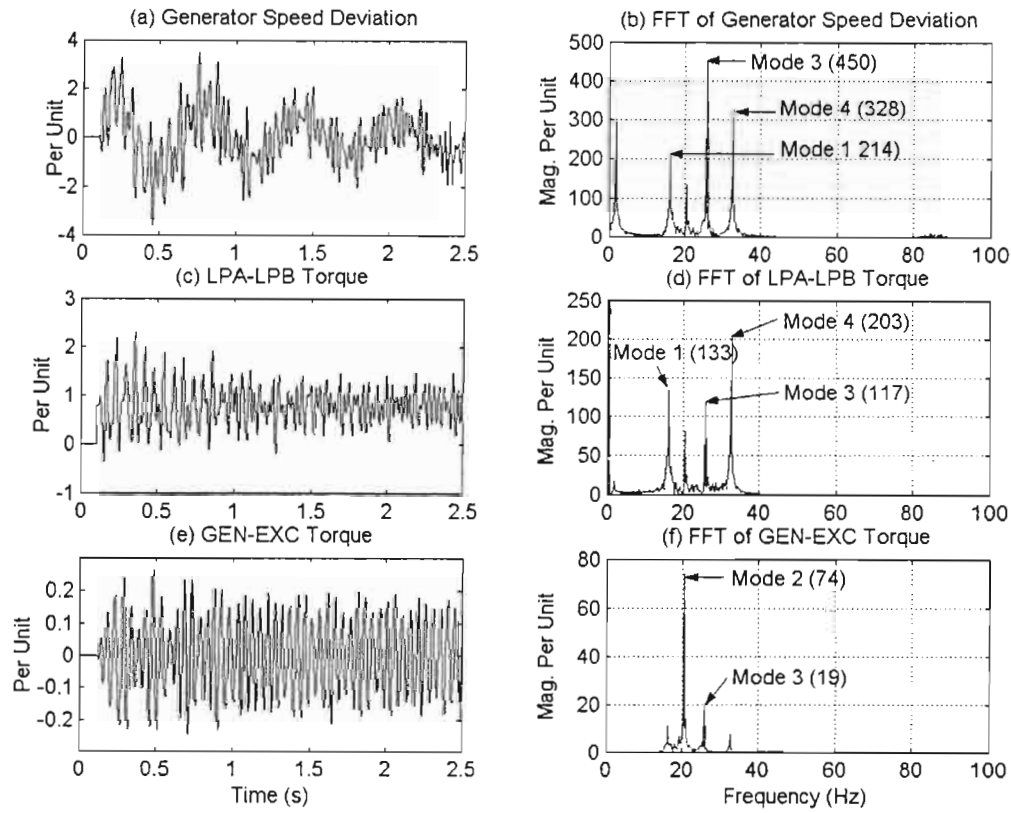


Fig.8.24: Time-domain response and frequency-domain characteristics for Case 2 dual-compensated system: Mode 1 and Mode 3 loops of the multi-modal damping controller designed for Case 3 dual-compensated system activated; $K_{SSR1} = 0.7$, $K_{SSR2} = 0.3$ and $K_{SSR3} = 0.05$.

The results of this section have shown that a multi-modal supplementary damping controller designed to damp out SSR for one combination of conventional series capacitor and SSSC compensation is not, in general, able to completely stabilise SSR for another, different combination of conventional and SSSC compensation. However, the results of these cross-case damping studies are positive in one respect: in nearly all cases considered, although the application of a damping controller designed for one dual-compensation case does not completely stabilise other such cases, it does generally provide some improvement in their stability. This, the aim of achieving a single-design of an SSSC supplementary damping controller that is applicable to a wide range of compensation values is clearly much more demanding in dual-compensated systems, than in a system compensated solely with an SSSC. However, it may be possible, using the multi-modal damping controller structure proposed in this chapter, to come up with a small set of pre-designed damping controllers that can be gain scheduled, according to the SSSC's value of X_q^* , in order to allow stable operation for a range of compensation values in a dual-compensated system.

8.6 Practical Considerations

This thesis has considered the application of an SSSC in the IEEE First Benchmark Model for the study of SSR, both in terms of the SSR characteristics of an SSSC, and in terms of its ability to damp SSR via supplementary controls. However, an important concern which cannot be ignored is the electrical rating of an SSSC that would be required for such an application. Reference [15] states that the MVA rating of inverter-based compensator equipment, and hence its cost, is derived from the product of peak ac voltages and currents, regardless of whether they occur together or not. In the IEEE First Benchmark Model, for which the system base power is 890MVA, a maximum value of SSSC compensation of 0.4pu (as considered in this thesis) would imply a MVA rating of the SSSC of approximately 360MVA. Such an SSSC rating is just over double that of the practical UPFC installation described in [15], albeit at a system voltage of 138kV as compared to 500kV for the IEEE First Benchmark Model. Thus, it should be noted that the inclusion of an SSSC in the IEEE First Benchmark Model is definitely an expensive technology option, and this fact would need to be borne in mind when considering the SSSC as an option in practice.

8.7 Conclusion

This chapter has considered whether supplementary damping control added to an SSSC is able to stabilise SSR when the SSSC is used in conjunction with conventional series capacitors to compensate the transmission line of a benchmark study system. The chapter began by investigating the resonant characteristics of this dual-compensation approach in the IEEE First Benchmark Model, using the detailed SSSC model developed in Chapter Three, for a range of values of both conventional and SSSC compensation. It was found that when the combination of SSSC and conventional series capacitors is used to compensate the system, the resonant characteristics become complex and strongly multi-modal in nature.

The chapter then considered whether a single supplementary damping controller can be used to damp the complex, multi-modal resonances in a dual-compensated transmission system in general, and not simply at one value of SSSC compensation as originally proposed in, and studied in, reference [65]. The results have shown that the ability to arrive at a successful supplementary SSR damper for the SSSC, even at one value of SSSC compensation, depends very much on the value of SSSC and conventional capacitor compensation used, and that *in general*, it is not possible to stabilise SSR in a system comprising conventional series capacitors and an SSSC with

a supplementary damping controller designed for a single mode frequency. Rather, it has been shown that such controllers, designed to damp one mode frequency, tend to destabilise other dominant modes. This finding does not contradict the findings in [65] *per se*: rather, the conclusion that can be drawn by revisiting the proposals in [65] in this chapter using a benchmark study system, and for a *range* of values of SSSC compensation, is that each dual-compensated system requires careful, individual analysis of the full range of compensation values likely to be provided by the SSSC in practice to determine whether the simple damping controller proposed in [65] will suffice.

This chapter then further extended the work described in [65] by considering the design of multi-modal supplementary damping controllers for an SSSC in the dual-compensated benchmark study system. The results of these studies have demonstrated that using the multi-modal extension of the idea proposed in [65], it is possible to successfully damp out the strong multi-modal torsional resonances evident in dual-compensated systems, at least for the range of values of compensation considered in the chapter. It can therefore be concluded that this multi-modal form of SSSC supplementary damping controller is much better suited to the task of damping out SSR in a dual-compensated study system than is the simpler supplementary controller structure proposed in [65], at least at the operating conditions for which the controller was designed.

However, the final section of this chapter has shown that even a multi-modal damping controller that is successfully able to damp torsional oscillations at one combination of conventional and SSSC compensation is not able to completely stabilise the system at different values of compensation. Thus, some form of supplementary damping controller gain scheduling would likely be required in practice to allow the dual-form of compensation to be used whilst allowing the full flexibility of the SSSC's variable compensation to be utilised without causing SSR instability.

CHAPTER NINE

CONCLUSION

9.1 Introduction

The first part of this thesis has dealt with the development of both detailed and simplified simulation models of inverter-based FACTS devices, namely the Static Synchronous Compensator (STATCOM), Static Synchronous Series Compensator (SSSC) and Unified Power Flow Controller (UPFC). Although the thesis has considered the mathematical modelling of all of these three inverter-based FACTS devices, most attention has been paid to the development of industry-standard, X_q -controlled SSSC, where the controllable ac series compensating voltage of the SSSC is *dependent* on the magnitude of the line current.

The second part of the thesis has then used the detailed simulation model of the SSSC to study the potential problem of subsynchronous resonance (SSR) being caused by this form of compensation. Furthermore, two different types of supplementary damping controller for the SSSC have been considered as possible practical solutions to the problem of SSR: a single-mode supplementary controller when the transmission line is compensated by an SSSC alone, and a multi-modal supplementary damping controller when the transmission line is compensated by the combination of conventional series capacitors and an SSSC.

This chapter now summarises and reviews the main findings and conclusions drawn from the previous chapters. The chapter also suggests further research work that may be undertaken in this area.

9.2 Three-Level Multi-Pulse Inverter Model

The power electronic inverter is the basic building block of any SSSC. In this thesis, multi-pulse inverter configurations were considered for study since they are typically employed in actual transmission line FACTS applications. Chapter Two focused on the theory of operation of three different types of three-level voltage-sourced inverters, namely, the 6-pulse, 12-pulse and 24-pulse

three-level inverter. Detailed simulation models of these inverters were developed for the simulation package PSCAD/EMTDC; the 6-pulse and 12-pulse inverter models were considered as intermediate steps towards the final goal of a 24-pulse, three-level inverter model. In each case, the simulation models developed represent the power electronic devices and the low-level firing controls required in the voltage-sourced inverter.

Using these detailed simulation models, Chapter Two demonstrated that in comparison to the 6-pulse and 12-pulse inverters' time-domain waveforms, the waveforms obtained from the 24-pulse inverter are near sinusoidal and that the quality of these waveforms remains high even at high values of dead angle γ . Moreover, the frequency-domain results from the 24-pulse inverter were shown to have a total harmonic distortion (THD) below 10% for a wide range of γ values, which is relatively low when compared to both 6-pulse and 12-pulse inverters. The time-domain and frequency-domain results obtained from each of the inverter simulation models developed in PSCAD/EMTDC were compared against their respective theoretical equations and showed close agreement.

The detailed simulation models of inverter-based FACTS devices subsequently presented in the thesis made use of this 24-pulse three-level inverter developed in Chapter Two.

9.3 Detailed Models of Inverter-Based FACTS Devices

Three essential components are needed to construct any inverter-based FACTS device: they are the voltage-sourced inverters, coupling transformers and the associated high-level controls. The development of detailed models of the three inverter-based FACTS devices in this thesis has employed the detailed 24-pulse three-level inverter simulation model described above, and the voltage injecting transformers are three simple single-phase transformers coupled onto the transmission line. The component that defines the characteristics and functioning of a particular inverter-based FACTS device is its high-level controller.

This thesis began the development of inverter-based FACTS devices by modelling two types of stand-alone X_q -controlled SSSC, namely, the two-level SSSC and the three-level SSSC. As the name "two-level SSSC" suggests, the 24-pulse three-level inverter was operated as a two-level device by setting the inverter dead angle γ to zero so that the dc-to-ac gain across the inverter was fixed at a certain value. In this mode of operation, the ac output voltage of the inverter can only be varied by adjusting the magnitude of the inverter's dc voltage. The three-level SSSC, on the

other hand, exploits the full functionality of a three-level inverter where the inverter's output ac voltage can be varied either by adjusting the inverter's dc voltage or by changing its dc-to-ac gain by means of the dead angle γ . Whereas the two-level inverter satisfies the operational and functional requirements of a stand-alone SSSC, it is not suitable for cases where the SSSC is combined with a STATCOM to form a UPFC; a three-level inverter with its controllable inverter gain, is required in such cases. The three-level SSSC, however, is not restricted to instances where the SSSC is operated as a part of a UPFC; it can also be employed for stand-alone SSSC applications.

The high-level control scheme within the two-level SSSC was closely based on the work in reference [34] and was implemented such that there were three inter-linked sections, namely, angle control, magnitude control and the dc voltage regulator. The 24-pulse two-level inverter, the high-level controller and the series injecting transformers complete the overall two-level SSSC simulation model, which was then connected to a simple ac transmission line model based on that in [34] for the purpose of benchmarking. A similar system configuration was used for the three-level SSSC, and a *modified* high-level SSSC controller was introduced to operate the inverter in three-level mode. In this three-level SSSC, the high-level control scheme now consisted of four control sections, namely, angle control, magnitude control, the dc voltage regulator, and the dead-angle calculator; this allowed the ac output voltage to be controlled by adjusting the inverter dead angle γ , while the inverter's dc voltage is regulated to some value set by an operator.

The simulation results from the two-level and the three-level SSSC models in PSCAD/EMTDC were compared to the results simulated in EMTP by Sen [34] and have shown that under steady state and dynamic conditions, the ac compensation performance of both the two-level and three-level SSSC are virtually identical to that of the two-level SSSC simulated in EMTP by Sen [34], and therefore confirm the correctness of the more detailed SSSC models developed in PSCAD/EMTDC. Hence, this study illustrated that the operation and functionality of either type of SSSC remains very similar despite differences in inverter technology and in the high-level SSSC controls.

The thesis has also demonstrated that by setting the desired dc voltage appropriately in the three-level SSSC, the total harmonic distortion (THD) of the injected ac voltage could be kept within acceptable levels as the operating conditions of the compensated transmission line change. Therefore, the ability to adjust the THD in the three-level SSSC is one advantage over the two-level SSSC where the THD is fixed at a certain level.

The thesis then extended the modelling study to the other two inverter-based FACTS devices, namely, the stand-alone, two-level static synchronous compensator (STATCOM) and a unified power flow controller (UPFC). The stand-alone STATCOM model is based on the two-level inverter where the output voltage is controlled by varying the inverter dc voltage. The desired shunt current that flows between the STATCOM and the transmission line determines the inverter's output voltage magnitude in relation to the line voltage. This in turn influences the reactive power being exchanged at the STATCOM terminals. In the UPFC model, the STATCOM is again operated as a two-level device (with $\gamma = 0^\circ$) and has sole control over the dc link capacitor voltage. Because the dc link voltage is control by the STATCOM, the SSSC as a part of the UPFC must be based on the three-level inverter where the magnitude of the series injection voltage is not dependent on the dc capacitor voltage but controlled by varying the dead angle γ , thus varying the inverter gain. The SSSC is then allowed to inject a voltage that is a two-dimensional vector quantity [14]; in other words, it is able to not only influence the reactive power in the line but also the active power depending on the mode of operation.

The STATCOM and UPFC models were closely based on reference [27] in which these FACTS device models were developed for the simulation program EMTF. The high-level control scheme within the stand-alone STATCOM consists of two inter-linked sections, namely, phase control and magnitude control. The 24-pulse two-level inverter, the high-level controller and the coupling transformers complete the overall two-level STATCOM simulation model, which was then connected to a simple ac transmission line model based on that in [27] for the purpose of benchmarking. A similar system configuration was used for the UPFC, with the inclusion of a three-level SSSC whose high-level control scheme also consisted of phase control and magnitude control, to allow the voltage vector to be inserted at any desired magnitude and phase in relation to the line voltage.

The simulation results from the STATCOM and UPFC models in PSCAD/EMTDC were then compared to the results simulated in [27] and were shown to be virtually identical, thus confirming the correctness of the more detailed STATCOM and UPFC models developed in PSCAD/EMTDC.

Although the PSCAD/EMTDC inverter-based FACTS device models developed in this thesis were based closely on those in [34] and [27], unlike [34] and [27] this thesis has represented the actual power electronic devices within the 24-pulse inverter as well as the low-level power electronic firing controls. Therefore the PSCAD/EMTDC model of the inverter-based FACTS devices presented in this thesis are thorough and detailed.

9.4 Continuous-Time SSSC, STATCOM And UPFC Models

The highly detailed inverter models are not always required to carry out performance studies on FACTS devices: often a simplified, continuous-time model of a voltage-sourced inverter is employed instead in order to save an otherwise large amount of simulation time. Furthermore, this modelling approach allows for more rapid analysis and debugging of high-level control schemes that are present in these inverter-based FACTS devices, at least in the initial development phase. In addition, for detailed analysis of issues like SSR, this continuous-time representation of the inverter allows the FACTS device model to be linearised about a particular steady state operating point so that eigenvalue analysis can be done. In the case of some FACTS device studies, it may even be possible to avoid using detailed inverter models without suffering too much loss in accuracy.

This thesis has therefore presented a continuous-time model of a voltage-source inverter developed for the simulation package PSCAD/EMTDC. This simplified inverter model outputs a continuous-time waveform that exhibits only the fundamental frequency component of the actual inverter voltages. The magnitude of this output voltage is based on the measured dc capacitor voltage and the required dead angle γ . This thesis has also described the process used to design such an inverter model in PSCAD/EMTDC.

This continuous-time inverter model was then used to develop simplified SSSC, STATCOM and UPFC models, the results of which have been shown to be very similar to those obtained from the detailed models developed in the thesis, and therefore validate the accuracy of these simplified inverter-based FACTS models. These models can now form the basis of further study in this area, including the development of linearised models, now that the characteristics of the full, detailed FACTS device models, in particular those of the SSSC, have been established for SSR studies.

9.5 Resonant Characteristics Of The Two-Level SSSC

When implementing series compensating devices like the SSSC, the resonant characteristics of the compensating device in the frequency domain are of importance and should be examined in detail due to the concern that such devices may cause subsynchronous resonance (SSR), which poses a serious threat to the power system. The literature review in this thesis has revealed many claims that inverter-based series compensating devices are essentially ac voltage sources that only

operate at the fundamental frequency, in other words that the reactances emulated by these devices are theoretically zero at all other frequencies. It has been claimed that as a result, these inverter-based series compensating devices are unable to form the classical series RLC resonant circuit that leads to SSR, and that they are therefore immune to SSR. Subsequently, contrary claims [18,33] have been made based on examining the electrical impedance characteristics of inverter-based series compensators in the frequency domain.

This thesis therefore carried out a simple frequency-domain analysis of the transmission line impedance in the IEEE First Benchmark Model for the study of SSR for the case where the line is compensated with the two-level SSSC model developed earlier in the thesis. The results from the frequency-domain study have shown that the transmission line compensated with the SSSC exhibits a resonant minimum in its impedance at a subsynchronous frequency, at which the total line impedance is purely resistive. Similar to conventional capacitor compensation, the SSSC acts as a capacitive reactance not only at the fundamental frequency but at *all* frequencies. This finding is therefore in agreement with the findings in [18,33], but in this thesis the frequency domain analysis has been carried out with a detailed SSSC model that includes that SSSC's inverter power electronics and low-level firing controls, and employs the type of inverter technology most likely to be used in high-power applications.

It has also been demonstrated that, as is the case in a transmission line compensated with conventional series capacitors, when the compensating capacitive reactance provided by the SSSC is increased, the resonant frequency in the line impedance increases. However, conventional capacitive compensation and the SSSC form of compensation result in different resonant frequencies for the same compensation ratio. Hence, the theoretical equation for the resonant frequency of a conventionally compensated line does not hold for the case of SSSC compensation. Once again, this finding is consistent with those in [18,33].

The thesis further investigated the interactions between a transmission line compensated by either two-level or three-level SSSCs and the multi-inertia turbo-generator of the IEEE SSR First Benchmark Model. The results have shown that, in a similar manner to conventional series capacitor compensation, the electrical resonant frequency caused by either type of SSSC may excite one or more mechanical shaft modes. This interaction may result in large, poorly-damped, or even self-excited oscillations. Also, even when the SSSC does not cause large persistent oscillations, it still excites shaft torque oscillations. It was therefore concluded that this inverter-based form of series compensation can cause torsional interaction but that the degree of destabilization caused is less than that caused by conventional capacitors. Therefore, special care is still needed when implementing such devices in practice in order to avoid unwanted

resonances, despite the numerous advantages that the SSSC provides over conventional capacitors.

9.6 Supplementary Controllers For The Three-Level SSSC

In order to provide practical solutions to the SSR problems that arise when a transmission line is compensated solely by an SSSC, a supplementary controller, proposed by others [65], was considered to damp out a single mode frequency found to be predominant in the system oscillations. The thesis described in detail the process used to design this single-mode supplementary damping controller in the work presented here. The simulation results have shown that the single-mode supplementary controller was able to successfully damp out the desired mode and stabilise the system at its design operating point.

Furthermore, the thesis considered the performance of this fixed-design, single-mode supplementary controller for the SSSC at values of SSSC compensation other than that at which the controller design was originally carried out. The results of these studies have shown that a single-design supplementary controller, added to the SSSC, can allow it to operate over a range of values of series compensating reactance without causing SSR, when the SSSC is the only form of compensation in the transmission line; also, the damping controller does not have a negative influence on the system damping for values of SSSC compensation that are already stable without supplementary control. These results have therefore extended the findings in [65], since that study considered the SSSC at a single value of compensation, purely to damp out SSR caused primarily by conventional series capacitors. This thesis has shown that the single-mode supplementary damping controller idea proposed in [65] can also be used to extend the safe variable-compensation operating range of an SSSC in systems where SSR is a concern and where only SSSC compensation is to be used.

Subsequently, the study into supplementary damping control in the thesis was extended to consider a more practical scenario in which the transmission line was compensated by both conventional series capacitors and a three-level SSSC. A detailed SSR analysis was conducted on this dual-compensation approach in the IEEE First Benchmark Model, for a range of values of both the conventional and the SSSC components of the dual compensation. The results of these studies showed that when the combination of SSSC and conventional series capacitors is used to compensate the system, the resonant characteristics become complex and strongly multi-modal in nature.

The study then considered the use of a single supplementary damping controller to damp the complex, multi-modal resonances in a dual-compensated transmission system for a range of values of compensation, and not simply at one value of SSSC compensation as originally proposed in, and studied in, reference [65]. The results have shown that *in general*, it is not possible to stabilise SSR in a system comprising conventional series capacitors and an SSSC with a supplementary damping controller designed for a single mode frequency. It was found that the possibility of the supplementary controller being able to successfully restore the overall system stability, even at one value of SSSC compensation, depends very much on the values of SSSC and conventional capacitor compensation used. Indeed, it was shown that in general, such controllers, designed to damp one mode frequency, tend to destabilise other dominant modes. This finding does not contradict the findings in [65] *per se*; rather, it can be concluded that for a *range* of values of SSSC compensation, each dual-compensated system requires careful, individual analysis of the full range of compensation values likely to be provided by the SSSC in practice to determine whether the simple damping controller proposed in [65] will suffice.

The thesis then further extended the work described in [65] by proposing the use of a multi-modal supplementary damping controller for an SSSC in dual-compensated systems. A detailed description of the design of such a damping controller was presented for a range of dual-compensation cases in the IEEE First Benchmark Model, and the performance of the proposed controller examined in depth. The results of these studies have demonstrated that by using the multi-modal supplementary controller, it is possible to successfully damp out the strong multi-modal torsional resonances evident in dual-compensated systems, at least for the range of values of compensation considered in the thesis. It can therefore be concluded that this multi-modal form of SSSC supplementary damping controller is much better suited to the task of damping out SSR in the dual-compensated study system, at least at the operating conditions for which the controller was designed.

However, it was shown that even a multi-modal damping controller that is successfully able to damp torsional oscillations at one combination of conventional and SSSC compensation is not able to completely stabilise the system at different values of compensation. Thus, some form of supplementary damping controller gain scheduling would likely be required in practice to allow the dual-form of compensation to be used whilst allowing the full flexibility of the SSSC's variable compensation to be utilised without causing SSR instability.

9.7 Suggestions For Further Work

This thesis has presented detailed models of the SSSC, STATCOM and UPFC, focusing in particular on the multi-pulse inverters at the heart of the devices, but also on the high-level controls of these inverter-based FACTS devices. The detailed SSSC models have been developed in order to be able to predict, with a high degree of confidence, any interactions that may occur between SSSCs and the rest of the power system. However, there are further areas in this field of inverter-based FACTS devices that still need to be explored and investigated. Therefore much scope exists for further research on this subject. Some suggestions for further work are as follows.

- (a) This thesis has focused solely on model development and investigation of the X_q -controlled SSSC. Future work could consider the V_q -controlled SSSC where the series compensating voltage is *independent* of the magnitude of the line current. As in this thesis, the detailed SSSC model could be used to investigate the resonant characteristics of this form of compensation, and to compare it to that of conventional and X_q -controlled SSSC compensation. Some work in this area has already been carried out [21,42,43,46] but, as with the X_q -controlled SSSC, contradictory claims regarding the resonant characteristics of the V_q -controlled SSSC have been made. The development of a detailed model of the V_q -controlled SSSC will also allow comparison to be made against the X_q -controlled SSSC in regards to performance and functionality in other FACTS application studies.
- (b) The thesis has developed a UPFC model for the use in voltage injection mode. However, as the UPFC also offers a variety of different operating modes that include reactance emulation mode, phase shifting mode and power flow control mode, each of these modes of operation could be considered in future work. Similar to the SSR study carried out on the SSSC, investigations could also be done on the resonant characteristics of a UPFC in a transmission line compensated by a UPFC alone, or by a combination of UPFC and conventional capacitors. Supplementary controllers could also be designed and implemented for the UPFC in order to assist in the overall system damping.
- (c) This thesis developed simplified, continuous-time models of inverter-based FACTS devices which can be used to develop linearised models of these FACTS devices for future eigenvalue studies into their SSR characteristics and the design of better supplementary damping controllers.

- (d) Finally, practical confirmation of the findings of this thesis could be considered by implementing a scaled-down laboratory test system with a three-level inverter-based SSSC. When considering practical implementation of multi-pulse inverter arrangements, the insight gained from the detailed power-electronic modeling of these inverters in this thesis would be valuable.

APPENDIX A

PSCAD/EMTDC SIMULATION MODELS FOR THREE-LEVEL INVERTERS

A.1 Introduction

Chapter Two of this thesis shows a series of simulation results to demonstrate the characteristics of the detailed models of multi-pulse, three-level inverters that have been developed for the PSCAD/EMTDC simulation program. In this appendix the development and design of these inverter simulation models is described in more detail. It can be seen from Chapter Two that the single-pole three-level inverter is the foundation of all the multi-pulse inverters.

A.2 The Single Pole Three-Level Inverter

Fig. A.1 shows the graphical representation of one phase-leg of a three-level inverter and associated voltage sources and low-level firing controls developed in PSCAD/EMTDC. The topology of the inverter in Fig. A.1 is the same as that in Fig. 2.1 in Chapter Two; the two capacitors have been replaced by two identical constant dc voltage sources, and the inverter is connected to a pure resistive load to ground.

As shown in Fig. A.1, the inverter topology is built up by assembling GTOs and diodes using the models of these individual power electronic switches provided in PSCAD/EMTDC. A three-phase ac source is used to mimic the ac voltage from a transmission line and to provide the desired instantaneous phase angle θ through the EMTDC built-in three-phase PI-controlled phase locked loop functional block which tracks the positive sequence of the input signal. The subroutine behind this functional block generates a ramp called “theta” (θ), shown in Fig. A.2(a) which varies between 0° and 360° , synchronized or locked in phase, to the phase-a voltage [80]. This θ is then connected to a user-defined-model in PSCAD/EMTDC called the “Modulo” which restrains ramps to between 0° and 360° at the fundamental frequency. These ramps are then converted to triangular signals by the Non-linear Transfer Characteristic functional block [56]. This phase angle together with the dead angle γ , are the inputs to the low-level inverter firing controls.

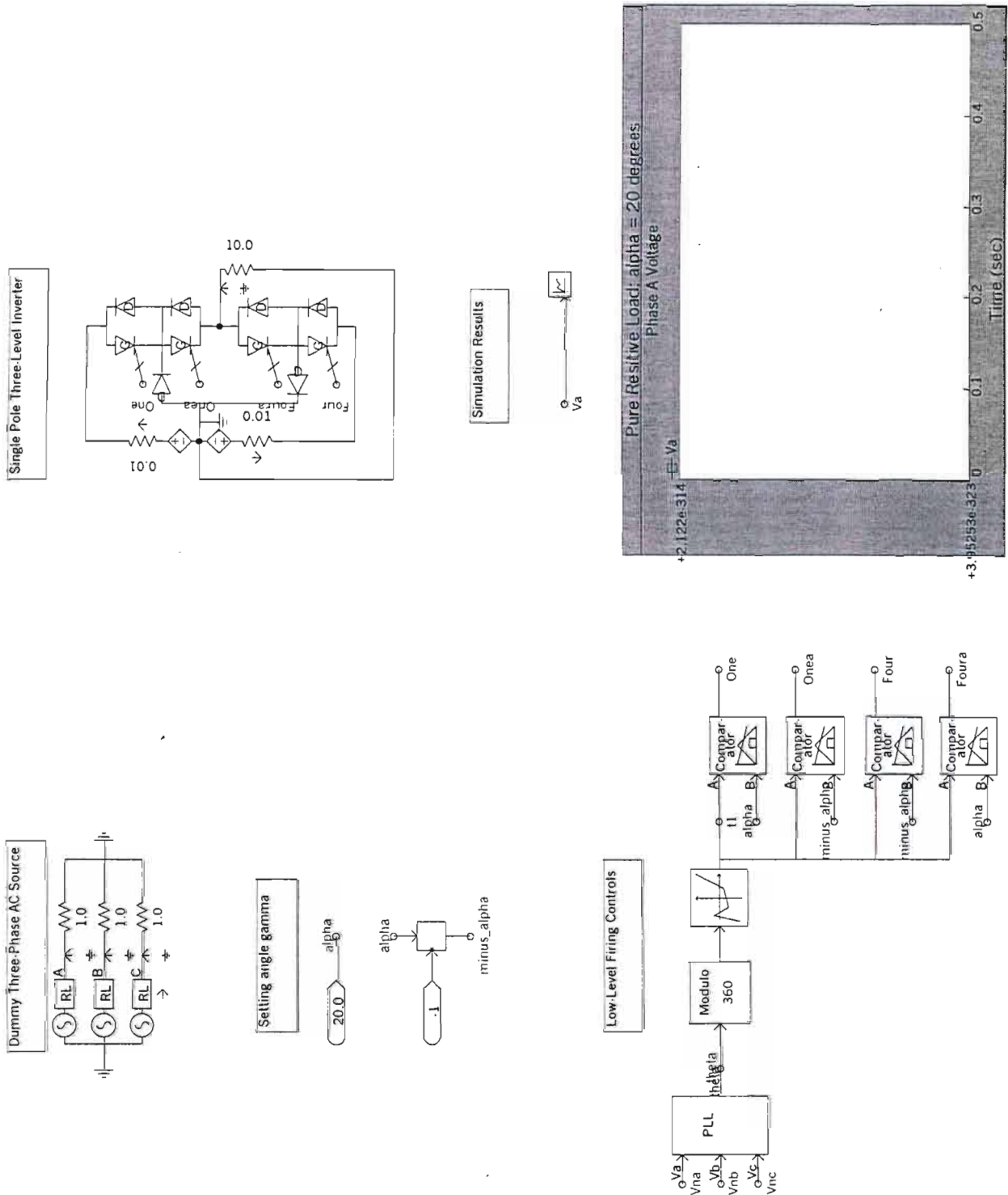


Fig. A.1: The detailed PSCAD/EMTDC representation of the single pole three-level inverter.

The firing control scheme itself uses specially designed functions and logic blocks to manipulate these inputs: a special triangular wave is generated from the instantaneous phase angle θ of the desired ac output waveform and this triangular wave is compared with $\pm\gamma$ to determine the turn on and turn off instants (and hence firing signals) for each of the GTOs. A timing diagram of this firing control scheme for a value of $\gamma = 20^\circ$ is shown in Fig. A.2.

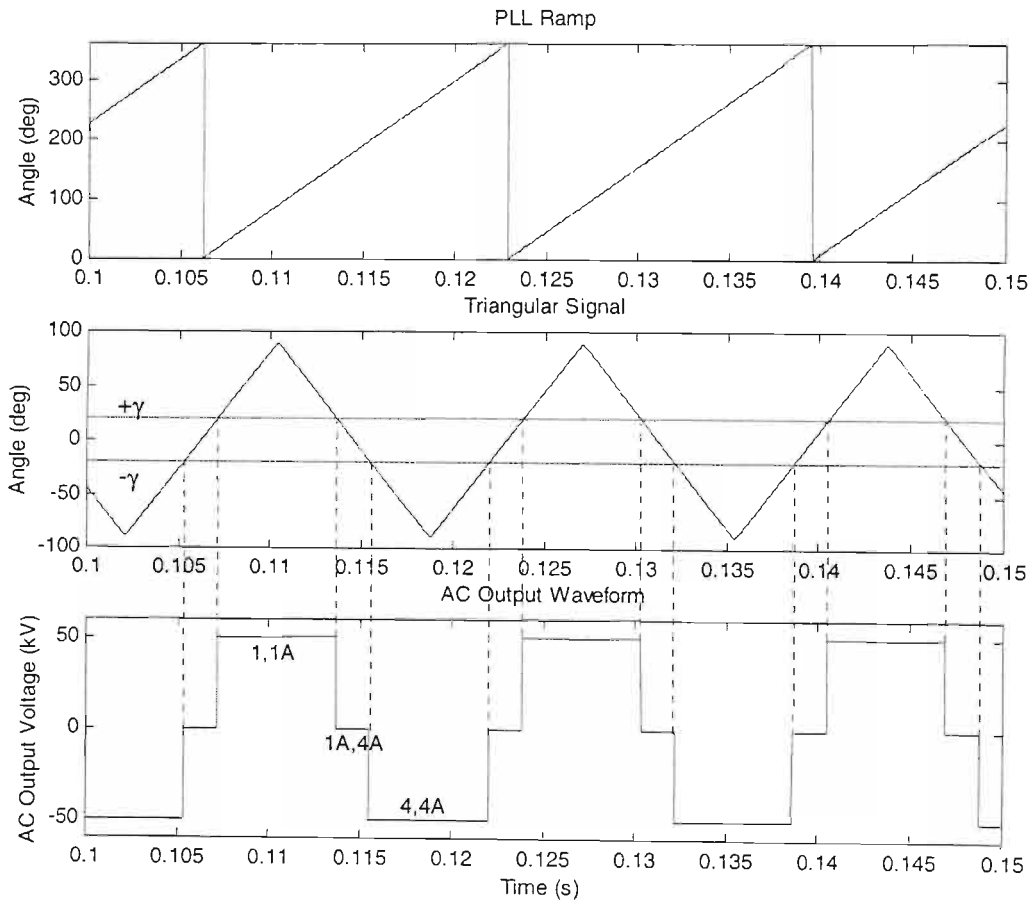


Fig.A.2: Timing Diagram of Low-Level Firing Controls for $\gamma = 20^\circ$: (a) Theta, the output from the Phase Locked Loop; (b) The triangular signal being compared to positive and negative γ ; (c) The output voltage waveform from the single pole three-phase inverter.

With the reference to Fig. A.2(b) and Fig. A.2(c), as well as Section 2.2.3 that described the switching sequence of the inverter GTOs, the following summarizes the logic behind the low-level firing controls.

```
IF  $S_{\Delta}(t) > \gamma^+$ 
THEN switch on GTOs 1 and 1A
ELSE IF  $S_{\Delta}(t) < \gamma^-$ 
THEN switch on GTOs 4 and 4A
ELSE switch on GTOs 1A and 4A
```

where $S_{\Delta}(t)$ is the instantaneous value of the triangular wave;

γ^+ is the positive value of the angle γ ;

γ^- is the negative value of the angle γ .

The outputs of these low-level firing controls are then connected to the gate inputs of the GTOs, so that the inverter output voltage follows the switching pattern.

This low-level firing control scheme for a three-level inverter is not a standard model provided in EMTDC; it has been developed by the author as part of the work of this thesis.

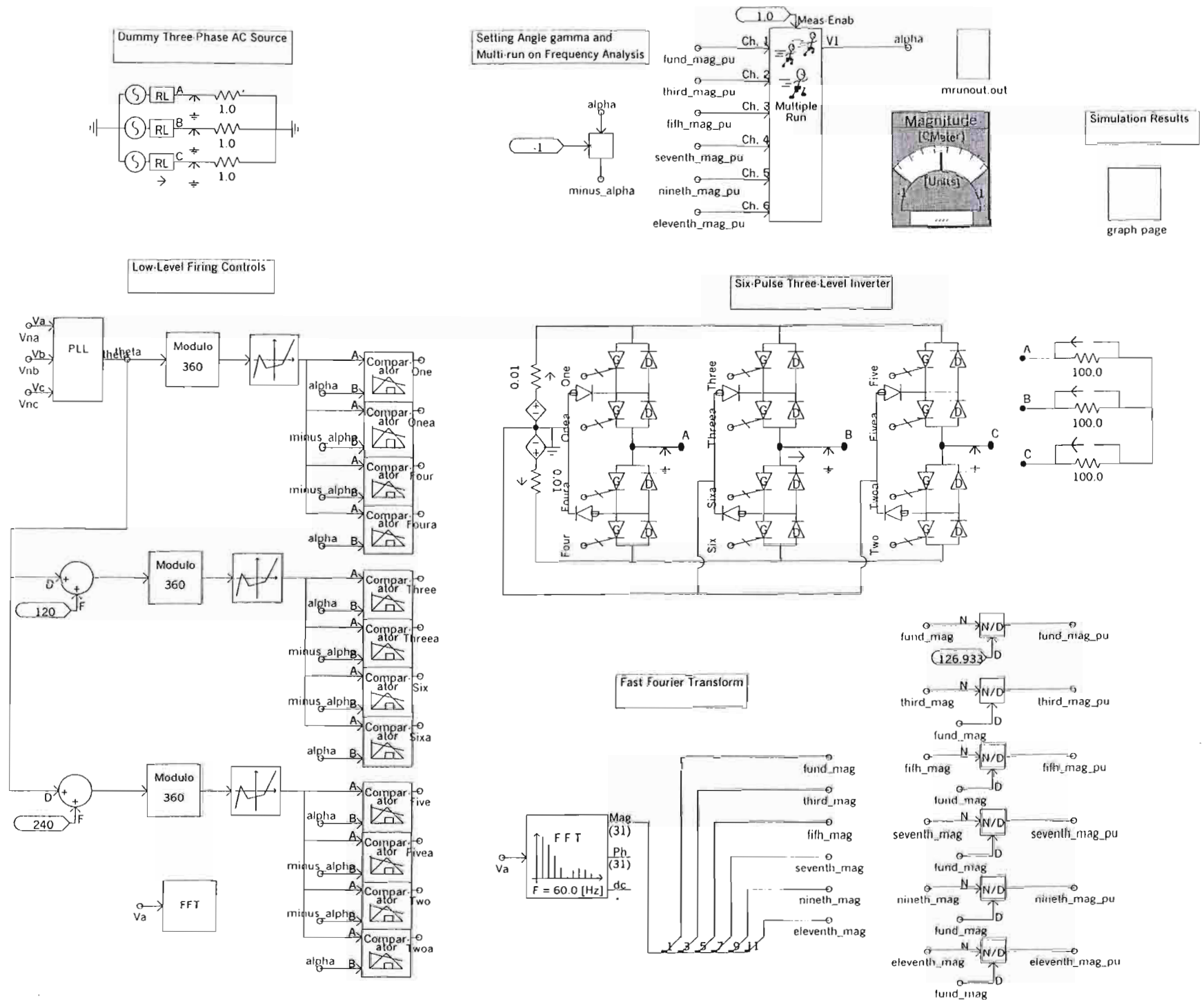
Note that the angle γ is labeled as “alpha” in the simulation models.

A.3 The 6-Pulse Three-Level Inverter

Fig. A.3 shows a detailed representation of the 6-pulse three-level inverter simulation model developed for the work in this thesis. The inverter topology is the same as that shown in Fig. 2.6 in Chapter Two; once again, the inverter topology has been built up using the models of individual GTO and diode switches provided in PSCAD/EMTDC.

The model again comprises a low-level firing control scheme for individual GTOs in the inverter; the inputs to this firing control scheme are the dead angle γ and θ the instantaneous angle of the desired ac waveform. The low-level firing control scheme for each phase or pole of the 6-pulse inverter is similar to the firing control scheme for the single-phase inverter arm described in previous section. However, the special triangular wave generated in each phase of the 6-pulse firing control scheme is phase shifted by 120° from the triangular waves in the other two phases. This 6-pulse three-level inverter firing control scheme is not a standard model provided in PSCAD/EMTDC; it has been developed by the author as part of the work of this thesis.

Fig. A.3: The detailed PSCAD/EMTDC representation of the 6-pulse three-level inverter.



The FFT (Fast Fourier Transform) functional block is used to investigate the harmonic content of the inverter output voltages. Multi-run is a device that allows the simulation model to be run a number of times with a changed value of a variable each time. In this case multi-run is used to vary the input variable γ , in order to investigate the relationship between the fundamental and harmonic frequency outputs and the inverter dead angle for the study in Section 2.3.4. Multi-run can also be deactivated for individual studies, where in the value of γ can be fixed with a floating point constant in PSCAD/EMTDC or imported as an input variable from a high-level FACTS controller. Finally, Fig. A.3 includes a “graph page” that contains all the necessary graphs showing the results from the simulation.

A.4 The 12-Pulse Three-Level Inverter

Fig. A.4 shows a detailed representation of the 12-pulse three-level inverter simulation model developed for the work in this thesis. The 12-pulse inverter topology is the same as that shown in Fig. 2.13 in Chapter Two: two 6-pulse inverters are connected in parallel before connecting to the magnetic circuit comprised of phase-shifting transformers to complete the 12-pulse inverter model. Again, each of the two 6-pulse inverters has been built up using the models of individual GTO and diode switches provided in PSCAD/EMTDC. The special topology of the magnetic circuit is built up from individual single-phase transformers provided in PSCAD/EMTDC.

The model comprises a low-level firing control scheme for individual GTOs in the inverter; the inputs to this model are the dead angle γ and θ the instantaneous angle of the desired ac waveform. Because the low-level firing control scheme for the 12-pulse inverter is relatively complex, it has been developed as a sub-page module whose details are shown in Fig. A.5; the required signals for the firing controls imported from and exported to the main simulation page. The low-level firing control scheme for each phase or pole of the two 6-pulse inverters is similar to the firing control scheme for the single-phase inverter arm described earlier. For each phase of the 6-pulse inverter, the triangular wave generated in the firing control scheme is phase shifted by 120° from the triangular waves in the other two phases. Furthermore, the triangular waves of all three phases of one of the two 6-pulse inverters are phase shifted by 30° with respect to those of the other 6-pulse inverter, thus completing the low-level control scheme.

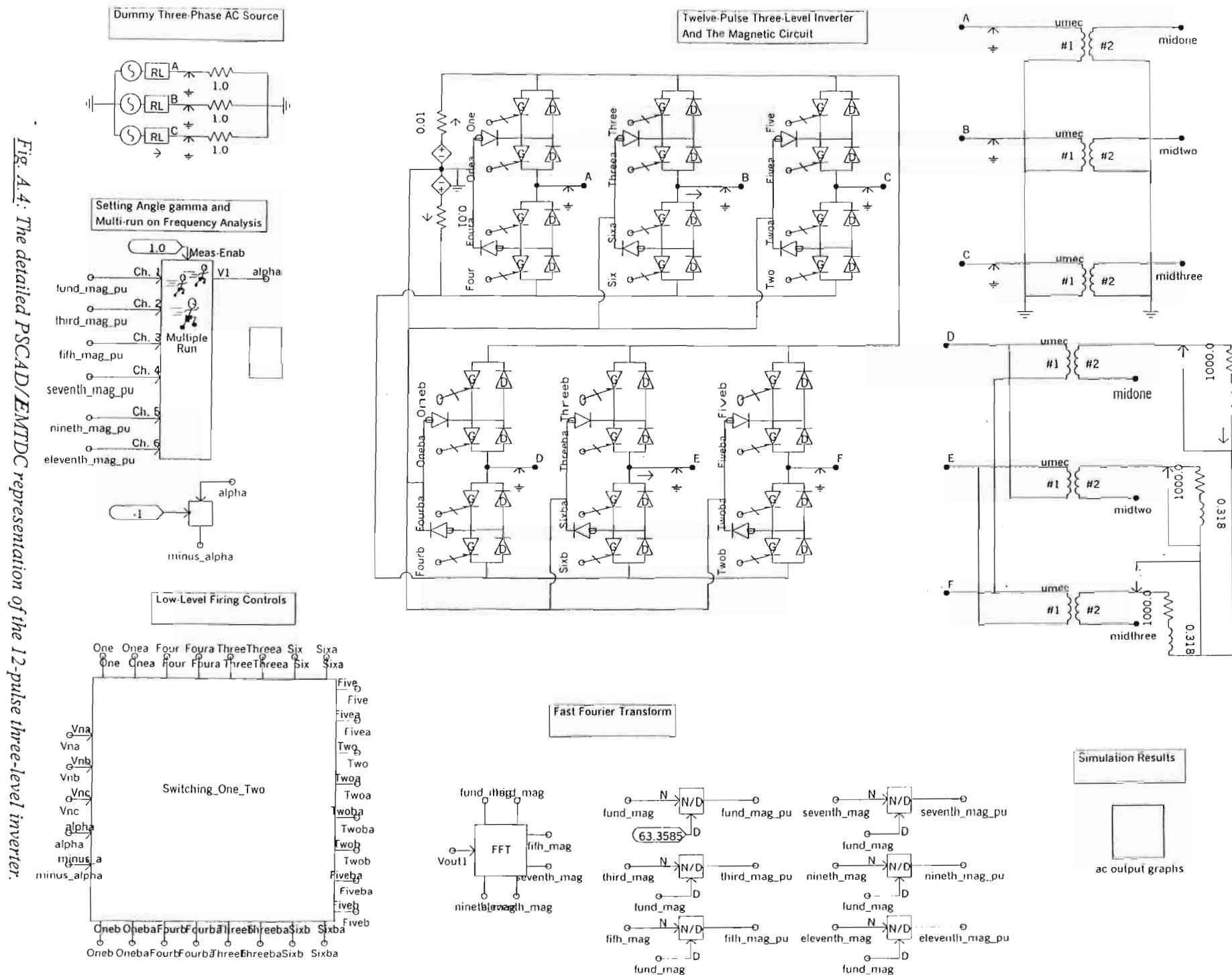


Fig. A.4: The detailed PSCAD/EMTDC representation of the 12-pulse three-level inverter.

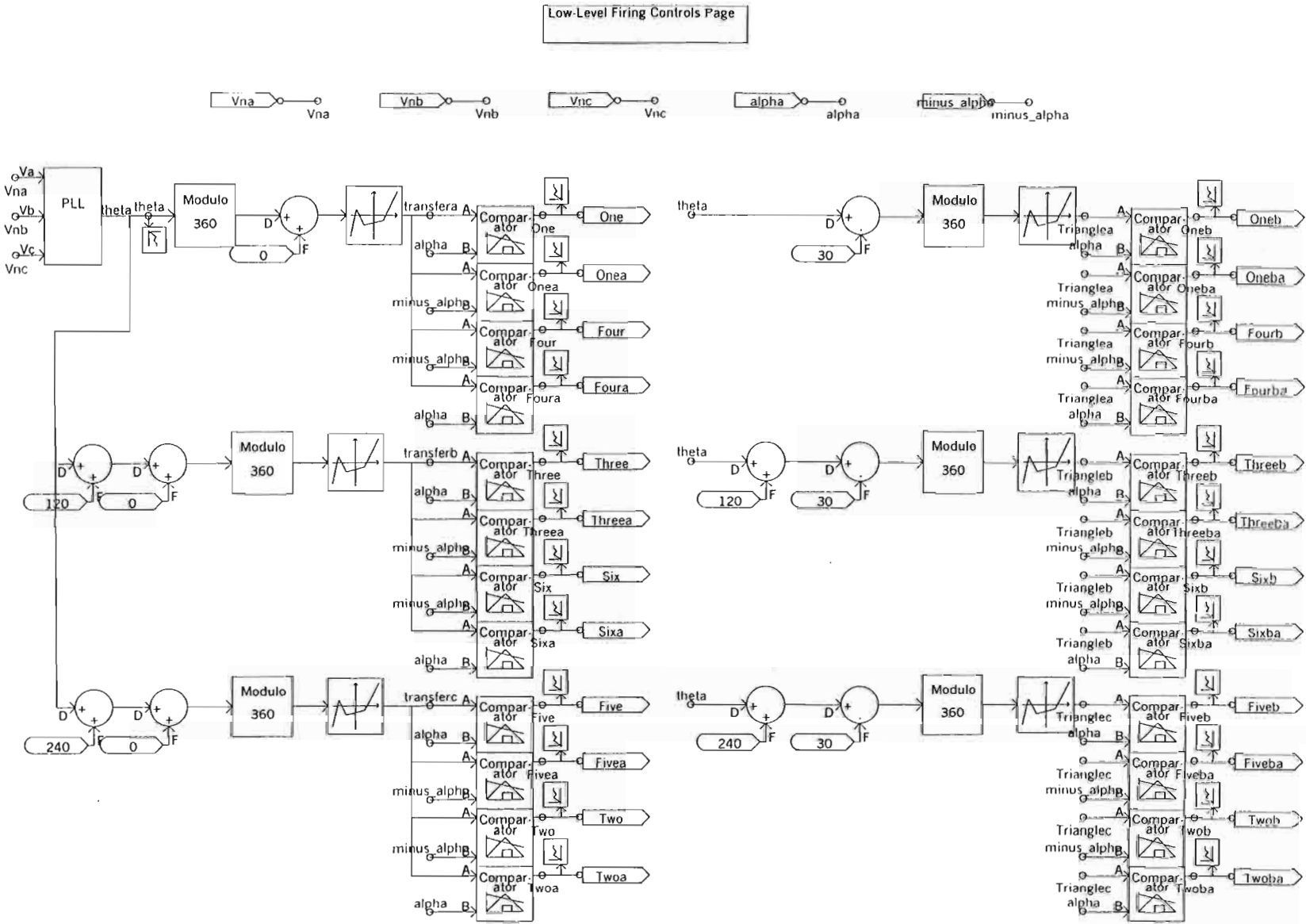


Fig. A.5: The detailed PSCAD/EMTDC representation of the low-level firing control scheme developed for the 12-pulse three-level inverter switching topology (sub-page module Switching_One_Two).

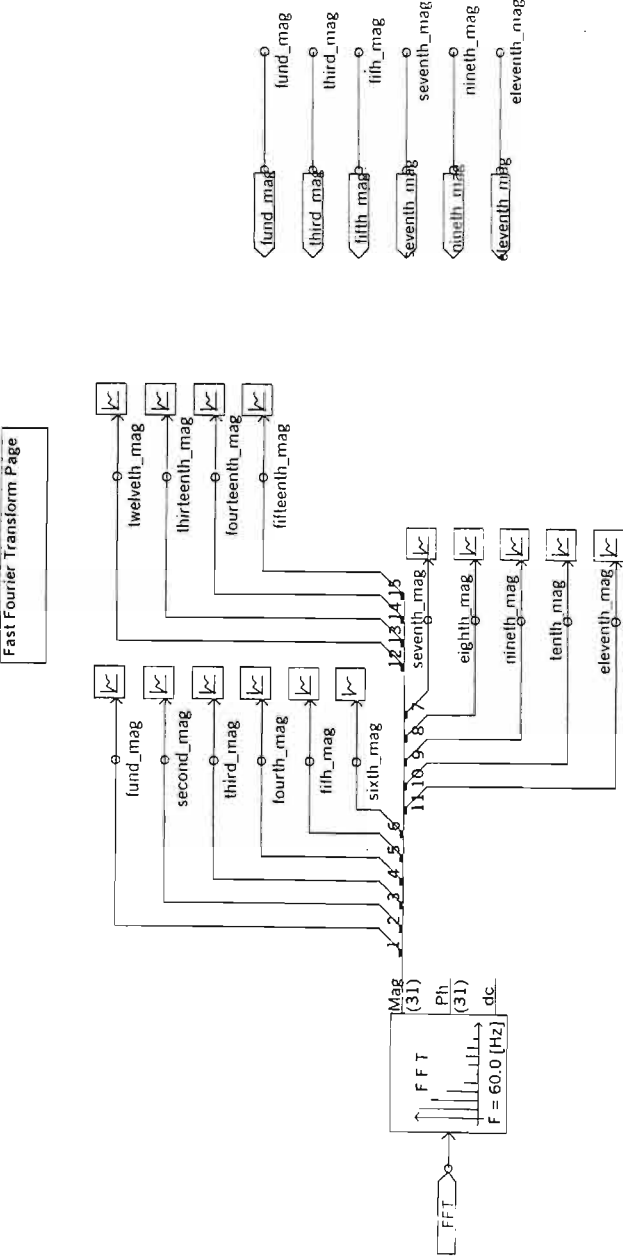


Fig. A.6: The frequency analysis of the 12-pulse three-level inverter model in PSCAD/EMTDC (sub-page module FFT).

This 12-pulse three-level inverter firing control scheme is not a standard model provided in PSCAD/EMTDC; it has been developed by the author as part of the work of this thesis.

In a similar manner to the low-level firing controls, the frequency analysis of the inverter output voltages is also done in a sub-page module called FFT as shown in Fig. A.6.

A.5 The 24-Pulse Three-Level Inverter

Fig. A.7 shows a graphical representation of the 24-pulse three-level inverter simulation model developed for the work in this thesis. The 24-pulse inverter topology is the same as that shown in Fig. 2.20 in Chapter Two: four 6-pulse inverters are now connected in parallel before they are connected to the magnetic circuit comprised of phase-shifting transformers to complete the 24-pulse inverter model. Each of the four 6-pulse inverters have been built up using the models of individual GTO and diode switches provided in PSCAD/EMTDC, and the special topology of the magnetic circuit is built up from individual single-phase transformers provided in PSCAD/EMTDC.

The model comprises a low-level firing control scheme for individual GTOs in the inverter; the inputs to this model are the dead angle γ and θ the instantaneous angle of the desired ac waveform. As with the 12-pulse inverter model, because of the complexity of the low-level firing control scheme for the 24-pulse inverter, it has been developed as two sub-pages modules; these are shown in details in Fig. A.8 and Fig. A.9. The low-level firing control scheme for each phase or pole of the four 6-pulse inverters is similar to the firing control scheme for the single-phase inverter leg described earlier. For each of the 6-pulse inverter, the triangular wave generated in each phase of the 6-pulse firing control scheme is phase shifted by 120° from the triangular waves in the other two phases. Furthermore, with reference to Fig. 2.20 in Chapter Two, all three triangular waves for the 6-pulse inverter A1B1C1 are phase shifted by $+7.5^\circ$. Similarly all three triangular waves for inverter D1E1F1 are phase shifted by -22.5° , those for inverter A2B2C2 by -7.5° and those for inverter D2E2F2 by -37.5° . This 24-pulse three-level inverter firing control scheme is not a standard model provided in EMTDC; it has been developed by the author as part of the work of this thesis.

Due to the large simulation model and the limited size of each page allowed, most components are linked from the main page to their own sub-page. The phase-shifting transformers within the magnetic circuit are shown in Fig. A.10, the Fast Fourier Transform frequency analysis is shown in Fig. A.11, and the result graph pages are all linked to their own sub-pages.

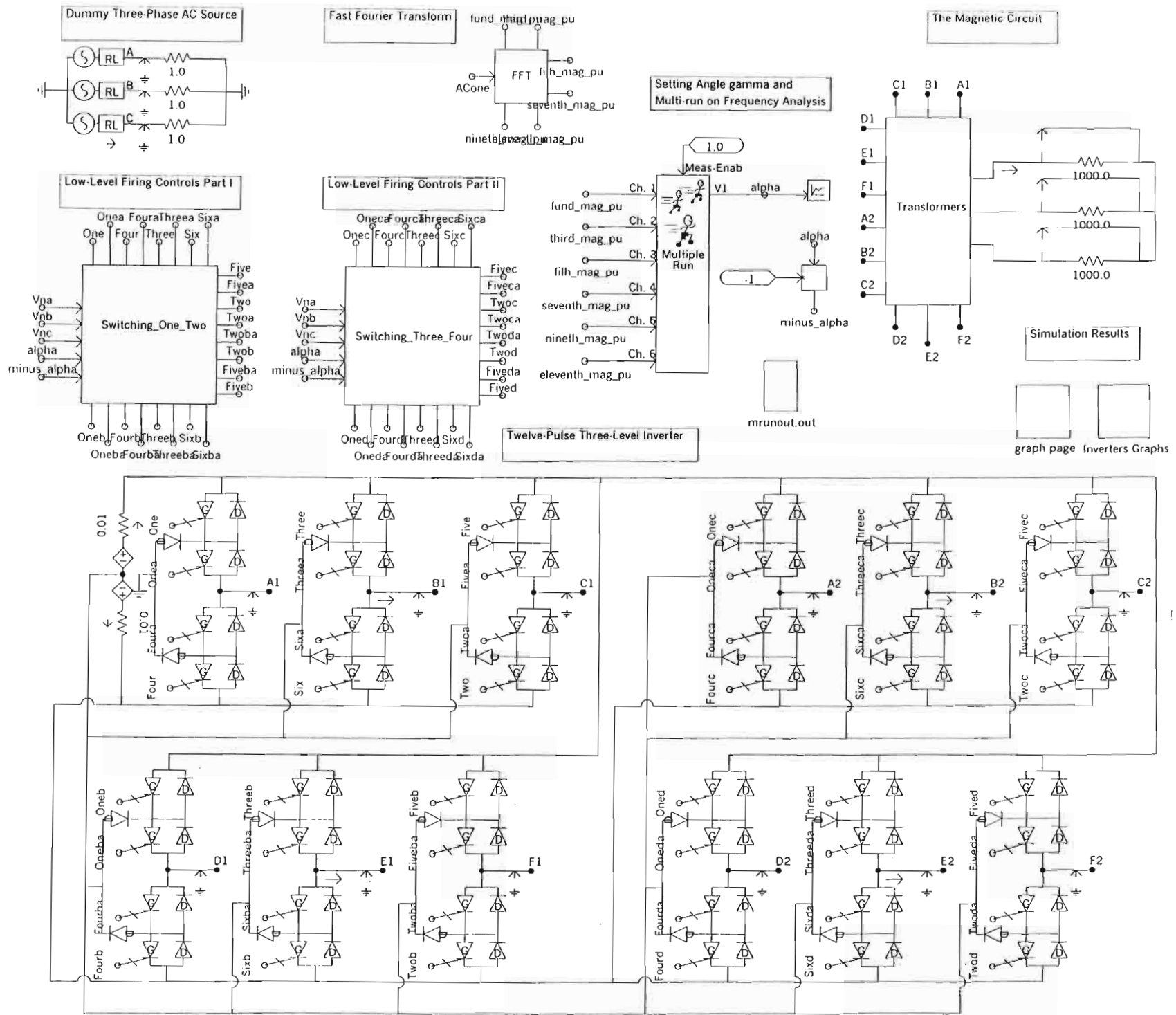


Fig. A-7: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter.

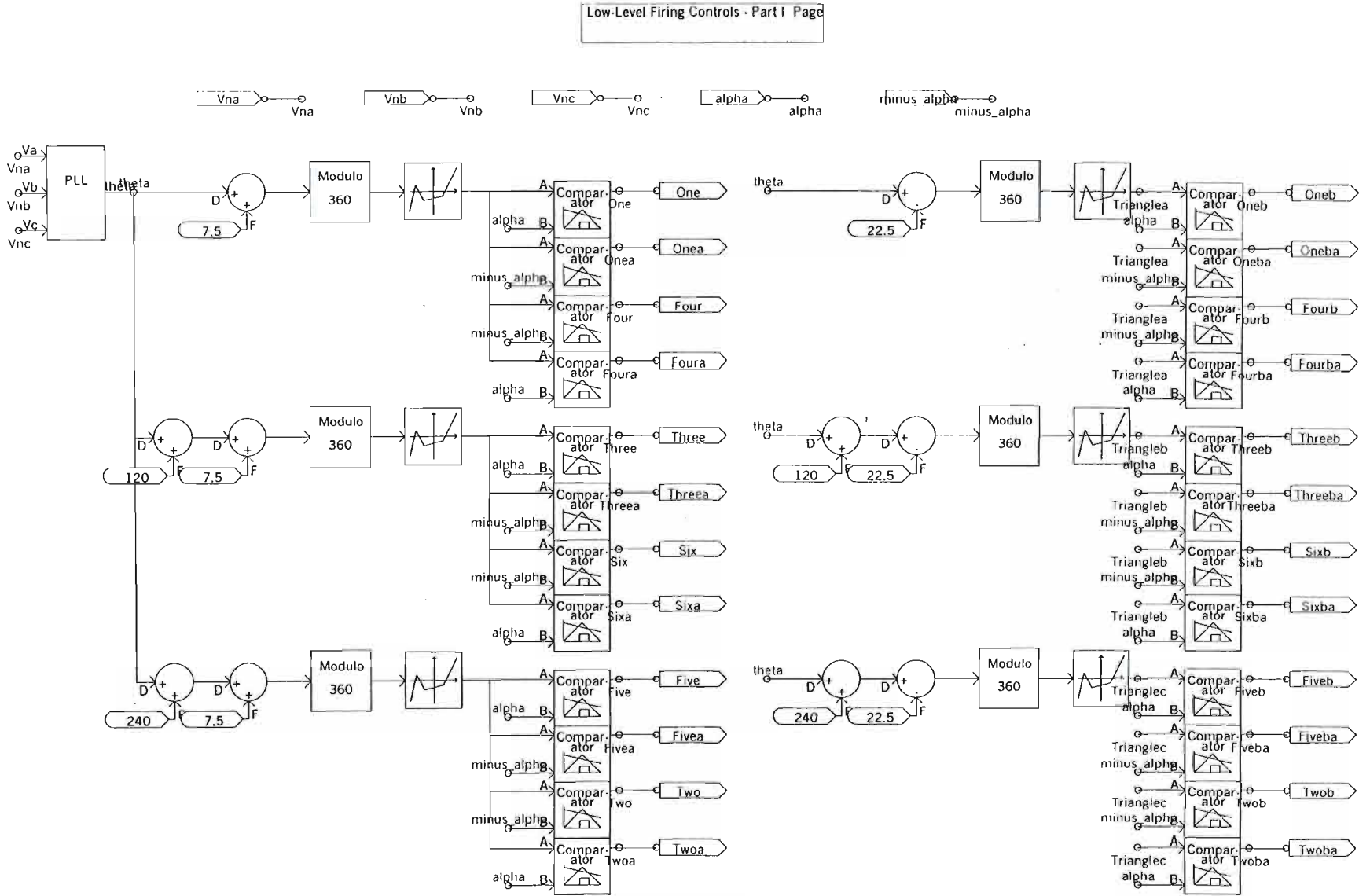


Fig. A.8: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter low-level firing controls - Part I (sub-page module Switching_One_Two).

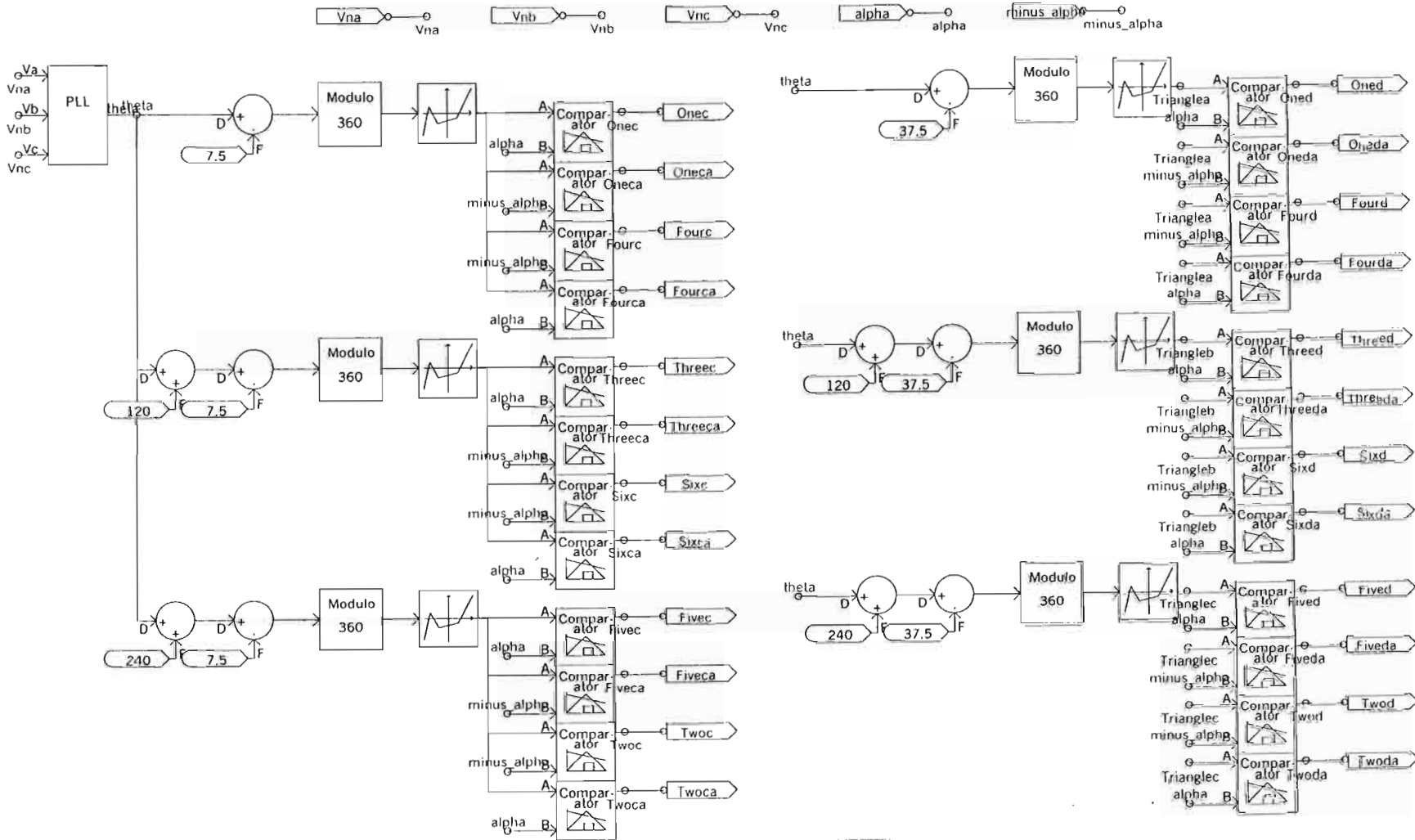


Fig. A.9: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter low-level firing controls - Part II (sub-page module Switching_Three_Four).

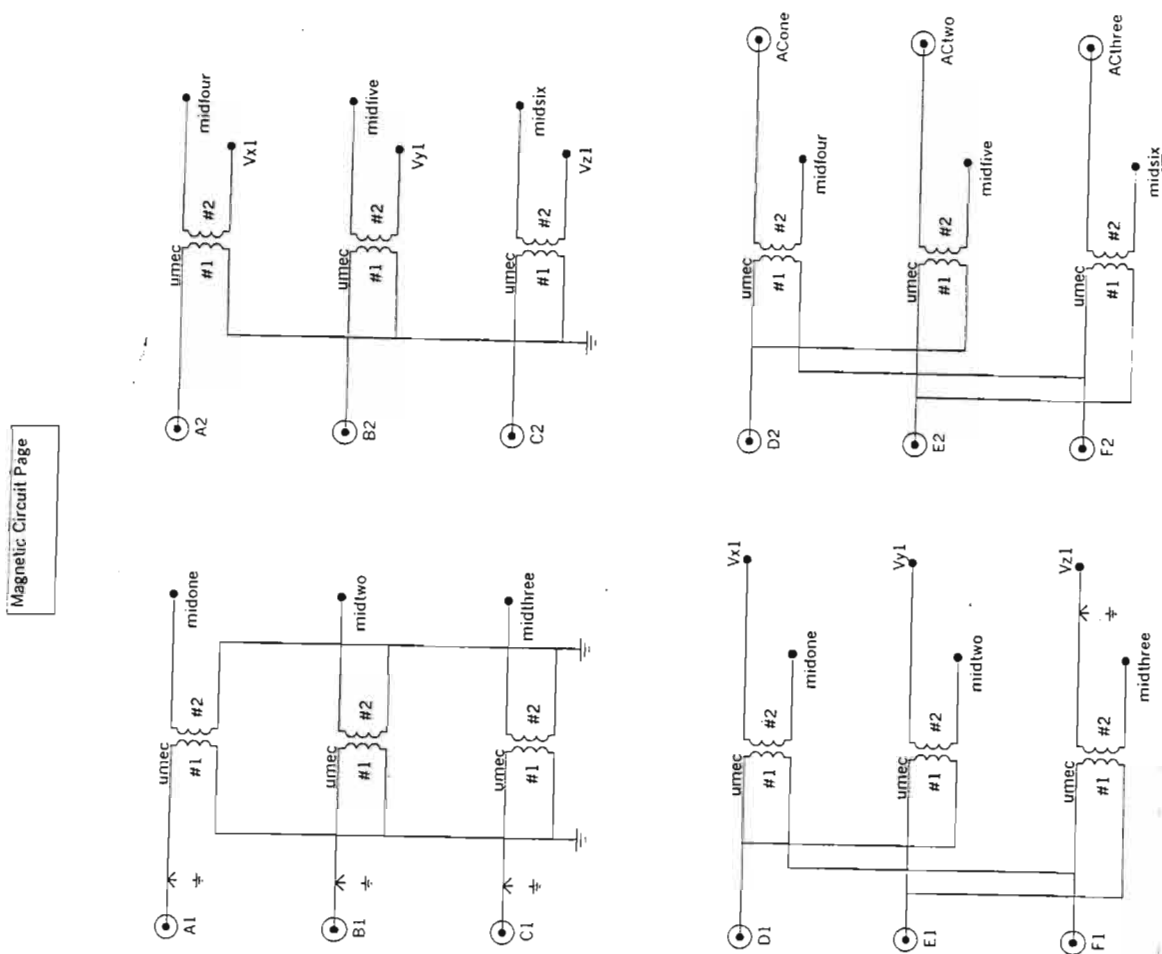


Fig. A.10: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter magnetic circuit (sub-page module Transformers).

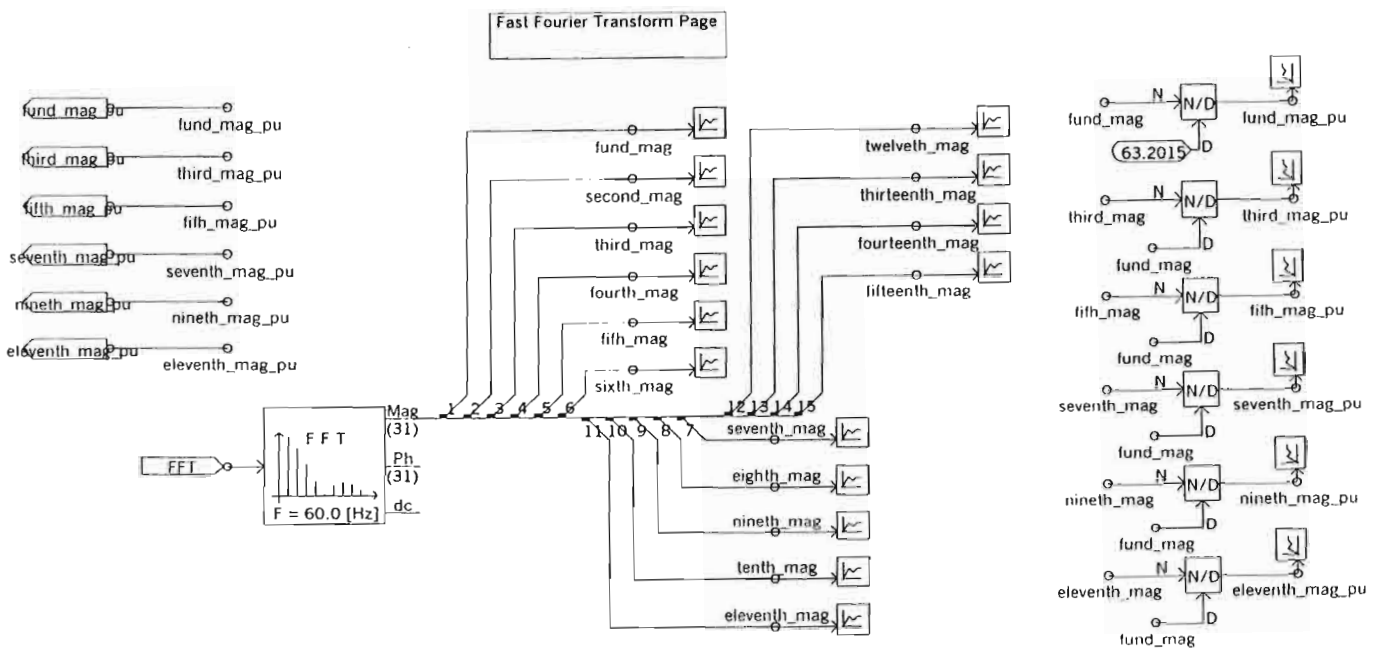


Fig. A.11: The frequency analysis of the 24-pulse three-level inverter model in PSCAD/EMTDC (sub-page module FFT).

APPENDIX B

PARAMETERS OF THE SSSC COMPENSATED TRANSMISSION SYSTEM AND ITS PSCAD/EMTDC MODELLING

This Appendix lists the parameters used in the study of the 24-pulse two-level inverter based SSSC in a series compensated transmission line as carried out in Chapter Three. The system is based on that in reference [34]. The Appendix also provides the details of the PSCAD/EMTDC modeling of the system developed in this thesis.

B.1 Parameters Of The SSSC Compensated Transmission System In Per-Unit Based on [34]

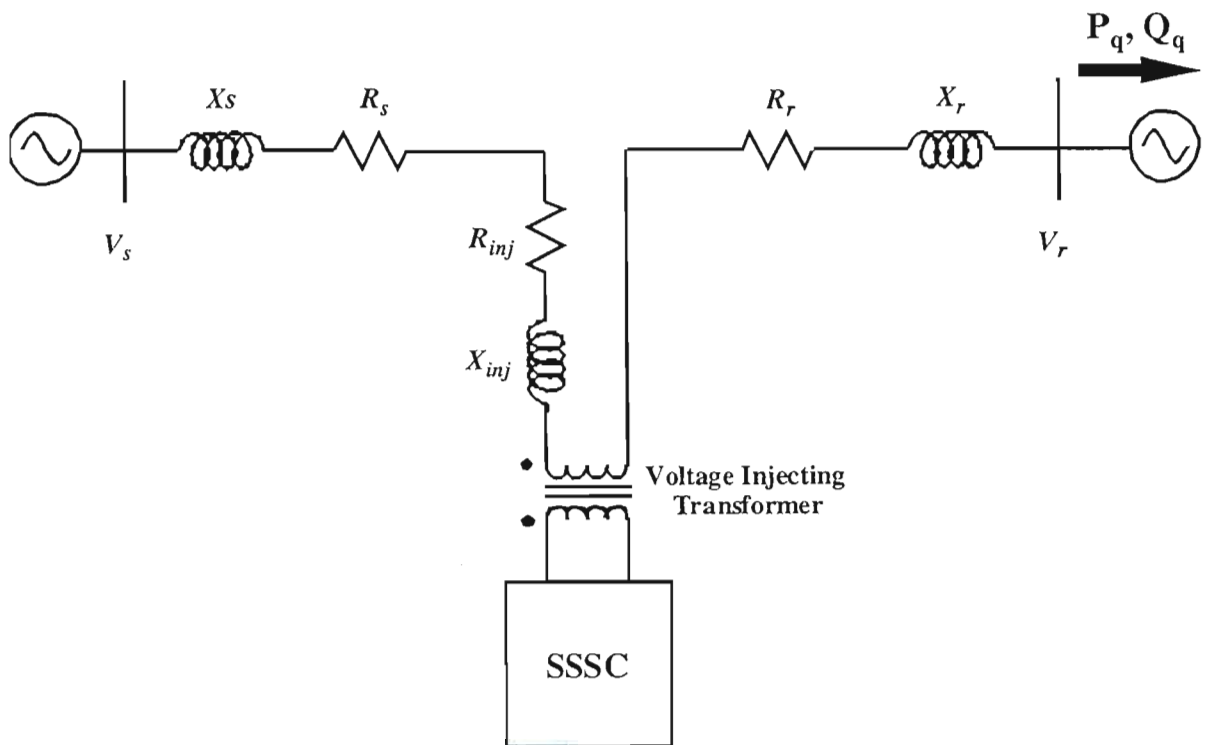


Fig.B.1: Simplified Diagram of the SSSC Compensated Transmission Line [34].

Fig. B.1 shows a simplified diagram (similar to that shown in Fig. 3.1 in Chapter Three) of the SSSC compensated transmission system based on [34]. The transmission system includes a sending-end voltage source V_s , a receiving-end voltage V_r , and inductive reactances X_s and X_r , as well as the series voltage-injecting transformer between the line and the SSSC. The following lists the parameters of the voltage sources on either end of the transmission line, the line and transformer impedances as well as the variables within the SSSC itself.

B.1.1 Per-Unit Base

Base voltage (phase to neutral) = 112 676.528 V = 112.676528 kV

Base current = 946.662704 A

Base impedance = 119.0250 Ω per phase

B.1.2 Transmission Line

Sending End:

$$V_s = 1 \angle 0^\circ \text{ pu}$$

$$R_s = 0.00845 \text{ pu}$$

$$X_s = 0.06249 \text{ pu}$$

Receiving End:

$$V_s = 1 \angle -30^\circ \text{ pu}$$

$$R_s = 0.02534 \text{ pu}$$

$$X_s = 0.18747 \text{ pu}$$

Injection Transformer:

$$R_{inj} = 0.015 \text{ pu}$$

$$X_{inj} = 0.15 \text{ pu}$$

B.1.3 The SSSC

Voltage Sourced Inverter:

$$K_{INV} = 2/\pi$$

$$\text{DC Capacitance} = 42 \times 10^{-6} \text{ F} = 42 \text{ } \mu\text{F}$$

SSSC Controller Gains:

$$K_{\text{PLL}i} = 250000$$

$$K_{\text{PLL}p} = 100000$$

$$K_{\text{ise}V} = 100$$

$$K_{\text{pse}V} = 10$$

B.2 PSCAD/EMTDC Representation Of The SSSC Based on [34]

Fig. B.2 shows a graphical representation of the SSSC simulation model developed for the work in this thesis. The SSSC compensated transmission system is the same as that shown in Fig. 3.1 in Chapter Three. The output compensating voltage from the SSSC is inserted into the line via the three-phase voltage-injecting transformer, which is built up from individual single-phase transformer models provided in PSCAD/EMTDC. Fig. B.2 also includes five different desired compensating reactances X_q^* for the purpose of comparing the dynamic operation of the SSSC to that predicted in [34].

Fig. B.3 shows a graphical representation of the 24-pulse three-level inverter simulation model developed. This part of the work has been described in detail in Appendix A.5. As before, due to the large simulation model and the limited size of each page allowed, most components are linked from the main page to their own sub-page. Fig. B.4 and Fig B.5 show the low-level firing control scheme for the 24-pulse inverter, and the magnetic circuit topology that comprises phase-shifting transformers is shown in Fig. B.6.

The high-level SSSC controls are shown in Fig. B.7; these are the detailed implementation of the scheme in Fig. 3.2 of Chapter Three. The phase locked loop, rotating frame transformer and magnitude and angle calculator are implemented using basic mathematical functional blocks provided in PSCAD/EMTDC according to the equations described in Chapter Three. These main controls, together with the dc link voltage regulator, then output the correct phase angle into the low-level firing controls for the turn-off devices in the inverter.

It should again be noted that for the investigations of Chapter Three, the inverter dead angle γ is kept at 0° and hence the three-level inverter is operated as a two-level device throughout this particular study.

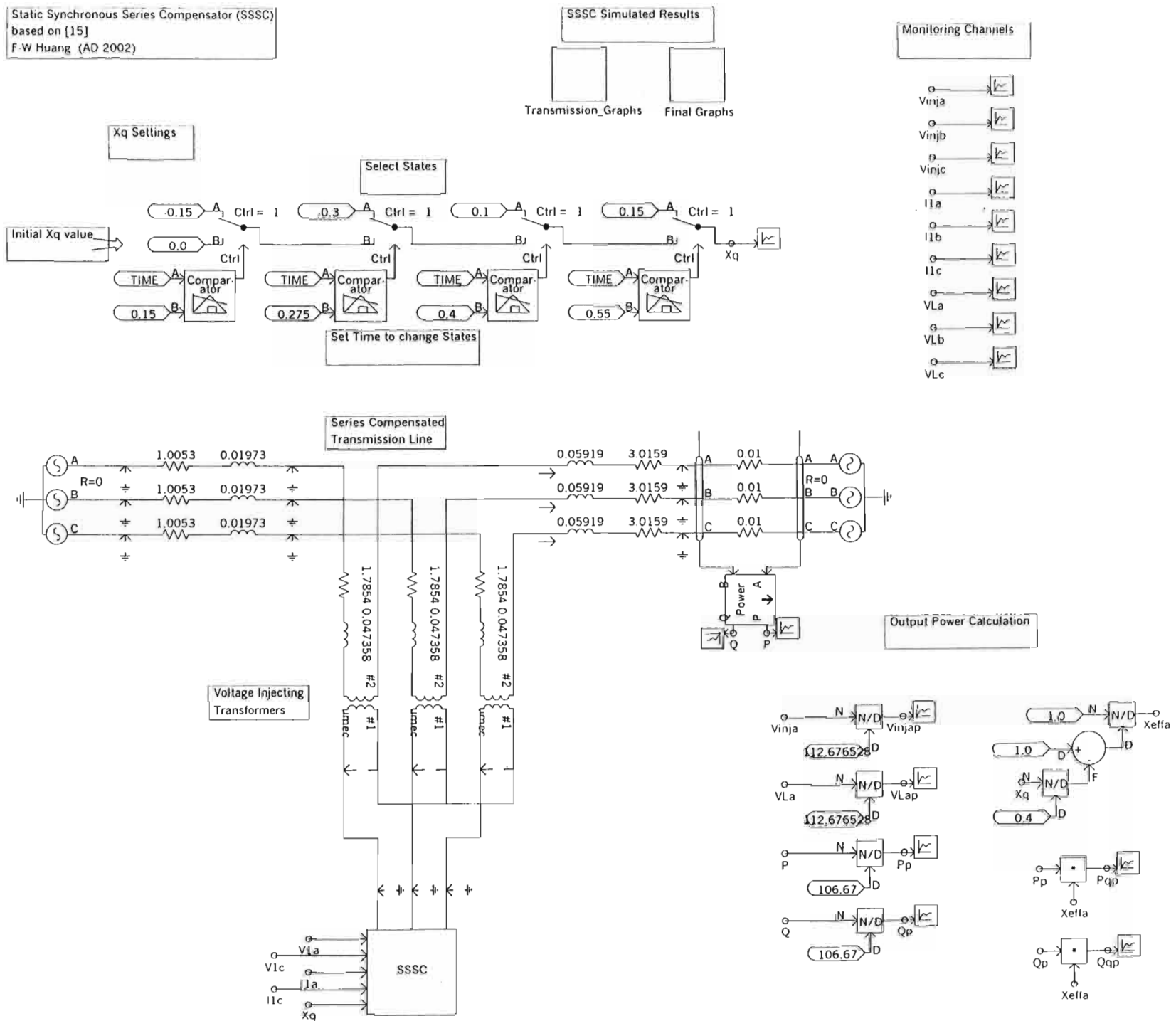


Fig. B.2: The SSSC compensated transmission line based on [34].

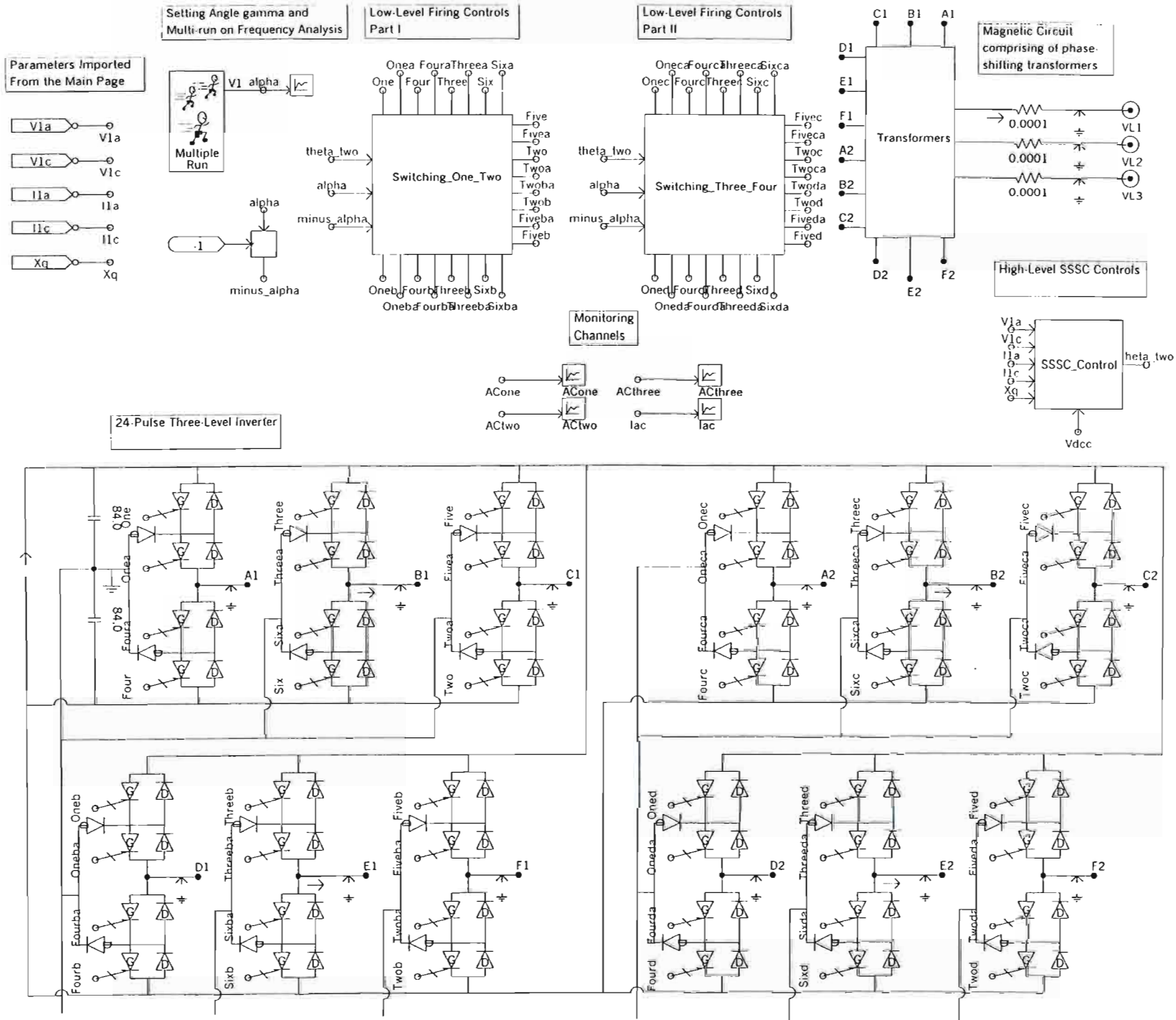


Fig. B.3: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter (sub-page module SSSC).

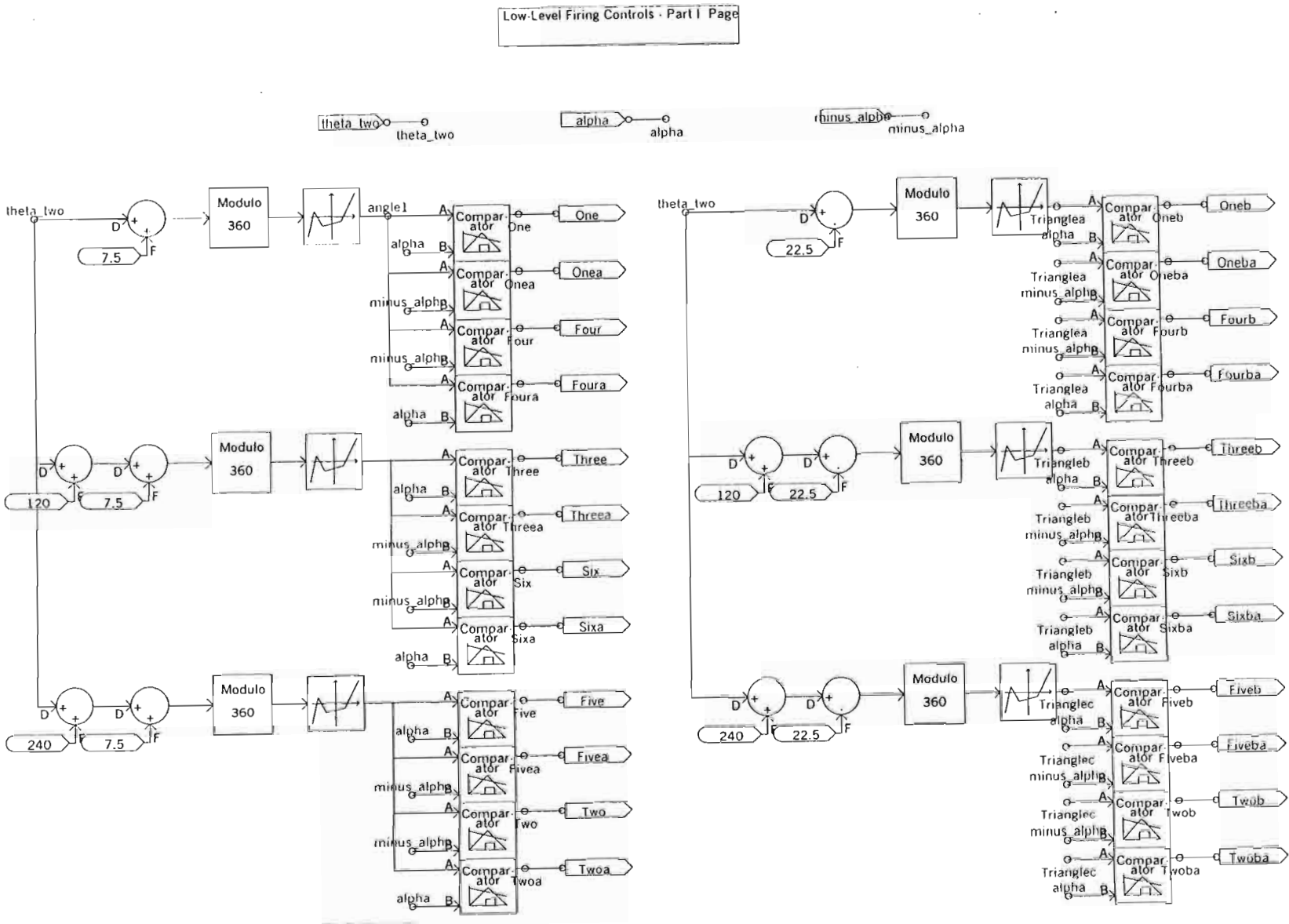


Fig. B.4: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter low-level firing controls - Part I (sub-page module Switching_One_Two).

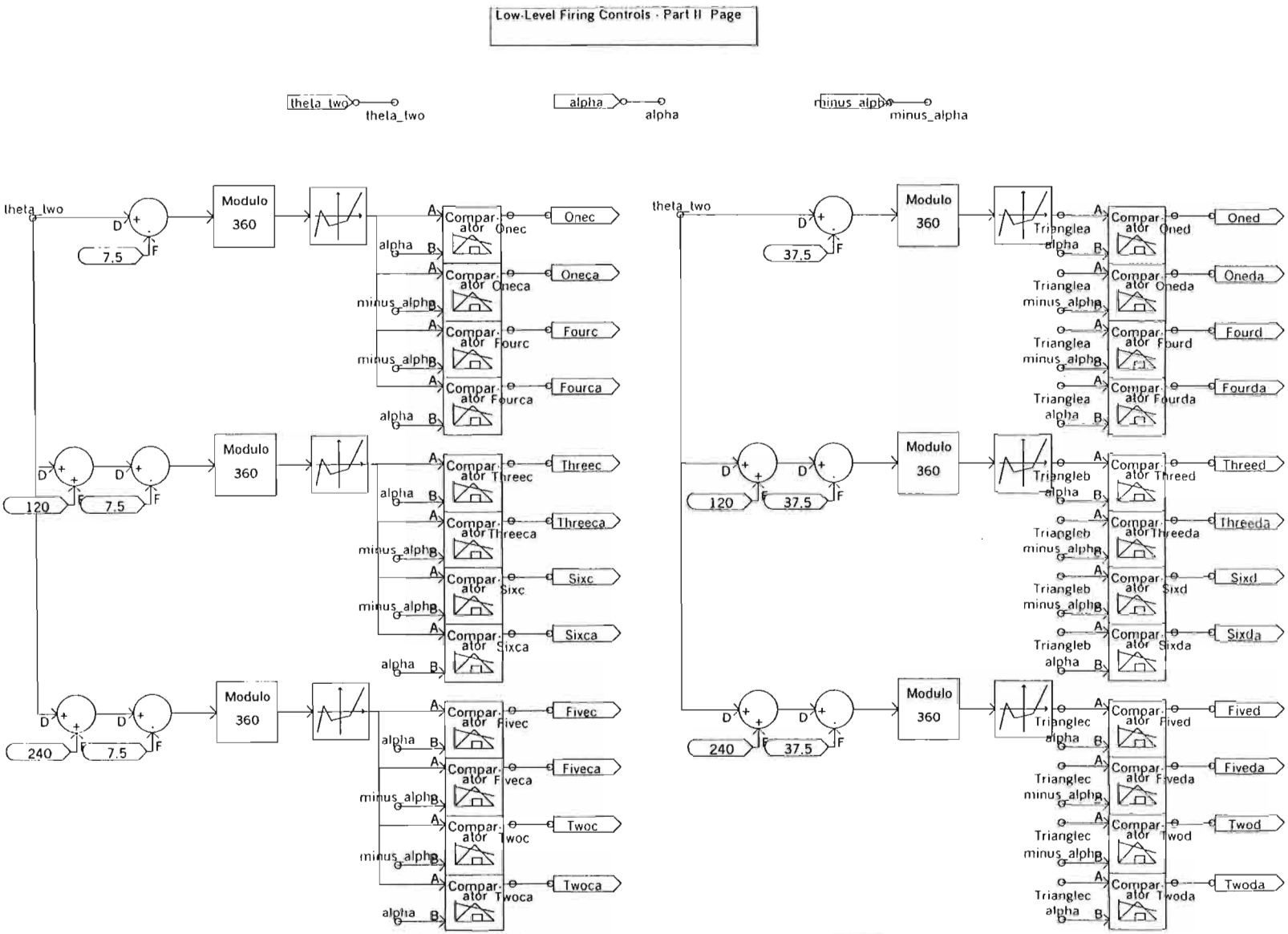


Fig. B.5: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter low-level firing controls - Part II (sub-page module Switching_Three_Four).

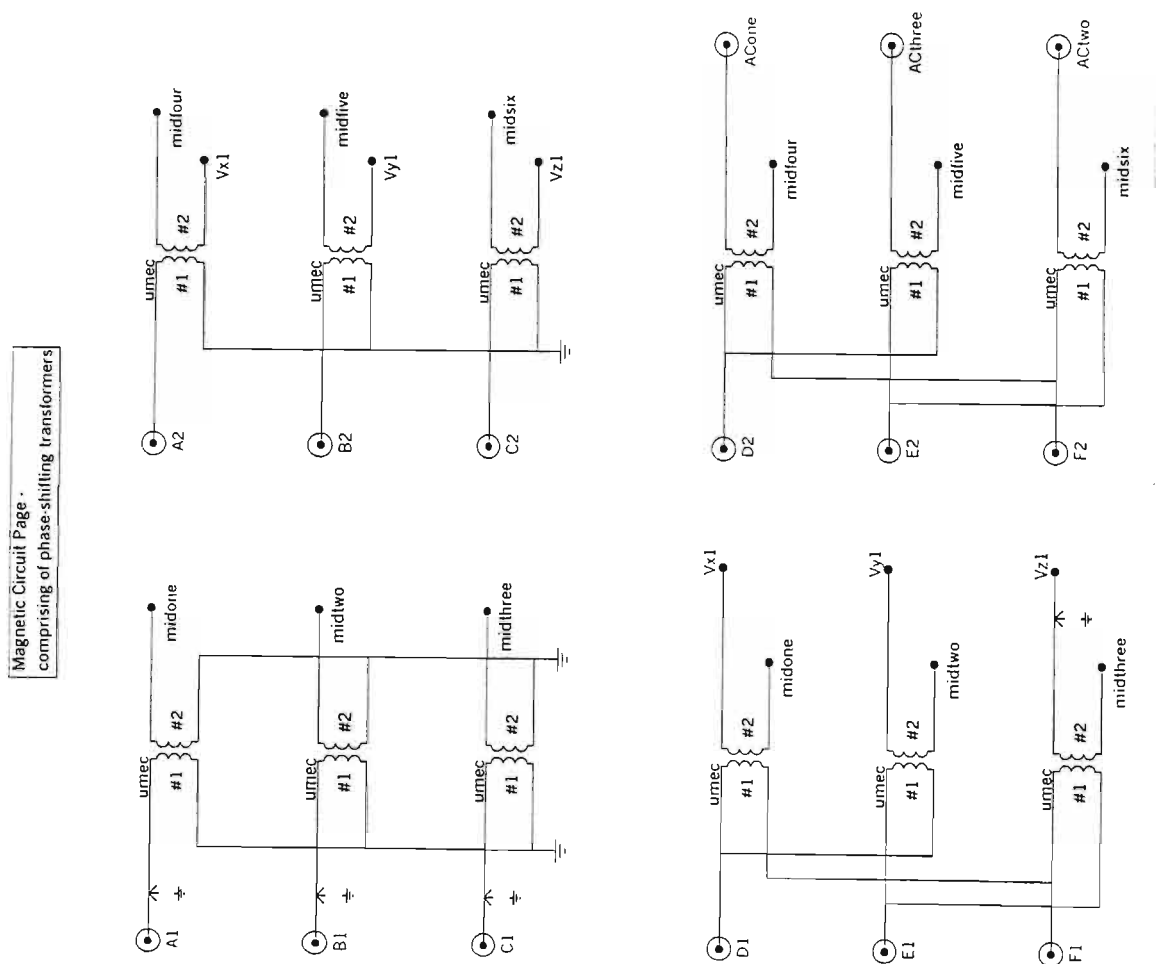


Fig. B.6: The detailed PSCAD/EMTDC representation of the 24-pulse three-level inverter magnetic circuit (sub-page module Transformers).

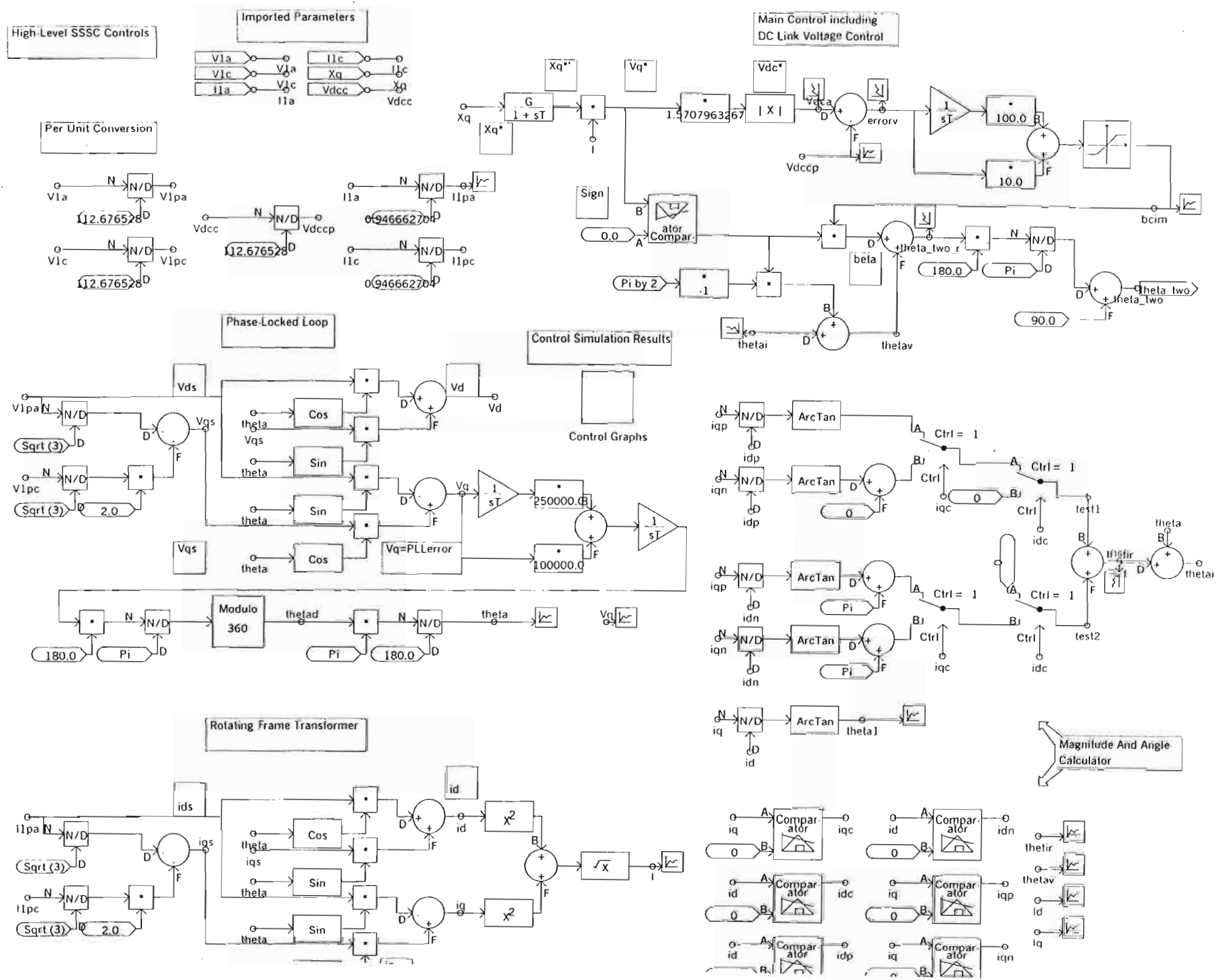


Fig. B.7: The detailed PSCAD/EMTDC representation of the SSSC high-level control (sub-page module SSSC_Control).

APPENDIX C

THE PSCAD/EMTDC MODELLING OF THE HIGH-LEVEL CONTROL WITHIN THE THREE-LEVEL SSSC

The system parameters used in the study of the 24-pulse three-level inverter-based SSSC in a series compensated transmission line as carried out in Chapter Three are the same as those used in the study of the 24-pulse two-level inverter-based SSSC in the same chapter. The sole changes from the two-level inverter-based SSSC and the three-level inverter-based SSSC lie within the high-level controller, where the output ac compensating voltage is now varied by adjusting the dead angle γ .

This appendix therefore provides the details of the PSCAD/EMTDC modeling of the high-level controller within the three-level SSSC. Fig. C.1 shows a graphical representation of the SSSC high-level control simulation model developed; this is the detailed implementation of the scheme in Fig. 3.11 of Chapter Three. The phase locked loop, rotating frame transformer and magnitude and angle calculator remain unchanged from that described in Appendix B. The change from the two-level SSSC lies in the main controls, where the desired magnitude of the ac compensating voltage is now the input of the dead angle calculator, and the input to the dc link voltage regulator is a set point reference determined by the operator. The high-level controller then outputs the correct phase angle θ_2 and the dead angle γ to the low-level firing controls for the turn-off devices in the inverter.

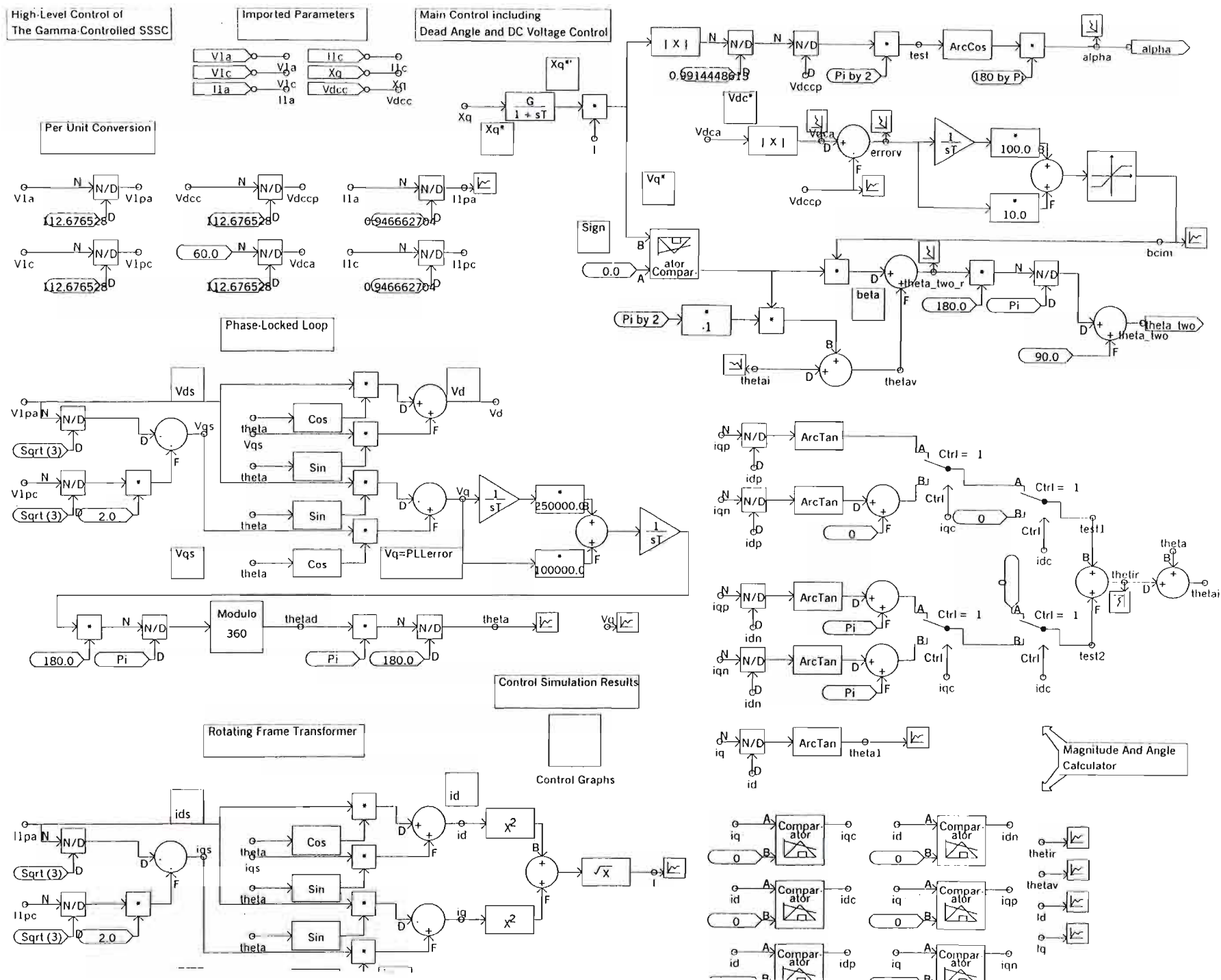


Fig. C.1: The detailed PSCAD/EMTDC representation of the three-level SSSC high-level control.

APPENDIX D

PARAMETERS OF THE STATCOM COMPENSATED

TRANSMISSION SYSTEM AND ITS PSCAD/EMTDC

MODELLING

This Appendix lists the parameters used in the study of the 24-pulse two-level inverter based STATCOM in a shunt compensated transmission line as carried out in Chapter Four. The system is based on that in reference [27]. The Appendix also provides the details of the PSCAD/EMTDC modeling of the system developed in this thesis.

D.1 Parameters Of The STATCOM Compensated Transmission System In Per-Unit Based on [27]

Fig. D.1 shows a simplified diagram (similar to that shown in Fig. 4.1 in Chapter Four) of the STATCOM compensated transmission system based on [27]. The transmission system includes a sending-end voltage source V_s , a receiving-end voltage V_r , and inductive reactances X_s and X_r , as well as the coupling transformer between the line and the STATCOM. The following lists the parameters of the voltage sources on either end of the transmission line, and transformer impedances as well as the variables within the STATCOM itself.

D.1.1 Per-Unit Base

Base voltage (phase to neutral) = 112 676.528 V = 112.676528 kV

Base current = 946.662704 A

Base impedance = 119.0250 Ω per phase

D.1.2 Transmission Line

Sending End:

$$V_s = 1 \angle 0^\circ \text{ pu}$$

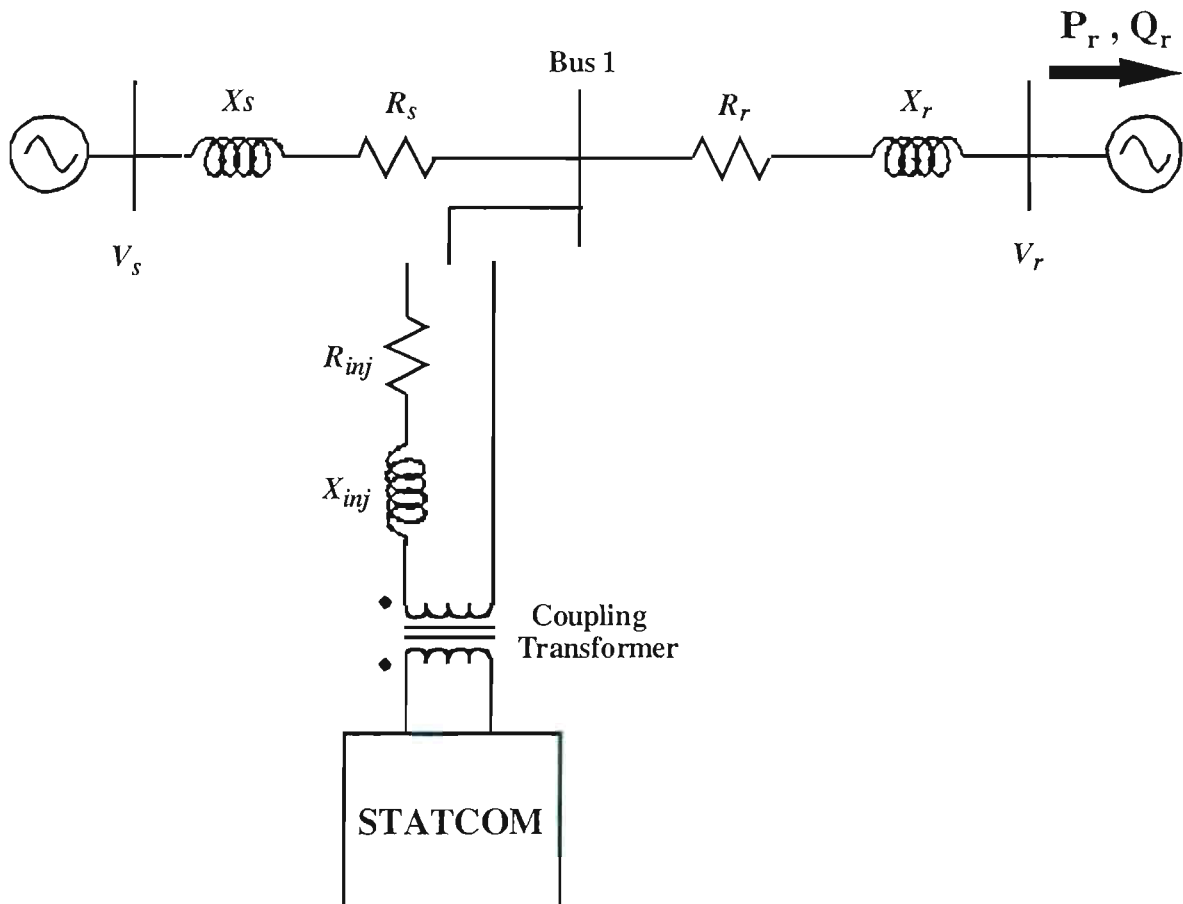


Fig.D.1: Simplified diagram of the STATCOM compensated transmission line [27].

$$R_s = 0.00845 \text{ pu}$$

$$X_s = 0.06249 \text{ pu}$$

Receiving End:

$$V_r = 1 \angle -30^\circ \text{ pu}$$

$$R_r = 0.02534 \text{ pu}$$

$$X_r = 0.18747 \text{ pu}$$

Injection Transformer:

$$R_{inj} = 0.015 \text{ pu}$$

$$X_{inj} = 0.15 \text{ pu}$$

D.1.3 The STATCOM

Voltage Sourced Inverter:

$$K_{INV} = 2/\pi$$

$$\text{DC Capacitance} = 42 \times 10^{-6} \text{ F} = 42 \text{ } \mu\text{F}$$

STATCOM Controller Gains:

$$K_{PLL_i} = 250000$$

$$K_{PLL_p} = 100000$$

$$K_{ishl} = 40$$

$$K_{pshl} = 0.45$$

D.2 PSCAD/EMTDC Representation Of The STATCOM Based on [27]

Fig. D.2 shows a graphical representation of the STATCOM simulation model developed for the work in this thesis. The STATCOM compensated transmission system is the same as that shown in Fig. 4.1 in Chapter Four. The shunt current from the STATCOM flows in and out of the line via the three-phase coupling transformer, which is constructed from individual single-phase transformer models provided in PSCAD/EMTDC. Fig. D.2 also includes three different desired quadrature component of the inverter current I_{iq}^* for the purpose of comparing the dynamic operation of the STATCOM to that predicted in [27].

The graphical representation of the 24-pulse three-level inverter simulation model, together with the low-level firing control scheme for the 24-pulse inverter, and the magnetic circuit topology that comprises phase-shifting transformers identical to that modeled for the SSSC in Chapter Three, and are shown in Fig. B.3, B.4, B.5 and B.6 in Appendix B.

The high-level STATCOM controls are shown in Fig. D.3; these are the detailed implementation of the scheme presented in Fig. 4.2 of Chapter Four. The phase locked loop and rotating frame transformer are implemented using basic mathematical functional blocks provided in PSCAD/EMTDC according to the equations described in Chapter Three. These main controls, together with the error amplifier (PI controller), then output the correct phase angle into the low-level firing controls for the turn-off devices in the inverter.

It should again be noted that for the investigations of STATCOM in Chapter Four, the inverter dead angle γ is kept at 0° and hence the three-level inverter is operated as a two-level device throughout this particular study.

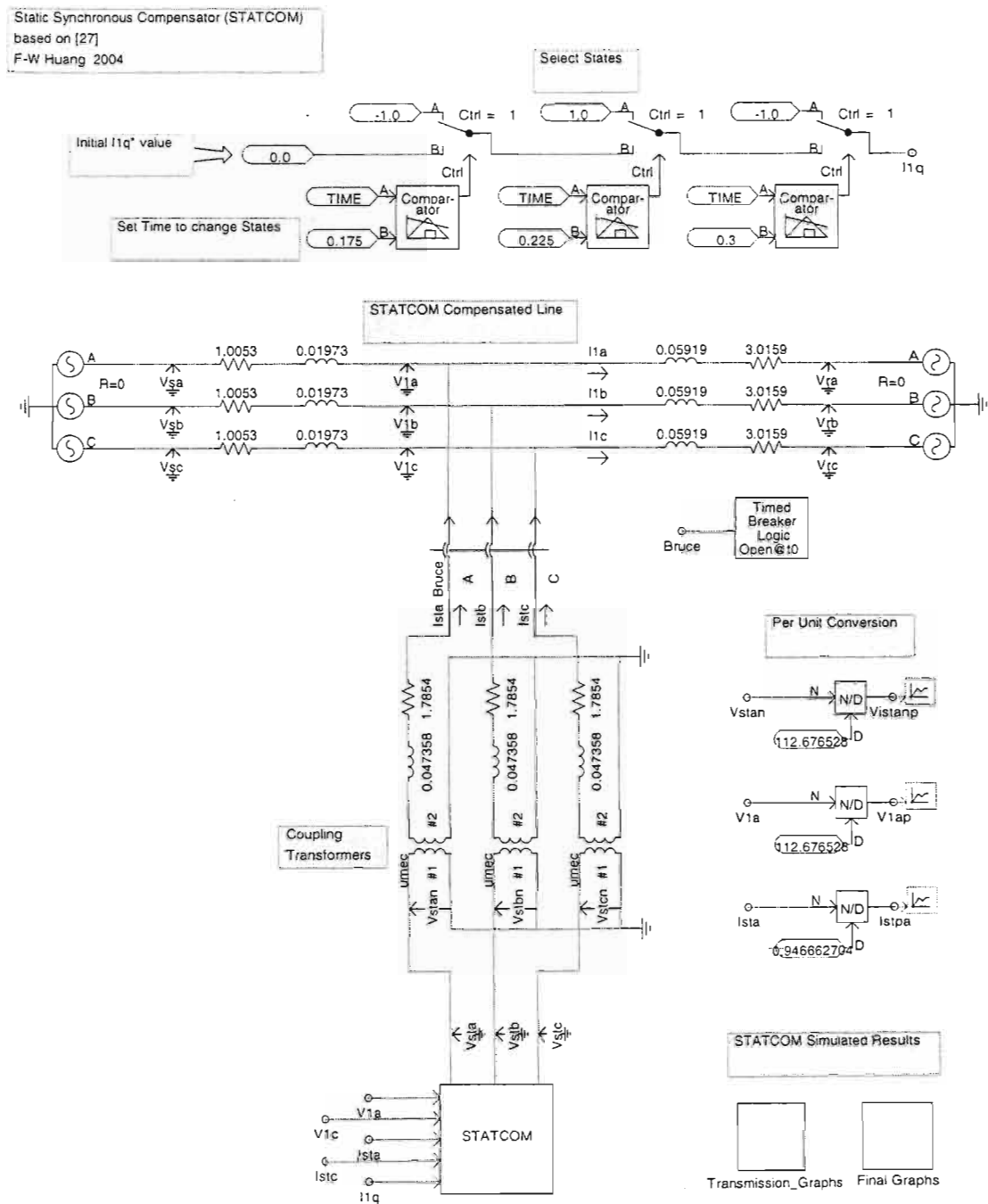


Fig. D.2: The STATCOM compensated transmission line based on [27].

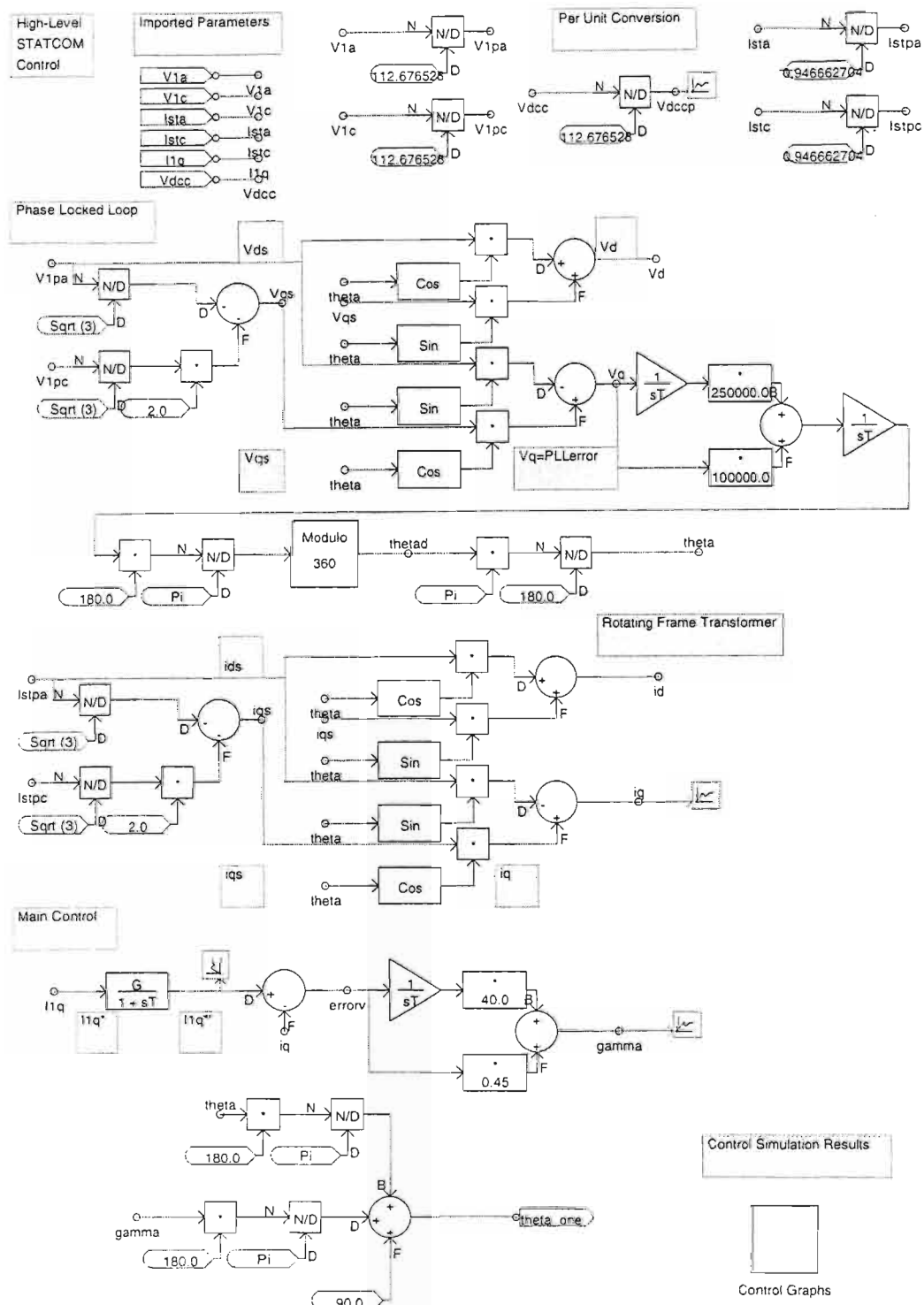


Fig. D.3: The detailed PSCAD/EMTDC representation of the STATCOM high-level control.

APPENDIX E

PARAMETERS OF THE UPFC COMPENSATED TRANSMISSION SYSTEM AND ITS PSCAD/EMTDC MODELLING

This Appendix lists the parameters used in the study of the 24-pulse three-level inverter based UPFC in a transmission line as carried out in Chapter Four. The system is based on that in reference [27]. The Appendix also provides the details of the PSCAD/EMTDC modeling of the system developed in this thesis.

E.1 Parameters Of The UPFC Compensated Transmission System In Per-Unit Based on [27]

Fig. E.1 shows a simplified diagram (similar to that shown in Fig. 4.7 in Chapter Four) of the UPFC compensated transmission system based on [27]. The transmission system includes a sending-end voltage source V_s , a receiving-end voltage V_r , and inductive reactances X_s and X_r , as well as the coupling transformers between the line and the UPFC. The following lists the parameters of the voltage sources on either end of the transmission line, and transformer impedances as well as the variables within the UPFC itself.

E.1.1 Per-Unit Base

Base voltage (phase to neutral) = 112 676.528 V = 112.676528 kV

Base current = 946.662704 A

Base impedance = 119.0250 Ω per phase

E.1.2 Transmission Line

Sending End:

$V_s = 1 \angle 0^\circ$ pu

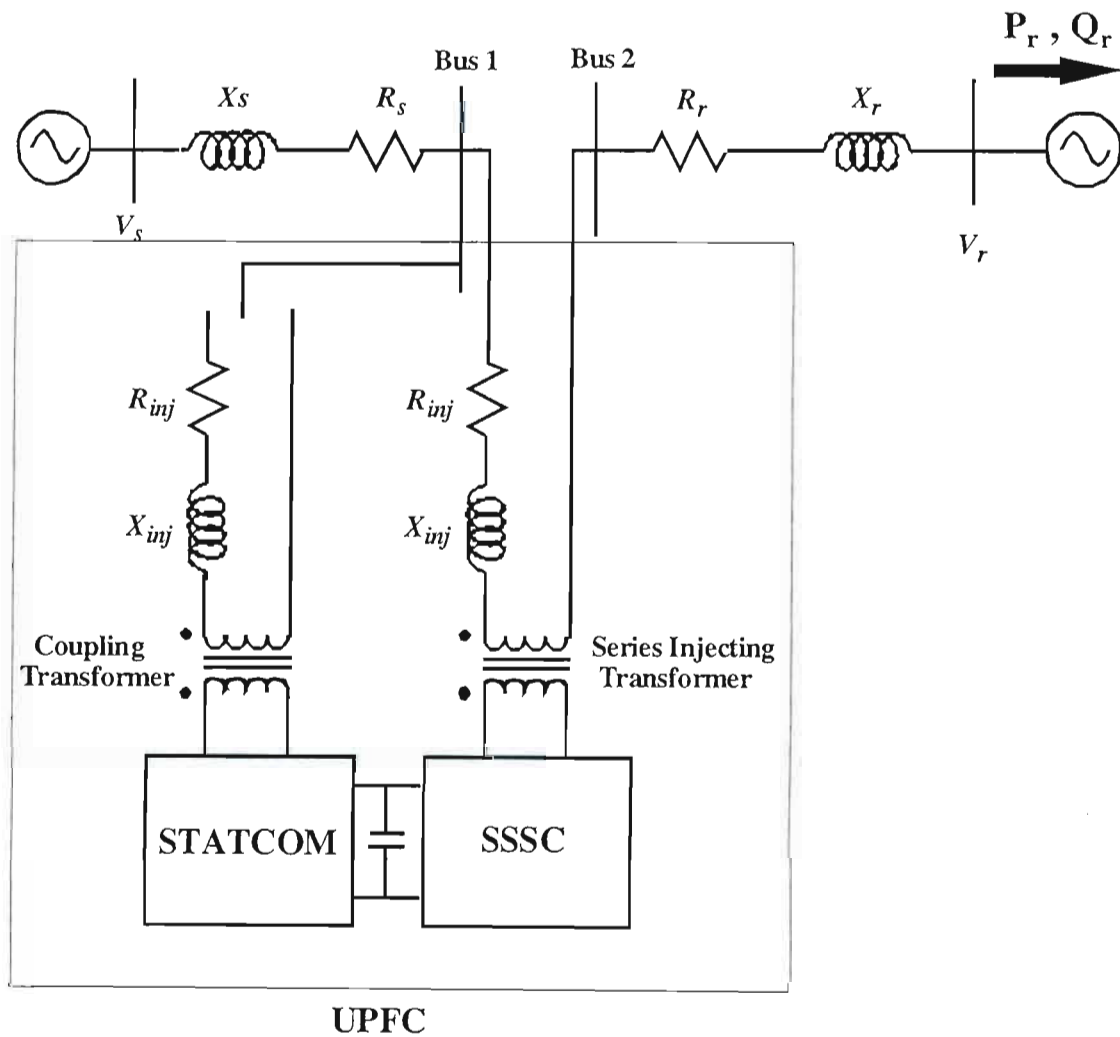


Fig.E.1: Simplified diagram of the UPFC compensated transmission line [27].

$$R_s = 0.00845 \text{ pu}$$

$$X_s = 0.06249 \text{ pu}$$

Receiving End:

$$V_r = 1 \angle -30^\circ \text{ pu}$$

$$R_r = 0.02534 \text{ pu}$$

$$X_r = 0.18747 \text{ pu}$$

Injection Transformer:

$$R_{inj} = 0.015 \text{ pu}$$

$$X_{inj} = 0.15 \text{ pu}$$

E.1.3 The UPFC

Voltage Sourced Inverters:

$$K_{INV} = 2/\pi$$

$$\text{DC Capacitance} = 42 \times 10^{-6} \text{ F} = 42 \mu\text{F}$$

UPFC Controller Gains:

$$K_{PLL_i} = 250000$$

$$K_{PLL_p} = 100000$$

$$K_{ishl} = 40$$

$$K_{pshl} = 0.45$$

E.2 PSCAD/EMTDC Representation Of The UPFC Based on [27]

Fig. E.2 shows a graphical representation of the UPFC simulation model developed for the work in this thesis. The UPFC compensated transmission system is the same as that shown in Fig. 4.7 in Chapter Four. The three-phase coupling transformers used in the UPFC modeling are built up from individual single-phase transformer models provided in PSCAD/EMTDC.

The graphical representation of the 24-pulse three-level inverter simulation model, together with the low-level firing control scheme for the 24-pulse inverter, and the magnetic circuit topology that comprises phase-shifting transformers identical to that modeled for the SSSC in Chapter Three, and are shown in Fig. B.3, B.4, B.5 and B.6 in Appendix B.

The high-level STATCOM controls stay the same as those shown in Fig. D.3 of Appendix D. The high-level SSSC controls are shown in Fig. E.3; these are the detailed implementation of the scheme presented in Fig. 4.8 of Chapter Four. Fig. E.3 also includes the step changes in the desired series inject voltage V_{dq}^* and relative angle β for the purpose of comparing the dynamic operation of the UPFC to that predicted in [27]. The dead angle calculator is implemented using basic mathematical functional blocks provided in PSCAD/EMTDC according to the equations described in Chapter Four. The phase angle θ is transported from the output of the phase locked loop in the STATCOM control. These main controls then output the correct phase angle and dead angle into the low-level firing controls for the turn-off devices in the inverter.

It should again be noted that for the investigations of STATCOM as a part of UPFC in Chapter Four, the inverter dead angle γ is kept at 0° and hence the three-level inverter is operated as a two-level device throughout this particular study.

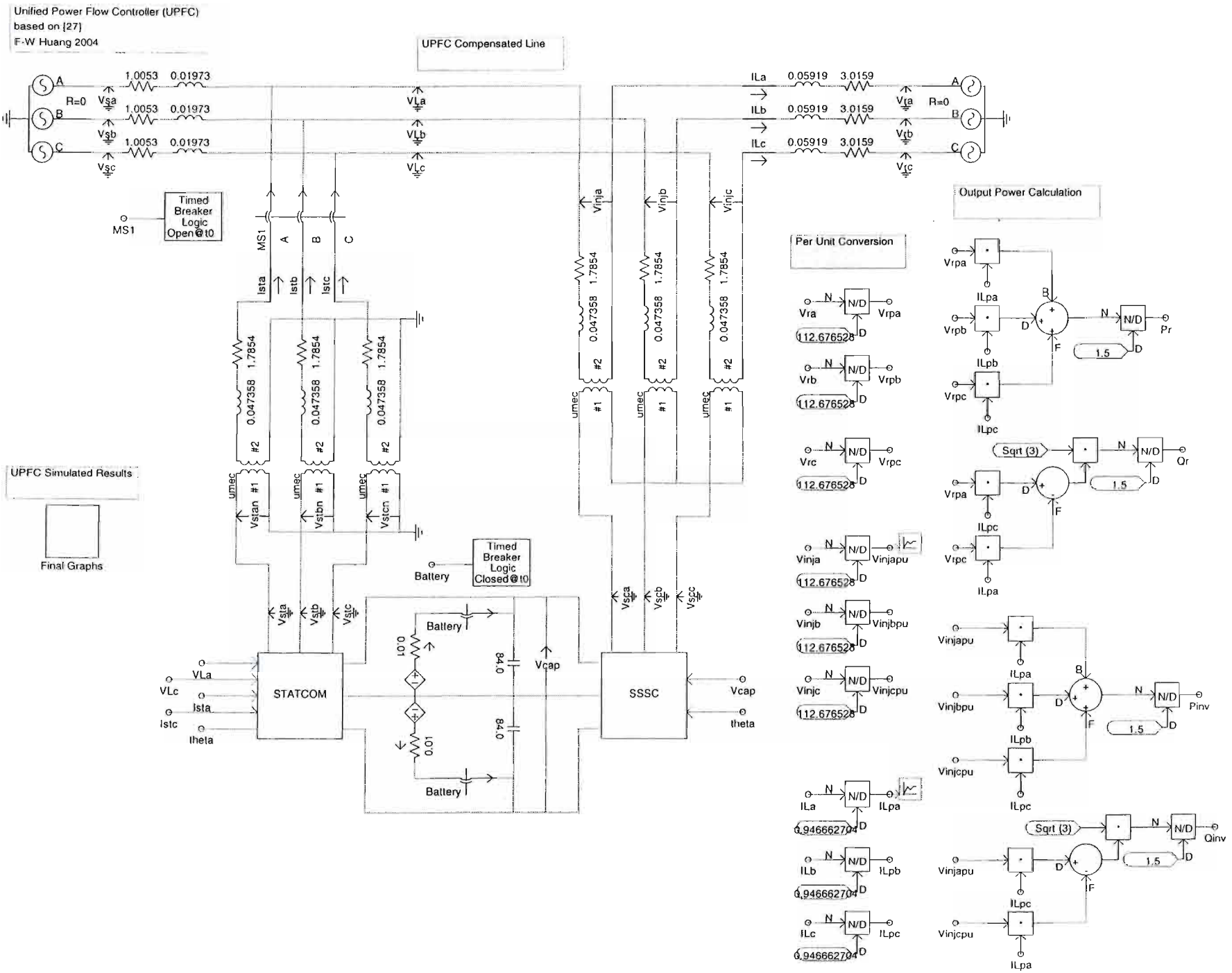


Fig. E.2: The UPFC compensated transmission line based on [27].

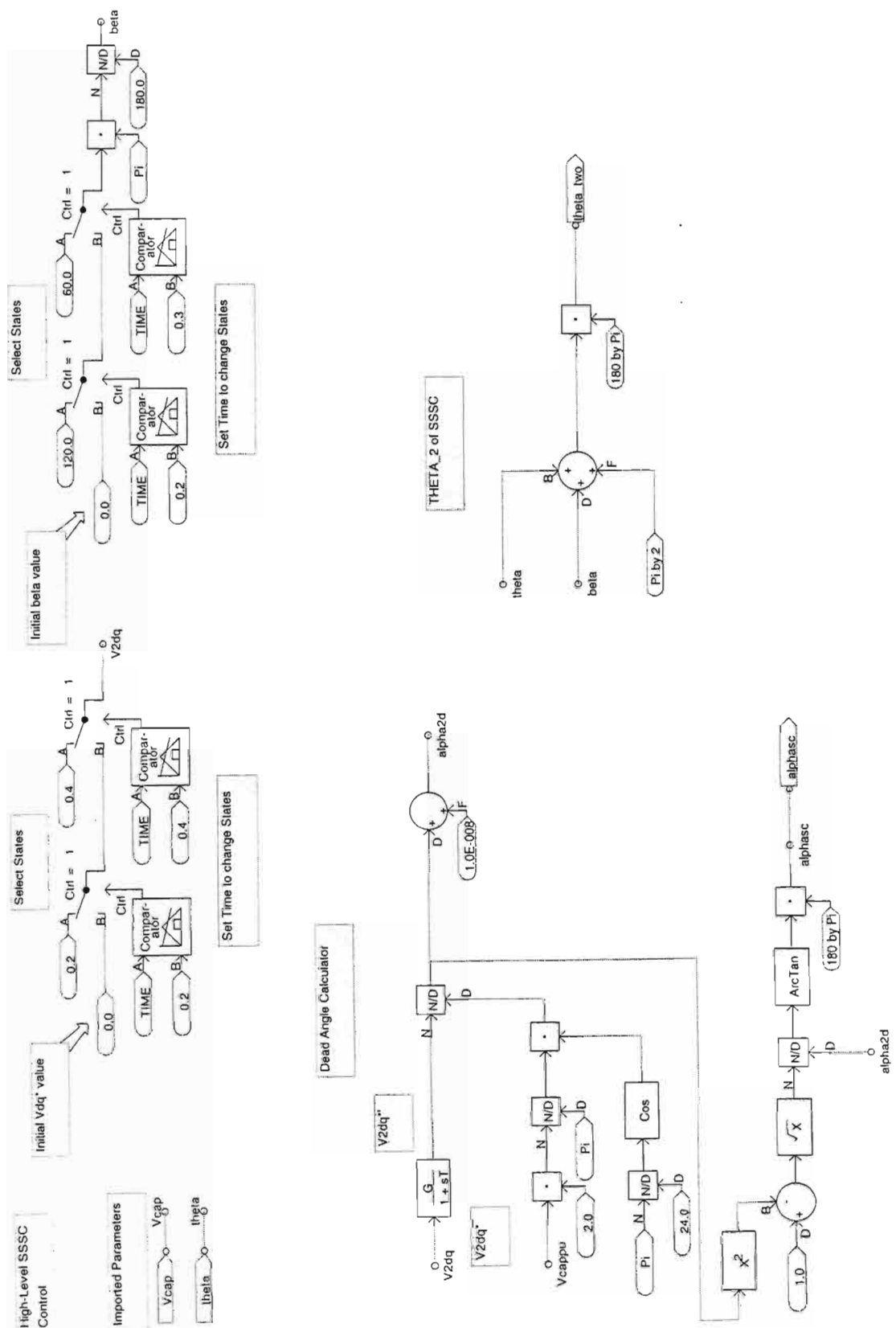


Fig. E.3: The detailed PSCAD/EMTDC representation of the SSSC high-level control.

APPENDIX F

CONTINUOUS-TIME INVERTER MODEL

IN PSCAD/EMTDC:

DESIGN AND RESONANT CHARACTERISTIC ANALYSIS

OF THE SSSC COMPENSATED TRANSMISSION LINE

F.1 Introduction

Chapter Five of the thesis described the development of a continuous-time inverter model in the simulation package PSCAD/EMTDC. The first part of this appendix describes in detail the various design steps required to develop this simplified inverter model. As an example, it also presents the graphical representation of the transmission system compensated by the simplified UPFC model as simulated in PSCAD/EMTDC.

Chapter Five also described simplified FACTS device models based on this continuous-time inverter model, one of which is the static synchronous series compensator (SSSC). The second part of this appendix examines this simplified SSSC model over a range of frequencies to determine whether or not it is able to predict the resonant characteristics of the SSSC that were shown using the detailed-model investigations in the thesis.

F.2 Design Of The Continuous-Time Inverter Model in PSCAD/EMTDC

In order to create a new component in the simulation package PSCAD/EMTDC, the visual graphics of the component and the necessary code have to be designed. The process of the design has been made simpler by the Component Wizard [80], the program within PSCAD/EMTDC that aids users to develop their own defined models.

By following the necessary steps using the Component Wizard, the graphics of the user-defined

component can be created. This initial phase of the design enables users to set up the required input, output and electrical nodes of the new component that will be connected to the rest of the elements in the simulation. The type of input or output variables, e.g. real, integer etc., are also defined in this section.

Fig. F.1 shows the component icon graphics of the continuous-time inverter model developed in PSCAD (i.e. the PSCAD implementation of the diagram shown in Fig. 5.2 in Chapter Five). A_p , A_n , B_p , B_n , C_p , and C_n are three-phase voltage source's electrical connections; dcp and dcn are the electrical nodes for the dc capacitor. Phase angle (θ) and dead angle (α) are defined as input data nodes. Current injection, I_{dc} , active power, P , and dc capacitor voltage, V_{capp} , are defined as output data nodes.

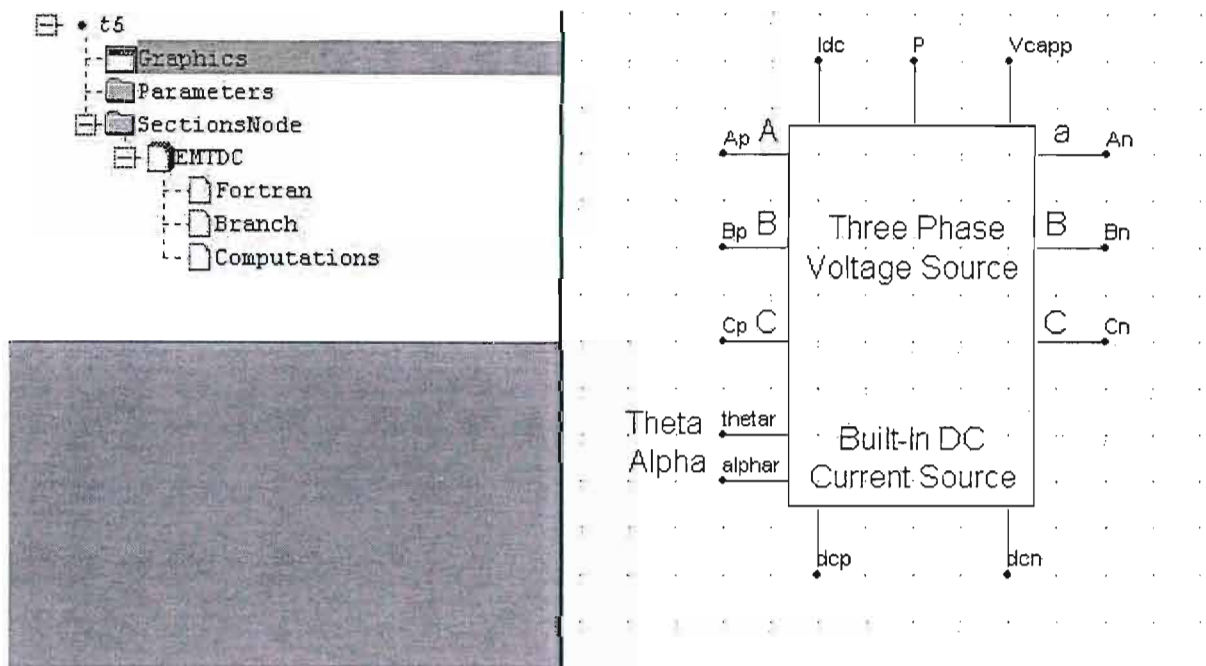


Fig. F.1: The graphics of the continuous-time inverter model developed in PSCAD/EMTDC.

All necessary properties that lie within the user-defined component are divided into various sections shown on the left hand side of Fig. F.1. The Parameter section can be designed to allow users to enter any required parameters related to the functionality of the component. For the purpose of the continuous-time inverter model design, this section is left empty.

Sections under SectionsNode, as shown in Fig. F.1, contain all the necessary coding of the designed component. This is the part that interfaces with the EMTDC simulation engine where all the mathematical solutions are performed.

Because the parameters entered into the component are not always compatible with the actual programming code, the Computation section is used for any pre-processing calculations before entering the actual programming codes. In the continuous-time inverter model, the calculations done in the Computation section are shown as follows.

COMPUTATION

```
REAL    Vm      = 2/pi*cos(pi/24)
REAL    PS      = 2*pi/3
```

Vm is defined as a real data variable and is partially based on equation (5.1) in Chapter Five, as the calculation for the dead angle will only be done in the later section. PS is the 120° phase shift between phase voltages in radians.

The Branch section declares any electrical resistor, inductor, capacitor, source or switch branches within the component [80]. For the continuous-time inverter model, the three-phase voltage source needs to be declared and is shown in the following code.

BRANCH

```
AnAp= $an $ap SOURCE 0.01 0.0 0.0
BnBp= $bn $bp SOURCE 0.01 0.0 0.0
CnCp= $cn $cp SOURCE 0.01 0.0 0.0
```

The Fortran section can often be used to hold all the code needed for a user-defined model; however, for more complex and lengthy code, this section is used to pass the required parameters to a subroutine where the complex code is placed. In the continuous-time inverter model, the Fortran section is shown as follows.

FORTRAN

```
#STORAGE REAL:1
!   Passing all necessary parameters and variables to and from the subroutine
#SUBROUTINE Test11
    CALL Test11($AnAp,$BnBp,$CnCp,$SS,
    & VDC($dcp,$SS),VDC($dcn,$SS),Vcap,
    & VDC($an,$SS),VDC($ap,$SS),VDC($bn,$SS),VDC($bp,$SS),VDC($cn,$SS),
    & VDC($cp,$SS),CBR($AnAp,$SS),CBR($BnBp,$SS),CBR($CnCp,$SS),
    & $thetar,$PS,$Vm,$alphar)
!   Variable Declaration
```



```
#LOCAL REAL power
#LOCAL REAL pa
#LOCAL REAL pb
#LOCAL REAL pc
#LOCAL REAL Idc
! PROGRAM BEGINS
! Calculation of single phase current injection based on eqns (5.5) and (5.6)
    pa = (VDC($ap,$SS)-VDC($an,$SS))*(-1)*CBR($AnAp,$SS)
    pb = (VDC($bp,$SS)-VDC($bn,$SS))*(-1)*CBR($BnBp,$SS)
    pc = (VDC($cp,$SS)-VDC($cn,$SS))*(-1)*CBR($CnCp,$SS)
    power = pa + pb + pc
    Idc = power / (VDC($dcp,$SS)-VDC($dcn,$SS))
! Output desired variables
    $idc = Idc
    $P = power
    $Vcapp = Vcap
! Activating the current injection source
    IF (TIME .LE. 0.01) THEN
#IF dcp!=0 {      CCIN($dcp, $SS) = CCIN($dcp, $SS) + 0}
#IF dcn!=0 {      CCIN($dcn, $SS) = CCIN($dcn, $SS) - 0}
        ELSE
#IF dcp!=0 {      CCIN($dcp, $SS) = CCIN($dcp, $SS) + Idc}
#IF dcn!=0 {      CCIN($dcn, $SS) = CCIN($dcn, $SS) - Idc}
        ENDIF
        IF (TIMEZERO) THEN
#IF dcp!=0
            ENABCCIN($dcp,$SS) = .TRUE.
#ENDIF
#IF dcn!=0
            ENABCCIN($dcn,$SS) = .TRUE.
#ENDIF
        ENDIF
! PROGRAM ENDS
```

Some of the parameters and variables are passed from the Fortran section to the subroutine where the programming of a voltage source is placed. This completes the continuous-time inverter model design. The voltage source subroutine is shown below.

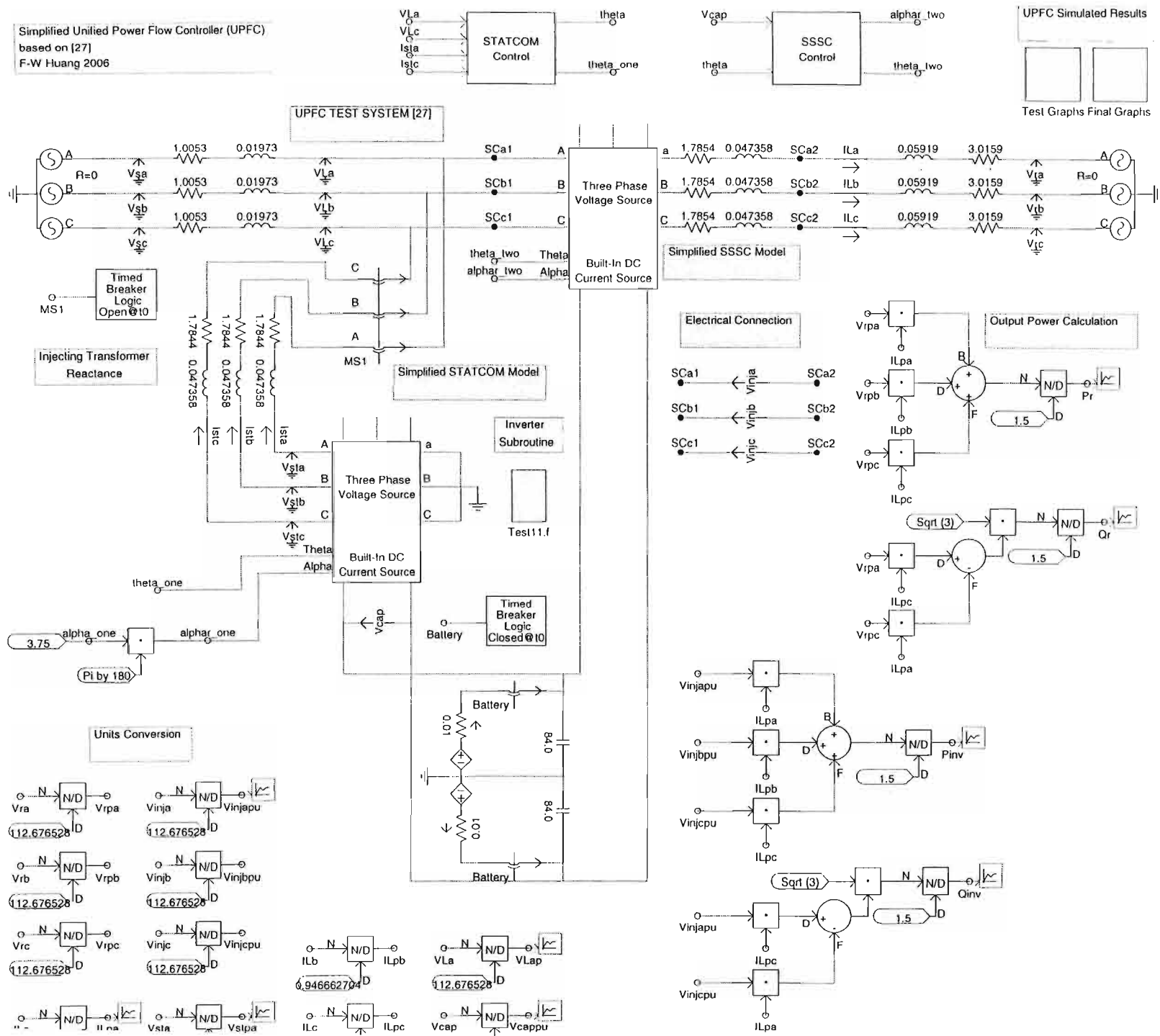
SUBROUTINE

```

!   Passing all necessary parameters and variables to and from Fortran section
SUBROUTINE Test11 (AnAp, BnBp, CnCp, SS,                                &
&                  vdcv, vdcn, vcap,                                &
&                  Van, Vap, Vbn, Vbp, Vcn, Vcp,                    &
&                  Ia, Ib, Ic,                                     &
&                  thetar, PS, Vm, alphas)
!   Global Variables
INCLUDE 'nd.h'
INCLUDE 's0.h'
INCLUDE 's1.h'
INCLUDE 's2.h'
INCLUDE 'branches.h'
!   Variable Declaration
REAL thetar, PS, Vm, alphas
REAL vcap, vdcv, vdcn
INTEGER AnAp, BnBp, CnCp, SS
!   PROGRAM BEGINS
!   Activate the source on branch ApAn
SOURCE(AnAp, SS) = .TRUE.
!   Activate the source on branch BpBn
SOURCE(BnBp, SS) = .TRUE.
!   Activate the source on branch CpCn
SOURCE(CnCp, SS) = .TRUE.
!   Calculate the dc capacitor voltage
vcap = vdcv - vdcn
!   Calculate the inverter's output ac voltage
EBR(AnAp, SS) = Vm*vcap*cos(alphas)*sin(thetar)
EBR(BnBp, SS) = Vm*vcap*cos(alphas)*sin(thetar-PS)
EBR(CnCp, SS) = Vm*vcap*cos(alphas)*sin(thetar+PS)
RETURN
END
!   PROGRAM ENDS

```

Fig. F.2 now shows a graphical representation of the UPFC simulation model developed using the simplified inverter model. The UPFC compensated transmission system is the same as that shown in Fig. 4.7 in Chapter Four.



F.3 The Impedance Versus Frequency Characteristics Of The Simplified SSSC Compensated Transmission Line

Chapter Six carried out a resonant study on a transmission line compensated by a two-level SSSC that was based on a detailed 24-pulse, three-level inverter. It was concluded that as effective as the SSSC is as a compensating device, it is not immune to SSR when operating in the capacitive mode as it, like conventional capacitors, causes a resonant minimum in the transmission line impedance at a subsynchronous natural frequency, at which frequency the line impedance is purely resistive, i.e. the SSSC acts as a capacitive reactance not only at the fundamental frequency but over the *entire* frequency spectrum.

However, this is in direct contradiction to the claim by various papers [16,17,26] in the past that have pointed out that SSSC cannot cause SSR because it injects voltages in series with the transmission line only at the fundamental frequency, it therefore *exhibits a theoretically zero impedance at all other frequencies*. It is therefore of interest to examine whether the simplified SSC model is able to predict the same resonant characteristics predicted by the detailed SSSC model in Chapter Six.

Therefore, in order to further test the suitability of the continuous-time inverter model, it was used to investigate the frequency-domain characteristics of an SSSC-compensated line using the same approach outlined in section 6.3.2 in Chapter Six. As shown in Fig. F.3, the results obtained using the continuous-time SSSC model are closely matched to those obtained using the detailed SSSC model at $X_q = 0.15$ pu. It is evident that at a subsynchronous frequency the line exhibits a resonant minimum in its impedance, and that the impedance at this frequency is small and purely resistive, irrespective of whether the SSSC model includes the detailed inverter switching. As the frequency increases, the line impedance shifts from inductive to capacitive as the phase of the impedance increases from -90° to $+90^\circ$.

These frequency-domain characteristics of the simplified SSSC-compensated transmission line shown in Fig. F.3 confirm the accuracy of the continuous-time simulation model and its suitability for studying subsynchronous network interactions.

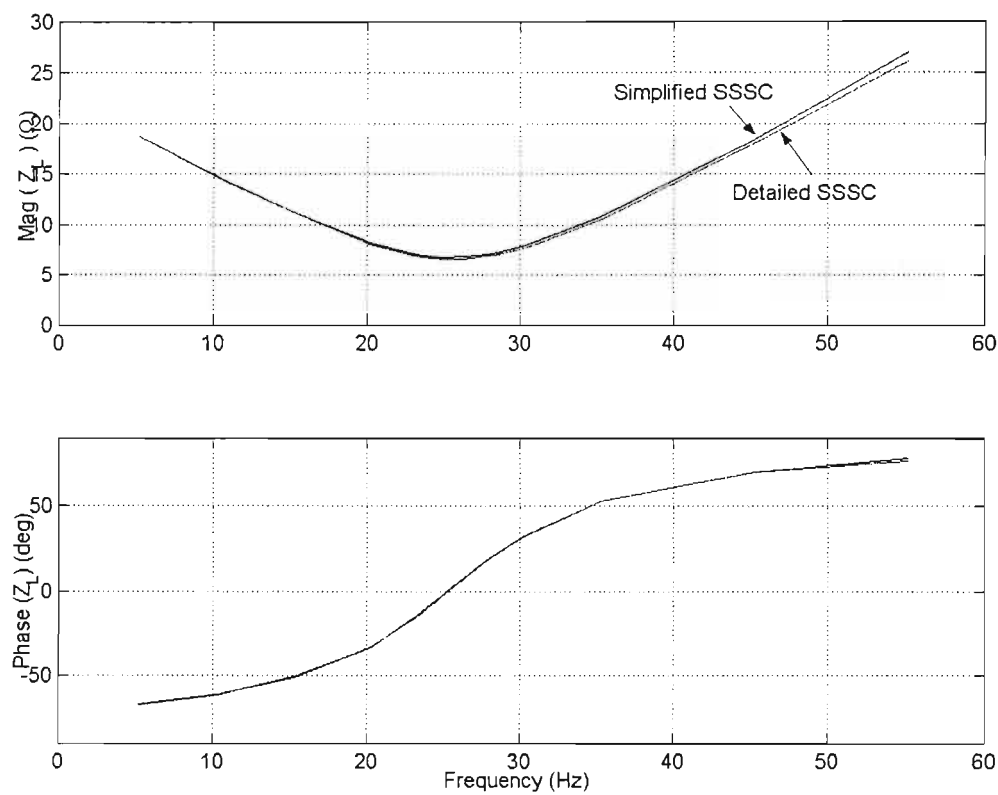


Fig. F.3: Magnitude and phase versus frequency of the total impedance of the detailed and simplified SSSC compensated transmission line at $X_q = 0.15$ pu.

APPENDIX G

THE PSCAD/EMTDC MODELS USED TO EXAMINE THE RESONANT CHARACTERISTIC OF THE SERIES COMPENSATED TRANSMISSION LINE

G.1 Introduction

Chapter Six of this thesis shows a series of simulation results to demonstrate the resonant impedance characteristics of the two-level SSSC and conventional capacitor compensated transmission line based on the IEEE First Benchmark Model [72] for the PSCAD/EMTDC simulation program. This appendix presents the simulation models used to investigate the transmission line impedance versus frequency characteristics, and the interaction between the series compensated (both by an SSSC and conventional capacitor) transmission line and the turbine-generator torsional shaft modes.

G.2 The Impedance Versus Frequency Characteristics Of The Series Compensated IEEE First Benchmark Model

Figs. G.1 and G.2 show a graphical representation of the simulation model developed for the work in this thesis. The conventional capacitor and SSSC compensated transmission system are both based on the IEEE First Benchmark Model, and the original network diagram is shown in Fig. 6.2 in Chapter Six. The existing case example of the IEEE First Benchmark Model in PSCAD/EMTDC is modified where the synchronous machine model is taken out and replaced by a grounded three-phase ac source, as the interest of this particular study is on the electrical resonance caused by the series compensating devices. Also, a small subsynchronous voltage source $V_{ss\ abc}$ of 5% of the sending-end voltage amplitude is inserted into each phase at the sending end of the transmission line where the frequency of the subsynchronous voltage $V_{ss\ abc}$ is set to some subsynchronous value ω_{ss} (i.e. $\omega_{ss} < \omega_0$) at which the impedance characteristics of the line are to be determined. The SSSC block shown in Fig. G.2 contains the two-level SSSC subpages shown in Appendix B.2.

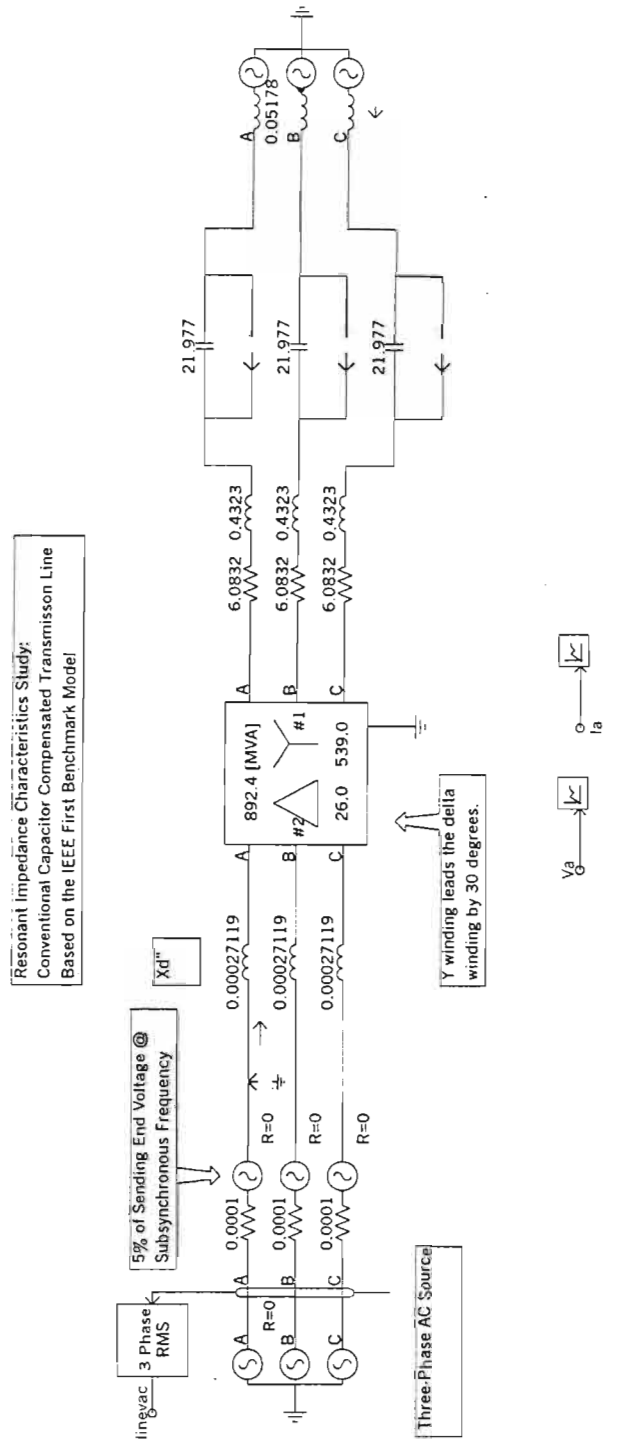


Fig. G.1: The conventional capacitor compensated First Benchmark Model transmission line used in the study of its resonant characteristic.

G.3 The IEEE First Benchmark Model Compensated With The SSSC And The Conventional Capacitors

Figs. G.3 and G.4 show a graphical representation of the IEEE First Benchmark simulation model developed for the work in this thesis. The three-phase ac sources used in the previous resonant impedance characteristic study are replaced by the original synchronous machine and machine shaft models in the IEEE First Benchmark Model. Also, the subsynchronous ac sources are removed. What is therefore presented in Fig. G.3 is the original IEEE First Benchmark Model transmission lines compensated with conventional capacitors. Fig. G.4 shows the replacement of these capacitors by the two-level SSSC. The SSSC block contains subpages of two-level SSSC shown in Appendix B.2.

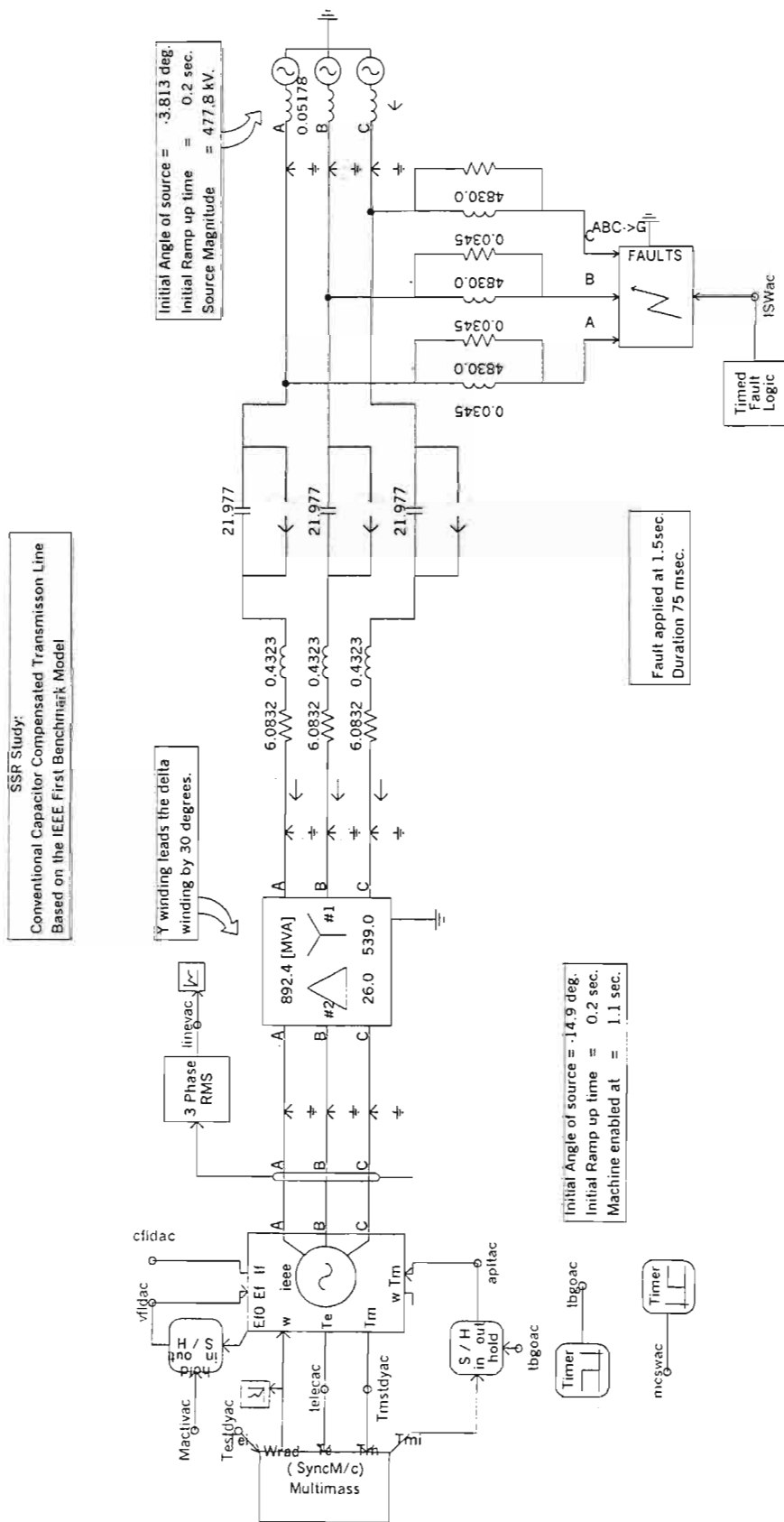


Fig. G.3: The original First Benchmark Model transmission lines compensated by the conventional capacitors in EMTDC used in the study of SSR.

APPENDIX H

LEAD COMPENSATOR DESIGN FOR THE SUPPLEMENTARY DAMPING CONTROLLER

H.1 Introduction

Chapter Seven of this thesis described the design procedure of a supplementary damping controller for the three-level SSSC. This appendix focuses on the design methodology of a lead compensator to counteract the phase lag between ΔX_q and ΔT_e , based on reference [85].

H.2 Lead Compensator Design

The supplementary controller is designed to damp out the Mode 4 frequency component of 32.285 Hz. The phase lag between ΔX_q and ΔT_e has been measured to be 41.8° . Therefore, 41.8° is needed by the lead compensator signal to correct the lagging angle.

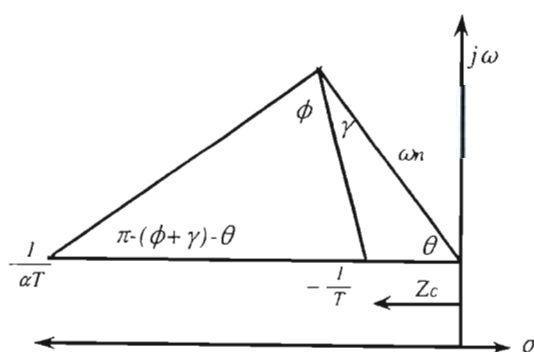


Fig. H.1: Determination of the pole and zero of a lead network [85].

The phase lead needed is $\phi = 41.8^\circ$

Assuming damping ratio of $\xi = 0.5$

then $\theta = \cos^{-1}(\xi) = \cos^{-1}(0.5) = 60^\circ$

based on Fig. H.1, for max k_v

$$\begin{aligned}\gamma &= \frac{1}{2}(\pi - \theta - \phi) \\ &= 39.1^\circ\end{aligned}$$

If $(\pi - \theta) > (\gamma + \phi)$, then the compensation angle can be achieved using a single lead network:

$$G_C(s) = \frac{s + Z_C}{s + P_C} = \frac{s + \frac{1}{T}}{s + \frac{1}{\alpha T}} = \alpha \frac{1 + sT}{1 + s\alpha T} \quad (\text{H.1})$$

From the above,

$$Z_c = \frac{\omega_n \sin(\gamma)}{\sin(\pi - \gamma - \theta)} = 129.5 \quad (\text{H.2})$$

$$P_c = \frac{\omega_n \sin(\phi + \gamma)}{\sin(\pi - \phi - \gamma - \theta)} = 317.7 \quad (\text{H.3})$$

Therefore, the lead network was determined:

$$G_c(s) = \frac{s + 129.5}{s + 317.7} = 0.4076 \frac{s + 0.0077}{s + 0.0031} \quad (\text{H.4})$$

The bode plot of such network is shown in Fig H.2.

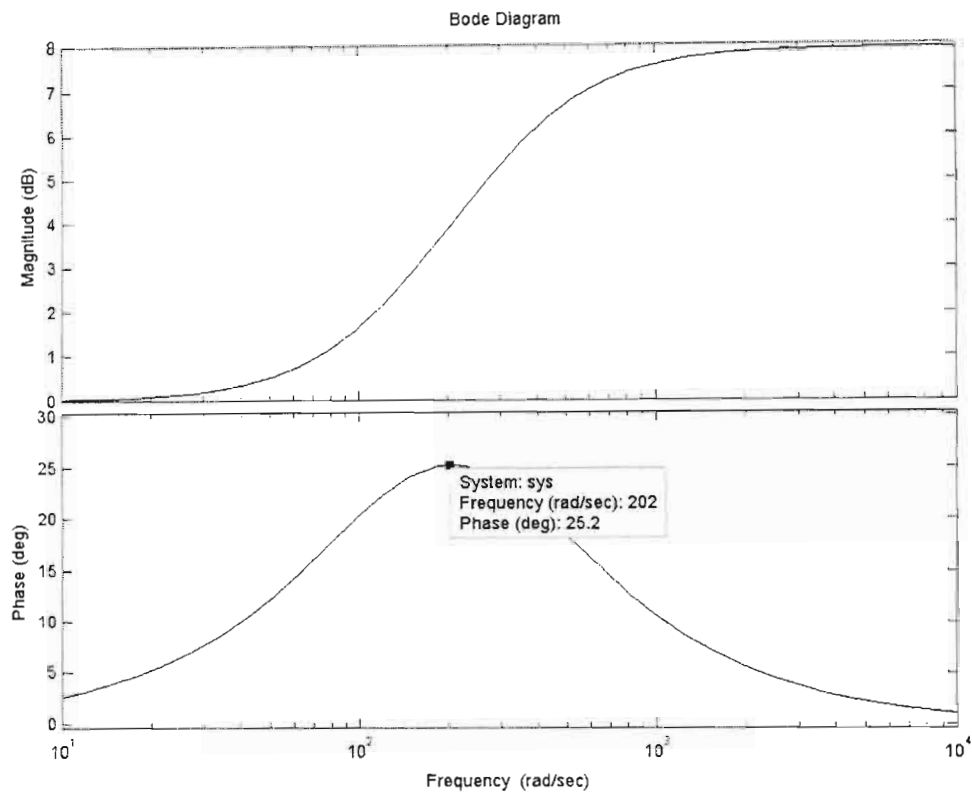


Fig. H.2: Bode plot based on the calculated poles and zeros.

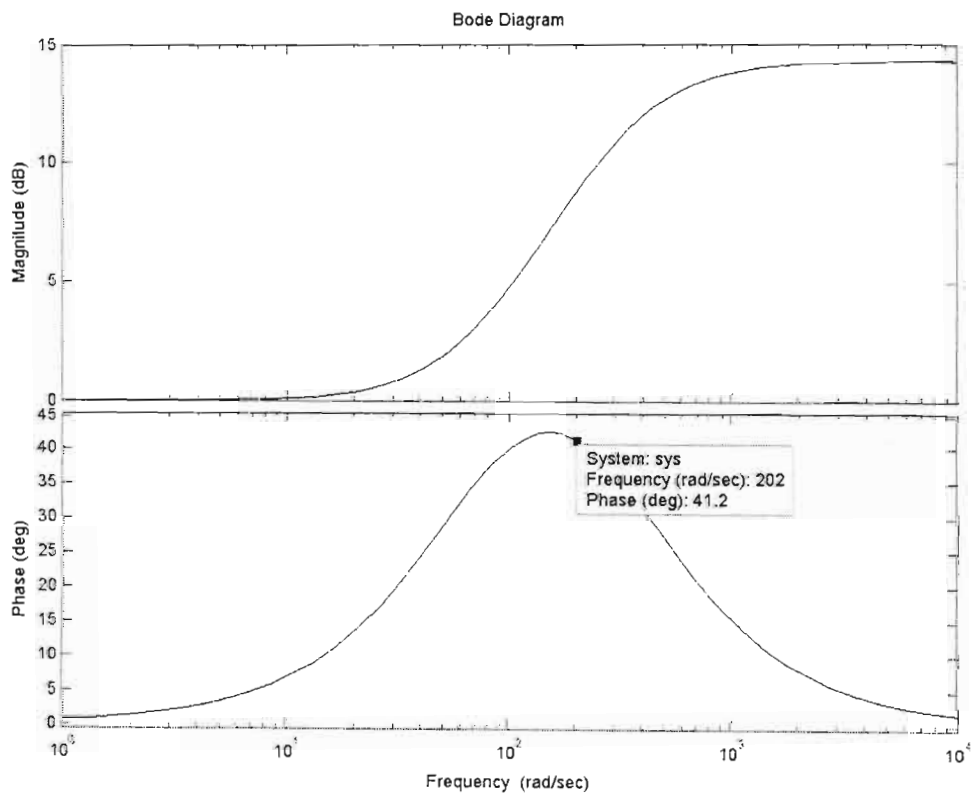


Fig. H.3: Bode plot based on the final poles and zeros used for the supplementary controller.

However, at the given frequency, the calculated poles and zeros of the lead compensator do not accurately counteract the required angle of 41.8° , as it only provides 25.2° of phase lead shown in Fig. H.2. The poles and zeros are, therefore, manually adjusted to provide a phase lead of 41.8° . The lead network is now

$$G_c(s) = \frac{s + 0.0150}{s + 0.0029} \quad (\text{H.5})$$

as shown in Fig. H.3.

The over all SSSC compensated transmission system with appropriate lead compensator in the supplementary damping controller is now presented in Fig. H.4.

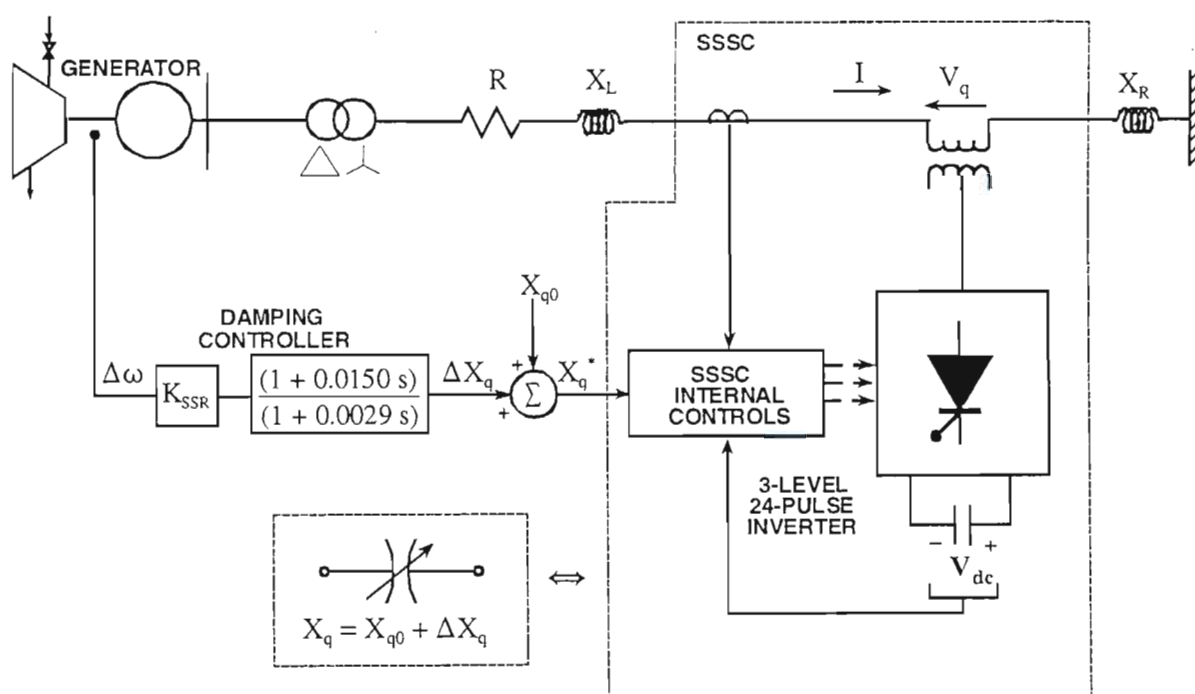


Fig.H.4: Three-level SSSC with supplementary controls in the IEEE First Benchmark Model transmission system to damp out Mode 4 frequency.

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